DESIGN AND IMPLEMENTATION OF NEUROMORPHIC SYSTEM FOR DESIGNING OF INTELLIGENT SYSTEM

DISSERTATION II

Submitted in partial fulfillment of the
Requirement for the award of the
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MASTER OF TECHNOLOGY
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MAY 2017

DECLARATION

I, Anirudha Singha, student of Master of technology under Department of ELECTRONICS AND COMMUNICATION ENGINEERING of Lovely Professional University, Punjab, hereby declare that all the information furnished in this Dissertation-II report is based on my own intensive research and is genuine.

The Dissertation-II, to the best of my knowledge, does not contain any part of my work which has been submitted for the award of my degree without proper citation.

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CERTIFICATE

This is to certify that I Anirudha Singha, bearing Registration no: 11502222 has completed objective formulation of thesis titled, **"Design and implementation of neuromorphic system for designing of intelligent system"** under my guidance and supervision for the partial fulfilment of the degree of MASTER OF TECHNOLOGY in Electronics and Communication Engineering during the academic section August 2016- May 2017 at Lovely Professional University-Phagwara
.

To the best of my knowledge, the present work is the result of his original investigation and study. No part of the thesis has ever been submitted for any other degree at any University.

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ABSTRACT

A simple CMOS circuitry using very less number of MOSFETs reproduce most of the electrophysiological cortical neuron types and is capable of producing a variety of different behaviours with diversity similar to that of real biological neuron cell. The firing pattern of basic cell classes like regular spiking (RS), chattering (CH), intrinsic bursting (IB), fast spiking (FS) and low threshold spiking (LTS) are obtained with a simple adjustment of two input voltages and input current make circuit suitable for applications in reconfigurable neuromorphic devices that implement biologically resemble circuit of cortex. This discusses spice simulation of the various spiking pattern ability with required and firing frequency of a given cell type. The circuit operation is verified for both conditions constant input and pulsating input. It represents a novel analogue VLSI circuitry that reproduces spiking and bursting firing patterns of cortical neurons, using only 19 transistors. The circuit provides a basic building block for the development of neuromorphic architectures. It enables implementation of many neurons in a single silicon chip while exhibiting flexibility in obtaining different types of adaptive and oscillatory neuron behaviours, by simply adjusting the biasing voltage. The simulation results, using a 180nm CMOS technology, are presented.

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CHAPTER 1 INTRODUCTION

1.1 HISTORICAL OVERVIEW

While the historical backdrop of actualizing electronic molds of neuro circuits reaches out return to the development of retinas (Rosenblatt, 1958) and perceptrons (Fukushima et al., 1970), the cutting edge forming of research using VLSI innovation and underlining the current which is non- linear and the transistor started with flow qualities in the mid 1980s with the cooperation that collaborated among noticeable researchers Carver Mead , Max, Richard Feynman, John Hopfield, and Delbrück (Hey, 1999). Propelled by evaluated synaptic dispatching in the retina, Mead looked to utilize the transistors for analog properties, as opposed to just working them as digitized switches which work as on–off. The way he demonstrated so that simple neuromorphic circuits (Mead, 1989) impart numerous normal physical belongings to protein diverts in neurons. As an outcome, these sorts of circuits require far less transistors than computerized ways to deal with imitating neural frameworks. It has been contended that neuromorphic circuits are perfect for building up another era of figuring advancements that utilization the same arranging standards of the natural sensory system (Sarpeshkar, 2006; Boahen, 2005; Douglas et al., 1995). In expansion to the calculations of a solitary neuron, numerous neuromorphic circuits likewise use spiking portrayals for correspondence, learning and memory, and calculation. The usage of unique spike-or mechanized event based depictions in electronic structures can be imperativeness powerful and accuse tolerant, making them ideal for building specific systems and making complex leadership hierarchies of count.

The best neuromorphic frameworks to date have been single chip gadgets that copy fringe tactile transduction, for example, silicon retinas, visual movement sensors, and silicon cochleas for a wide assortment of utilizations. The technique used to transmit spikes crosswise over chip limits in these frameworks depends on (AER; Mahowald, 1994) the address-occasion portrayal.

1.2 BIOLOGICAL NEURON MODEL

Natural networks for neural systems are motivated by our human main sensory block. The human cerebrum has around 1015 synapses and 1012 neurons. A neuron comprises of a soma (cell body), axons (send signs), and dendrites (gets signs). Any neural connection associates dendrite to an axon. To give a signal, a neural connection may build (energize) or diminish (repress) electrical voltage potential. After generation of the electrical potential, neuron fires to a breaking point. Learning may happen in light of changes in the neural association.

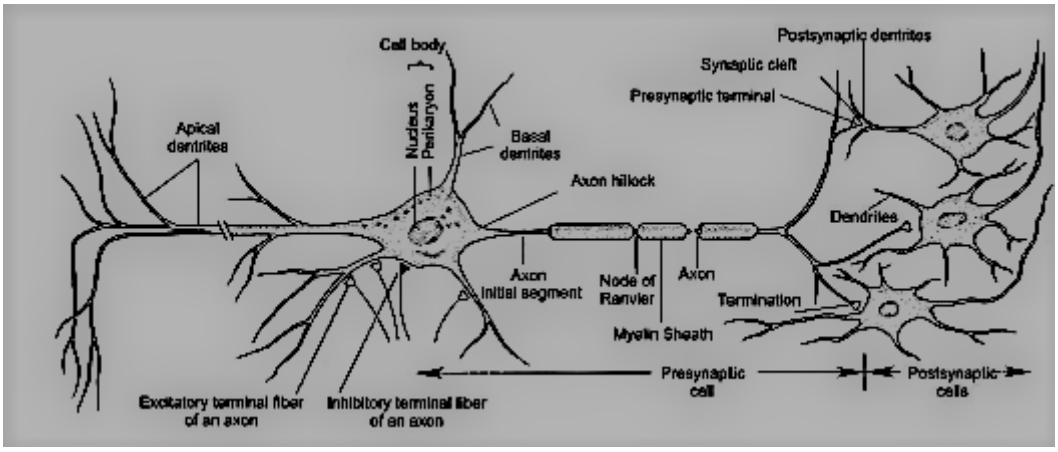

Fig.1.1 Biological Neuron Model [33]

Above figure indicates natural neuron and the fundamental four sections are highlighted which are dendrites, soma, neurotransmitter, and axon. For left neurotransmitter, the axon is from the Presynaptic neuron and the postsynaptic neuron is also a neuron model, so presynaptic form is a neuron and dendrite is a postsynaptic neuron form through adopted form.

1.2.1 Soma

The cell body, or soma, is the focal piece of the neuron. There are a wide range of specific sorts of neurons, and their sizes differ in measurement. It contains the core of the cell (the storage facility of hereditary data), and along these lines is the place most protein amalgamation happens. Generally, the soma is the "central processing unit" that plays out a vital nonlinear preparing step: if the aggregate information surpasses a specific threshold voltage, at that point a output signal is produced.

1.2.2 Dendrites

Dendrites are the extended projections of a neuron that demonstration to lead the electrochemical incitement got from other neural cells to the cell body, or soma, of the neuron from which the dendrites extend, assume the part of the "information device". Figuratively, this general shape and structure is assigned to as a dendritic tree. This is the place the greater part of contribution to the neuron happens. Electrical simulated is transmitted onto dendrites by upstream neurons by meaning of neurotransmitters which are placed at several focuses all over the dendritic arbor. Dentrites and soma constitute the real piece of the information periphery of the neuron.

1.2.3 Axon

The axon, which assumes the part of the "yield device", is a prolonged fiber that stretches out to the terminal endings from the cell body and it transmits the neural flag. The transmitting component of neurons can change extraordinarily long; most axons in the central sensory system are thin (in the vicinity of 0.2 and 20 micrometers in breadth) analyzed with the width of the cell body (50 micrometers or more). Numerous axons are protected by a greasy sheath of myelin that is hindered at regular intervals by the hubs of Ranvier.Nodes of Ranvier are tightening influences in the myelin sheath that encompass the axons of the nerve cells, or

neurons. They happen at roughly one millimeter interims along the length of the axon. The activity potential, the cell's leading signal, is started either at the axon hillock, the underlying fragment of the axon, or sometimes marginally more distant down the axon at the primary hub of Ranvier [Kandel et al., 2000].

1.2.4 Synapses

The region between two neurons is known as a synapses. Branches of the axon of one neuron (the presynaptic neuron) transmit signs to another neuron (the postsynaptic neuron) at a site called the neurotransmitter. The branches of a solitary axon may frame neural connections with upwards of 10.000 different neurons. While the axon is the yield component of the neuron, the dendrites are the info components of the neuron. Together with the cell body, they received synaptic contacts from different neurons. Neurons can be coupled by substance and electrical neurotransmitters. Neurons impart by compound and electrical neurotransmitters in a procedure known as synaptic transmission.

1.3.5 Plasma membrane

Like every single creature cell, a plasma membrane encompasses a cell neuron, a bilayer of lipid particles with lot sorts of protein forms installed in it. A lipid bilayer is an effective electrical cover, however in neurons, a significant number of the protein structures inserted in the film are electrically dynamic. These incorporate ion channels that allow electrically charged particles to stream over the layer, and particle pumps that effectively transport particles from one side of the membrane to the next (Figure 1.2). Inside the cell, the convergence of particles is not the same as that in the encompassing fluid. The charge partition offers ascend to a distinction of electrical potential over the membrane called the membrane potential.

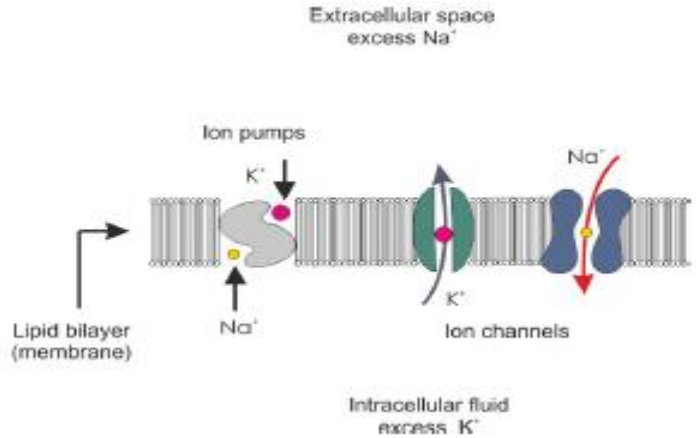

Fig.1.2 Plasma membrane operation [33]

In an organic layer, the inversion capability of a particle is the film potential at which there is no net stream of that specific particle from one side of the membrane to the next. The inversion potential is frequently called the "Nernst potential" as it can be computed from the Nernst condition [Feiner and McEvoy, 1994]. In a single ion system, the inversion potential is synonymous with balance potential. Balance alludes to the way that the net particle flux at a specific voltage is zero. At the end of the day, the outward and internal rates of particle

development are the same; the particle flux is in balance. The connection between the expressions "reverse potential" and "equilibrium potential" just remains constant for single-ion frameworks. In multi-ion frameworks, there are zones of the cell layer where the summed streams of the different particles will break even with zero. While this is an inversion potential as in the layer current inverts bearing, it is not a balance potential on the grounds that not the greater part of the particles are in harmony and consequently have net fluxes over the membrane.

1.3 ACTION POTENTIAL

Neurons simultaneously accumulates contributions from different neurons up and down their dendrites at purposes of contact called neurotransmitters. As already specified, these sources of info appear as little electrical aggravations that are alluded to as post synaptic possibilities. Close axon hillock, the particle directs exists in significantly high thickness, these are profoundly powerless to minor irritations. These particles channels consistently screen the cell body potential with the end goal that at the point when the cell potential surpasses a limit around 40mv, the neuron triggers an activity potential appeared in Fig.1.3 that that is passed down to axon towards a synaptic terminal i.e. the cells "tune in" to the neuron. As said above, at the axon hillock, electrically particular gated sodium and potassium channels are found. Electrically gated implies, the proteins that manage these channels are touchy to deviations in the film potential shape its resting estimation of - 65mv. Presently the length of the cell is hyperpolarized or depolarized nothing unordinary happens. However , when the depolarization is adequately sufficiently extensive to drive the layer potential above - 40mv, the particular ionic channels open up, allowing the free section of particular particles all through the axon.

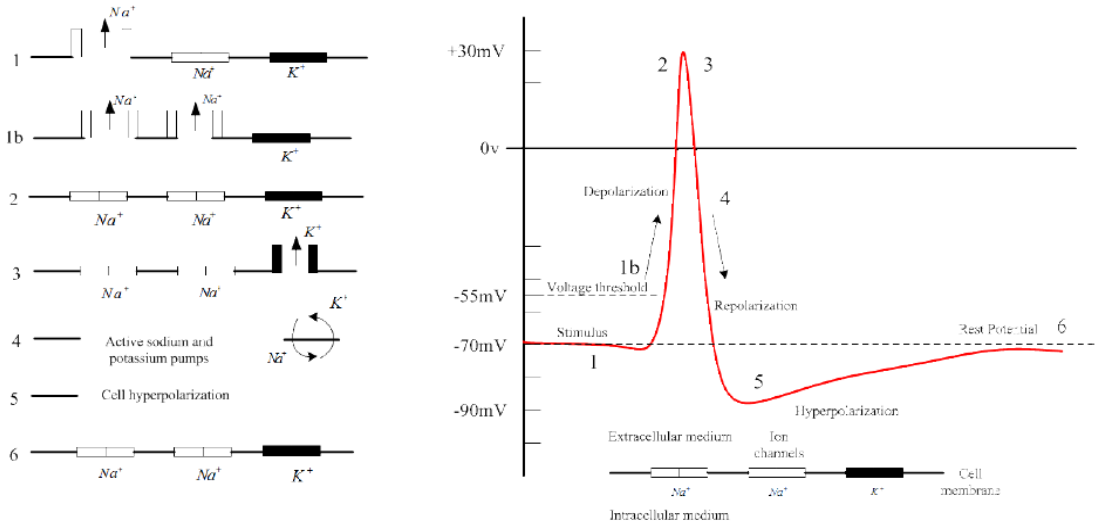

Fig.1.3 Action Potential and ion channel[34]

Neurons have a dynamic conduct; they pass on heartbeats to different cells. This was watched before measuring the electrical movement of the squid big axon. Hodgkin and Huxley showed tentatively the flow of action potential proliferated along nerve cells. The accompanying occasions portray the era of activity possibilities in sensitive cells.

1.4 ARTIFICIAL NEURON MODEL

Neuromorphic engineers have proposed an assortment of critical thinking strategies which are both human and nature enlivened like Genetic Algorithm and Artificial Neural Network. These have brought about three distinct eras of neural systems in light of three unique sorts of neurons. The First designed was proposed by Pitts and McCulloch (1943). Those were made out of neurons which depend on threshold otherwise called two sample units. That was the most basic neuron display. At the point when the addition of the considerable number of contributions to any neuron is bigger than a predefined limit, neuron fires, which is called as a Pulse, is utilized to speak to a binary state. This sort of neuron can performs essential Boolean expression however for computational issues this model was totally unreasonable. After the new model came, then the model (second era) which was more practical than the original as it uses the consistent yield work as opposed to binary stage. The initial two era models were worried about the rate of conveying data and were free of information and yield timings. These yield timings and information were critical to be considered as they were in charge of acknowledgment and the learning. This inlet and outlet connection brings timing without hesitation which makes a move model of neurons known as spiking neurons. The third era of the artificial neural system called SNN. The SNN are made out of spiking neurons and neurotransmitters. The spike conveys data to different neurons and neurotransmitters in the system. These spikes are only activity possibilities. Propagating these spikes convey data and this data is moved in the SNN.

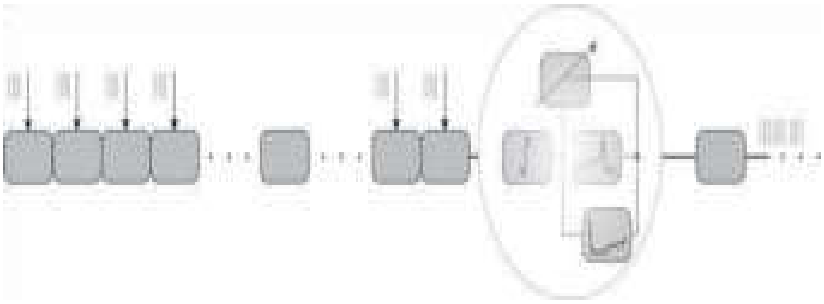

Fig.1.4 Artificial Neuron Model [33]

From a practical perspective, a artificial neuron comprises of at least one than one neurotransmitter pieces which are said to be in charge of accepting signals(spikes) from different neurons and coordinating every one of the signs all together after some time and changing over them into current of output signal as appeared in fig.3. There is another major section known as a soma piece, in charge of the spatiotemporal combination of the info signals and furthermore, it creates the output simple analog action possibilities or potentially digitized spike occasions. Also, to both these neurotransmitter and soma obstructs, there are units which display the neuron's structure(spatial) and execute the flag handling that happens in dendritic trees and axons, individually.

Table 1.1. The comparison of biological and artificial neural network

BNN	ANN
Soma	Unit
Axon & Dendrite	Inter-Connection
Neuro-transmitter	Updated Weight
Potentiation	Weighted Sum
Threshold	Biasing Weight

Neurons which is spiking as the name suggests are the neuron. The neuron is utilized a spike (electric heartbeat) to exchange data. Silicon made neural system is comprised of spiked neurons and neurotransmitters. The unique connection is made on the premise of data coding in the types of rate, timing and mixture of both by the methods for which neurons convey to each of them. Alongside spiking neurons, neurotransmitters are a standout amongst the most essential building hinders in SNN. These neurotransmitters are only the association between two neurons. Through this neurotransmitter or change in weight (ANN), exchange of data happens insight the neural system.

1.5 NEURON MODELS

Neurons have been actualized in silicon utilizing taking all models. These are the spike based neuron models:

1.5.1 Integration and Fire Neuron Model (I&F) :

The leaky integrate and fire neuron models is used most frequently in neuromorphic. The equation is given by

$V_{mem} = I + a - bV_m$, …….. (1.1)

If $V_{mem} >= V_{threshold}$ and V_m <-c ……..... (1.1.1)

Where V_{mem} is the membrane voltage, input current is I, a,b,c and vthreshold are parameters.
Class 1 excitable is the I&F neuron. Tonic spikes are generated with same frequency and it is act as an integrator. The iteration equation as $V_m(t+1) = V_m(t)+[I+a-bv(t)]$. Spikes has fixed threshold with no latencies.At the point when the current in defined as input which is connected. After that membrane voltage increments concerning with time (t). It achieves threshold voltage (V_{th}) and a spike is generated. It is the voltage and action potential will reset to its initial potential.

1.5.2 Integration and Fire With Adaption :

We can say I&F is a 1-Dimensional. It has same properties and burst of neurons as above model. Second linear equation is given by

$V(t+1) = V_{mem}(t) + [I + a - V_{mem}(t)]$ ……..... (1.2)

$V_{mem} = I + a - bV_{mem} + f(d-V_{mem})$ ……..… (1.2.1)

And $f' = e[\delta(t)-f]$ ……..…. (1.2.2)

It activates K current, has high threshold value and it is dynamic in nature.

1.5.3 Integration and Fire or Burst:

The modification equation is written as-

$V_{mem} = I + a - bV_{mem} + fH(V_{mem}-V_{threshold})\ h(V_{mem}T - V_{mem})$ …..…. (1.3)

If $V_{mem}= V_{threshold}$, then $V_{mem} > V_{threshold}$ …….. (1.3.1)

$h^{'} = -h/\Gamma$, if $V_{mem} > V_{threshold}$ …….. (1.3.2)

$= (1-H/\Gamma^{+})$, if $V_{mem}< V_{threshold}$ …… (1.3.3)

1.5.4 Quadratic Integration and Fire :

The defective I&F neuron is otherwise called Quadratic I&F neuron.The condition is known as

$V_m = I + a(V_{mem}-V_{reset}-V_{threshold})$ if $V_{mem}= V_{peak}$, then$V_{mem} <– V_{reset}$ …… (1.4)

It comes under any class 1 excitable system. 1ms time taken for seven operation and it uses in large scale networks.

1.5.5 Resonate and Fire Neuron Model :

The R&F is portrayed as 2-Dimensional simple of the Integrate-and-fire neuron. This condition is described as –

$R^{'} = I + (b + w)R$ …….. (1.5)

Where $I_{mem}=V_{threshold}$, then $R <- R_0(R)$. ……. (1.5.1)

Z is a membrane voltage potential. Parameters are b, w and $V_{threshold}$ and an arbitrary function is Ro=(R).

1.5.6 Hodgkin and Huxley Neuron Model :

In 1952, the neuron model is created by A.L. Huxley and A.L. Hodgkin. The probed squid axon and created popular neuron demonstrate. The neuron display clarifies development of sodium and potassium streams with sodium and potassium conductance. This is first spike based model and imitates the ion channel of the neuron. The aggregate membrane current is given as

$V= I_1 V_2- I_2 V- I_3 U_2+ I_4 U+ I_5,$ ……. (1.6)

when $V>= u- V_{threshold}$

$= m_1V_2-m_2V-m_3UV+ m_4$, otherwise ……. (1.6.1)

$U= k_1V_2- k_2V- k_3U_2+ k_4U + k_5$ …… (1.6.2)

if $V>V_{threshold}$, Ii and ki are constant on parametrs.

1.5.7 Fitzhugh-Nagumo Neuron Model

The neuron circuit is created by Richard Fitzhugh in 1961, after that Naymo made a neuron model circuit. It depicts the model of volatile framework. That model is oscillatory in which as outside connected current surpasses limit an attributes change in stage space is happened. Thusly spikes are created in neuron. The dynamic conditions are given by

$V_{mem} = a+bV_{mem}^2+c\ V_{mem}^2+d\ V_{mem}^2- 4$ …….. (1.7)

$U^{'} = €(e\ V_{mem} - U)$ …… (1.7.1)

The model has Bonhoeffer-vander pol oscillator have exceptional situations where a=b=0. Tentatively decided variales are set by a=-0.7, b=0.80

1.5.8 Morris-Lecar Neuron Model

The model produced by Harold Lecar and Catherine Mooris in 1981. The scientists intimate oscillatory conduct within potassium conductance and goliath barnacle music fiber. The model displays class 1 and class 2 sesitivity. Hodgkin and Huxley and Fitzhugh-Nagumo both are joined and it display through calcium channel voltage gated with deferred rectified channel of potassium. The conditions are set to

$CV_{mem}= I - gL(V-V_L) - g_{ca}\ m_\infty(V_{mem})*(V_{mem}-V_{ca}) - gk\ n(V_{mem}-V_k)$ ……..... (1.8)

where

$n= \lambda\ (v)\ [n_\infty(v) – n]$ ……..... (1.8.1)

$m_\infty(v) = 1/2\{1+\tanh[(V_{mem}-V_{mem1})/V_{mem\ 2}]\}$ ……. (1.8.2)

$n_\infty(v) = 1/2\{1+\tanh[(V_{mem}-V_{mem3})/V_{mem4}]\}$ ……..… (1.8.3)

$\lambda_\infty(v) = 1/2\ \lambda\cosh[(V_{mem}-V_{mem3})/2V_{mem4}]\}$ ……. (1.8.4)

1.5.9 Hindmarsh-Rose Neuron model

In the year 1984, Hindmarsh and Rose produced this model to concentrate the spike blasting conduct of the layer potential voltage in the neuron. This is additionally oscillatory neuron show. Here the spiking variable y(t), which measures the vehicle of the particles by quick ion channels and the brusting variable z(t), which measures the conduction of the particles by moderate ion channels. The non-direct differential conditions depicting those dynamic factors are set to be:

$V_{mem}= U - f(V_{mem})+ I – W$ …….. (1.9)

$U^{'} = g(V_{mem}) – U$…….. (1.9.1)

$W^{'} = [H(v)-w] / T$ …… (1.9.2)

1.5.10 Wilson Polynomial Neuron Model

This model uses in polynomial equations. From differential equation is consisted here. We have to select parameters very carefully. To simulate 180 operations, it takes 0.25ms. Here we are not describing the model equations.

1.5.11 Izhikevich Neuron Model

In 2003, the circuit model was designed by Izhikevich. That is a basic circuit clarified by two state factors through two sample non-direct differential conditions. IZ model wass decreased model of Hodgkin and Huxley neuron display utilizing bifurcation investigation. Two complex conditions that are clarify the neuron is set to :

$Cdv/dt= k(V_{mem} -V_r)(V_{mem} -V_t) – U- I(1)$ …… (1.10)

$du/dt= a(b\ V_{mem} - V_r) – U$ ……. (1.10.1)

where $V_{mem}= C$ and $U= U+d$ ……..… (1.10.2)

a,b,c,d are variables, V_r is reset potential, I is applied step input current.

1.6 CORTICAL NEURON MODEL

1.6.1 BIOLOGICAL CORTICAL NEURON MODEL

The neocortex is that piece of the cerebrum which makes up the external 2 to 4 mm of the cerebral halves of the globe. It is the 'dim matter' of the cerebrum lying on the cerebral 'white matter' made out of myelinated axons that interconnect diverse locales of the mind. All the more elevated amount psycho-physical capacities tangible recognition, question and occasion portrayal, arranging, and basic leadership are accepted to take as their natural substrate the exercises of interconnected and dispersed systems of neurons in the neocortex. Despite the fact that it is very thin, the cortex structure is profoundly collapsed with many depressions (called 'sulci'). This collapsed plan takes into consideration a far more prominent volume of cortical matter to be contained inside a given estimated cerebrum cavity than would be conceivable if the cortex were laid out in a "sheet" specifically underneath the skull. The sulci give advantageous "points of interest" for helping anatomists to arrange diverse areas of the cerebral cortex. All tangible data achieving the neocortex is passed on through a sub-cortical (beneath the cortex) structure called the thalamus. Different signs, thought to be principally "control" flags that balance cortical action, likewise come into the neocortex from around 20 sub-cortical locales of the mind. It sends some of these signs to the cerebrum stem or straightforwardly to the spinal rope, and others in a round about way by method for the cerebellum. Diverse areas of the neocortex seem, by all accounts, to be specific to take an interest in particular sorts of psycho-physical capacities, e.g. the visual cortex, the sound-related cortex, the essential engine cortex, the dialect region, and so forth. In any case, it must be completely valued that no single territory of the cerebrum has been effectively distinguished as the sole utilitarian region of any psycho-physical marvel. Or maybe, the mind seems to have an exceptionally disseminated

usefulness with a wide range of regions of the cerebrum (both cortical and non-cortical) making critical commitments to each such capacity.

1.6.2 ARTIFICAL CORTICAL NEURON MODEL

The neocortex is that piece of the cerebrum which makes up the external 2 to 4 mm of the cerebral halves of the brain. It is the "gray matter" of the cerebrum lying on the cerebral "white matter' made out of myelinated axons that interconnect diverse areas of the mind. All the more elevated amount psychophysical capacities tangible discernment, question and occasion portrayal, arranging and basic leadership are accepted to take as their organic substrate the exercises of interconnected and disseminated systems of neurons in the neocortex. The cortex structure is thin and very collapsed with many scores. All tangible data achieving the neocortex is passed on through a sub-cortical (underneath the cortex) structure called the thalamus. Different signals, thought to be basically "control" signals that modulate cortical movement, additionally come into the neocortex from roughly 20 sub-cortical areas of the mind. Distinctive locales of the neocortex give off an impression of being particular to participate in particular sort of psychophysical capacities. No single range of the cerebrum has been effectively distinguished as the sole practical region of any psycho-physical wonder.

Neuron cells are major basic component of the cortical microcircuits. Trying to copy it is operation in silicon circuots is a research interest now a days. Efficient emulation engine is provided by analog VLSI model. This help to lead the electronic devices to copy the operation of biological brain. Researches will go to make more realistic model of human brain. Researchers are trying to characterizing what nervous system do, obtaining how they functions.

To design certain model is required area and power consumption with least number of transistor, adopted the VLSI networks that assembles of many thousands of neurons.

Developing interest approaches towards the spike-based neural system as they seems to give promising answer for an assortment of complex issues which can not be fathomed by most capable PCs. This paper concentrates on the diverse spiking and terminating examples of the cortical neuron. Commonly utilized I&F (Integrate &Fire) cells devour around 20 transistors to actualize low power versatile neuron hardware. This is not fit for copying the preparing of human sensory system, as around 90% of the cortex is made of nonlinear oscillatory neuron as opposed to basic spiking neurons. Thusly work concentrates on the use of the base number of transistors giving diverse sorts of terminating examples getting distinctive sorts of versatile and oscillatory neuron practices in a solitary chip.

The component of natural neural system are ascribed to it is structure and capacity. Essential unit of the system is known as a neuron or a nerve cell. It comprises of a cell body or soma where the cell core is found. Tree like nerve filaments called dendrites are related with the cell body. These dendrites gets signals from different neurons. Reaching out from the cell body is a solitary long fiber called the axon, which branches into strands and sub strands interfacing with numerous other neuron at the synaptic intersections or neurotransmitters.

For the most part the electrical action is restricted to the inside of a neuron, while the compound system works at the neurotransmitters. The dendrites fill in as receptors for signs from different

neurons, while the motivation behind an axon is transmission of the created neural movement to other nerve cell or to muscle fiber.

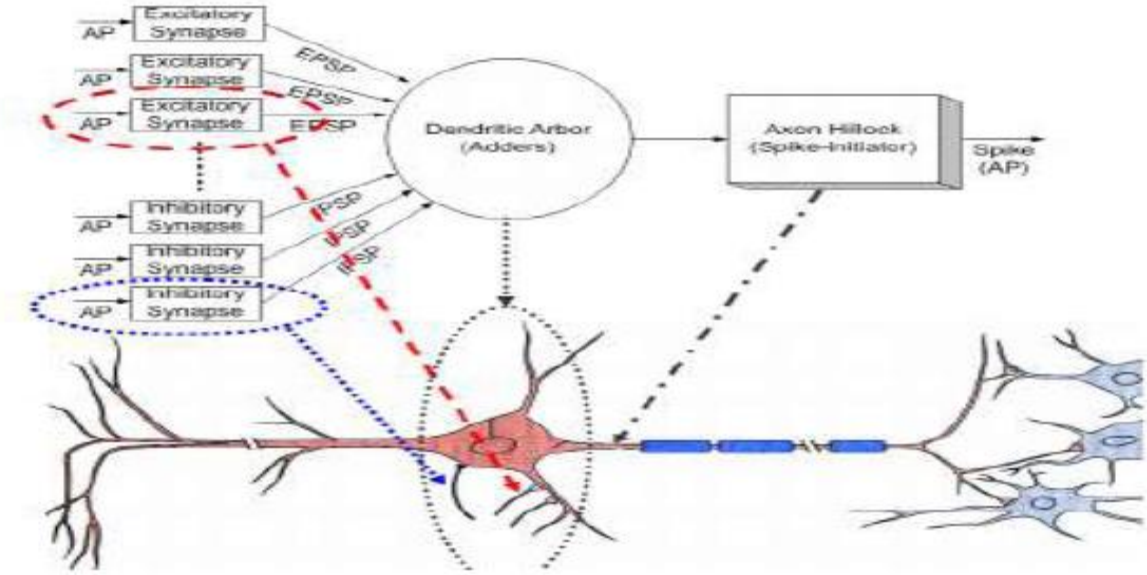

Fig.1.5 Comparing BNN and ANN Model [34]

Artificial neural system (ANN) is an exceedingly streamlined model of the structure of the natural neural system. ANN comprises of interconnected preparing units. The general model of a preparing unit comprise of summing part took after by yield part. The summing part gets u1,u2 - un input values(w1,w2 - wn) and figures a weighted entirety. The weighted entirety is known as the enactment esteem. The yield part delivers a flag from actuation esteem. The indication of the weight for each information decides if the info is excitatory(positive weight) or inhibitory(negative weight). The information could be discrete or consistent information values, and in like manner the output likewise be deterministic or stochastic or fuzzy. In a artificial neural system a few preparing units are interconnected by some topology to fulfill an example acknowledgment assignment. Subsequently the contribution to a preparing unit may originate from the yield of other handling units, as well as from outside sources. The yield of every units might be given to a few units including itself. The measure of the yield of one unit got by 8 another unit relies on upon the quality of the association between the units and it is reflected in the weight esteem related with the interfacing joins. In the event that there are n enactment estimation of the system characterizes the actuation condition of the system right then and there.

CHAPTER 2 SCOPE OF THE STUDY

The scope of study is very vast in neuromorphic part of the VLSI domain. Neuromorphic systems describe robust and efficient neural computation using software and hardware implementations that simulate in physical time. These come under event driven or data driven systems. It consists of low power, parallel hybrid analog or digital VLSI circuits. These circuits are using the same physics of computation implemented by the neuron system.

We concentrate about cortical neuron VLSI circuit which generates several spiking depending on the respective parameters. These spikes are very much similar to our human neuron signal spiking. Body information signal transmits through neurons via spiking signal. Signal should be exceed the threshold value of the circuit to operate the working principle transmit spiking signal through neurons. This action same as our analog electronic circuit does, Signal must be crossed the threshold value of that particular circuit to transmit the signal or information. The generation of spike is depending on values of (W/L) ratios, supply voltage, threshold voltage and modulated bias voltage.

Here we are concentrate to generate several types of spikes as a information signal. Types of spiking describes as chattering, intrinsic bursting, fast spiking, regular spiking and low threshold spiking. The interest is growing very fast in spike-based neural networks. It is inspired by neuro-biology domain. Here we can easily compute solutions for complex of problems. Although some of the circuits have beyond the capability of most powerful computers.

CHAPTER 3 OBJECTIVES OF STUDY

Izhikevich model is a new neuron model that is used widely. Hodgkin and Huxley model is a previous model of Izhikevich model. This model is very simple and consist two state variables U and V_{mem} to narrate the dynamics of the neuron.

$Cdv/dt= k(V_{mem} -V_r)(V_{mem} -V_t) – U- I(1)$ …….. (3)

$du/dt= a(b V_{mem} - V_r) – U$ ……... (3.1)

where $V_{mem}= C$ and $U= U+d$ …… (3.2)

a,b,c,d are variables, V_r is reset potential, I is applied step input current.

Biological neuron is less faster than biological neuron. It is 10^5 times faster than the biological neuron. The circuit is efficient to generate linear and non linear resposes.

Here we are concentrating to generate output spiking patterns. These are as follows :

- Chattering
- Intrinsic bursting
- Fast spiking
- Regular spiking
- Low threshold spiking

Steps :

1. To design membrane circuit to generate membrane voltage potentials.
2. To increase the leakage current of the membrane potential slow variable circuit is used and goes down depolarization after the spike. It gives the accommodation property of spiking.
3. Comparator circuit is used to provide needed amplitude and duration of the step input pulses.

CHAPTER 4 LITERATURE REVIEW

4.1. Giacomo Indiveri (2001) :

In this paper we show a neuromorphic equipment model of a particular consideration system actualized on an VLSI chip, utilizing simple circuits. The chip makes utilization of a spike-based portrayal for getting input signals, transmitting yield signals and for moving the choice of the went to information boost after some time. It can be interfaced to neuromorphic sensors and actuators, for executing multichip particular consideration frameworks. In circuit the AER correspondence convention enables the chip to trade information while handling signals in parallel, continuously. In this convention input and output signal are transmitted as offbeat binary information streams which convey the simple data in their transient structure. Every occasion is spoken to by a parallel word encoding the address of the sending hub. The address of the sending component is passed on in parallel alongside two handshaking control signals. Frameworks containing more than two AER chips can be developed actualizing extra unique reason off-chip discretion plans. In a framework containing AER sensors interfaced to the specific consideration chip, address occasions would reach, at the info phase of every cell of the 8 exhibit, excitatory synaptic (integrator) circuits that change over the advanced voltage beat streams into simple analog input current flows. The yield current of each WTA cell is utilized to actuate both a integrate and fire (I&F) neuron and two position to voltage circuits. This test exhibited how the chip's predisposition parameters can be utilized to force diverse practices of the framework and proposed conceivable applications.

4.2. Giacomo Indveri (2003) :

A simple low power circuit is used for actualizing cracked incorporate and firing neuron model is to be exhibited. The circuit which is proposed incorporates components for executing spiking recurrence adjustment, for setting a self-assertive headstrong time and expends low power and balancing the neuron's edge voltage. Circuit which is I&F ordinarily coordinate little streams upon a capacitor until a limit is come to. As the voltage on the capacitor surpasses the limit a quick spike is produced and the capacitor is reset. In the circuit outlined a source adherent for augmenting the direct incorporation run and for tweak the neuron's edge voltage is utilized, an inverter with positive criticism for diminishing the exchanging short out streams at the info, an inverter with controllable slew-rate for setting discretionary unmanageable periods, an advanced inverter for producing the beats that flags the event of a spike, a transient current-reflect integrator for actualizing the spike –frequency adjustment instrument, furthermore, a base size transistor for actualizing a consistent hole. Absolutely this neuron comprises of 20 transistors and a capacitor. The circuit is actualized in 1.5um standard CMOS innovation handle.

4.3. Izhikevich (2003) :

He proposed a new neuron model that is suitable for generating bursting and spiking characteristics of the neuron. This model provides computational efficiency like integrate and fire model as well as produces dynamics exactly same as conductance based neuron model which are usually implemented using Hodgkin and Huxley model. This model was proposed in

2003 and still numerous neuroscientists are utilizing this model with a specific end goal to imitate the electrophysiological properties of the neuron. In this paper reenactment done in MATLAB.

4.4. Richard B. Wells (2005) :

This paper is an instructional exercise audit of the structure, organization, and factual demonstrating of the association of the neocortex. It starts with a general review of the layered structure of the neocortex and its association as a system of interconnected utilitarian segments. Next it talks about the different classes of neurons that populate the neocortex utilizing as an arrangement framework the few bland sorts of signs created by cortical neurons. This is trailed by an examination of qualities in neuron-to-neuron flagging. At long last, it surveys a portion of the general patterns found in the cortical association. This paper has exhibited an instructional exercise diagram of the neocortex. Our perspective has been that of portrayal of the flag handling pathways exhibit in neocortex, and of the flagging qualities of the neurons which make it up. Extra and more itemized data can be acquired from the references and from their references.

4.5. John Koestar and Steven A. Siegelbaum :

In this paper, they represent many types of membrane voltage potential discussion. We can generate membrane potential using neuron models. Almost all neuron models are generating membrane potential. It is a main source to generate output spiking pattern. Action potential takes major part to generate membrane potential. Na^+ and K ions are taken part of these operation. In biological neurons, it is a main source to activate action potential to transmit the information respective neuron circuitry. It helps the respective neuron circuit to reset or set the operation.

4.6. Thomas J. Koickal and Alister Hamilton (2007) :

In this paper an on-chip versatile spike timing based balance cancelation plot for neuromorphic detecting gadgets is exhibited. A spike-time subordinate learning calculation suited to simple VLSI usage is produced for weight adaption. A simple VLSI circuit usage of the balance cancelation plan is exhibited. Circuit recreations are performed utilizing balanced details drawn from a neuromorphic olfaction sensor to show the viability of the plan. A versatile counterbalance cancelation chip manufactured in simple VLSI utilizing 0.35 μm CMOS innovation is at present under test. In a neuromorphic detecting gadget, the non-idealities at the detecting hardware show as spike timing mistakes at 13 neuronal output. The sensor particulars are drawn from a formerly actualized neuromorphic olfactory concoction sensors. The sensor is demonstrated with a counterbalanced voltage of 300 mV. The reference spike day and age for zero balance conditions is 10 ms. Subsequently the time window period for every dynamic period of the spike time subordinate learning capacity Twin/2 is intended to be 4.8 ms. The underlying weights of the adaption circuit are set haphazardly. Before taking in, the underlying planning blunder because of the sensor balance voltage was 1.75 ms. At first tactile neuron spikes touch base out of stage with zero balance reference spikes and the underlying planning blunder because of the sensor counterbalance voltage was 1.75 ms. As learning advances, result demonstrates that normal spike timing mistake logically diminishes and the tangible neuron

spikes begin to bolt on to the zero counterbalance reference spikes. The normal last spike timing blunder at adaption time of 500 ms is lessened to 10 μs in this way exhibiting the adequacy of the counterbalance cancelation plot actualized here.

4.7. A. Jimeneze-Fernandez (2008), et al. :

This paper displays a few approaches to make an interpretation of AER spikes into DC engine control, and to control a DC engine speed, in light of Pulse Frequency Modulation. Address-Event Portrayal (AER) is a neuromorphic correspondence convention for exchanging data of spiking neurons actualized into VLSI chips. These neuro-motivated executions have been utilized to plan sensor chips (retina, cochleas), preparing chips (convolutions, channels) and learning chips, what makes conceivable the advancement of complex, multilayer, multichip neuromorphic frameworks. In that paper they indicated two unique procedures to actualize a spike-based shut circle control framework. Late work is engaged in coordinate an AER retina, with an ongoing AER-based protest identification framework, in a mechanical stage controlled by the uncovered control methods.

4.8. Giacomo Indiveri, Sadique Sheik (2011), et al. :

To execute complex occasion based neuromorphic frameworks it is important to interface the neuromorphic VLSI sensors and gadgets among each other, to mechanical stages, and to workstations. This obviously straightforward objective requires meticulous work that traverses different levels of many-sided quality and controls: from the custom format of microelectronic circuits and nonconcurrent printed circuit sheets, to the advancement of question situated classes and techniques in programming; from electrical building and material science for simple/computerized circuit configuration to neuroscience and software engineering for neural calculation and spike-based learning strategies. So they created to rearrange the arrangement of multi-chip neuromorphic VLSI frameworks, and mechanize the mapping of neural system demonstrate parameters to neuromorphic circuit predisposition values. Theye demonstrated how Python programming devices can be utilized to naturally arrange neuromorphic equipment for copying spiking neural systems. The structure is open, and particular keeping in mind the end goal to effectively incorporate an extensive variety of extra modules. These modules run from drivers (for interfacing the devices to custom VLSI chip), to programs for controlling estimation instruments(and gaining information from the equipment setups),and streamlining schedules.

4.9. Giacomo Indiveri, Cecilia Laschi (2013), et al. :

In this paper executing an occasion driven neuromorphic vestibular sensor utilizing a business Inertial Measurement Unit (IMU) and a custom simple VLSI neuromorphic chip. They research a model of the vestibular sensor that copies the spiking reactions of hair cells in the half circle waterways and align the neuromorphic chip to coordinate the parameters of a neuro logical computational model. a usage of a neuromorphic vestibular sensor utilizing a business Inertial Measurement Unit (IMU) and a custom simple VLSI neuromorphic chip. The neuron display utilized as a part of our investigation of the vestibular afferents is an adjusted cracked incorporate and-fire neuron with a dynamic edge. To gauge rakish speeds around the three tomahawks, specialists utilized an iNEMO-M1 IMU. The gadget incorporates, other than

different parts, a Micro electro mechanical 16-bit computerized yield whirligig and a 32-bit ARM microprocess. The ARM center runs a firmware written in C programming dialect, and gathered with the GNUARM instrument chain. Trial comes about approving the equipment usage and the alignment system are exhibited.

4.10. Giacomo Indiveri, Cecilia Laschi (2014), et al. :

In this work, they propose a constant equipment model of a simulated vestibular framework, executed utilizing a custom neuromorphic Very Large Scale Integration (VLSI) multi neuron chip interfaced to a business Inertial Measurement Unit. The simulated vestibular framework is acknowledged with spiking neurons that duplicate the reactions of natural hair cells introduce in the genuine half circle trenches and otholitic organs. They show the constant execution of the hybrid analog-computerized framework and describe its reaction properties, exhibiting estimations of an effective encoding of rakish speeds and also straight increasing velocities. As an application, a novel usage of a repetitive integrator arrange equipped for monitoring the current angular position. The test comes about gave approve the equipment usage by means of correlations with a detailed and computational neuroscience display. A perfect instrument for creating bio-motivated automated advancements, this work gives a premise to building up an entire low-control neuromorphic vestibular framework which coordinates the equipment model of the neural flag handling pathway depicted with custom bio-mimetic gyroscopic sensors, abusing neuromorphic standards in both mechanical and electronic angles.

4.11. Jayawan, H.B. Wijekoon, and Piotr Dudek (2006) :

This paper displays a novel simple VLSI hardware that imitates spiking and blasting terminating examples of cortical neurons, utilizing just 14 MOSFETs. The circuit gives a fundamental building square to the improvement of neuromorphic designs. It empowers usage of numerous neurons in a single silicon chip while displaying adaptability in acquiring distinctive sorts of versatile and oscillatory neuron practices, by essentially changing the biasing voltage. The reenactment comes about, utilizing a 0.35um CMOS innovation, are exhibited.

4.12. Jayawan, H.B. Wijekoon, and Piotr Dudek (2007) :

The paper exhibits a silicon neuron circuit that impersonates the conduct of known classes of natural neurons. The terminating examples of fundamental cell classes: regular spiking (RS), fast spiking (FS), chattering (CH) and intrinsic bursting (IB) are acquired with a basic change of two biasing voltages. The simulations uncover the capability of the circuit to give a wide assortment of cell practices with required settlement and terminating recurrence of a given cell sort. The neuron expends just 14 MOSFETs empowering the combination of numerous neurons in a little silicon region. Consequently, the circuit gives an establishment to planning hugely parallel simple neuromorphic systems that nearly look like the circuits of the cortex.

4.13. Jayawan, H.B. Wijekoon, and Piotr Dudek (2009) :

This paper proposes a silicon neuron circuit which utilizes a moderate variable controlled spillage term to develop the collection of spiking examples achievable in an integrate and fire model. The reproductions uncover the capability of the circuit to give a wide assortment of

neuron terminating designs saw in neocortex, including adjusting and non-adjusting, customary spiking, fast spiking, chattering, bursting, and etc. The terminating examples of essential cell classes are acquired with a straightforward change of four biasing voltages. The circuit works in the sub-threshold administration, with time constants like natural neurons, and henceforth is reasonable for use in frameworks requiring such working paces. Conceived uses of the proposed circuit are in large scale simple VLSI frameworks for spiking neural system simulations, mind motivated circuits for mechanical autonomy and mixture silicon/science frameworks.

4.14. A.D. Tete and Dr. A.Y. Deshmukh (2011) :

A straightforward CMOS hardware utilizing less number of MOSFETs repeat the greater part of the electrophysiological cortical neuron sorts and is fit for delivering an assortment of various practices with differences like that of genuine organic neuron cell. The terminating example of fundamental cell classes like normal spiking (RS), gabbing (CH), inherent blasting (IB) and quick spiking(FS) are gotten with a straightforward change of just a single biasing voltage makes circuit reasonable for applications in reconfigurable neuromorphic systems that execute naturally look like circuit of cortex. This paper talks about spice simulation of the different spiking design capacity with required and firing ranges of a given cell sort. The circuit operation is confirmed for both conditions-steady iinput and Step input current.

4.15. Ethoti Radhika, Sanjeev Kumar, Anita Kumari (2015) :

Neuron is the essential substance that transmits and process data through created activity potential or spikes in neuromorphic frameworks. In genuine situation there is no settled threshold in the cortical neuron however it differs for each neuron. In this work, the neuron with threshold modulation ability is actualized in simple VLSI utilizing CMOS innovation. The proposed neuron circuit produced time changing threshold voltage that applies to neuron enter. The circuit is equipped for producing an assortment of various spiking designs with differing qualities like that of genuine natural neuron cell. The paper depicts how threshold voltage is accomplished other than operation of the circuit. Recreation aftereffects of various examples are exhibited alongside threshold modulation to the circuit and in addition control examination for each example. The neuron circuit is proficient to be utilized as a part of microcircuits as it expends low power. Cortical neuron is the essential component of the neocortex that includes in complex procedures like insight, engine control and so on. Building cortical systems prompts advancement of keen frameworks that learns by adjusting to nature. In this work cortical silicon neuron is introduced that comprises of 19 transistors. Proposed circuit is equipped for showing the elements of genuine neuron, for example, spike recurrence adjustment, after spike resetting component alongside limit balance. The circuit displayed create a wide range of blasting, spiking pattern examples of the cortical neuron. The introduced minimal CMOS circuit is planned utilizing just 14 transistors and it gives adaptable exchanging between various cortical neuron sorts essentially, controlling the outer voltages, Vc and Vd. Aside from getting distinctive sorts of neurons, this circuit is additionally fit for giving an assortment of various behavioral cell bunches in each cortical neuron sort, with differing qualities like that of genuine organic neuron cells. The voltage-tuning empowers modifications against process variety. The stage plane examination of the circuit gives better comprehension of the spike elements that happen in the circuit which encourages the distinguishing proof of circuit parameters

specifically identified with a property of a spike or spike trains. Thus, the circuit gives straightforward, smaller and effectively configurable widespread cortical neuron for building hugely parallel simple neuromorphic systems that nearly look like the circuits of the neocortex.

4.16. Giacomo Indiveri and Stefano Fusi (2014) :

As the quantity of VLSI executions of spike based neural systems is consistently expanding, and the advancement of spike-based multi-chip frameworks is winding up noticeably more well known it is vital to configuration spike-based learning calculations and circuits, good with existing arrangements, that invest these frameworks with adjustment and order capacities. We propose a spike-based learning calculation that is very compelling in characterizing complex examples in semi-managed form, and present neuromorphic circuits that bolster its VLSI usage. We portray the engineering of a spike-based learning neural system, the simple circuits that execute the synaptic learning component, and present outcomes from a model VLSI chip containing a full system of incorporate and-fire neurons and plastic neurotransmitters. We show how the VLSI circuits proposed replicate the taking in model's properties and satisfy its essential necessities for grouping complex examples of mean terminating rates.

4.17. A. Aggarwa l a and T.K. Horiuchi (2015) :

A second-order low pass filter using log-domain technique produces synaptic current which is the main input current of proposed circuit. Synapsis neuron circuit has to be made to generate the input current. The synapsis observes the advantage over those currently common as the output current is proportional to the number of spiking. It shows delay the peak current from 0.5 to 50ms. The proposed circuit is using two low pass filter in a cascade of two current mode. The circuit is triggered by logic level digital pulse. The second order function is established the shape of the output current of that circuit. To get a proper output synapsis current they also changed the ratio of (W/L).

4.18. Gagandeep Kaur, Raghav Gupta and Jyotirmoy Pathak (2016) :

The Brain is the key some portion of any living creature. It acts as indicated by the evolving condition. The mind performs calculations in parallel as it has neurons which are electrically dynamic cells that work at the same time. Neurons are the basic piece of the artificial neural system. Neurons are in charge of the transmitting and handling data through the spikes in the neuromorphic frameworks. This paper exhibits the neuron circuit which is actualized on the premise of the neuron models that attempt to imitate the genuine neurons. The neuron circuits exhibited in this paper is executed in 0.18um innovation in rhythm virtuoso. The izhikevich neuron show based neuron circuit, can deliver the prattling conduct while the incorporate and fire neuron circuit creates the basic and consistent spiking conduct of the spiking neuron.

4.19. Thomas J. Koickal (2006), et al. :

In this paper, displayed the simple circuit outline and usage of a versatile neuromorphic olfaction chip. A simple VLSI gadget with on-chip chemo sensor exhibit, onchip sensor interface hardware and on-chip learning neuromorphic olfactory model has been manufactured in a solitary chip utilizing Austria Microsystems 0.6 ,um CMOS innovation. Drawing motivation from organic olfactory frameworks, the neuromorphic simple circuits used to

process signals from the on-chip scent sensors make utilization of worldly "spiking" signs to go about as transporters of smell data. An on-chip spike time subordinate learning circuit is coordinated to progressively adjust weights for scent discovery and arrangement. All the part subsystems executed on chip have been effectively tried in silicon.

4.20. Romain Brette and Wulfram Gerstner (2014) :

In this report, they will present a versatile exponential integrate and-fire (aEIF) demonstrate that joins the three augmentations specified above and demonstrates that every single model parameter can be deliberately removed from a progression of standard incitement ideal models. To demonstrate the attainability of the approach, the technique in this paper was connected to simulated information produced from an itemized conductance-based model of a general spiking neuron.

CHAPTER 5 RESEARCH METHODOLOGY

5.1 EXPLANATION OF SUB COMPONENTS OF THE CORTICAL NEURON CIRCUIT

To understand the main circuit implementation we should have a clear view of each and every circuit sub blocks. Initially cortical neuron circuit is divided into three blocks Such as membrane potential circuitry, slow variable circuitry and comparator circuit block. Here we discussed all sub circuit blocks individually as sequence manner follows as :

5.1.1 MEMBRANE POTENTIAL CIRCUIT

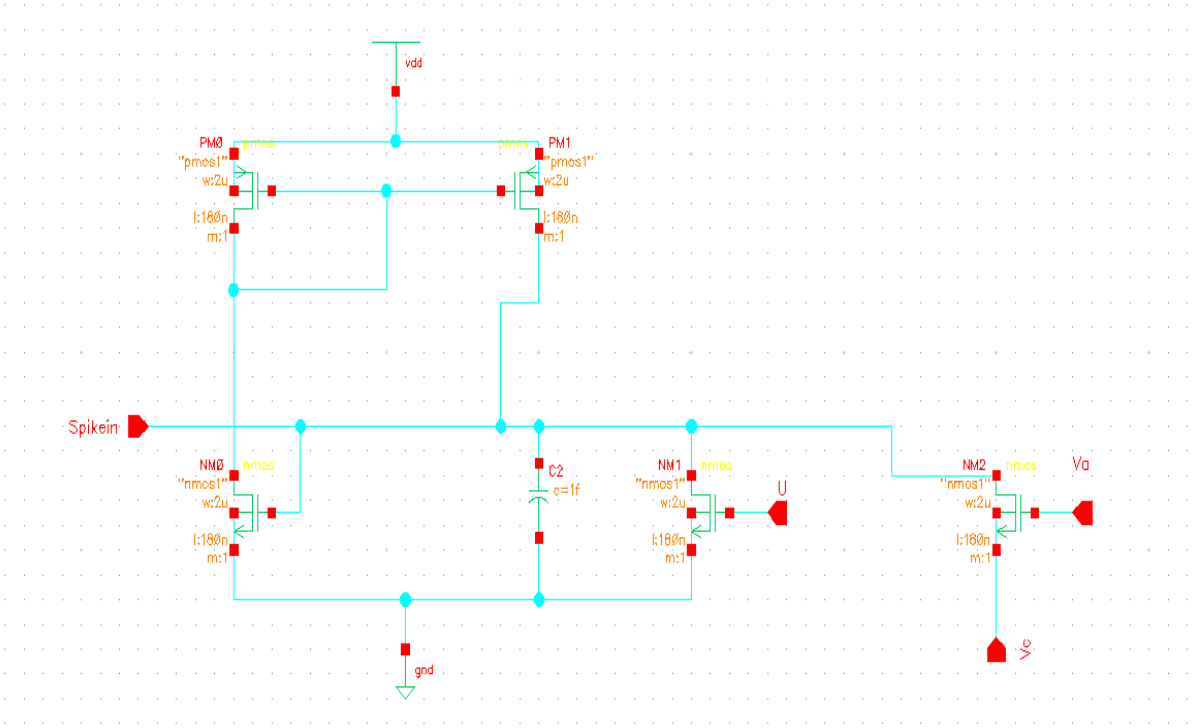

Fig.5.1 Membrane Potential circuit

Above fig.5.1 describes the circuit implementation of membrane potential where the current value through M_3 transistors, I_v is maintained by the membrane potential V_{mem}. In a current mirror circuit, transistors M_2 and M_3 is forming current, with the help of input current generated by M_1. To generate spikes, the current I_v behaves as positive feedback. Transistor M_4 is generating current I_1 whch is the leakage current and it is maintained by the slow variable U. The post synaptic current is the main input current. It is generated by external synapses circuitry. But here we are generating that input current using external input pulse circuit. The net aggregate of all currents is implemented on membrane capacitor, C_v. V_{mem} is increased by positive input current. V_{mem} is rapidly increased in generating the spike. By comparator circuit, V_A is generated when the spike is detected. Subsequently transistor M_5 on and V_m is rapidly hyperpolarized. The transistor M_5 is customized so that the capacitor C_v is fully discharged

during the V_A pulse, so that value of membrane voltage after hyper-polarization is fully observed by the value set by voltage V_c.

5.1.2 SLOW VARIABLE CIRCUIT

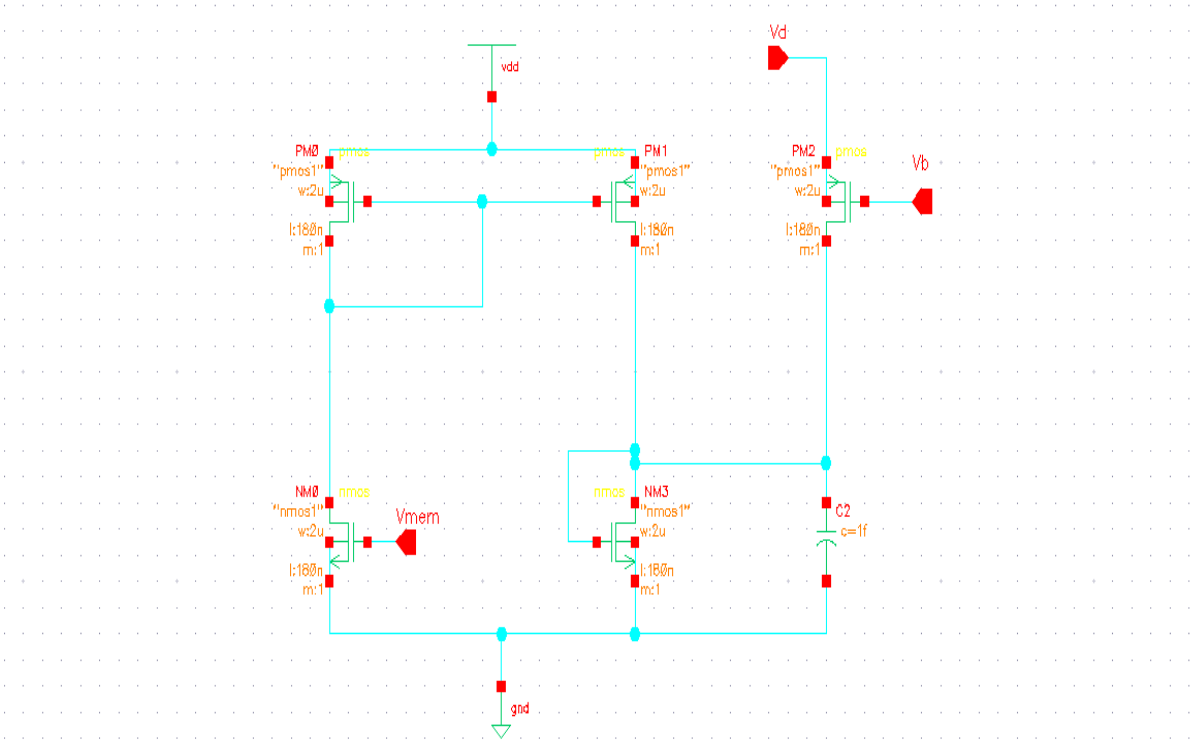

Fig.5.2 Slow variable circuit

The value of the current is observed by M_7, I_{vu} is calculated by membrane voltage. A current mirror circuit is established using transistors M_2 and M_7 with step input current provided by M_1. Scaling the transistor for the drain current of transistor M_7 is less than that of M_3 and the capacitive C_u value is larger than of C_v value. This condition shows that potential U is varying more slowly than V_{mem}.

The Transistor M_6 acts as a non-linear resistive and I_u is a function of the slow variable potential U, so that current goes through M_6.

Measuring the spike of the membrane voltage potential, the comparator circuit provides a short pulse, V_B to on the transistor M_8. The size of transistor M_8 is narrow and short pulse V_B determined that the capacitance, C_u is partially reset to V_d, though an extra charge is controlling by V_d, is followed to C_u. So each spike gives a quick increase in the slow variable potential which goes high the leakage current of the membrane voltage and decreased the depolarization after the spiking.

5.1.3 COMPARATAR CIRCUIT

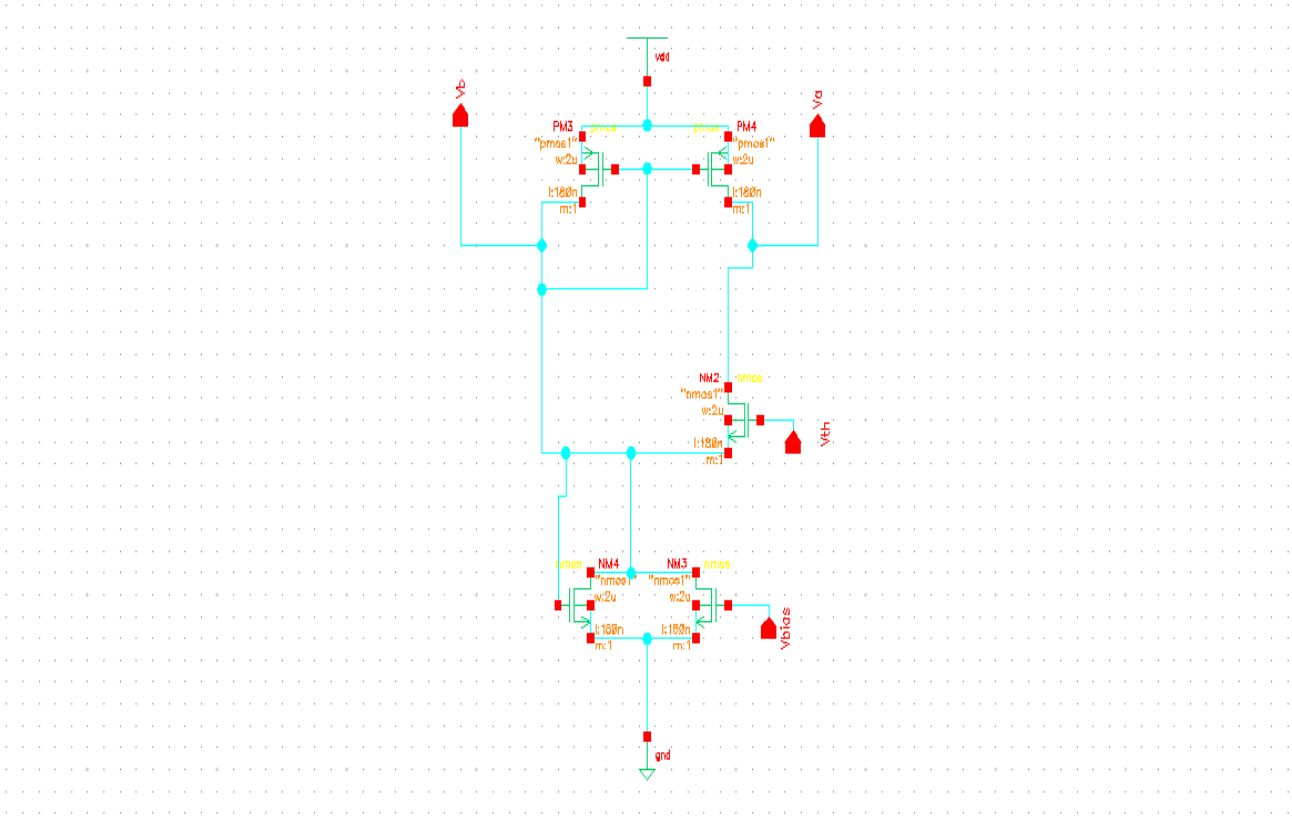

Fig.5.3 Comparator circuit

As above fig.5.3 is shown comparator circuit. The V_{th} is the spike threshold of membrane potential. Bias current is generated by bias voltage in the comparator circuit. When the membrane voltage goes rise to V_{th}, the potential at V_B is decreased and V_A is increased. It generates reset pulse of that circuit. The speed of comparator is limited and for switching the reset pulse is getting delayed. So V_{mem} goes to rise above V_{th}, and onto Vdd, though once V_A is increased. The membrane voltage goes reset to V_C which is less than V_{th}. After that V_A and V_B goes down to reset potential level, so it completes reset pulse. The required amplitude and duration of the reset short pulse V_B is provided by the transistor M_{14} through increasing current during spike.

5.2 IMPLEMENTATION OF CORTICAL NEURON CIRCUIT MODEL

Cortical microcircuits are equipped for performing modern data handling, dealing with high computational throughput of sensory recognition, subjective procedures, control and basic leadership with low energy utilization. The fundamental segment of the cortical microcircuits are neuron cells. Emulating their operation in silicon circuits is the point of the paper. It is trusted that simple VLSI model of neural circuits will give extremely productive cerebrum inspired computer engineering. It is a critical through to outline a neuron circuit with minimal number of transistors and with slightest energy dissipation , particular because of the way that such circuit is proposed to be utilized as a part of large scale VLSI neural systems that comprises of a large number of neuron while considering directly accessible neuron models the integrate and fire (I&F) neuron model is generally criticized because of it is simple operation – run of the I&F neuron cells utilize roughly 14 transistors to execute low power neuron hardware.

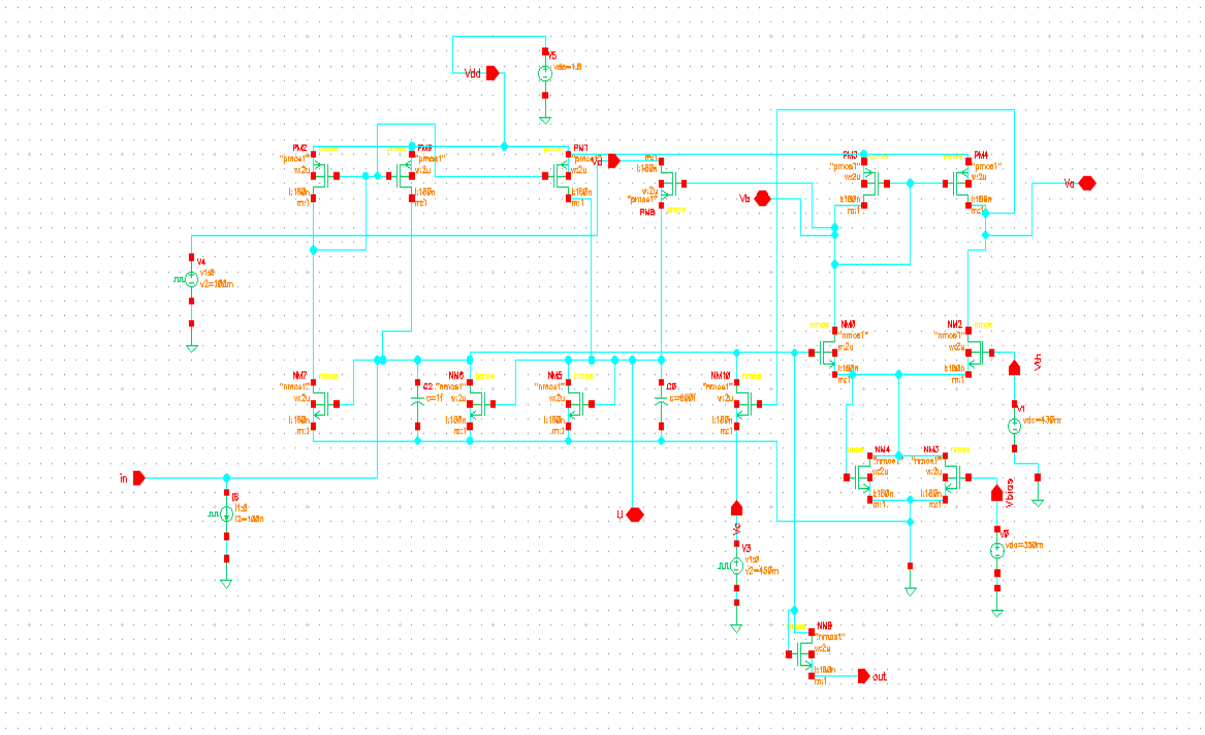

Fig.5.4 Circuit of Cortical Neuron

Be that as it may, I&F neurons show straightforward terminating conduct just, this would not be sufficient for the improvement of VLSI hardware which would fit for mimicking the handling of the cortex, which is comprised of countless complex non direct oscillatory neurons displaying an accumulation of natural terminating designs. Hodgkin-Huxley consists of large numerous of transistors in conductance based circuit implementation. Other neuron models such as Fitzhugh-Nagumo model, Resonate and Fire model and Hindmarsh-Rose model also consist near 20 transistors. But the shape of spikes do not generate correctly in all these models in neuro science. These models are not capable of generating different types of spiking and bursting in one circuit with just adjustable parameters. Here the model represents 19 transistors which is defined under non-linear characteristics of MOSFETs. The circuit generating shapes of spiking is same as real time neuron shape of spikes. Using spike frequency adaption the

circuit generates linear and non-linear characteristics and also generates different types of spiking such as chattering, intrinsic bursting, low threshold spiking, regular spiking and fast spiking. The proposed low power silicon circuit consists of 19 MOSFETs. Membrane potential(V_{mem}) and Slow variable(U) are two state variables are figured by voltages across capacitors(C_v and C_u). Four functional block is present in this circuit such as membrane potential circuitry, slow variable circuitry, comparator circuitry and modulated bias voltage circuitry.

5.3 PROPOSED IMPLIMENTATION

5.3.1 MODIFIED BIAS MODULATION CIRCUIT

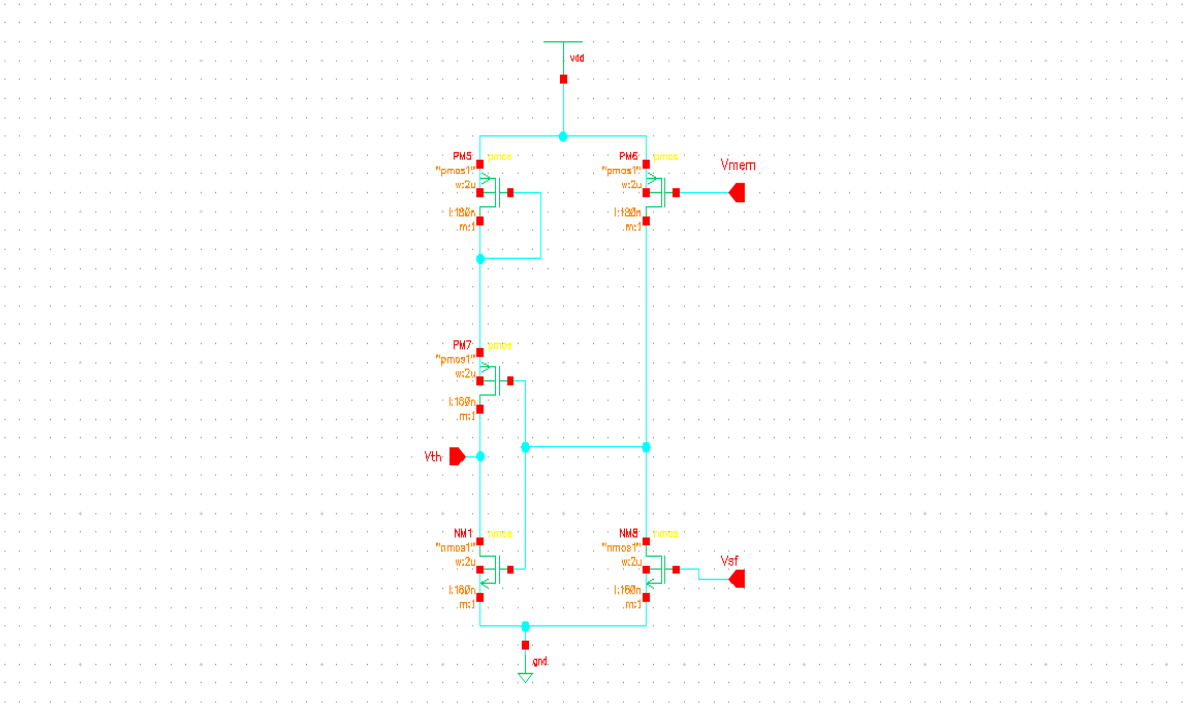

Fig.5.5 Bias modulation circuit

Bias modulation is by the transistor M_{15}-M_{19} as shown in fig.5.2. In the neuron, bias voltage is not fixed value instead it changes with respect to membrane voltage. In the circuit to achieve that membrane voltage is connected in feedback through follower and invert circuits. Membrane voltage is controlled by source follower whose output is to be

$$V = k\,(V_{mem} - V_{sf})$$

Where k= slope coefficient, V_{mem} is membrane voltage and V_{sf} is voltage applied at source follower. The voltage is to be given in inverter and it generates the bias voltage as shown in fig.xxxx. Thus it helps to achieving the dynamic behaviour of the real neuron.

5.3.2 PROPOSED IMPLEMENTATION OF CORTICAL NEURON CIRCUIT MODEL

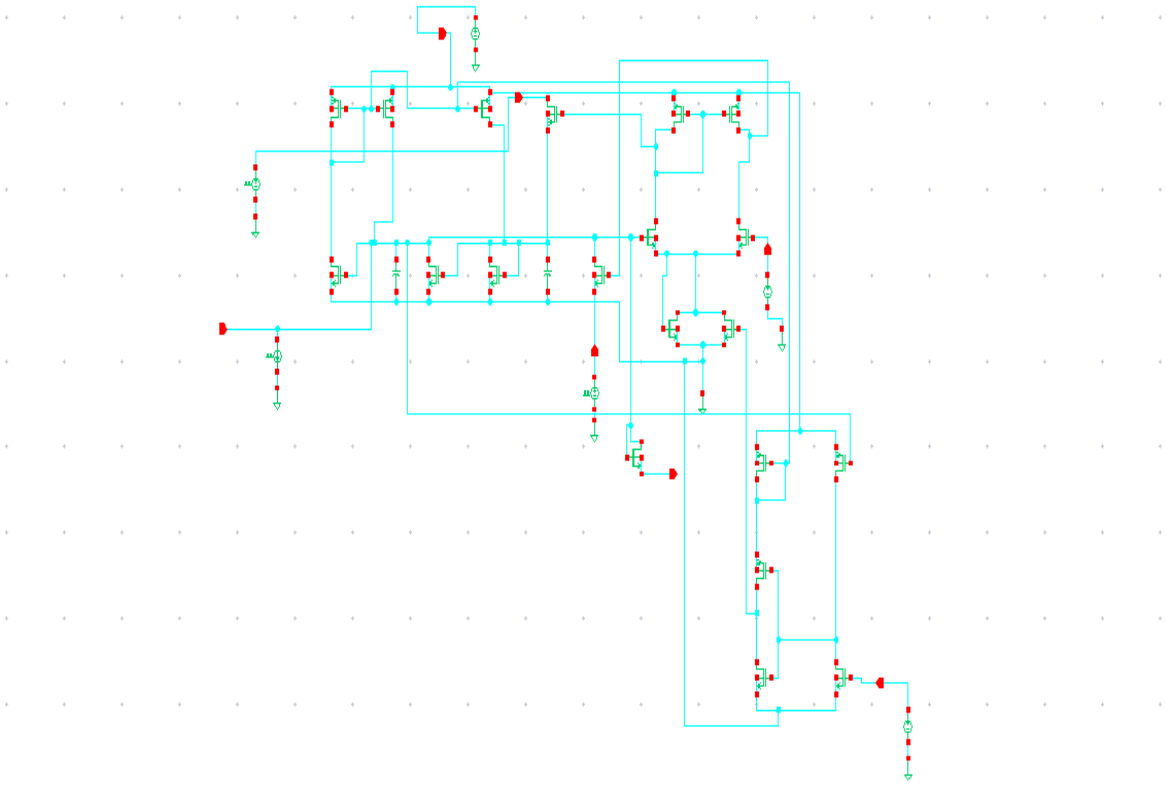

Fig.5.6 Proposed cortical neuron circuit

Above fig. 5.6 is shown the proposed cortical neuron circuit. We modulate biasing voltage. Instead of fixing the biasing voltage, it is varying with membrane voltage potential. 19 transistors are using in this proposed circuit. It is efficient to generate all types of spiking with modulated bias voltage and giving the dynamic behaviour of real neuron.

6.1 WAVEFORMS OF THE SUB-CIRCUITS AND THE INPUT

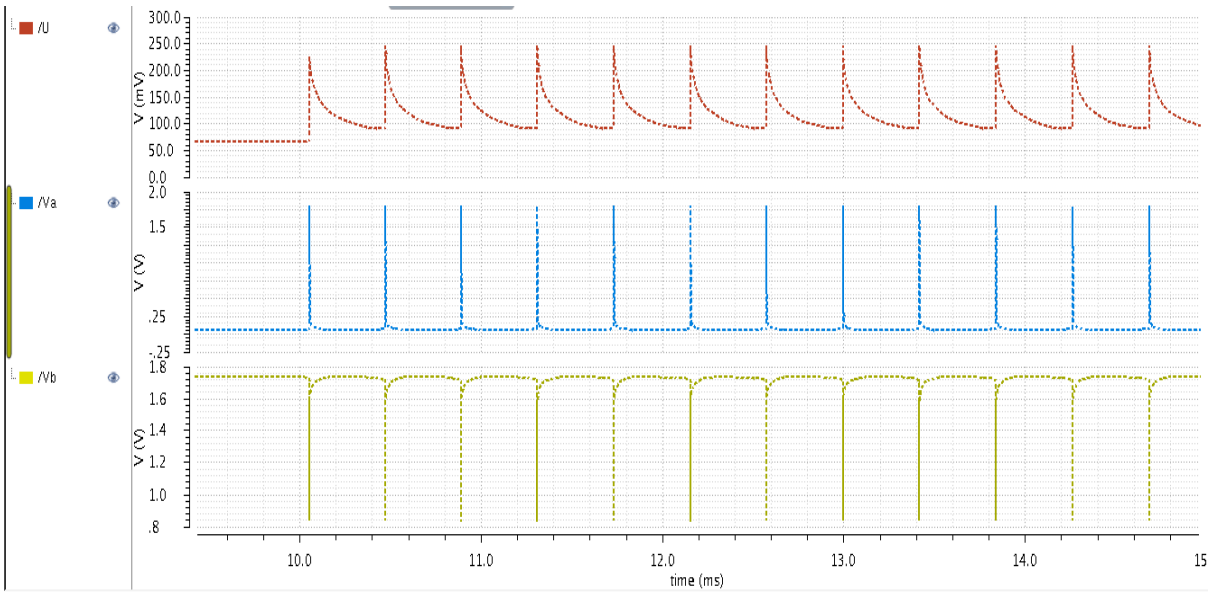

Fig.6.1 Output Waveforms of sub-circuits

(a) Slow variable potential (b) Comparator waveforms- Reset pulse V_A and V_B

As above fig.6.1 represents the output waveforms of each sub circuitry blocks. In section (a) shows the slow variable potential waveform which lies in the range of 50mV to 250mV. The transistor sizing and the capacitance value of C_u varies the slow variable output waveform. In the section (b) represents the two comparing output waveforms of the comparator. V_A lies between the range of 0.15V to 1.8V and V_B lies between the range of 1.8V to 0.8V.

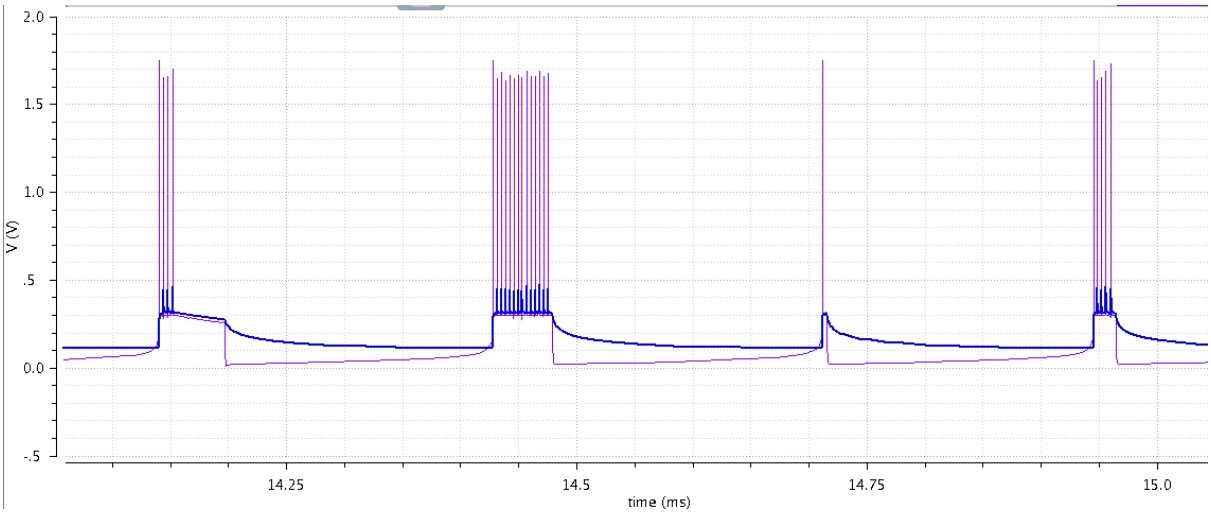

Fig.6.2 Reaction of the CH cell to a 0.1µA step post synaptic current infusion demonstrating starting and consequent spike groups of the membrane potential and respective slow variable potential.

At the point when the V_{mem} is crossed, the orbit takes after another dynamic-path in Fig. 6 creating a fast release of the slow variable until the trajectory achieves the U where the rate of increment in V_{mem} winds up noticeably huge. When V_{mem} ends up noticeably predominant, since the slow variable U is at a lower potential, it obeys same cycle as the initial section. It is repeatable until the supra-threshold voltage exists. So the overall dynamics produce chattering behaviour.

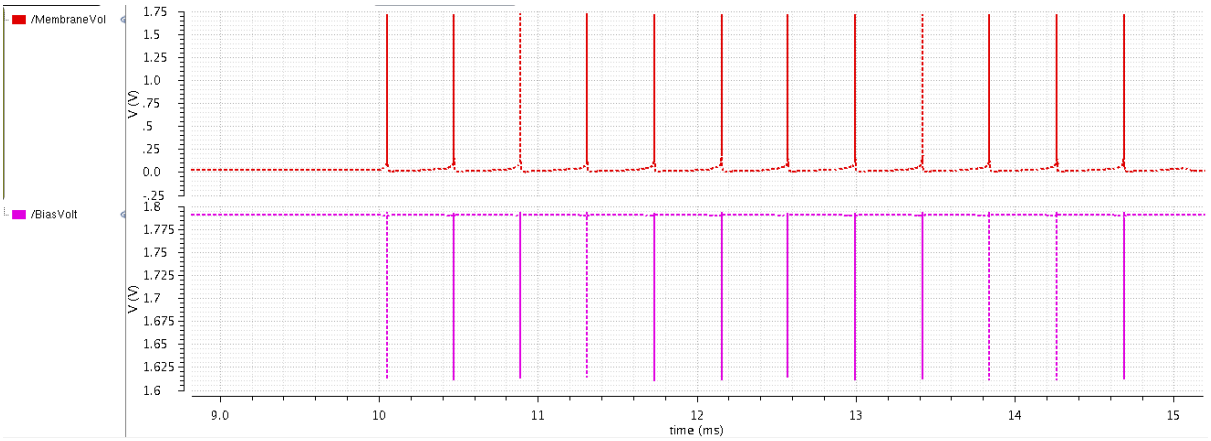

Fig.6.3 Alteration in membrane potential with respect to bias voltage

Here we represent variation in membrane voltage potential with respect to bias modulated voltage. It shows variation with respect to regular spiking. So we conclude that from that fig.6.3, bias voltage is not fixed or previously determined. It varies according to V_{mem} voltage and bias voltage is modulated by membrane potential.

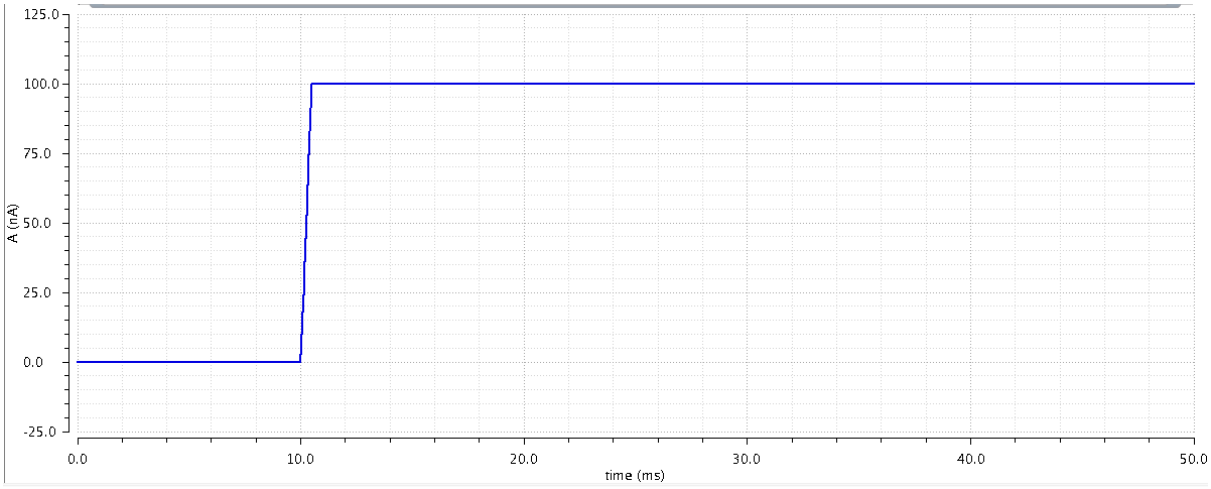

Fig.6.4 Input step current

This is the step input current for cortical neuron circuit. This current acts as synaptic current in the circuit.

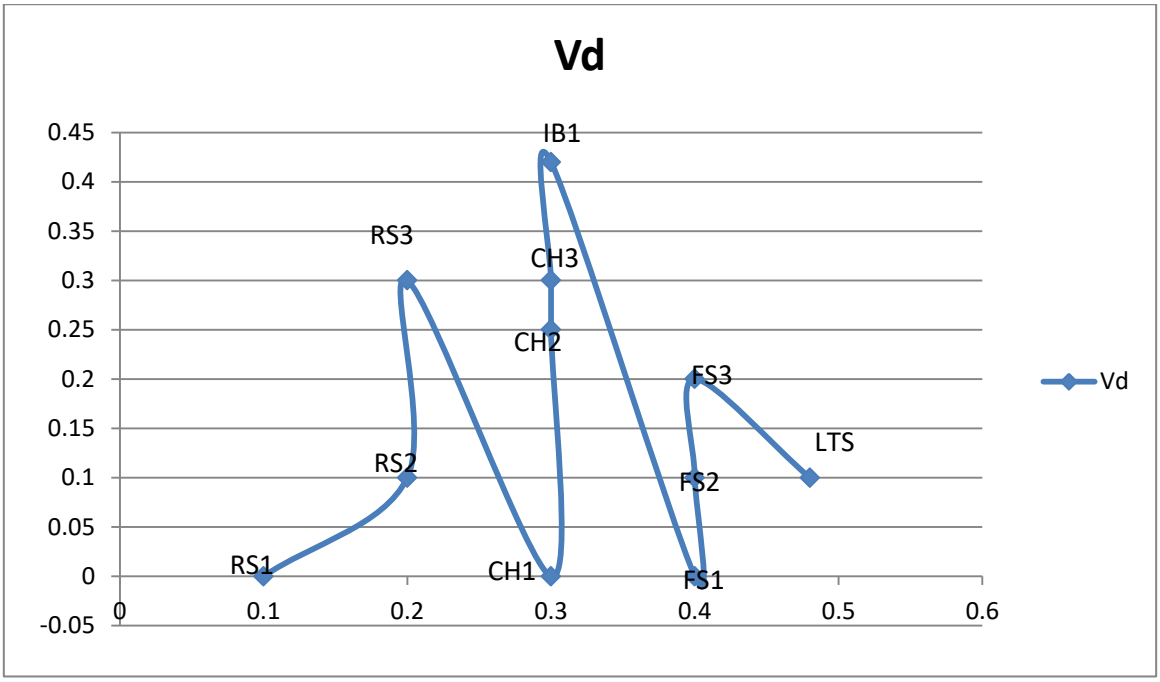

Fig. 6.5: Values of Vc and Vd to determine the spike output

6.2 OUTPUT WAVEFORM OF THE PROPOSED CIRCUIT

6.2.1 REGULAR SPIKING

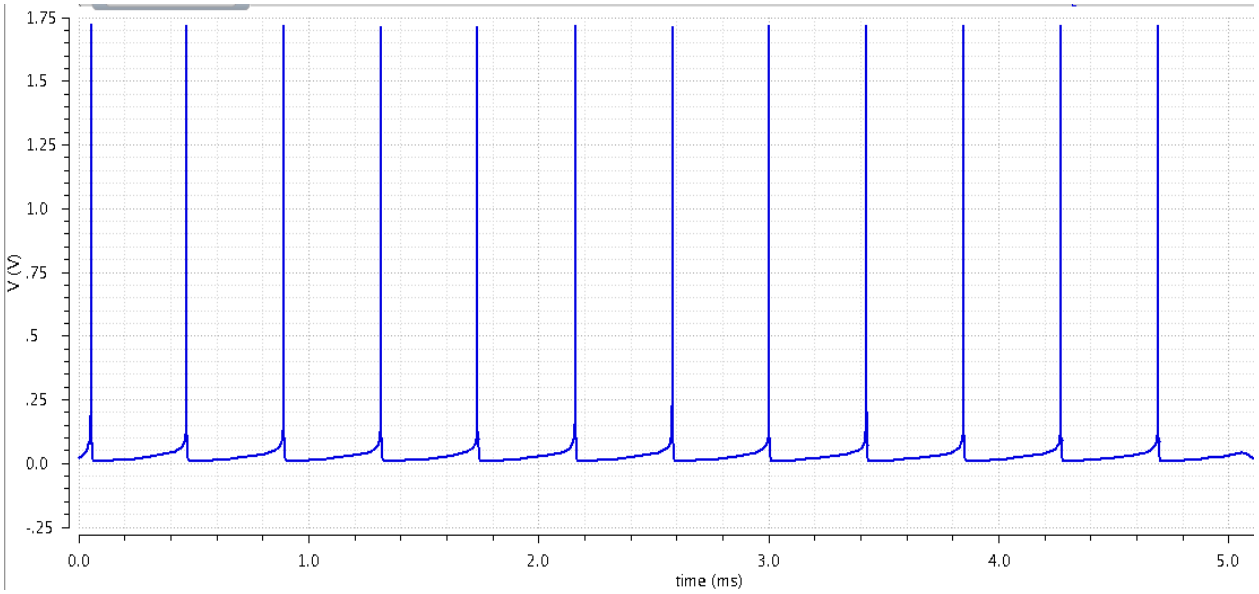

Fig.6.6 Regular Spiking (RS1)

As name mentioned Regular spiking (RS) gives a single repeated spike output at regular intervals. The step input current is 0.1µA for that simulation. It is observed that time taken in millisecond of VLSI neuron model. Here V_d is set to 0V and V_c is set to 0.1V for RS1.

Comparator circuit is maintained range at 0.35V. For changing V_c and V_d, pattern of output spiking is changing. Single spike fire is important for the neuron cell.

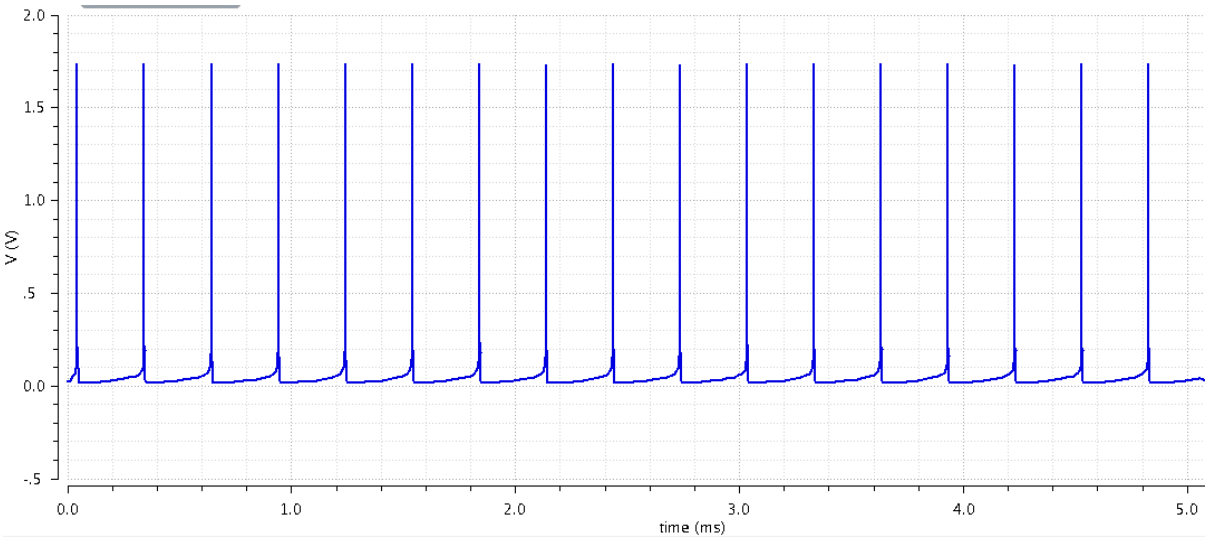

Fig.6.7 Regular Spiking (RS2)

Here the value of Vc = 0.2V and V_d = 0.1V. From above fig.6.6, it shows regular spike is more than previous one.

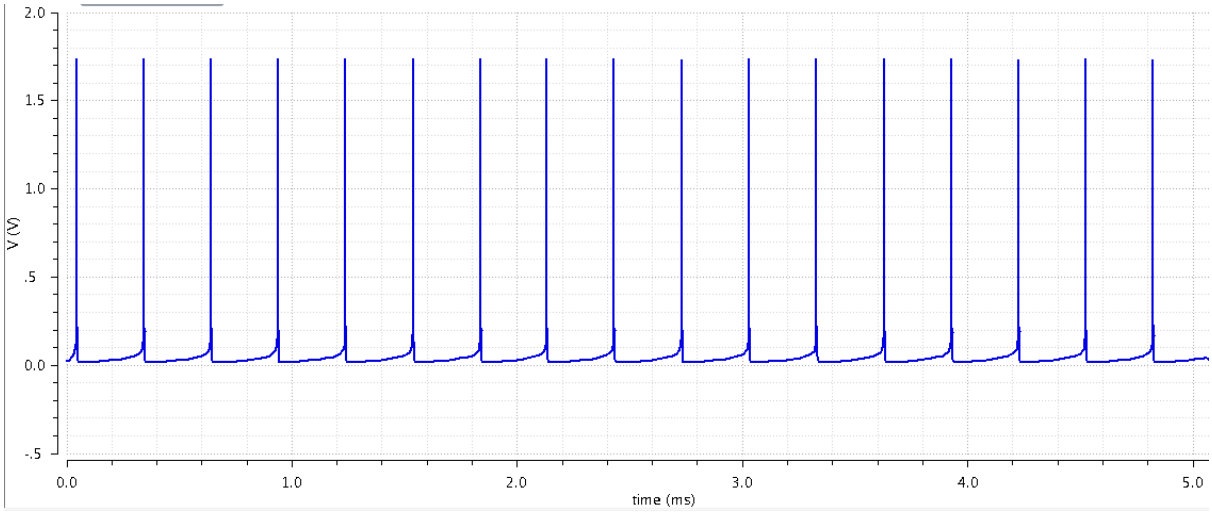

Fig.6.8 Regular spiking (RS 3)

Here the value of Vc = 0.2V and V_d = 0.3V. The spike patterns are more as shown in above diagram.

6.2.2 CHATTERING

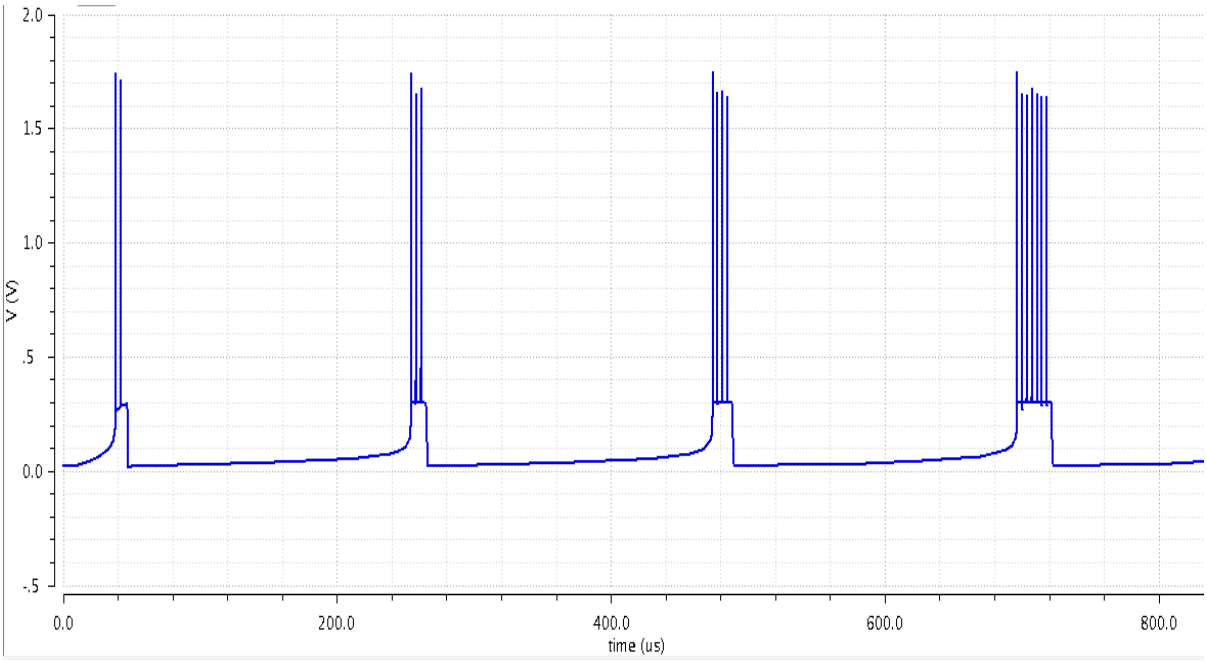

Fig.6.9 Chattering (CH1)

Chattering is a pattern of more than four to twelve spike or burst is continued at irregular intervals. The number of spikes is depending on accommodation period to fire the neuron cell. Here we kept at V_d = 0V and V_c = 0.3V. As V_d increases, the number of spikes is also increased. The step input current is 0.1µA.

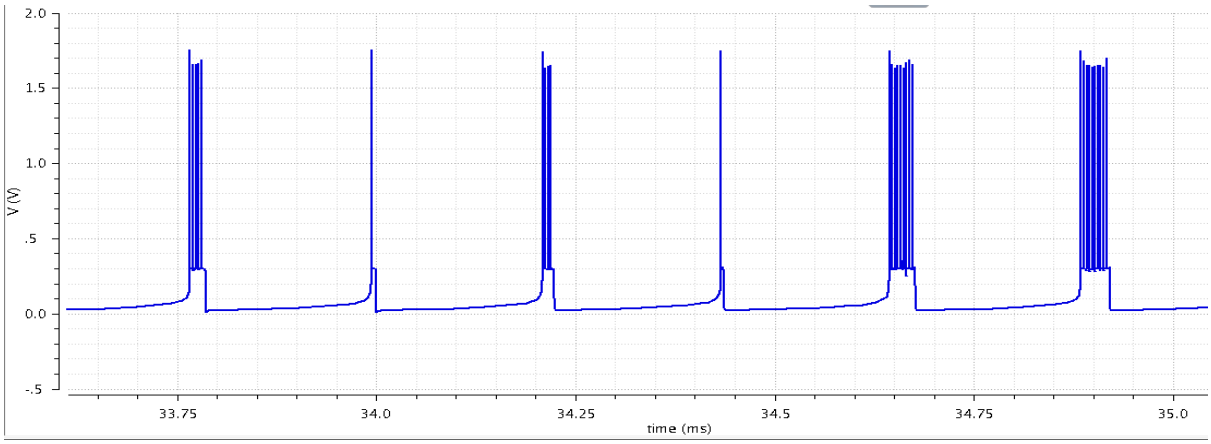

Fig.6.10 Chattering (CH2)

Here we kept at V_d = 0.2V and V_c = 0.3V. The pattern of bursting is more.

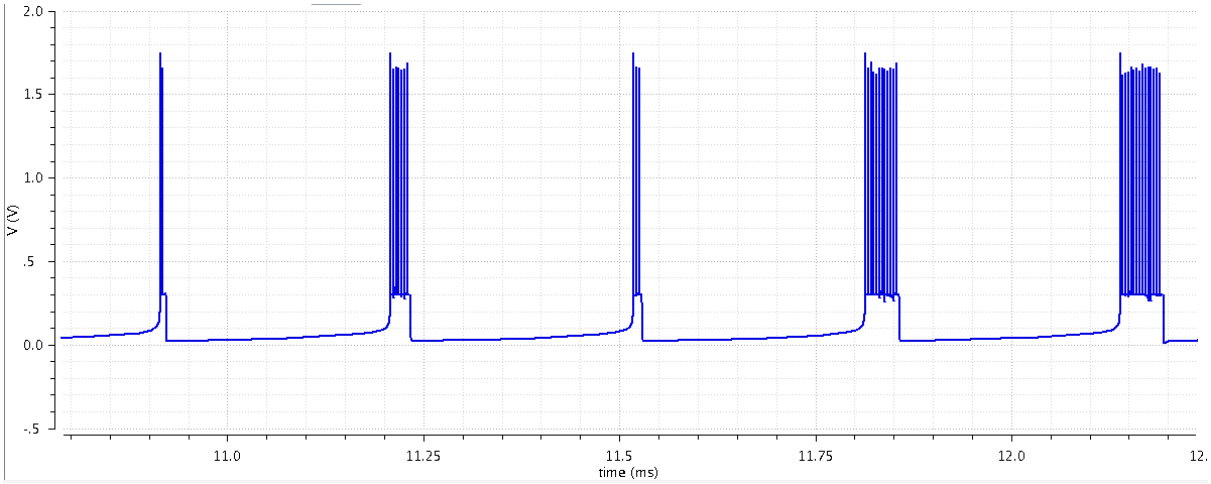

Fig.6.11 Chattering (CH3)

Here we kept at V_d = 0.3V and V_c = 0.3V. The spike pattern is more and more as we V_d is increased. The input current is always same or constant at 0.1µA.

6.2.3 INTRINSIC BURSTING

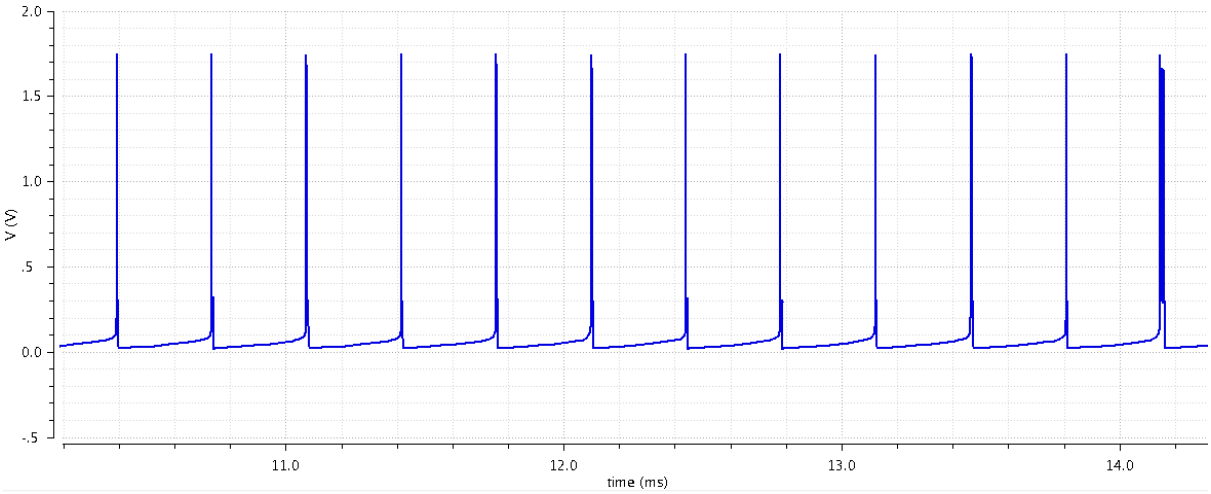

Fig.6.12 Intrinsic Bursting (IB1)

Intrinsic bursting is a pattern of more than two spikes is continued at regular intervals. The number of spikes is depending on accommodation period to fire the neuron cell. From the above fig.6.11 shows the spike out is generated when V_d is set to 0.1V and V_c is set to 0.35V. As the value of V_d is increased, the pattern is more realistic.

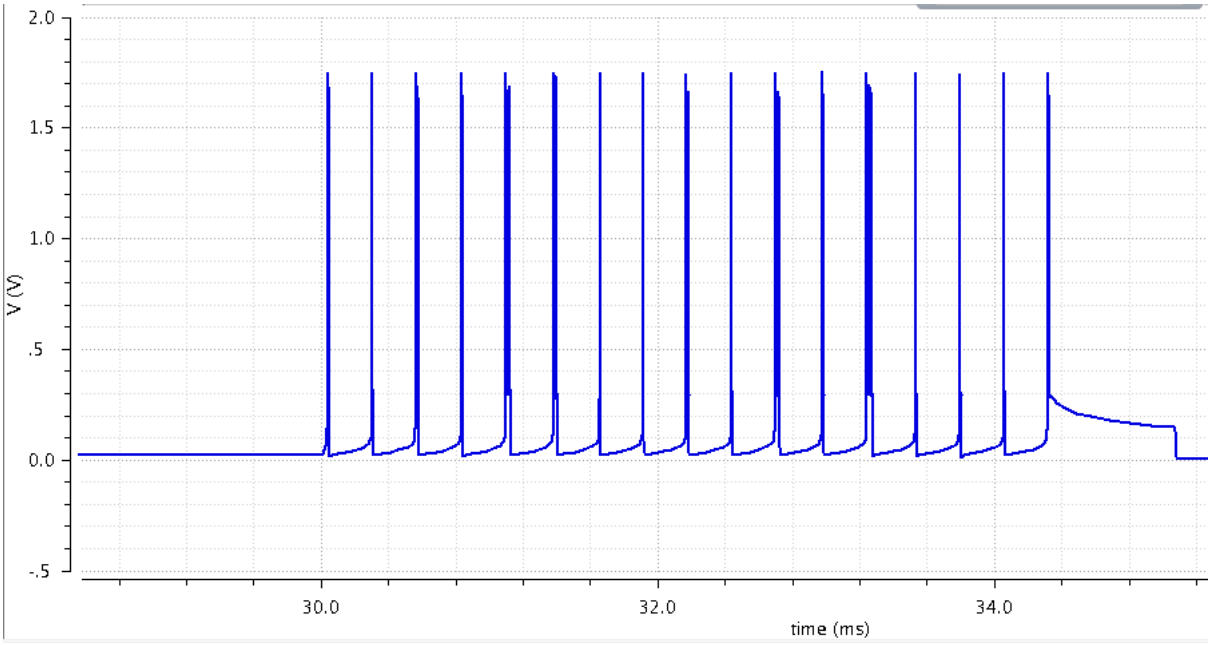

Fig.6.13 Intrinsic Bursting (IB2)

Here V_d is set to 0.35V and V_c is set to 0.35V. The step input current value is 0.1µA. The bursting pattern is more dense as shows in fig.6.13.

6.2.4 FAST SPIKING

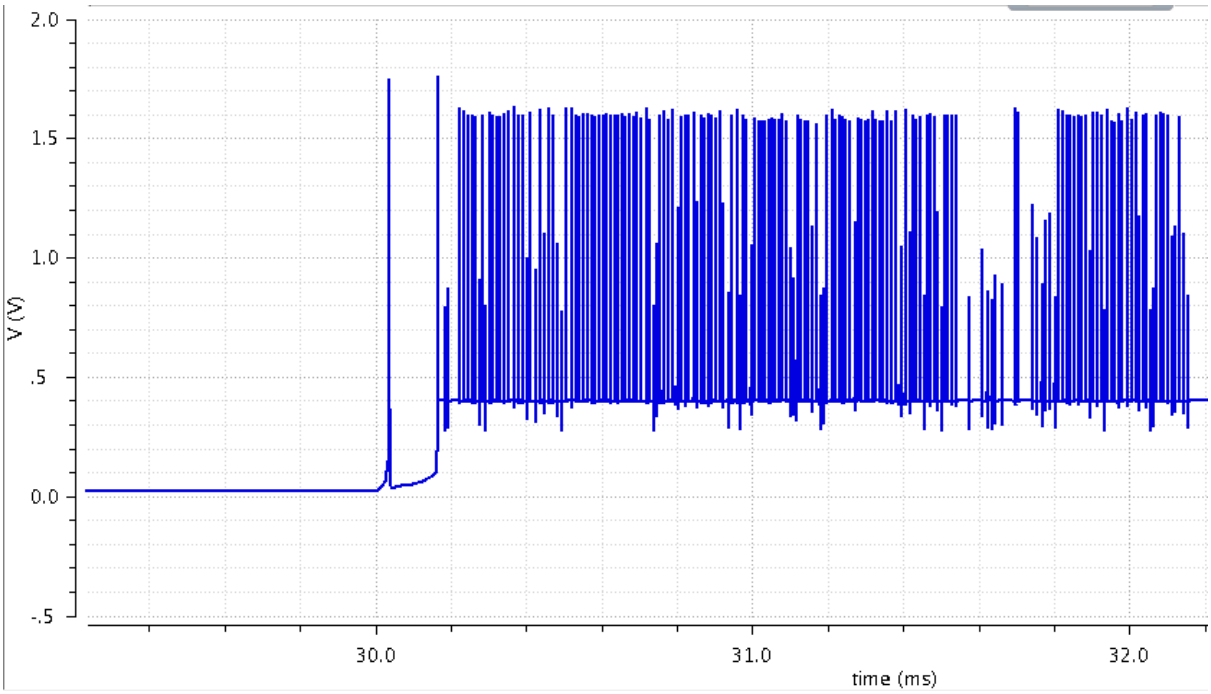

Fig.6.14 Fast Spiking (FS1)

In Fast spiking, there is no accommodation to sustained supra-threshold current. The input current is a step function and the value is 0.1µA. Supply voltage is set at 1.8V. Here we are controlling V_c and V_d value. As V_d is increased, the spike pattern is more fast and continued. Here we kept V_d = 0V and V_c = 0.4V .

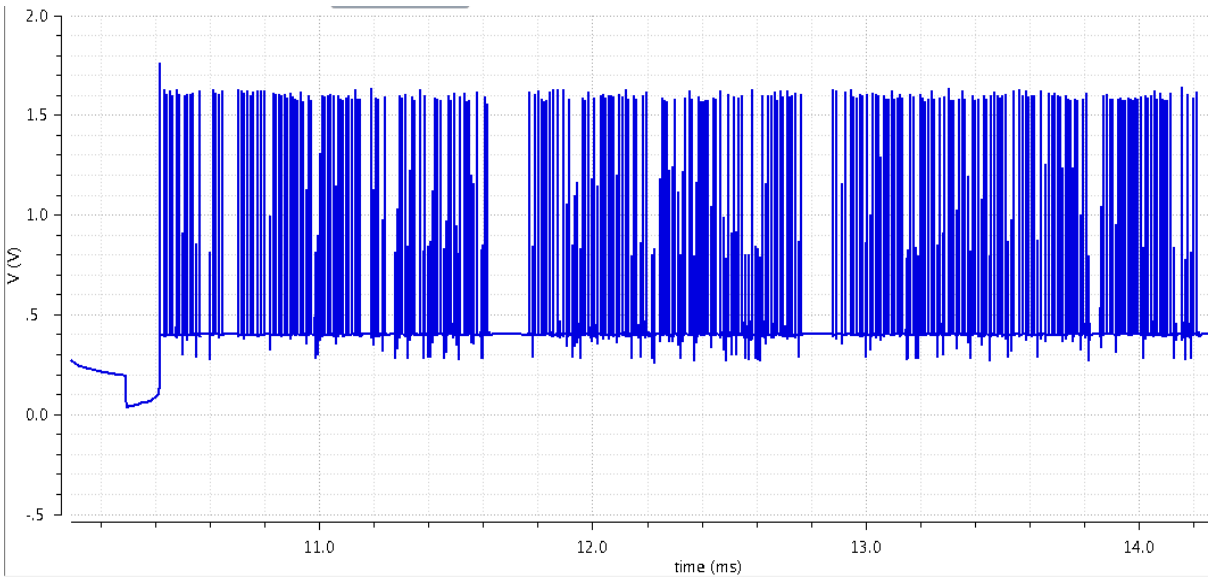

Fig.6.15 Fast Spiking (FS2)

Here Vd is kept to 0.1V and Vc is kept to 0.4V. No accommodation is required for fast spiking.

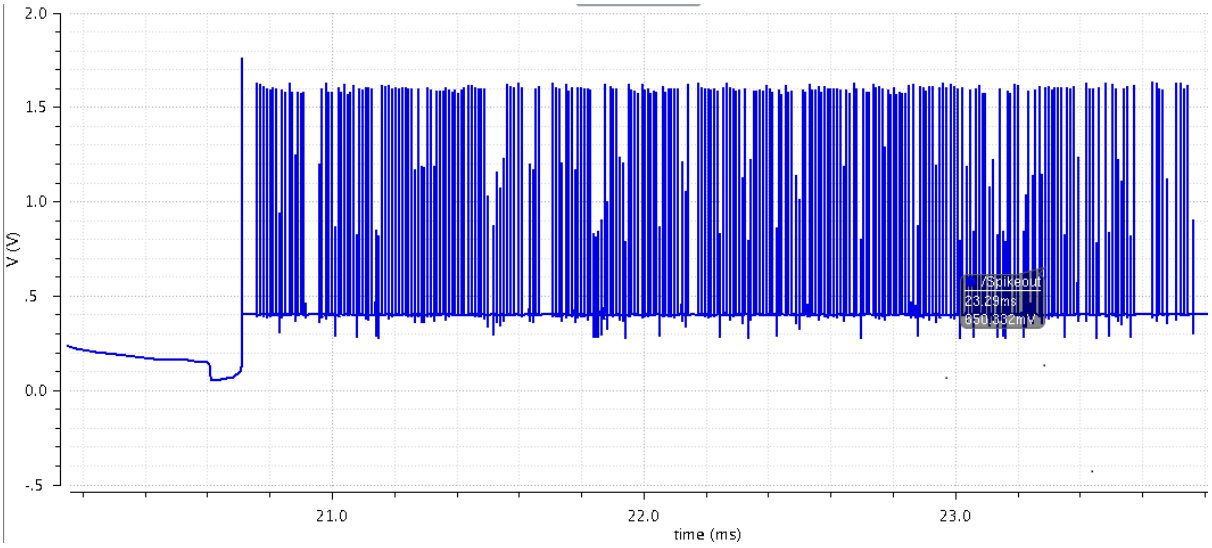

Fig.6.16 Fast Spiking (FS3)

Here V_d is kept to 0.2V and V_c is kept to 0.4V. It repeats very fast, so it is called as fast spiking. The value of capacitor C_u is not get enough time to get discharge and fast spike out is observed.

6.2.5 LOW THRESHOLD SPIKING

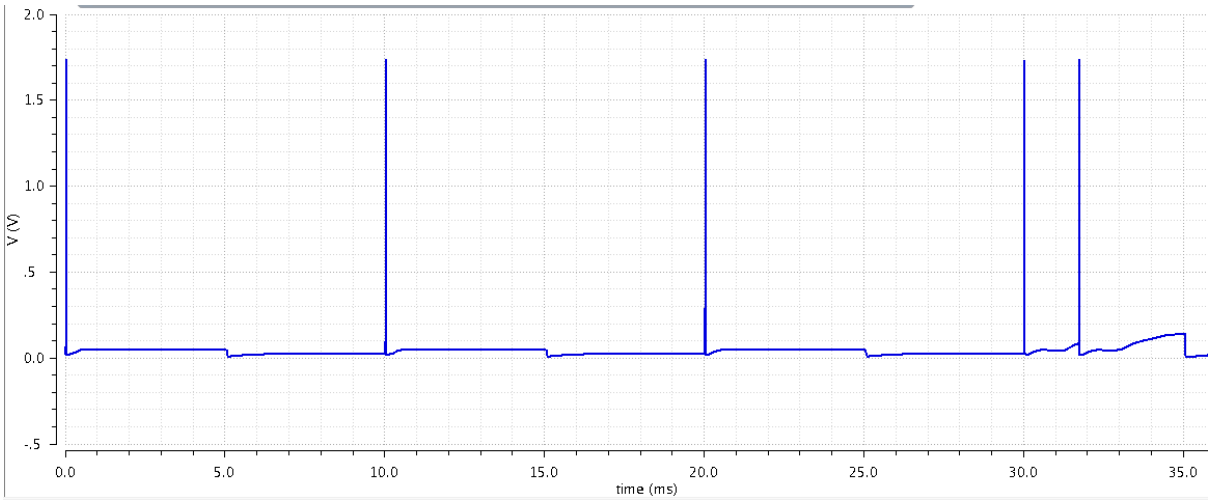

Fig.6.17 Low threshold spiking

LTS operates at the level of threshold value. A myth in neuromorphic engineering is belief that neuron cells have a constant threshold voltage. Firstly we consider a input as same as subthreshold pulse of voltage. After that the neuron fires again because it is threshold is lowered by pre input. The input step current is 0.01µA. The value of V_c is set to 0.2V and V_d is set to 0.5V.

6.3 POWER CALCULATION

In the past, the device density and operating frequency were low enough that it was not constraining factor in the chips. As the scale of integration improves, more transistors, faster and smaller than their predecessors, are being packed into a chip. This leads to the steady growth of the operating frequency and processing capacity per chip, resulting in increased power dissipation. New generations of processing technology are being developed while present generation devices are at a very safe distance from the fundamental physical limits. A need for low power VLSI chips arises from such evolution forces of integration circuits. From environmental concerns, low power chips and system have a major demand. When it comes to portability power is the main constraints.

Here we concerning about mainly output spiking. Power dissipation is not main concern. We are calculating for each spiking output. It describes how power dissipation is going to be changed depending upon input current

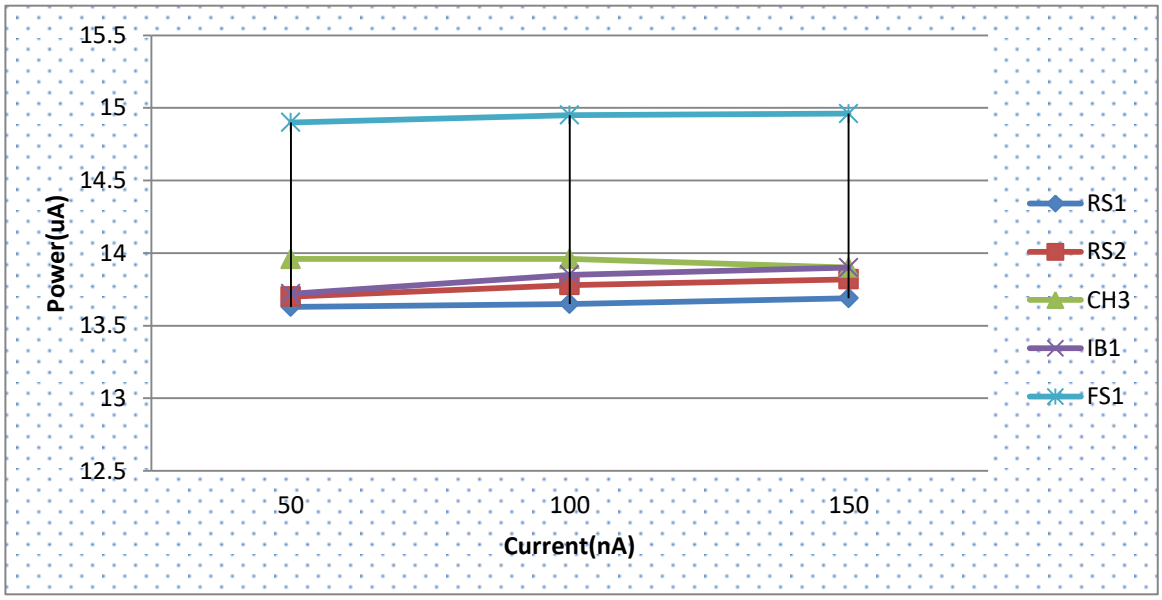

Fig 6.18: Power analysis at different currents

The above graph shows the graphical representations of the power for different types of spiking. Here we can see FS consumes the higher power but in other patterns consume very less. This occurrence happens for fast rising and falling rates of membrane voltage in FS. Regular spiking consumes less power while CH and IB consume comparatively high power.

Table 6.1: Power Analysis at Different Currents

Types of Spikes	Current	Power
RS1	50 nA	13.63*10^-6 µW
	100 nA	13.65*10^-6 µW
	150 nA	13.69*10^-6 µW
RS2	50 nA	13.70*10^-6 µW
	100 nA	13.78*10^-6 µW
	150 nA	13.83*10^-6 µW
CH3	50 nA	13.96*10^-6 µW
	100 nA	13.96*10^-6 µW
	150 nA	13.90*10^-6 µW
IB1	50 nA	13.72*10^-6 µW
	100 nA	13.85*10^-6 µW
	150 nA	13.90*10^-6 µW
FS1	50 nA	14.90*10^-6 µW
	100 nA	14.95*10^-6 µW
	150 nA	14.96*10^-6 µW

Here we are calculating power for varying the input current. Power is to be increased while varying the input current for each spike out pattern. We kept constant the two input voltage V_c and V_d. For some cases spike out pattern may vary for changing the input current.

6.4 COMPARISION WITH DIFFERENT NEURON MODELS

Comparison between different neuron models and proposed model give an idea to evaluate the best model. We can determine the different characteristics, output patterns and no of components used. It gives also the power consumption value to determine which one is best for low power design.

Table 6.2: Comparison between different neuron model with respect to proposed neuron model

Neuron Model	**Number of Transistors**	**Types of Spiking (RS, CH, IB, FS, LTS)**	**Shape of Spikes**	**Threshold Modulation**	**Power (µW)**
Conductance-based	27-30+	Normal Spiking	Good	_	60
Integrate and fire	18-20	Normal Spiking	Fair	Yes	0.3-1.5
Fitz Hugh-Nagomo	21	Oscillatory	Envelope	_	_
Morris-Lecar	22	Oscillatory	Envelope	_	_
Resonate and Fire	20	Oscillatory	Pulse	_	_
Hindmarsh-Rose	90	Bursting (CH)	Fair	_	163.4
Compact Silicon Neuron	14	All types	Good	_	8-40
Proposed Circuit	19	All types	Good	Yes	13.63-14.96

In above table we are discussing comparison of the performance of different neuron models and proposed neuron model. The proposed model is capable to generate all types of spiking and the output spike patterns is also good as compare to others.

CONCLUSION

The CMOS neuron circuit is generating bursting and spiking firing characteristics with a biological spike shapes. The behaviour of that circuit is verified through cadence simulation. The proposed circuit is capable of mimics to generate different types of spiking which is resembles of the real neuron cells. The characteristics of cortical cells should be adjusted by threshold voltage and biasing voltage. Here biasing voltage is modulated by membrane potential. The circuit is implemented using 19 transistors. Because of the less number of transistors is used so that it can be integrated in large arrays of cortical micro circuits and take a small silicon area. To generate parallel analog neuromorphic networks, we are using simple, compact and easily configurable cortical neuron. It is as similar as neocortex characteristics by changing (W/L) ratio of the transistors M_4, M_6, M_7. This circuit is designed using 180nm technology. The spiking output is mainly vary when two voltages V_c and V_d is changing respectively. The circuit is consumed low power compared to other neuron circuits. So it helps to use in building low power cortical neuron microcircuits.

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