DESIGN AND ANALYSIS OF LOW POWER MULTI-BIT FULL ADDER

DISSERTATION-II

Submitted in partial fulfillment of the

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By

Rishab Goyal

Under the Guidance of

Mr. Sanjeev Sharma

Assistant Professor

Department of ECE

Electronics and communication engineering

Lovely Professional University Punjab

April 2017

CERTIFICATE

This is to certify that the Dissertation-II titled "Design and Analysis of Low Power Multi-Bit Full Adder" that is being submitted by " Rishab Goyal" is in partial fulfillment of the requirements for the award of MASTER OF TECHNOLOGY DEGREE, is a record of bonafide work done under my /our guidance. The contents of this Dissertation-II, in full or in parts, have neither been taken from any other source nor have been submitted to any other Institute or University for award of any degree or diploma and the same is certified.

Mr. Sanjeev Sharma
(Assistant Professor)
Dissertation-II
LPU

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Place: LPU, Jalandhar
Rishab Goyal
Date: April 2017
Reg.No:11503677

DECLARATION

I, Rishab Goyal, student of M-Tech Electronics and communication under Department of Electronics and communication of Lovely Professional University, Punjab, hereby declare that all the information furnished in this Dissertation-II report is based on my own intensive research and is genuine.

This thesis does not, to the best of my knowledge, contain part of my work which has been submitted for the award of my degree either of this university or any other university without proper citation.

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ABSTRACT

Several circuit design techniques are compared in order to find their efficiency in terms of speed and power dissipation. The increasing demand for low-power VLSI (Very Large Scale Integration) can be addressed at different design levels, such as architectural, circuit layout, and the process technology level. In today era, one of the biggest challenge is to fabricate that type of circuit which gives not only the low power but also gives the high performance VLSI circuits. Also power and delay parameters of any VLSI circuits can be diminished at the corresponded time, for that we can improve these two parameters to get the appropriate result.

The developed purpose of using convenient electronics systems has manufactured power dissipation and crucial design specification in current electronics. Portable equipment's that work utilize the battery contains finite energy supplies and thus have a generation that are recognize by their power consumption.

Some design techniques has been proposed using the combination of Gate Diffusion technique with Pass Transistor Logic, Domino Logic with Gate Diffusion technique as well as Adiabatic Logic with Gate Diffusion technique which plays a very vital role for the low power consumption and propagation delay. The simulation work is carried out using 180nm technology. As far as now, power was not only the major issue because of the opportunity of vast packages and cooling techniques that has the ability of reducing the dissipation in the generated heat. Despite, due to extending developing density as well as the intensity of the chip in the classification might purpose obstacle in contributing adequate cooling and accordingly, add appropriate price to the system. That is why we demand a circuitry who can decrease the power dissipation although the number of components are integrated on an individual chip. The mail goal is to reduce the power dissipation in the digital CMOS VLSI Circuits. The developed requirement for the low power IC's has headed to the various low power consumption methodologies. Adiabatic Logic is one of the most prominent technique which plays a very vital role for the power consumption in the circuit. In VLSI, another most prominent technique which is used to reduce the power i.e. Domino Logic Circuit. As we know, designing of low power with high speed performance is one of the biggest protest in the VLSI design circuits

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LIST OF ABBREVIATIONS

AC	Alternate Current
CMOS	Complementary Metal Oxide Semiconductor
ECRL	Efficient Charge Recovery Logic
GDI	Gate Diffusion Input
GND	Ground
NMOS	N-Type Metal Oxide Semiconductor
PDP	Power Delay Product
PTL	Pass Transistor Logic
PFAL	Positive Feedback Adiabatic Logic
PMOS	P-Type Metal Oxide Semiconductor
TFA	Transmission Function Adder
TG	Transmission Gate
VDD	Voltage Drain to Drain
VLSI	Very Large Scale Integration

CHAPTER 1
INTRODUCTION

In today's era, there are two main issues which we as a VLSI design engineers are facing todays i.e. Power Dissipation and Propagation Delay. We can work and design our circuit by using various technologies but on every design technologies there are some constraints which cannot be neglected. In the applications of microprocessor, digital signal processing and image processing the operations which are commonly used i.e. Subtraction, Addition, AND and OR. In Digital Signal Processing application, the perspective of throughput, latency and delay are the major aspects for the performance of addition. Most of the adder circuits not only increases the delay but also dissipates the huge amount of power. So in the circuit our main focus is to reduce the power and delay.

To developing the achievement of VLSI circuits as well as consolidate higher performance into the each individual chip, intensity of transistor is frequently decrease that result not only the power consumption in the circuit but also increases the complexity of the chips. In today era, one of the biggest challenge is to design that type of circuit which gives not only the low power but also gives the high performance in the VLSI circuits and also the delay parameters can be decreased at the corresponded time. For that we can improve these two parameters to get the appropriate result.

In Complementary Metal Oxide Semiconductor (CMOS) circuits, there are three major improvements through which we can consume the power is mentioned below:-

- The active power due to charging and discharging of the circuit capacitances during switching.
- Due to the leakage current, there is a leakage power in the circuit.
- There is a short circuit current that moves from Supply to GND where the P-Sub as well as N-Sub Network of Complementary Pass Transistor Logic Gate charge simultaneously.

Adiabatic Logic is one of the most prominent technique which plays a very vital role for the power consumption in the circuit. Adiabatic logic aims to decrease the power in the logic circuit. Although there are many other techniques like pass transistor logic who helps to reduce the power but adiabatic logic is one of the most prominent technique which is used for the consumption of power.

In VLSI, another most prominent technique which is used to reduce the power i.e. Domino Logic. In Very Large Scale Integration Circuit, performance plays a very vital role for the architecture of low power and high speed in the circuit. For division, multiplication as well as exponential operations, full adder is one of the basic block. In VLSI design circuits, hybrid logic is also used to reduce the power and gives the high speed performance. It is the combination of the Transmission Gate (TG) logic and C-CMOS (Complementary Metal Oxide Semiconductor) logic.

1.1 Classifications of Adders

An adder is a digital circuit that performs addition of numbers. In many computers and other kinds of processors adders are used in the arithmetic logic units. They are also utilized in other parts of the processor, where they are used to calculate addresses, table indices, increment and decrement operators, and similar operations. Some of the important classifications of Adders are given below:-

1.1.1 Full Adder

Full Adder circuits is used for the addition of 1-bit binary numbers i.e. C A B as an input and two 1-bit binary numbers i.e. SUM and CARRY as an output. It is a normally a component in the adder of cascade, which adds binary numbers i.e. 8, 16, 32 etc. The truth table of the full adder is shown below:-

A	B	Cin	Cout	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Table 1.1 Truth table of Full adder

The full adder expression is mentioned below:-

SUM = A XOR B XOR C

CARRY = AB+BC+CA

Circuit Diagram:-

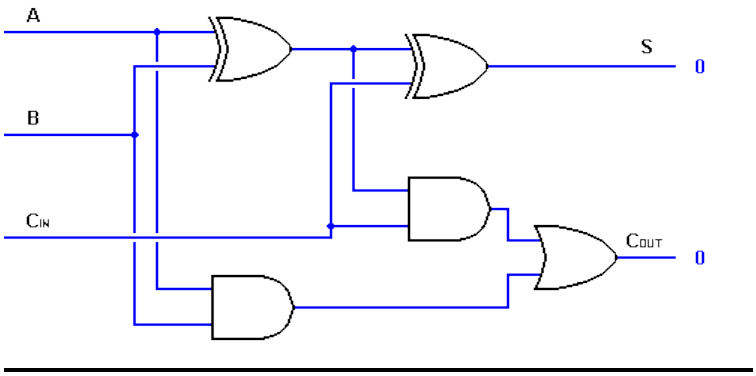


Figure 1.1 Full Adder

Full Adder using Half Adder:-

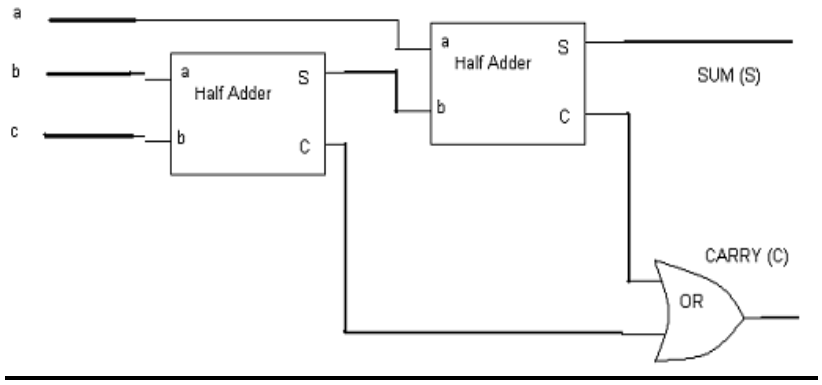


Figure.1.2 Full Adder using Half Adder

1.1.2 Ripple Carry Adder

An N-bit adder can be constructed by cascading N-full adder circuits which is connected in series as shown in **Figure.1.3**

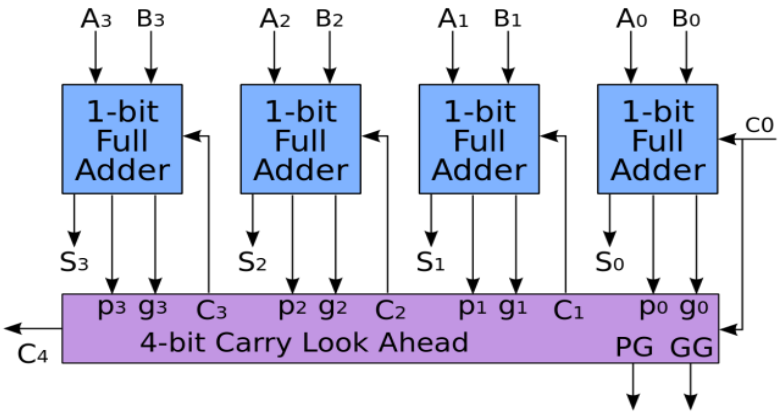


Figure 1.3 Ripple Carry Adder

In the ripple carry adder, the carry bit 'ripples' from one stage to the other. For some input signals, no rippling effects occurs at all, while for others, the carry has to ripple from LSB to MSB. The expression of the ripple carry adder is:-

For division, multiplication as well as exponential operations, full adder is one of the basic block.

Tadder ~ (N-1) Tcarry + Tsum

Where, "Tcarry" and "Tsum" equals to the propagation delays.

1.1.3 Carry Skip Adder

Carry by-pass adder is also known as the carry skip adder. Carry skip adder has the four NAND Gate as an input for propagation signals in the 4-bit group. The figure of the carry skip adder is mentioned below:-

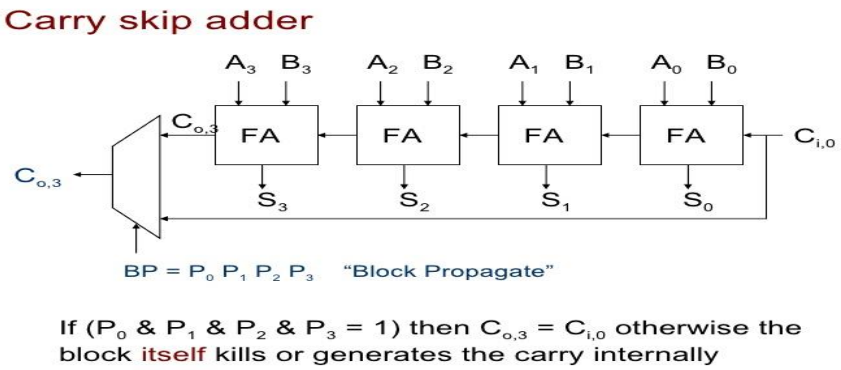


Figure 1.4 Carry Skip Adder

In carry skip adder, carry is generated along with the critical path from bit-1 and after propagating it through the remainder of the adder. Through the next 3 bits, the carry must ripple but after it skips the next four bit. The expression of Carry skip adder is mentioned below:-

$$\mathbf{Tskip = Tpg + 2(n-1)\ Tao + (k-1)\ Tmux + Txor}$$

1.1.4 Carry Look ahead Adder

Carry skip adder is quiet alike to the carry look-ahead adder. It is used to measure the group propagate signals and group generating signals to neglect the delay for the ripples if the group first generates a carry. The carry look-ahead circuit diagram is given below:-

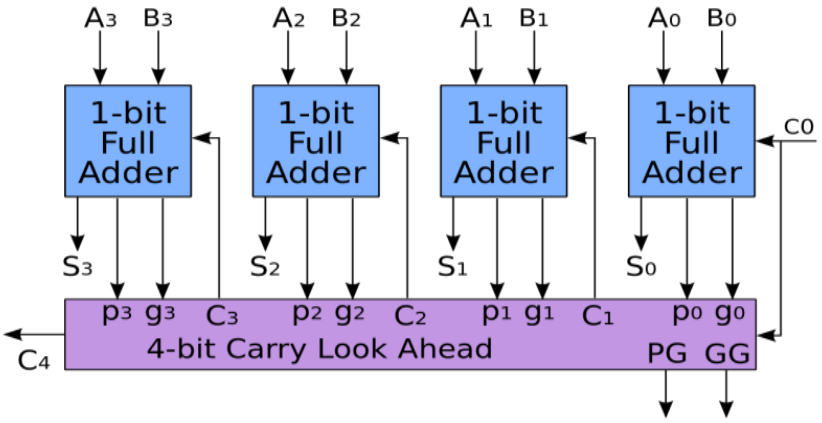


Figure 1.5 Carry Look-ahead Adder

For the reduction of propagation delay of N-bit addition, carry look-ahead adder usually utilize higher bit cells for measuring the carry in parallel. . In general, the carry look-ahead adder using k group of n-bit is

$$\mathbf{Tcla = Tpg + tpg\ (n+ [(n-1) + (k-1)]\ Tao + Txor}$$

1.5 GDI Technique

The basic GDI cell was recommended by Morgenshtein. In the digital combinational circuit, this technique is utilize for the low power consumption. It is very adjustable for digital circuits. The GDI cell consists of three inputs:-G (Common gate input of NMOS and PMOS), P ((input to the source/drain of PMOS) and N (input to the source/drain of NMOS).Bulks of both NMOS and PMOS are connected to N and P respectively.

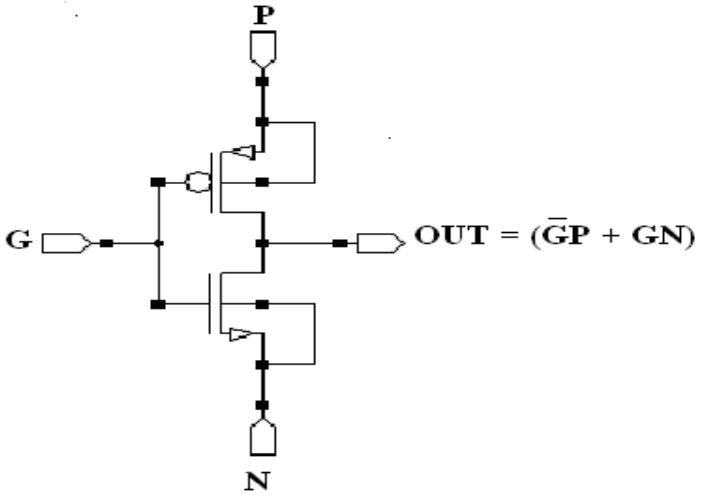


Figure 1.6 Basic cell of GDI

As compared to conventional complementary pass transistor logic, the Gate Diffusion Input technique is used to implement for increasing the spped and consumption of power in the circuit by usimg the logic operations.

N	P	G	OUTPUT	FUNCTION
0	1	A	A`	INVERTER
0	B	A	A`B	F1
B	1	A	A`+B	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	A`B+AC	MUX
B`	B	A	A`B + B`A	XOR
B	B`	A	AB +A`B`	XNOR

Table1.2 Logic function of the basic GDI cell

Table-1 shows the logic functions which is implemented by using the Gate Diffusion Input logic based on the various input values. In the Complementary Metal Oxide Semiconductor and the Gate Diffusion Technique, the prime difference is that in the Gate Diffusion Input Technique the Voltage drain-to drain source is not attached with the PMOS as well as the Ground is not attached to the NMOS which makes the Gate Diffusion Input circuit flexible.

1.5.1 Advantages of GDI over CMOS

- Power Circuit Design is less
- Propagation Delay is reduced
- Power Consumption is reduced
- Area of Digital Circuit is reduced
- Low Complexity of logic design is maintained

1.5.2 Advantages of GDI Technique

- Power Dissipation is optimized.
- Transistor count is reduced.

- This technique is applicable for low power designs, fast in comparison with the complementary metal oxide semiconductor.
- It is also used to improve the power characteristics in a circuit.

1.6 Adiabatic Logic

Adiabatic circuits are considered for the power consumption in the circuits, utilize **"reversible logic'** to consume energy. Adiabatic logic is applicable on the theory of the switching activities which is used to decrease the power. Therefore we can say that in Very large Scale Integration Circuit the "Adiabatic Logic" is used for the low-power consumption in the circuit which implements the reversible logic. There are two main rules in adiabatic logic through which we can reduce the power in the circuit which are:-

- When there is a Voltage Potential between the Source and Drain, never turn ON the transistor.
- When current is flowing through it, never turn OFF the transistor.

In adiabatic logic, the power clock plays a crucial role in the principle of operation. Every phase of power clock provides the user to get three major aspects architecture rules for adiabatic logic circuit design is:-

- If VDS>0 never turn ON a transistor.
- If IDS ≠ 0, never turn OFF a transistor.
- Through a diode never pass current.

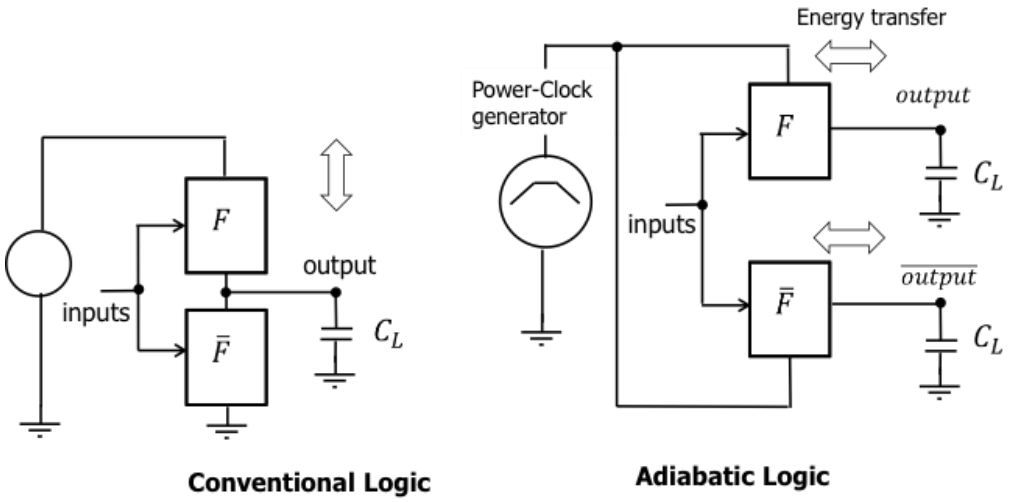


Figure 1.7 Schematic Diagram of Adiabatic Logic

1.6.1 ECRL Logic Design

In the adiabatic logic circuit architecture, the Efficient Charge Recovery Logic is suggested for the low-energy. Charge Recovery Logic is based on the ECRL when it compare with the conventional circuits because it receives the high power. In terms of Power consumption as well as the security manner, ECRL is one of the best adiabatic logic architecture among all the adiabatic logic circuits.

Therefore, it can be used for the power consumption and for increasing the speed in the digital circuits.
ECRL gates composed of PMOS loads and NMOS pull-down transistor. The figure of the ECRL Inverter is shown below:-

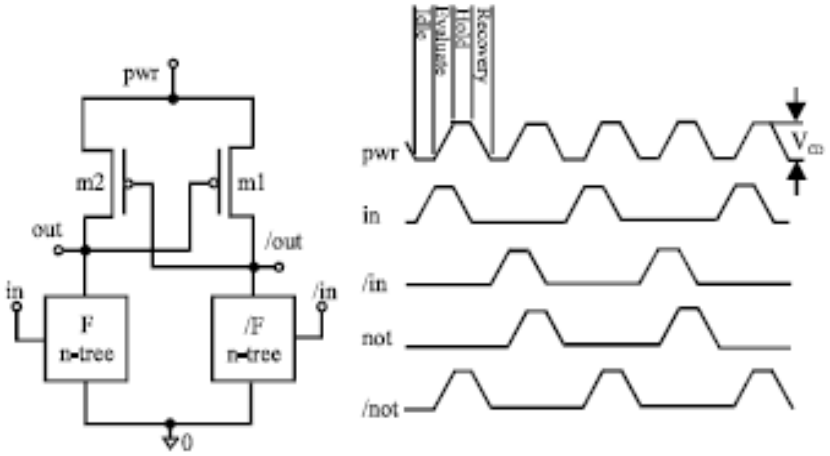


Figure 1.8 ECRL Inverter

1.6.2 Pros and Cons of ECRL Logic Design

- Slower than the conventional CMOS
- It require the special power supply
- Less Power if high switching activity or disconnect system from power supply while idle (sleep transistor).
- Require more area.

1.7 Domino Logic

Domino logic is depend on CMOS which is based on the dynamic logic techniques depend on either PMOS or NMOS transistor. It confess a rail-to-rail logic swing. It is utilized to increase the speed in the circuit. Domino logic architecture is generally used to develop the speed in the circuit as compare to the static logic architecture. For parity checker, comparator as well as the multiplier, full adder has the basic component for the arithmetic operations.
There are two main logic aspects for the designing a full adder:-

- Static full adder
- Dynamic full adder

Due to the consumption of minimum area of silicon, the dynamic full adder is faster as well as more compact. It also absorbs not only more power but also more susceptible to the noise in comparison to the static full adder. It confess a rail-to-rail logic swing. It is utilized for increasing the speed in the circuit. Domino logic architecture is generally utilized to develop the speed in the circuit as compare to the static logic architecture. For parity checker, comparator as well as the multiplier, full adder has the basic component for the arithmetic operations. To design an adequate full adder, there are lots of parameters which plays a very prominent role i.e. low power consumption and performance in circuit, area, noise, number of transistor count, noise immunity and good driving capacity.

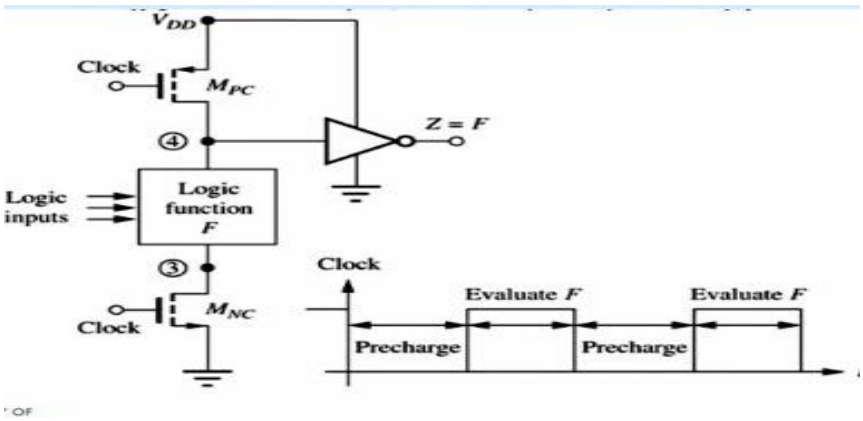


Figure 1.9 Dynamic Domino CMOS Logic

1.7.1 Features of Domino Logic

- They have the smaller areas than the conventional CMOS logic.
- Parasitic Capacitance so that high operating speed is possible.
- Due to the presence of the inverting buffer, only non-inverting buffer are possible.
- Charge distribution may be a problem.

1.7.2 Drawbacks of Domino Logic

In domino logic, the pre-charge "1" state of the prime gate may effects the second gate to discharge soon, therefore the prime gate has reached its appropriate state. This utilizes up the "pre-charge" of the second gate which can be able to store again till the next clock cycle, so there will not be any recovery from this error.

In procedure of the cascade dynamic logic gates, one of the explanation is Dynamic logic, which include the simple static inverter among all the stages. Although it might be the failure of the concept of dynamic logic, since the inverter possess the P-FET. One of the main goal of dynamic logic design to avoid the P-FET is speed. There are two main reasons through which dynamic logic works such as:-

- There is no fan-out in the multiple P-FET so the dynamic logic gets easily connects to one inverter so that the gate works at very high speed. Furthermore, in dynamic logic design the inverter gets only connect with the N-FET so it work too fast.
- In an inverter, the P-FET can be made smaller in comparison with the some types of the logic gates.

1.7.3 Problems of Domino Logic Gates

- During the pre-charge phase, the output voltage is maximum.
- Once an output node has been discharged, it cannot go high until the next pre-charge phase.

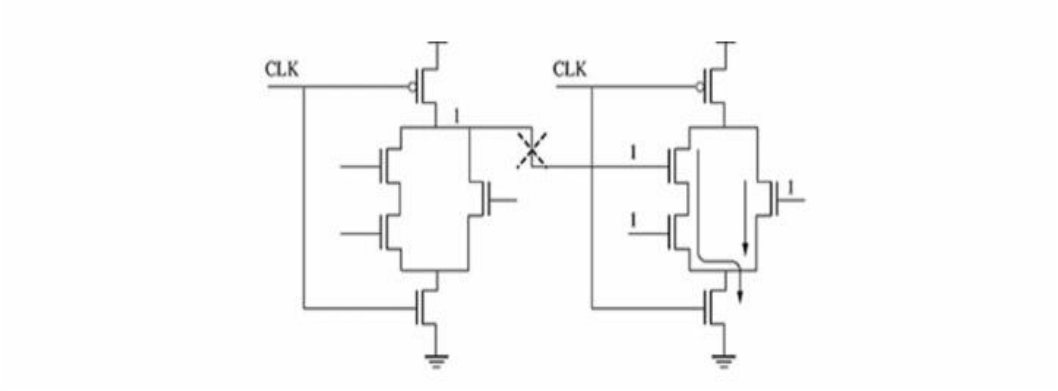


Figure 1.10 Problems in Domino Logic Gates

1.8 Hybrid Logic

Full Adder circuits is used for the addition of 1-bit binary numbers i.e. C A B as an input and two 1-bit binary numbers i.e. SUM and CARRY as an output. The expression of Full Adder is mentioned below:-

S= A XOR B XOR Cin

Cout =A.B + Cin (A XOR B)

Hybrid CMOS logic architecture utilize more than single module for the architecture of full adder. The General form of Hybrid CMOS logic design architecture is given below:-

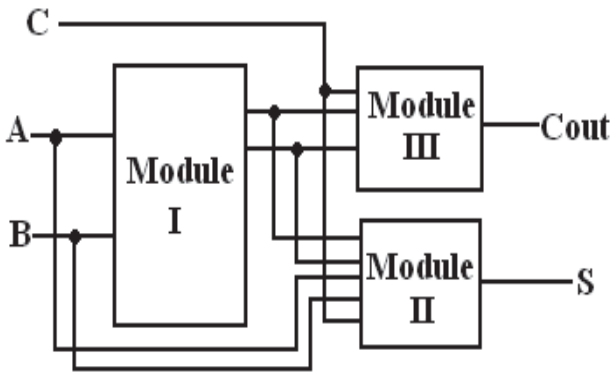


Figure 1.11 General form of Hybrid CMOS Logic Design

The circuit requires minimum power and gives minimum delay and due to the transistor at the output which is connected to the supply voltage and GND gives the great driving ability. But due to the few sequence of the inputs such as “00” and “11”, it provide quiet higher delay. In hybrid CMOS logic XOR and XNOR is widely used in it. The figure of the XOR/XNOR circuit using Hybrid Logic and the modified XOR/XNOR circuit using Hybrid Logic is given below:-

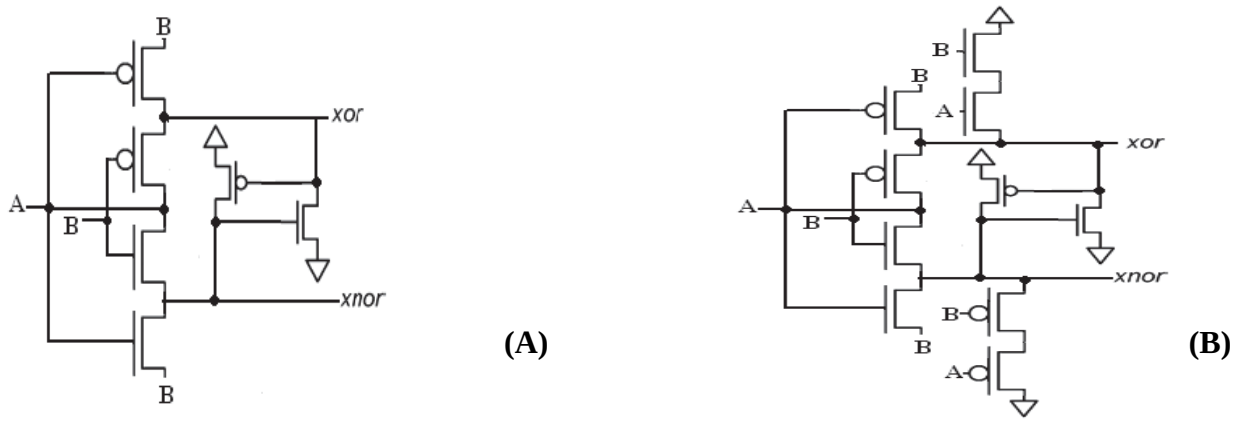


Figure 1.12 (A) -- Basic XOR/XNOR Circuit using Hybrid Logic
(B)—Modified XOR/XNOR Circuit using Hybrid logic

Figure.1.12 (A) represents the 6 transistor and gives complete output swing. In the hybrid CMOS logic architecture Figure.1.12 (A) is widely used. The circuit requires minimum power and gives minimum delay and due to the transistor at the output which is connected to the supply voltage and GND gives the great driving ability. But due to the few sequence of the inputs such as "00" and "11", it provide quiet higher delay.

Figure.1.12 (B) is the upgraded version of the Figure.1.12 (A) circuit. In this Figure.1.12 (B), the pull-up and pull-down transistors utilize to increase the performance of delay in the circuit. Although it is used to increase the performance but the failure of the circuit is used to increase the overall delay.

CHAPTER 2
LITERATURE REVIEW

2.1 Area and Power Efficient Carry Select Adder using 8T Full Adder
B. Sathyabhama, M. Deepika, and S. Deepthi, 2015

In this paper 8T full adder is used as a building block for 8-bit SQRT CSLA. 8T full adder is designed by XNOR hybrid CMOS design. To perform fast arithmetic operations, carry select adder is one of the fastest adders which is used for the processing of data complex.. The SQRT CSLA consists of 8T XNOR full adder. By using the Pass Transistor Logic, 8T XNOR full adder is performed. SQRT CSLA is constructed by equalizing the delay through two carry chains. To achieve low power consumption 8T FA is used as the building block for ripple carry adder. A hybrid CMOS full adder with 8T is constructed by using 3T XNOR circuit. Since XNOR consists of 3 transistors only. Figure.2.1, shows the 3T XNOR circuit. This 3T XNOR is designed using pass transistor logic (PTL). It is a highly compact design. XNOR operation is performed twice in 8T full adder and by using multiplexer, sum and carry were determined. The key factor for high speed design is the number of P-transistors should be less than N-transistor.

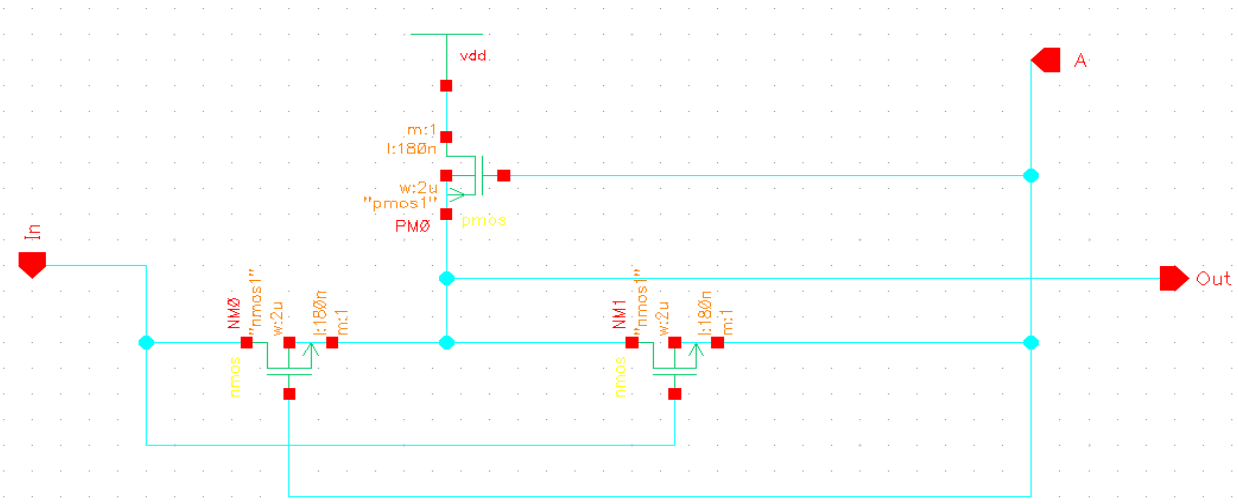


Figure.2.1 3T XNOR Circuit

In the Fig.2.2. Circuit 8T full adder is shown. This 8T full adder is used in Ripple Carry Adder (RCA) block of the 8-bit SQRT CSLA. The Boolean expression of sum and Carry of the full adder is given below:-

Sum = ((A+B) + C)

Carry = (A.B) + [(A+B).C]

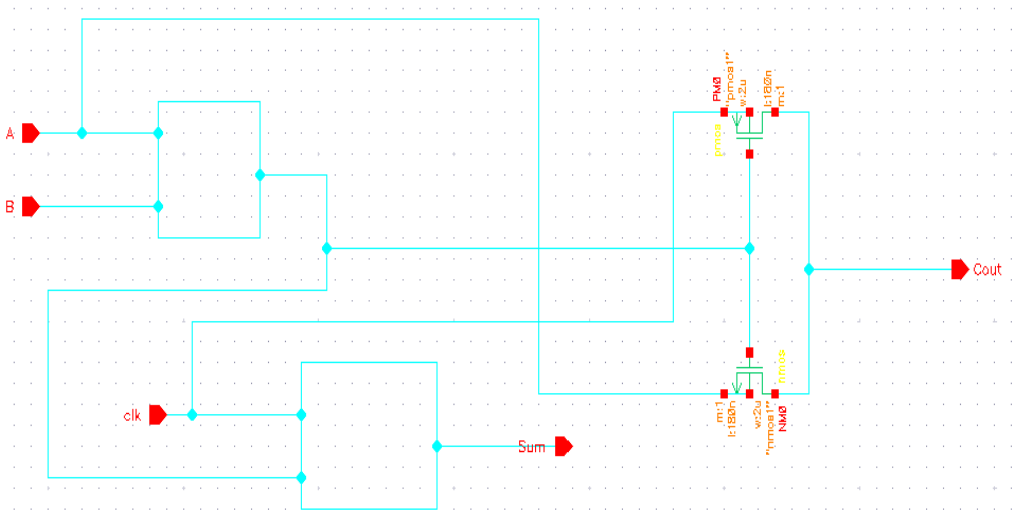


Figure.2.2 8T Full Adder Circuit

2.2 A Competent Design of 2:1 Multiplexer and Its Application in 1-Bit Full Adder Cell

Amit Dubey Sachin Dubey Shyam Akashe, 2012

In this paper, an architecture of 2:1 Multiplexer has been proposed. As we know that Multiplier is also known as MUX. In terms of consumption of power, temperature, delay and load capacitance of output, MDCVSL gives the good result by the addition of double weak P channel. In terms of delay, consumption of power and load capacitance of output the modified multiplexer of DCVSL 2:1 gives the better result. In the MDCVSL, the connection of six NMOS and the four PMOS is done and single addition of supply is utilized on the circuit for switching. VPULSE is connected on every input port out of six input on which we find out the fall time, rise time, voltages V1 and V2, time period and width of pulse and Z and Zb is connected at the two output port and at the ground port GND is connected in the circuit.

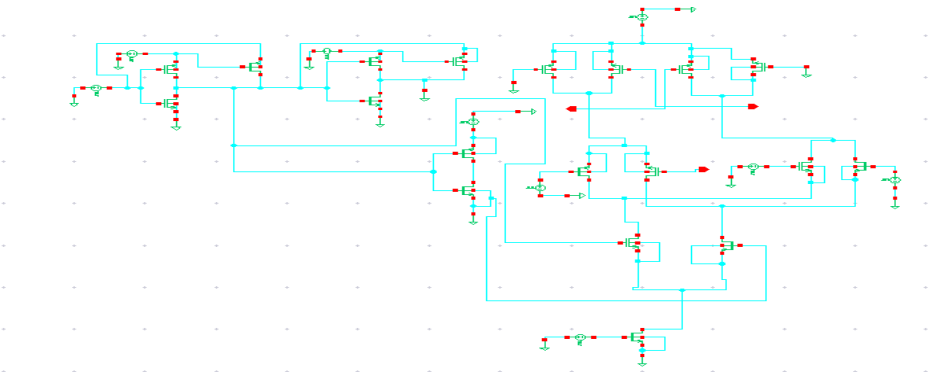


Figure.2.3 Adder Circuit using MDCVSL

2.3 1-Bit Hybrid Full Adder by GDI and PTL Technique

Kshitij Shant, Rita Mahajan, 2016

In this paper 1 bit full adder hybrid circuit has been proposed which consist of two techniques i.e. Pass transistor Logic and Gate Diffusion Technique. A single bit full adder cell is designed to represent the efficiency of the proposed architecture. For the designing of low power the method (GDI and PTL) is used. The typical complication in PTL and GDI technique is that the swing output is less because the Vdc is not included in the Gate Diffusion Input as well as the Pass transistor Logic. In conclusion of Power dissipation and delay it analyzed that the performed data of adder of hybrid is varies in between the PTL and the GDI. On increasing the supply voltage of input, the characteristics of hybrid adder also changes. Due to the deficiency of voltage source (Vdc), the GDI and PTL do not produce the output of full swing. On increasing the supply voltage of input (Vp) extra voltages is required for the transmission from input to output through which the other transistors can easily executed.

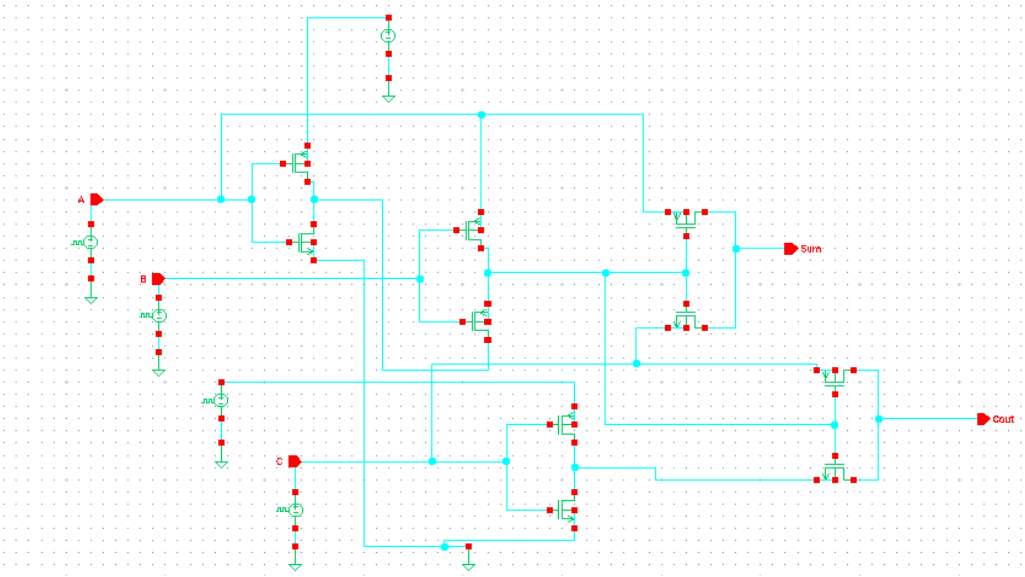


Figure.2.4 1-Bit Hybrid Full adder Circuit

2.4 Low Power Technique in Domino Logic Circuit

Neha Vaish, Sampath Kumar V, 2015

In this paper, a new procedure is for diminishing the power absorption and developing the speed beyond reacting the noise margin is reviewed. In this paper, a technique of threshold voltage of the keeper transistor is diverse utilizing body bias generator circuit. In this paper, 3 different body bias generator circuits are implemented which are:-

- Dynamic Body Bias Generator
- Capacitive Body Bias Generator
- Cross Couple Capacitive Body Bias Generator

For carry look-ahead adder, simulations are done on tanner EDA tool at 65nm as well as 180nm technology. The simulations output read presents that Capacitive Body Bias Generator (CBBG) and cross couple capacitive body bias generator (CCCBBG) decreased less power consumption and propagation delay as compared with another circuit architectures. In this paper, the dynamic

body bias generator with double supply voltages develops the keeper transistor's threshold voltage by changing the substrate biasing of the keeper transistor. Dynamic body bias generator with triple supply voltage develops body bias voltage for the keeper transistor decreasing the power absorption beyond reacting noise margin. Capacitive body bias generator changing the voltage of capacitance C develops variable body bias voltage and it also develops a voltage which is two times more than the applied voltage.

2.5 Analysis of Full Adder using Adiabatic Charge Recovery Logic

Amalin Marina, S Shunbaga Pradeepa T, Dr. A Rajeswari, 2016

This paper shows the correlative study of full adder utilizing various adiabatic logic architecture. Power analysis is executed at 45nm for various frequencies and output represents that at less frequencies Efficient Charge Recovery Logic (ECRL) absorbs 69% minimum power as compared it with the conventional CMOS logic design whereas at higher frequencies the power consumption of Secured-Quasi Adiabatic logic possess 71.8% lesser as compare it with the CMOS.

SQAL is the advancement over ECRL. Analysis represents that the ECRL is capable at less frequencies as well as it represents minimum in power of 68% in comparison with CMOS whereas SQAL is more capable at maximum frequencies and it represents the decrease in power of 71%in comparison with conventional CMOS logic style.

For architecture of full adder there are two relationship accesses which are:

- Static
- Dynamic

A dynamic full adder is faster and more compact, consumes less silicon area, but it consumes more power and more sensitive to noise as compared to static full adder. That's why for designing a 1-bit full adder cell, we use domino logic style and after comparison with the static logic which is depend on 28T full adder cell and 10T full adder cell and also correlated with the 27T domino full adder cell. The architecture of 1-bit 22 Transistor is shown below:-

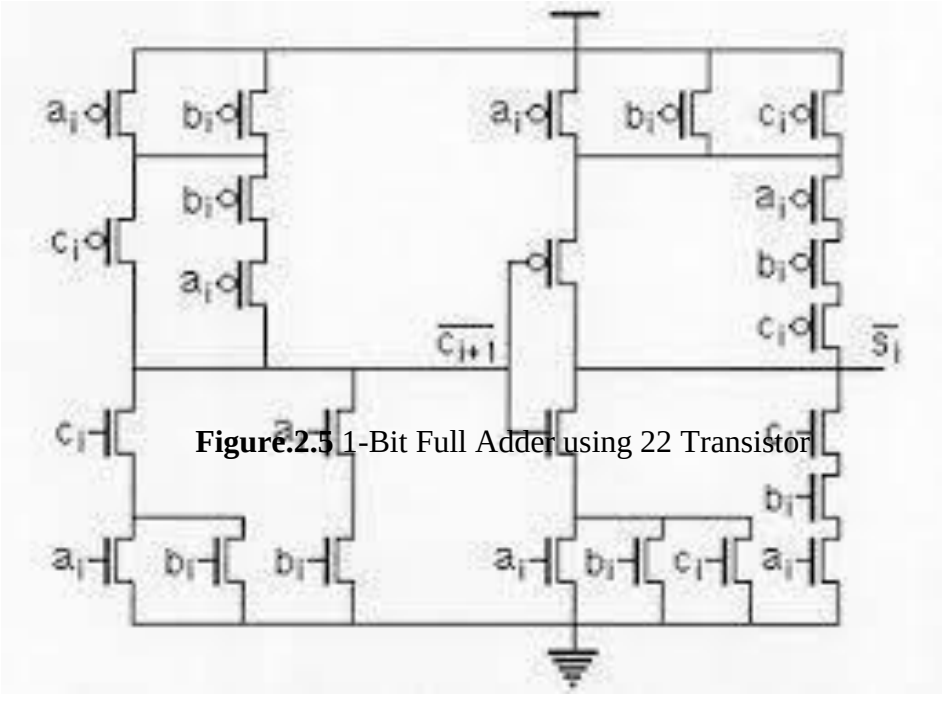


Figure.2.5 1-Bit Full Adder using 22 Transistor

2.6 Modified Positive Feedback Adiabatic Logic for Ultra Low Power Adder

Shiv Pratap Singh Kushawaha, Trailokya Nath Sasamal, 2016

This paper recommend Modified Positive Feedback Adiabatic Logic (MPFAL) which is utilize for ultra-low-power circuits. MPFAL is depend upon positive DC voltage ranging from 0.1V-0.3V. Half Adder and 1-bit full adder consolidate this technique used for the low power circuits. After compared between these two techniques, we concluded that the average power is minimized in case of Modified Positive Feedback Adder as compared to the Positive Feedback Adiabatic Logic All the simulations are executed in Cadence Virtuoso Tool utilizing UMC 180nm CMOS Technology. This technique can be utilized in ultra-low power digital circuits executed in maximum frequencies.

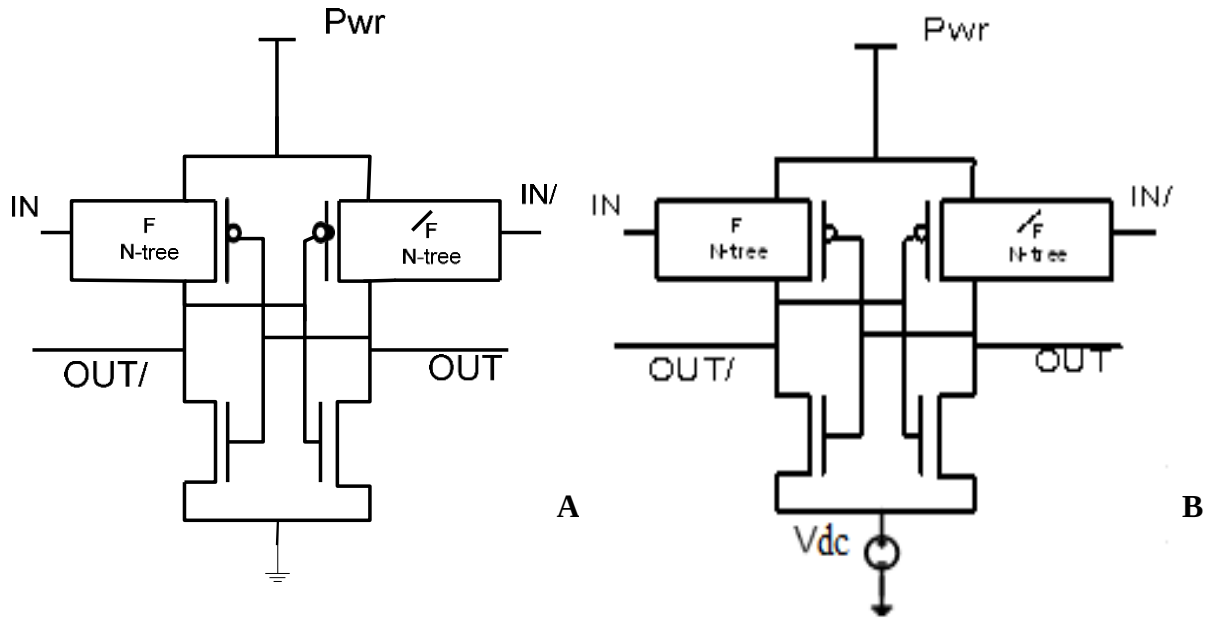


Figure. 2.6 A—PFAL Inverter, **B—**Modified PFAL Inverter Circuit

2.7 Energy Efficient Low Power High Speed Full Adder design Using Hybrid Logic

M Nikhil Theja, Dr T Balakumaran

In this paper, hybrid logic architecture utilize to construct the full adder. The prime goal of this architecture is, complete maximum speed as well as minimum power. Hybrid logic style utilize the combination of C-CMOS logic (Complementary Metal Oxide Semiconductor) and Transmission Gate (TG) logic. The circuit was appliance using Micro-wind tool in 90nm as well as 180nm Technology. Average power absorption of the proposed architecture is organized to 1.114W at 90nm technology for 1.2V supply and 5.641W at 180nm for 1.8V supply. Delay in the signal propagation is calculated as 0.011ns and 0.087ns for 90nm and 180nm technology. Thus absorbing extremely low power and depend upon minimum time in comparison to the existing architecture for the double testing status. Power delay product (PDP) is measured as product of Power and Delay digits represent energy demand of the architecture. Proposed architecture needs

71% minimum energy in comparison to TFA and 81% minimum energy than TGA and 92% minimum energy in comparison to conventional CMOS-adder.

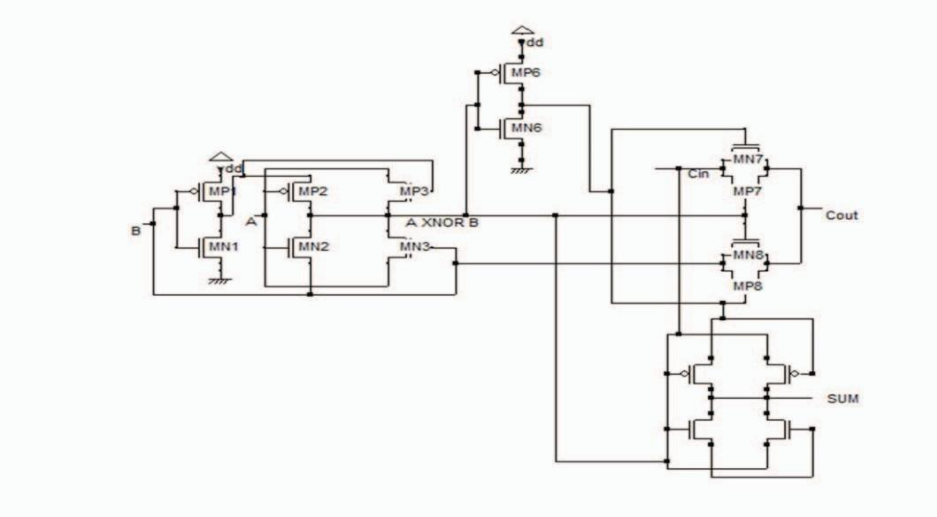


Figure.2.7 Full Adder Design with Integrated Sum and Carry Module

Energy efficiency of the proposed hybrid logic architecture is measured in terms of PDP. C-CMOS needs 92% more energy in 90nm technology and 83% more energy in 180nm in comparison to hybrid logic design. TGA needs 89% more energy in 90nm technology and 81% more energy in 180nm technology in comparison to hybrid logic. TFA needs 83% needs more energy in 90nm whereas 71% more energy in 180nm technology in comparison to hybrid logic. In this way, hybrid logic considered as the most energy efficient logic architecture.

2.8 Adiabatic Logic: An Alternative approach to Low Power Application Circuits

Preeti Bhati, Navaid Z. Rizvi, 2016

In this paper, there is a comparison between PFAL Logic and CMOS Logic is executed at various voltages and frequencies. PFAL is also known as Partial Energy Recovery Circuit because it possess a great robustness. It is also known as the dual-rail circuit. The architecture of PFAL circuit is shown below:-

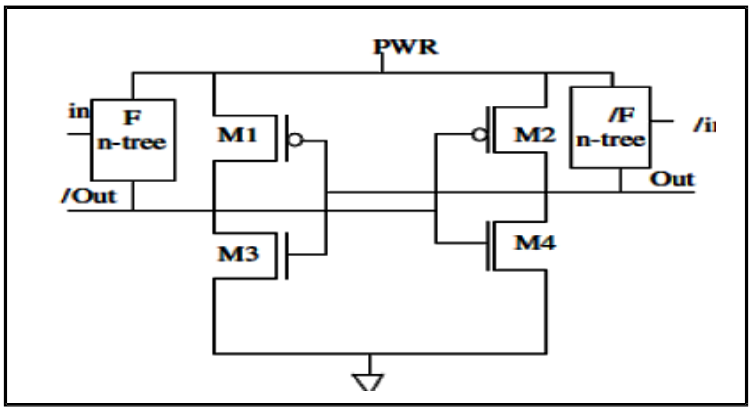


Figure.2.8 Basic PFAL Architecture

In this paper, 1-bit sum and carry adder are fabricated and simulated on CADENCE VIRTUOSO using 180nm Technology. The Adiabatic logic has become a solution of the question of power

dissipation. The proposed technique represents the minimization of power dissipation in comparison with the conventional CMOS architecture style switching events. We concluded that the power dissipation in PFAL is less as compare with the conventional CMOS logic circuits. PFAL logic architecture shows the significant power minimization and gives the better performance results as compared with the conventional CMOS logic. Although PFAL go through the great switching period, therefore it is not suitable when the delay is critical.

CHAPTER 3
SCOPE OF STUDY

3.1 Objectives

To develop the performance of VLSI circuits the size of the transistor is reducing which result not only in the circuit power consumption as well as it develop the complexity of the chips. In today period, designing of the less power consumption and the and high speed achievement has become a major issue in the VLSI circuits. Also, we have to reduce the power as well delay in the circuit at the same time.

The increased utilize of electronics equipment's has made power dissipation a crucial parameter in the modern electronics. Electronic devices that work for utilizing a battery has the limited supply of the battery. Up till now, power consumption in a circuit was not the biggest issue because cooling techniques has the capacity of consuming the produced heat. Although due to continuously developing intensity as well as the density of the chips in the system cause obstruction of providing the appropriate cooling. Accordingly, it add appropriate price to the system. That is because we need a circuit who gives a low power consumption even if a numerous components are fabricated over a single chip.

- To design and analyze the Basic operations of GDI, PTL, Domino and Adiabatic Logic
- To reduce low power in the circuit
- To reduce the Propagation Delay in the circuit.
- To work on the size of the circuit.
- To compare the proposed design with other existing techniques.

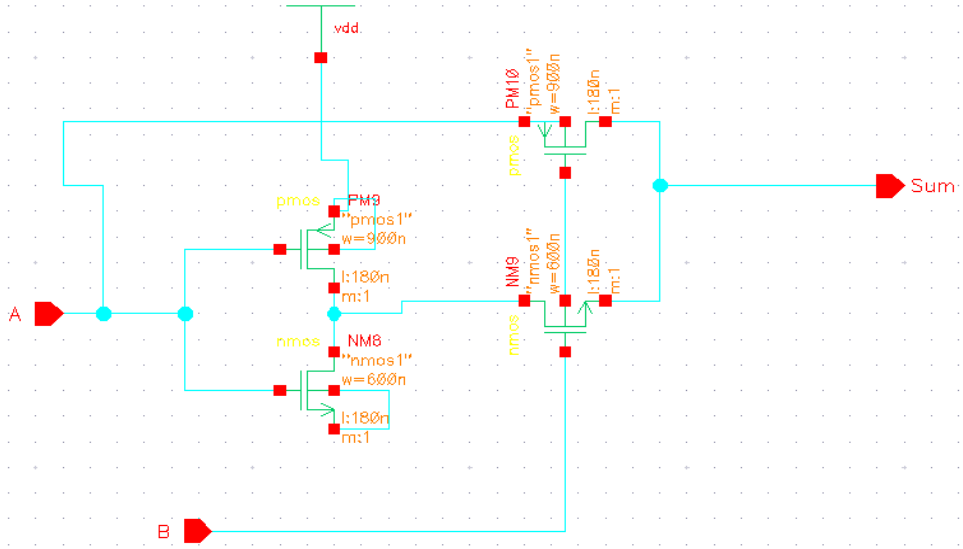
3.2 Problem Formulation

Power dissipation and delay in the circuit are the two main issues which we as a VLSI design engineers are facing today. In this, we proposed a single bit hybrid full adder circuit which consist of two techniques i.e. Gate Diffusion Input (GDI) technique and Pass transistor Logic (PTL) technique. In last few decades there is significant development in the scenario of design. Adder which is considered to be basic blocks of applications like Arithmetic Logic Unit, Digital Signal Processing and Microprocessor have been under scrutiny now or then. We observed that the common problem in both Gate diffusion Technique and the Pass Transistor Logic is the low swing output because both the techniques don't include voltage source Vdc.

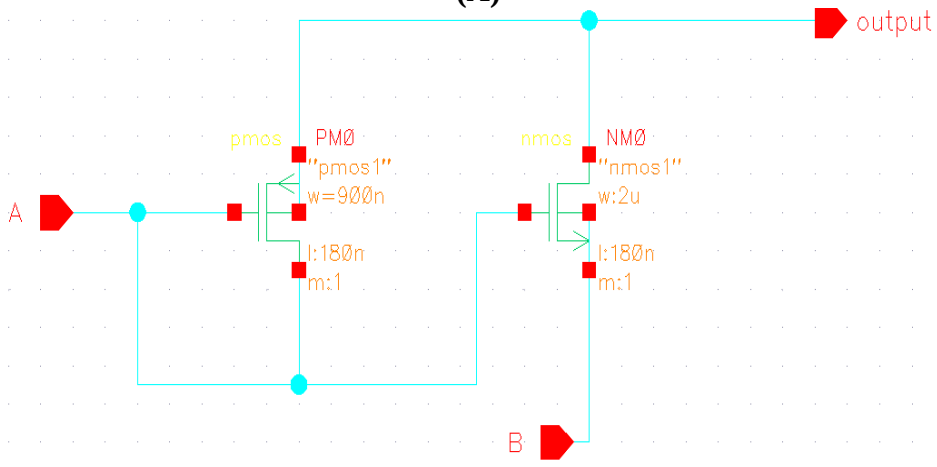
CHAPTER 4
DESIGN PROCEDURE OF HYBRID FULL ADDER

4.1 Pass Transistor Logic (PTL) based XOR Gate and AND Gate

The XOR and AND is very useful circuit that can be utilize in many different types of the computational circuit. In this the width of PMOS is 900n M and the width of the NMOS is 600n M. The schematic diagram of Pass transistor Logic based XOR and AND gate is shown below:-



(A)

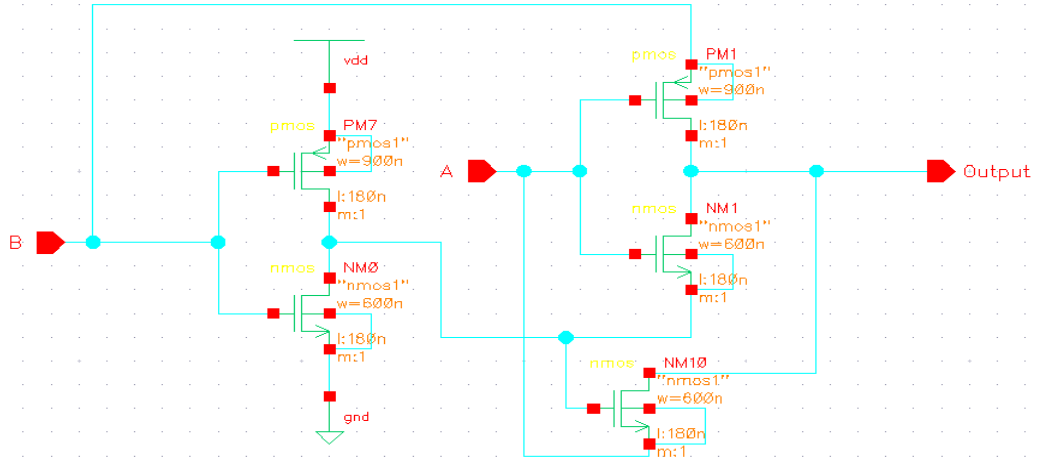


(B)

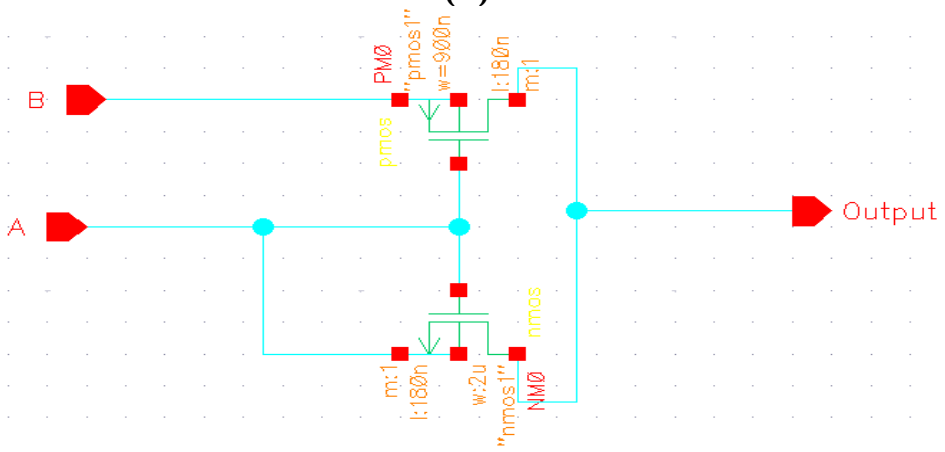
Figure.4.1 (A) PTL based XOR Gate
(B) PTL based And Gate

4.2 Gate Diffusion Input (GDI) based XOR Gate and OR Gate

While making the GDI based XOR gate and OR gate the width of PMOS and NMOS is 900n M and 600n M respectively. The schematic diagram of GDI based XOR gate and OR gate is shown below:-



(A)



(B)

Figure.4.2 (A) GDI based XOR Gate
(B) GDI based AND Gate

4.3 Schematic Diagram of Single-Bit Hybrid Full Adder Cell on the combination of Gate Diffusion Input (GDI) and Pass Transistor logic (PTL)

In this, the width of PMOS and NMOS is 900n M and 600n M respectively at the supply voltage of 1.8 V. The schematic diagram of single bit hybrid full adder cell using the combination of Gate Diffusion Input and Pass Transistor Logic is given below:-

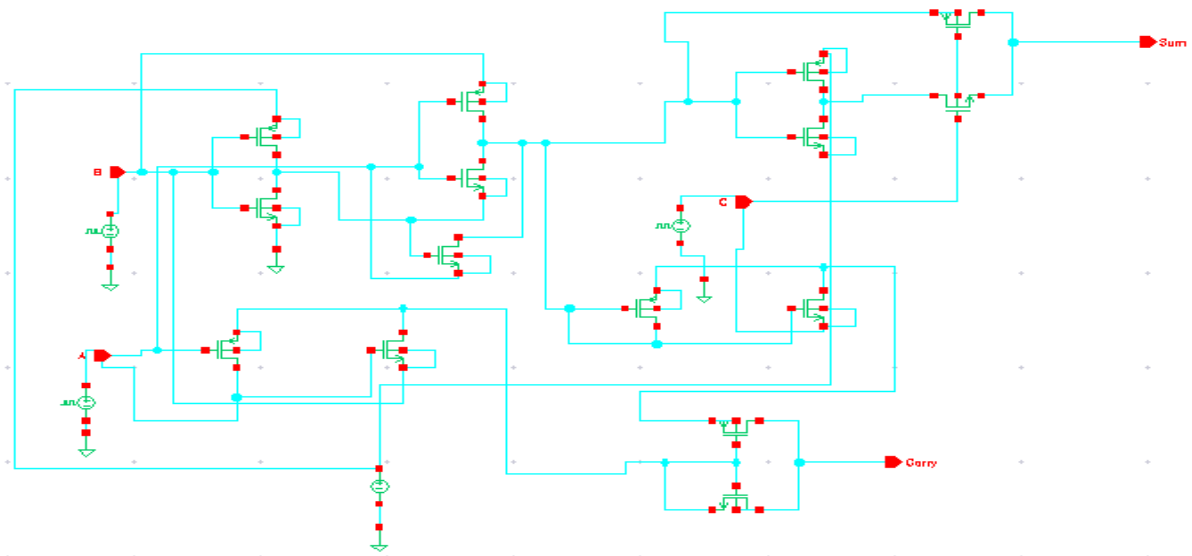


Figure.4.3 Single bit Hybrid Full Adder Cell using the combination of Gate Diffusion Input and Pass Transistor Logic

While making the single bit Hybrid Full adder Cell using the combination of Gate Diffusion Input and Pass Transistor Logic, the specification that take on different input are:-

Name	V1	V2	Pulse Width	Period
A	0	1.8V	20n s	10n s
B	0	1.8V	20n s	10n s
C	0	1.8V	20n s	10n s

Table 4.1 Specifications on hybrid Full adder Cell using the combination of Pass transistor Logic and Gate Diffusion Input

4.3.1 Transient Analysis

The Transient Analysis of single bit hybrid full adder cell on the combination of Gate Diffusion Input (GDI) and Pass Transistor logic (PTL) is shown below:-

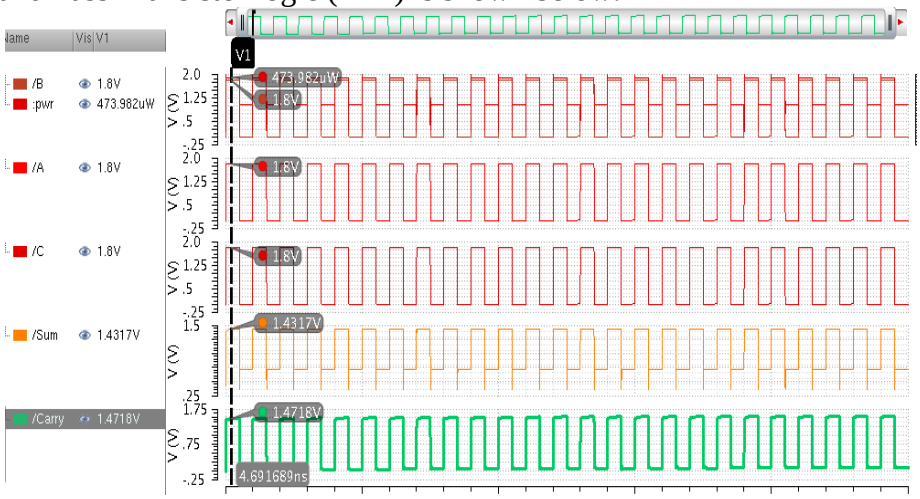


Figure.4.4 Transient Analysis of Single-Bit Hybrid Full Adder Cell on the combination of PTL and GDI

4.3.2 Comparison between Power and Voltage

The comparison between Power and Voltage of single bit hybrid full adder cell on the combination of PTL and GDI is shown below:-

Circuit design	Supply Voltage	Power consumption	Transistor Count
Hybrid Full Adder Cell	1.8V	473.982uW	15

Table 4.2 Comparison between Power and Voltage

4.3.3 Comparison between Delay and Voltage

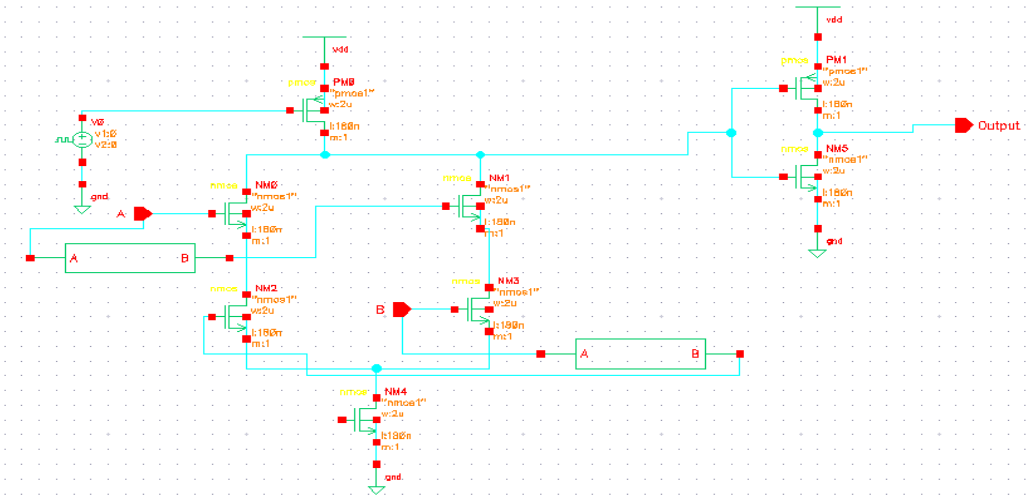
The comparison between Delay and Voltage of single bit hybrid full adder cell on the combination of PTL and GDI is shown below:-

Circuit Design	Supply Voltage	Delay	Transistor Count
Hybrid Full Adder Cell	1.8V	1850ps	15

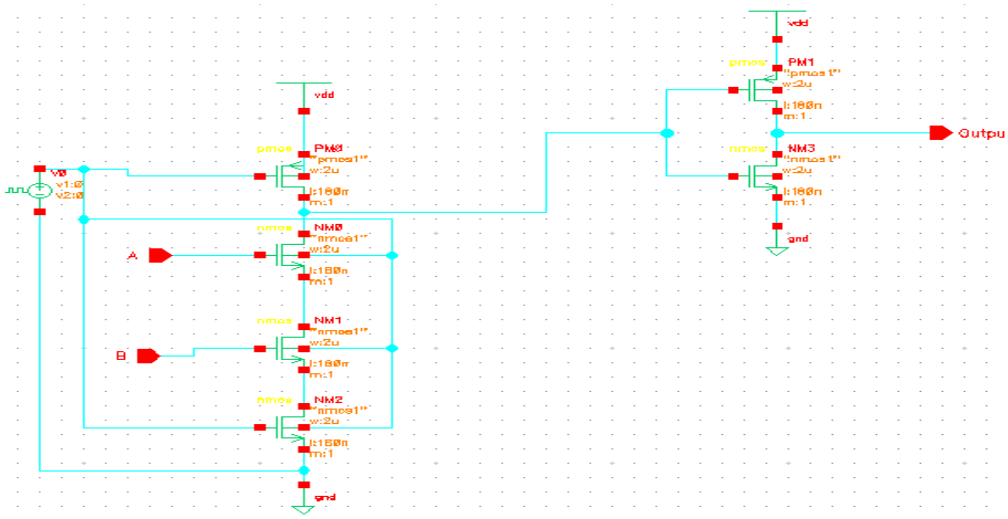
Table 4.3 Comparison between Delay and Voltage

4.4 Domino Logic based XOR Gate and AND Gate

While making the domino logic based XOR gate and AND gate the width of PMOS and NMOS is 900n M and 600n M respectively. The values on "VPULSE" at V1=0V, V2=1.8V, Period=40n s and Pulse Width=20n s. The schematic diagram of domino logic based XOR gate and AND gate is shown below:-



(A)



(B)

Figure.4.5 (A) Domino Logic based XOR Gate
(B) Domino Logic based AND Gate

4.5 Schematic Diagram of 4-Bit Full Adder Cell on the combination of Gate Diffusion Input (GDI) and Domino Logic

In this, the width of PMOS and NMOS is 900n M and 600n M respectively at the supply voltage of 1.8 V. The schematic diagram of four bit full adder cell using the combination of Gate Diffusion Input and Domino Logic is given below:-

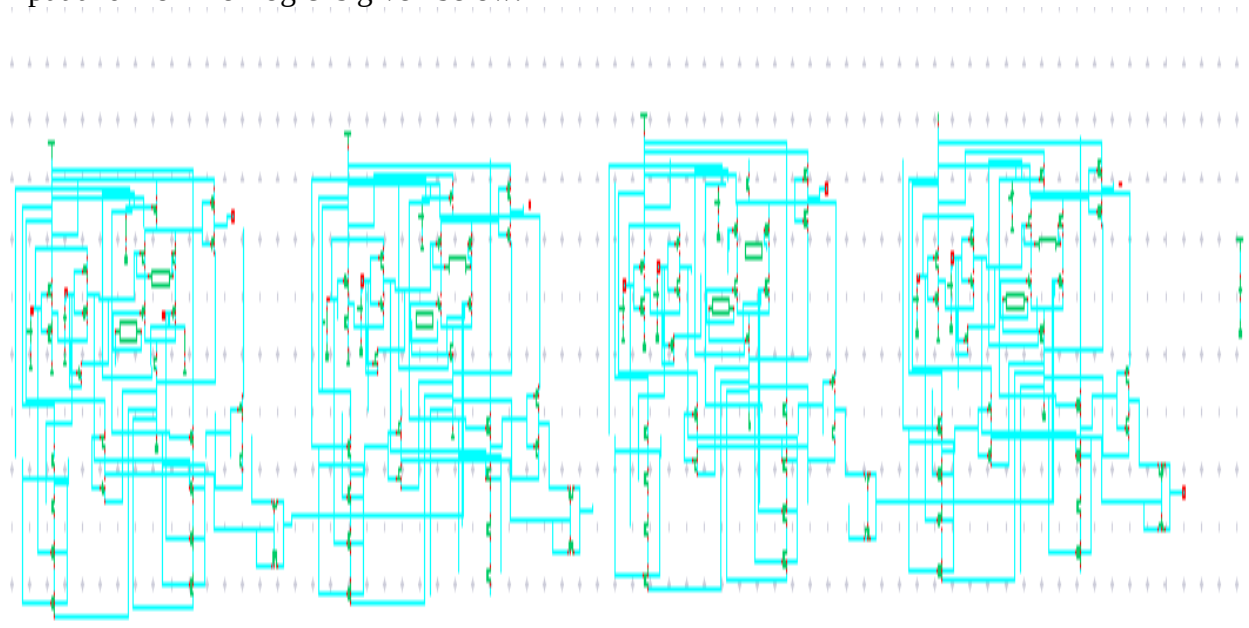


Figure.4.6 Four bit Full Adder Cell using the combination of Gate Diffusion Input and Domino Logic

While making the four bit Full adder Cell using the combination of Gate Diffusion Input and Domino Logic, the specification that take on different input are:-

Name	V1	V2	Pulse Width	Period
A0	1	1	20n s	10n s
B0	1	1	20n s	10n s
A1	1	1	20n s	10n s
B1	1	1	20n s	10n s
A2	1	1	20n s	10n s
B2	1	1	20n s	10n s
A3	1	1	20n s	10n s
B3	1	1	20n s	10n s

Table 4.4 Specifications on hybrid Full adder Cell using the combination of Gate Diffusion Input and Domino Logic

4.5.1 Transient Analysis

The Transient Analysis of four bit full adder cell on the combination of Gate Diffusion Input (GDI) and domino Logic is shown below:-

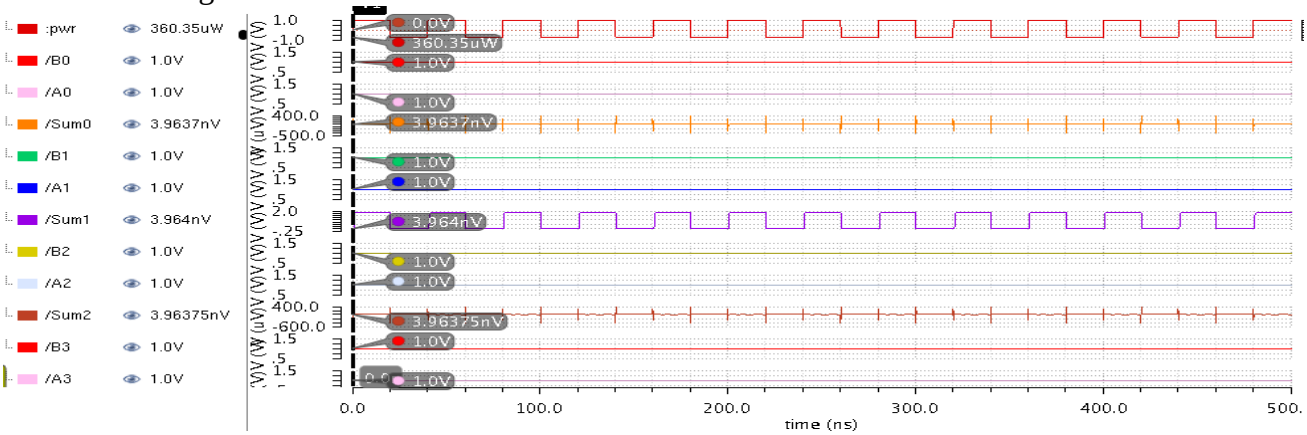


Figure.4.7 Transient Analysis of four Bit Full Adder Cell on the combination of GDI and Domino Logic

4.5.2 Comparison between Power and Voltage

The comparison between Power and Voltage of four bit full adder cell on the combination of GDI and Domino Logic is shown below:-

Circuit Design	Supply Voltage	Power Consumption
Domino Full Adder	1.8V	360.35uW

Table 4.5 Comparison between Power and Voltage

4.5.3 Comparison between Delay and Voltage

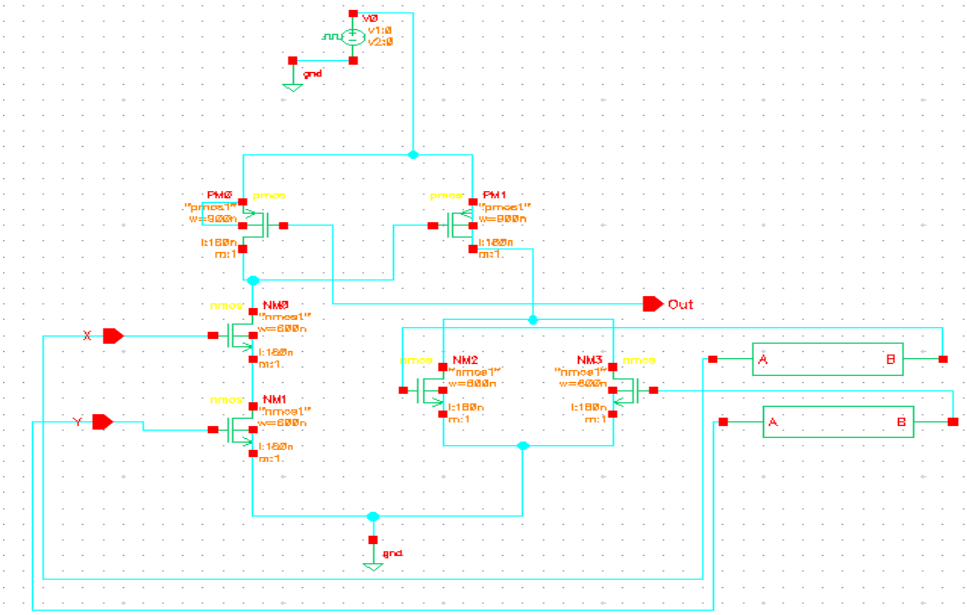
The comparison between Delay and Voltage of four bit full adder cell on the combination of GDI and Domino Logic is shown below:-

Circuit design	Supply voltage	Delay
Domino Full Adder	1.8V	464.7ps

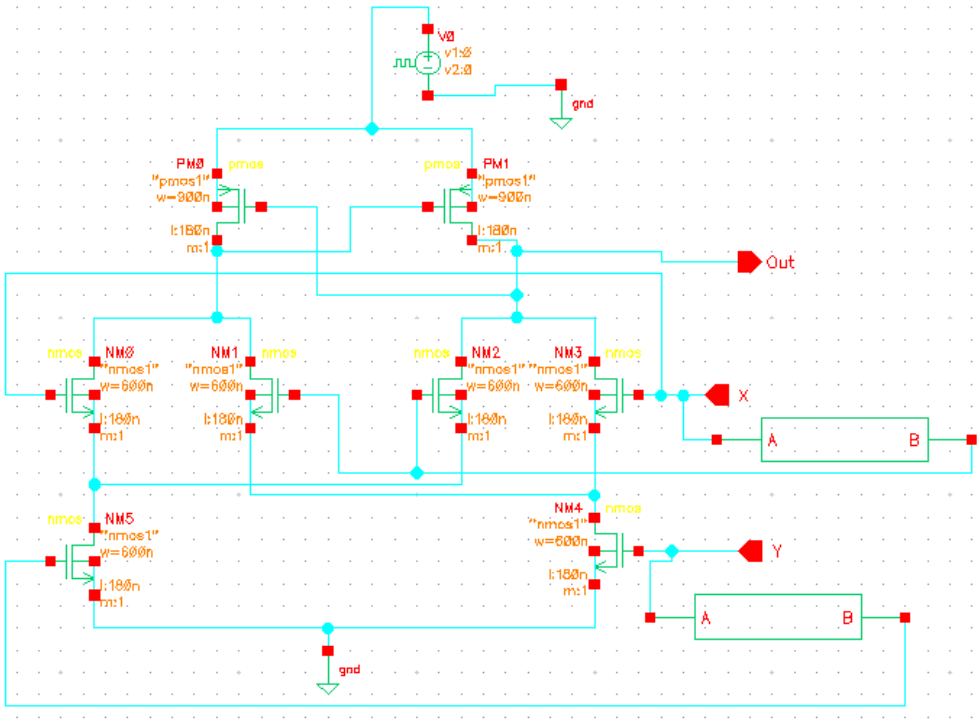
Table 4.6 Comparison between Delay and Voltage

4.6 Adiabatic logic of ECRL based AND Gate and XOR Gate

While making the adiabatic logic of ECRL based XOR gate and AND gate the width of PMOS and NMOS is 900n M and 600n M respectively. The values on "VPULSE" at V1=0V, V2=1.8V, Period=40n s and Pulse Width=20n s. The schematic diagram of adiabatic logic of ECRL based XOR gate and AND gate is shown below:-



(A)



(B)

Figure.4.8 (A) Adiabatic Logic of ECRL based XOR Gate
(B) Adiabatic Logic of ECRL based AND Gate

4.7 Schematic diagram of 8-bit Full adder Cell on the combination of Gate Diffusion Input (GDI) and Adiabatic Logic of ECRL

In this, the width of PMOS and NMOS is 900n M and 600n M respectively at the supply voltage of 1.8 V. The schematic diagram of four bit full adder cell using the combination of Gate Diffusion Input and Domino Logic is given below:-

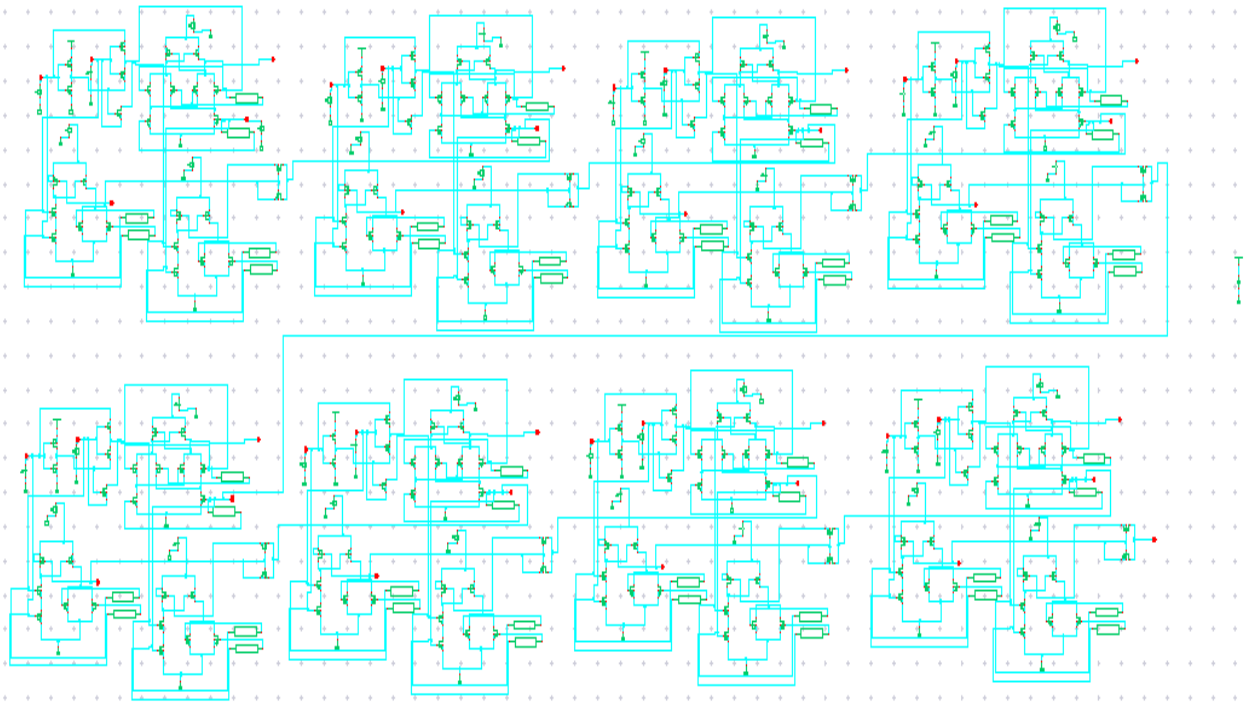


Figure.4.9 8-Bit Full Adder Cell using the combination of GDI and Adiabatic Logic of ECRL

While making the four bit Full adder Cell using the combination of Gate Diffusion Input and Domino Logic, the specification that take on different input are:-

Name	V1	V2	Pulse Width	Period
A0	1	1	20n s	10n s
B0	1	1	20n s	10n s
A1	1	1	20n s	10n s
B1	1	1	20n s	10n s
A2	1	1	20n s	10n s
B2	1	1	20n s	10n s
A3	1	1	20n s	10n s
B3	1	1	20n s	10n s
A4	1	1	20n s	10n s
B4	1	1	20n s	10n s
A5	1	1	20n s	10n s
B5	1	1	20n s	10n s
A6	1	1	20n s	10n s
B6	1	1	20n s	10n s
A7	1	1	20n s	10n s
B7	1	1	20n s	10n s

Table 4.7 Specifications on hybrid Full adder Cell using the combination of Gate Diffusion Input and Adiabatic Logic of ECRL

4.7.1 Transient Analysis

The Transient Analysis of eight bit full adder cell on the combination of Gate Diffusion Input (GDI) and Adiabatic Logic of ECRL is shown below:-

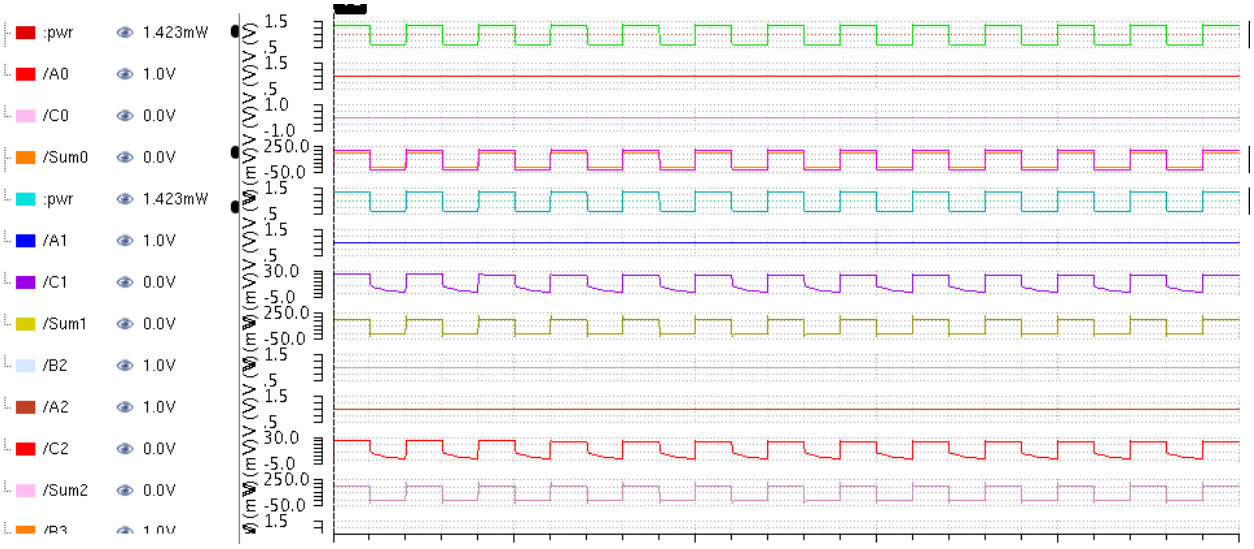


Figure.4.10 Transient Analysis of 8 Bit Full Adder Cell on the combination of GDI and Adiabatic Logic of ECRL

4.7.2 Comparison between Power and Voltage

The comparison between Power and Voltage of 8 bit full adder cell on the combination of GDI and Adiabatic Logic of ECRL is shown below:-

Circuit Design	Supply Voltage	Power Consumption
Domino Full Adder	1.8V	1.423mW

Table 4.8 Comparison between Power and Voltage

4.8 Comparison between Single bit Hybrid Full Adder Cell using the combination of GDI and PTL with different existing Techniques

The comparison between single bit hybrid full Adder cell using the combination of GDI and PTL with different techniques in terms of power and delay is shown below:-

Circuit design	Supply Voltage	Power Consumption	Transistor Count
Hybrid full Adder	1.5V	887.9uW	10
3T XNOR Gate	1.8V	9130uW	11

8T Full Adder	1.8V	805uW	8
Adder using MDCVSL	1.8V	~550uW	10
Modified Hybrid Full Adder	1.8V	473.982uW	15

Table.4.9 Comparison of Power Consumption for Various Circuits

Circuit design	**Supply Voltage**	**Delay**	**Transistor Count**
Hybrid full Adder	1.5	1770ps	10
Adder using MDCVSL	1.8	~1300ps	10
Modified Hybrid Full Adder	1.8	1850ps	15

Table.4.10 Comparison of delay for Various Circuits

4.9 Comparison Between four bit Full Adder Cell using the combination of GDI and Domino Logic with different existing Techniques

The comparison between four bit hybrid full Adder cell using the combination of GDI and Domino Logic with different techniques in terms of power and delay is shown below:-

S.No.	**Technique**	**Supply Voltage**	**Power(uW)**
1.	SDL	1.8V	372.1
2.	DBBG	1.8V	439.4
3.	MT-CMOS Domino Logic	1.8V	1610.1
4.	**Proposed Design**	**1.8V**	**360.35**

Table.4.11 Comparison of Power consumption for various Circuits

S.No.	Technique	Supply Voltage	Delay(ps)
1.	SDL	1.8V	889.6
2.	DBBG	1.8V	384.7
3.	MT-CMOS Domino Logic	1.8V	~750
4.	**Proposed Design**	**1.8V**	**464.7**

Table.4.12 Comparison of delay for Various Circuits

4.9 Comparison Between 8 bit Full Adder Cell using the combination of GDI and Adibatic Logic with different existing Techniques

The comparison between eight bit hybrid full Adder cell using the combination of GDI and Adiabatic Logic with different techniques in terms of power and delay is shown below:-

S.No.	Technique	Supply Voltage	Power
1.	Carry Look-Ahead adder (CLA)	1.8V	5.64mW
2.	8-bit Multiplier using GDI	1.8V	1.5mW
3.	MT-CMOS Domino Logic	1.8V	1610.1
4.	**Proposed Design**	**1.8V**	**1.423mW**

Table.4.11 Comparison of Power consumption for various Circuits

CHAPTER 4
CONCLUSION AND FUTURE SCOPE

4.1 Conclusion

In this single-bit hybrid full adder cell using the combination of the Gate Diffusion Input (GDI) and Pass Transistor Logic (PTL) has been implemented using VIRTUOSO software. For simulation VIRTUOSO and for synthesis VIRTUOSO @6.1.6-64bhas been used. As a result it has been concluded that Single bit full adder on the combination of the Gate Diffusion Input (GDI) and Pass Transistor Logic (PTL) gives optimized result as compared to different existing techniques like 3T-XNOR, 8T Full Adder and Adder using MDCVSL in 180nm Technology. Delay is also reduced in single bit Hybrid full Adder cell using the combination of PTL and GDI. Total Power consumption is also reduced In case of single bit Hybrid Full adder cell in comparison with different techniques like 3T XNOR, 8T Full Adder and Adder using MDCVSL.

In this four bit full Adder cell using the combination of GDI and Domino Logic has also been implemented. . For simulation VIRTUOSO and for synthesis VIRTUOSO ® 6.1.6-64b has been used. As a result it has been concluded that four bit full adder cell using the combination of GDI and Domino Logic gives optimized result as compared to SDL, DBBG and MT-CMOS Domino Logic in 180nm Technology. Total Power consumption is also less in case of four bit full adder cell using the combination of GDI and Domino logic. Delay is also reduced in the four bit full adder cell using the combination of GDI and Domino Logic. And it also gives the better result.

In this eight bit full Adder cell using the combination of GDI and Adiabatic Logic has also been implemented. For simulation VIRTUOSO and for synthesis VIRTUOSO ® 6.1.6-64b has been used. As a result it has been concluded that eight bit full adder cell using the combination of GDI and Adiabatic Logic gives optimized result as compared to CLA and 8-Bit Multiplier using GDI in 180nm Technology. Total Power consumption is also less in case of eight bit full adder cell using the combination of GDI and Adiabatic logic. Delay is also reduced in the four bit full adder cell using the combination of GDI and Domino Logic. And it also gives the better result.

4.2 Future Scope

In future we will utilize the transistor the hybrid adder can also be used in performing a Multiplier, Subtractor, Compressor and the sequential circuits. As the proposed designs have proven to work efficiently in terms of various performance parameters thus; the more effective results are expected to be obtained while incorporating these circuits to implement other complex systems in the field of low power VLSI design.

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