To Fabricate Ag/ZnO/PEDOT:PSS/ZnO/Ag based Memristor and Reliability Testing using Artificial Intelligence Techniques.

Submitted in partial fulfillment of the
Requirement for the award of the Degree
of

MASTER OF TECHNOLOGY IN
Electronics and Communication Engineering

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CERTIFICATE

This is to certify that Keerthipati Thulasiram varma bearing Registration no. 11605395 have completed objective formulation/Base Paper implementation of the thesis titled, " To Fabricate Ag/ZnO/PEDOT:PSS/ZnO/Ag based Memristor and Reliability Testing using Artificial Intelligence Techniques." under my guidance and supervision. To the best of my knowledge, the present work is the result of his original investigation and study. No part of thesis has ever been submitted for any other degree at any university.

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We are also indebted to all authors of the research papers and books referred to, which have helped us in carrying out the research work.

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DECLARATION

I, Keerthipati thulasiram varma, student of M. Tech under Department of Electronics and Communication of Lovely Professional University, Punjab, hereby declare that all the information furnished in this Dissertation-II report is based on my own intensive research and is genuine.

This report does not, to the best of our knowledge, contain part of my work which has been submitted for the award of my degree either of this University or any other University without proper citation.

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ABSTRACT

Memristor so called fourth passive element plays a major role in optimizing the size of circuit and help in creating RRAM(Resistive Random Access Memory) circuit which operate faster than present existing RAM. The thesis work is divided into two halfs, first half deals with studying different types of memristor fabrication methodology using Tio_2 , Zno and PSPICE model of memristor is explained.

Second half deals with methods and advantages of polymer based (PEDOT:PSS) poly(3,4-ethylenedioxythiophene):poly(styrenesulfonate) sandwiched between ZnO layers and two silver layers which act as the electrodes memristor is explained. Artificial Intelligence (A.I) techniques to analyse the performance of the circuit and reliability of the memristor component. This project will increase scope of using low cost polymers materials which acts as the synapse in neuromorphic computing area.

LIST OF ABBREVIATIONS

RRAM/RERAM - Resistive Random Access Memory.

PEDOT:PSS - poly(3,4-ethylenedioxythiophene):poly(styrenesulfonate).

Tio_2 - Titanium dioxide.

Zno - Zinc oxide.

Ag - Silver.

CMOS - Complicated Metal Oxide Semiconductor.

TFET - Tunnel field effect transistor.

MRL - Memristor Ratioed Logic .

MOSFET - Metal oxide semiconductor field effect transistor.

SRAM - Static random access memory.

DRAM - Dynamic random access memory.

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CHAPTER - 1

Introduction:

Prof. Leon O. Chua presented the concept of Memristor in the year of 1971, Relating magnet flux linkage and electric charge , where i= $\frac{dq}{dt}$ and v= $\frac{d\Phi}{dt}$. The mathematical flux while relations explains the memristor electrical resistance based on the previously flowed current through the it, This explains the non-volatility property of memristor. Another perspective of the memristor is the functional slope of a two-terminal passive element whose functional relationship between the time integral of voltage and current.

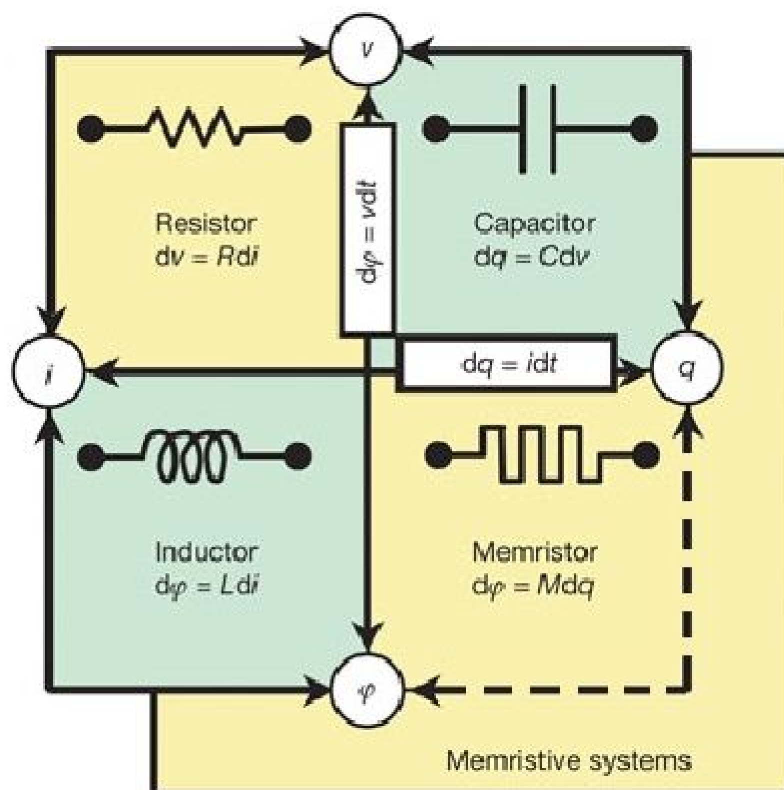

Figure 1.1 : electrical properties of passive components.

Image courtasy of : J.J Yang/HPLabs

Flux is function of charge $\phi = F(q)$ differentiating on both sides we get

$$\frac{d\phi(q)}{dt} = \frac{F(q)}{dt}\frac{dq}{dt} \quad (1)$$

Chua presented new equation by replacing $\frac{F(q)}{dt}$ with $M(q(t))$ where M represents memristor, $\frac{d\phi(q)}{dt}$ derivative of flux with voltage and $\frac{dq}{dt}$ derivative of charge with current.

$$v(t) = M(q(t))i(t) \quad (2)$$

Memristor units is Ω ohms its resistance depends on current passed through it.
Similar to memristor, mem conductance equation can be derived by considering flux function in inverse form, $q = F^{-1}(\phi)$ [1][2].

$$i(t) = M(q(t))v(t) \quad (3)$$

Advantages like non-volatile and low-power, Attracting several research fields like neuromorphic systems to mimic biological neurone systems and analog computation. In 2008 HP Labs observed memristor properties using titanium Dioxide sandwiched between platinum conductors[3]. The availability of commercial memristor IC estimated in the market by 2018

.

In 2011 Leon Chua extended the definition of memristor by adding all two terminal systems independent of device materials properties and physical operation which provides the frequency dependent hysteresis loop in $v - i$ plane are known as memristors.

Memristor is used in RRAM (Resistive Random Access Memory) cells whose size can be scaled down by the order of tens of nanometers which provide in fabricating high density memory devices. Compare to CMOS based RAM, RRAM provided high ON/OFF ratio, With all this advantages it can play a major role in next generation universal memory. The switching property of memristor is shown in Figure[1.2]

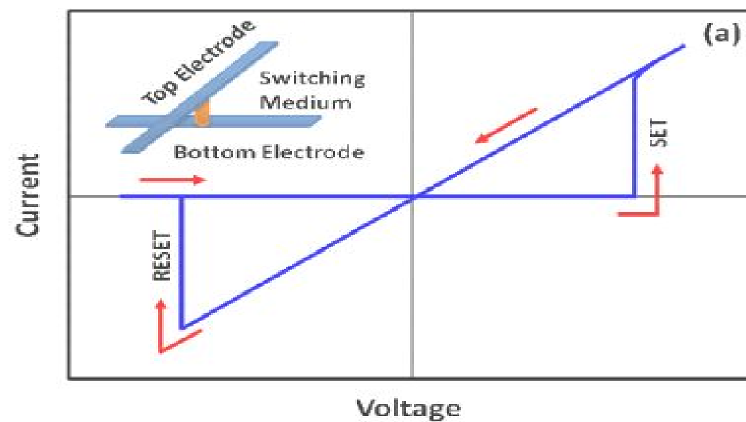

Figure 1.2 : current voltage characteristics of digital (M-I-M memristor)

biological operation of synapse is observed in memristor with analog switching with continues increase in resistance with relatively slow ON/OFF ratio which is shown in Figure 3 will help in mimicking of human brain in chip which is main application of neuromorphic engineering. Crossbar memristor structure helps in increasing the inter neuron connections and neuron density of order 10^{10}.

Memristor based neuromorphic system also provides STP/LTP (short/long term plasticity), interaction between different neurons and their connection strength in the form of weights, spiking rate and learning experience.

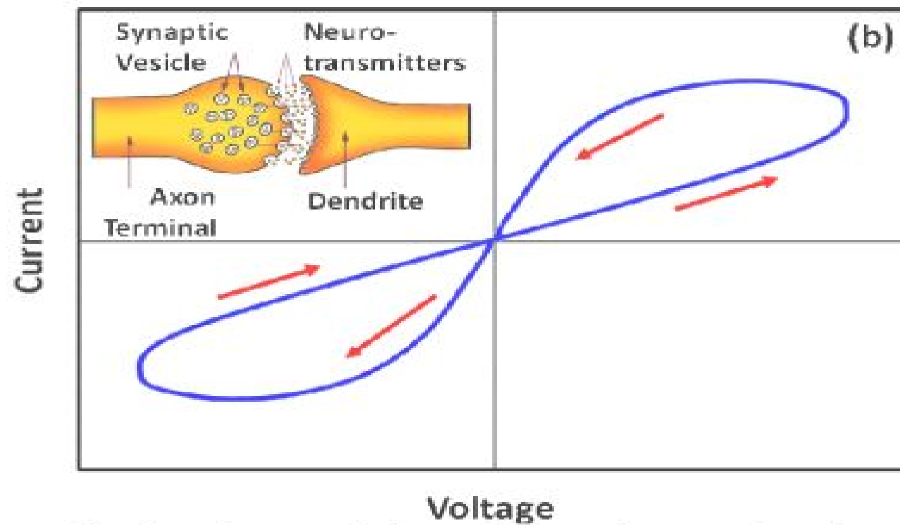

Figure 1.3: switching behavior of analog (biological synapses)

Polymer materials has advantages compare to metal oxide and other inorganic components because of their flexibility, low cost, easy processing and ductility. Fabrication process of polymer based memristor is easy compare to metal oxide materials.

Linear regression using tensor flow is used to predict the reliability of the fabricated component where it provide the relation between the independent and dependent variables[4][5][6].

CHAPTER - 2

Memristor Operation

2.1 Theory of Memristor

The non-linear relationship between magnetic flux linkage Φm(t) and electric charge q(t) is given as.

$$f(\Phi m(t), q(t)) = 0 \quad (4)$$

$$M(q) = \frac{d\Phi_m}{dq}$$

$$M(q(t)) = \frac{d\Phi_{m/dt}}{dq/dt} = \frac{V(t)}{I(t)} \quad (5)$$

A mathematical model for switching rate($R_{on} \ll R_{off}$) of titanium dioxide base memristor is given by HP Labs in 2008 is [3]

$$M(q(t)) = R_{off}.\ (1 - \frac{\mu_v R_{on}}{D^2}\ q(t)) \quad (6)$$

R_{off} - high resistance , R_{on} - low resistance, μ_n - mobility of dopants in the film,
D - oxide layer thickness.

nonlinear ionic drift and boundary effects are differentiated using window functions.
Power equation for memristor is given as

$$P(t) = I^2(t) M(q(t)) \quad (7)$$

2.2 Memristor as a Switch

The switching property of memristor is due to change in resistance. Considering applied voltage constant energy dissipation during on and off state of resistance with respect to time is given as[8].

$$E_{switch} = V^2 \int_{T_{off}}^{on} \frac{dt}{M(q(t))} = V^2 \int_{Q_{off}}^{Q_{on}} \frac{dq}{I(q)M(q)} = V^2 \int_{Q_{off}}^{Q_{on}} \frac{dq}{V(q)} = V\Delta Q \quad (5)$$

2.3 Pinched Hysteresis

Input current on a y-axis and the output voltage on the x-axis gives the hysteresis loop which explains the electrical resistance and switching behavior for different resistance this leads to two-terminal resistance memory and RERAM[9].

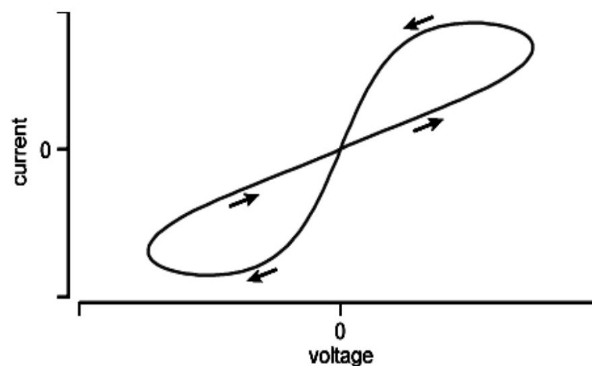

Figure 2.1 **:** Pinched hysteresis loop of memristor.

2.4 Operation of Memristor

The resistance of memristor depends on the length of the doped and undoped region, The internal state variable diagram in (fig 2.2(a)) shows the lower resistance at doped region with high resistance at undoped region. The total resistivity of the device can be changed by applying an external voltage or current source.

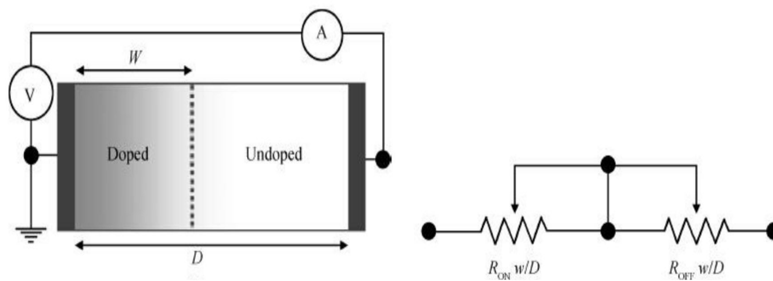

Figure 2.2 : **(a)** internal state variable diagram, **(b)** circuit of a memristor acts as a potentiometer.

The (fig 2.2(b)) represents memristor as analog variable resistor between two oxide layers. Depending on the polarity the oxygen atoms move in either directions which lead to change in oxide layer thickness and resistance. The last resistance before off state is maintained after turning off the memristor which leads to non volatility property[3].

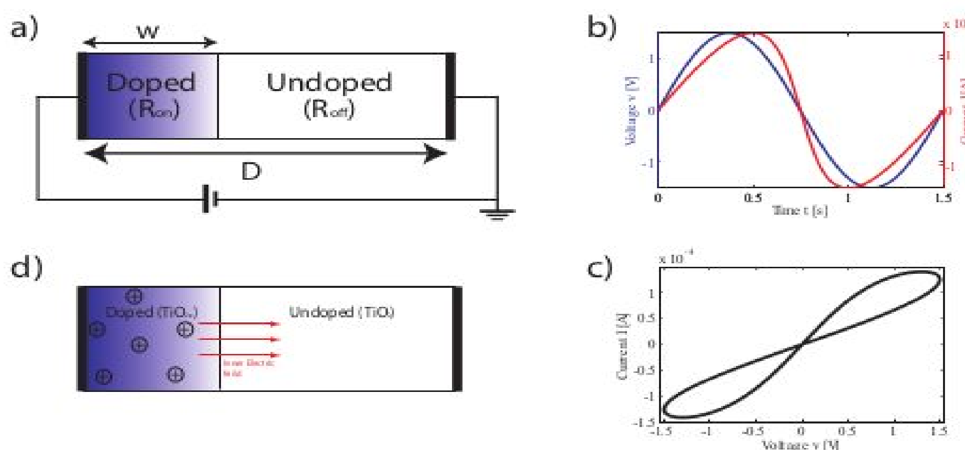

Figure 2.3 : HP memristor characteristics.

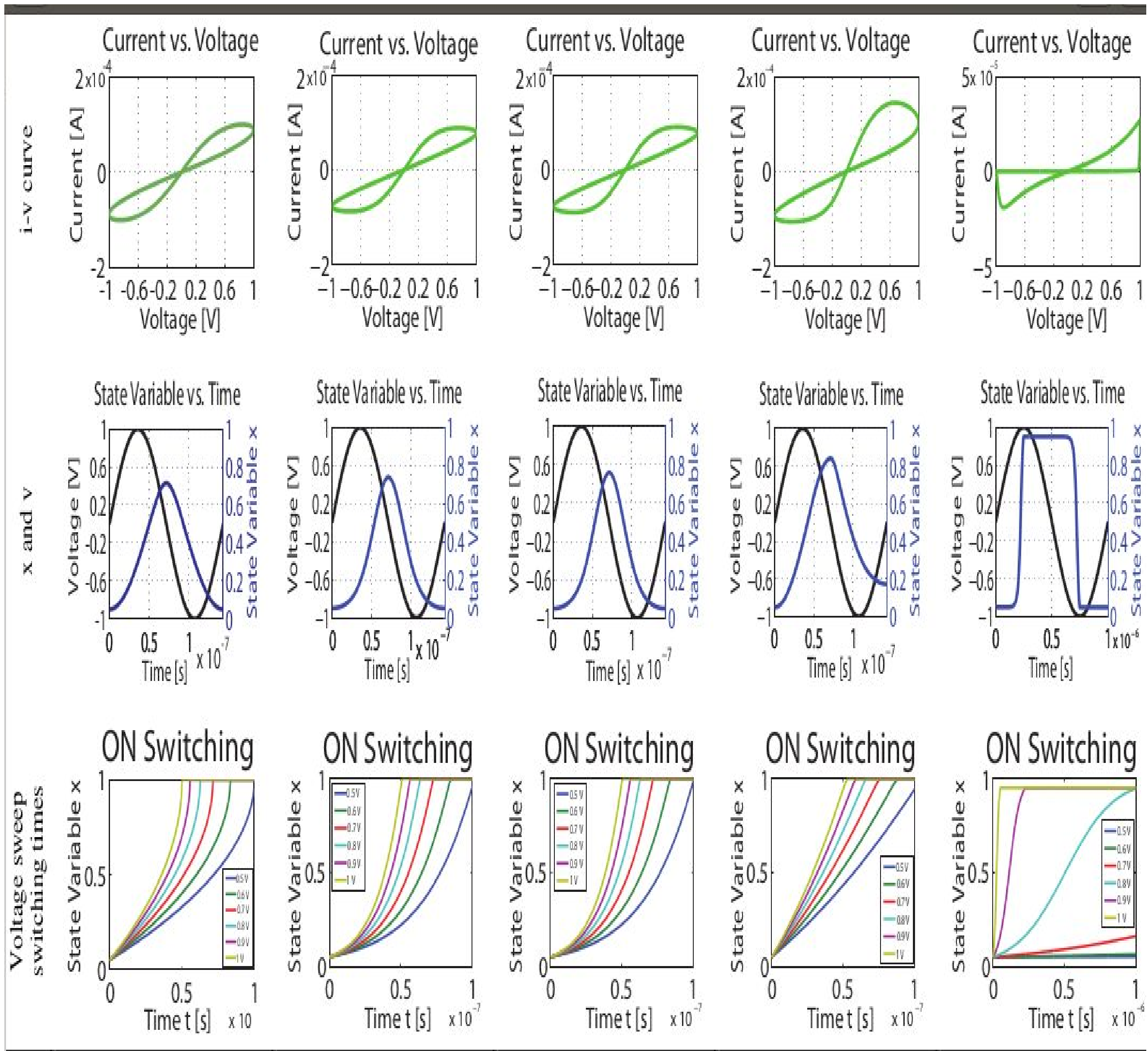

Figure 2.4 : comparison of different models for current and voltage, state variables and time, switching vs time

Models	**Linear**	**Nonlinear**	**Exponential**
Boundary Conditions	NO	YES	YES
Window Function	NO	YES	YES
Nonlinear in Electric Field	NO	NO	YES
Voltage sensitivity	Linear	Linear	Highly nonlinear
Switching time	Symmetric	Symmetric	Symmetric (polarity-dependence resistance)

Table 2.1 : comparison of models

CHAPTER - 3

Literature Review

3.1 Methods to Fabricate

Metal Insulator Metal (MIM) fabrication process is to sandwich insulator layer in between two metal layers. Titanium dioxide, Zinc oxide, Organic insulators, Polymers, Amorphous silicon and Ferroelectric material are suitable for the intermediate insulator layer. Conductor materials like Platinum(Pt), silicon(Si), Silver(Ag), Copper(Cu) and Gold(Au) are commonly used top and bottom layers[10].

3.2 Zinc Oxide (Zno) - Based Memristor

Ashish Kumar and his team explained the fabrication process in their research paper "Fabrication and Characterization of the ZnO-based Memristor". step by step fabrication process of Zinc oxide based Memristor is explained in following figure 3.1 [11].

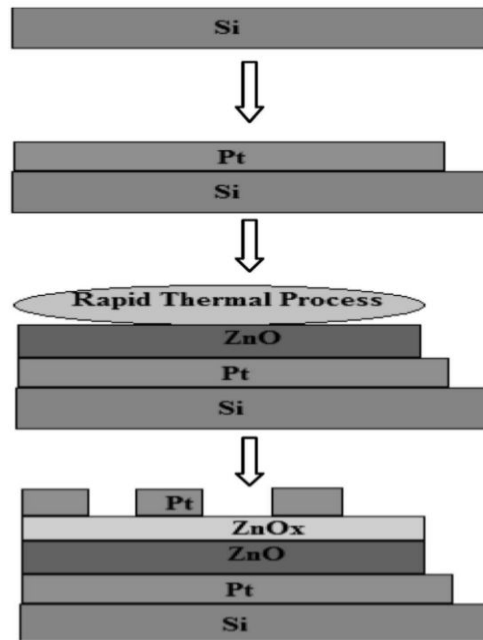

Figure 3.1 **:** Zinc oxide based memristor

1)Silicon as a base substrate.

2) Platinum(Pt) is deposited on silicon substrate.

3) A profilometer is used to determines thickness and roughness of the sample.

4) 400 nm of zno is deposited on Pt layer with the help of by dielectric sputter system and thickness is measured.

5) To get Zno_x layer heat treatment (annealing) is performed at 500°C in the presence of 800 standard centimetre cubic per minute (SCCM) oxygen flow.

6) The top Pt layer is shadow mask with holes of diameter 400(micrometre) and thickness of 100nm[11][12].

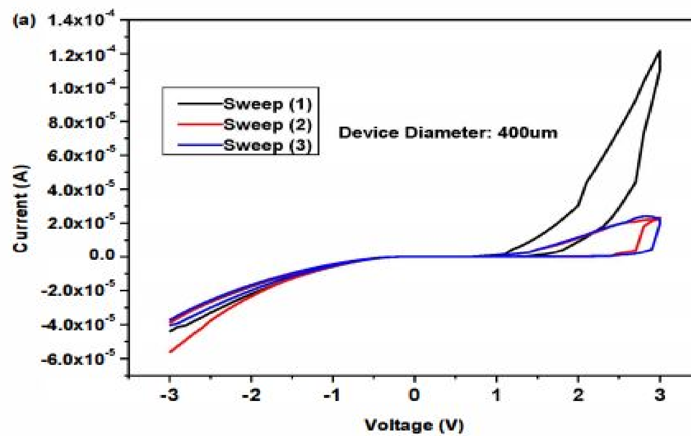

Figure 3.2 : without annealing i-v curve

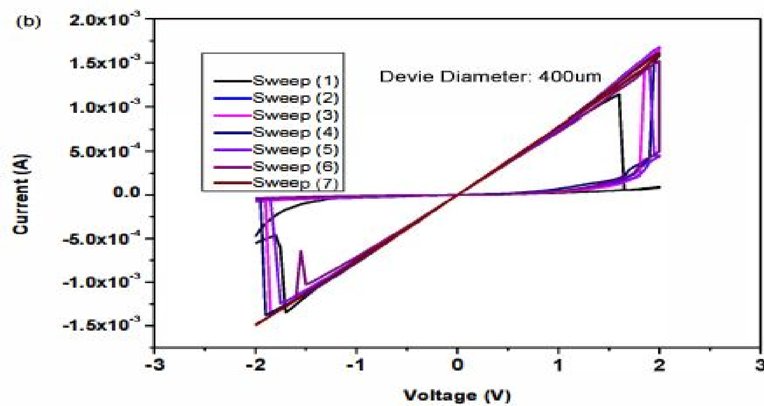

Figure 3.3 : with annealing i-v curve

3.3 Titanium Dioxide (Tio_2)- Based Memristor

Weisong Wang and his team explained fabrication process in their paper "Fabrication, Characterization, and Modeling of Memristor Devices" with different insulated layers as shown in following figures[3.2].

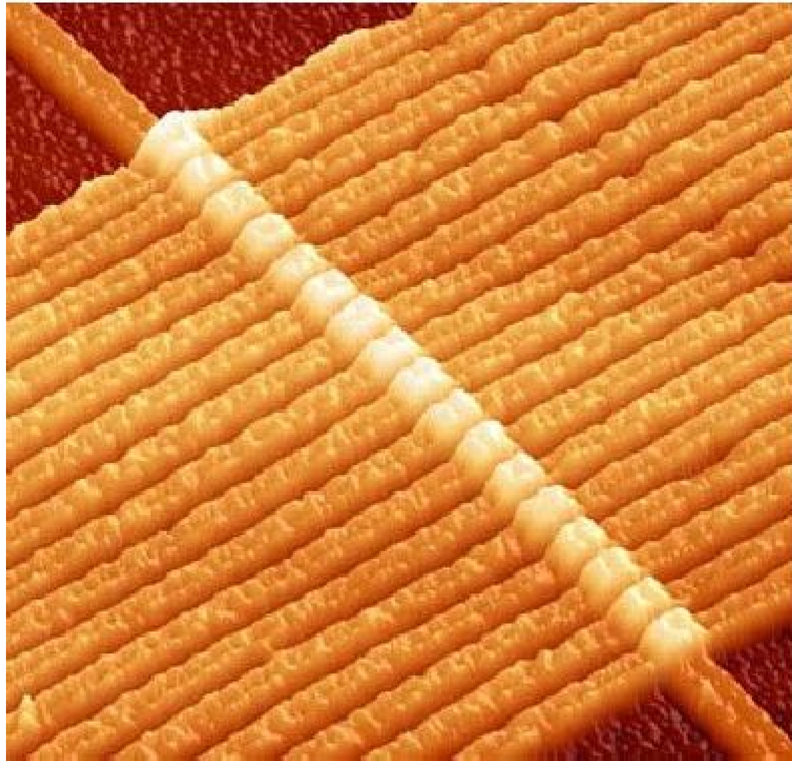

Figure 3.4 : Tio_2 based memristor by HP Labs

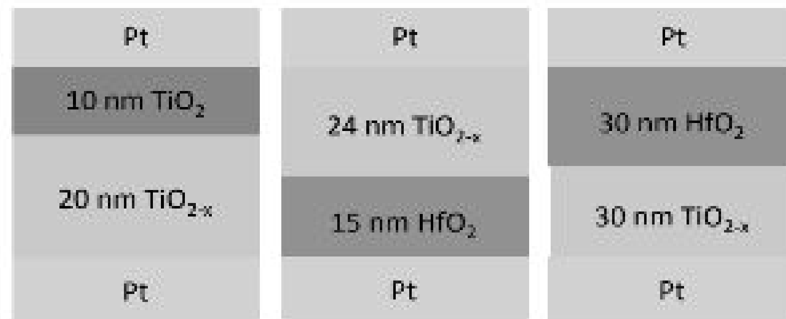

Figure 3.5: **(a)** $Pt/Tio_2/Tio_{2-x}/Pt$ **8(b)** $Pt/Tio_{2-x}/Hfo_2/Pt$ **8(c)** $Pt/Hfo_2/Tio_{2-x}/Pt$

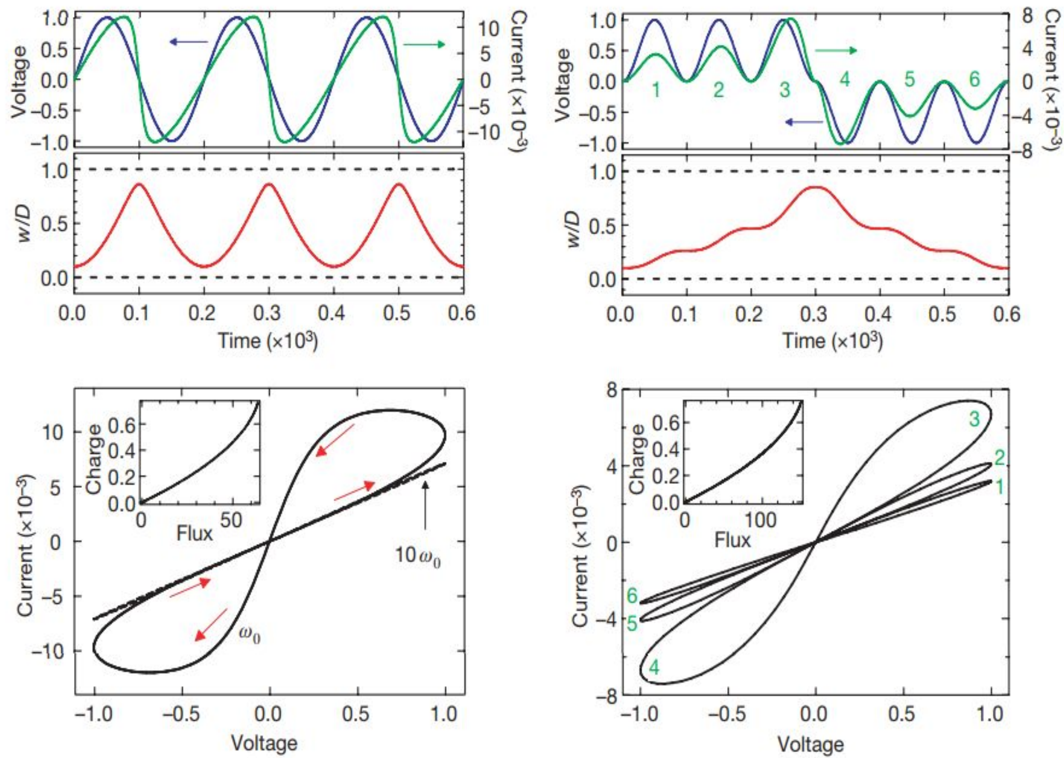

Figure 3.6 : i-v curve and hysteresis loop of Tio_2 based memristor

1) Platinum(Pt) layer is used as top and Bottom terminals of memristor.

2) Reactive sputtering or Atomic layer deposition (ALD) methods are used to deposit middle oxide layers.

3) 20nm thickness of oxygen deficient titanium dioxide (Tio_{2-x}) is deposited on bottom platinum layer.

4) stoichiometric Tio_2 , Hfo_2 and Tio_{2-x} layers based on the thickness provided is deposited on base oxide layers[13].

Logic Gate Implementation

There are three major logic gate design using memristor is explained by S. Kvatinsky and his team in their paper “Memristor-based IMPLY Logic Design Flow”[14].

3.4 MRL (Memristor Ratioed Logic)

MRL (Memristor Ratioed Logic) is voltage- dependent hybrid CMOS-memristor . Logical OR and AND operators are implemented and CMOS inverters is added to provide signal restoration. The schematic of an MRL NAND and NOR are is shown in (Figure 3.4)[14][15].

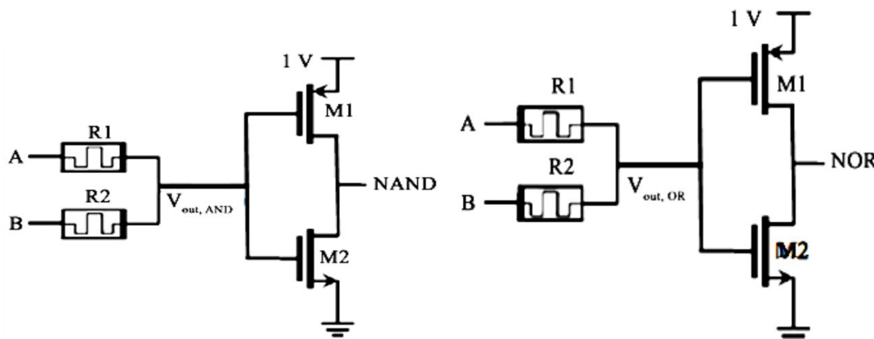

Figure 3.7**:** Implementing NAND and NOR logic using memristor and CMOS inverter.

MRL (Memristor Ratioed Logic) model requires less area and faster to perform any logical operation compared to traditional CMOS logic transistor .

3.5 Material Implication (IMPLY):

Logical state is represented as a resistance in Material Implication model. The model performs computing and the output is stored as a resistance in one of the inputs memristors. Material Implication model requires voltage levels (controller and resistor)[16].

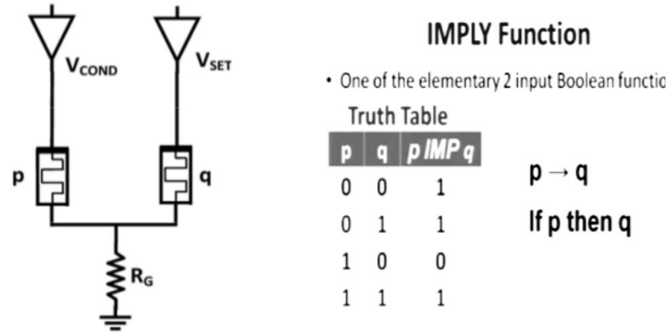

Figure 3.8: Material Implication using Imply function.

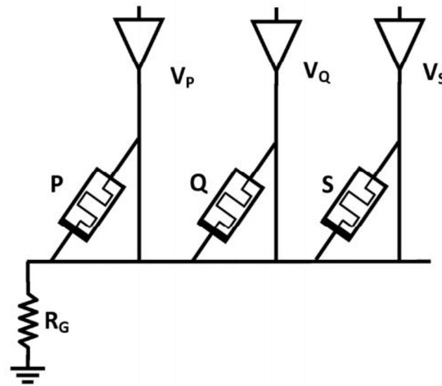

Figure 3.9 : NAND gate using Imply model

3.6 Magic Implication

The disadvantages like voltage levels and storage of the output in the same input memristor of Material Implication (IMPLY) is overcome in this model. MAGIC-based logic gates fabricated within a crossbar, the Stable output is achieved by applying voltage pulse at the gateway of the circuit, the circuit is shown in (fig 3.6)[17].

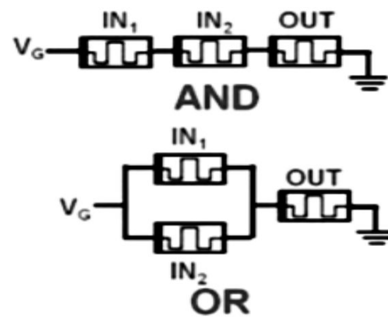

Figure 3.10: Magic implementation of AND and OR operation.

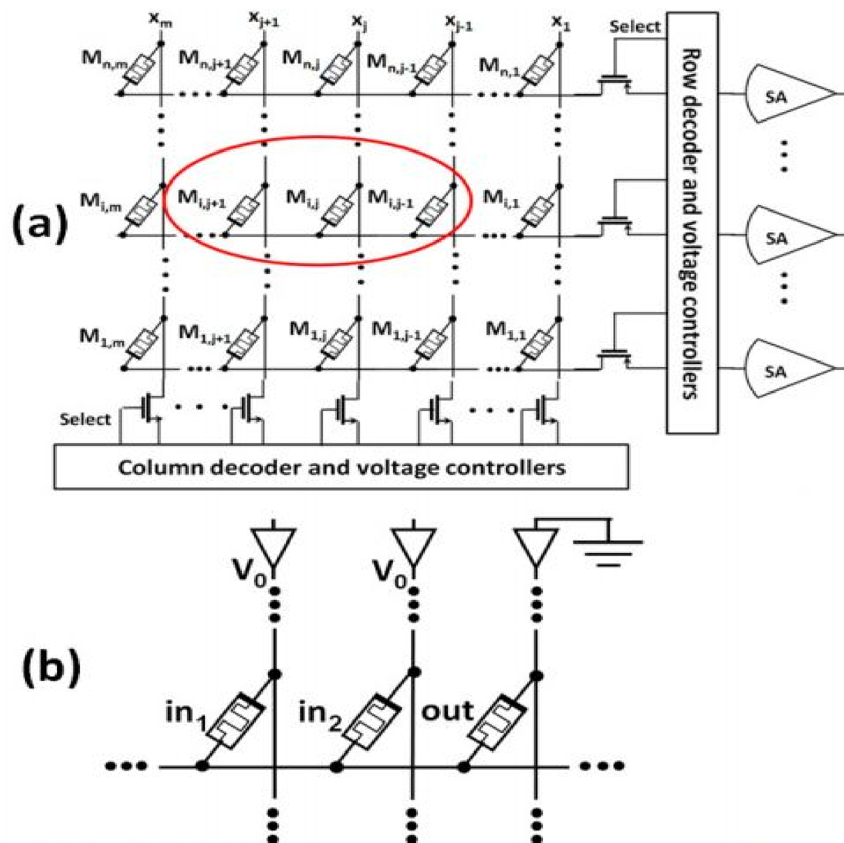

Figure 3.11 : (a)memristor crossbar structure, (b) two input NOR gate crossbar schematic.

	IMPLAY	**MAGIC**
NO. of voltages	2($V_{SET,}V_{COND}$)	1(V_0)
Separate input and output	No	Yes
Basic functions	IMPLY(+FALSE)	OR,AND,NOR,NAND,NOT
No. of memristor for NOR/NAND	3(+a resistor)	3
NO. of clock cycles for NOR/NAND	4	2
Within memort	Yes	Yes
Logically complete	False	Yes

Table 3.1 : IMPLY and MAGIC comparison

CHAPTER - 4

Objective of Study

4.1 Objective and problem

In R.Dennard method channel length (L_g) and oxide thickness (t_{ox}) of MOSFET is scaled down by 1/K and substrate is scaled up by K, this leads to scale down of applied voltage by factor of 1/K[2][3].

This method reaches its efficiency limit at 0.35um of channel length(L_g). Fig 1 explain the effects of scaling down the channel length with respective to gate overdrive voltage(V_{dd}-V_t or V_{gs} -V_t). The threshold voltage(V_t) reduces to 50% of its initial value after V_{dd} cut down to half, and after 0.35um gate overdrive voltage remained almost constant.

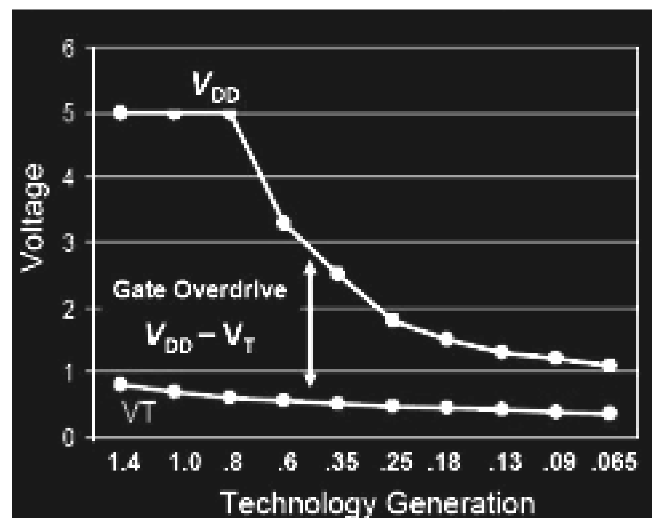

Figure 4.1 : technology generation Vs voltage

As overdrain voltage decrease ON current decreases leads negative effect on ON and OFF ratio. Increase in V_{dd} and decrease in V_t will resolve the problem[4].

$$P_{dynamic}= FC_L V_{DD}^2$$

$$P_{static}= I_{leak} V_{DD}$$

To improve performance and overcome the problems organic polymers come into picture with their flexible and low cost properties.

The importance of selecting (PEDOT:PSS) poly(3,4-ethylenedioxythiophene): poly(styrenesulfonate) polymer is its resistivity at negative input voltage and increase in conductivity at positive input voltage.

The problems in existing Ag/PEDOT:PSS/Ta Memristor is transition point for conductivity is high due to the redox reaction at Ag and PEDOT and at the same time Ag ions which are oxidized will combine with PEDOT:PSS and leads to reduced conduction initially.

To enhance the performance of the component and to predict the best outcomes of combining different components and at different compositions can be analysed using the testing algorithm by feeding the neural network with test data of the component and trying the system to generate a solution for the problem.

4.2 Research methodology:

1. Placing PEDOT:PSS in between two zinc oxide layer will stop movement of electrode ions into the PEDOT substrate ZnO act as the protecting layer for PEDOT:PSS polymer. And basic idea to selecting Ag(Silver) as electrodes is because of their high conductivity property[18].
2. Alternative material instead of ZnO is Zn doped Fe_3O_4 which act as insulator at (100k-170k)temperature and at room temperature it will act as the good conductor so this composition can use as shielding layer to PEDOT:PSS[19].

By using this type of matology we can improve the conduction rate by eliminating transition time this leads to high speed data processing and it also provided hardware stability.

Developed training algorithm will understanding the problem with available data and help

us in developing much better components and systems[12].

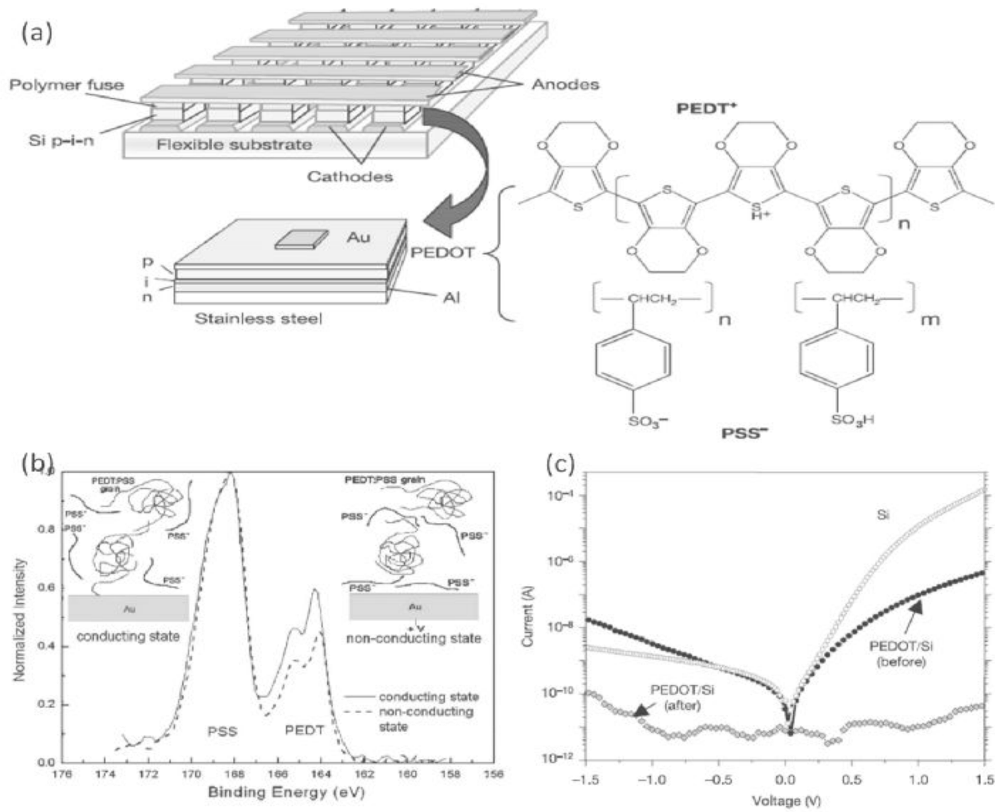

Figure 4.2: PEDOT:PSS structure and i-v characteristics of PEDOT:PSS based memristor

4.3 Workflow:

1) Ag(silver) wafer of 100 nm is deposited on Glass as base substrate.
2) Oxidation : 30-50 nm thin layer of ZnO.
3) PEDOT of 0.5wt% and PSS of 0.8wt% in PEDOT:PSS aqueous solution is spin coated.
4) 3000 rpm for 30s and 1500 rpm for 20s respectively using spin coater.
5) heated for 10 min at 120 degrees centigrade.

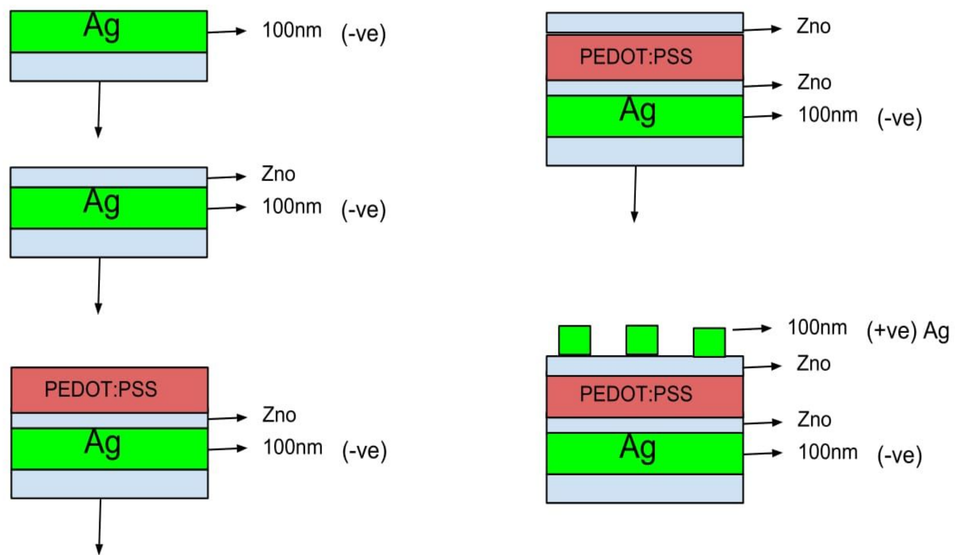

Figure 4.3 : Ag/Zno/PEDOT:PSS/Zno/Ag physical structure.

4.4 Equipment and Materials

s.no	**chemical compositions**
1	PEDOT:PSS (**poly(3,4-ethylenedioxythiophene): poly(styrene sulfonate)**)
2	Ag (silver)
3	Ta (Tantalum)
4	Sio2 (Silicon dioxide)

Table 4.1 : list of components.

s.no	**lab equipments**
1	Spin coating
2	Glovebox with Nitrogen
3	Filter with micro membrane of pore size of 0.45um

Table 4.2 : lab equipments required.

Software requirement:

1) Tensoeflow python based library.
2) ORCAD Pspice.
3) Xilinx-9.2.

CHAPTER - 5

Experimental Work

5.1 Linear Regression:

Linear regression gives the relationship between scalar dependent variable Y and independent variables X. using linear regression linear models are generated which contains estimated parameters using present data. Conditional probability deals with value of Y for given X, and joint probability deals with both X and Y. linear dependent models are easy to fit than non-linear models to identify unknown data.

Application areas of linear regression is error reduction, forecasting and prediction. By observing the previous values of X and Y it can predict value of Y for given value of X. the basic expression of linear regression is given in equation.

$$Y = a + bx$$

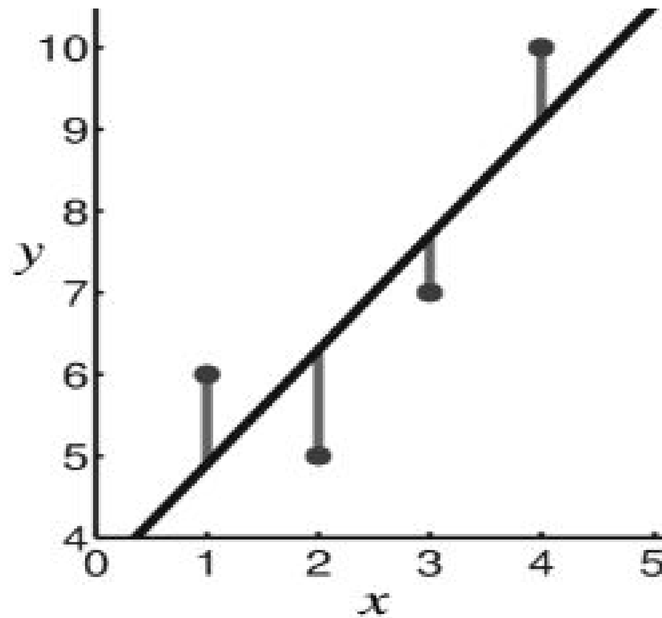

Figure 5.1: linear regression graph

5.2 Tensor Flow:

Tensor Flow is a open source python based math library used for neural network applications developed by google brain team.

```
----------- Training Data -------------
X = numpy.asarray([3.5,4.7,5.6,6.70,6.83,4.148,9.780,6.18,7.49,2.157,
                  7.04,10.771,5.31,8.03,5.652,9.29,3.10])
Y = numpy.asarray([1.76,2.66,2.9,3.29,1.594,1.563,3.37,2.376,2.530,1.21,
                  2.817,3.565,1.065,2.94,2.52,2.84,1.30])
n = X.shape[0]

-------------------Set model weights--------------------
w = tf.Variable(rng.randn(), name="weight")
b = tf.Variable(rng.randn(), name="bias")

-------------Construct a linear model-------------------
pred = tf.add(tf.multiply(X, w), b)
```

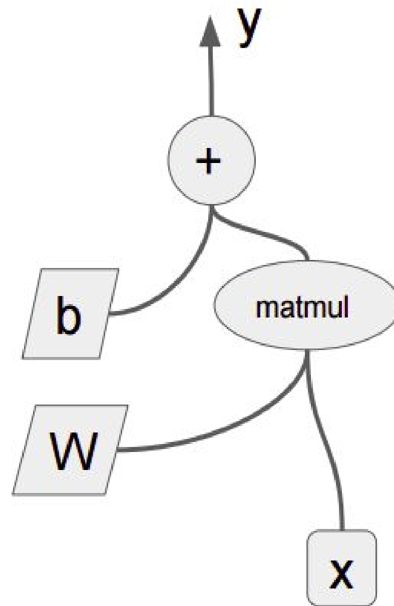

Figure 5.2: Linear regression flow graph

----------------Mean squared error---------------

cost = tf.reduce_sum(tf.pow(pred-Y, 2))/(2*n_samples)

--------------Gradient descent----------------------

optimizer = tf.train.Gradient Descent Optimizer (learning_rate).minimize(cost)

----------------Linear regression-------------------------

plt.plot(X, sess.run(w) * X + sess.run(b), label='Fitted line')

```
Epoch: 0050 cost= 0.322175068 W= 0.526353 b= -1.18952
Epoch: 0100 cost= 0.293855995 W= 0.509093 b= -1.07111
Epoch: 0150 cost= 0.268885385 W= 0.494412 b= -0.95974
Epoch: 0200 cost= 0.246647269 W= 0.479851 b= -0.854992
Epoch: 0250 cost= 0.227047533 W= 0.466157 b= -0.756474
Epoch: 0300 cost= 0.209711149 W= 0.453277 b= -0.663817
Epoch: 0350 cost= 0.194376588 W= 0.441163 b= -0.57667
Epoch: 0400 cost= 0.180812925 W= 0.429769 b= -0.494706
Epoch: 0450 cost= 0.168815494 W= 0.419054 b= -0.417616
Epoch: 0500 cost= 0.158203691 W= 0.408975 b= -0.345111
Epoch: 0550 cost= 0.148817331 W= 0.399496 b= -0.276918
Epoch: 0600 cost= 0.140515119 W= 0.39058 b= -0.212782
Epoch: 0650 cost= 0.133171842 W= 0.382195 b= -0.152459
Epoch: 0700 cost= 0.126676783 W= 0.374309 b= -0.0957247
Epoch: 0750 cost= 0.120931976 W= 0.366891 b= -0.0423645
Epoch: 0800 cost= 0.115850836 W= 0.359915 b= 0.00782289
Epoch: 0850 cost= 0.111356720 W= 0.353354 b= 0.0550239
Epoch: 0900 cost= 0.107381791 W= 0.347183 b= 0.0994183
Epoch: 0950 cost= 0.103866168 W= 0.341378 b= 0.141172
Epoch: 1000 cost= 0.100756735 W= 0.33592 b= 0.180443
Optimization Finished!
Training cost= 0.100757 W= 0.33592 b= 0.180443
```

Figure 5.3 : output values

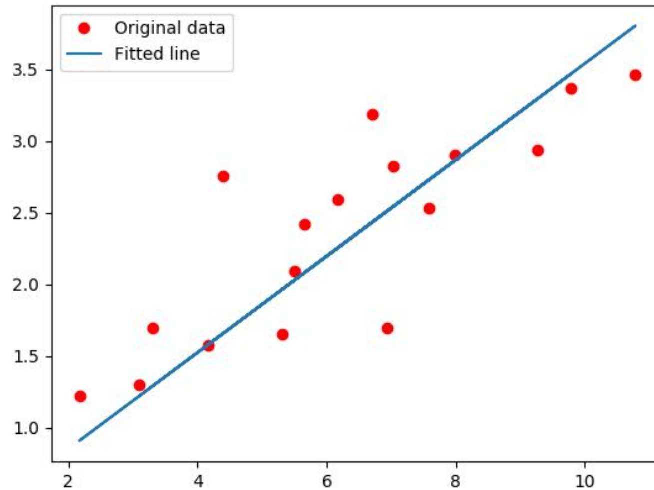

Figure 5.4 : regression graph

5.3 PSPICE Model of Memristor:

Pspice model help in relating mathematical model values and provide input and output voltage curves. The code for ORCAD Pspice model is provided below.

```
.SUBCKT memristor 1 2 3
Eres 1 9 POLY (2) (8,0) (10,0) 0 0 0 0 1
Vsense 9 4 DC 0V
Fcopy 0 8 Vsense 1
Rstep 8 0 1k
Rser 2 4 10
Gmem 3 0 VALUE={I(Vsense)*max(v(3,0)*(1-v(3,0)),0)}
Cmem 3 0 50nf
Ecpy 10 0 VALUE= {min(max(v(3,0),0),1)}
Rsp 3 0 1000 Meg
.ENDS
*$
```

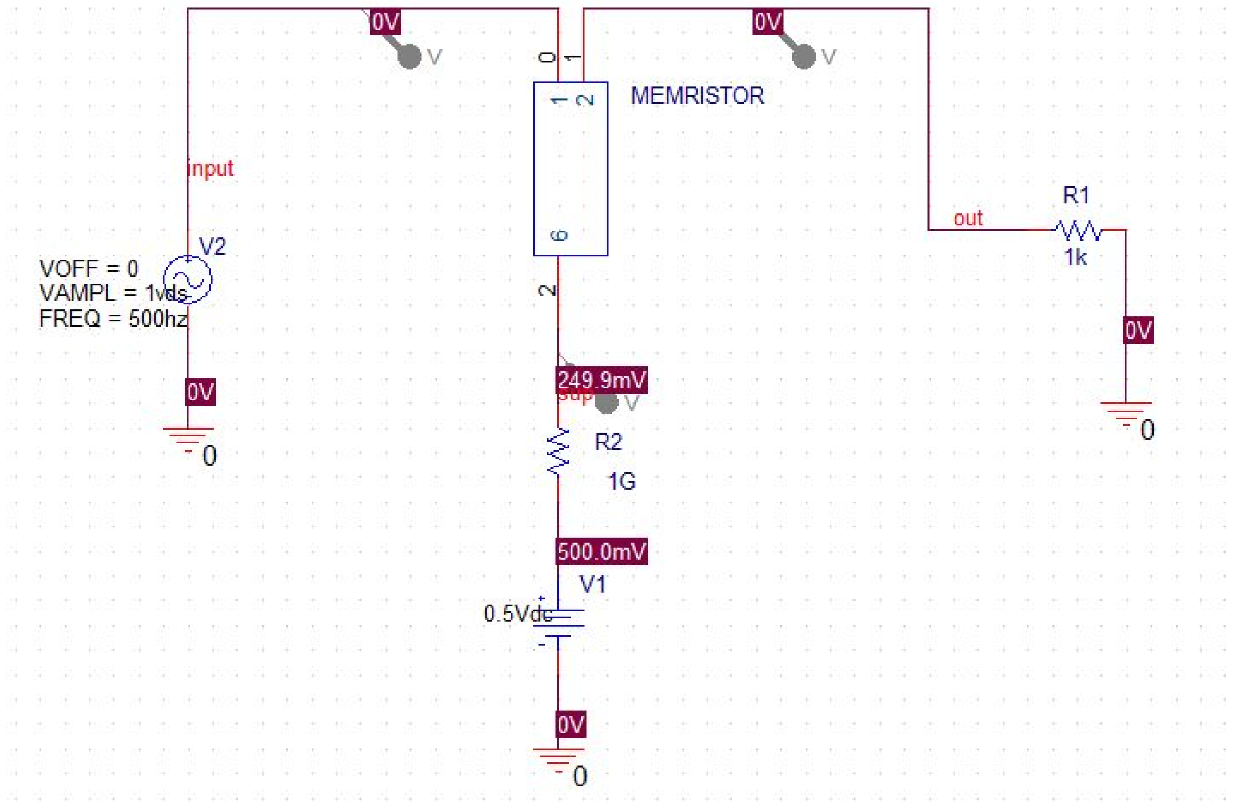

Figure 5.5 : memristor in/out voltage analysis circuit.

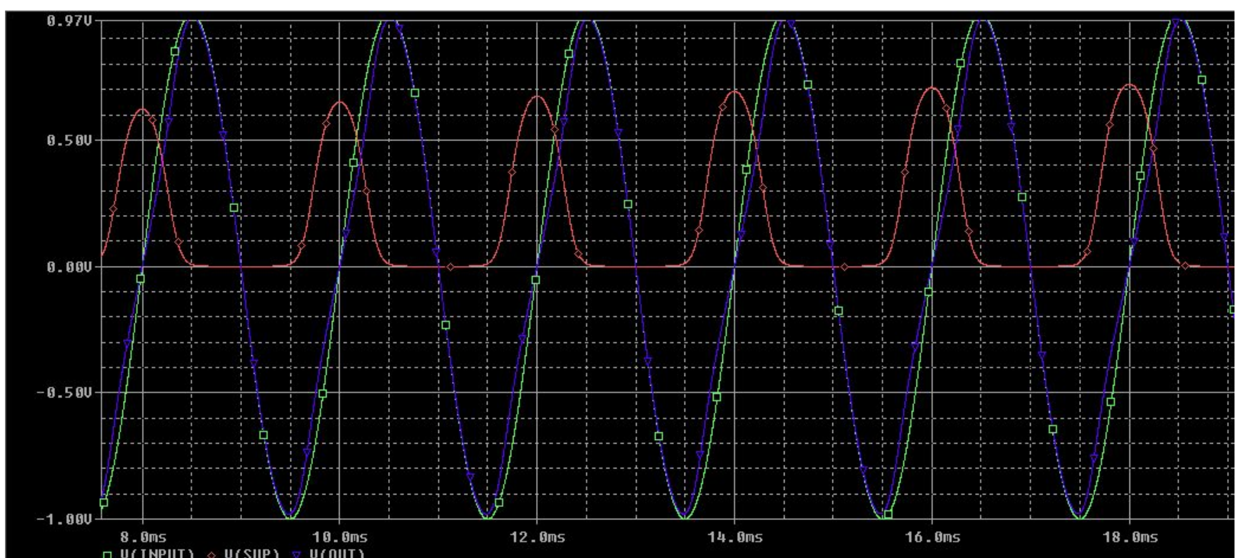

Figure 5.6 : memristor in/out voltage output.

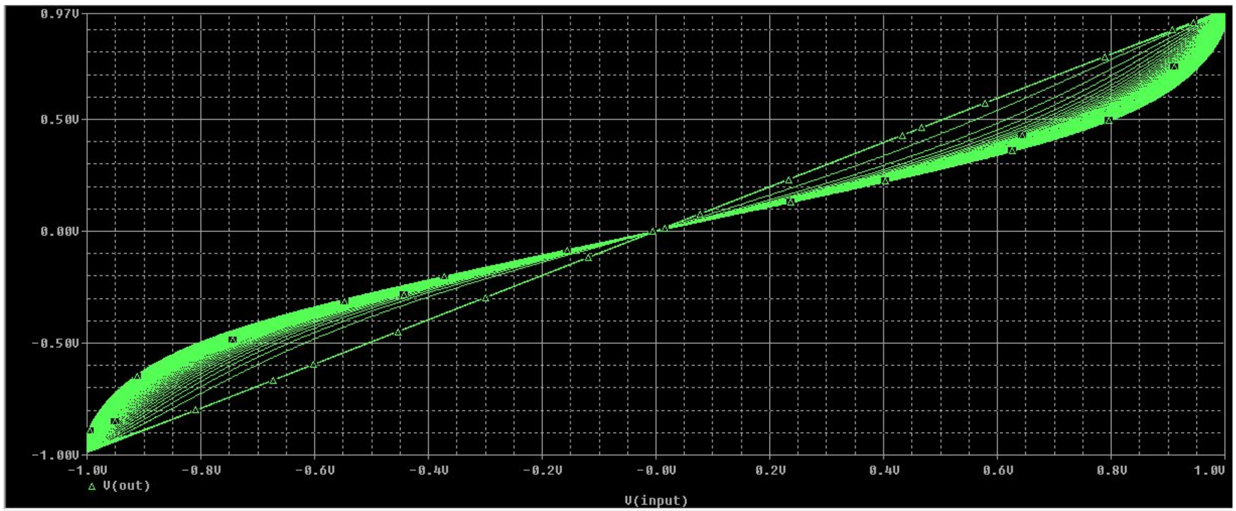

Figure 5.7 : memristor pinched hysteresis loop.

CHAPTER - 6

Laboratory Investigations

Fabrication Work Plan:

Registered for using fab lab at IIT-B(Indian Institute of Technology Bombay) through INUP(Indian Nanoelectronics Users Program).

Program : Short-term measurements/fabrication (3 Months)

January-2018	February -2018	March-2018
Training on usage of equipments	Fabricating Memristor	Implementing A.I algorithms and training the system using output data.

Table 6.1 : workflow.

CHAPTER-7

Applications:

The proposed model of memristor (Ag/Zno/PEDOT:PSS/Zno/Ag) has property of Resonant-tunneling diode memristors which operate based on the quantum tunneling which has major application in low power electronics and it also overcome the short channel effects, high leakage current, low value of ON-OFF ratio and parasitic effects of CMOS transistors.

7.1 Structure and operation:

P-I-N (p-type, intrinsic, n-type) is the structure of general TFET gate terminal on the intrinsic region controls the electrostatic potential. Unlike thermal injection in MOSFET
for charge movement BTBT(band to band tunneling) is used. There are three terminal in TFET Source, Gate and Drain, source region is used to provide charge carriers, gate terminal is used to control the charge carrier from source to drain. The subthreshold slope (SS) of TFET lower the 60 mv is good for low power applications. Initially Intrinsic region between source and drain has large provides large barrier potential so the transistor will be in OFF state and when gate voltage (Vg) is greater than threshold voltage(Vt) the potential reduces and flow of current increases. This transmission from source to drain is calculated using Wentzel Kramers Brillouin(WKB) equation[20][21].

$$T_{wkb} = \left[\frac{4\lambda\sqrt{2mE_g^3}}{3qh[E_q+\Delta\phi]}\right]$$

m - effective mass, E_g- band gap, λ - screening tunnel length

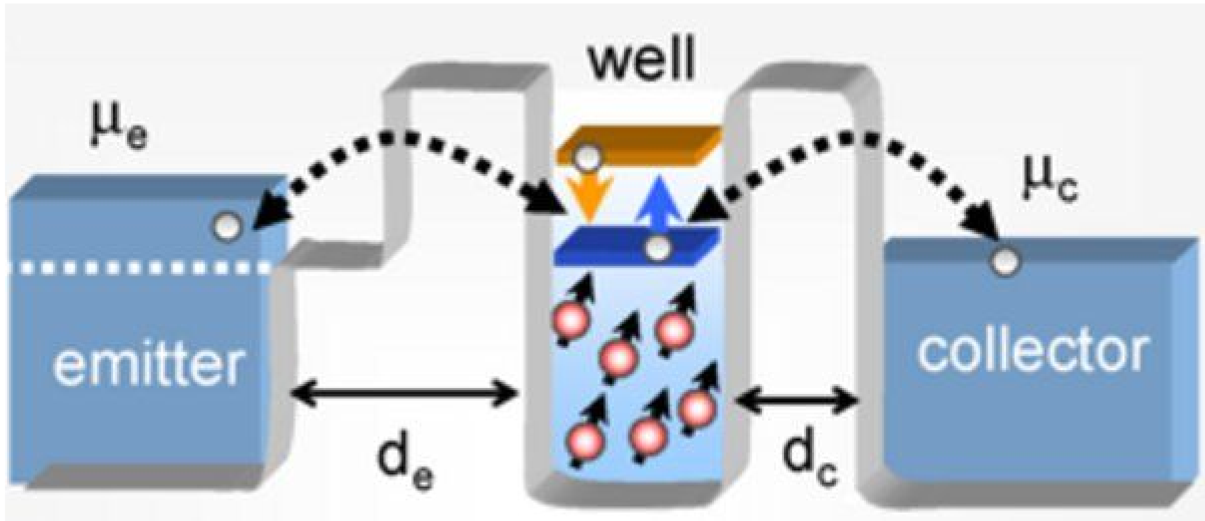

Figure 7.1 operation of Resonant-tunneling diode

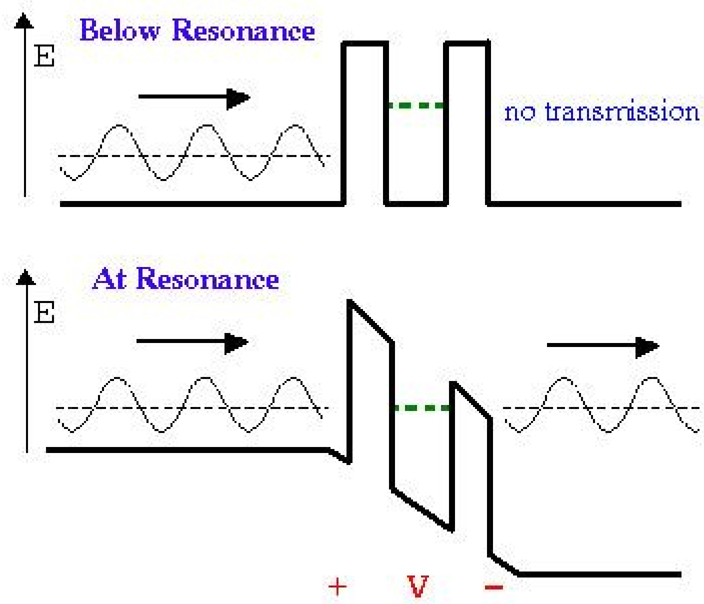

Figure 7.2 : close and open channel

7.2 Neural networks:

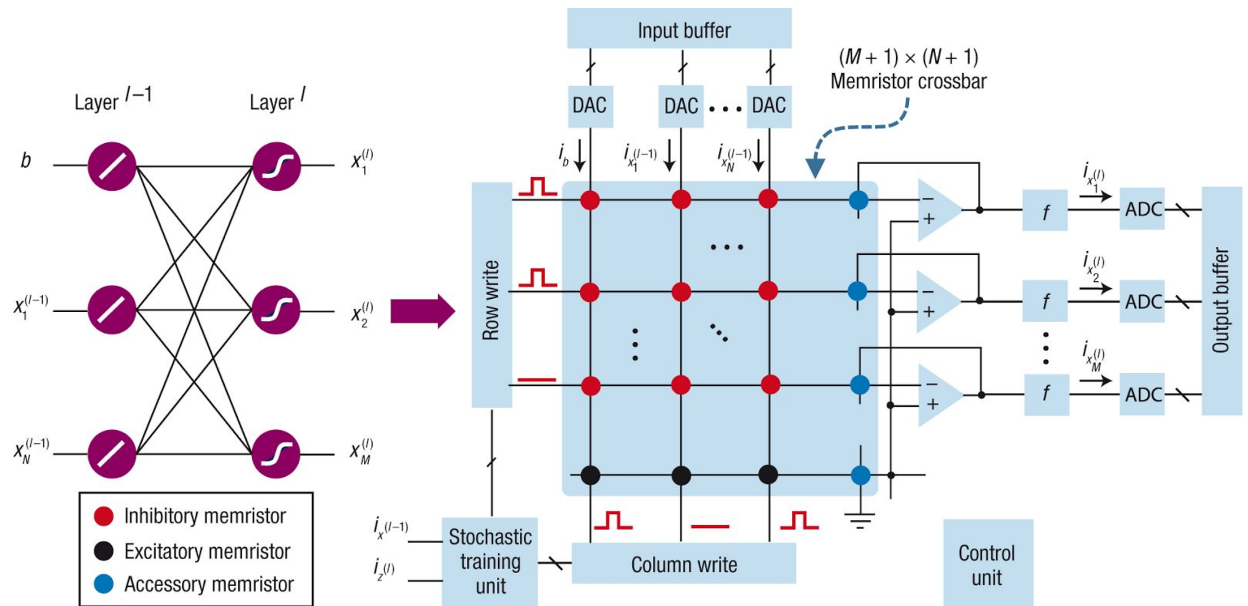

Figure 7.3 : Implementing neural network model using memristor crossbar method.

7.3 Comparison and Advantages :

Specifications	**RRAM**	**SRAM**	**DRAM**
volatile	No	Yes	Yes
Speed	Faster	Fast	Medium
Power Consumption	Low	Medium	High
Density	High	Low	High

Table 7.1: comparison between RRAM, SRAM and DRAM

	Emerging Memories				Established Memories	
	FeRAM *(or FRAM)*	MRAM	ReRAM *(or RRAM)*	PCRAM *(or PRAM, PCM)*	DRAM	Flash NAND
Nonvolatile	YES	YES	YES	YES	NO	YES
Endurance	High (10^{12})	High (10^{15})	Medium (10^{8})	Medium (10^{8})	High (10^{15})	Low (10^{5})
2012 latest technological node produced (nm)	130 nm	130 nm	R&D	45 nm	30 nm	20 nm
Cell Size (cell size in F^2)	Large (15-20)	Large/Medium (6-40)	Medium (6-12)	Medium (6-12)	Small (6-10)	Very small (4)
Write speed	Medium (100ns)	High (10 ns)	Medium (75 ns)	Medium (75 ns)	High (10ns)	Low (10 000 ns)
Power Consumption	Low	High/Low	Low	Low	Low	Very High
Cost ($/Gb)	High ($ 10 000/Gb)	High ($ 1000 – 100 /Gb)	R&D	Medium (few $/ Gb)	Low ($1/Gb)	Very Low ($ 0.1/Gb)

Figure 7.4 : RRAM compared with emerging memories and established memories.

CHAPTER - 8

Conclusion

This report explains Operation, Logic gate design,Fabrication methods of the memristor based on research papers given in reference section, pspice model of memristor and reliability of memristor using linear regression is performed . There by report concludes at Nanoscale level polymer based memristor performance is better and require less area in fabrication than the transistor. High-end processing and Neuromorphic engineering are the major application of memristor.

CHAPTER - 9

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