December-2017

Design of High-Speed Low Voltage CMOS Schmitt Trigger

DISSERTATION-II REPORT

Submitted in partial fulfillment of the requirement for the Award of the Degree of

MASTER OF TECHNOLOGY
IN
(Electronics and Communication Engineering)

By

Bhavika Khanna

11607925

Under the Guidance of
Mr. Raghav Gupta (22026)

School of Electronics and Communication Engineering
Lovely Professional University
Phagwara, Punjab-144411

CERTIFICATE

This is to certify that the Dissertation-II titled "**Design of High-Speed Low Voltage CMOS Schmitt Trigger**" that is being submitted by Bhavika Khanna (11607925) is in partial fulfilment of the requirements for the award of the Degree of M.Tech in Electronics and Communication Engineering, is a record of bonafide work done under my guidance. The contents of this Dissertation-II, in full or in parts, have neither been taken from any other source nor have been submitted to any other Institute or University for award of any other degree to the best of my knowledge and beliefs.

Dissertation Supervisor
Mr. Raghav Gupta
(22026)
School of Electronics & Electrical Engineering
Lovely Professional University
Phagwara, Punjab

DECLARATION

I Bhavika Khanna bearing registration number 11607925 student of Master of Technology under the Department of Electronics and Communication Engineering of Lovely Professional University, Phagwara, Punjab, hereby declare that all the information furnished in this Literature review report is based on my own intensive research and is genuine.

This Dissertation-II report contain part of my work which has been submitted for the award of my Degree of Master of Technology under the department of Electronics and Communication Engineering from this University. This is to certify that the matter embodied in this project work has not been submitted earlier for award of any degree to the best of our belief.

Date:30-11-2017

Name Bhavika Khanna

Registration No.:11607925

Signature

ACKNOWLEDGEMENT

I take this opportunity to present my votes of thanks to all those guideposts who really acted as lightening pillars to enlighten our way throughout this literature review that has led to successful and satisfactory completion of this study. It was very exciting for me to work on the literature review of 'Schmitt trigger'. During this work I have gained both practical as well as theoretical knowledge of great significance.

I am highly obliged and thankful to our institute 'Lovely Professional University' and its management and technical staff for its support and cooperation.

I am highly thankful to my mentor Mr. Raghav Gupta for his active support, valuable time and advice, whole-hearted guidance, sincere cooperation and pains-taking involvement during the study and to decide the dissertation topic within the time stipulated.

Bhavika Khanna
11607925

ABSTRACT

As the world is currently heading towards an era of prolonged battery life which has forced the chip designers to go for the scaling down of the supply voltage i.e to operate in the sub threshold region for the reduced power supply consumption, thereby causing the performance deterioration of the circuit in terms of the noise immunity. So, comes the need of such a circuit which can be used as a provision for improving the noise immunity of the circuit, thereby resulting in the development of the Schmitt trigger. This report presents the circuit design of low voltage high speed Schmitt trigger with the feature of adjustable hysteresis, which is implemented using the body biasing technique and a comparison of the results in terms of the propagation delay is presented with respect to the conventional Schmitt trigger circuit in 180nm CMOS technology using Cadence Virtuoso. Also, the effect of the body biasing voltage for controlling the width of the hysteresis-loop is shown thereby suggesting the appropriate voltage of the body terminal of CMOS transistors based upon the fact that greater the width of the hysteresis loop greater will be the immunity of the circuit. In the later section of the report a design using DTMOS CMOS technique suitable for the sub-threshold conduction region has been presented in order to have the minimum possible power dissipation in the system.

TABLE OF CONTENT

LIST OF FIGURES

LIST OF TABLES

CHAPTER 1: INTRODUCTION

Schmitt trigger, as its name suggests, will trigger the output when there is a sufficient amount of change in the input signal. The reason because of which the Schmitt trigger is so popular is its hysteresis property or its ability to work on two different threshold levels which makes it efficient to be used for the purpose of the noise suppression in various analogue as well as the digital circuits [1]. Schmitt trigger provides a valuable solution for improving the sensitivity of the circuit from the electromagnetic interference that means they are used for enhancing the Static Noise Margin of the circuit at the cost of the power and delay consumption [2]-[3]. Schmitt trigger is also known by the name of the bi-stable circuit because of its capability to work on two different threshold values. Because of two different threshold voltages, the Schmitt trigger will switch the output when the input is less or greater than the lower or the upper threshold voltage levels respectively and in between the voltage levels Schmitt trigger will retain the output value. This property of the Schmitt trigger also facilities the conversion of the analogue signal into digital one thus resulting in the reshaping of the pulses. A Schmitt trigger is basically the comparator circuit with the positive feedback signal which means that the loop gain of the circuit is greater than one. The feedback is used for the reason of providing different threshold voltages to the Schmitt trigger in order to have the hysteresis property for the purpose of improving the noise sensitivity of the CMOS device so that the device can have a noise stable operation.

Schmitt trigger functions as a signal restoring circuit [4] which means that they are used to infer out the amount of the original input signal information present by eliminating the noise content from it. The Schematic of a traditional Schmitt trigger consists of two inverters and two output transistors [5] which are connected as shown in the fig.1 below.

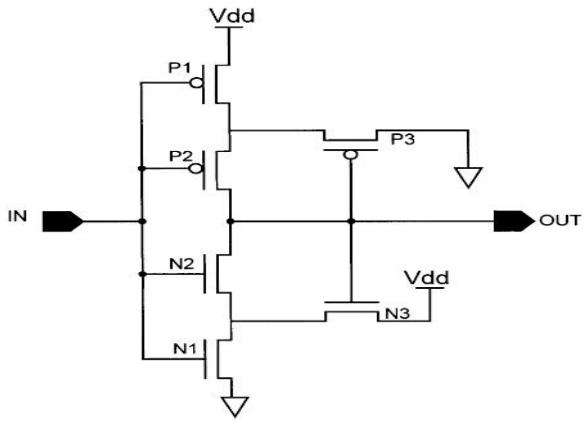


Figure 1 Traditional Schmitt trigger Design

The conventional 6T based Schmitt trigger circuit is basically composed of two sub-sections, section 1 and section 2, where section 1 represents the PMOS circuitry consisting of three PMOS transistors which are responsible for the generation of the lower threshold switching voltage VL and the section 2 represents the NMOS circuitry consisting of three NMOS transistors which are responsible for the generation of the upper threshold switching voltage VH. The PMOS and the NMOS devices are connected with output in order to provide the feedback for the purpose of the elimination of the unwanted noise signal from the output when the changes in the amplitude of input signal are not more than the switching threshold voltage difference.

1.1 Types of Schmitt trigger based upon the technique used for its Implementation

The Schmitt trigger can be implemented using various design methodologies depending upon the performance requirement in terms of the delay, power and area of the circuit design. Based upon the design specifications there are several approaches to design the Schmitt trigger circuit much suited for high speed, lesser amount of voltage and less amount of power consumption applications such as by using the following mentioned design techniques.

1.1.1 VTCMOS Schmitt trigger Buffer

The Conventional CMOS Schmitt trigger design can also be implemented using Variable threshold CMOS technique in which the threshold voltage of CMOS transistors can change by driving the body terminal of the transistors with the help of the any other terminal for example the drain terminal of the transistor as shown in the fig. 2 below. This technique of designing the Schmitt trigger is used in the applications requiring the minimized amount of the power utilization thus making it suitable for the low-power design.

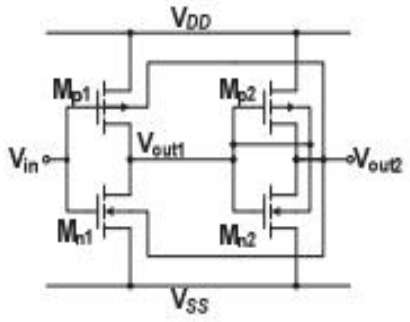


Figure 2 VTCMOS Schmitt trigger Buffer

By using the VTMOS Schmitt trigger buffer, the area utilization of the circuit also gets reduced to a significant amount as the number of the transistors used for the implementation of VTMOS Schmitt trigger buffer is very less when compared to the traditional Schmitt trigger buffer [10].

1.1.2 Self-Bias transistor based Schmitt trigger

The Schmitt trigger circuit can also be re-designed using the Self-Bias transistor technique in which a self-bias CMOS transistor is made to be connected between the voltage- supply and the apex of PMOS section of the circuit as shown in the fig. 3 below in order to decrease the standby as well the active mode power dissipation of the circuit.

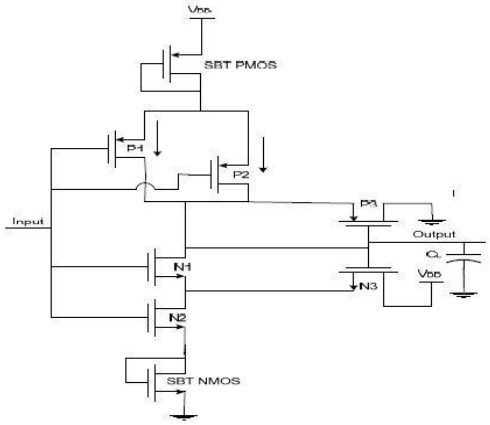


Figure 3 Self-Bias transistor based Schmitt trigger

In the above design the pull up section of the traditional Schmitt trigger has been redesigned in order to decrease the resistance of the circuit for having the minimum possible delay thus making it much suited for the applications requiring high speed and low power [6].

1.1.3 MTMOS based Schmitt trigger

The conventional Schmitt trigger circuit can be redesigned using Multiple threshold i.e MTMOS technique with the help of which the propagation delay of the circuit gets reduced thus making it suitable for the high-speed applications. In this technique for the Schmitt trigger implementation the transistor having different threshold voltages are used as shown in the fig.4 below. This technique is based upon the concept of the employment of the low and high threshold voltage transistors for controlling the switching of the output in order to have the minimum possible delay. As the greater value and the lesser threshold voltage based transistors are used so the turning on and the turning off of the transistors can be controlled accordingly in order to reduce the amount of the active power dissipation of the circuit making it a good candidate for the low power applications [1].

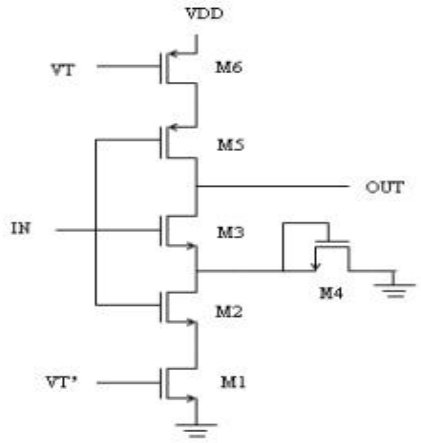
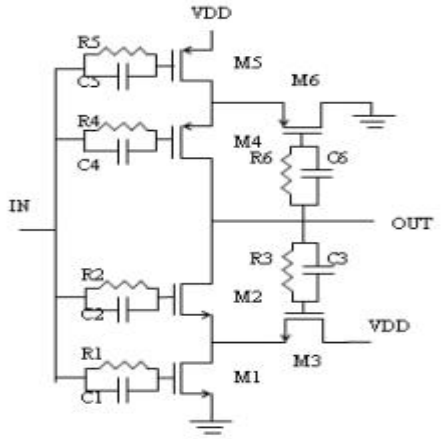


Figure 4 MTMOS based Schmitt trigger Design

1.1.4 FGMOS based Schmitt trigger

The Schmitt trigger can also be implemented using Floating gate CMOS technique as shown in the fig. 5 below:



.Figure 5 FGMOS based Schmitt trigger

In the FGMOS based Schmitt trigger a floating capacitance is connected at the gate terminal of the CMOS transistors below for the purpose of controlling the threshold voltage of the circuit in order to change power dissipation as well as the propagation delay of the circuit. The width of the hysteresis loop was found to be maximum in the case of the FGMOS based Schmitt trigger when compared to the traditional Schmitt trigger circuit thus making it reliable for the circuits requiring better noise-immunity from electromagnetic interferences [1].

1.1.5 Body-Biasing based Schmitt trigger buffer

The Schmitt trigger circuit can also be implemented using the body biasing technique as shown in the fig.6 below. The body control voltages are used in a way because of which threshold

voltage of circuit can be adjusted as a result of which the delay of the circuit gets changed. The body biasing technique is also used for the adjustment of the width of the hysteresis loop thus making it flexible to be used in applications requiring variable width of the hysteresis loop [10].

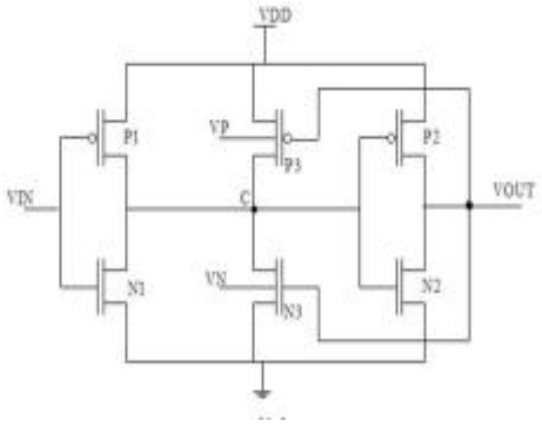


Figure 6 Body-Biasing based Schmitt trigger buffer

CHAPTER 2: REVIEW OF LITERATURE

Suresh Ambothu [6] In this paper the author has presented a Schmitt trigger design on the basis of the usage of Self-bias transistor methodology which is used for the reduction of the static and dynamic i.e. switching power consumption of the circuit. When compared to conventional Schmitt trigger circuit, the self-biased transistor based Schmitt trigger design is able to operate at lesser voltages ranging from (0.8V- 1.5V). The propagation delay of the circuit also gets reduced as the author has redesigned the PMOS circuitry of the Conventional Schmitt trigger and the modification in the PMOS circuitry reduces the overall resistance of the circuit to half there by decreasing the propagation delay and the product of energy component and delay of the circuit.

Joseph et. al.[1] In this paper the author has proposed a Schmitt trigger design suitable for the operation in the sub-threshold conduction region using different low voltage implementation techniques such as Dynamic Threshold MOS (DTMOS), Variable Threshold MOS (VTMOS), Floating Gate MOS(FGMOS), Multiple Threshold MOS (MTMOS) and the analysis on the basis of delay and power for each of the implemented technique has been performed. Out of the above mentioned techniques, the width of the hysteresis loop was found to be maximum in Floating-Gate MOS Schmitt trigger and the width was minimum in case of MTMOS based Schmitt trigger where as the propagation delay was found to be minimum in the MTMOS Schmitt trigger case and it was maximum in the FGMOS Schmitt trigger case, and the dissipation of power was found to be maximum in the case of the DTMOS where as it was found to be minimum in the MTMOS based Schmitt trigger design. These simulation of the designs are carried out at 0.5 volts and these circuits are designed using 180nm CMOS technology.

Kadu et. al.[7] In this paper the author has presented the design of logic gates using Schmitt trigger based upon Variable threshold CMOS technique i.e VTCMOS suitable for the conduction in sub-threshold region for minimization of overall power dissipation, also the reduction in the area of the circuit at the cost of the increase in the propagation delay of system. The percentage of power saving by using VTCMOS technique is approximately 79%. The logic gates have been implemented using Cadence Virtuoso-180nm CMOS technology which are suitable for the low power applications.

Kumar et. al.[8] In the paper, author has improvised the traditional CMOS S.T circuit design for the better noise margin of the system by proposing a design for the increased hysteresis

width which is achieved by using the two feedback loops in contrast to the single positive feedback loop used in the traditional Schmitt trigger circuit, as greater the hysteresis width the greater will be the noise immunity of the circuit. Also the effect of the aspect ratio on the width of the hysteresis loop and the analysis on the basis of the static and the dynamic power is explained in this paper. The simulation of the design is carried out using .25um and .18um CMOS technology.

Vasundara Patel et. al.[9] In this paper a new FinFET based SRAM design has been proposed which uses a modified Schmitt trigger design thus reducing the probability of the read failure and the amount of the power consumed in contrast of the traditional SRAM design. This design is also helpful forsw the reduction in the read and the write time of the SRAM thus making it a better design than the conventional Schmitt trigger based SRAM. The validation of the results for its accuracy is carried out using 32nm FinFET technology in the HSPICE simulator.

Chen et. al. [10] In this paper the author has presented a new design for the Schmitt trigger using the body biasing technique due to which the threshold of the circuit can be adjusted as a result of which the delay of the circuit gets changed, when we apply the body biasing technique in such a way that the threshold voltage of circuit gets reduced, delay of circuit is also reduced, thus making the circuit more suitable and reliable for the high speed and the low voltage applications. The width of the hysteresis loop can also be adjusted by manipulating the body biasing voltages. The simulation of the design is carried out using HSPICE with BSIM4 device model and the designing of the circuit is done using 40nm CMOS technology with 1V.

Kim et. al.[11] In this paper the author has proposed the Schmitt trigger based logic gates capable for the operation in the sub-threshold conduction region using the Variable threshold MOS technique which is used for the adjustment of the minimum conducting voltage of the MOS transistors for improvement of noise withstand capability of the circuit. With the usage of the VTMOS technique the overall power dissipation as well as the area of the circuit gets reduced significantly when comparison is made to the traditional Schmitt trigger logic gates. The verification for the results in terms of the immunity of the circuit are carried out using ISCAS 85 benchmark.

Sapawi et al. [12] In this paper the author has proposed a new design for the Schmitt trigger by manipulating the PMOS section as well as the aspect-ratio of the Conventional Schmitt trigger design for reducing the delay and energy-delay product i.e. EDP of circuit. The effect of the load capacitance on the width of the hysteresis loop is explained and it has been shown that the

width of the hysteresis loop is less sensitive to the change in the load capacitanwce and supply voltage.

Lotze et al. [13] In this paper, the author has presented the analysis of Schmitt trigger logic in depth and has demonstrated the implementation of hardware design with minimum possible supply voltages such as 62mV. The logic gates implemented with the help of Schmitt trigger reflects the only approach for allowing the digital circuits for the operation at sub–threshold voltage supply which are very less to the capacity of CMOS standard logic. Also, the effect of voltage supply reduction on geometrical aspect of Schmitt trigger logic and standard CMOS base logic has been presented, because of which Schmitt trigger gates are more reliable for the supply voltages which are less than 100–120 mV with respect to area and for the supply voltages which are less than 70–80 mV with respect to power dissipation and propagation delay.

Kulkarni et al. [14] In this paper, the author has analysed the Schmitt trigger logic based SRAM cell for very low supply voltage operation and it has been presented that the Schmitt trigger logic based SRAM cell have better read and write operations stability when comparision is made to the standard SRAM . The proposed Schmitt trigger logic based SRAM cell has got a in built mechanism for feedbacks in order to make the circuit more tolerable for process variations.

Arjun et. al.[15] In this paper the author has proposed a new design for the Schmitt trigger based upon the usage of FinFET technique for reducing the consumption of the leakage power and the comparison of the results in the name of propagation delay, leakage power, slew rate and EDP has been done. It has been found that the power dissipation using the FinFET technology was 1.396 in magnitude where as that consumed in the case of CMOS Schmitt trigger is 90.46 which is very high when compared to that consumed in the Schmitt trigger designed using FinFET technology thus making this designing technique reliable for low power applications. The other parameters which are improvised using FinFET technology are delay, leakage power which are found to be very less when compared to the Schmitt trigger designed using CMOS technology thus making this technique much suitable to be used for systems requiring high speed applications. The designing of circuit is carried out at 45nm CMOS technology.

Hang et al.[16] In this paper, the author has proposed a new design of Schmitt trigger on the basis of the usage of the multi input floating gate MOSFET (FGMOS) technique for controlling the hysteresis loop. The most important characteristic of the proposed Schmitt trigger is shifting of the hysteresis window by changing the capacitive coefficients connected on the gate terminal of MOS transistors. The analysis of the presented circuit is carried out on HSPICE simulations with 3.3V power supply.

Nejati et al.[17] In this paper the author has proposed a bulk-driven technique for the designing of low voltage Schmitt trigger which is capable of operating in the sub threshold conduction region. As the author has used the bulk driven technique for the designing of the Schmitt trigger, the threshold voltage in the circuit can be adjusted thereby adjusting the width of the hysteresis loop of the proposed circuit. This design is able to withstand with lower supply voltage as 0.4V and the designing in simulation of the proposed circuit is carried out using 180nm CMOS technology.

Moghaddam et al.[18] In his paper the author has presented a study over a Schmitt trigger logic buffer design using Carbon Nanotube Field Effect Transistors (CNTFET) for less amount of power consumption applications. The circuit designed using CNTFET technique have got very high gain when compared to the CMOS circuits making them much suited for robust design. The Schmitt trigger proposed in this paper has been used for the designing of a hardened latch, which has got more superiority in the process and temperature variations. The simulations are carried out on the Stanford CNTFET model using 16nm technology.

Raza et al.[19] In this paper the author has presented a design for Schmitt trigger and its layout using pull-up section and pull-down section. Also, semi-custom and full-custom layout design of the Schmitt trigger has been shown and the comparison of the results with respect to power dissipation and surface area has been presented. It has been shown that the layout which is generated automatically covers maximum area and consumes much of the power when compared to semi-custom and full-custom layout design of Schmitt trigger. The simulation has been carried out using 90nm CMOS technology.

Sreenivasan et.al.[20] In this paper a Single ended Static RAM bit cell using the Schmitt trigger logic has been presented in order to have high static noise margin for read and write operations.

The author has used the concept of Dual-threshold CMOS technique, the proposed circuit is efficient enough to with stand with the lower supply voltages. The designing and the simulation of the circuit design has been carried out using 45nm CMOS technology with the supply voltage of 0.45 V. It has been presented in the simulation analysis that 0by using proposed design for the SRAM designing, there is a drastic decrease in the power dissipation for the hold and the write operations for the SRAM bit-cell i.e. there is an approximate decrease of 89% for the average static power dissipation for the hold operation and an approximate decrease of 39% for the write operation by using the proposed Schmitt trigger for the SRAM bit-cell designing.

Ahmad et. al.[21] In this paper the author has proposed Schmitt trigger logic using Single ended Static RAM cell due to which the noise margin for both the read and the write operation gets increased there by making the system having high SNM with the lesser amount of the power consumption. The Conventional six transistor based SRAM cell faces the problem of the failures during read and the write operation when value of supply voltage is scaled down to a greater extent. The SRAM have got Bit-Line (BL) and Word-Line for the purpose of reading and writing and most of the power in the case of read and the write operation was consumed during the BL switching that is done during the read and the write operation. Single ended SRAM cell basically reduces this BL switching power thus making the circuit efficient to be used at low power but at the slight expense of elevation in the access time of the read and the write operation. This circuit offers higher amount of stability when subjected to the change in the supply voltage, temperature and so on.

CHAPTER 3: SCOPE OF THE STUDY

Schmitt trigger is basically used to suppress the effect of electromagnetic interference present in the system thereby enhancing the noise margin of the system. With the scaling down of the voltage supply, the circuits are becoming much prone to electromagnetic noise. So, the designing of a Schmitt trigger is really important. Schmitt trigger provides a valuable solution for improving the sensitivity of the circuit from the electromagnetic interference that means they are used for enhancing the Static Noise Margin of the circuit at the cost of the power and delay consumption. Schmitt trigger is also known by the name of the bi-stable circuit because of its capability to work on two different threshold values. Hence here, a low power, low voltage and high speed Schmitt trigger is designed to consume a very less amount of power so that it can be used for ideal cases. Here a Schmitt trigger capable for sub-threshold conduction operation using the Variable threshold MOS technique which is used for the adjustment of the minimum conducting voltage of the MOS transistors for the improvement of the noise immunity of the circuit is designed. With the usage of the VTCMOS technique the overall power dissipation as well as the area of the circuit gets reduced significantly when comparison is made to the traditional Schmitt trigger. In the case of VTCMOS based Schmitt trigger design, as the channel length and width of transistor increases, system output was improved but increasing channel length and width will increase the transistor size also due to which total area of the system will increase. Due to increase in size of transistor the dynamic power of the system is also very less because electrons have enough space in the channel to travel from source to drain. Due to large channel length and width collision between electrons is very less and hence power loss is very less. Also, a new design for the Schmitt trigger using the body biasing technique due to which the threshold of the circuit can be adjusted as a result of which the delay of the circuit gets changed, when we apply the body biasing technique in such a way that the threshold voltage of circuit gets reduced, delay of circuit is also reduced, thus making the circuit more suitable and reliable for the high speed and the low voltage applications. The width of the hysteresis loop can also be adjusted by manipulating the body biasing voltages. The Schmitt trigger has got a capability to operate on two different threshold voltages represented with the help of a hysteresis loop. This property of the Schmitt trigger also facilities the conversion of the analogue signal into digital one thus resulting in the reshaping of the pulses. A Schmitt trigger is basically the comparator circuit with the positive feedback signal which means that the loop gain of the circuit is greater than one. The feedback is used for the reason of providing different threshold voltages to the Schmitt trigger in order to have the

hysteresis property for the purpose of improving the noise sensitivity of the CMOS device so that the device can have a noise stable operation. Schmitt trigger functions as a signal restoring circuit which means that they are used to infer out the amount of the original input signal information present by eliminating the noise content from it and this functionality of the system has been verified.

CHAPTER 4: OBJECTIVES OF STUDY

The main objective is to implement a CMOS Schmitt trigger with high speed low voltage and better hysteresis width which will result in increased noise immunity for the digital as well as analogue circuits. As the supply voltage is reducing day by day because of which the systems are becoming more prone to noise effects, so we have implemented a system using the body biasing technique which has enabled the system to withstand with the different scenarios of noise as the different voltages at the body terminals of the CMOS transistors are used to adjust the width of the hysteresis loop thereby making the system to withstand under different noise conditions. Also, the system capable of high speed application is implemented because the threshold voltages of the individual transistors has been reduced due to which the delay of the system gets reduced and a new system capable of providing the least amount of switching power has been implemented and the results has been analyzed based on the different models of Schmitt trigger.

CHAPTER 5: RESEARCH METHODOLOGY

The Schmitt trigger can be implemented using various design methodologies depending upon the performance requirement in terms of the delay, power and area of the circuit design. Based upon the design specifications there are several approaches to design the Schmitt trigger circuit suited for high speed, less amount of voltage and less power consumption based applications. We have used two techniques for implementing the Schmitt trigger design, the methodologies used for the implementation of the Schmitt trigger buffer design are Body-biasing and VTCMOS technique out of which by using the body biasing technique the delay of the Conventional CMOS Schmitt trigger has been reduced and by using the VTCMOS technique the switching power of the traditional design has been reduced. This section explains the mathematical modelling of the body biased based Schmitt trigger design there by showing all the operating modes as well as the equations for the input and the output currents. The implemented Schmitt trigger circuit is composed of two sub-sections i.e. first section and second section where section-1 is composed of two transistors PM0 and NM0 and section-2 is composed of two inverter circuits (PM1, NM1, PM2, NM2) in which one inverter circuit's body is controlled using body biasing technique for adjusting the threshold of the circuit and controlling the switching of the output in order to reduce propagation delay of the circuit. The operation of the body biased Schmitt trigger is as follows, as the implemented circuit is behaving as a buffer so when the voltage at the input terminal is low i.e. .when V1 is low, the voltage at the output terminal also goes low i.e. V_{out} is also low so, the CMOS transistors NM0, NM3 operates in cut-off region and the transistors PM0, PM1 operates in saturation region. But when the input is changed for a transition i.e. when the input undergoes a transition i.e. it is changed from low logic to high logic the transistor NM0 is turned on and the voltage at node 'x' decreases as it is dropped down to ground through the transistor NM0.The voltage at node 'x' is used to control the switching at the output terminal i.e. V_{out}, as the voltage V2 at the body terminal of PM2 is used for setting out the threshold voltage of PM2 thus it helps in switching the output with lesser amount of propagation delay.

When the transistor NM0 goes in saturation region, the current through the transistor NM0 is equal to the current through the transistors PM0 and PM2. So we can represent the equations for current flowing through circuit as:

$$\frac{\mu_p C_{ox} W_{PM0} (V_{DD} - V_{LH} - |V_{TH0,PM0}|)^2}{2L_{PM0}} + \frac{\mu_p C_{ox} W_{PM2}}{2L_{PM2}}$$

$$(V_{DD} - V_{LH} - |V_{TH,PM2}|)^2 = \frac{\mu_n C_{ox} W_{NM0} (V_{LH} - V_{TH0,NM0})^2}{2L_{NM0}}$$

$$|V_{TH,PM2}| = V_{T0} - \gamma(\sqrt{|2\varphi_F| + V_p - V_{DD}} - \sqrt{|2\varphi_F|}$$

$$V_{LH} = \frac{m((V_{DD} - |V_{TH0,PM0}|) + n(V_{DD} - |V_{TH,PM2}|) - V_{TH0,NM2} + \mathrm{d}}{m + n + 1}$$

where

$$\mathrm{d} = \sqrt{n(V_{DD} + V_{TH0,NM0} - |V_{TH0,PM0}|)^2 + m(V_{DD} + V_{TH0,NM0} - |V_{TH,PM3}|)^2 + mn(V_{TH0,PM0} - |V_{TH,PM2}|)^2)}$$

$m=\frac{K_{P1}}{K_{N1}}$, $n=\frac{K_{P3}}{K_{N1}}$ where K_N, K_P are given as $\frac{\mu C_{ox} W}{2L}$

In a similar way, when the voltage at the input terminal is high i.e. when the input goes high the voltage at the output terminal is also changed to a voltage level equivalent to the voltage at the input terminal i.e. the output also goes high because of which transistors PM0, PM2 operates in cut-off region and NM0, NM2 operates in saturation region. . But when the input is changed from high to low the transistor PM0 is turned on and the voltage at node 'x' increases as it is dropped up to Vdd through the transistor PM0.The voltage at node 'x' is used to control the switching at the output terminal i.e. V_{out}, as the voltage V3 at the body terminal of NM2 is used for setting out the threshold voltage of NM2 thus helping in switching the output with lesser amount of propagation delay [10].

When the transistor PM0 goes in saturation region, the current through the transistor PM0 is equal to the current through the transistors NM0 and NM2. So we can write the equation for current flowing through the circuit as:

$$\frac{\mu_n C_{ox} W_{NM0} (V_{HL} - |V_{TH0,NM0}|)^2}{2L_{PM0}} + \frac{\mu_N C_{ox} W_{NM2}}{2L_{NM2}}$$

$$(V_{HL} - |V_{TH,NM2}|)^2 = \frac{\mu_P C_{ox} W_{PM0} (V_{DD} - V_{HL} - V_{TH0,PM0})^2}{2L_{PM0}}$$

$$V_{HL} = \frac{p(|V_{TH0,NM0}|) + q(|V_{TH,NM2}|) - V_{DD} + V_{TH0,PM0} + \mathrm{e}}{q + p + 1}$$

$$\mathrm{e} = \sqrt{q(V_{DD} + V_{TH,NM2} - |V_{TH0,PM0}|)^2 + p(V_{DD} - V_{TH0,NM0} - |V_{TH0,PM0}|)^2 + pq(V_{TH0,NM0} - |V_{TH,NM2}|)^2)}$$

$m=\frac{K_{N1}}{K_{P1}}$, $n=\frac{K_{N3}}{K_{N1}}$ where K_N, K_P are given as $\frac{\mu C_{ox} W}{2L}$

It is seen from the equations of V_{LH} and V_{HL} that these voltages are dependent upon the body biasing voltages V2 and V3 respectively thus the body biasing voltages are used to control the switching action of the output voltage thus change the delay of the circuit. As in this case the body-biasing voltages are chosen in such a way that we get the minimum possible value of the delay.

CHAPTER 6: IMPLEMENTED DESIGNS

In this section the various implemented designs of the Schmitt trigger have been presented starting from the conventional 6T based CMOS Schmitt trigger till the Schmitt trigger design suitable for high speed low voltage applications. All the designs have been implemented and simulated using 180nm CMOS technology.

6.1 Traditional CMOS Schmitt trigger

A conventional Schmitt trigger circuit is basically composed of two sub-sections, section 1 and section 2, where section 1 represents the PMOS circuitry consisting of three PMOS transistors i.e PM0, PM1 and PM2 as shown in the figure below which are responsible for the generation of the lower threshold switching voltage VL and the section 2 represents the NMOS circuitry consisting of three NMOS transistors i.e. NM0, NM1, and NM2 which are responsible for the generation of the upper threshold switching voltage VH. The transistors NM2 and PM2 are used for providing the positive feedback for the purpose of enhancing the noise immunity of the circuit.

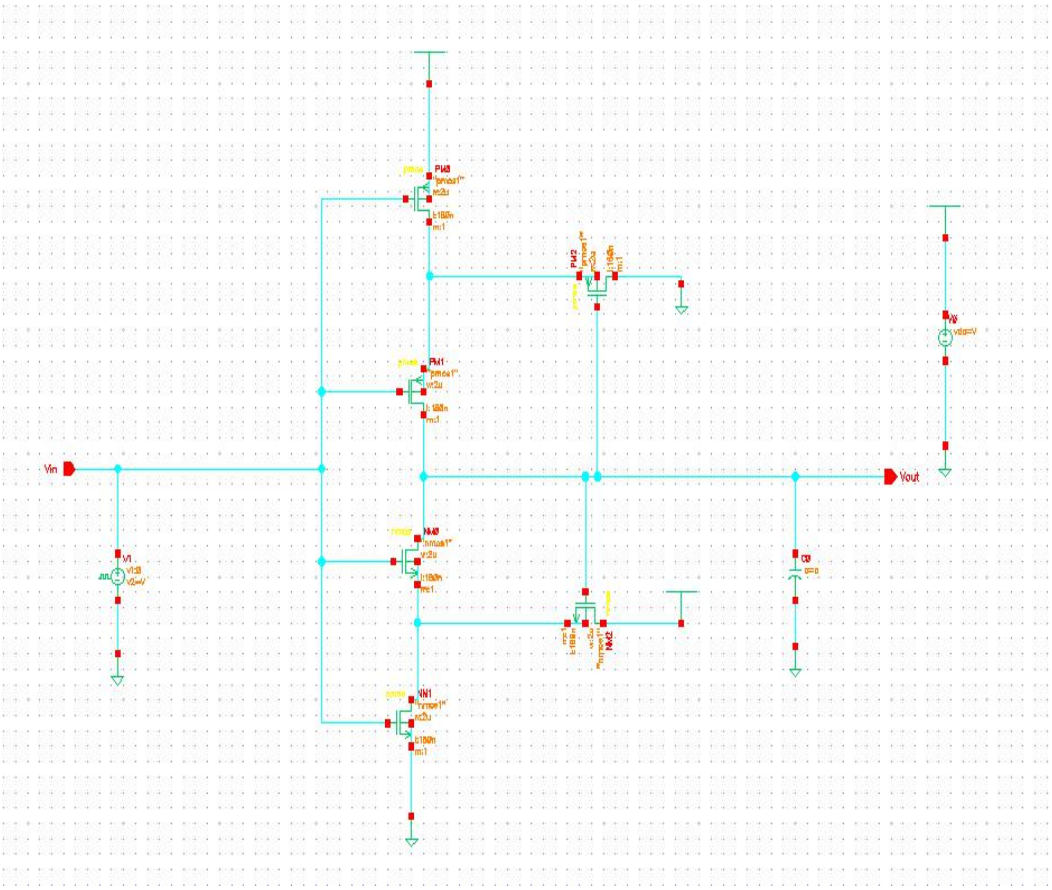


Figure7: Conventional 6T based Schmitt trigger Design

6.2 4T based CMOS Schmitt trigger

The traditional CMOS Schmitt trigger uses six transistors for the purpose of providing the hysteresis property which is basically used for enhancing the noise immunity of the system but when analysed for various design parameters like delay and power the results obtained were not very much appropriate. So, a new design has been implemented for improving the design parameters of the system which is shown in the figure below. The modified Schmitt trigger design is composed of four transistors PM0, NM0, NM1, NM2 out of which the transistor NM2 is used for providing the positive feedback. As this modified circuit has got less number of transistors in P-section so the overall delay and power dissipation of circuit has been reduced when compared to the traditional CMOS Schmitt trigger design.

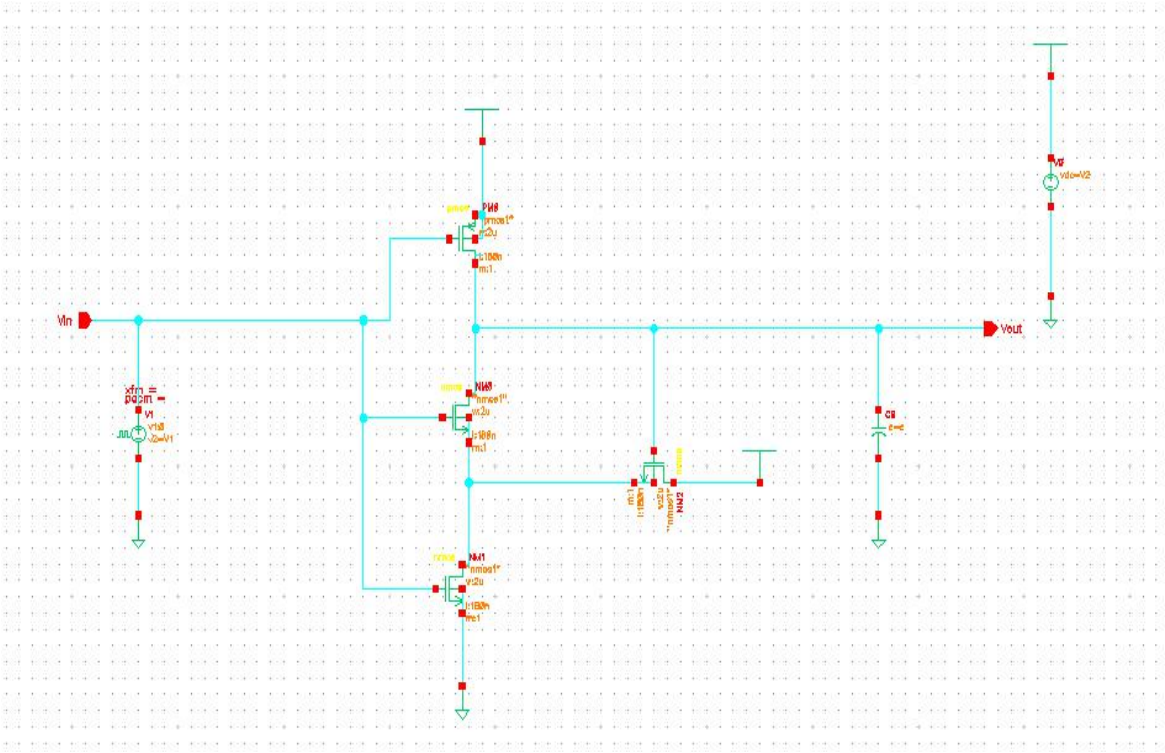


Figure 8: Modified Schmitt trigger Design

6.3 Body Biasing based CMOS Schmitt trigger buffer

The above implemented Schmitt trigger designs are not much suited for applications requiring more immunity in terms of noise and high-speed operations so a new design using the body-biasing technique have been implemented. The implemented circuit is composed of two sub sections i.e section-1 and section-2 where section-1 is composed of two transistors PM0 and NM0 and section-2 is composed of two inverter circuits (PM1, NM1, PM2, NM2) in which one

inverter circuit's body is controlled using body biasing technique for adjusting the threshold of the circuit and controlling the switching of the output in order to minimize the propagation delay of the circuit. Also by controlling the voltages at the body terminal of the transistors PM1 and NM1 the width of the hysteresis loop is adjusted thus making it much suited for the applications requiring the variable noise immunity.

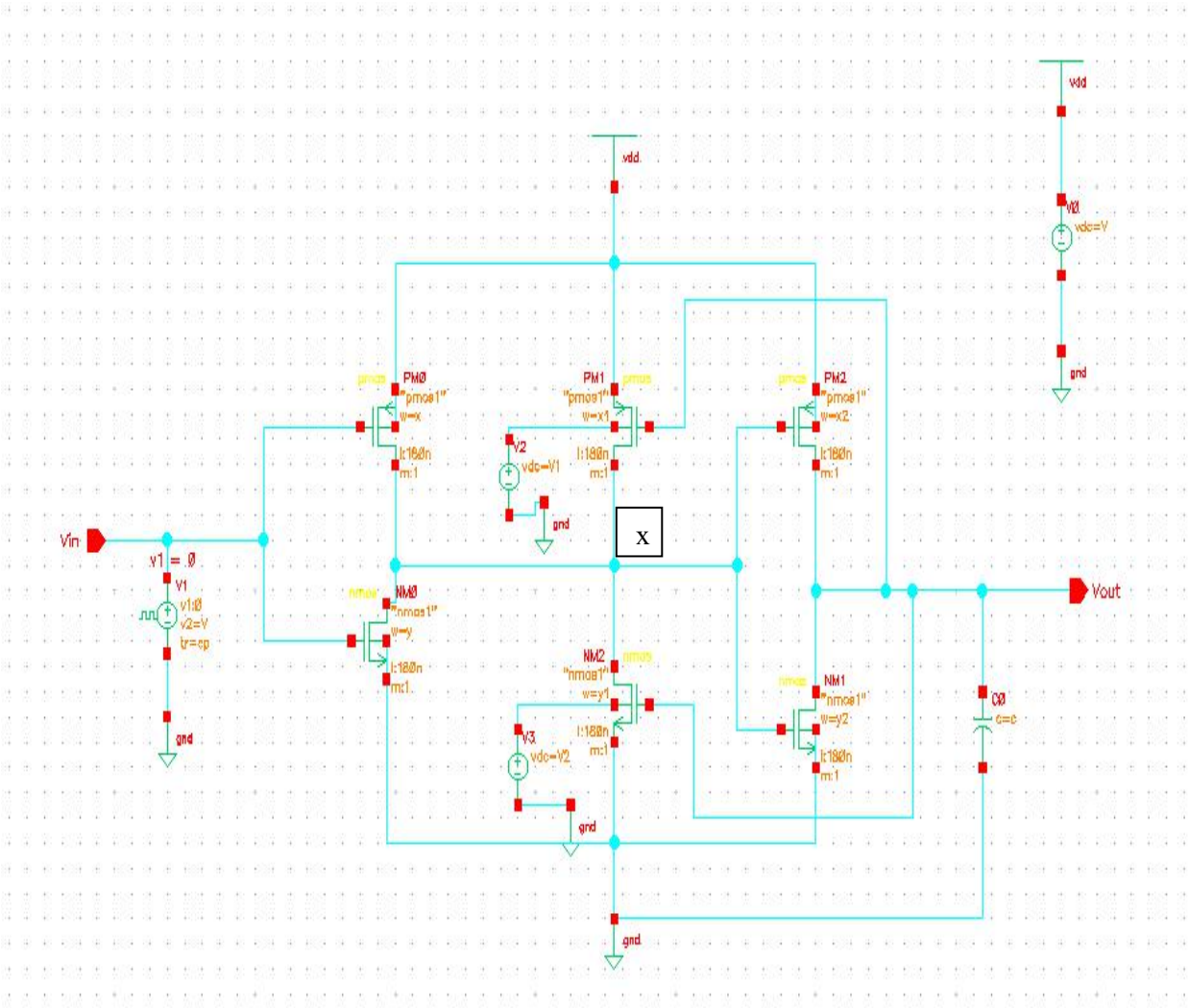


Figure 9: Body biasing based Schmitt trigger Design

6.4 VTCMOS based CMOS Schmitt trigger buffer

The designs presented in the above figure are not suited for sub-threshold conduction operation so Schmitt trigger capable for sub-threshold conduction operation using the Variable threshold MOS technique which is used for the adjustment of the minimum conducting voltage of the MOS transistors for the improvement of the noise immunity of the circuit. With the usage of the VTCMOS technique the overall power dissipation as well as the area of the circuit gets reduced significantly when comparison is made to the traditional Schmitt trigger.

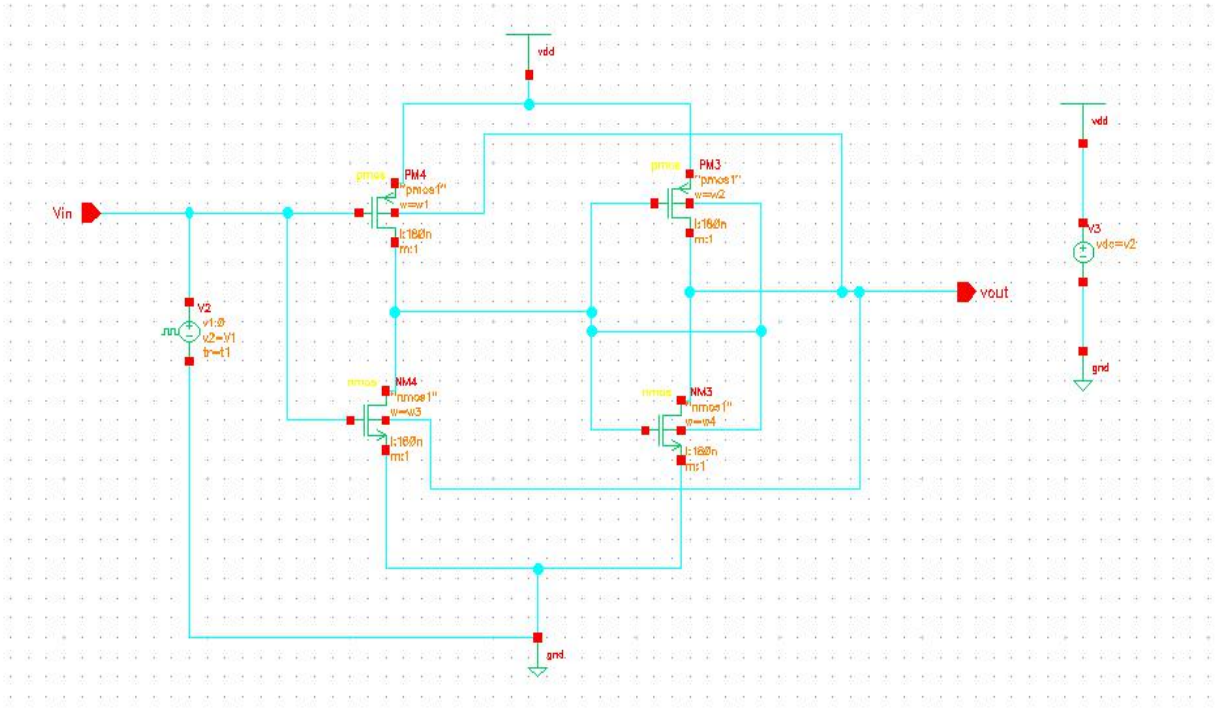


Figure 10: VTCMOS Schmitt trigger Buffer

6.5 NAND GATE based design using Conventional Schmitt trigger

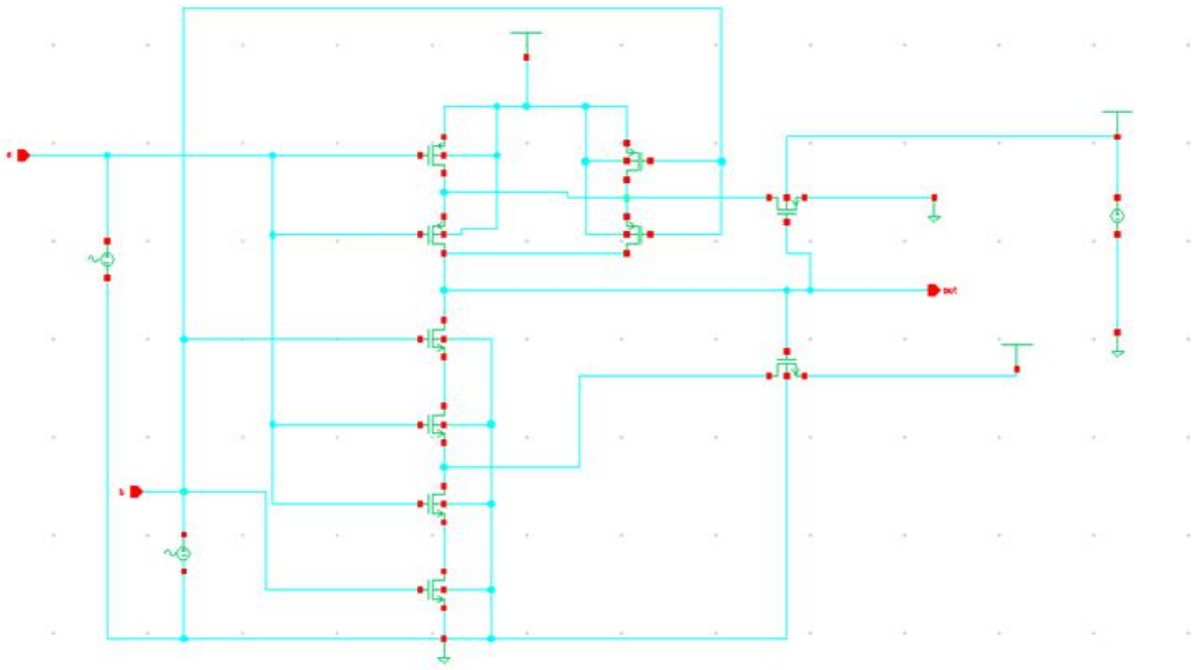


Figure 11: Schematic of the Schmitt trigger based NAND Gate

The figure above shows the schematic of the universal logic gate implemented using traditional CMOS Schmitt trigger design which is composed of in total of eight transistors. As Schmitt

trigger is used to remove the noise from the system, so a NAND gate has been implemented to verify the functionality of Schmitt trigger to suppress the effect of noise from system.

CHAPTER 7: RESULTS AND DISCUSSION

The Schmitt trigger is a bi-stable circuit because of its capability to work on two different threshold values. This property of the Schmitt trigger also facilities the conversion of the analogue signal into digital one thus resulting in the reshaping of the pulses. The figures below show the values of two different threshold voltages obtained for different design of Schmitt trigger.

7.1 Hysteresis Loop of Conventional CMOS Schmitt trigger

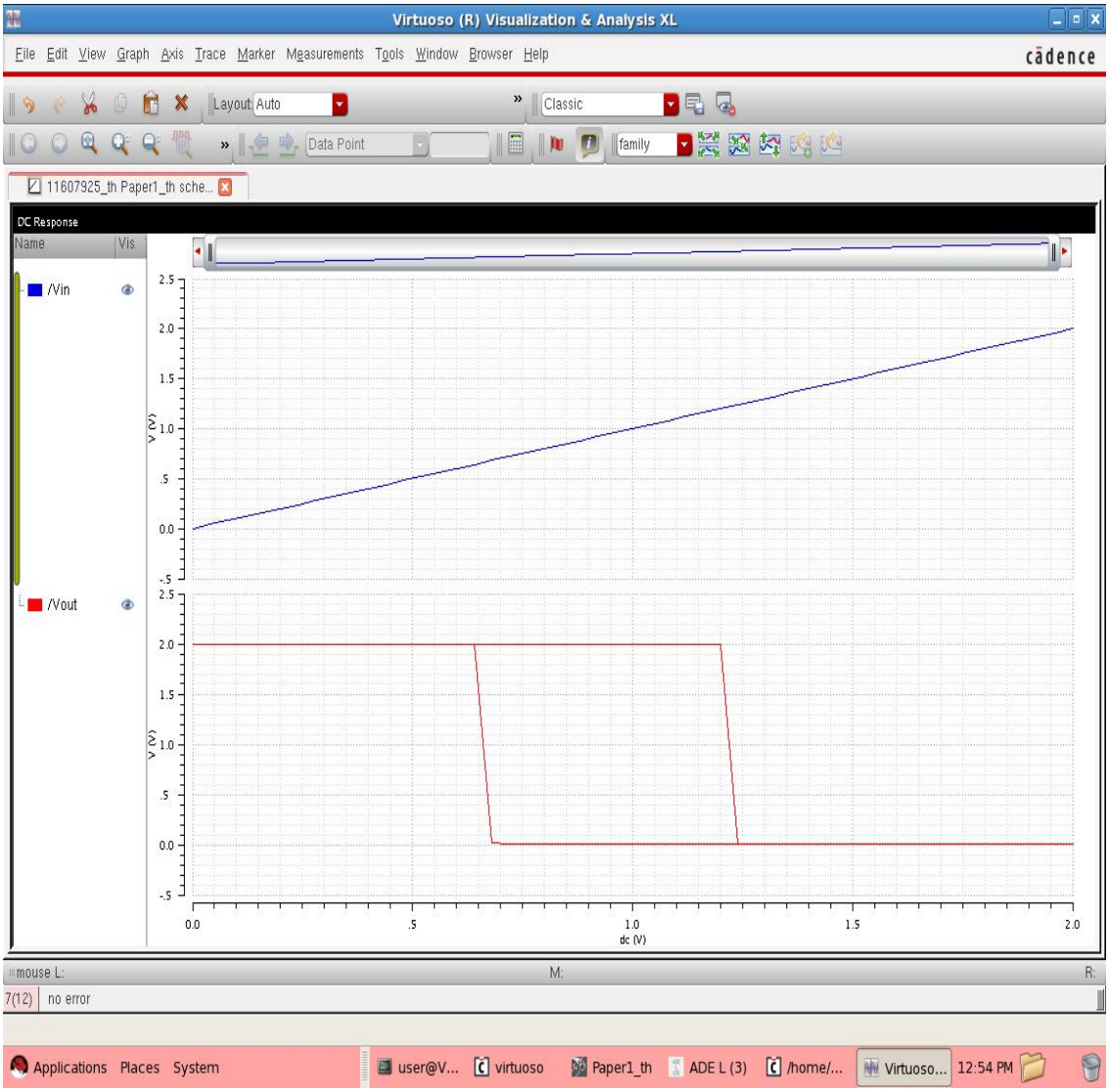


Figure 12: Hysteresis loop width of 6T based Schmitt trigger Design

The figure above shows that the width of the hysteresis loop for the conventional CMOS Schmitt trigger lies in the range of 660.345mV-1.219V.

7.2 Hysteresis Loop of 4T based CMOS Schmitt trigger Design

Figure 13: Hysteresis loop width of 4T based Schmitt trigger Design

The figure above shows that the width of the hysteresis loop for 4T based CMOS Schmitt trigger lies in the range of 0.93V-1.23V.

7.3 Hysteresis Loop of Body biasing based CMOS Schmitt trigger Design

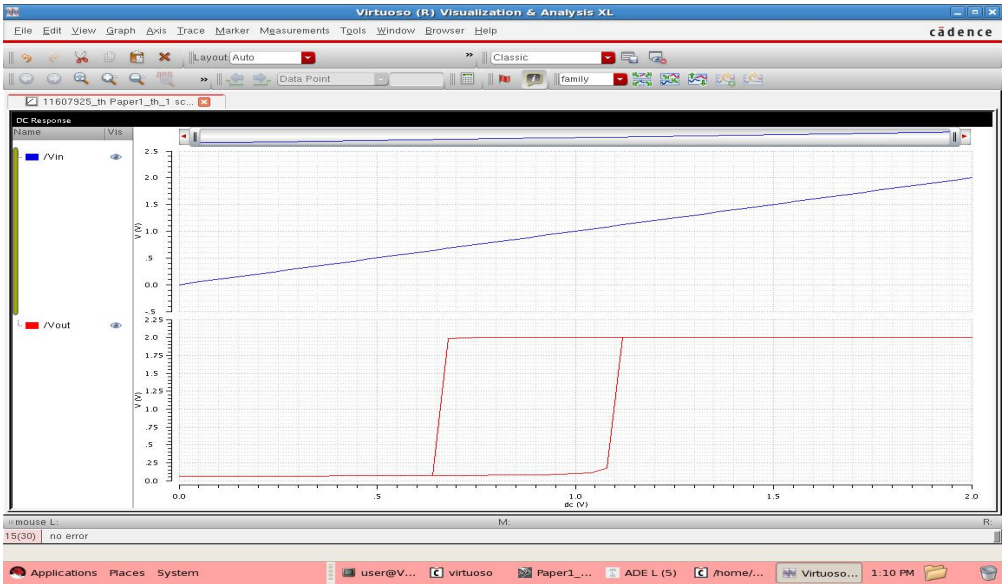


Figure 14: Hysteresis loop width at V_n=1.2V and Vp=0.5v for body biasing based Schmitt trigger Design

The figure above shows that the width of the hysteresis loop for 4T based CMOS Schmitt trigger lies in the range of 658.81mV-1.097V.

7.4 –Hysteresis Loop for VTCMOS based CMOS Schmitt trigger Design

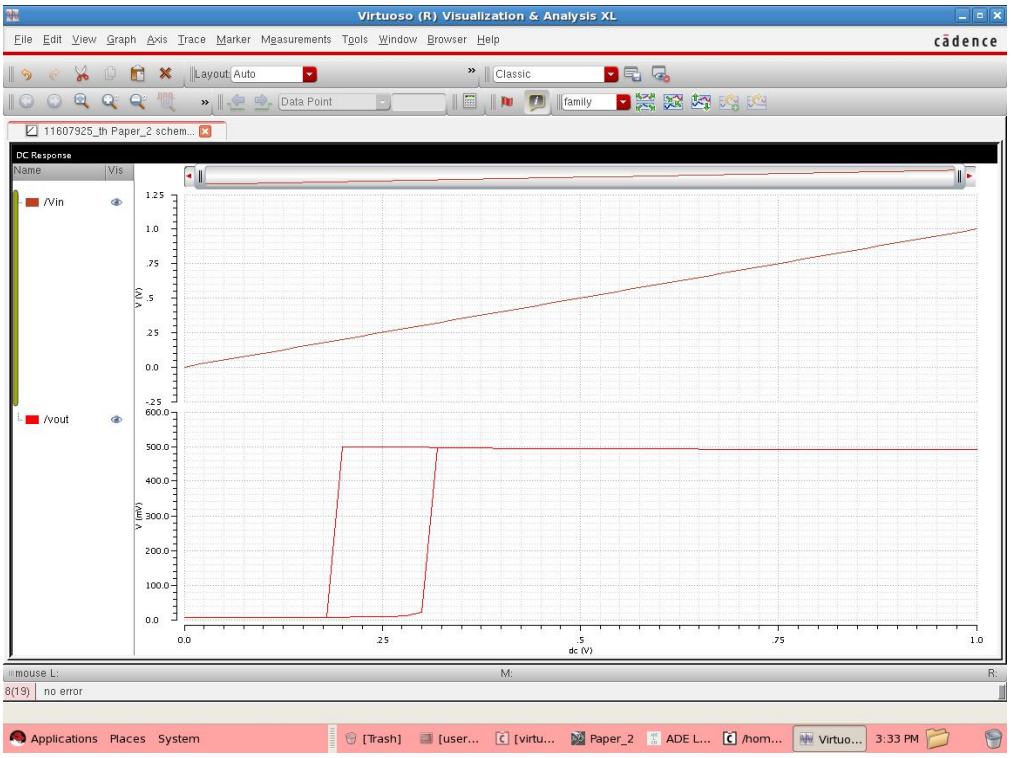


Figure 14: Hysteresis loop width for VTCMOS based Schmitt trigger Design

7.5 Hysteresis Loop of CMOS Schmitt trigger based NAND Gate

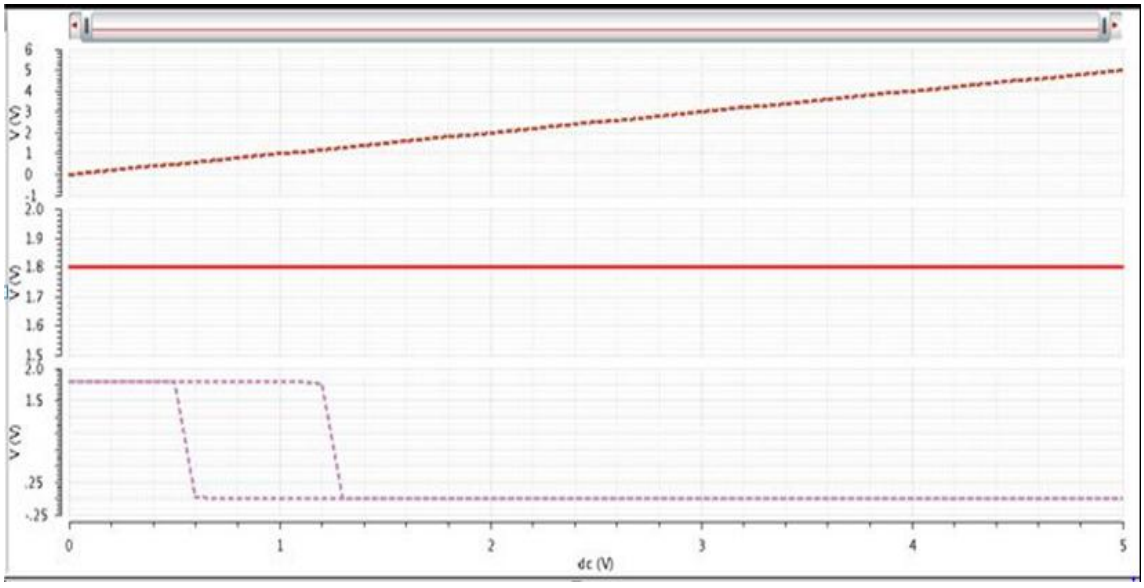


Figure 15: Hysteresis loop width for Schmitt trigger based NAND Gate Design

7.6 Simulation Results of Conventional CMOS Schmitt trigger

This section represents the input output characteristics for Schmitt trigger simulated using 180nm technology in Cadence Virtuoso.

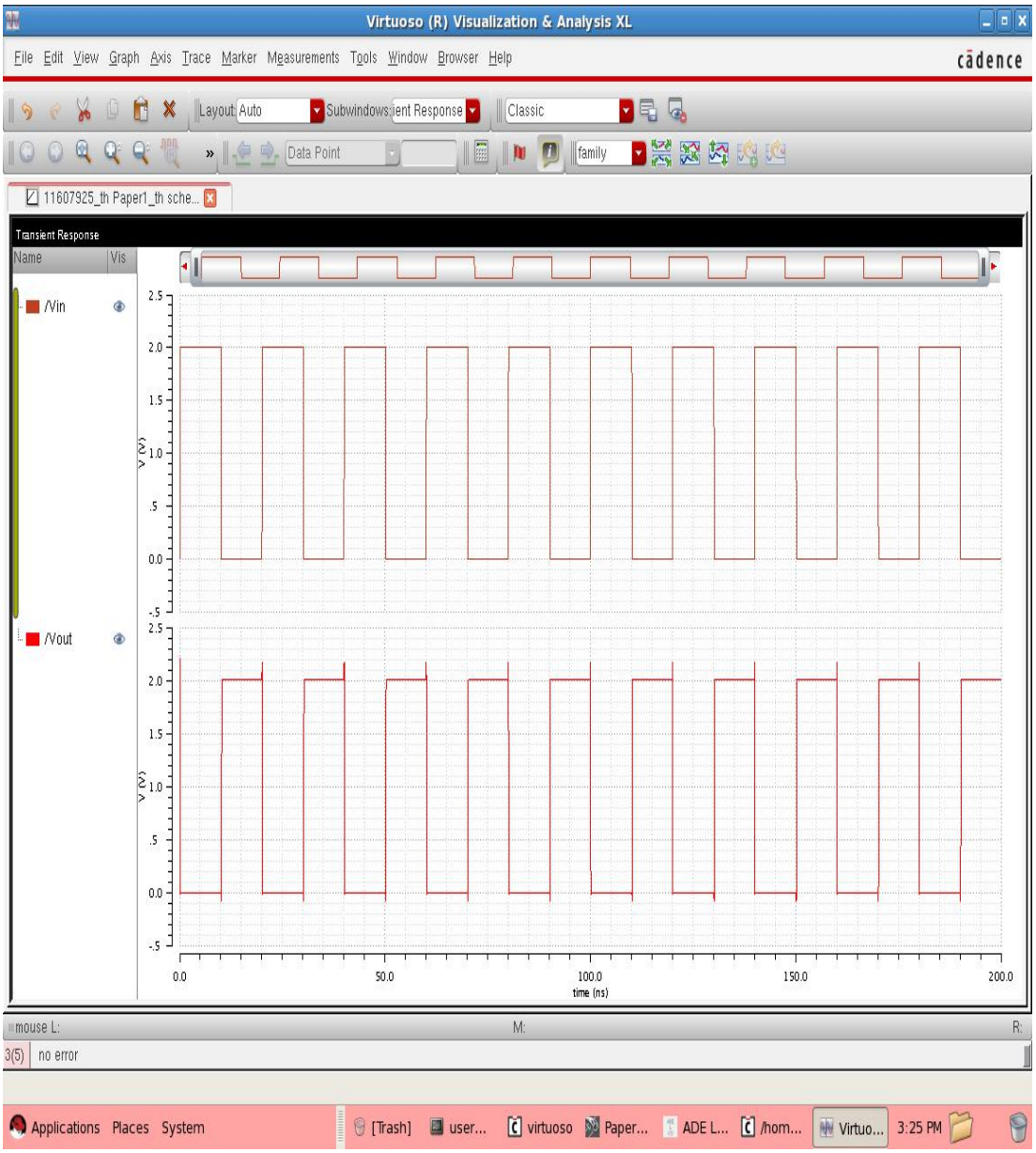


Figure 16: Transient Response for 6T based Schmitt trigger Design

It can be analyzed from figure 16 that the 6T Schmitt trigger(conventional design) design gives an inverted output i.e. when the input is at level zero the pmos section is on and the output goes to a high logic level. And when the input is at level one the NMOS section is on and the output drops to ground.

7.7 Simulation Results of 4T based CMOS Schmitt trigger

Figure 17: Transient Response for 4T based Schmitt trigger Design using pulse wave as Input

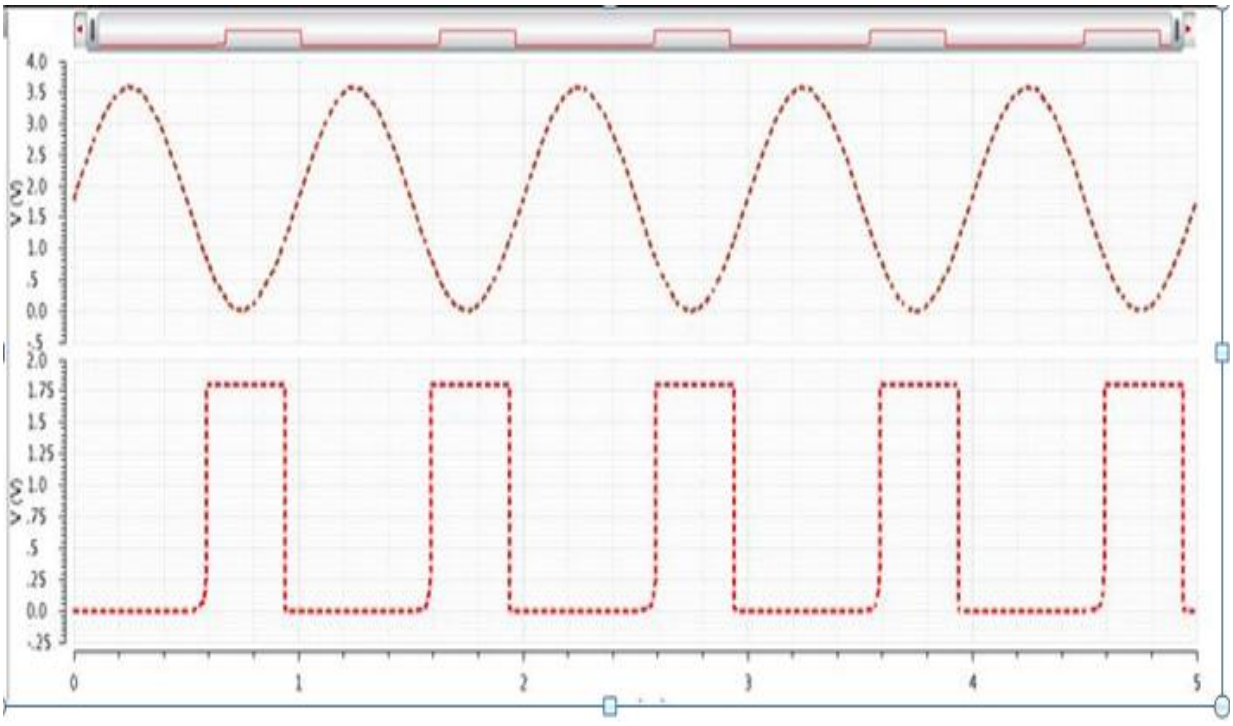


Figure 18: Transient Response for 4T based Schmitt trigger Design using Sinusoidal wave as Input

It can be analyzed from figure-18 that the 4T based Schmitt trigger design gives an inverted output i.e. when the input is at level zero the pmos section is on and the output goes to a high logic level. And when the input is at level one the NMOS section is on and the output drops to ground.

7.8 Simulation Results of Body Biasing based CMOS Schmitt trigger

Figure 19: Transient Response for Body biasing based Schmitt trigger Design at Vn=1.2v and Vp=0.5v

It can be analyzed from figure-19 that the body biasing based Schmitt trigger design acts as a buffer. It is also clear that input-output voltage is range is also same for the buffer i.e. input is 2V and output is also of same level.

7.9 Simulation Results of VTCMOS Schmitt trigger

Figure 20: Transient Response of VTCMOS Schmitt trigger

The above figure shows transient response of VTCMOS Schmitt trigger. As the channel length and width of transistor increases, system output was improved but increasing channel length and width will increase the transistor size also due to which total area of the system will increase. Due to increase in size of transistor the dynamic power of the system is also very less because electrons have enough space in the channel to travel from source to drain. Due to large channel length and width collision between electrons is very less and hence power loss is very less.

7.10 Simulation Results of CMOS 6T Schmitt trigger based NAND Gate

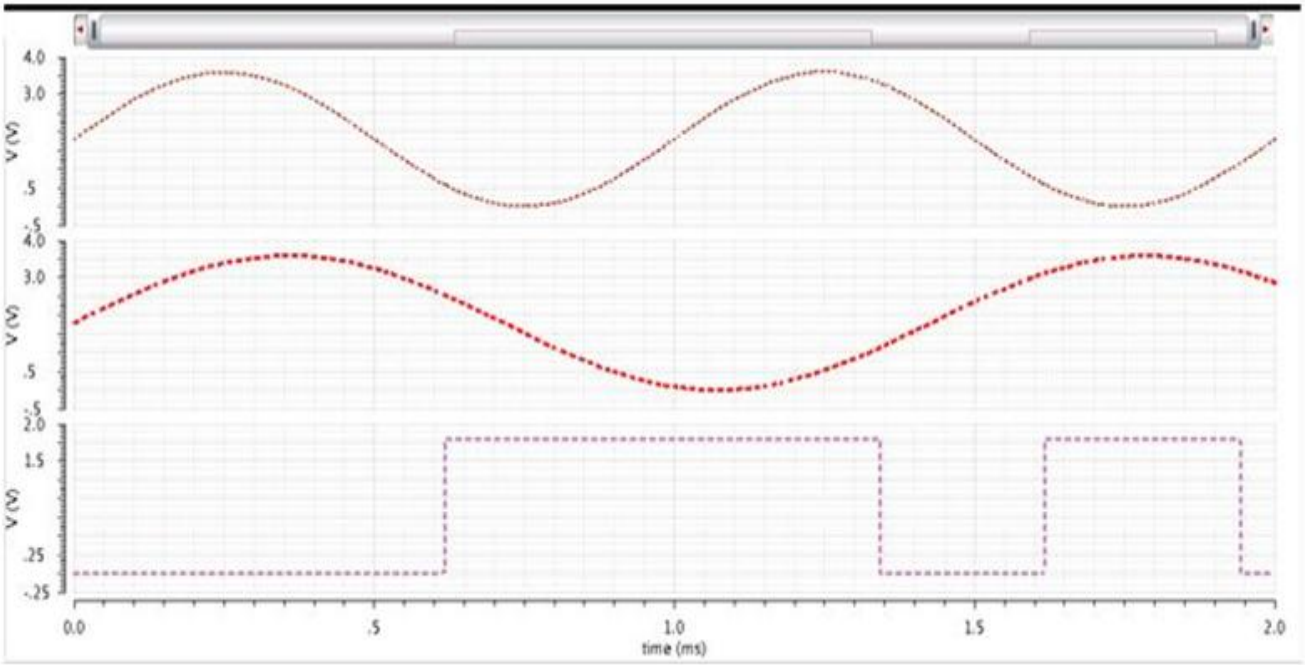


Figure 21: Transient Response for 6T Schmitt trigger based NAND Gate

The above figure shows transient response of NAND gate using 6t model of Schmitt trigger. As Schmitt trigger is used to remove the noise from the system so i have given sinusoidal signal to the system at both inputs of NAND gate and resulting output is a pulse wave which shows that the 6t model is removing noise and is performing basic task of Schmitt trigger.

7.11 Analysis of Different Designs of Schmitt trigger

In this section the different designs of Schmitt trigger have been compared on the basis of different design parameters such as delay, switching power and so on. For delay analysis i have added a load capacitance at the output of every kind of Schmitt trigger. Different values of load capacitances were taken for the analysis purpose.

7.11.1 Analysis of Body biased Schmitt Trigger

Below figure represents delay analysis of body biased Schmitt trigger. Different values of delay were taken for different capacitive load as well as different Vn and Vp values. System is giving minimum delay when Vn is approaching to Vdd and Vp is approaching to ground voltage. Table 1 represents value of capacitance used and value of Vn and Vp for calculation of delay at output.

Table 1: Value of delay (us) for different capacitance (pF)

Capacitor	Delay at vn=vp=1.5	Delay at vn=vp=1.2	Delay at vn=1.2 vp=0.5	Delay at vn=1 vp=0.5	Delay at vn=1.6 vp=0.5
0	53.5	53.95	48.95	51.9	46.66
0.005	55.15	55.2	50.85	53.5	48.4
0.01	56.75	56.45	52.8	55.34	50.1
0.015	58.4	57.65	54.75	57.04	52.04
0.02	60	58.9	56.75	58.65	54.01
0.025	61.65	60.05	58.6	59.56	55.9

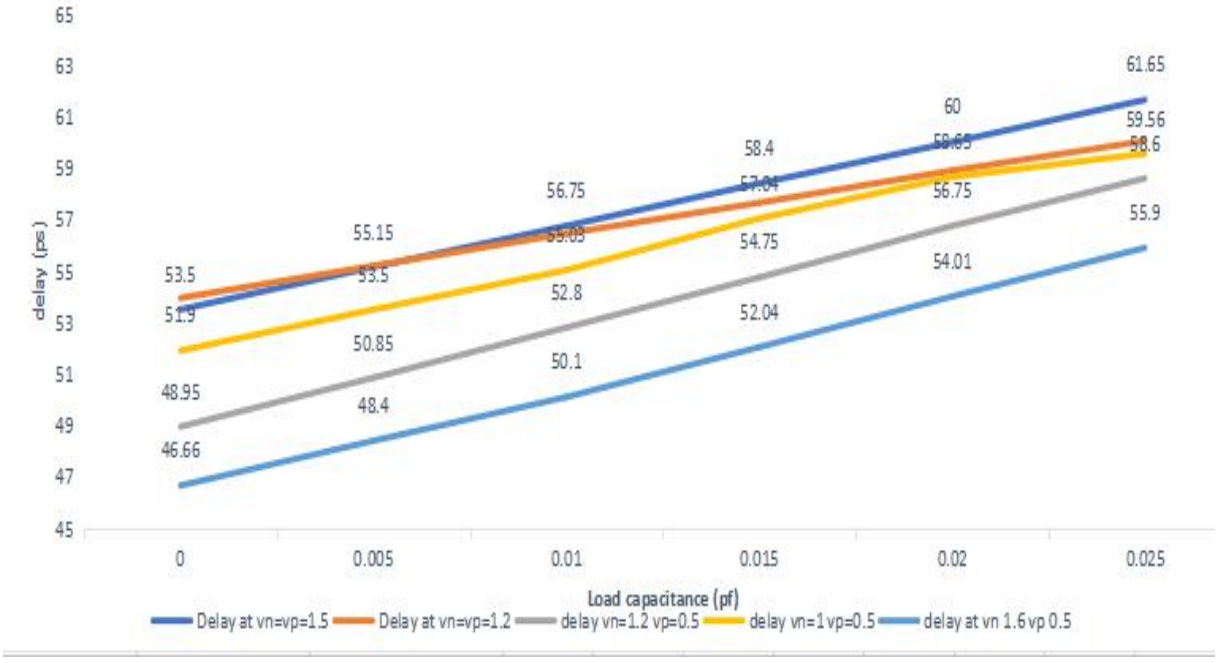


Figure 22: Delay Analysis of body biased Schmitt trigger at different Vn and Vp value

7.11.2 Analysis of 6T, 4T and Body biased Schmitt Trigger

Below figure represents delay analysis of 6T, 4T and Body biased Schmitt trigger. Body biased Schmitt trigger is taken with Vn approaching to Vdd and Vn approaching to ground. Out of the three considered Schmitt triggers, body biased circuit has minimum delay and 6T model i.e. conventional model of Schmitt trigger is having maximum delay. Table 2 shows delay values for 6T, 4T and body biased Schmitt trigger for different capacitive loads

Table 2 Delay analysis for 6T, 4T and body biased Schmitt trigger

Capacitor	Delay in conventional S.T	Delay in 4T S.T	Delay of body biased S.T
0	57.5	45.58	48.95
0.005	72	46.57	50.85
0.01	85.75	55.2	52.8
0.015	99.05	63.25	54.75
0.02	112.3	71.25	56.75
0.025	125.3	79.15	58.6

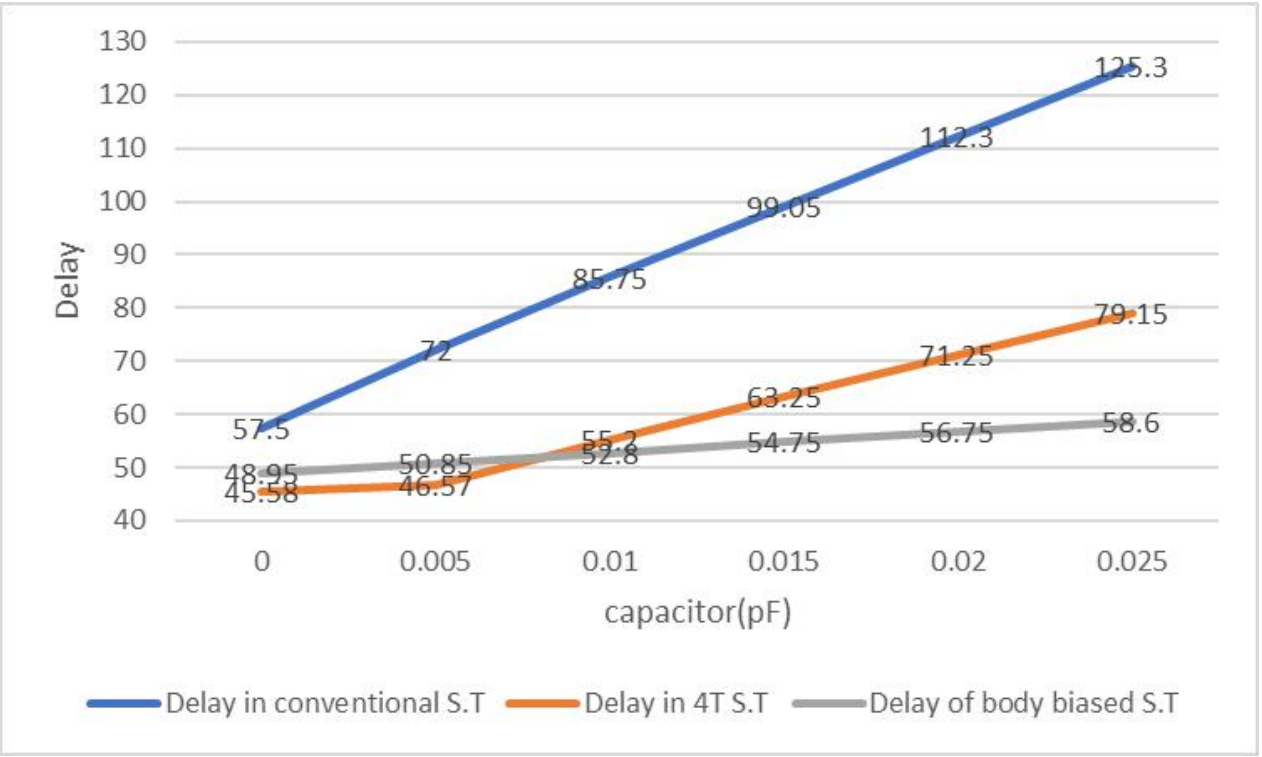


Figure 23: Delay Analysis of 6T, 4T and Body biased Schmitt trigger

7.11.3 Power Analysis of 6T, 4T and VTCMOS Schmitt Trigger

Below figure shows analysis on dynamic power of 4T, 6T and VTCMOS Schmitt transistor with different capacitive load at output. It is observed that power loss in 6T transistor is max and as load capacitance value is increasing power also increases. 4T has a moderate power consumption among three models. Also in 4T model as capacitive load increases, dynamic power also increases. The third model i.e. VTCMOS model is having minimum power consumption. Also with increase in capacitive load dynamic power is not affected as compared to other models for same value of capacitive load. Table 3 shows dynamic power of 6T, 4T and VTCMOS transistor for different capacitive loads

Table 3 Dynamic power of 6T, 4T and VTCMOS transistor

Capacitor	Power_6T	Power_VTCMOS	Power_4T
0	58.51	5.579	42.17
0.005	59.43	5.58	43.17
0.01	60.4	5.59	44.17
0.015	61.37	5.609	45.18
0.02	62.34	5.617	46.2
0.025	63.31	5.626	47.23

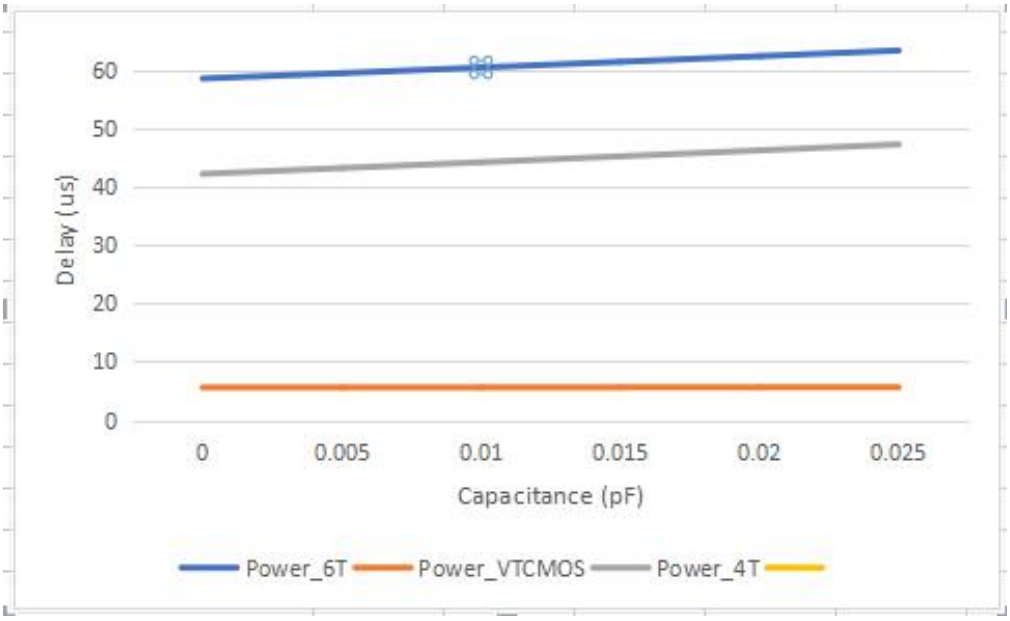


Figure 24: Power analysis with different capacitive loads

7.11.4 Hysteresis Analysis of Schmitt Trigger

The table 4 presented below shows analysis of hysteresis width of different transistor models of Schmitt trigger. It is clear that Body biased Schmitt trigger is giving best hysteresis width. Width of Schmitt trigger defines noise immunity of the circuit. More the width more is the noise immunity. Hence it is required that a Schmitt trigger must provide maximum hysteresis width. Out of the all implemented models, body biasing based CMOS Schmitt trigger at Vn approaching to Vdd and Vp approaching to ground level is giving maximum hysteresis width.

Table 4: Hysteresis Width Analysis for different configurations of Schmitt trigger

Model of Schmitt trigger	**Hysteresis Width**
6T based Schmitt trigger	660.345mV-1.219V
4T based Schmitt trigger	0.93V-1.23V
Body biased based S.T with Vn = Vp = 1.5V	701.537mV-1.22V
Body biased based S.T with Vn = Vp = 1.2V	660.028mV-1.21V
Body biased based S.T with Vn = 1V Vp = 0.5V	659.345mV-1.09V
Body biased based S.T with Vn = 1.2V Vp= 0.5V	658.81mV-1.217V
Body biased based S.T with Vn = 1.5V Vp= 0.5V	701.021mV - 1.009V

CHAPTER 8: CONCLUSION AND FUTURE WORK

This Dissertation-II report represents the work on different models of Schmitt trigger like 4T model, 6T Model (Conventional model), Variable Threshold based CMOS and Body biased Schmitt Trigger design. In this report I have compared propagation delay at the capacitance load of body biased CMOS Schmitt trigger at different values of Vn and Vp. Also delay of conventional Schmitt trigger, 4T model of Schmitt trigger is compared with the body biased Schmitt trigger at Vn=1.2V and Vp=0.5V. The main reason behind selecting this Vn and Vp is, Schmitt trigger is giving maximum hysteresis width at this particular value. As Hysteresis width should be as max as possible, so in this report we have considered this value of Vn and Vp. Also, the dynamic power is also analyzed for different models of Schmitt triggers. It is observed that VTCMOS is having minimum switching power dissipation but is having less hysteresis width. In the similar way 4T model has better hysteresis width but is having more delay where as Body biased CMOS Schmitt trigger is having less delay, better hysteresis width but is having more power consumption.

In the future I'll be working with digital circuits using hybrid design of Schmitt trigger, i.e. different Schmitt triggers will be used to implement logic gates using hybrid technique and then these logic gates will be used to implement digital circuit. I'll be also working with layout designing of these digital circuits and logic gates as well so that all parameters i.e. area, power and delay can be considered.

REFERENCES

[1] Joseph, J. S., Shukla, R., & Niranjan, V. (2015, September). Performance evaluation of low voltage Schmitt triggers using variable Threshold techniques. In *Reliability, Infocom Technologies and Optimization (ICRITO)(Trends and Future Directions), 2015 4th International Conference on* (pp. 1-5). IEEE.

[2] Kulkarni, J. P., & Roy, K. (2012). Ultralow-voltage process-variation-tolerant schmitt-trigger-based SRAM design. *IEEE transactions on very large scale integration (VLSI) systems*, *20*(2), 319-332.

[3] Lotze, N., & Manoli, Y. (2012). A 62 mV 0.13$\mu $ m CMOS Standard-Cell-Based Design Technique Using Schmitt-Trigger Logic. *IEEE journal of solid-state circuits*, *47*(1), 47-60.

[4] Saxena, A., & Akashe, S. (2013, April). Comparative analysis of Schmitt trigger with AVL (AVLG and AVLS) technique using nanoscale CMOS technology. In *Advanced Computing and Communication Technologies (ACCT), 2013 Third International Conference on* (pp. 301-306). IEEE.

[5] Filanovsky, I. M., & Baltes, H. (1994). CMOS Schmitt trigger design. *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, *41*(1), 46-49.

[6] Suresh, A. (2014, May). A low power Schmitt Trigger design using SBT technique in 180nm CMOS technology. In *Advanced Communication Control and Computing Technologies (ICACCCT), 2014 International Conference on*(pp. 533-536). IEEE.

[7] Kadu, A. W., & Kalbande, M. (2016, November). Design of low power Schmitt trigger logic gates using VTCMOS. In *Green Engineering and Technologies (IC-GET), 2016 Online International Conference on* (pp. 1-5). IEEE.

[8] Kumar, M., Kaur, P., & Thapar, S. (2012). Design of CMOS Schmitt trigger. *International Journal of Engineering and Innovative Technology (IJEIT) Volume*, *2*.

[9] Vasundara Patel, K. S., Bhushan, H. N., Gadag, K. G., Nischal Prasad, B. N., & Haroon, M. (2014). Schmitt Trigger Based SRAM Using Finfet Technology-Shorted Gate Mode. *World Academy of Science, Engineering and Technology International Journal of Computer, Electrical, Automation, Control and Information Engineering*, *8*(2).

[10] Chen, Z., & Chen, S. (2017, May). A high-speed low voltage CMOS Schmitt Trigger with adjustable hysteresis. In *Computer and Information Science (ICIS), 2017 IEEE/ACIS 16th International Conference on* (pp. 293-297). IEEE.

[11] Kim, K., & Kim, S. (2015). Design of Schmitt trigger logic gates using DTMOS for enhanced electromagnetic immunity of subthreshold circuits. *IEEE Transactions on Electromagnetic Compatibility*, *57*(5), 963-972.

[12] Sapawi, R., Chee, R. L. S., Sahari, S. K., & Julai, N. (2008, May). Performance of CMOS Schmitt trigger. In *Computer and Communication Engineering, 2008. ICCCE 2008. International Conference on* (pp. 1317-1320). IEEE.

[13] Lotze, N., & Manoli, Y. (2017). Ultra-Sub-Threshold Operation of Always-On Digital Circuits for IoT Applications by Use of Schmitt Trigger Gates. *IEEE Transactions on Circuits and Systems I: Regular Papers*, *64*(11), 2920-2933.

[14] Kulkarni, J. P., & Roy, K. (2012). Ultralow-voltage process-variation-tolerant schmitt-trigger-based SRAM design. *IEEE transactions on very large scale integration (VLSI) systems*, *20*(2), 319-332.

[15] Arjun, N., Marwah, A., & Akashe, S. (2015, November). The alleviation of low power Schmitt trigger using FinFET technology. In *Communication Networks (ICCN), 2015 International Conference on* (pp. 328-333). IEEE.

[16] Hang, G., & Zhu, G. (2015, November). A new Schmitt trigger with adjustable hysteresis using floating-gate MOS threshold inverter. In *ASIC (ASICON), 2015 IEEE 11th International Conference on* (pp. 1-4). IEEE.

[17] Nejati, A., Bastan, Y., & Amiri, P. (2017, May). 0.4 V ultra-low voltage differential CMOS Schmitt trigger. In *Electrical Engineering (ICEE), 2017 Iranian Conference on* (pp. 532-536). IEEE.

[18] Moghaddam, M., Moaiyeri, M. H., & Eshghi, M. (2017). Design and Evaluation of an Efficient Schmitt Trigger-Based Hardened Latch in CNTFET Technology. *IEEE Transactions on Device and Materials Reliability*, *17*(1), 267-277.

[19] Raza, G. A., & Mehra, R. (2015, September). Area and power efficient layout design of Schmitt trigger. In *Computer, Communication and Control (IC4), 2015 International Conference on* (pp. 1-4). IEEE.

[20] Sreenivasan, D., Purushothaman, D., Pande, K. S., & Murty, N. S. (2016, December). Dual-threshold single-ended Schmitt-Trigger based SRAM cell. In *Computational Intelligence and Computing Research (ICCIC), 2016 IEEE International Conference on* (pp. 1-4). IEEE.

[21] Ahmad, S., Gupta, M. K., Alam, N., & Hasan, M. (2016). Single-ended Schmitt-trigger-based robust low-power SRAM cell. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, *24*(8), 2634-2642.