DESIGN AND IMPLEMENTATION OF LOW POWER FULL ADDER USING SEMI-XNOR ON 180NM, 90NM AND 45NM TECHNOLOGY

DISSERTATION-1 REPORT

Submitted in partial fulfillment of the requirement for the Award of the Degree of

MASTER OF TECHNOLOGY

IN

(VLSI DESIGN)

By

Seelam. Rajasekhar Reddy (Reg.no:11613876)

Under the Guidance of

Dr. Ravishankar Mishra

Associate professor, L.P.U

School of Electronics and Communication Engineering

Lovely Professional University

Phagwara, Punjab-144411

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CERTIFICATE

This is to certify that Seelam Rajasekhar Reddy bearing Registration no.11613876 have completed objective formulation/Base Paper implementation of the thesis titled, **"DESIGN AND IMPLEMENTATION OF LOW POWER FULL ADDER USING SEMI-XNOR ON 180NM, 90NM AND 45NM TECHNOLOGY"** under my guidance and supervision. To the best of my knowledge, the present work is the result of his original investigation and study. No part of thesis has ever been submitted for any other degree at any university.

Dr. Ravi Shankar Mishra
Associate Professor
School of Electronics and Communication
Lovely Professional University
Phagwara, Punjab

Date:

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We are also indebted to all authors of the research papers and books referred to, which have helped us in carrying out the research work.

Seelam Rajasekhar Reddy
Reg.No:11613876

DECLARATION

I, Seelam.Rajasekhar Reddy, student of M. Tech under Department of Electronics and Communication of Lovely Professional University, Punjab, hereby declare that all the information furnished in this Dissertation-I report is based on my own intensive research and is genuine.

This report does not, to the best of our knowledge, contain part of my work which has been submitted for the award of my degree either of this University or any other University without proper citation.

Seelam. Rajasekhar Reddy
Reg.No.11613876

ABSTRACT

Power consumption, Area, Delay and Speed are major concern in integrated circuit. Due to advancement of technology density of chip became increased and lot of hardware present in the circuit. Which in turn more power consumption and delay and further it consuming more silicon area. Because of these limitations concern low power circuits playing vital role in today's technology. We are introducing new concept called semi-XNOR gate. XOR and XNOR gates are basic building blocks of full adder. We are using the same concept to design Full adder and working under the platform of Cadence virtuoso and we are going to evaluate parameters like power, delay and power delay product using technology of 180nm, 90nm, and 45nm.

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LIST OF ABBREVIATIONS

CMOS - Complementary Metal Oxide Semiconductors
VLSI - Very Large Scale Integration
FA - Full Adder
IC - Integrated Circuits
FPGA - Field Programmable Gate Arrays
ASIC - Application Specific Integrated Circuits
DSP - Digital Signal Processors
GIDL - Gate Induced Drain Leakage
SOC - System On Chip
CCDM - Column Compression Dada Multiplier
PDP - Power Delay Product
ALU - Arithmetic logic unit

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CHAPTER-1

INTRODUCTION

In recent years we have seen that the density of integrated chip increased drastically. Most of the designs are highly integrated and circuits inside a chip becomes more and more complex which in turn many issues such as cross talks, coupling effects, distortions, and heating effects other than these we have other related issues like setup time, hold time violations, skew and jitter and many more issues. These issues are mainly because of complexity of the systems. Why low power devices playing vital role in today's technology? ever increasing and exponential growth of portable devices like laptops, mobile phones and portable devices, researchers has been started exploring innovations on low power devices in fact a certain concepts already available. There are some reasons which tells you how much these low power devices are effective in your design. Low power circuits not only reducing area but also it reduces power consumption of a circuit. The power consumption mainly due to frequent switching of clock, in such scenario we can incorporate a new method called clock gating to mitigate frequent switching of clock. For instance consider a laptop in which having lot of features, as features are increasing battery backup decreasing. perhaps every one of us need battery backup for long time so that we can use it for long time without power requirement however the complexity of your system design not going to sustain battery backup for long time.

As we know that when the technology is upgrading from 180nm to 45nm or any other technology mainly power area and performance are important factors. As a result of technology up grading transistor dimensions may vary like length and width. So the transistor scaling down as result to leakage power in earlier days leakage power is ignored.

As technology improving from one technology to another the main issue is of power consumption. Power consumption is mainly categorized into three types they are

$P_{total} = P_{dynamic} + P_{dp} + P_{static}$

Dynamic power consumption - Each transistor in a chip dissipate small amount of power when it switched from high to low or low to high. If transistors switches more rapidly leads to more power. Dynamic power dissipation mainly depends on clock speed. If clock speed is higher, more frequent switching of transistor. Hence transistor switching is more which result to more dynamic power dissipation.

$P_T = C_{PD} . V^2_{CC} . f$

P_T - circuit's internal power dissipation.

C_{PD} - power dissipation capacitance

V_{CC} - power supply voltage

f - transition frequency.

Total dynamic power dissipation of a cmos circuit is

$P_D = (C_{PD +} C_{L)} . V^2_{CC} . f.$

C_L - capacitive load.

Short circuit power consumption - It is occurred when Both pull up transistor and pull down transistor on simultaneously as a result of direct path exist from vdd to gnd with small interval of time.

Static power consumption - due to sub-threshold leakage and reverse biased PN junction.

Static power consumption of a circuit given as

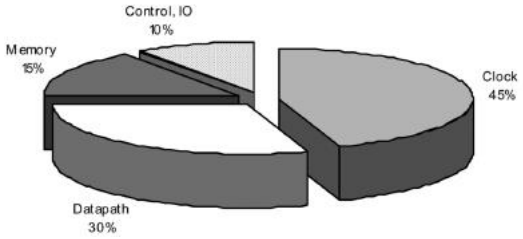
$P_{static} = I_{leakage} V_{DD.}$

$I_{Leakage}$ has five components

- .Reverse biased PN junction current.
- Sub-threshold leakage
- Gate induced drain leakage(GIDL)
- Punch through
- Gate tunneling.

These three constraints are mainly relying on complexity of your design, which leads to heating problems. To control heat dissipation of your system need to incorporate cooling systems into your system.as we deploying of extra devices incurred additional area and additional cost. As much as you reduce the complexity of your design, you can reduce area as well as cost.

For instance you considered as a microprocessor, in which we just considered as a power. We are breaking down the power for multiple purpose such as for clock, data paths, memory and control IO paths. Out of which clock consuming 45% of the total power, data path of 35% , memory of 15% and control IO paths consuming 10% of the total power. Adders are used to design data paths. I have already mention above that the data paths in microprocessors consume 35% of the total power. If you reduce power consumption of full adder you can reduce power consumption in microprocessor.



Fig[1.1]: power breakdown in high-performance microprocessors

Delay also one of the important factor in digital circuits. Delay is caused due to interconnecting wires And also due to primitive cells such as AND, OR, XOR, NOT gates. Delay can be defined as the amount of time that the input is propagating to output. If the propagating time of input takes long time to reach output, the circuit has critical paths (wire which has longest computation time). Supply power also one of the important consideration to cause of delay. If supply power is more then delay will be less vice-versa.

Perhaps in your design more number of interconnects and more number of cells, result to more delay generating at the output side. To compute your design with lesser delay circuit must having lower number of interconnection and cells.

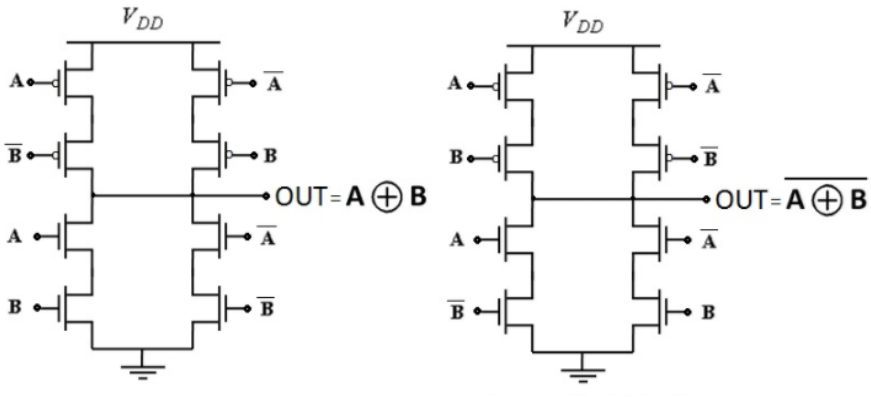
The main motive of designing of adder is to reduce delay as well as power. If we reduce the usage of cell primitives in adder designing than automatically delay can be reduced.

In very large scale integration (VLSI) Binary addition is basic building block for many arithmetic operations like addition, subtraction, multiplications. In addition to this adder also applicable for application specific integrated circuits(ASIC), microprocessors and digital signal processors(DSP) under which Other related applications like data compressors, data converters, parity checker, error-detection or error-correction codes, phase detector in PLL circuits, data paths circuits etc.

1.1 Conventional XOR-XNOR gates:

XOR or XNOR are basic building blocks for full adder design shown in figure 1 and figure 2. To develop XOR gate has 12 transistors are required and 14 transistors for XNOR .Since it has more transistors count which result to consuming more area and power .If the XOR or XNOR gate of transistors are decreased! Automatically requirement of transistor for designing full adder also diminished that is the reason why most of the designers have been concentrate on designing of XOR or XNOR gate with different approaches.

XOR-XNOR gates mostly used in various circuits mostly in arithmetic circuits, parity checker, comparators, compressors, error-detecting and error-correcting codes, phase detector and code converters



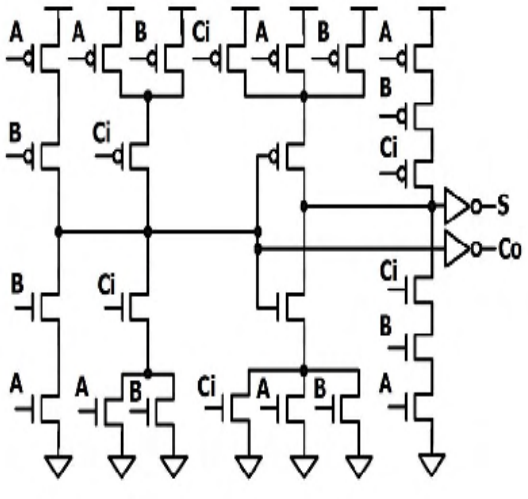
Fig[1.2] : Standard XOR and XNOR gates

A	B	XOR	XNOR
0	0	0	1
0	1	1	0
1	0	1	0
1	1	0	1

Table[1.1]: truth table of XOR-XNOR gates

1.2 conventional Full adder:

Figure demonstrate that it is a standard full adder. It has implanted with the help of 14 pull up transistors (PMOS) and 14 pull down transistors (NMOS). Full adder adds binary numbers and it adds three one bit numbers, it often written as A, B, Cin. Output of full adder consists of sum and carry. It change their state as per the input given. Irrespective of area of full adder it provides better performance in terms of speed, high noise immunity and better driving capability however it consume more power and area these are main drawbacks of standard full adder. There are many logics which were used to implement full adder such as double-pass transistor logic, swing restored pass transistor logic, complimentary pass transistor logic, transmission gate logic etc.



Fig[1.3] : conventional CMOS full adder

Many advanced designs have been derived from full adder such as ripple carry adder, carry-look a head adder, carry save adder, carry skip adder and multiplier.

A	B	C	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table[1.2] : full adder truth table

SUM= A’B’C+A’BC’+ABC’+ABC

CARRY=BC+AB+AC

CHAPTER-2

SYSTEM DISCRIPTION

Earlier designs of XNOR gates are, 6T XNOR gate using pass transistor logic with less power dissipation reported. 8T XNOR gate with high output swing voltage and high driving capability is reported. Another 8T XNOR gate with low power consumption were reported. Pass transistor based 3T XNOR is reported with less power consumption with limited driving capability reported. XNOR gate design with FINFET technology with low power consumption is reported. Novel 4T XNOR gate with less delay and less power consumption were reported. 2T XNOR design using Pass transistor logic with less area is repored.

Proposed design has been implemented with the help of two XNOR gates with one multiplexer. XNOR gate is designed with three transistors one PMOS transistor and two of NMOS transistors.
As they were mension that for designing 3T XNOR, the gate length of all three transistor is o.35um and width of N1 ad N2 transistors would be taken as 5.0um and 1.0um and width of P1 transistor would be taken as 2.0um.
When A=B=0 output is logic high because transistor P1 is high and N1 and N2 transistors are off. P1 transistor providing low resistance path from vdd to output. For A=0 and B=1 output is logic low because transistor P1 and N1 transistor are in off condition and N2 transistor is of on condition. N2 transistor would provide a low resistance path from output to gnd.For A=1 and B=0 P1 and N1 both transistors are of on condition, output provide logic low because it provides low resistance path from output to gnd. For A=1 and B=1 output provides logic high because width of N1 is made larger which is equal to 5um and it provides low resistance, as a result signal B is reached output with less delay

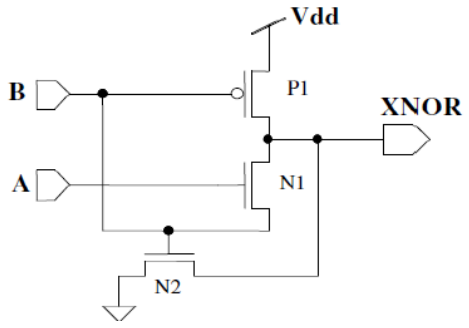


Fig [2.1] :proposed 3T XNOR gate

As Width of N1 transistor has been increased threshold voltage of NI will become decreased

$$V_{TN} = V_{TO} + \gamma(\sqrt{|V_{SB} + 2\phi_F|} - \sqrt{|2\phi_F|})$$

V_{TN} – threshold voltage when body bias is present

V_{SB} – substrate to body bias voltage

ϕ_F - surface potential

V_{TO} – threshold voltage for zero substrate bias

Proposed full adder design has been implemented with the help of two XNOR gates and one multiplexer. XNOR design with three transistors and their respective width and length also already mension. For multiplexer designing we have taken as transmission gate logic because it provide output with less delay. For gate lenth for PMOS and NMOS transistors would be taken as 0.35um and width is of 1.0um and 2um respectively .As we compared it with earlier designs transistor count drastically decreased which result to minimum power consumption and minimum delay and high performance.

SUM is being driven by the two XNOR gates and Carry is driven by the multiplexer shown in fig

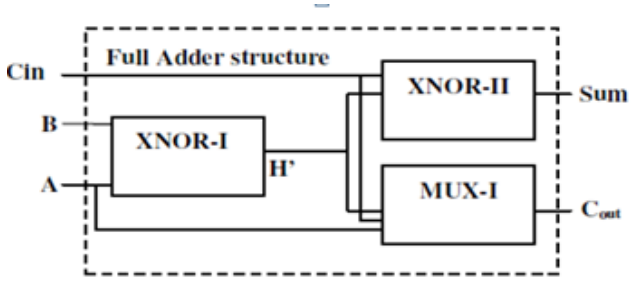
SUM = (A XOR B) XOR Cin

Cout = A.B + Cin (A XOR B)

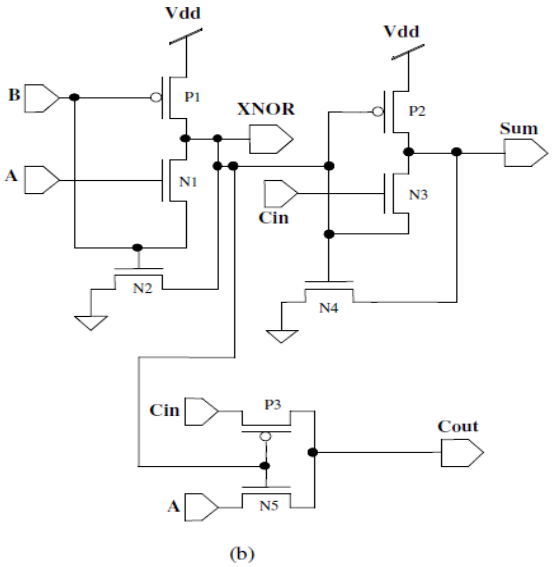
Structured implementation of full adder as shown in figure

SUM = H XOR Cin = H. Cin'+ H' Cin

Cout= A. H'+ Cin. H



Fig[2.2] : Structure of single bit full adder



Fig[2.3]: Full adder using two 3T XNOR gates and multiplexer circuit diagram

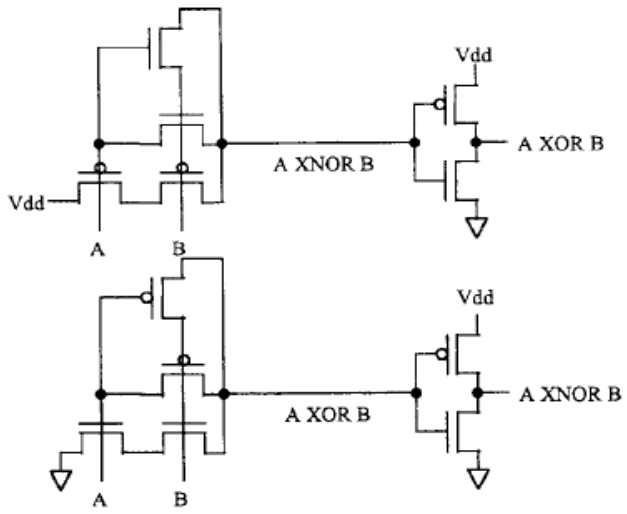
CHAPTER-3

Literature review:

This paper contains the review of literature about XOR-XNOR gates and full adder circuits. I have studied journals and conference papers, articles related to my topic and few of these those papers are listed below. In this literature review I have mentioned some of reference papers and platform of implementation and technology of investing parameters. further I have discussed about advantage and disadvantages (if there is any) and applications of each reference papers .

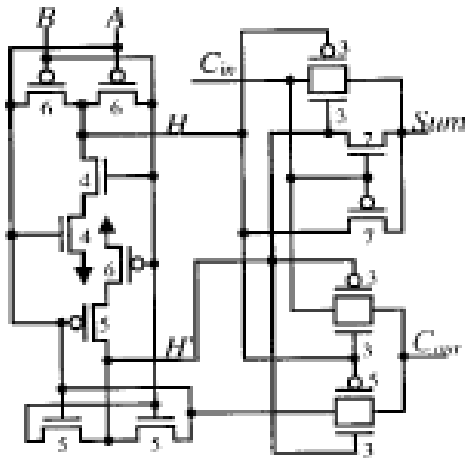
Veena Tiwari[1]: This paper proposed 3T XNOR based full adder. XNOR gate has power dissipation of 550.7272uw and 581.542uw for proposed full adder. This adder has been implemented in TPICE tool. Parameters has been evaluated and Investigated on 0.12um technology. Supply voltage has taken from the range of 1.5V to 3.3V. Compared to earlier designs proposed adder has better in terms of power and delay and also it consuming less silicon area.

Jyh-Ming Wang[3]: Two new techniques are proposed to execute the exclusive- OR and exclusive- NOR works on the transistor level. The primary strategy utilizes non-complementary signal inputs and minimal number of transistors. The other one enhances the execution of the earlier strategy however two more transistors are used. later utilized the same number of transistors to enhance the driving capability . Two GATES have been completely Simulated by HSPICE on a SUN SPARC 2 workstation.



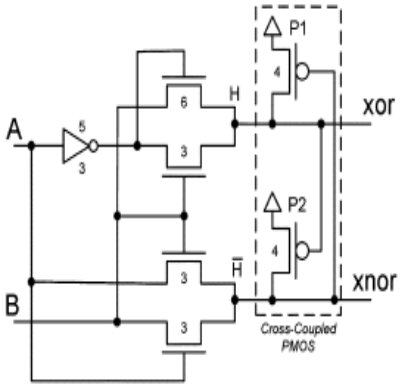
FIG[3.1]: Novel XOR – XNOR gates

Ahmed M. Shams[4]: An execution investigation of 1-bit full-adder cell is introduced. The adder cell is dissected into littler modules. The modules are contemplated and assessed extensively. A few plans of each of them are produced, prototyped, simulated and investigated. Twenty distinctive 1-bit full-adder cells are developed (the majority of them are novel circuits) by associating blends of distinctive outlines of these modules. Each of these cells shows diverse power utilization, speed, region, and driving capacity figures. Two sensible circuit structures that incorporate adder cells are utilized for simulation. A library of full-adder cells is created what's more, exhibited to the circuit architects to pick the full-adder cell that fulfills their particular applications.

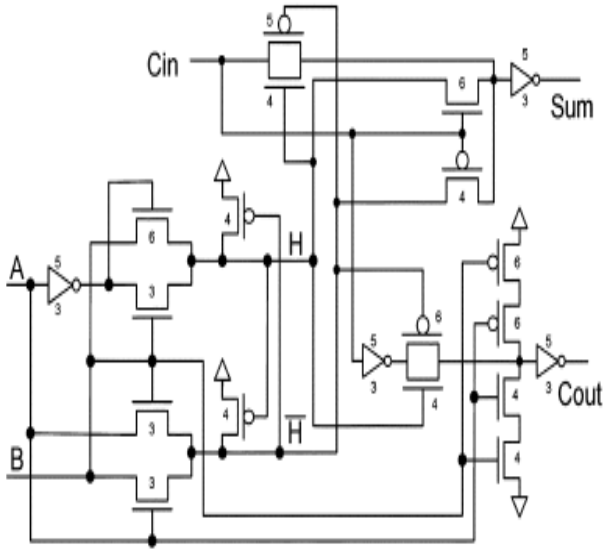


Fig[3.2]: 16T full adder

Sumeer Goel[5]: In this paper presented a new design for 1-bit full adder featuring hybrid-CMOS design style. To achieve a good-drivability, noise – robustness, and low-energy operations for deep sub micro meter guided this research to explore hybrid CMOS style design. This paper incorporated CMOS logic styles to build adder to achieve desired performance . This adder provides the designer to target a wide range of applications. The proposed XOR-XNOR gate will provide full swing outputs simultaneously. This adder has good driving capabilities and it reduces buffer usage between cascaded stages. This paper claimed that previously reported adders has suffered from the problem of low swing and high noise problem when operated with low supply voltage. This proposed full adder successfully operated at low supply voltage with excellent signal integrity and driving capability. There is 40% reduction in power delay product when it compared to its best counter part.



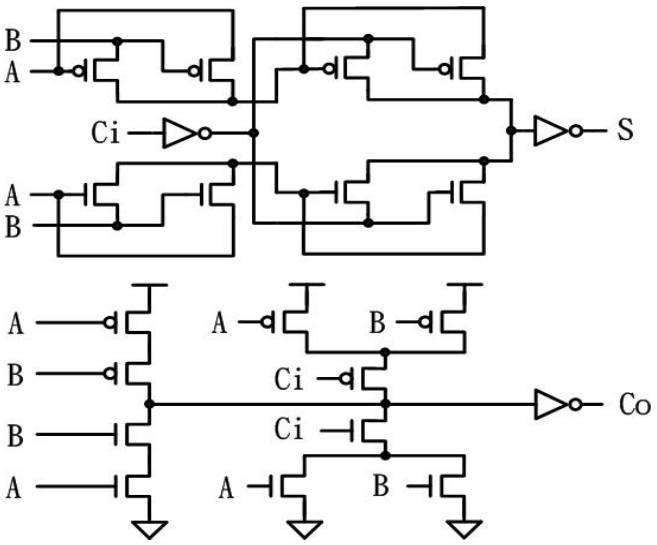
Fig[3.3] : 8T XOR- XNOR gates



Fig[3.4] : 24 T hybrid CMOS full adder

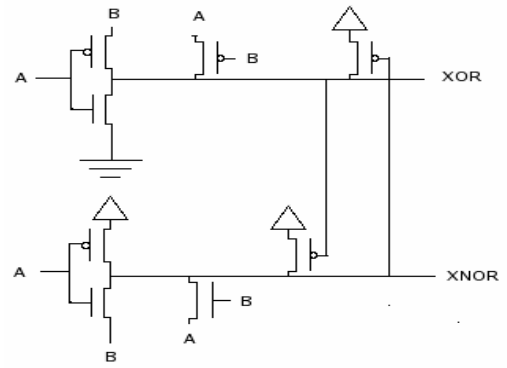
Chiou-Kou Tung[6]: In this paper, a low-control high speed CMOS full adder is proposed for embedded framework. In light of another three-input exclusive OR (3-XOR) outline, the new hybrid full adder is made out of pass-transistor logic and static CMOS logic. The primary design targets for the full adder are giving low power and rapid as well as with driving ability. Utilizing TSMC CMOS 0.35-µm innovation, the attributes of the trial circuit contrasted and earlier writing demonstrate that the new adder enhances 1.8% to 35.6% in control power utilization, 11.7% to 41.2% in time delay of Co, and 13.7% to 91.4% in power delay product of Co. The circuit is demonstrated to have the base power utilization and the speediest reaction of complete flag among

the adders chose for examination. Because of the low-power and fast properties, both the new select OR circuit and the new full adder can be coordinated in a framework on-a-chip (SoC) or an implanted framework.



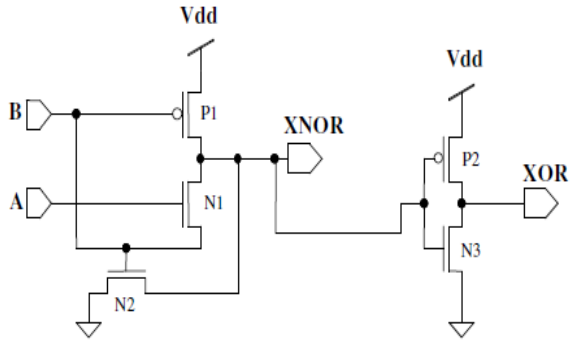
Fig[3.5] : 24T hybrid full adder

Shiv Shankar Mishra[7]: A new XOR – XNOR gates has been proposed. This circuits are proposed to improve the performance in terms of speed and power. Proposed models modeled using TSMC 0.18um. XOR- XNOR circuits evaluated at different supply voltage ranges starting from 0.6v to 3.3v.These evaluated results have been simulated from HSPICE. By investigating obtained results, proposed XOR- XNOR gate is better compared to available gates. It provides better outcomes for power and delay and also efficient in power delay product. This XOR – XNOR circuits basic building for arithmetic circuits, comparator, compressor, code converters, parity checker, phase detectors and error- detecting and error correcting codes.

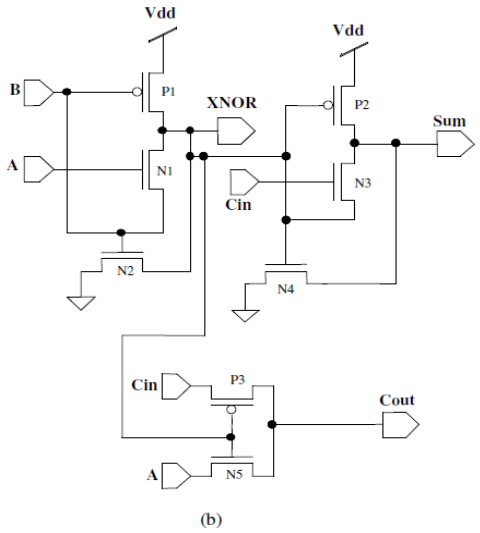


Fig[3.6] : 8T Novel XOR – XNOR gates

Manoj Kumar[8]: This paper has been reported that new XNOR gate using three transistor has been presented. Results shows Power dissipation of full adder is 581.542uw in 0.35um technology with supply voltage of 3.3v. Maximum level for low output of 0.32v and minimum level for high output 3.2v have been obtained when it compared with previous results. Previous results were maximum level for low output of 0.084v and minimum level for high output of 2.05v with supply voltage of 3.3v. Simulation results have been performed by using 'SPICE' based on TSMC 0.35um CMOS technology. The proposed full adder has better improvement in terms of power consumption and area. short circuit currents also eliminated because there is no direct path from vdd to gnd.

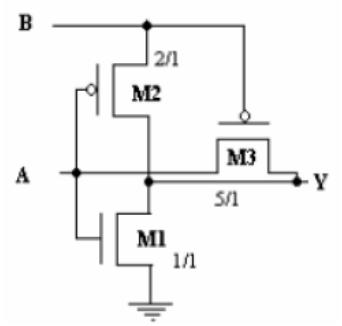


Fig[3.7]: XOR – XNOR gates

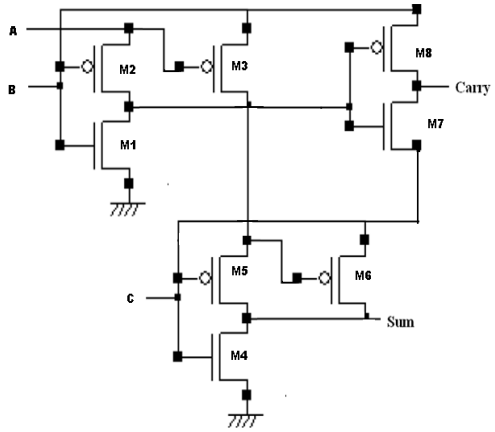


Fig[3.8] : 8T full adder using 3T XNOR circuits and Multiplexer

Deepak Garg[9]: This paper employed a novel full adder using two XOR gates along with one 2 to 1 multiplexer. An eight transistor full adder has been investigated using 0.18um cmos technology and simulations results are performed by TANNAR tool. Proposed adder has compared with 10, 12, 16, 28 transistors adder, computed results tells that it better than the other adders and it is has been providing significant improvement in area, power and delay. This adder has consumed average power of 1.129uw and delay of 12.512 ps and power delay product of 14.123j.



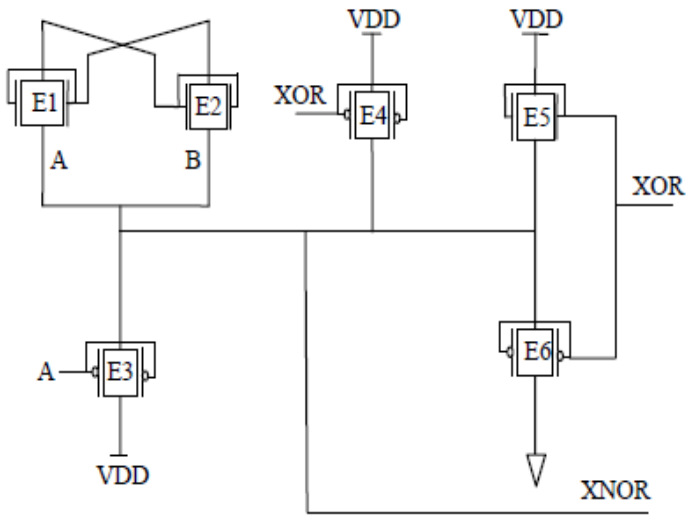
Fig[3.9] : 3T XOR gate using pass transistor logic



Fig[3.10] : 8T full adder using pass transistor logic.

Neha Yadav[10]: To limit the short channel impact Double-gate FinFET can be utilized as a part of place of regular MOSFET circuits because of the self-arrangement of the two entryways. Outline for XOR and XNOR circuits is recommended to enhance the speed and power. These circuits go about as essential building blocks for some, math circuits. This paper differentiates and assesses the

execution of conventional CMOS and FinFET based XOR-XNOR circuit outline. It depends on the investigation of fast, low power, and little territory in XOR-XNOR computerized circuits. The proposed FinFET based XOR and XNOR circuits have been composed utilizing Cadence VIRTUOSO Tool applying voltage supply of 0.2 to 1.2 voltages, with temperature at 270C and all the recreation comes about have been produced by Cadence spectre simulator test system at 45nm technology. Simulations comes about low power, delay, power delay product (PDP), and normal dynamic power utilization.

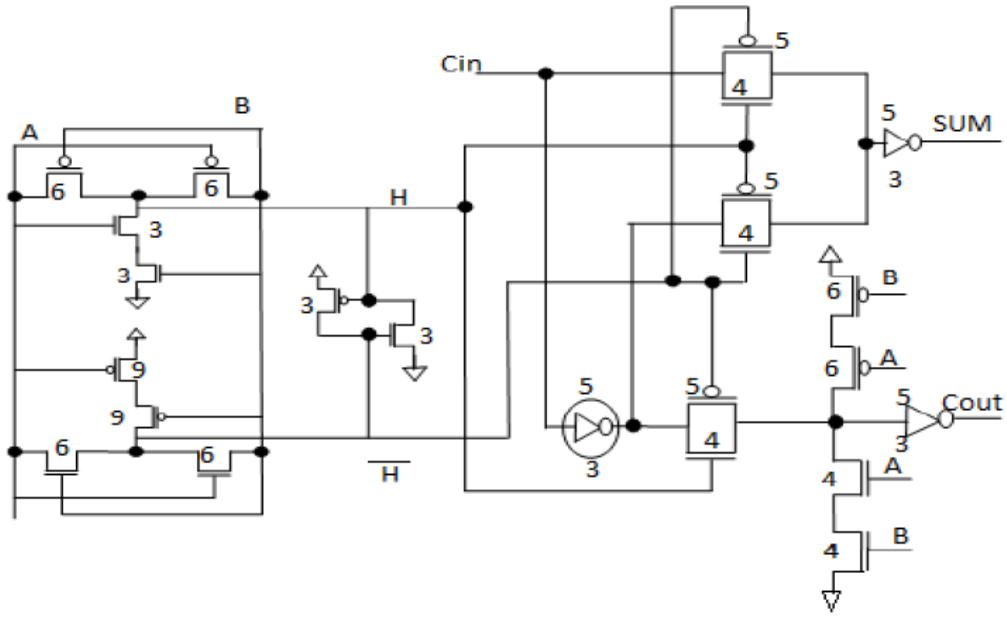


Fig[3.11]: XOR – XNOR gate design using FINFET technology

R.P.Meenaakshi Sundari[11]: This paper has been implemented full adder using pass transistor logic. Main motive to introduce this pass transistor logic is, it consume very less power because there is no power supply element in the circuit. Pass transistor logic based low power full adder has been designed and results carried out in 'TANNER EDA' tool. Proposed full adder is very efficient in terms of speed, area and power consumption. It has been implemented with 17 transistors.

Jehangir Rashid Dar[12]: This paper employed a new novel low power energy efficient full adder. Full adder has been developed using one of the cmos logic i.e pass transistor logic. The main advantage of incorporating transmission logic over pass transistor logic is provides better output signal swing in addition to that better driving capability. Proposed design has better improvement in delay and power delay product. Simulation has carried out in TANNER tool using PTM 65nm

technology files. Simulations carried out for different supply voltage and loading condition to tackle performance of the design.



Fig[3.12]: 26 T full adder

V. Anandi[13]: In this paper employed a novel design of full adder cell based on sense energy recovery concept using novel XNOR gates is presented. This circuit design is optimized for low power at 180nm and 90nm process technology. When we compare proposed new XNOR gate provide better outcomes compared to the existing work based on speed, power consumption and power delay product (PDP). Proposed full adder has implemented and simulated in cadence tool. proposed full adder can work more reliably at different range of supply voltage over a frequency ranges. Simulations were conducted at supply voltage ranging from 0.7v to 1.5v for different frequencies i.e 5MHz, 50MHz, 100MHz, and 200MHz. The simulations results tells that the proposed adder has 37.3% power saving capability over a conventional 28-T cmos adder . The proposed adder has been used as the basic building for column compression dada multiplier (CCDM).

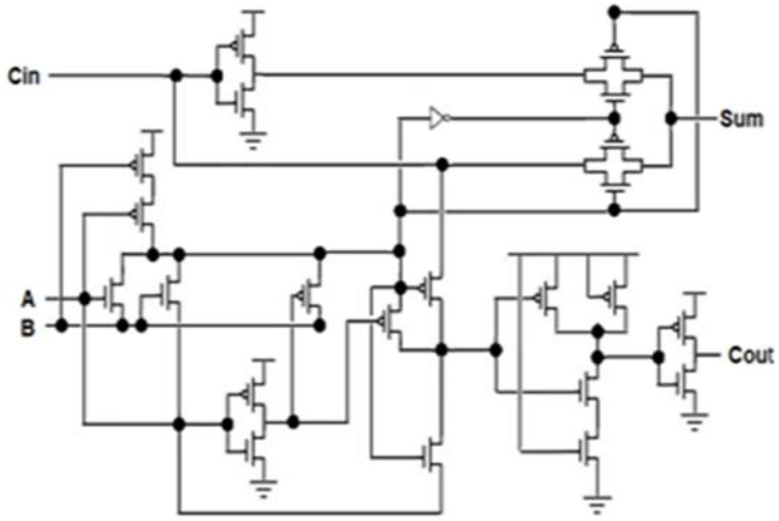
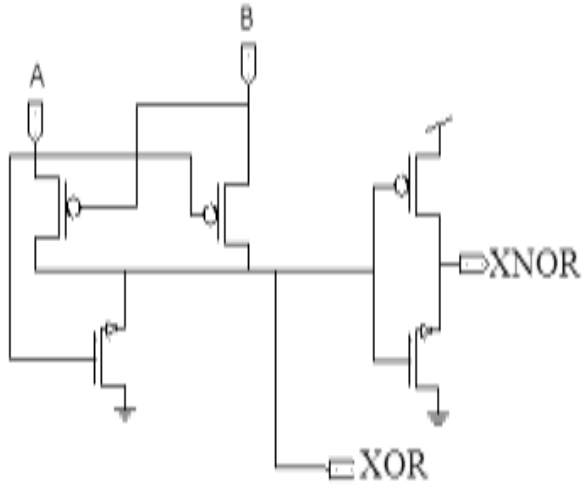
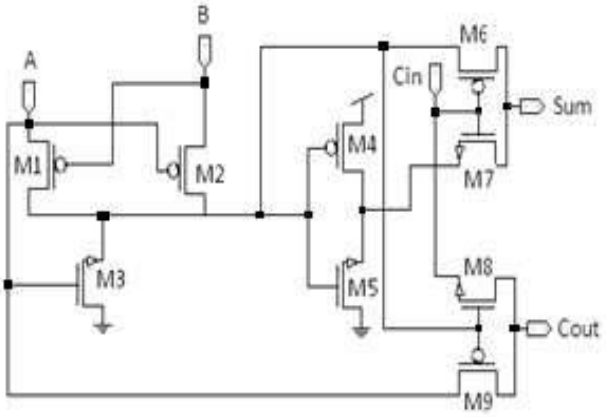


Fig [3.13]: 28T full adder

Sandeep Gotam[14]: In this paper novel design of full adder has been reported and it has been implemented with 5 transistor XOR - XNOR gates along with two MUX circuits however these 5T XOR – XNOR gate provide bad output results to certain input combinations. This full adder implementation and simulations done in HSPICE tool at voltage 5V using 180nm CMOS technology. Irrespective of results it provide better results in terms of power consumption, delay and power delay product(power delay product = power consumption x delay)

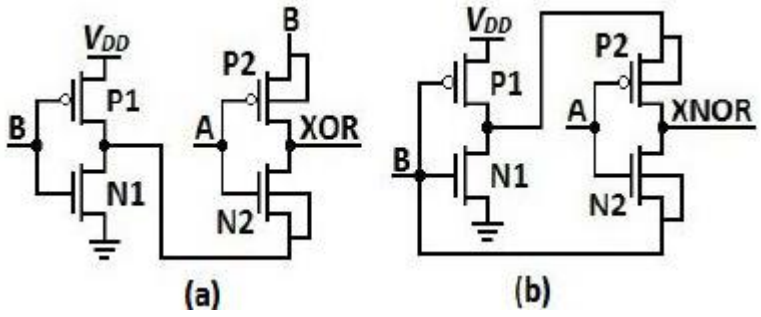


Fig[3.14]: XOR-XNOR circuit



Fig[3.15] : 9T full adder using XOR-XNOR gate and 2 multiplexer.

Neeraj Kumar Singh[15]: This paper advances a strategy for planning 1 bit full adder utilizing a recently proposed 4T XOR gate. The 4T XOR gate is framed of 2 PMOS and 2 NMOS transistors. The total is framed utilizing 2 XOR gate and the sum is framed utilizing a 2T mux. The subsequent 1 bit full adder is comprised of 10 transistors. The simulations is done utilizing Cadence Virtuoso Simulator utilizing 180nm technology and 1.8V power supply.



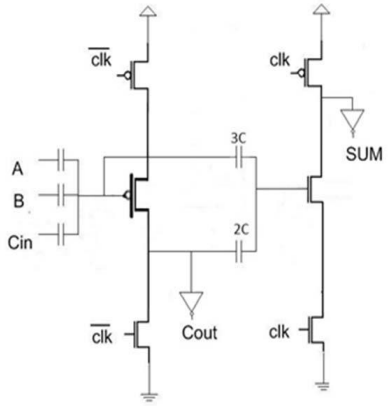
FIG[3.16]: Novel XOR and XNOR gates.

R.N.Nivethitha[16]: The paper proposed the novel plan of a 3T EX-NOR gate using corresponding CMOS and multiplexer. This paper displays as low power productive full adder with eight transistors(8T).All the DSP processors comprises of adder circuits. The power utilization in a full adder circuit is significantly because of EX-NOR gates. Adders have turned out to be one of the vital segments in the advanced world such that there is no outline without it. Adders are utilized for increases, as well as utilized as a part of numerous different capacities like Subtractions,

Multipliers, and Dividers and so on. In the field of Very Large Scale Integration (VLSI), Adders are utilized as the fundamental module from processors to ASIC's. Consequently an all around enhanced Adder configuration is required. A single bit full adder utilizing eight transistors has been planned utilizing proposed XNOR cell, which demonstrates power dissipation of 581.542μW. Simulations have been performed by utilizing MICROWIND apparatus.

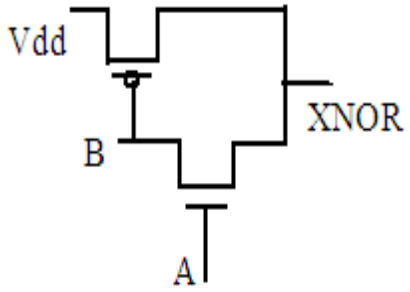
Bhavani Prasad[17]: This papers shows the acknowledgment of full adder outlines utilizing Complimentary CMOS Design, Complimentary Pass Transistor Logic Design and XOR-XNOR Design in a single unit. The primary intention of this paper is to decide the near investigation of energy, delay, power delay product (PDP) of various Full adder designs utilizing CMOS Logic Styles. Simulations results clearly verifies that XOR-XNOR type Full adder Design is better contrasted with Complimentary CMOS style and Pass Transistor Design concerning power, delay .Power Delay Product Comparison. The XOR-XNOR usage gives better execution and requires less number of transistors contrasted with other full adder outlines. The execution of design utilizing GPDK180nm with supply voltage of 1.8V in Cadence Virtuoso Schematic Composer and simulations done by utilizing specter Environment.

Vahid Foroutan[18]: In this paper a novel effective, high-speed and ultra-low power 1-bit full adder cell is exhibited. The execution: power, time delay and power delay product (PDP) of the proposed adder cell has been investigated in correlation with the four existent low-power, fast adders. The circuits being examined are optimized at 0.18-μm CMOS process technology and simulations are performed using cadence environment.

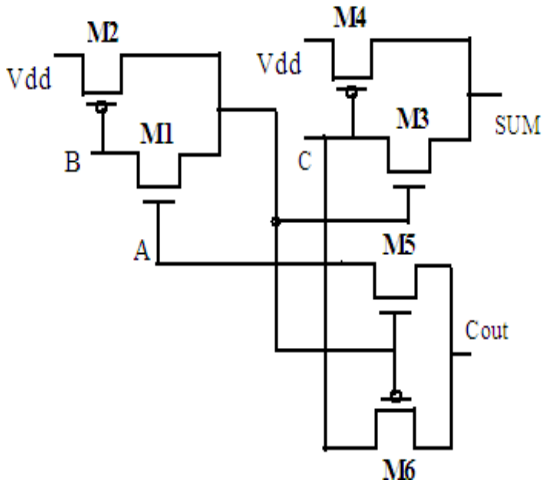


Fig[3.17] : 10T full adder

Krishna Chandra[19]: This paper proposed a novel design of 2T XNOR gate using pass transistor logic. Proposed adder has designed with 6 transistors and implemented it with 2XNOR gates and a mux circuit. The prior advantage of this circuit is it consume very less power and also it consume very less area when it compared with previous design. Obtained results investigated from TSPICE and using 0.18um technology.



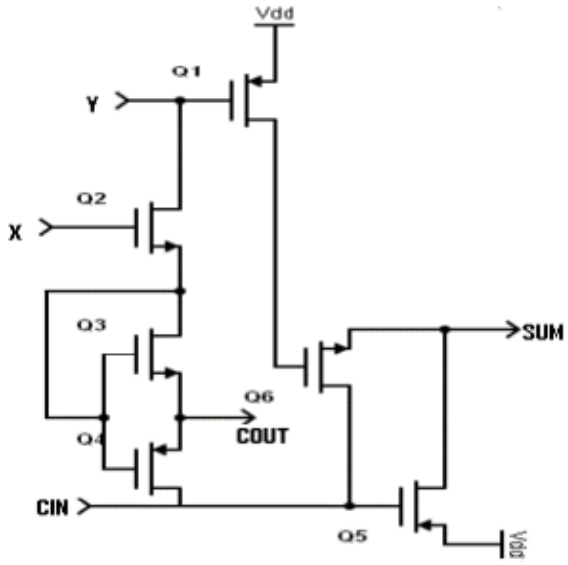
Fig[3.18] : 2T XNOR gate



Fig[3.19] : 6T full adder

Sugandha Chauhan[20]: This paper presents 1-bit CMOS full adder cell utilizing standard static CMOS logic style. The examination is taken out utilizing a few parameters like number of transistors, delay, speed, power consumption and power delay product (PDP). The circuits are planned at transistor level utilizing 180 nm and 90nm CMOS innovation. Different full adders are displayed in this paper like Conventional CMOS (C-CMOS), Complementary pass transistor rationale FA (CPL), Double pass transistor rationale FA , Transmission gate logic FA (TGA), Transmission work FA, New 14T,10T, Hybrid CMOS, HPSC, 24T, LPFA (CPL), LPHS, Hybrid Full Adders.

S. Selvi[21]: A fast development is been seen in the region of Integrated Circuits (IC) innovation. Every one of the ICs are to be planned in an upgraded way with the goal that they meet every one of the necessities of being quicker, possessing less region and diminished power utilization. One of the circuits which possess the vast majority of ICs is ALU which is a blend of arithmetic and logic units. Of the arithmetic units two are most critical which are the adders and multipliers. This paper portrays a productive technique to configuration full adders which is the essential unit of adders in ALUs.



Fig[3.20]: 6T full adder

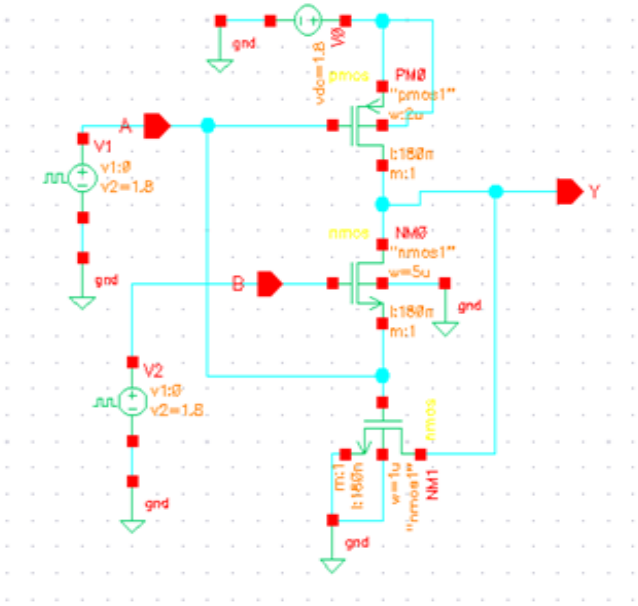
Sanjeev Kumar[15]: This paper shows another plan of 2T XNOR circuit. A six transistor full adder has been planned utilizing the proposed 2T XNOR circuit. The circuit indicates control utilization variety in the scope of 125.1241μW to 421.7256 μW. Most extreme yield postponement of the circuit indicates variety in the scope of 4.2528 ns to 3.1605 ns. Moreover, control defer item (PDP) of circuit is changing from 532.1277 (fJ) to 1332.8637 (fJ) with adjustment in supply voltage from 1.8V to 3.3V. The composed 6T full adder has been contrasted and before revealed full adder circuits what's more, an extensive change in control utilization, PDP and range has been gotten. The simulation has been conveyed utilizing SPICE in TSMC 0.18μm CMOS innovation.

Anurag Kothari[16]: In this paper a new novel full adder has been proposed. This proposed full adder has been implemented and analysed using DSCH and micro wind tool. Designed full adder

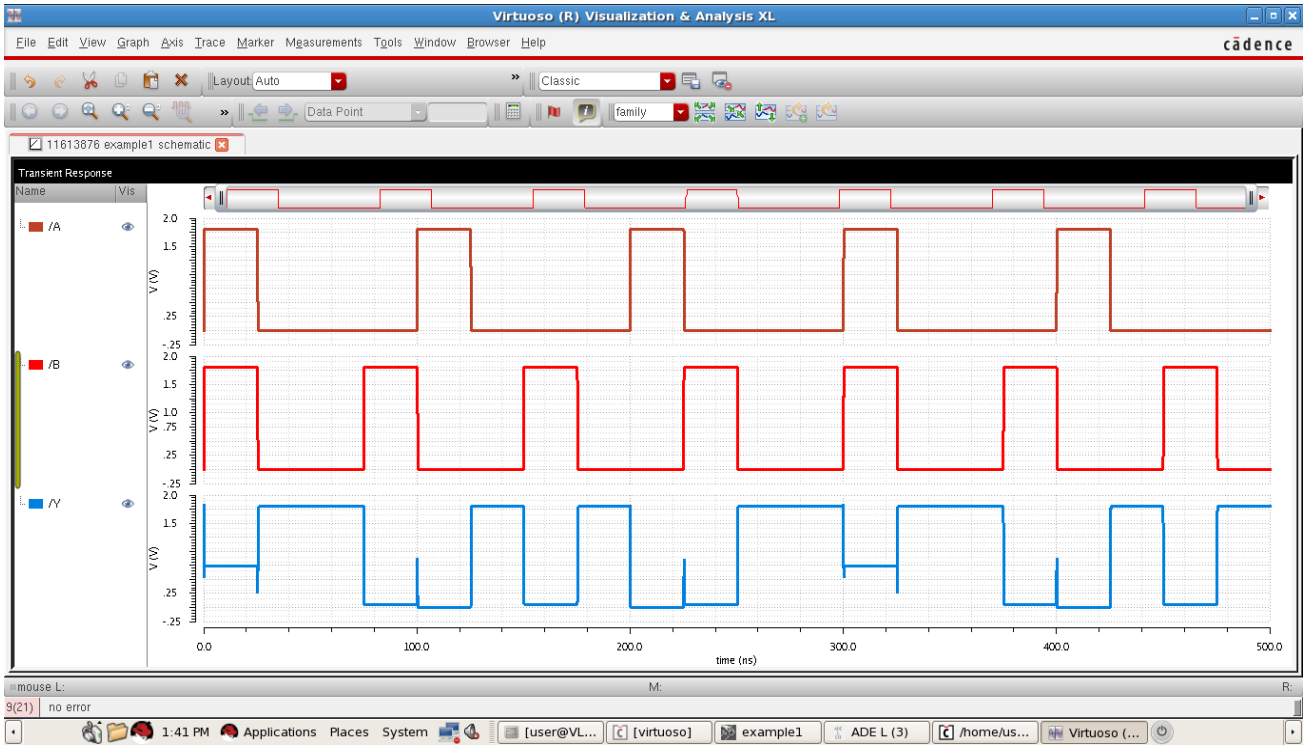
has been developed using cmos logic styles. Pass transistor logic used to compute sum function and static CMOS logic to compute carry function. Further, 9 transistor has been taken to implement adder. Simulation results clearly demonstrated that proposed adder having better improvement in speed and delay.

CHAPTER-4

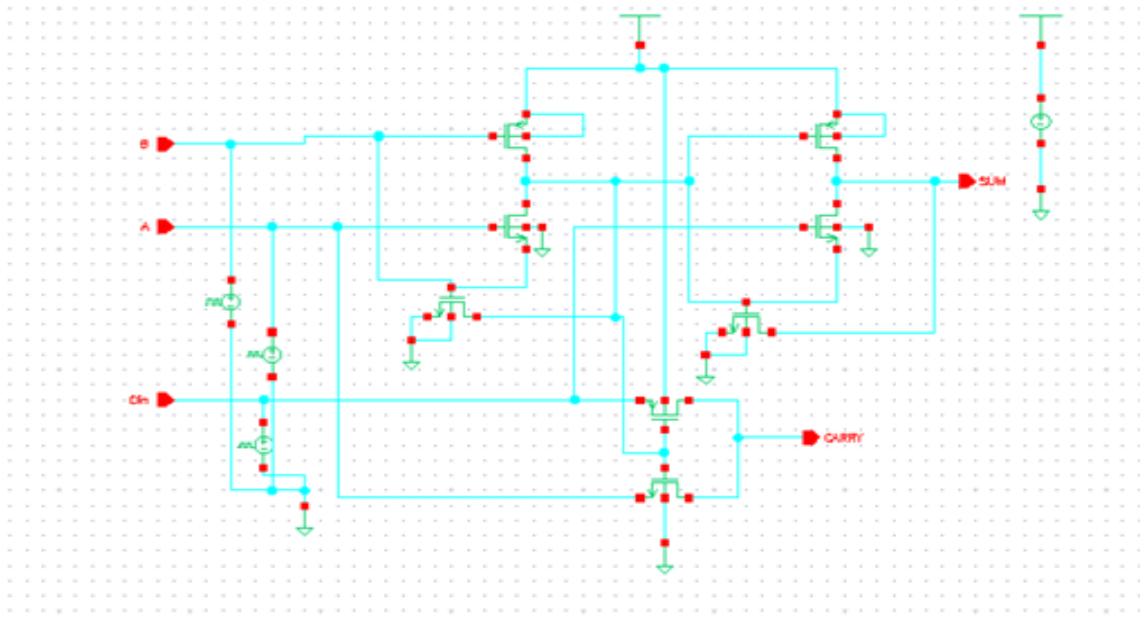
RESULTS



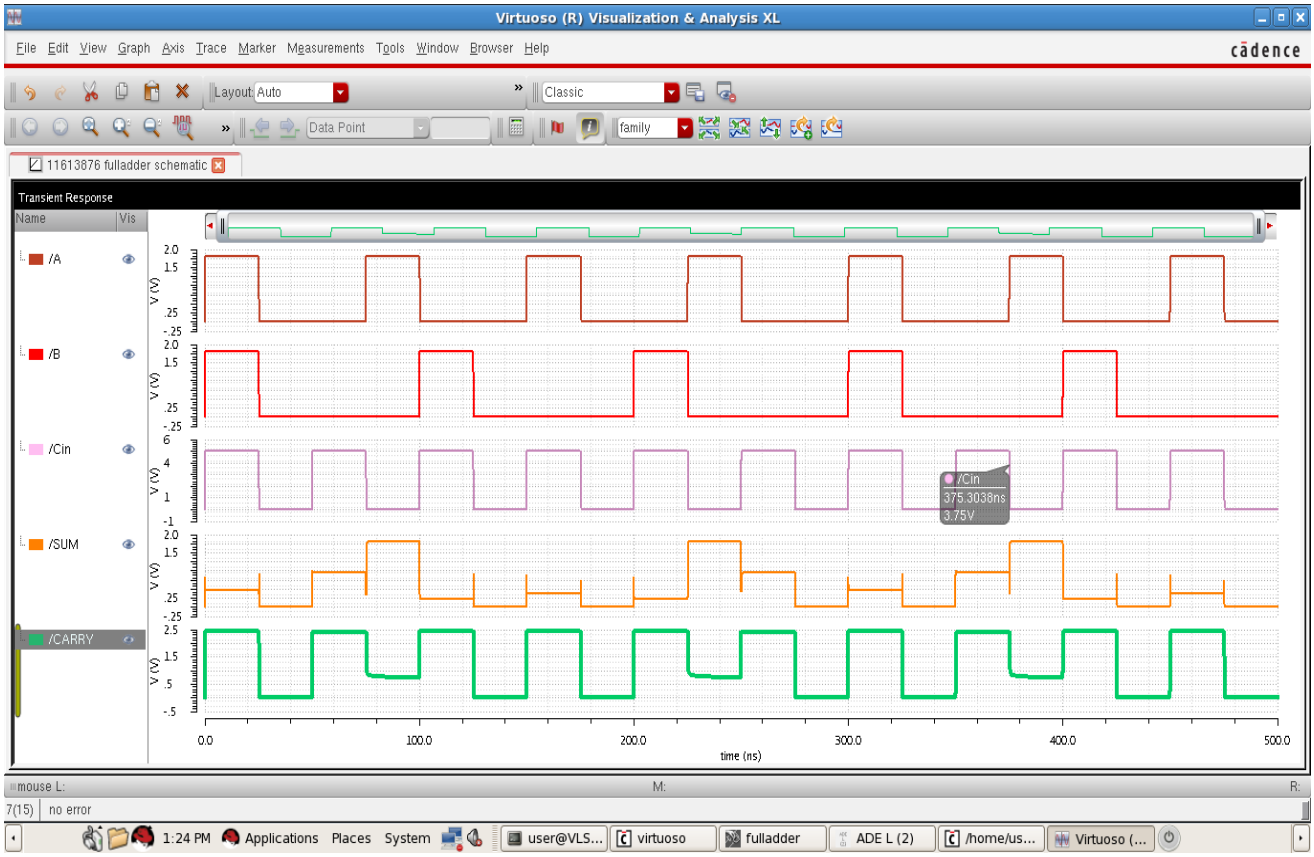
Fig[4.1] : Proposed XNOR gate



Fig[4.2] : waveforms of XNOR gate

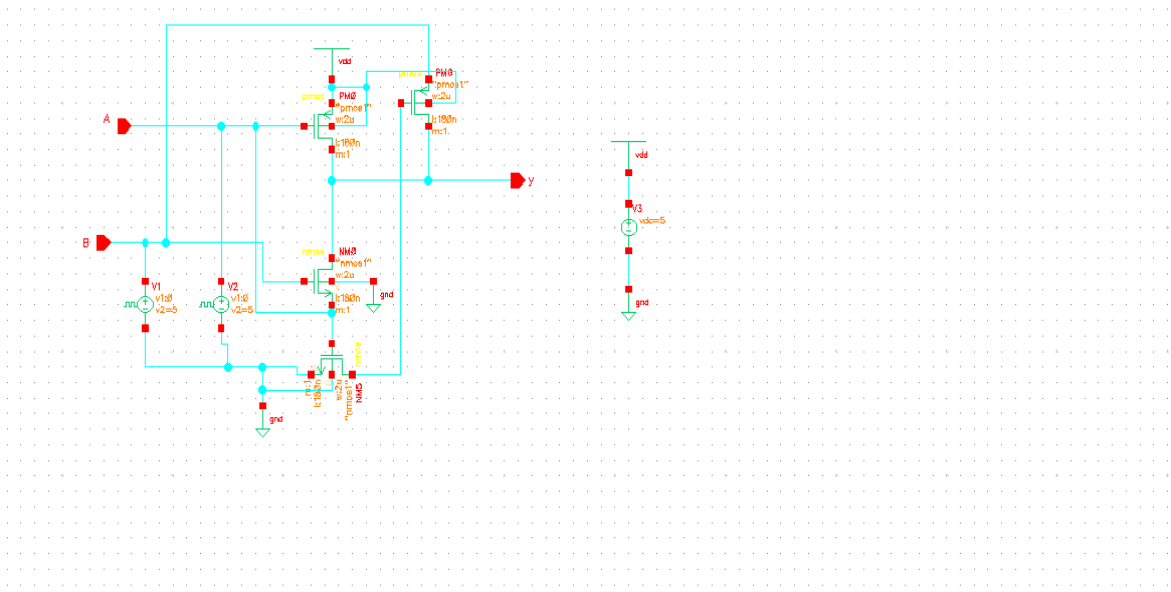


Fig[4.3] : full adder using two 3T XNOR gates and one MULTIPLEXER circuit



Fig[4.4] : Wave forms of Full adder

NOVEL 4T XNOR gate (additional work)



Fig[4.5]: Novel 4T XNOR gate circuit

Fig[4.6] : Wave forms of 4T XNOR gate

As we knew that in conventional CMOS logic above 3.5v to 5v we consider it as a logic 1 and 0 to 1.5v we consider it as a logic 0 at supply voltage of 5v. Above novel 4T XNOR gate will satisfy all the input combinations when we considered as standards of CMOS logic.

If we analyze the wave forms of 4T XNOR gate 3.8 to 5v considered as logic 1 and 0 to 1.5v considered as logic 0 it is satisfying all the input combinations compared to 3T XNOR gate

POWER CALUCULATIONS

Supply voltage	Dynamic power	Static power
1.8	650.2E-6	8.6385508e-11
2.0	725.5E-6	8.6385508e-11
2.2	817.1E-6	8.6385508e-11
2.4	951.2E-6	8.6385508e-11
2.6	19.97E-3	8.6385508e-11
2.8	123.2E-3	8.6385508e-11
3.0	268-9E-3	8.6385508e-11
3.3	563.6E-3	8.6385508e-11

Table[4.1]: power calculations of full adder

DELAY

SUPPLY VOLTAGE	RISE TO FALL	FALL TO RISE
1.8	25.37E-9	-34.09E-12
2.0	25.39E-9	-28.31E-12
2.2	25.14E-9	-23.78E-12
2.4	25.42E-9	-20.06E-12
2.6	25.43E-9	-17.06E-12
2.8	25.44E-9	-14.17E-12
3.0	25.45E-9	-12.19E-12
3.3	25.46E-9	-9.279E-12

Fig[4.2]: Delay calculations of full adder

CHAPTER -5

CONCLUSION AND FUTURE SCOPE

Conclusion: Simulation results tells that proposed XNOR gate has not satisfying some of the inputs as compared to conventional XNOR gate, however irrespective of results it is better interns of power dissipation, delay and area.

Future Scope:

The proposed XNOR and full adder as better in terms of power and delay. We can use these in low power applications and proposed XNOR gate also applicable for parity checker, comparators, compressors, error-detecting and error-correcting codes, phase detector and code converters applications. Proposed full adder can be applicable for where the area requirement is major concern like ASIC, DSP microprocessors etc.

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