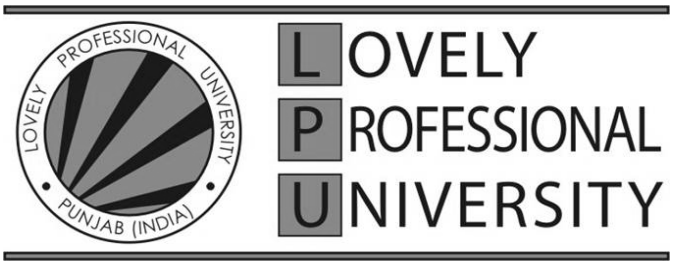

Low Power Analog VLSI Implementation of Cortical Neuron with Threshold Modulation

A Dissertation submitted
by

Ethoti
Radhika

to

Department of Electronics and Communication Engineering

In partial fulfillment of the Requirement for the

Award of the Degree of

Master of Technology in
Very Large Scale Integration

Under the guidance of
Dr. Anita Kumari

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Department of Electronics and Communication Engineering
Lovely Professional University
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ABSTRACT

Neuron is the central processing unit of the brain that transmits and process signal in the form of action potential or spikes in biological systems. These systems are emulated in Very Large Scale Integration using analog principles called neuromorphic systems. Generally threshold voltage in the neuron leads to all or none spike generation. In real scenario threshold voltage is not fixed in the cortical neuron but it varies based on many factors like membrane potential, synaptic connections and activation and inactivation of the ion channels. In this work, the neuron that works with variable thresholds is presented. The proposed cortical neuron circuit generates time varying threshold voltages based on membrane potential. The circuit is capable of generating various types of spiking and firing patterns with diversity similar to that of real biological cortical neuron cell. This circuit is implemented in above threshold design style. The paper describes how threshold modulation is achieved besides operation of the circuit. Simulation results of different patterns are presented along with power that each pattern consumes. The threshold modulation dynamics with respect to circuit is also shown. The circuit is implemented in 0.18µm technology in Cadence Design Environment. The neuron circuit is efficient to be used in microcircuits as it consumes low power.

CERTIFICATE

This is to certify that **Ethoti Radhika** bearing Registration no. **11311233** has completed objective formulation of thesis titled, **"Low Power Analog VLSI Implementation of Cortical Neuron with Threshold Modulation"** under my guidance and supervision. To the best of my knowledge, the present work is the result of her original investigation and study. No part of the thesis has ever been submitted for any other degree at any University.

The thesis is fit for submission and the partial fulfillment of the conditions for the award of M.Tech in VLSI.

Dr. Anita Kumari
Research and Development
Lovely Professional University
Phagwara, Punjab.

Date :

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(Ethoti Radhika)

Reg. No. 11311233

DECLARATION

I, Ethoti Radhika, student of M.Tech VLSI under Department of Electronics and Communication Engineering of Lovely Professional University, Punjab hereby declare that all the information furnished in this thesis report is based on my own intensive research and is genuine.

This thesis does not, to the best of my knowledge, contain part of my work which has been submitted for the award of my degree either of this university or any other university without proper citation.

Date : Signature and Name of the student

Registration No.: 11311233 Ethoti Radhika

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INTRODUCTION

1.1 Biological neural systems:

Biological neural networks performs physiological functions such as thinking, perceiving, motor controlling, sensory processing, decision making etc. with relatively very low energy consumption. These functions are handled by massively parallel neural architectures and yet they are robust. Biological neural systems are comprised of very large number of neurons of nearly about 10^{11}. These neurons are interconnected to other neurons through dendrites with the help of synapses. These neurons are asynchronously activated by the synapse and the interconnections between neurons are quite complex as one neuron is connected to many thousands of neurons. Neurons receive the information from receptor or previous neuron in the form of electrical signal, and it processes the signal before sending it other neuron or effectors. These operations are done at very low noise and almost zero fault tolerance. These systems are very accurate and outperform the modern digital computers in terms of computational efficiency. So now there is vast research going on to understand fundamental principles underlying neural networks which helps to build cognitive processing machines which can adapt to changes, learn, control the functions using parallel architectures. These machines in turn are used to understand the functionality of the brain, used in medical applications such as prosthesis, used in robotic applications etc.

Generally the neural systems can be implemented using computational science which is termed as artificial neural networks (ANN). Artificial neural networks are the models which are inspired by mammal's central nervous system, especially brain. A neural network constitutes of neurons that are interconnected and performs computations on the inputs by feeding information through the neural network. Neural Networks are statistical models which consist of adaptive weights that will be adapted through a learning algorithm, and also neural networks are capable of approximating non-linear functions of the inputs. Though artificial neural networks are widely used they do not provide real time dynamics of the neurons. In order to build an intelligent

processor, neurons which replicate the real neurons are necessary. And in order to emulate exact behavior of the neurons, they are designed using transistors and thus morphing the biological systems into silicon chips is termed as neuromorphic engineering.

1.2 Neuromorphic Engineering:

According to Moore's law the number of transistors on the silicon gets doubled for every 1.5 years. Now if we look at the technology, typically we are using 14nm process which goes further beyond this technology. At some point we can conclude that we build integrated circuits that operate on relatively low power where cmos technology is no longer the option to use. So we need a technology and architecture where devices can be designed without subjecting to such limitations. The great example for such architectures is brain. Because as device technology shrinks then electrons in the transistors will be as messy as ions in the neurons. These analogies lead to the introduction of neuromorphic engineering. And thus from this discussion, neuromorphic engineering has been evolved. The term Neuromorphic engineering was introduced by Carver mead [14], a scientist in Caltech in early 1980's.

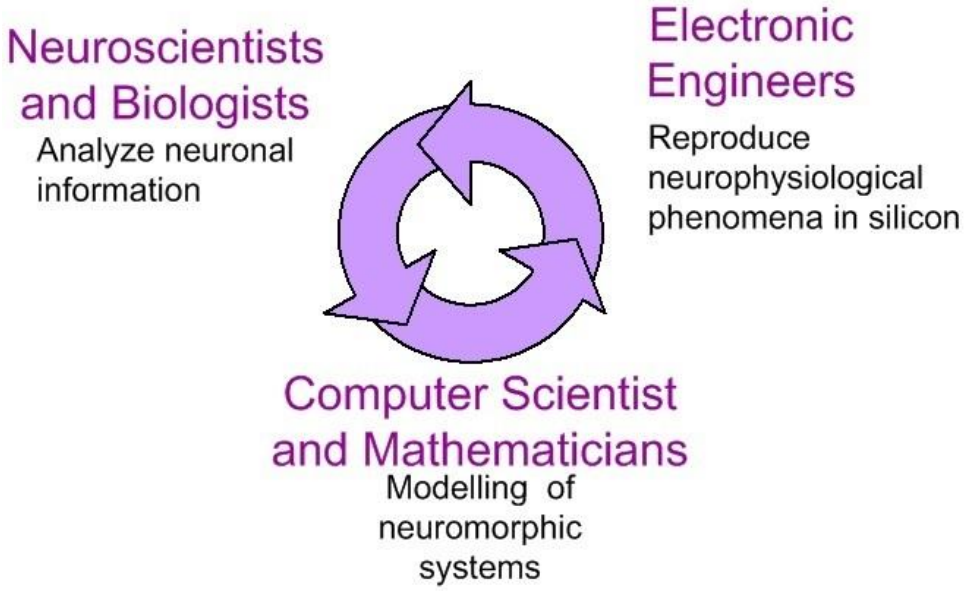


Fig 1.1 Evolution of neuromorphic engineering

Neuromorphic engineering is emulating the biological neural systems in Very Large Scale Integration (VLSI) using analog principles [13] and to understand information processing,

plasticity, neuromorphic computation, neuromorphic modeling etc. The neuromorphic engineering helps us to build a system that is smart and operates fast with low power consumption. Neuromorphic engineering is a interdisciplinary topic that takes inspiration from mathematics, biological sciences, computer sciences and electronics engineering.

1.3 Spiking neural networks:

Spiking neural networks are the most suitable systems to study biological neural circuits realistically as they relate spike-timing to the operating model. The models of spike based neurons provide neural dynamics, timing for computational field of neuroscience. So, there is lot of research going on systems based on spiking neural systems inspired by biological systems. Cortical circuits are designed using spiking neural networks to build an intelligent system that adapts to the environment. There are many ongoing projects inspired by neuroscience, like Blue Brain Project, where neurons in the rat brain are simulated, a project at IBM where 900 million neurons are simulated using 9 trillion synapses of the cortical layer, Neurogrid project at where it uses analog circuits in subthreshold region to simulate cortex region rather than using supercomputers that consumes more power, SpiNNaker project which is a digital processor that is build neural networks, BrainScaleS project in which mixed signal representation is used to model the neurons, which is computationally accelerated i.e. rate of simulation is fast and energy consumption is very low compared to computers used to simulate large scale simulations.

1.4 Neuron:

Neurons are the elementary processing units of the brain or central nervous system. Generally a neuron is made up of soma which is cell body, many thin extended structures called dendrites that arise from soma and axon which is an extension that arises from soma site called axon hillock and are very long. These dendrites are like input devices which receive input currents from other neurons, soma is central processing unit that generates the spike and this is carried to other neurons by axon which acts like output device. The connection between two

neurons is called synapse. The neurons produce electrical signals or chemical signals in order to communicate with neighboring neurons through synapses.

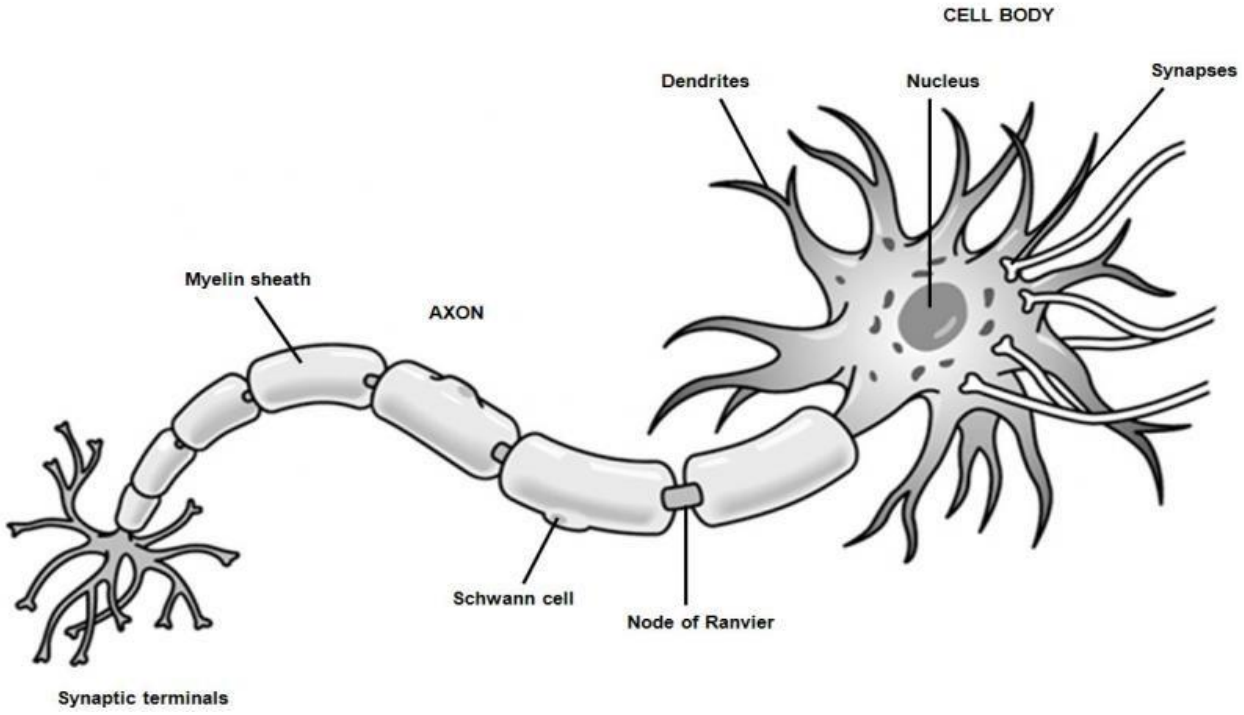


Fig 1.2. Neuron: basic cell

1.4.1 Action potential:

The output of a neuron is an electrical signal of short duration. It has amplitude of about 100mv with duration 2 to 3ms and this is called action potential. Action potential is generated by the neuron when Na^+ and K^+ ions move across the neuronal membrane ion channels that open and close due to the change in membrane potential. When the concentration of the ions inside the neuron changes, then the potential of the membrane changes this results in opening or closing the ion channels. Resting potential of the membrane is approximately -70mv which is said to be polarized. The inflow and outflow of ions through ion channels during neurotransmission will make the inside of the target neuron more positive causing depolarization. When depolarization reaches threshold, large signal is generated called ACTION POTENTIAL. This depolarization is caused due to rapid opening of the Na^+ ion channels and rushing of sodium ions into the cell. After that signal experiences depolarization it will fall and this is called repolarization. Repolarization is caused due to delayed activation K^+ ion channels where the ions rush out of the

cell. When Na^+ channels are inactivated, it takes some time for ion channels to get activated causing hyperpolarization i.e., the membrane potential gets more negative. During this though strong stimulus is applied no action potential will be generated. This period is called absolute refractory period. After 1-2ms the signal gets back to its resting potential where action potential can be generated if strong stimulus is applied. This period is called relative refractory period. In this way spikes are generated and passed forward to other neurons through synapses.

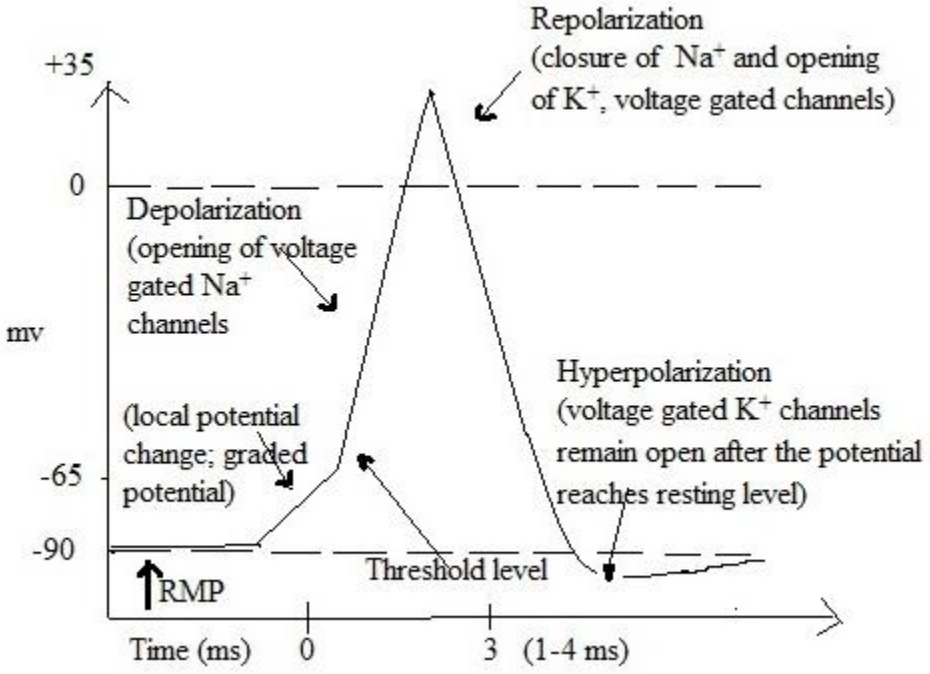


Fig 1.3. Action potential

There will be no change in the form of the signal as it propagates through the axon and form of the signal does not carry any information, but the timing of the spikes that carry information that occurs at regular or irregular intervals.

1.4.2 Silicon neuron:

Neuron is the main element of the brain and silicon neuron is nothing but emulating the electrophysiological behavior of the real neuron. These are implemented in Very Large Scale Integration using analog principles. Using the similarities between ion distribution in the neuron and electron distribution in the transistor we can use the CMOS technology to implement neural

systems which produces exact dynamics. As transistors and neurons share direct analogy they can replicate the self growing connections and make neural computations easy.

Table no.1: Similarities between neuron and transistor:

Neuron	Transistor
There is exponential relation between ion conductance and the voltage across the neuron membrane.	In transistor current and voltage are exponentially dependent on each other in subthreshold region.
The ion channels in the neuron will open based on potential of the membrane.	The number of carriers that causes current depends on the channel whose growth depends upon gate voltage.
The non linear characteristics of the neuron are described by differential equations.	The non linear characteristics of the transistors are also explained by differential equations.

Mixed signal technology (analog and digital) or analog or digital implementations can be used to design the silicon neuron. But analog implementations are advantageous over other implementations as they produce exact behavior of the real neurons, they enables neural prosthesis which operate in real time and they act as a modeling tool to simulate large neural networks. Hardware implementations are preferred over digital implementations even though they are easy because hardware designs are highly efficient in the terms of the energy, they provide exact similarity of the biological systems and neuromorphic systems. Generally not only neurons have been designed, but also synapses are also been modeled in silicon technology to provide post synaptic input current through different ways.

The properties and the dynamics of the real neurons that should be emulated in the silicon neuron are temporal integration, threshold modulation, spike frequency adaptation and absolute refractory period, etc. Temporal integration is integrating all the presynaptic input currents received by the postsynaptic neuron to generate a spike. Threshold voltage is responsible for the all or none spike, i.e., if membrane potential crosses the threshold it will generate a spike otherwise nothing.

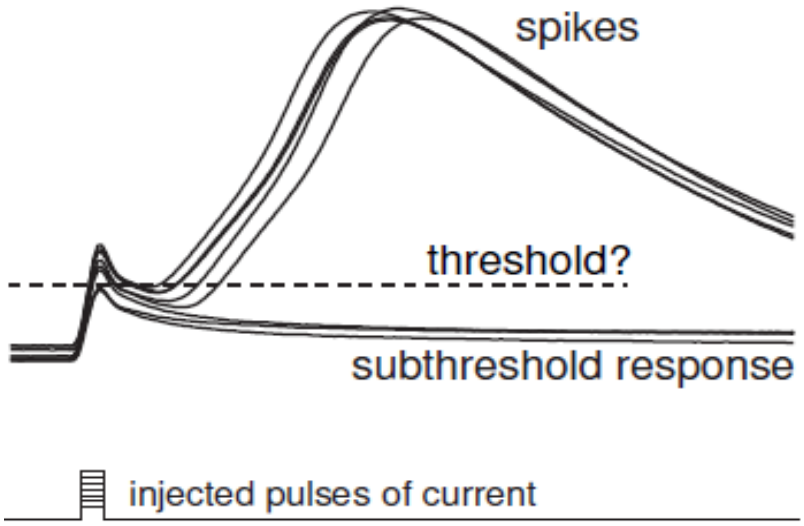


Fig 1.4. Effect of threshold voltage on membrane voltage

Spike frequency adaptation is the one of the dynamics of the neuron that explains increase in the frequency of the action potentials that have been fired with constant stimulus caused by many factors in the neuron. A silicon neuron should be designed where it generates action potential as well as produces the dynamics of the neuron emulating the real neuron.

1.4.3 Neuron models:

Neurons have been implemented in silicon using following models. These are the spike based neuron models:

1. **Integration and fire neuron model:**

   This is simple neuron model and mostly used. This is the first neuron model explained by Lapicque in 1907. Neuron is represented in this model is given as

$$I(t) = C_m \frac{dV_m}{dt}$$

Where c_m is given as membrane capacitance and

v_m is membrane voltage

When input current is applied then the membrane voltage increases with respect to time t and when it reaches threshold v_{th} a spike is generated which is action potential and the voltage will reset to its resting potential. The firing frequency increases as the current increases with respect to time.

Leaky integrate and fire neuron model and exponential integrate and fire neuron models are introduced after this model. They provide better spikes than integrate and fire model as leaky neuron model includes memory element in the form of leaky capacitor and exponential model produces exponential signal that depends on many factors. The shape of the spike is accurate and these are improved models of integrate and fire neuron model.

2. Hodgkin and Huxley model:

This neuron model was developed in the year 1952 by A.L. Hodgkin and A.L. Huxley. They experimented on squid axon giant axon [4] and developed famous neuron model. The neuron model explains evolution of sodium and potassium currents with sodium and potassium conductances. This is first spike based model and emulates the ion channels of the neuron. The total membrane current is given as

$$I = c_M \frac{dv}{dt} + g_k n^4 (v - v_k) + g_{Na} m^3 h (v - v_{Na}) + g_l (v - v_l)$$

Where

$$\frac{dn}{dt} = \alpha_n (1 - n) - \beta_n n$$

$$\frac{dm}{dt} = \alpha_m (1 - m) - \beta_m m$$

$$\frac{dh}{dt} = \alpha_h (1 - h) - \beta_h h$$

And g_{Na} and g_k are the sodium and potassium conductances respectively and m, n, h are the gating variables used in the neuron model to attain the action potential. This model provides rich dynamics similar to real neuron.

3. Fitzhugh-Nagumo neuron model:

This model was named after Richard Fitzhugh who suggested the system in 1961 and Nagumo created the circuit which describes a prototype of the excitable system. This model is oscillatory in which as external applied current exceeds threshold a characteristic change in phase space is occurred. In this way spikes are generated in neuron. The dynamic equations are given by

$$\frac{dv}{dt} = v - \frac{v^3}{3} - w + I_{ext}$$

$$\tau \frac{dw}{dt} = v + a - bw$$

This is simplified version of Hodgkin and Huxley model. The oscillator in this model as Bonhoeffer-vander pol oscillator as it have special cases where a=b=0. Experimentally determined parameters are given by a=-0.7, b=0.8.

4. Morris-Lecar model:

This was developed by Catherine Morris and Harold Lecar in the year 1981. They reproduced an oscillatory behavior in giant barnacle music fiber with calcium and potassium conductance. Class-1 and class-2 excitability neurons are exhibited in this model. They combined both Hodgkin and Huxley model and Fitzhugh-Nagumo model into voltage gated calcium channel with delayed rectifier potassium channel. The equations described are

$$c \frac{dv}{dt} = -I_{ion}(v, w) + I$$

$$\frac{dw}{dt} = \varphi \frac{w_\infty - w}{\tau_w}$$

Where

$$I_{ion}(v, w) = g_{ca} m_\infty (v - v_{ca}) + g_k w (v - v_k) + g_l (v - v_l)$$

5. Hindmarsh-Rose model:

This model is developed by Hindmarsh and Rose in the year 1984 to study the spiking bursting behavior of the membrane potential in the neuron. This is also oscillatory neuron model. Here y(t) is the spiking variable which measures the transport of the ions through fast ion channels and z(t) is the bursting variable which measures the transport of the ions through slow ion channels. The non-linear differential equations describing these dynamic variables are

$$\frac{dx}{dt} = y + ax^2 - x^3 - z + I$$

$$\frac{dy}{dt} = 1 - bx^2 - y$$

$$\frac{dz}{dt} = r(4\left(x + \frac{8}{5}\right) - z)$$

Where x, y, z are the state variables

6. Izhikevich neuron model:

This model was proposed by Izhikevich [7] in the year 2003. This is a simple model explained by two state variables with two simple non linear differential equations. This model is computationally efficient and produces the rich dynamics that a real neuron defines. Iz model is reduced model of Hodgkin and Huxley neuron model using bifurcation analysis. The two differential equations that explain the neuron are

$$\frac{dv}{dt} = 0.04v^2 + 5v + 140 - u + I$$

$$\frac{du}{dt} = a(bv - u)$$

If v > 30 mv then v = c and u = u+d and a, b, c, d are state variables. The state variables are used to achieve the different firing patterns of the neuron. It is a simple model that produces spiking, mixed mode spiking patterns, bursting, subthreshold oscillations, spiking with frequency adaptation etc with the help of state variables.

1.4.4 Cortical neuron:

Cortical neurons are the cells that exhibit the most complex activity of the brain such as perception, cognitive processes, voluntary movement etc. This neuron shows different non-oscillatory firing, bursting and spiking patterns [2]. Cortical neurons are not physiologically homogenous, the spikes generated by them in response to step current are different for different neurons. We divide these patterns of firing mainly into three classifications: Regular Spiking (RS), Fast Spiking (FS) and Intrinsically Bursting (IB). Cortical neuron firing patterns are different because of the location, dendrite and synaptic connection etc.

Regular Spiking (RS): RS neurons are typical neurons found in neocortex, and when stimulated they produce spikes with short spike frequency and as we prolong the stimulus, frequency of spike decreases achieving spike frequency adaptation. RS neurons are excitatory cortical cells, the firing patterns in RS neuron is it fires few inter short spikes with a step input and after that period increases. This kind of spiking can be found in excitatory pyramidal neurons.

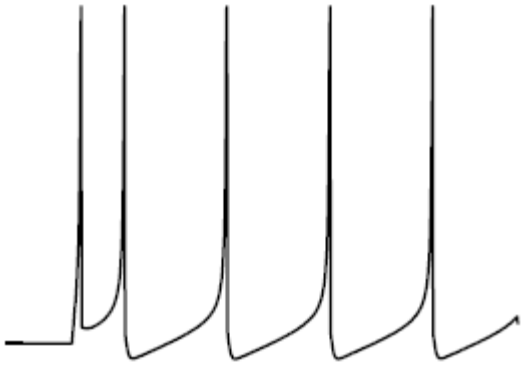


Fig 1.5. Regular spiking pattern

Fast spiking (FS): FS neurons are inhibitory cells and fires spike continuously and in fast manner and spike frequency adaptation property is not exhibited by these cells. The fast spiking interneurons are responsible for the synchronization of the neural network and firing patterns of these neurons are complex. This kind of firing patterns can be seen in bitufied cells, small & large basket cells, nest basket cells etc. in neocortex.

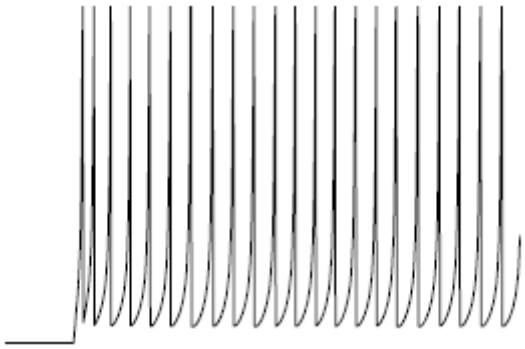


Fig 1.6. Fast spiking pattern

Intrinsically Bursting (IB): IB neurons are excitatory cells and come under bursting category. Burst is a response to the minimal stimulus applied to the circuit. It is similar to the regular spiking with a little difference in after depolarization. It produces a burst of spikes followed by single spikes fired repeatedly thus converting the bursting into spikes. IB firing patterns are mostly seen in bipolar cells and martinotti cells in the brain's neocortex.

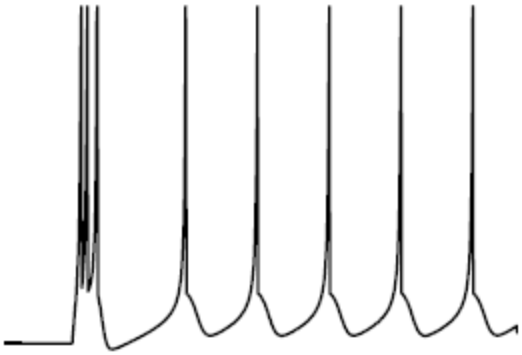


Fig 1.7. Intrinsically Bursting pattern

Chattering (CH): CH neurons are excitatory cells and produces burst of spikes periodically for sustained input. The inter-burst frequency generated has frequency of 40-50 Hz. The cells that perform chattering pattern also comes under bursting category.

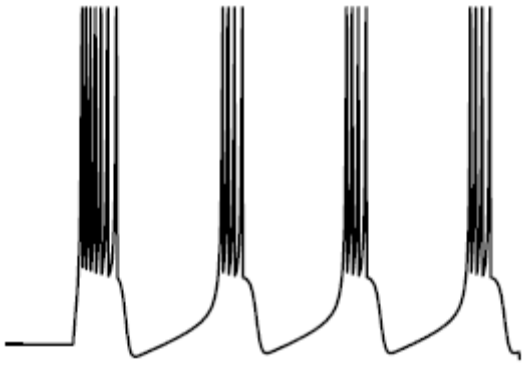


Fig 1.8. Chattering pattern

CHAPTER 2

LITERATURE REVIEW

In this chapter we present the work that is done already related to silicon neuron.

1. **Misha Mahowald & Rodney Douglas (1991) [12]:** On the basis of similarity between semiconductor physics and biological membrane physics neuron is designed. Using VLSI technology ion currents are designed, together they form silicon analogue biological neuron which can be used for implementing mathematical abstractions of the neuron. The activation and inactivation of the membrane conductances that control the sodium current and potassium current are both time and voltage dependent. Here the cell membrane is represented by a capacitor and the membrane conductances and control mechanisms are represented by the individual circuits and connections between these circuits are also well explained to produce Na depolarization, K repolarization and Ca after hyperpolarization. Analogy between real nerve cell and proposed neuron circuit is presented to compare how well the silicon neuron is emulating the real neuron.

2. **Barranco, Sinencion, Rodriguez & Huertas (1991) [10]:** In this Fitzhugh-Nagumo neuron model is presented in which fundamental description of biological mechanisms is given, mathematical model for this model and the circuit description regarding mathematical equations is explained. This oscillatory neuron is mostly used in small biological systems. In this Na, K, Cl ion channels has been emulated, by realizing non-linear differential equations. Generally Fitzhugh Nagumo model is the modified and simple model of Hodgkin & Huxley neuron model. In order to implement equations directly transconductance mode technique is used to implement linear and nonlinear equations. Generally in order to implement nonlinear equations translinear circuits are used. It is implemented in 2um cmos technology.

3. **Schultz & Jabri (1995) [20]:** explains separate integrate and fire circuits for silicon design. It contains two comparators to generate action potential, feedback loops to exhibit spike frequency adaptation and also explains how after hyperpolarization is achieved. The silicon neuron consists of 20 transistors.
   In this feedback loop is used to achieve refractory period and additional negative feedback loop is used to achieve spike frequency adaptation. With applying certain voltage values action potential is produced. This neuron is implemented in orbit 1.2um technology.

4. **Patel & Deweerth (1997) [18]:** A silicon neuron based on Morris Lecar neuron model is designed. Generally motor control in the brain is done by neural oscillators. In biological systems, these oscillatory patterns are generated due to the synaptic interconnectivity among a group of individual neurons. These oscillatory patterns are emulated with two state simple differential equations of Morris Lecar model. In order to generate bursts the membrane should have slow intrinsic time constant in addition to the fast time constant. In this neuron is designed using slow variable and membrane variable and their nullcline analysis is also explained. The shape of nullcline is linear in the case of slow variable where as in membrane variable it is cubic in shape. The circuit is biased in such a way that all three modes such as silent mode, bursting mode, tonic mode are operated in the circuit. It is implemented in 350nm cmos technology and simulated in HSPICE.

5. **L.F. Abbott (1999) [11]**: he explained integrate and fire neuron model that was implemented using an electrical circuit by Lapicque in 1907. The circuit consists of a capacitor and leakage resistor. Even though it does not produce actual action potentials it was used to compute the firing frequency of the nerve fiber. This allows us to design neural systems without expending time and energy on modeling a phenomenon, where neural computations are not important and the generation of action potentials are mattered in that case we can use this model.

6. **Simoni & Deweerth (1999) [21]:** Biological neuron that implements self-adaptation of its parameters is presented in this neuron model. Adaptation can be added to the neuron models to decrease their parameter space, compensate for device mismatch, and stabilize the behavior by modulating parameters continuously. Self-adaptation can facilitate single parameter control over a multi parameter system, stability of the system to fluctuations in parameters and coordinated modulation of parameters to achieve a desired behavior. Silicon neuron has a membrane block as well as adaptation block. We have four VLR differential pairs, two smaller amplifiers which are standard five-transistor OTA's and the larger amplifier is a VLR OTA. It emulates the conductance-based model explained by Hodgkin & Huxley.

7. **Rasche & R. Douglas (2000) [19]:** The improved silicon neuron has less circuitry and fewer parameters than previous circuits thereby improving the spiking characteristics. The differential equations governing the revised circuits are described and are used them for explaining the spiking properties of the SN. We also describe how to tune the parameters efficiently to bring the neuron quickly into its correct operating regime. In this different ion conductance circuits are designed such Na ion conductance, K ion conductance, leakage current conductance etc. The building blocks used in SN circuit are the transconductance amplifier (TCA), the follower integrator (FI), the current mirror (CM) and the half wave rectifier. The circuit was implemented in 1.2um CMOS standard technology.

8. **Giacomi Indiveri (2003) [6]:** A low-power analog circuit for implementing leaky integrate and fire neuron model is presented. The proposed circuit includes elements for implementing spike frequency adaptation, for setting an arbitrary refractory period and for modulating the neuron's threshold voltage and consumes low-power. Integrate and fire (I&F) circuits typically integrate small currents onto a capacitor until a threshold is reached. As the voltage on the capacitor exceeds the threshold a fast spike is generated and the capacitor is reset. In the circuit designed a source follower for increasing the linear integration range and for modulating the neuron's threshold voltage is used, an inverter with positive feedback for reducing the

switching short-circuit currents at the input, an inverter with controllable slew-rate for setting arbitrary refractory periods, a digital inverter for generating the pulse that signals the occurrence of a spike, a transient current-mirror integrator for implementing the spike-frequency adaptation mechanism, and a minimum size transistor for implementing a constant current leak. Totally this neuron consists of 20 transistors and a capacitor. The circuit is implemented in 1.5um standard CMOS technology process.

9. **Izhikevich (2003) [7]:** He proposed a new neuron model that is suitable for generating bursting and spiking characteristics of the neuron. This model provides computational efficiency like integrate and fire model as well as produces dynamics exactly same as conductance based neuron model which are usually implemented using Hodgkin and Huxley model. This model was proposed in 2003 and still many neuroscientists are using this model in order to emulate the electrophysiological properties of the neuron. In this paper simulations are done in MATLAB.

10. **Lee et. al. (2004) [9]:** In this neuron is designed using Hindmarsh-Rose neuron model. Difference between digital implementation and analog implementation is presented. Analog controller is used in robot systems and this is designed based on three differential equations. In order implement the above equations, subthreshold op amps, current sources, multiplier cores, resistors are used. Operation and design of each building block used in this design are presented. Mos resistor is used to reduce the power and size. This is implemented in 250nm technology.

11. **Nakada, Asai & Hayashi (2005) [17]:** In this paper resonate and fire neuron model is implemented based on Izhikevich resonate and fire equations. This neuron is designed based on volterra system that is used to implement nonlinear differential equations. The RFN model is a simple spiking neuron model that exhibits dynamic behaviors observed in biological neurons, such as fast subthreshold oscillation, post-inhibitory rebound, and frequency preference. The RFN circuit consists of a membrane circuit, a threshold-and-fire circuit, and current mirror integrators as

excitatory and inhibitory synapses. The membrane circuit was derived from the Volterra system to mimic membrane dynamics of the RFN model.

12. **Wijekoon and Dudek (2007) [23]:** In this a compact silicon neuron is designed which emulates the cortical neuron. In this different firing patterns are obtained by controlling two variables. The number of transistors used in this model is 14. Spiking is achieved by membrane circuit, slow variable circuit and comparator circuit. This neuron follows the izhikevich neuron model. It is explained in this report and different firing patterns are also presented. This circuit uses low power and also exhibits all the dynamics of the real neuron. This can be implemented in large neural networks as they are consuming low power as well as low silicon area.

13. **Stefan Mihalas and Ernst Neibur (2009) [15]:** In this paper, a generalized leaky integrate and fire model is presented. It produces various tonic, phasic, spiking, bursting and adapting responses of the neuron. The neuron implemented in this paper is modeled using a set of differential equations that explain the membrane potential generation, variable threshold voltage and number of induced currents. Each variable in the neuron have biological significance and is updated by an update rule when the spike reaches threshold. It exhibits rich dynamic behavior obtained due to complex update rules.

CHAPTER 3

3.1 Objective of the study:

Generally neuromorphic engineering is the hardware emulation of the neural systems. Silicon neuron is the analog VLSI implementation of the biological neuron, where it replicates the characteristics of the real neuron. The advantage of silicon neurons over artificial neurons is that they provide better computational power, they use parallel architectures for biological plausibility, and they can simulate the electronic properties of the neuron directly. So, this technology is used to design the cortical area where complex activities occur in order to build a intelligent system like brain. To build an efficient intelligent system, neurons should emulate the exact behavior of the neuron. The dynamics of the neurons such as spike frequency adaptation, temporal integration, sensory adaptation etc should be effectively implemented with less number of transistors and with low power consumption. In this work cortical neuron is designed and explained in following sections. The objective of the study is to generate every pattern that a cortical neuron produces and exhibit the dynamics of the neuron as well. As we compare the proposed circuit with other silicon neurons it is capable of providing almost all dynamics of the neuron.

3.2 PROBLEM FORMULATION:

Generally a real neuron produces action potential and some dynamics which explain their explicit behavior. But artificial neurons are meant only to produce action potentials they do not produce any dynamics. On the other hand silicon neuron produces action potential as well as electrophysiological behavior of the neuron. In order to emulate brain mimicking systems silicon neurons are preferred over artificial neurons. In many neuron designs it is assumed that an action potential in a neuron is initiated after crossing fixed threshold voltage. But recent study [8] says that threshold voltage is not fixed in the cortical neuron but it varies depending on various factors in the neuron. The change in threshold voltage in real neurons are because of opening and closing of voltage gated slow potassium ion channels and voltage gated sodium ion channels, synaptic connections through dendrites and site in the soma where spike is initiated. And experimental results show that spike threshold and membrane potential are inversely proportional to each other [20]. Due to increase in threshold voltage, voltage gated sodium will get inactivated thus decreasing the membrane potential. This change in threshold voltage is called threshold modulation. The proposed neuron circuit achieves threshold modulation, where threshold voltage is changes with respect to membrane potential. The circuit proposed in produces all bursting and firing spikes but it does not exhibit threshold modulation. So a circuit should be proposed where it can produce all spiking and bursting characteristics and also exhibits threshold modulation, achieving the dynamic behavior of the real neuron.

3.3 Methodology:

Cortical neuron cells exhibit the most complex activities in the brain such as perception, cognitive signal processing, voluntary motor control etc. It exhibits non linear oscillatory behavior due to which it produces different firing and spiking patterns. In order to implement these non linear characteristics in analog principles, efficient model that is capable of providing dynamics of real cortical neuron is to be selected. We can use Integrate and Fire model as it is widely used because of its simplicity and computational effectiveness but it cannot produce bursting and firing patterns like a cortical neuron does. Other model which provides rich dynamics is Conductance-based neuron model but it is not computationally adaptive. Other oscillatory models such as Fitz Hugh Nagumo, Resonate-and-Fire, Morris Lecar, Hindmarsh-Rose and Hardware Oregonator cannot be used as they produce poor spikes. So Izhikevich neuron model is used which is computationally effective as well as biologically plausible as HH model.

3.3.1 Circuit Description:

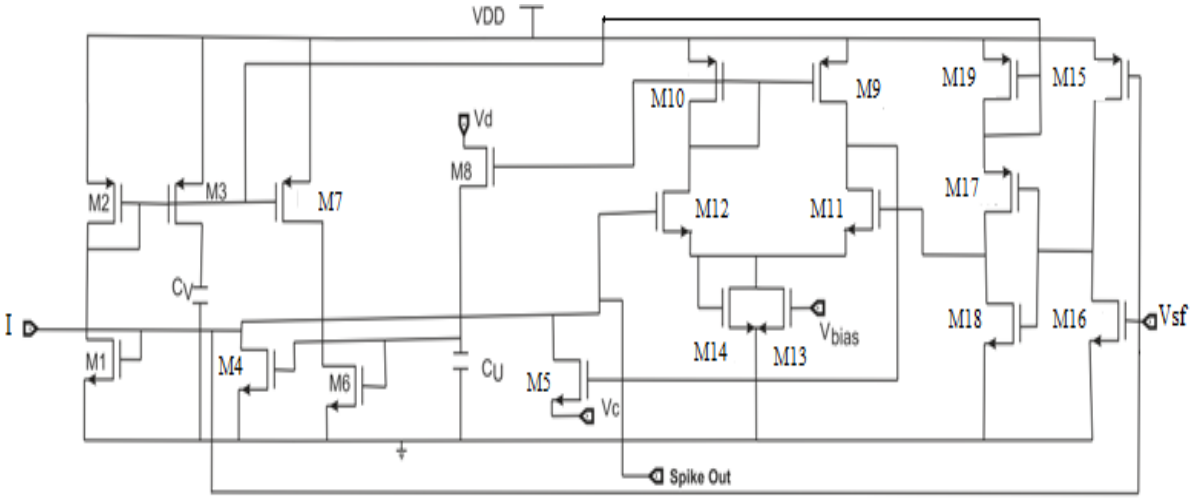


Fig. 3.1. Proposed neuron circuit

The proposed neuron circuit emulating the cortical neuron is presented in Fig 3.1. The circuit consists of 19 transistors. It implements two state variables of the neuron model they are

membrane potential (V) and slow variable (U). The circuit is mainly divided into four blocks i.e., membrane potential circuit (M1-M5) to generate the spike, slow variable circuit (M1, M2, M6-M8) also called as accommodation variable to achieve frequency adaptation, comparator circuit (M9-M14) for after spike resetting and threshold modulation circuit for variable thresholds.

3.3.1.1 Membrane potential circuit:

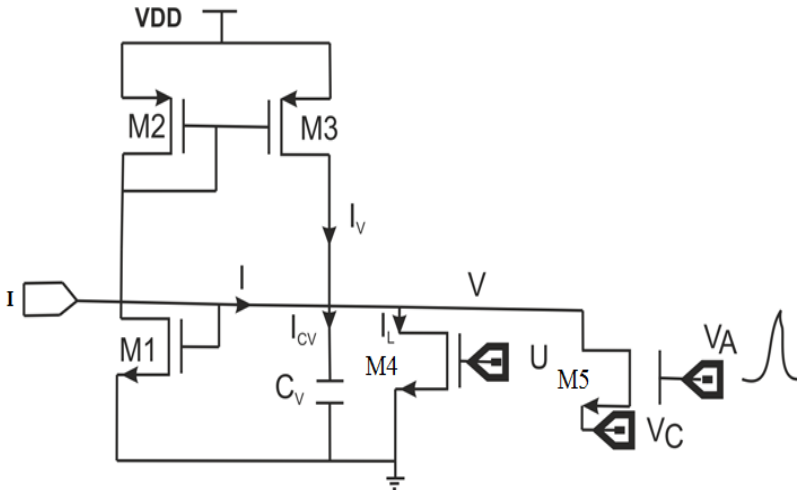


Fig. 3.2. Membrane potential

The circuit shown in Fig 3.2 is used to implement the state variable 'V'. The current mirror circuit (M1-M3) copies the current onto transistors M2 and M3 and produce the membrane current I_v. The membrane current is positive feedback current to membrane capacitor C_v that helps to generate the spike. I_l is the leakage current through M4 which is controlled by slow voltage and I is pre synaptic current. All these currents are integrated on to membrane capacitance and is given by

$$C_v \frac{dv}{dt} = I_v - I_l + I$$

In this increase in the input current increases the membrane potential and thus producing the spike as shown in Fig 3.6(a). After the spike is generated it is detected by the comparator circuit. The comparator circuit generates a pulse V_a when the membrane potential is greater than

threshold voltage, this pulse is fed to transistor M5 that will make the membrane capacitor to discharge completely and thus the membrane potential will be reset to V_c. In this way after spike resetting is achieved.

3.3.1.2 Slow variable circuit:

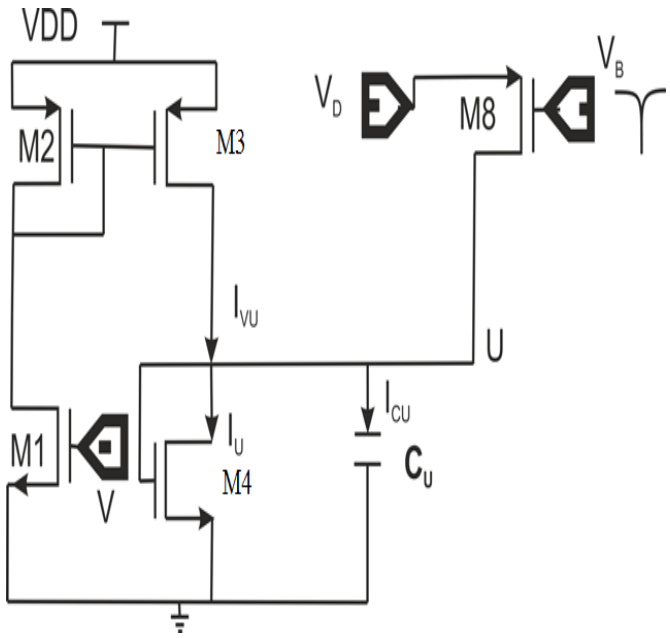


Fig. 3.3. Slow variable circuit

Slow variable also called as the accommodation variable i.e., adaptation variable implements the second equation of the neuron model. As shown in the Fig 3.3 the current I_{cu} is controlled by the transistor M1 through the current mirror circuit M2 and M7. The current Iu is controlled by the transistor M6 which is a nonlinear resistor. The currents that are integrated on the slow variable capacitor C_u are given as:

$$C_u \frac{du}{dt} = I_{vu} - I_u$$

When spike crosses the threshold voltage comparator generates a pulse V_b which is connected to transistor M8. Due to narrow width of M8 the capacitor will not be completely reset to V_d instead the charge gets added on to the slow variable capacitor and this results in the spike

frequency adaptation as shown in Fig 3.6(b). Generally to achieve frequency adaptation capacitor Cu is selected to be larger than the membrane capacitor C_v as well as to vary slow variable u slowly we make the size of M7 smaller than M3.

3.3.1.3 Comparator circuit:

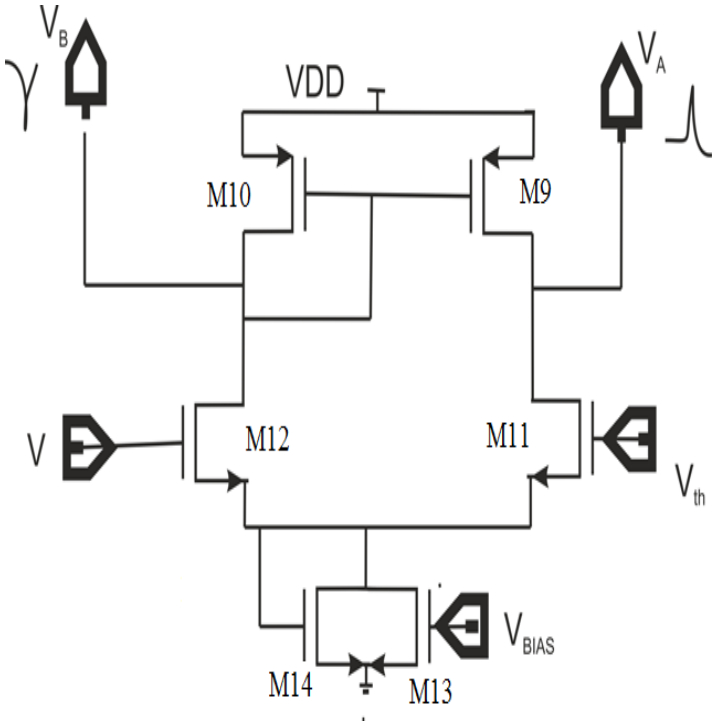


Fig. 3.4. Comparator circuit

The comparator circuit shown in Fig 3.4 compares the membrane potential and threshold voltage and when spike crosses the threshold two pulses V_a and V_b will be generated such that V_a will be greater than V_b. V_a will be connected to transistor M5 which will reset the membrane voltage to V_c and V_b is connected to transistor M8 such that slow variable will be set to $u+V_d$. Here transistors aspect ratios are considered such that when the spike crosses the threshold the circuit takes some time to generate the pulses and till then the action potential will be generated. V_{bias} provides the biasing to the comparator circuit. The pulses generated are shown in Fig 3.6(c)&(d).

3.3.1.4 Threshold modulation circuit:

Threshold modulation is provided by the transistors M15-M19 as shown in Fig 3.5. In the neuron, threshold voltage is not fixed value instead it changes with respect to membrane potential. In the circuit in order to achieve this membrane potential is connected in feedback through source follower and inverter circuits. Source follower is used to control the membrane voltage whose output will be

$$V_{th} = k(V_{mem} - V_{sf})$$

where k=slope coefficient, V_{mem} is membrane potential and V_{sf} is bias voltage applied at source follower. This voltage will be given to inverter that generates the threshold voltage as shown in Fig 3.6(d). This circuitry provides time varying threshold voltages for action potentials generated thus achieving the dynamic behavior of the real neuron.

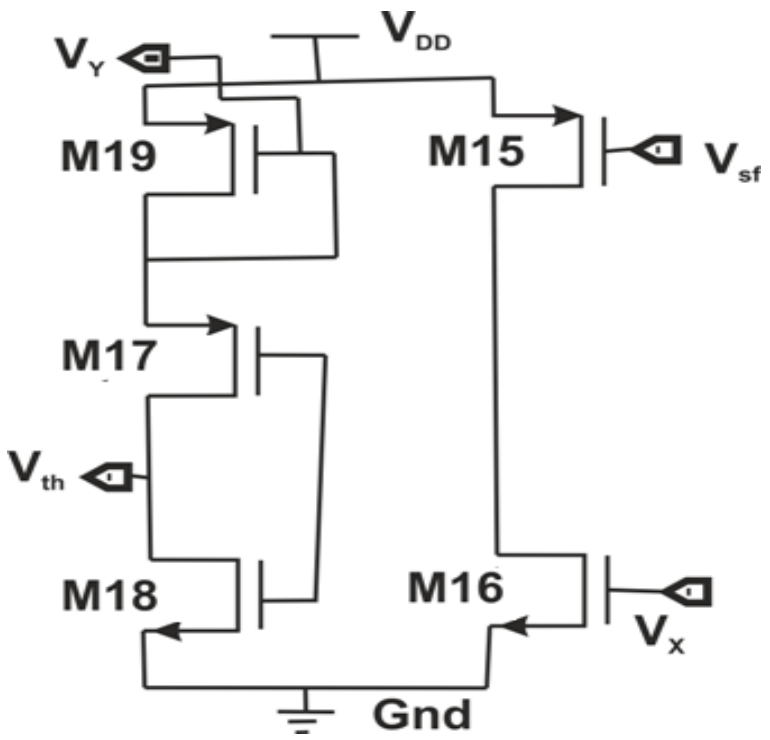


Fig. 3.5. Threshold modulation circuit

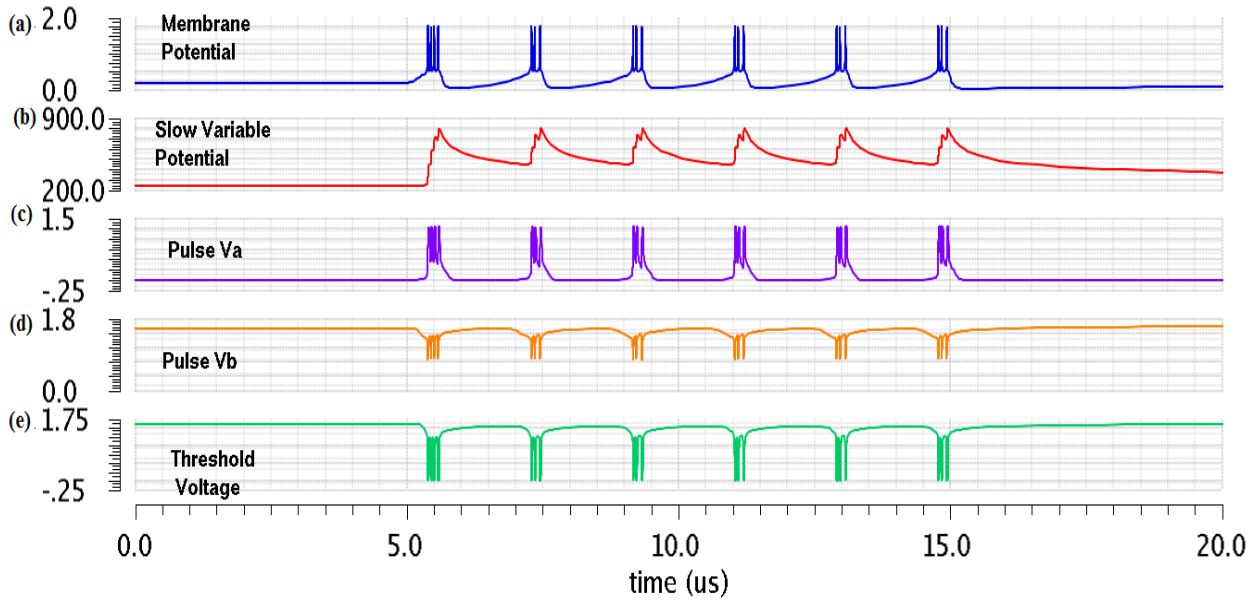


Fig. 3.6. Waveforms of the sub circuits of the neuron circuit

3.4. Mathematical model of the circuit:

Any non linear system can be well explained by first order differential equations. The proposed neuron is also explained by the mathematical model that will provide the dynamics of the cortical neuron. Consider equation of the membrane potential explained in section 3.3.1.1,

$$C_v \frac{dv}{dt} = I_v - I_l + I$$

can be expanded as follows

$$C_v \frac{dv}{dt} = \begin{cases} \frac{1}{2}\alpha\mu_n C_{ox}\frac{W}{L}_{M1}(V - V_t)^2 - \frac{1}{2}\beta\mu_n C_{ox}\frac{W}{L}_{M4}(U - V_t)^2 + I \; when \; V \geq U - V_t \\ \frac{1}{2}\mu_n C_{ox}\frac{W}{L}_{M4}((U - V_t)V - \frac{1}{2}v^2 + I \;\; when \; V < U - V_t \end{cases}$$

As the transistors enters into saturation for higher membrane potential values and remains in linear region when membrane potential is less than slow variable voltage. Because of this voltage increases slowly until transistors enters into saturation region there after it increases the voltage rapidly.

From slow variable equation from the section 3.3.1.2,

$$C_u \frac{du}{dt} = I_{vu} - I_u$$

can be expanded as follows

$$C_u \frac{du}{dt} = \frac{1}{2}\alpha\mu_n C_{ox} \frac{W}{L}_{M1} \frac{L}{W}_{M2} \frac{W}{L}_{M4} (V - V_t)^2 - \frac{1}{2}\gamma\mu_n C_{ox} \frac{W}{L}_{M6} (U - V_t)^2$$

As I_{vu} current is due to current mirror M1-M2 and also due to leakage transistor M6, and all the transistors are in saturation.

As threshold varies according to the membrane potential the output of source follower is given as follows,

$$V = k(V_{mem} - V_{sf})$$

and threshold voltage is the inverted output of above equation 'V'. 'k' depends on drain to source diffusion capacitance and gate oxide capacitance.

In the above equations (W/L) are the aspect ratios of the respective transistors. α, β, γ are the parameters that depend on V, U and V_t and their values are given in the Table 2.

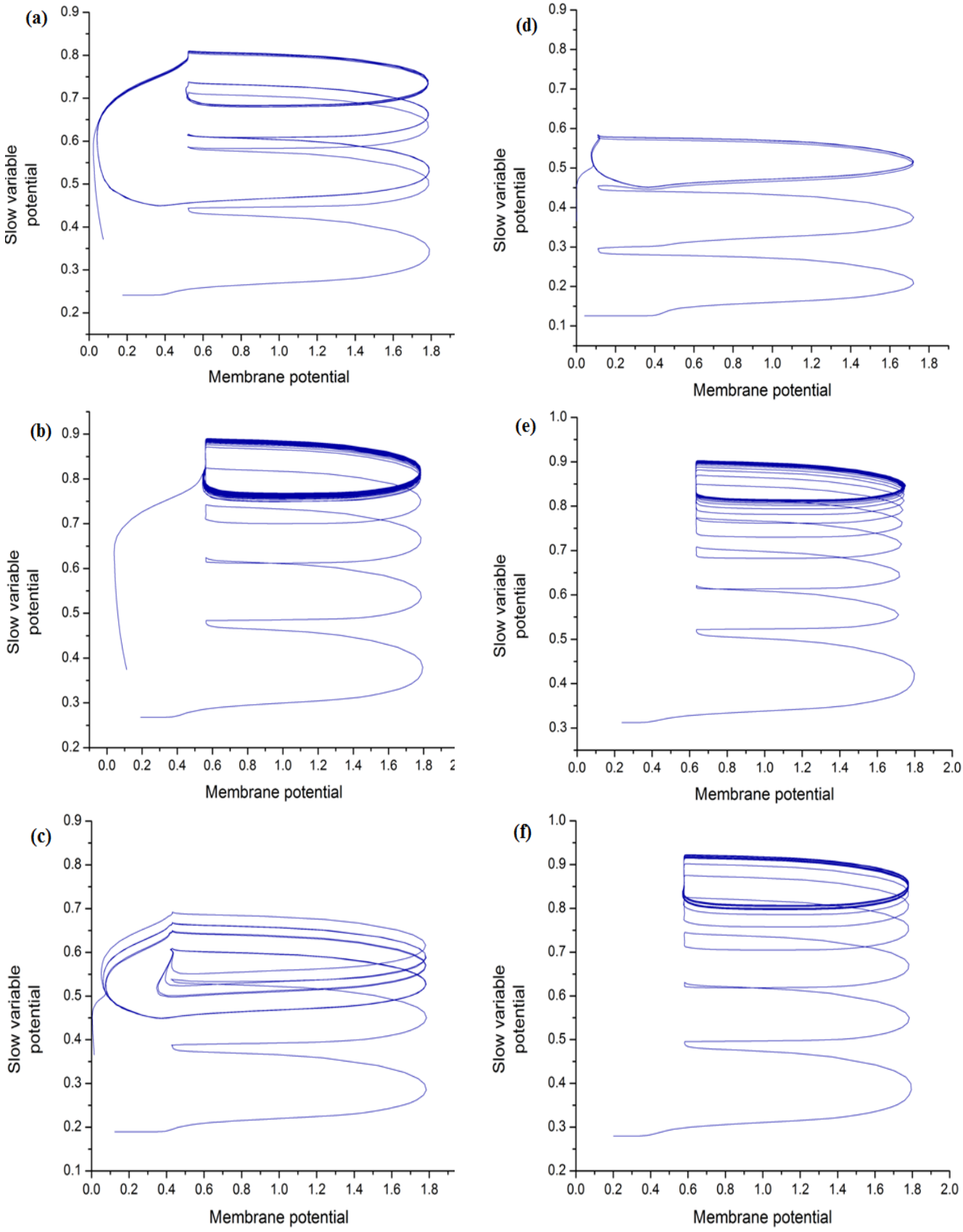
Table no.2: Parameter values used in the neuron circuit

parameters	**V<U-V_t**		**V>=U-V_t**	
	U<V_t	**U>=V_t**	**U<V_t**	**U>=V_t**
α	0	0	1	1
β	0	1	1	1
γ	0	1	0	1

3.5. Operation of the circuit:

The proposed circuit consists of 19 transistors that is divided into four sub blocks as explained in above section. Input stimulus current of about 0.1μA is applied to the neuron. A cortical neuron exhibits different spiking and bursting characteristics, these various responses can be achieved by tuning two voltages appropriately i.e., V_c and V_d. The operation of the circuit is explained by state trajectories. The state trajectories explain the dynamics and the new route it takes after attaining certain dynamic in the terms of two state variables membrane potential (V) and slow variable potential (U).

Consider state trajectory of CH shown in Fig 3.7(a), the membrane potential increases because of input stimulus and then due to positive feedback in the circuit it increases rapidly causing upswing of the spike and after spike is fired, comparator detects the spike and resets the membrane potential by discharging capacitor C_v to the value V_c. As $V_c < V_{th}$, the reset circuit will be deactivated. As shown in the Fig slow variable also increases with each spike, at a certain point the trajectory undergoes a dynamic change and follows new route at which the capacitor C_u starts discharging. Thus slow variable 'u' decreases and after that membrane potential becomes dominant compared to slow variable potential and due to this series of spikes are produced at that time repeating the cycle. Until the input stimulation is provided this process of generating the spike continues. This process is same for all the firing patterns RS, FS, CH, IB etc. of the cortical neuron. In this way various patterns are obtained and their respective state trajectories are shown in Fig. In order to achieve threshold modulation the membrane voltage is connected in the feedback with source follower circuit and the inverter. This circuitry will be responsible to achieve the reverse relation between membrane potential and threshold voltage.


(a)
(b)
(c)
(d)
(e)
(f)
Slow variable potential
Membrane potential

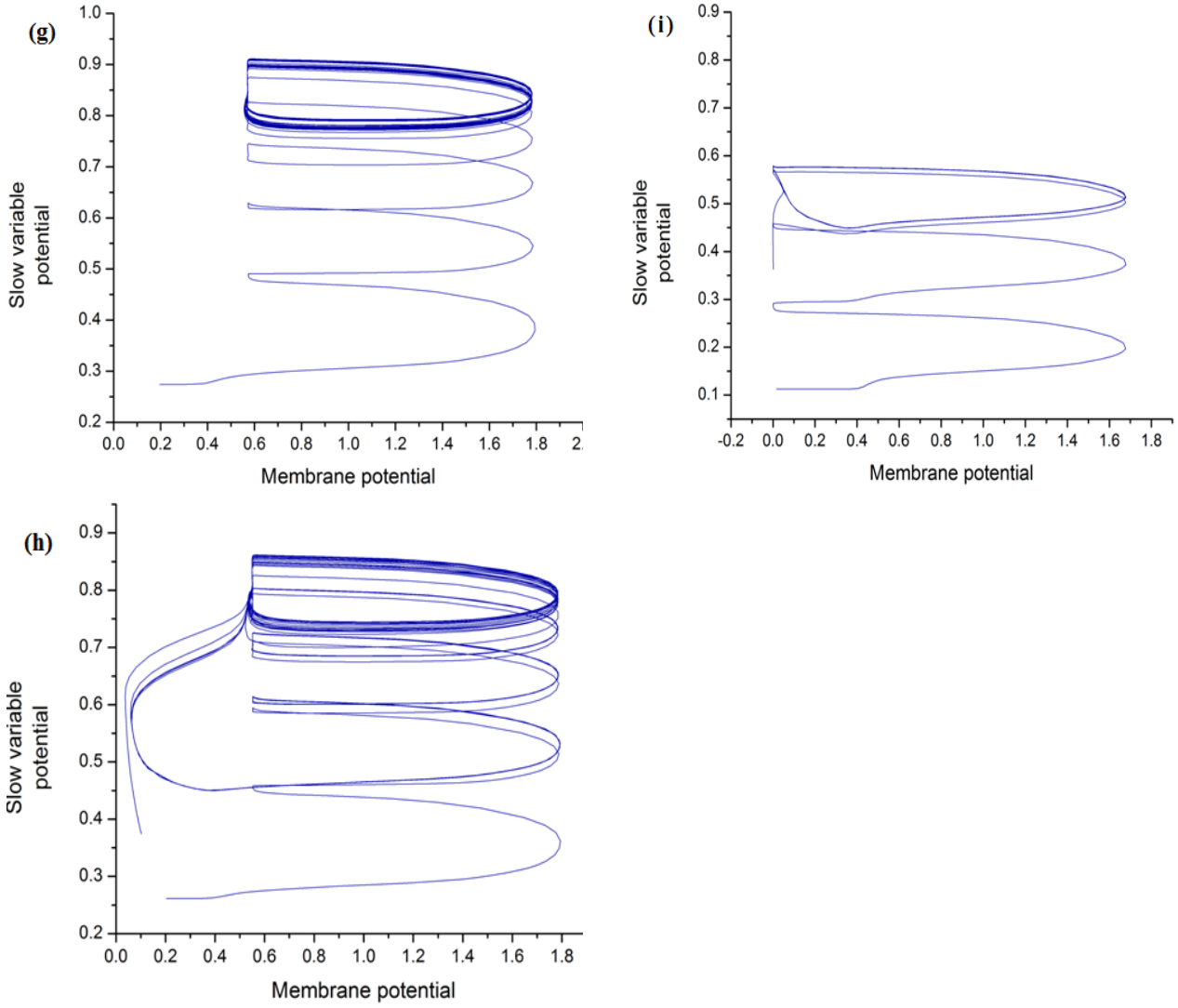


Fig. 3.7. State trajectories of the firing patterns of the cortical neuron: (a) CH1 (b) LTS (c) IB2 (d) IB1(e) FS3 (f) FS2 (g) FS1 (h) CH2 (i) RS2-1

3.6 Results and Discussions:

The circuit simulations are done in cadence design environment in 180nm technology. The neuron circuit simulated is shown in the Fig 3.8.

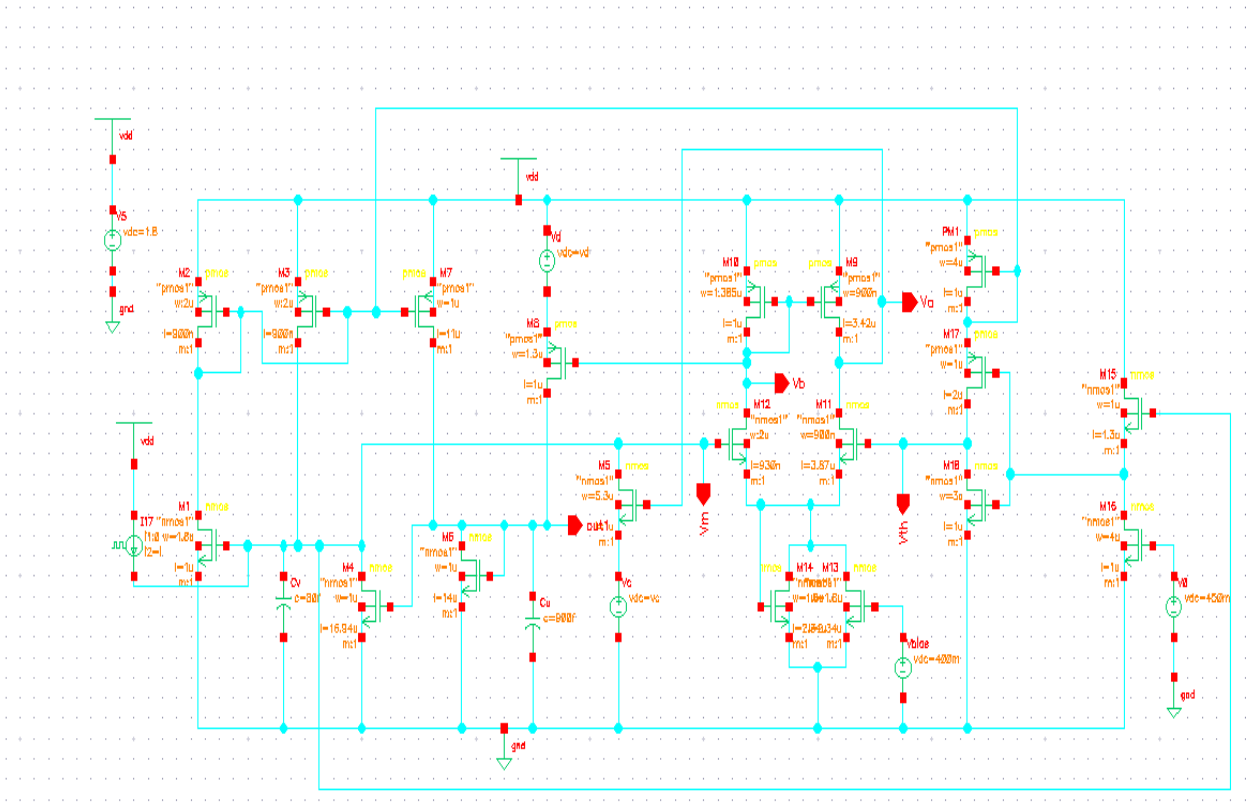


Fig. 3.8. Circuit diagram of the cortical neuron

The circuit consists of 19 transistors where there are 8 Pmos transistors and 11 Nmos transistors which comprise that the circuit is implemented in Cmos technology. The aspect ratios of the transistors used in the circuit for the simulations are given in the table 3 with V_{dd}=1.8V, V_{bias}= 0.4V, V_{sf}=0.45V, C_v=80fF, Cu =900fF.

Table no.3: Aspect ratios of the transistors used in the neuron circuit

Transistors	W(in µm)	L(in µm)
M1	1.8	1
M2	2	0.9
M3	2	0.9

M4	1	16.94
M5	5.3	1
M6	1	14
M7	1	11
M8	1.3	1
M9	0.9	3.42
M10	1.38	1
M11	0.9	3.97
M12	2	0.93
M13	1.8	2.34
M14	1.8	2.34
M15	1	1.3
M16	4	1
M17	1	2
M18	3	1
M19	4	1

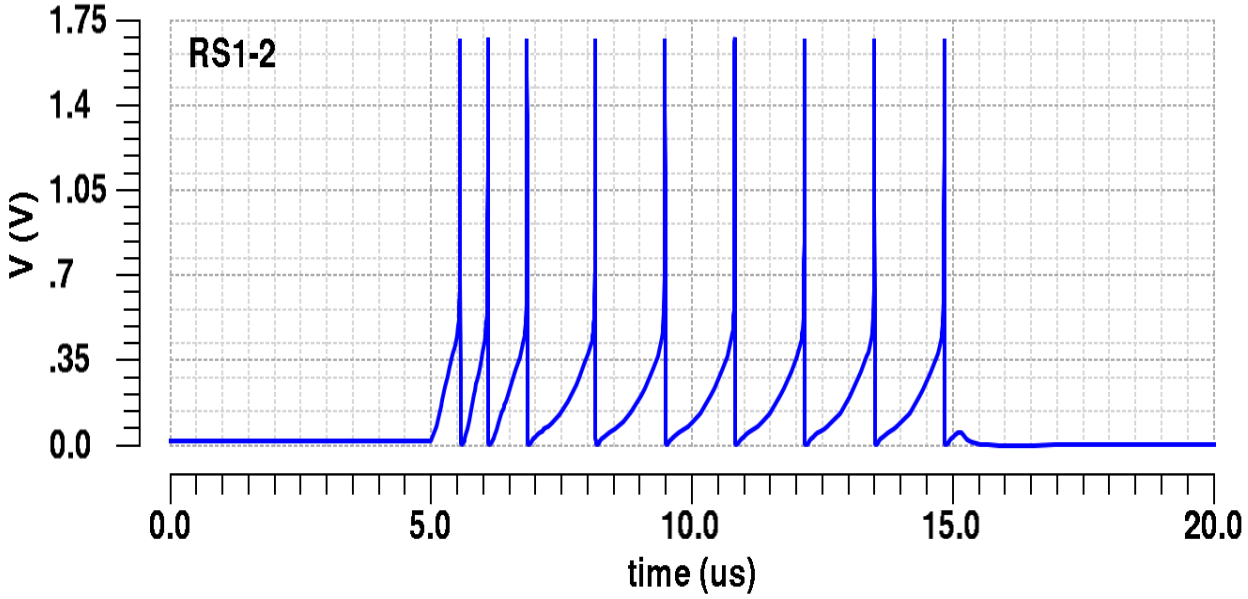
Various patterns of the cortical neuron are obtained by changing the tuning parameters V_c and V_d in the proposed circuit. Table 4 shows values at which different firing and spiking patterns are obtained.

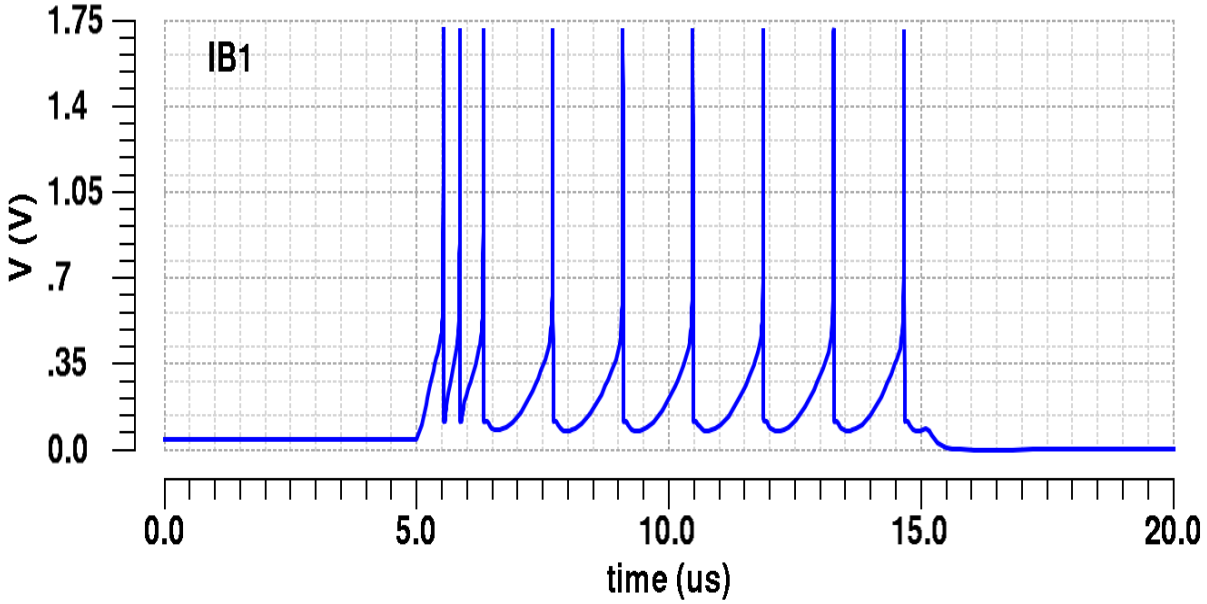
Table no.4: Tuning parameters to obtain different patterns

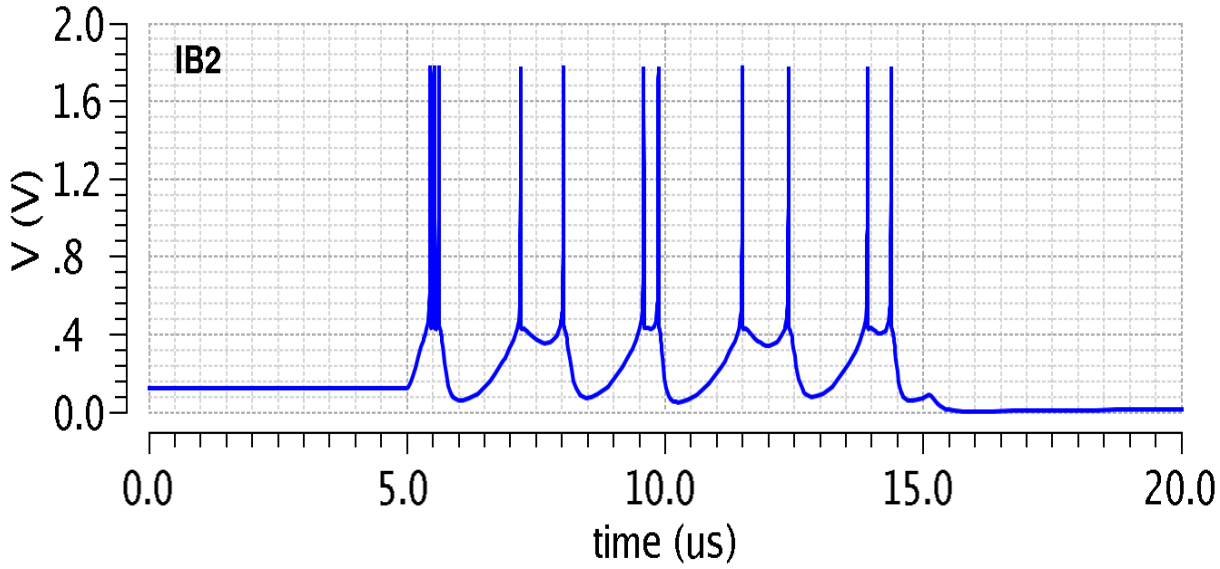
Spiking type	**V_c(in mv)**	**V_d(in mv)**
RS2-1	0	0
IB1	110	0
IB2	429	7
IB3	430	10
CH1	520	10
CH2	550	20
LTS	560	0
FS1	570	0

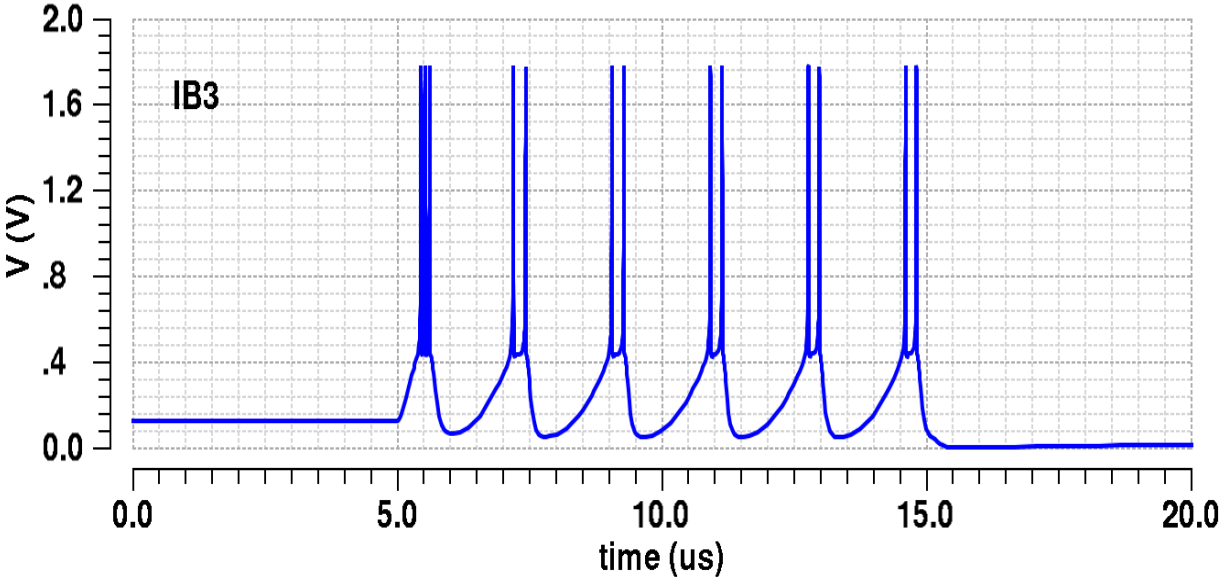
FS2	578	0
FS3	630	10

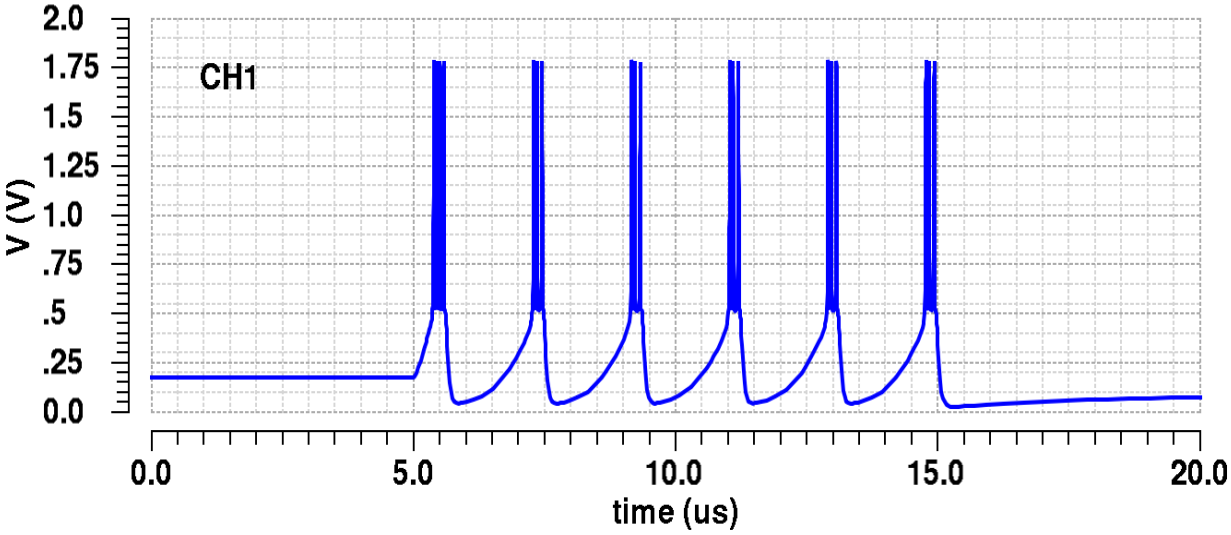
The results of different firing and spiking patterns in response to input stimulus 0.1µA are shown in the Fig 3.9. The spike accuracy and number of spikes can be increased by changing the aspect ratios of the transistors and also the ratio of membrane potential and slow variable capacitances.

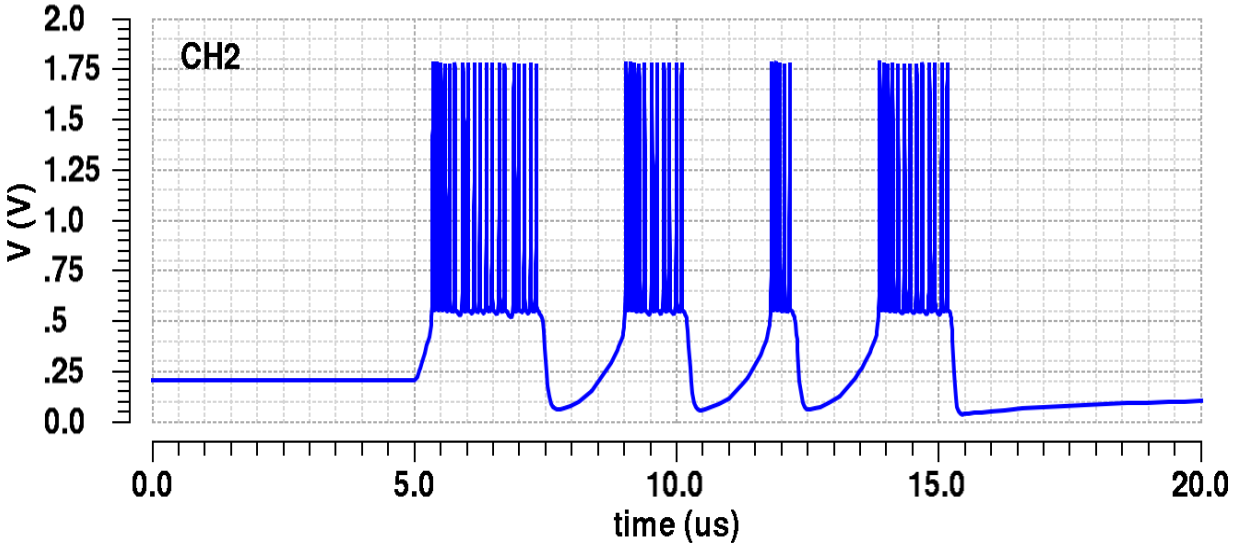


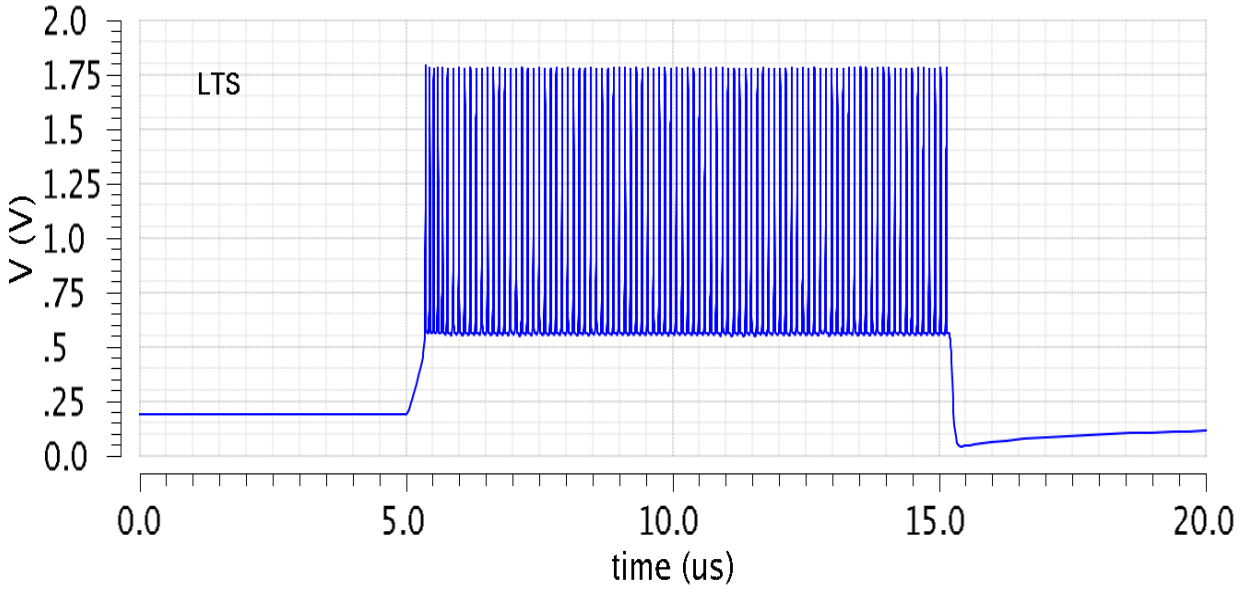


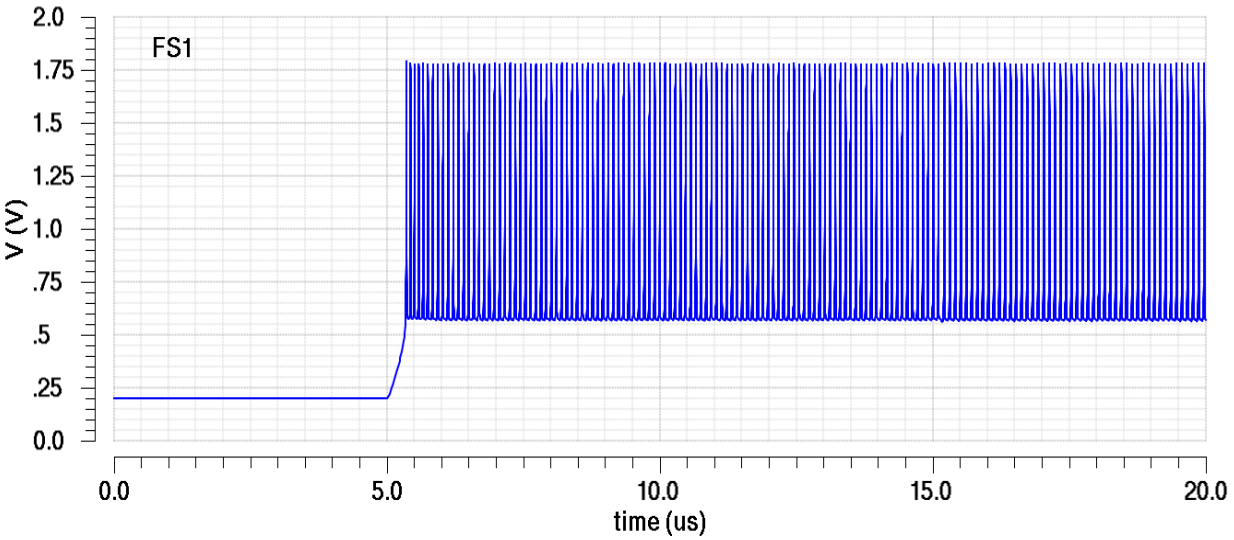

IB2
V (V)
2.0
1.6
1.2
.8
.4
0.0
0.0
5.0
10.0
15.0
20.0
time (us)


IB3
V (V)
2.0
1.6
1.2
.8
.4
0.0
0.0
5.0
10.0
15.0
20.0
time (us)


CH1
V (V)
2.0
1.75
1.5
1.25
1.0
.75
.5
.25
0.0
0.0
5.0
10.0
15.0
20.0
time (us)


CH2
V (V)
2.0
1.75
1.5
1.25
1.0
.75
.5
.25
0.0
0.0
5.0
10.0
15.0
20.0
time (us)


LTS
V (V)
2.0
1.75
1.5
1.25
1.0
.75
.5
.25
0.0
0.0
5.0
10.0
15.0
20.0
time (us)


FS1
V (V)
2.0
1.75
1.5
1.25
1.0
.75
.5
.25
0.0
0.0
5.0
10.0
15.0
20.0
time (us)

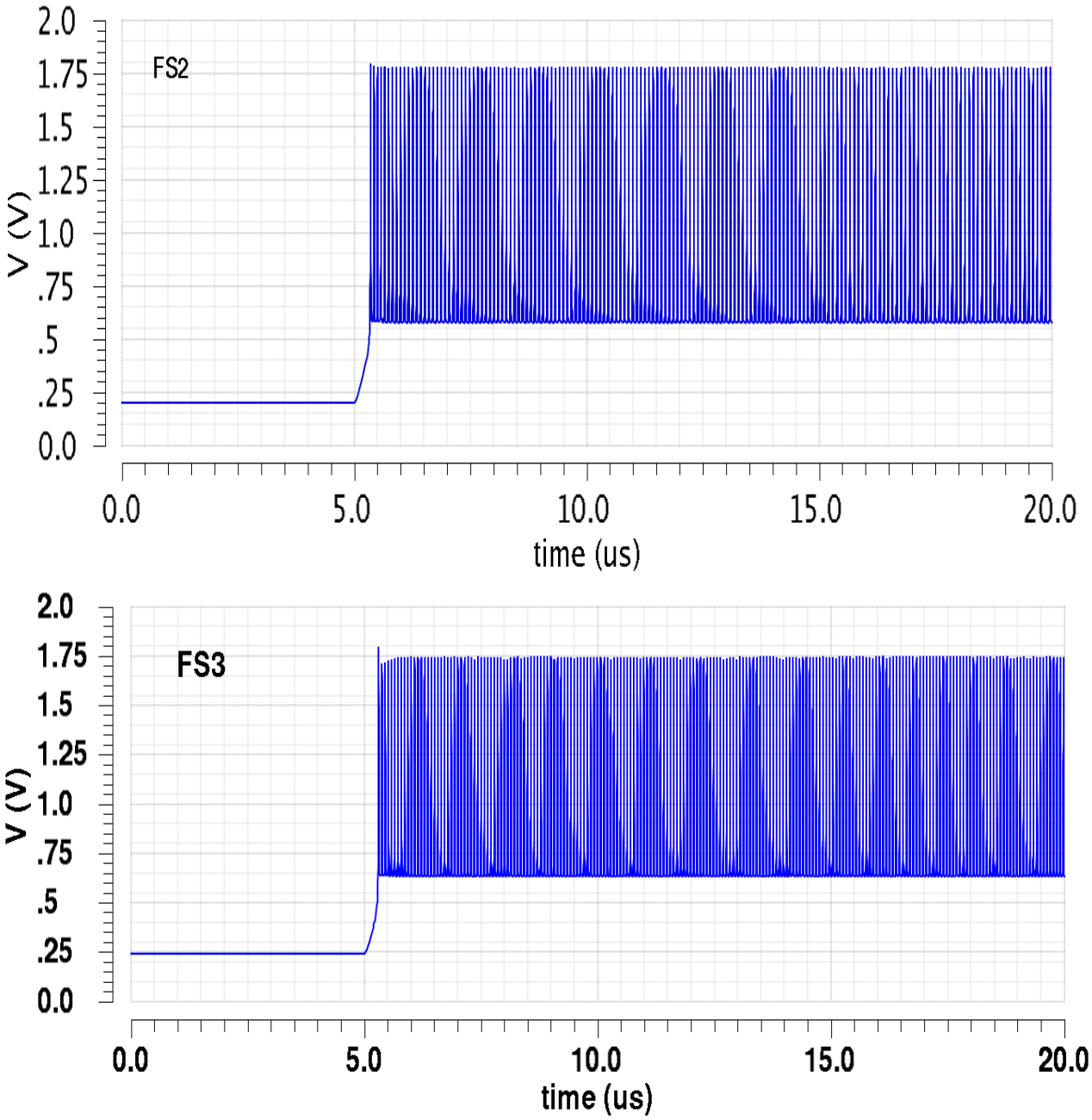
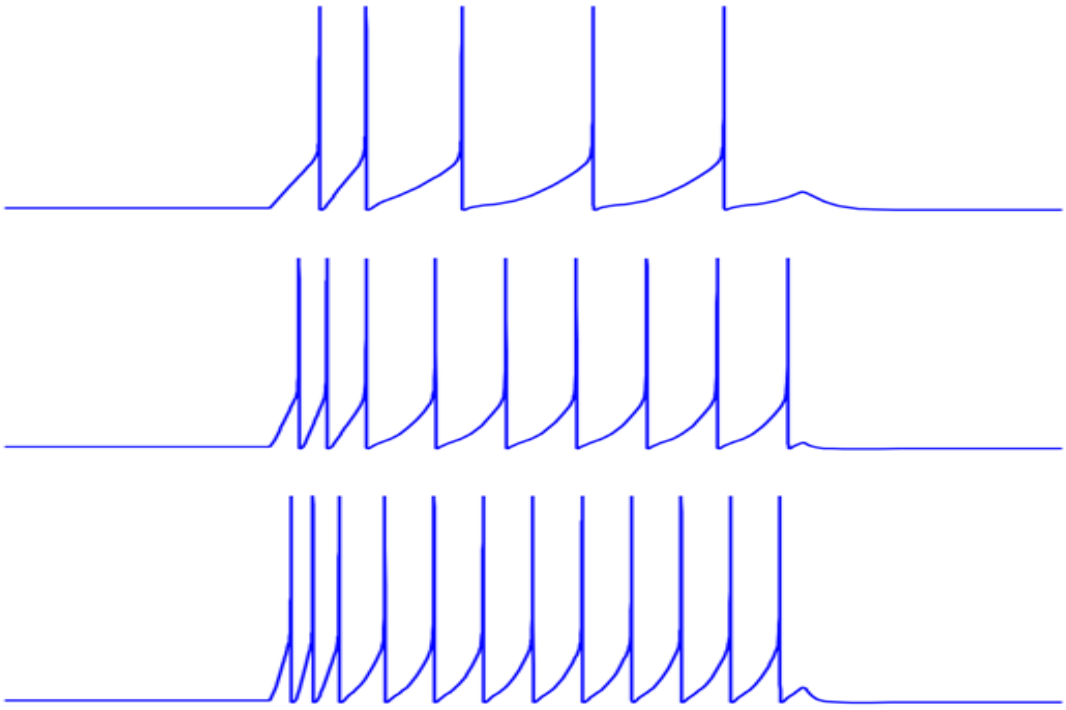
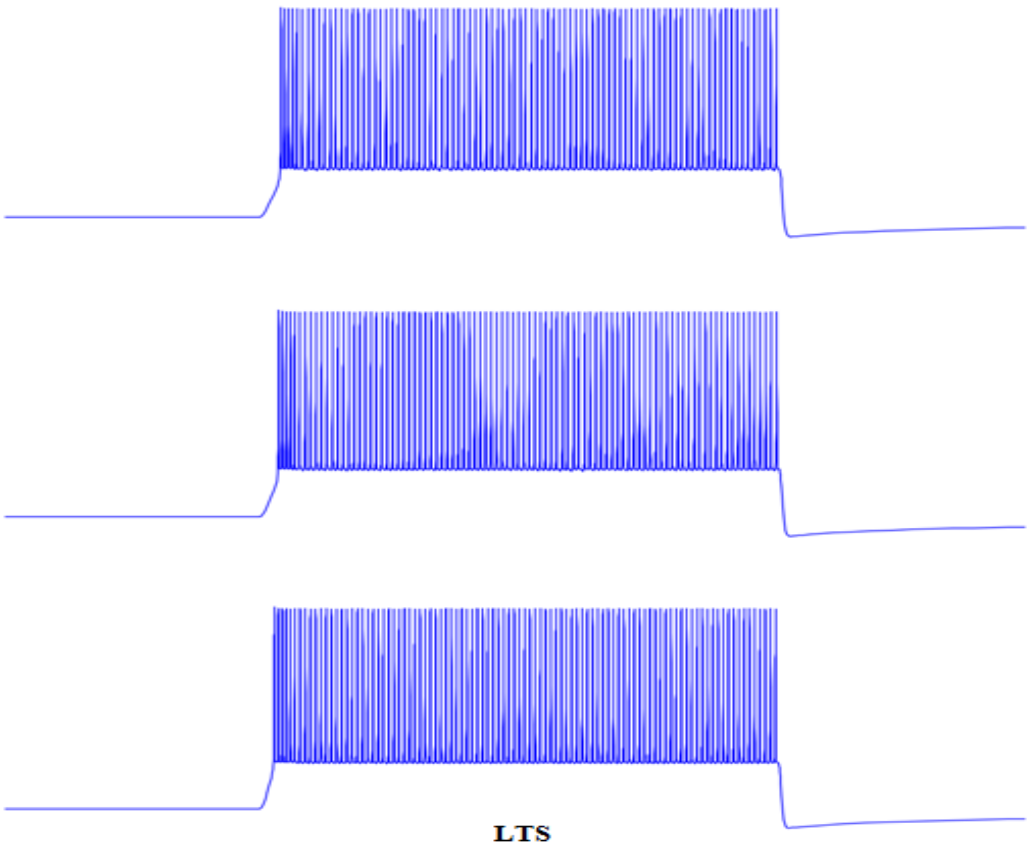


Fig. 3.9. Different firing and spiking responses of proposed circuit to 0.1µA input stimulus

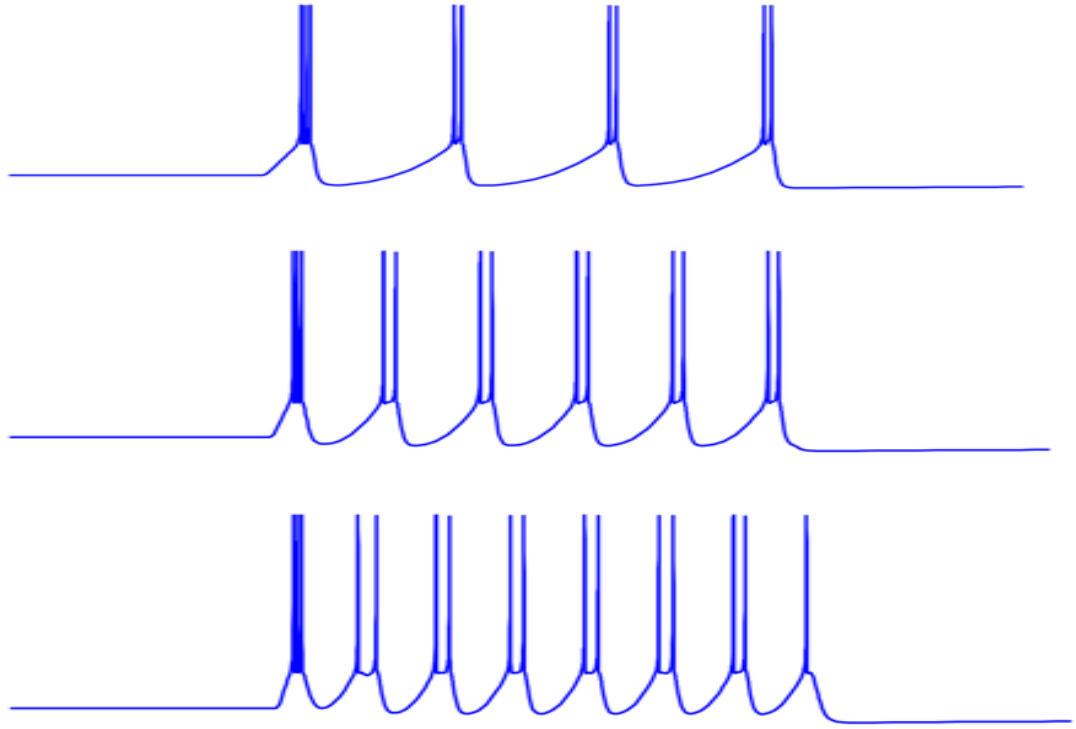
Fig 3.10 shows waveforms of different patterns in response to different input currents (50nA, 100nA, 150nA). These waveforms shows the sensitivity of the cortical neuron towards the input current applied. As input stimulus increases number of spike also increases mimicking the behavior of the real neuron in which as incoming synaptic inputs increases more spikes will be generated.



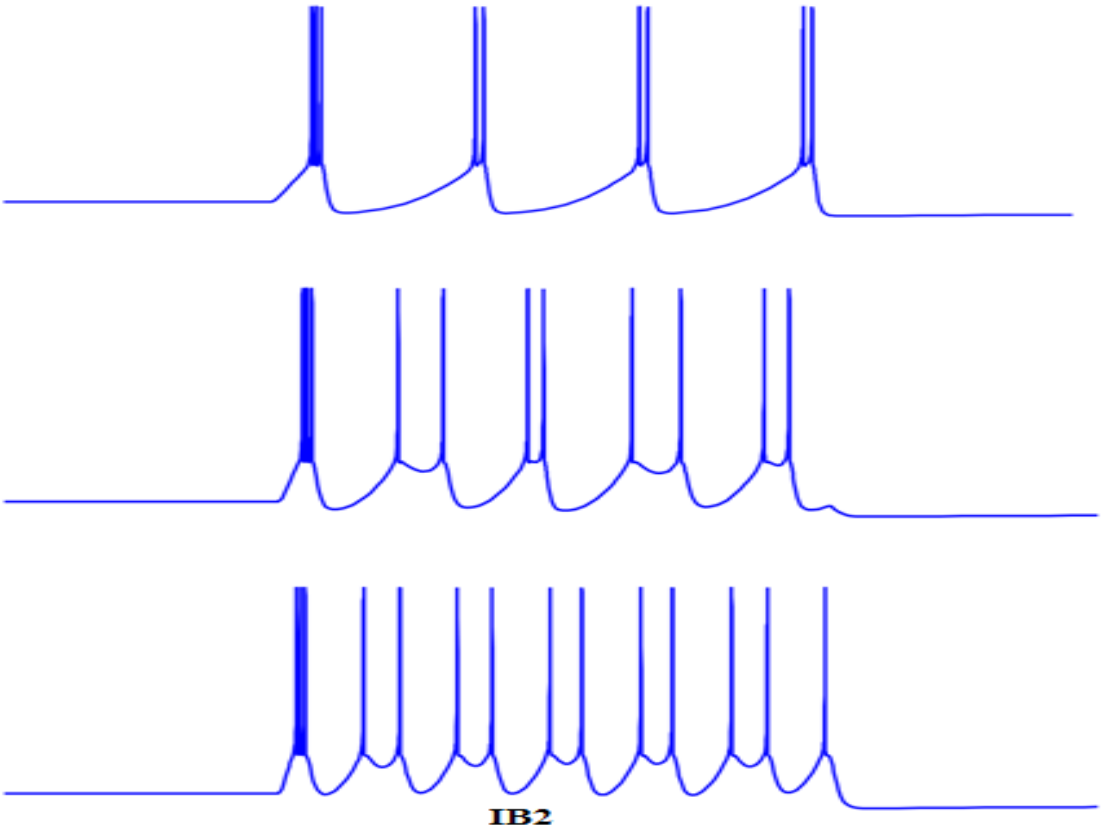
(a) RS 2-1



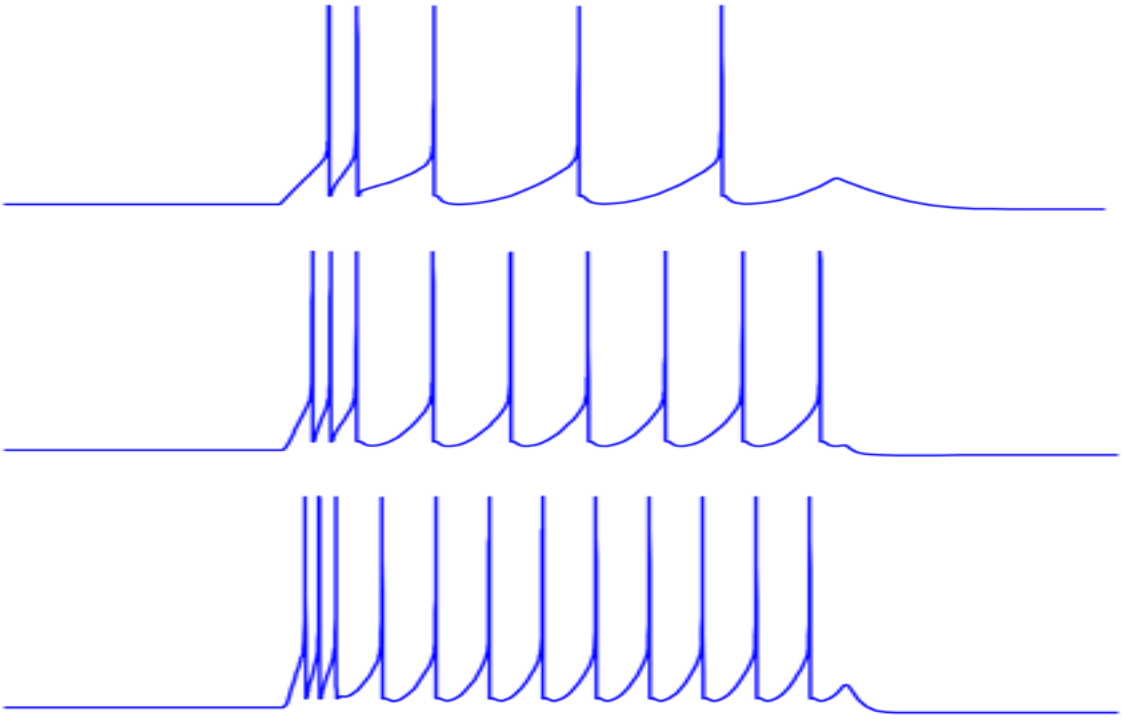
LTS



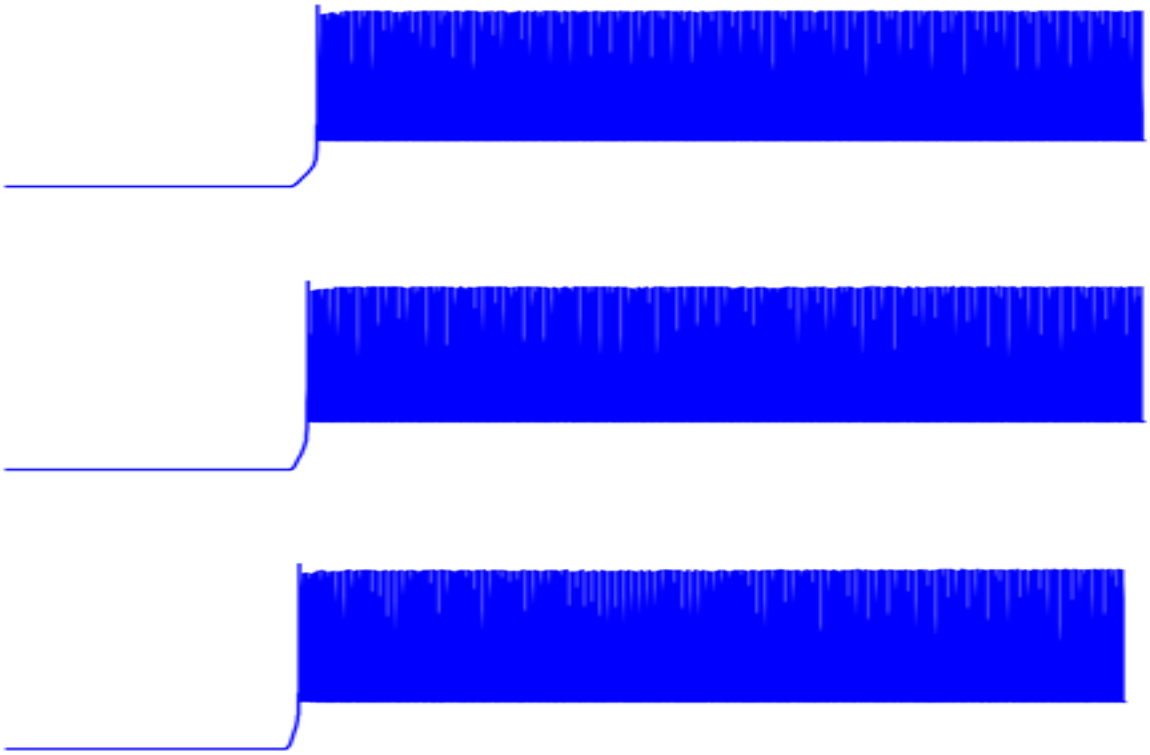
IB3



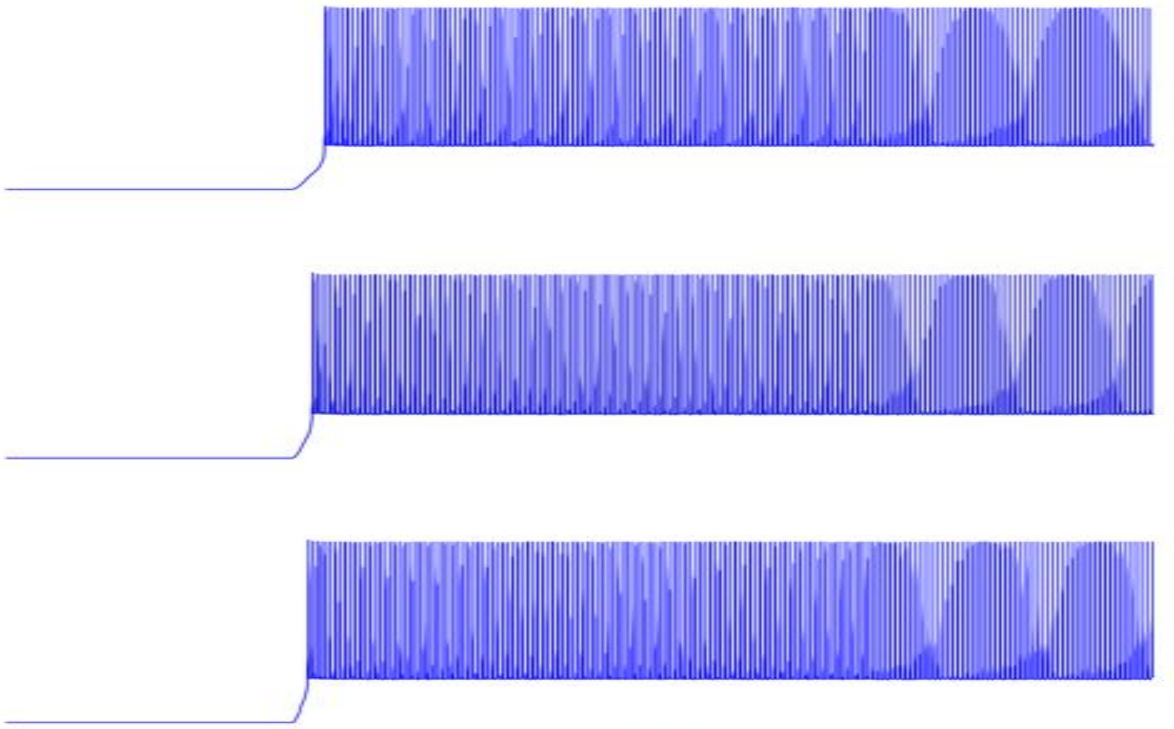
IB2



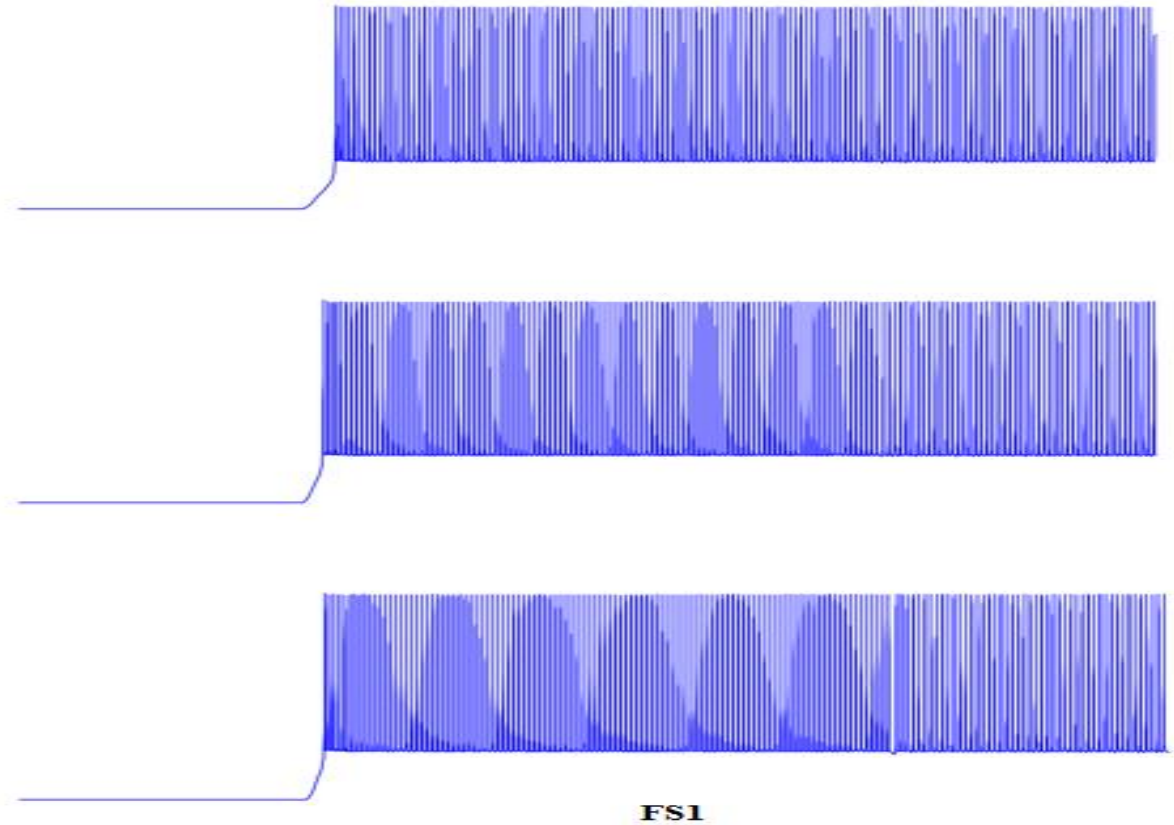
IB1



FS3



FS2



FS1

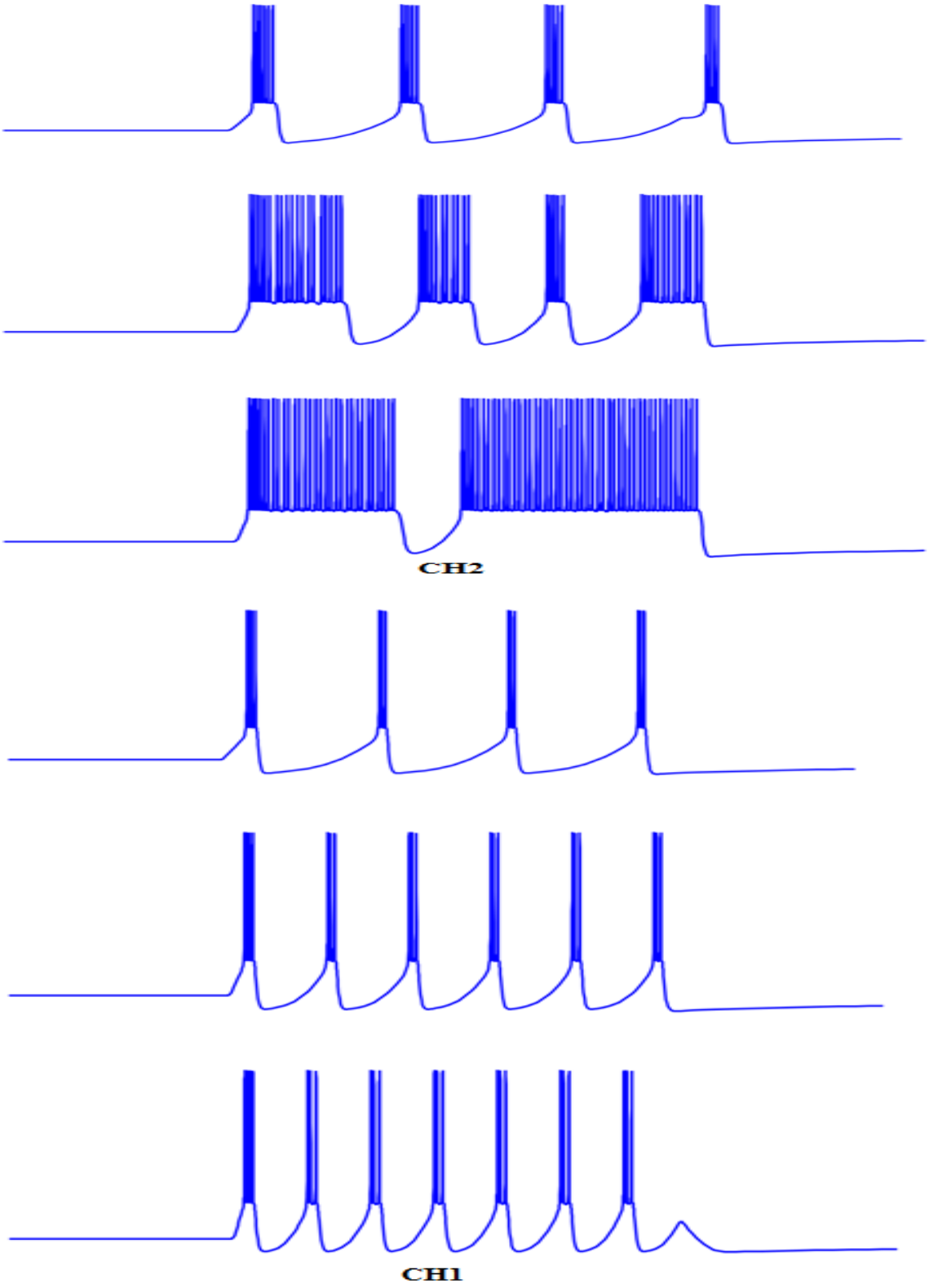


Fig. 3.10 Firing patterns in response to different input currents (50n, 100n, 150n)

Power consumed by each pattern is presented in the Fig 3.11. The plot shows that FS pattern consumes relatively more power while other patterns consume very low power. This is because of fast falling and rising rates of spike in FS and continuous firing even in the absence of input stimulus. Continuously firing without input can be compensated by applying inhibitory input.

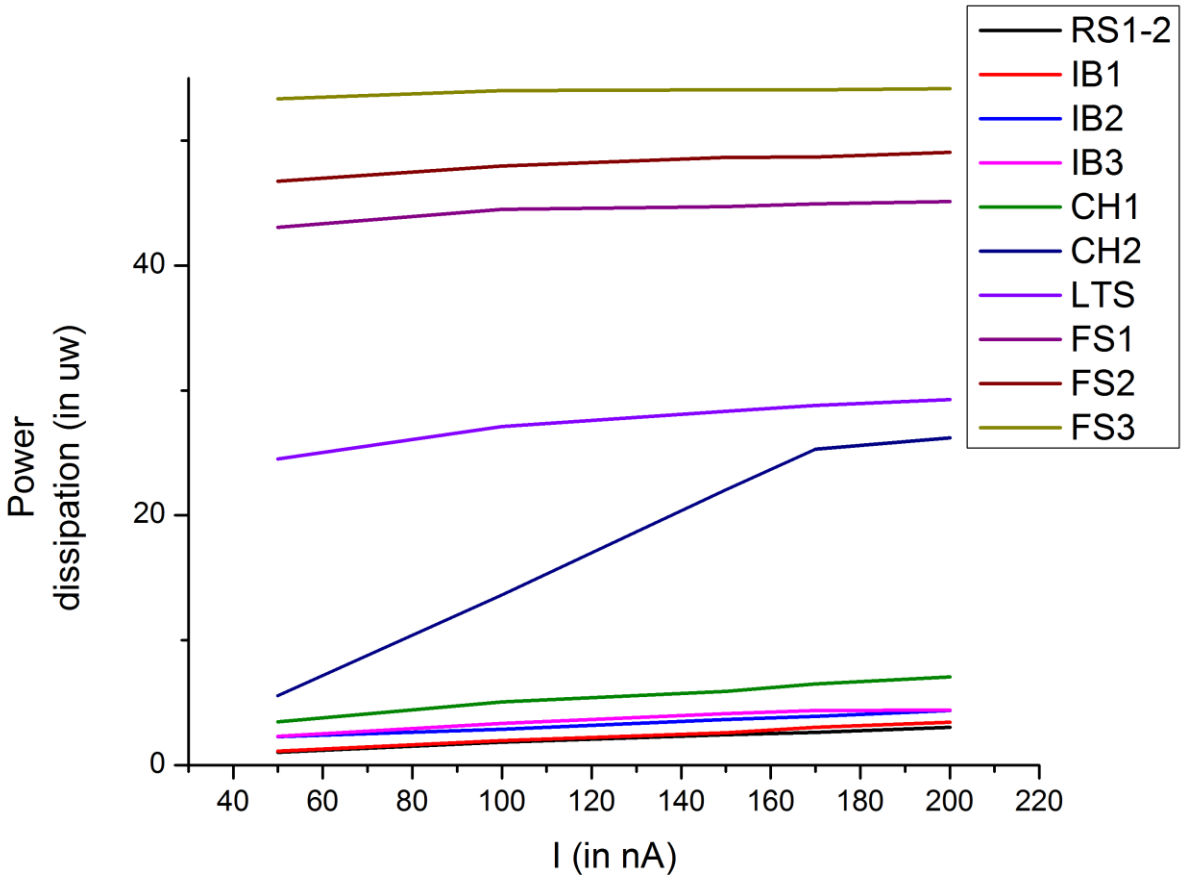


Fig. 3.11. Power dissipation of each pattern at different currents

Generally several neuron models like integrate and fire model, conductance based model, Izhikevich model have been used to design silicon neuron with constant threshold voltage. In these circuits when the spike crosses threshold voltage action potential will be generated. In the Fig 3.12 shown, the graph depicts that with constant threshold voltage it does not show any dynamic of the neuron regarding threshold modulation. Fig 3.13 shows membrane potential Vs threshold voltage graph in which threshold voltage variability is attained with membrane potential. This graph depicts the dynamics of the threshold modulation i.e., every

spike is generated with different threshold voltages rather than constant threshold voltage similar to the real neuron in which threshold voltage is not constant.

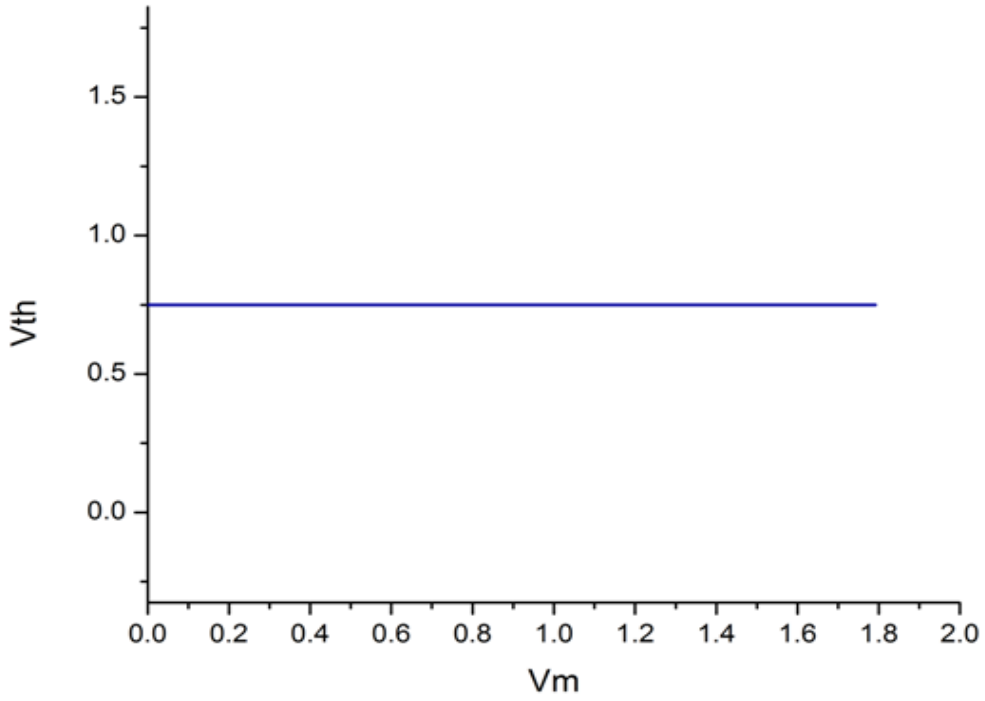


Fig 3.12 Dynamic with constant threshold voltage

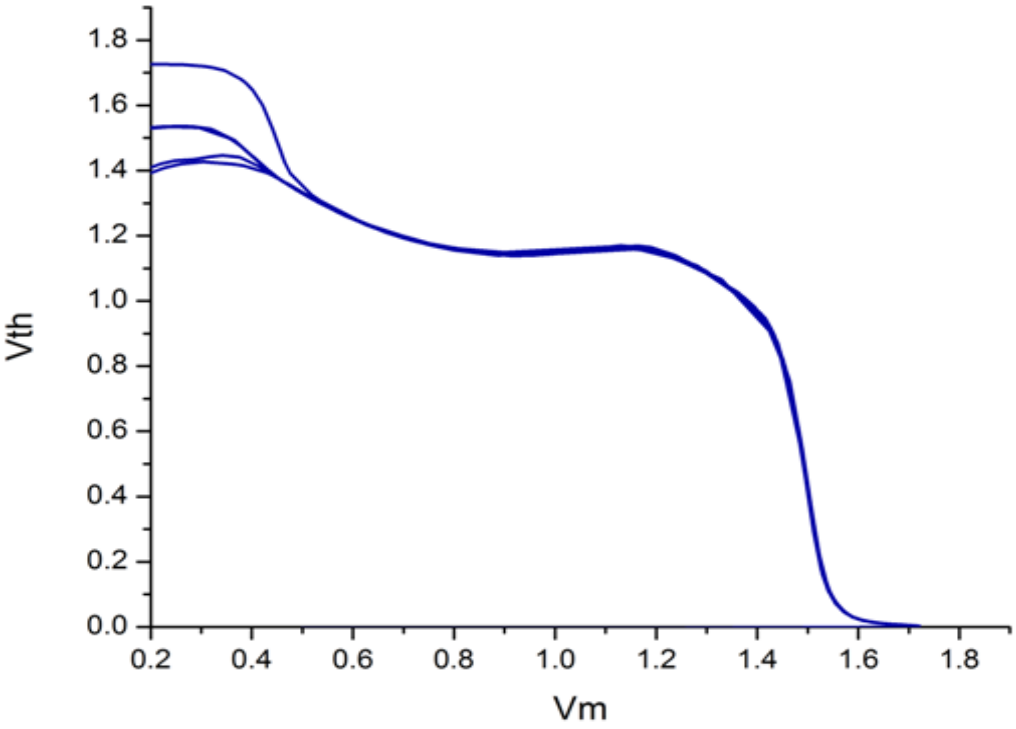


Fig 3.13 Dynamic with threshold modulation

Fig 3.14 shows the layout of the proposed circuit and it occupies less area, so a number of neurons can be fabricated on the same chip to emulate the cortical microcircuit.

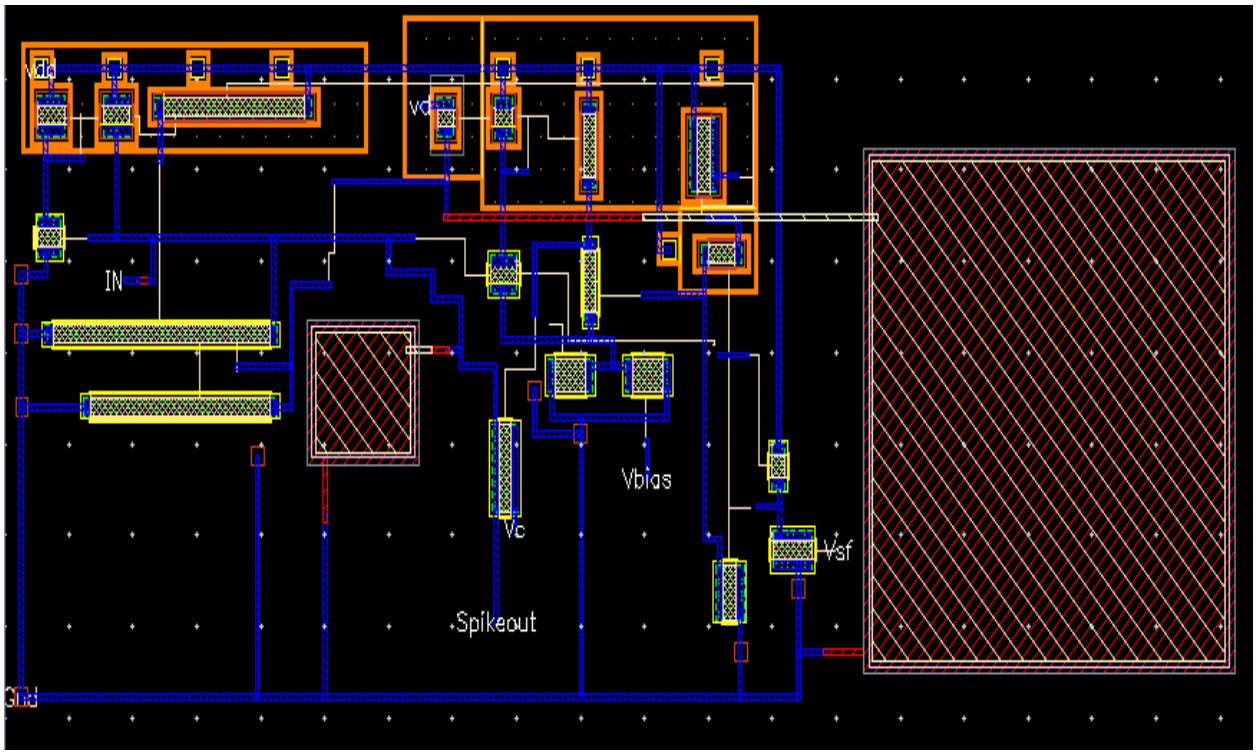


Fig 3.14 Layout of the proposed circuit

Table 5 shows the neurons designed with different models and comparisons between each model is also presented in the terms of number of transistors used in the model, spikes generated, degree of spike shape, threshold modulation etc. Integrate and fire neuron model proposed in exhibits threshold modulation but it is not capable of generating all patterns. Compact silicon neuron circuit proposed in produces all types of firing patterns but do not exhibit threshold modulation property. Circuit proposed in this paper is capable of producing all types of spiking with threshold modulation thus achieving the dynamic behavior of the real neuron.

Table no.5: Comparison of the proposed neuron circuit with other models

Neuron Model	No. of transistor used	Types of spiking(FS, RS, CH and IB)	Shape of spikes	Threshold Modulation	Power(µm)	References
Conductance-based	27-30+	Simple Spiking	Good	-	60	[12]
Integrate and fire	18-20	Simple Spiking	Fair	Yes	0.3-1.5	[6]
Fitz Hugh-Nagumo	21	Oscillatory spiking	Envelope	-	-	[10]
Morris-Lecar	22	Oscillatory spiking	Envelope	-	-	[18]
Resonate and Fire	20	Oscillatory spiking	Pulse	-	-	[17]
Hindmarsh - Rose	90	Bursting (CH)	Fair	-	163.4	[9]
Compact silicon neuron	14	All types	Good	-	8-40	[23]
Proposed Circuit	19	All types	Good	Yes	8-54	Proposed Circuit

3.7 Conclusions and future scope:

Cortical neuron is the main element of the neocortex that is reason for the complex processes that happens in the brain like signal or image processing, thought enabling, voluntary motor control etc. Building cortical networks leads to evolution of intelligent systems that learns by adapting to the outer environment. These cortical circuits comprises of cortical neuron which are connected with silicon synapses that provides connection between neurons on the same chip. In this work cortical silicon neuron is presented that consists of 19 transistors. Proposed circuit is capable of exhibiting the dynamics of real neuron such as spike frequency adaptation, after spike resetting mechanism along with threshold modulation. The circuit presented generates all types of firing, bursting and spiking patterns of the cortical neuron. The circuit is designed in cadence design environment and simulations are carried out in 0.18µm technology. The patterns are generated by tuning two voltages in the range of $0<V_c<0.63$ and $0<V_d<0.1$. The proposed circuit uses less number of transistors so, this can be used to integrate in large circuits of cortical microcircuits that emulate large cortical areas, as they occupy less area on the chip. The proposed circuit also consumes low power compared to other circuits so the circuit is energy efficient to use in building low power cortical microcircuits.

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