A

DISSERTATION-II REPORT

On

WIDE TUNING RANGE OF Gm-C FILTER USING BUTTERWORTH DESIGN

Submitted in the partial fulfilment of the requirement for the award of degree

Masters of Technology

In

VLSI

Submitted by

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DECLARATION

I hereby declare that the Dissertation-II report entitled "**WIDE TUNING RANGE OF Gm-C FILTER USING BUTTERWORTH DESIGN"**, is an authentic record of my own work carried out as the requirements for the award of degree of Master of Technology in VLSI Design at Lovely Professional University, Jalandhar under the guidance of **Mr. Sandeep Bansal**, Assistant Professor, Department of Electronics and Communication Engineering.

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It is certified that the above statement is correct to the best of my knowledge and belief.

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CERTIFICATE

This is to certify that **Kumar Rajmanyu** (11310656) has completed objective formulation of his Dissertation-II titled, "**Wide Tuning Range Of Gm-C Filter Using Butterworth Design**" under my guidance and supervision. To the best of my knowledge, the present work is the result of his original study and research. No part of this report has ever been submitted for any other degree at any University.

The dissertation is fine for the submission and fulfilment of the conditions for the award of degree Masters of Technology in VLSI.

(Project Supervisor)

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ACKNOWLEDGEMENT

"*Karmanye vadhikaraste, maa faleshu kadachana.*"

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Finally, the acknowledgment would become incomplete if I don't mention my entire family who are the eternal source of inspiration in my brightened carrier. In fact, I would like to dedicate this thesis work to my family and seek blessings from them forward in my life.

My acknowledgements would not be complete without expressing my gratitude towards Almighty God. I feel very fortunate to come to know Him during all these months of my life and have continually been blessed by His endless love ever since. He is the true shepherd of my life.

ABSTRACT

The need for wireless communication increases rapidly. Therefore, a low-power, high –speed and cost-effective RF circuit is always desirable in this scenario. Recent developments require high level of integration in the receiver side of the communication system as mobile and wireless communication is going to be labelled with multimedia systems. A high DC gain operational transconductor is presented here in this paper which will be effect fully used in the multi order butterworth Gm-C filter. Simulation results along with proof and further Future scopes to increase the gain is described in the paper. Active Gm-C filter of triode based MOS transistors are good candidates for low power consumption and high linearity. Linearity can be maintained by compensation technique and increasing the output impedance with examined sizes of transistors will yield us the desired result. Butterworth prototype is used for wide tuning range filters.

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CHAPTER 1

INTRODUCTION

1948 is the year from which the applicatory explanation of the electronics world is completely changed by the three giants of this field Mr John Bardeen, Mr William Shockley and Mr Walter Brattain when they discovered the very first TRANSISTOR in the laboratory of BELL. The charge sharing or flowing between three different regions of a doped semiconductor has created the never ending opportunity and optimism in almost the every branch of electronics and semiconductor-device physics and all the colours of a luxurious life in present scenario is actually by the grace of that event occurred in 1948. Technically, invention of transistor leads the possibility of existence of VLSI (very large scale integration) in 21st century. In fact, today we are in the evolution process into the ULSI (ultra large scale integration) world which is more complex and integrated than VLSI.

Table 1.1: Evolution of VLSI

VLSI System Evolution

1. Transistors	1950s
2. Integrated circuits	1960s
3. Micro-processors	1970s
4. Digital signal-processors	1980s
5. FPGAs/ASICs	1990s
6. System-on-chip (SOC)	2000s

As we all know transistors are placed on a silicon wafer or plate with interconnections between them which named the system as an INTEGRATED CHIP. With the need of the fast growing technology, the numbers of transistors also increase on the same chip area. Various sustainable techniques are imposed to allow the placement and floor-planning of increasing numbers of transistors. According to

MOORE's LAW, the numbers of transistors almost double in 18-24 months for same area of silicon chip.

Table 1.2: No. of transistors with techniques

Small scale integration (SSI)	Few 10s of transistors	Early 1960s
Medium scale integration	Few 100s of transistors	Late 1960s
Large scale integration	Tens of thousands of Transistors	Mid 1970s
Very large scale integration	Hundreds of thousands of Transistors	Early 1980s
Ultra large scale integration	1 million transistors	Early 2010s

With a drastic increase in transistors in a system-on-chip or integrated chip, the device enlarges its applicallity in the various fields of technology and modern science. Home appliances, automobile industry, multimedia world, effective scientific computation, industrialization, robotics, signal processing, embedded world, nano-technology, defence industry are some of the areas where VLSI chips has become as important as oxygen for the mankind. Among all these application fields, communication field catches larger attention of my consciousness as without communication the universe will be so isolated within itself that I could not have been able to disclose my research work with anybody if I would have not been blessed with some mode of communication.

It will be not an unexpected terminology if I term the 21^{st} century is the century of communication. The world is heavily dependent upon the best quality of communication, can be employed. The vocabulary of 21^{st} century's communication is not just confined within the mere range of sending and receiving of texts only; rather it is expanded even beyond the scope of MP_3s, MP_4s and compressed data with the eye-blinking speed from one end of the world to the another far-end. To accommodate this vast communication, we use the medium of Bluetooth, CDMA, wireless, IEEE a/b/g/n LAN, Wi-Fi, cloud-storage, infra-red etc. The bandwidth and

tuning range associated with the communication medium defines the productivity of that medium.

Success of the communication is heavily dependent upon the transceiver used in the communication circuitry as the parameters such as bandwidth and tuning range is directly associated with the filter present in the transceiver which is the most important member in the family of transceiver. Usually low-pass filters are used in the transceivers which can be replaced by band-pass filters for some special operations like ASICs.

1.1 SCOPE OF THE STUDY

The advent of the technology is direct proportional to the demand of the consumers. And, it will be hilarious to explain the necessity smaller size (portable), fast working, multimode application features for an electronic device. And, of course there is always zeal of competitiveness between the vendors or manufacturers of the electronic field. Therefore, the level of integration is increased in RF transceivers for a better communication process. Therefore, C-MOS emerges as the best technology for cost effectiveness, simpler design process, smaller area consumption, lesser power consumption, lesser power dissipation and minimum delay because RF, mixed signal and digital circuits are generally integrated on a single system-on-chip (SOC). For example; mobile computing, multimedia systems etc.

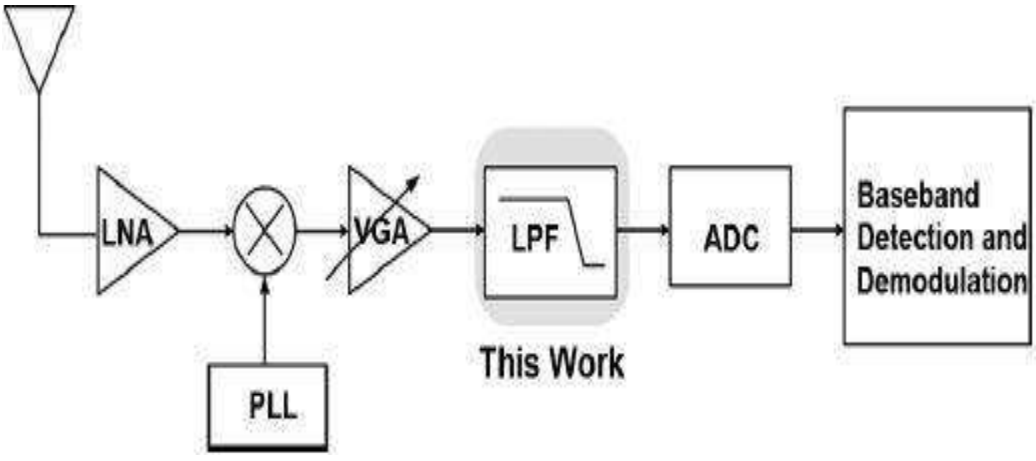

Fig 1.1: Architecture of Transceiver

Recently direct-conversion receivers are most preferred for analog-signal processing because of their highest capability of achieving integration on their own system and also for easiness of their system design [1].

The key architecture within the receiver, which must be conceived as transceiver throughout this article is the "Channel Selection Filter" present in the system. Receiver converts the RF signal to baseband signal (wanted or unwanted signal both). Then the objective of the channel selection filter is to filter-in the desired signal from the baseband signal which is termed as DEMODULATION.

"An ideal filter not only rejects the unwanted signal from the desired one but also has the same and stable response for all desired signals."

To achieve an ideal filter as close as possible an array or stack of filters can be applied in the channel selection filter. But definitely this out-dated method will consume more power and silicon space which is always undesirable. The best way to go is a single filtered channel selection module which can perform or will be able to meet the requirements of a multi-mode application. Conventionally, filters were mostly RC type. They were composed of resistors and capacitors which are likely to be dumped as resistors and capacitors alone can never achieve the multi-mode requirements and if so, they will consume a huge silicon area on the chip and power to be operated which can be acceptable in present scenario where we concern about speed, area and performance.

Therefore, use of MOSFETs are considered as the best suited technology and my research further discovers that the configuration of Gm-C filter in BUTTERWORTH PROTOTYPE using different modes of MOSFETs will be able to address the issue with best possible manner in terms of low power, low cost, lesser area and high linearity and high stability.

1.2 OBJECTIVE OF THE STUDY

This research work coincides with research already done by Dr Mohammed Ismail, professor of Electrical and Computer Engineering and Founding Director of Analog VLSI Lab at Ohio State University and his team on Gm-C filter in analog signal processing. Objective of this research work is to improve the quality of mentioned filter with respect to various parameters of a filter such as power consumption, area, cut-off frequency, linearity and applied technology etc.

1.2.1 System Parameter Analysis

1.2.1.1 Parameter Analysis In 1997

Table 1.3: Work done in 1997

Used Gm-C filter	Fifth order
Cut-off frequency	280 KHz – 405 KHz
Out-put	700 m V_{PP}
Harmonic distortion	1 %
Power dissipation	2.8 mW
Area	1.62 mm^2
Supply voltage	3 v

Technology	1.2 µm

1.2.1.2 Parameter Analysis In 1999

Used Gm-C filter	Fourth order
Cut-off frequency	Up to 200 KHz
Distortion	Negligible
Supply voltage	2.7 v
CMRR	70 dB

Table 1.4: work done in 1999

1.2.1.3 Parameter Analysis In 2003

Used Gm-C filter	Third order
Cut-off frequency	15 KHz – 85 KHz
Power dissipation	240 mW
Harmonic distortion	1 %
Supply voltage	1.2 v
Technology	1.8 µm

Table1.5: work done in 2003

1.2.1.4 Parameter Analysis In 2005

Used Gm-C filter	Two active fourth order
Area	0.9 mm^2
Power consumption	3.4 mW(UMTS) 14.2 mW(WLAN)
Technology	0.13 µm

Table1.6: work done in 2005

1.2.1.5 Parameter Analysis In 2005

Used Gm-C filter	Third order
Cut-off frequency	50 KHz – 2.2 MHz
Area	0.5 mm^2
Power consumption	7.3 mW
Technology	0.25 µm SiGe Bi-CMOS

Table 1.7: work done in 2005

1.2.1.6 Parameter Analysis In 2006

Used Gm-C filter	Fourth order
Area	0.9 mm^2
Power consumption	3.4 mW(UMTS) and 11.42 mW(WLAN)
Technology	0.13 µm

Table 1.8: Work done in 2006

The circuits presented below in subsequent chapters along with its simulation result are the optimized study for the tables mentioned above. This solution circuit was experimentally produced by Dr Mohammed Ismail and his team in the year of 2009. Further, my approach is to create a more suitable circuit to be utilized in a new Gm-C filter in accordance with some relevant techniques which are evolved during a vast Literature Review.

CHAPTER 2

TERMINOLOGY AND LITERATURE REVIEW

The introductory part of this dissertation paper clearly describes its objectives towards achieving an optimized point between the various performance-parameters associated with a circuit consisting of several transistors. Therefore, success of this research is very much relying upon understanding those parameters accurately. Obviously, the first step of the literature review goes through defining the basic operational concepts of a transistor (BJT or MOSFET).

2.1 Power Dissipation and Consumption

Except nuclear sources everything on earth stockpiles energy from the sun. In fact, the earth is a huge battery that has been charged up for billions of years by the sun. The dissipated energy is stored in the plants, and then it turns into carbons and then oils, oils transferred into heats and then electricity. Finally, electricity is converted into chemical energy or any other form of energy or stored in the battery. Now-a-days, we are getting energy directly from sun via solar systems or wind or hydro systems. If to summarize the importance of the last conversation technically, we have to state that as the power is defined as the rate of energy transfer, „power dissipation" is a measure of the rate at which energy is dissipated or lost from a system [7]. When an electric current works on a circuit, the internal energy of that particular circuit increases. There is also increase in temperature of the circuit beyond the ambient or surrounding temperature. Like water, energy also flows from high end to lower end and this causes energy to dissipate from the circuit to the atmosphere in the form of heat transfer. The rate of this heat transfer (joules per second) is termed as "power dissipation" (in watts).

The instantaneous power P (t) consumed or supplied by a circuit element is the product of the current through the element and the voltage across the element.

$$P(t) = I(t).\ V(t) \qquad (2.1) \qquad [7]$$

The energy consumed or supplied over some time period is the integral of the instantaneous power

$$E = \int^{T} p\,(t).\ d\,(t)$$

(2.2)

Average power:

$$P_{avg} = E/T = 1/T\ = \int^{T} p\,(t)\,d\,(t)$$

(2.3)

2.2 Cut-off Frequency

The actual concern in this research work is for designing a filter. Filters are categorized as low-pass filter, high-pass filter and band-pass filter. The identity of a filter is solely dependent upon the frequency range it is operating on. The allowable frequency range through a particular filter is termed as the cut-off frequency of that filter. An ideal filter has 100% acceptance to the frequencies under its cut-off range and 100% rigidness or 0% acceptance to the frequencies beyond the cut-off range. More the cut-off range more is the operational value of the filter [8].

2.3 Area

Size really matters in today's populous world. When the population is exploding with the constant resources available, the objective is to utilize minimum amount of resources for producing same application. Integrated chips are designed on the silicon wafer or body generally. Silicon is not an immortal material on the earth. Therefore, using lesser silicon area as possible for IC designing will solve our problem up to certain extent.

2.4 Technology

Meaning of technology in C-MOS processes is quite different what it means in other general fields. There are two types of transistors present in electronics such as BJT (bipolar junction transistor) and MOSFET (metal oxide semiconductor field effect transistor). The recent market is turned on to the MOSFET because of its cost effectiveness and ease of manufacturing though current conduction property is more reliable in BJT which is now used in some special operations only. The architecture of MOSFET is divided as gate, source, drain, and body and at last but not the least "channel". The length of the channel defined the technology used in designing the circuit or fabricating the IC. The most advanced technology has reached up to the technology of 0.014 µm process. But, this research is done by using the 0.18 µm process because of the non-availability of desired technology.

2.5 Stability

The designer must be able to the response of its designed circuit after giving some input. If this is possible, the system is stable; otherwise the system is unstable. An unstable system always oscillates between different possible output responses. The stability problem is a frequent problem in case of feed-back systems or sequential systems.

2.6 Linearity

A linear circuit is an electronic circuit in which for a sinusoidal input voltage with frequency, "f", any steady state output of the circuits will also be sinusoidal with same frequency, "f". But the output needs not to be in phase with the input. A linear circuit always obeys the Superposition Principle.

$$F(x) = ax_1(t) + bx_2(t) \tag{2.4}$$

Linearity increases with increase in the gain of the circuit. In feedback systems, linearity is the most essential parameter to be considered for the system designers [7].

2.7 Gain

In every aspect of life, this word, “gain” carries a very high preference amongst almost every individual. Electronically, “gain” is denoted as “A_V” and is associated with every circuit. Generally we talk much about “gain“ when there is a scope for amplifier.

Amplifier amplifies anything supplied to its input side (current or voltage). Gain for a circuit can be defined as the amount of output it produces with respect to the input fed to its supply side. Obviously, everyone will be interested for more output magnitude than the input; that means a positive gain. Typically, a general amplifier has a gain factor of about 10^1 to 10^5. That means if we provide 1 V to the input of an amplifier, it will give us a minimum output of 100 V; but still there is other factors are associated with amplifier which we have mentioned earlier in this chapter.

2.8 Input Output Swing

Suppose a high quality microphone is receiving audio signals from an orchestra group and amplification is done at the speaker to the audience. There are different instruments playing in the orchestra having variety of bandwidths. If the system is able to cope with all these bandwidths with minimum of noise produced then the system has high input as well as output swing. But again, large swing can make a space for low-stability and non-linearity [8].

2.9 Total Harmonic Distortion

Total harmonic distortion is a complex and often confusing concept to understand. However, when looking down into the basic definitions of harmonics and distortion, it becomes easier to understand. Imagine a power system with an AC source and an electrical load.

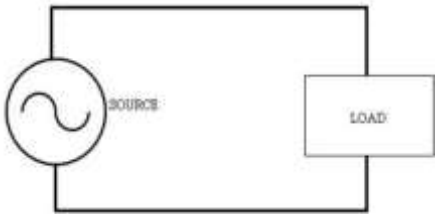

Fig 2.1: Power source

Now suppose that this load takes on one of two basic types; linear or nonlinear. The type of load is going to affect the power quality of the system. This is due to the current draw of each type of load. Linear loads draw current that is sinusoidal in nature so they generally do not distort the waveform shown below. Most household appliances are categorized as linear loads. Non-linear loads can draw current that is not perfectly sinusoidal and the waveform is also shown below. Since the current waveform deviates from a sine wave, voltage waveform distortions are created.

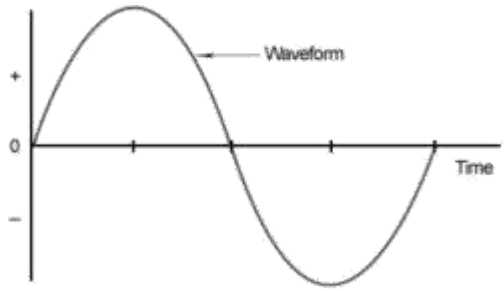

Fig 2.2: Ideal sine wave

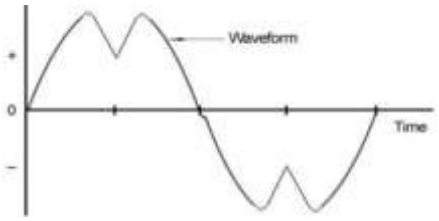

Fig 2.3: Distorted sine wave

As can be observed from the waveform distortions can drastically alter the shape of the sinusoid. However, no matter the level of complexity of the fundamental wave, it is actually just a composite of multiple waveforms called harmonics. Harmonics have frequencies that are integer multiples of the waveform's fundamental frequency. For example, given a 60Hz fundamental waveform, the 2nd, 3rd, 4th and 5_{th} harmonic components will be at 120Hz, 180Hz, 240Hz and 300Hz respectively. Thus, harmonic distortion is the degree to which a waveform deviates from its pure sinusoidal form because of the composite presence of all these harmonic elements. In ideal sine wave, there is no harmonic component and no one is present to distort the original wave form. THD is the summation of all the harmonic components present

in the wave compared to the original, non-distorted wave and mathematically defined as:

$$THD = (V_2^2+V_3^2+V_4^2+\ldots\ldots+V_n^2)^{1/2} / V_1 * 100\% \qquad (2.5)$$

All these parameters mentioned above are in tight trade-off with each other which makes the design of an electronic circuit (analog/digital/mixed), an optimization problem of multi-dimension. The careful study of the circuit and experience reaches us to allowable sacrifice of various parameters keeping in mind of the application area of the circuit. The recent trade of getting smaller size and lesser supply voltage makes this optimization even tighter.

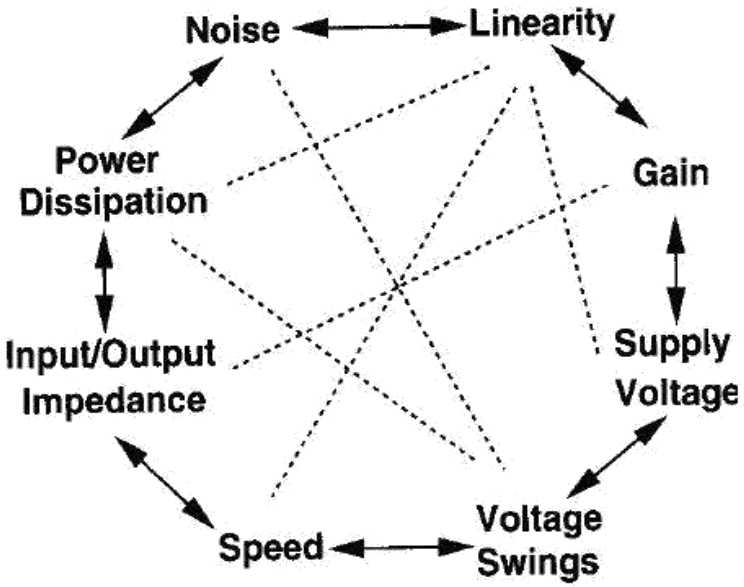

Fig 2.4: Octagon of optimization [4]

2.10 MOSFET [Structure and Operation]

The basic building block of CMOS circuit, according to this study is a MOSFET generally. Though we all are very much familiar with structural and operational basics of MOSFET, for the sake of beginners some elementary concepts are discussed below. Firstly, there are two types of MOSFET are present; NMOS and PMOS.

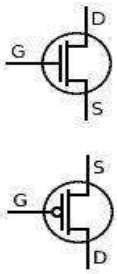

Fig 2.5: symbols for NMOS and PMOS

There are four sides of a MOSFET; gate, drain, source and body: out of which "body" terminal are generally not shown in common practices. Current conduction between drain and source occurs because of the voltage applied at the "gate" terminal. Therefore, this device is a voltage controlled current conducting device.

There is another most important parameter or value is attached with every transistor called "threshold voltage" (V_T). If the value of V_{GS} exceeds the value of "V_T", a channel is created under the gate connecting drain and source. If holes are moving via the channel; that means source and drain are of p-type and body is n-type, then the device is called as PMOS. Similarly NMOS devices have exactly opposite conditions. The channel is always in the reversed doping of the body and hence called as the "inverting channel". Generally V_T is positive for a device and we have to apply some positive bias at the gate terminal to run the device. These types of devices are called enhancement-type or "normally-off" device. If V_T is of having negative value and at the zero biasing gate, there is also current flowing through the device then the device is called as depletion-type which are rare in use.

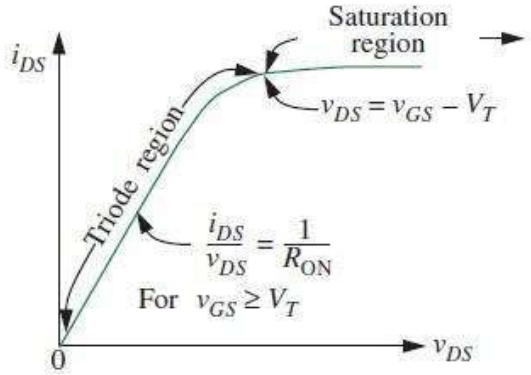

Fig 2.6: Operating regions of MOSFET

For the value of V_G below the value of V_T, the transistor is in cut-off region or is simply OFF. But when the value of V_G is more than V_T, there arises two conditions with respect to V_{DS} and of course in turn with respect to I_D also [7]. When V_{DS} is less than V_{GS}-V_T, transistor acts in the "triode or linear region" and when V_{DS} is greater than or equal to V_{GS}-V_T, transistor acts in the "saturation region".

The increase of drain current (I_D) with respect to the increase of V_{DS} is prominent in the linear region where our expectation is severely hampered about rise of the drain current in saturation region. But for the amplification circuitry, transistors operating in saturation region are much more valuable than the linear ones and hence the transistors operating in saturation region are called the "active device" [8].

$$I_D = 1/2\mu_n C_{ox} w/l \left((V_{GS}-V_T)\, V_{DS}-V_{DS}^2/2\right) \{ V_{GS}>V_T \text{ and } V_{DS} > V_{GS}-V_T\} \quad (2.6)$$

$$I_D = 1/2\mu_n C_{ox} w/l \,(V_{GS}-V_T)^2 \{V_{GS}>V_T \text{ and } V_{DS}< V_{GS}-V_T\} \quad (2.7)$$

2.11 Gm Filter

Gm stands for transconductance here. Where an input voltage is fed to an OP-AMP connected with a capacitor at the output of the amplifier current is sensed and appeared output.

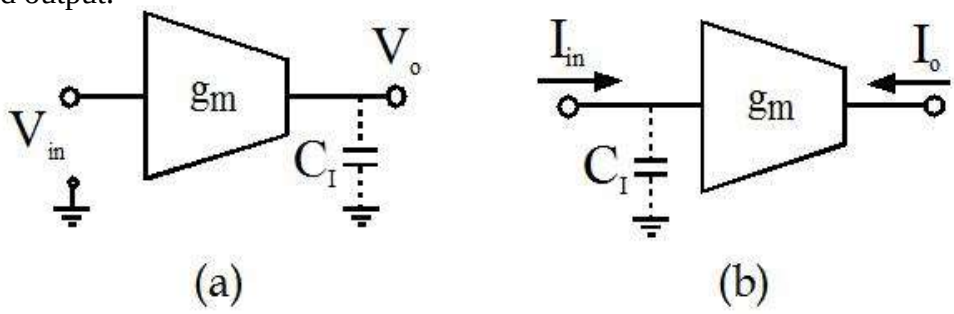

Fig 2.7: Simplest Gm-C Filter

The reason for using Gm-c filter is to achieve maximum or wide tuning range. And, we can also change the value of "Gm" and "C" to slow-down or fast-up the amplifier [1].

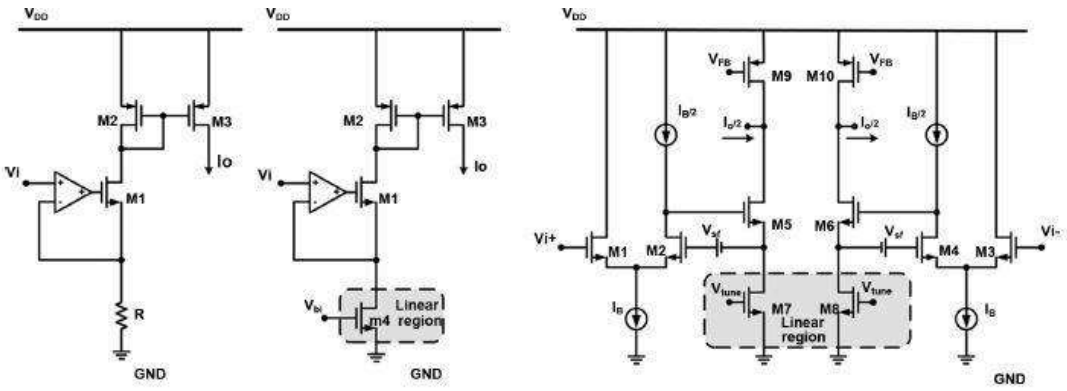

Fig 2.8: Transconductor circuit

Transconductor is the basic building block of Gm-c filter. And here there are three different types of transconductors are presented. To achieve wide tuning range previously resistors or series of resistors were added in the transconductor circuit. But this method increased the chip area and the precision of the transconductance got limited by the choice of the programmable resistors. Therefore, to achieve more tuning with less chip area these passive resistors are replaced by a N-MOS in linear region [1]. In linear region, a drain current is obtained and a linear voltage-to-current relationship for the circuit is obtained [4].

This research report is concerned about more tuning possibilities with the transconductor with again minimizing the chip area taking linearity of the circuit into consideration. Therefore further literature survey shows the possibility of achieving the desired goal by replacing the single N-MOS transistor by differential transistor circuit as shown in the figure. Gm-C filter always goes through a trade–off between noise and linearity. While linearity can be achieved by using C-MOS technological structures and circuits noise can be minimized by using BUTTERWORTH PROTOTYPE of Gm-C filter [1]. The circuit presented in the next chapter (literature survey) is a simplified approximate model of the desired circuit level of the Gm-c filter using transconductor as its basic operator.

Various transistors are used in butterworth prototype to form the application of a transconductor. Therefore, unfortunately SHORT CHANNEL EFFECTS still occurs and high order non-linearity components degrade the linearity of the V-I conversion, especially for nanoscale technology [1].

2.12 CMFB CIRCUIT

The full form of the abbreviation is “Common Mode Feedback Circuit”. This is an important structure finding a very special space in this research. Generally it is a feedback circuit followed by a differential amplifier to reduce the noise level by performing CMRR operation [4]. It senses the common-mode voltage, compares with a valid reference source and finally feeds back the correcting common mode signal to both the nodes of fully differential circuit to cancel out the output common mode current component and to fix the DC output up to a desired level [3].

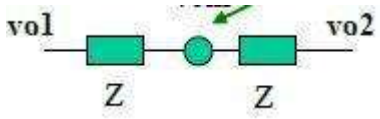

Fig 2.9: Simplest CMFB circuit

The arrow pointed node is “V_{CM}”. It is known as common mode voltage and defined as:

$$V_{CM} = V_{01}+V_{02}/2 \tag{2.8}$$

Advantages of using CMFB circuit are that it provides large transconductance gain with enough phase margins and also consumes minimum power to be operated. Also, common mode feedback circuit prevents the output from drifting out of the range in a fully differential OTA. Generally OTAs containing a CMFB circuit are high gain OTAs.

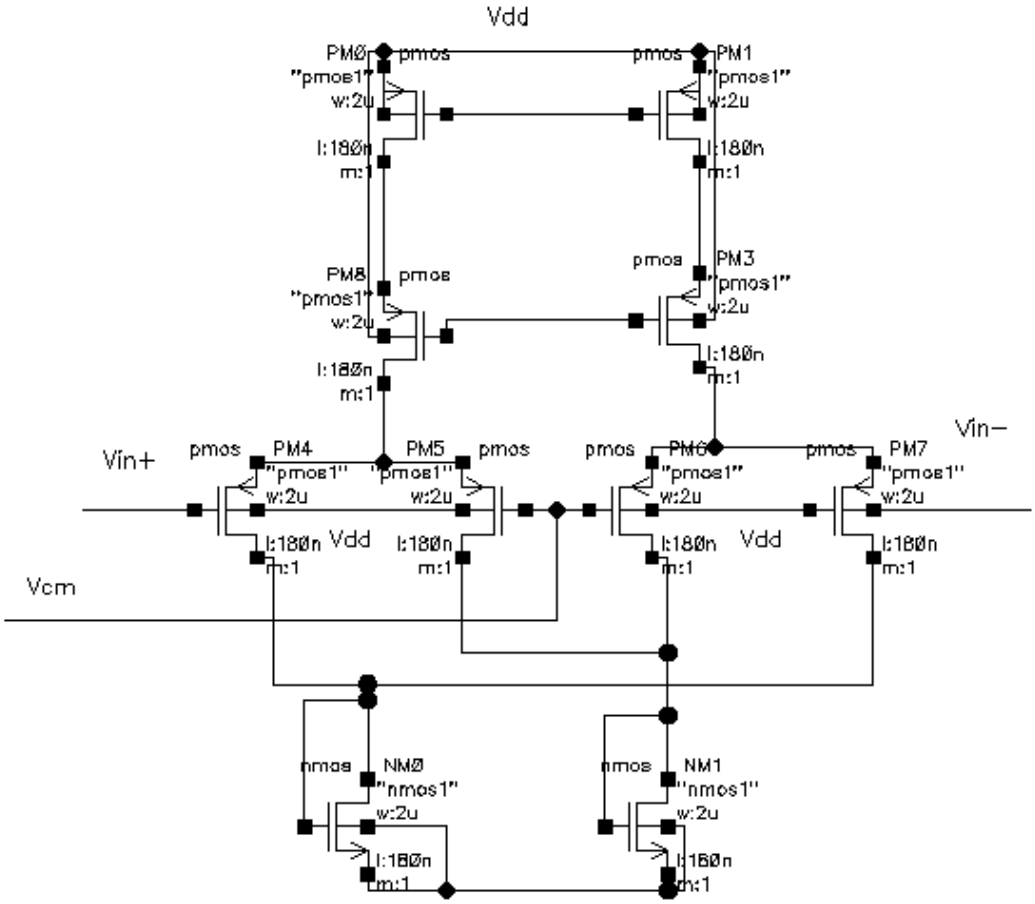

Fig 2.10: CMFB circuit

There are two differential pairs of MOSFETs are present to sense the difference between average output voltage coming from OTA and common mode voltage, V_{cm}. V_{cm} is applied to the circuit externally. Two biasing transistors are used below the differential pairs to provide biasing current.

2.13 Transconductor and OTAs

Transconductors are versatile building blocks employed in many analog and mixed signal circuit applications, such as continuous time filters, delta sigma modulators, variable gain amplifier or data converter. The transconductor performs voltage to current conversion [9]. Linearity is the most critical parameter in designing a transconductor. The tuning ability of transconductor is also mandated to adjust centre frequency and quality in the filter application.

The portable electronic equipment is in the trend of consumer market. Therefore, low power consumption and low supply voltage become the major challenge in designing CMOS VLSI circuits. However, designing for low voltage and highly linear transconductor, it requires taking into account some aspects which have already discussed in the previous literature. First is the linear input range. The range of linear input is justified by the constant transconductance, Gm. Since the distortion of transconductor is determined by the ratio of output currents versus input voltage [2]. Next is the controlling voltage of the transconductor. This voltage can greatly impact the value of transconductance, linear range and power consumption [2]. When controlling voltage increases, the transconduactance also increases but the linear input range of transconductor is reduced and power consumption is increased. Hence, it is critical in designing a transconductor to be operated in low supply voltage. Next factor is the symmetry of the two differential outputs. If the transconductance of the positive and negative output is: $Gm+=IO+/Vi$ and $Gm-=IO-/Vi$, then how close $Gm+$ and $Gm-$ should be a critical issue where $IO+$ is positive output current and $IO-$ is the negative one and Vi is the input differential voltage [9]. This factor is the major cause of common mode distortion of transconductor which occurs at the output.

Generally, design of differential transconductor can be classified into triode mode and saturation mode methods depending up on the operation regions of the input transistor. Triode mode transconductors have better linearity [4]. In general, the design of differential transconductor can be classified into triode-mode and saturation-mode methods depending on operation regions of input transistors.

Triode-mode transconductor has a better linearity as well as single-ended performance [5]. On the other hand, saturation-mode transconductor has better speed performance. However, it only exhibits moderate linearity performance. Furthermore, the single-ended transconductor of saturation-mode suffers from significant degradation of linearity.

Source degeneration using resistors or MOS transistors is the simplest method to linearize transconductor. However, it requires a large resistor to achieve a wide linear input range. In addition, MOS used as resistor exhibits considerable variations affected by process and temperature and results in the linearity degradation. Crossing-coupling with multiple differential pairs is designed only for the balanced input signals [7]. The Class-AB configuration can achieve low power consumption. On the other hand, the linearity is the worst due to the inherited Class-AB structure. The adaptive biasing method generates a tail current which is proportional to the square of input differential voltage to compensate the distortion caused by input devices. However, the complication of square circuitry makes this technique hard to implement.

The constant drain-source voltage of input devices is a simple structure. It can achieve a better linearity with tuning ability [9]. However, it needs to maintain VDS of input Source degeneration using resistors or MOS transistors is the simplest method to linearize transconductor [9]. However, it requires a large resistor to achieve a wide linear input range. In addition, MOS used as resistor exhibits considerable variations affected by process and temperature and results in the linearity degradation [8].

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Five basic types of OTA configurations are reviewed in this thesis work with their respective advantages, disadvantages and applications in analog circuits. Modifications on the basis of proven theory to these basic topologies are done in experimental work.

2.13.1 Single stage OTA

Configuration for single stage operational transconductance amplifier is shown in the figure below. This is the simplest OTA possible in electronics and hence the speed is very high.

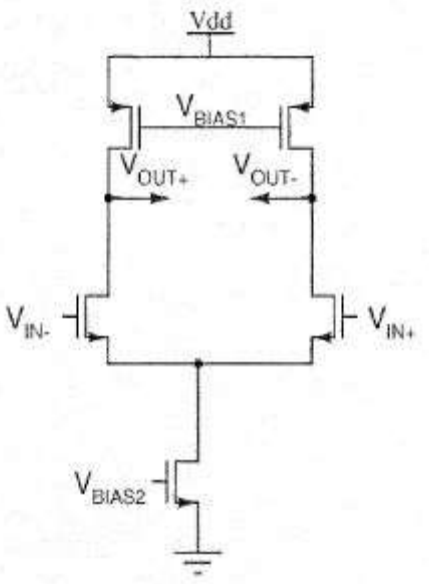


Fig 2.11: Single stage OTA

But the gain is relatively very low because, the output impedance of the circuit is very low. Low gain and low output impedance provide high unity bandwidth gain and therefore, higher speed.

2.13.2 Two stage OTA

One more stage is added to the single stage OTA. Addition of another stage brings the benefit of more gain up to a certain level. Of course, addition of extra circuitry increases complexity. This complexity reduces the speed of the amplifier.

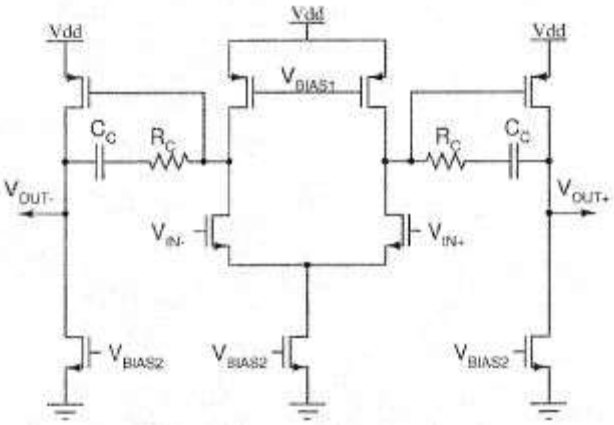


Fig2.12: Two stage OTA

An appropriate compensation technique is used to stabilize the two stages OTA. Miller effect is most popular technique to be used to find the compensating capacitance for this circuit.

2.13.3 Telescopic cascade OTA

Single stage amplifier is unable to provide high gain because of the low output impedance. So the basic idea is to boost up gain by increasing the output impedance. We can increase the output impedance by placing more and more cascade transistors along with an active load at the output of the OTA.

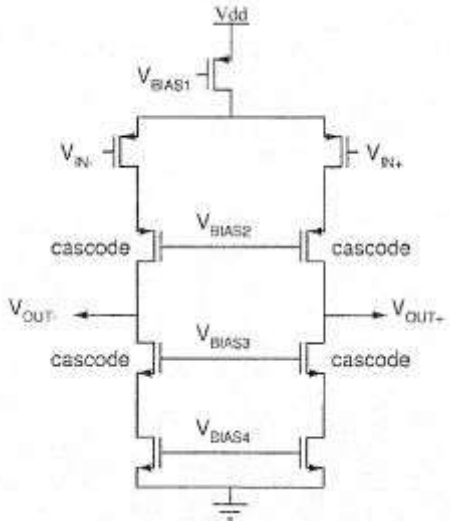


Fig 2.13: Telescopic cascode OTA

The telescopic cascode OTA provides high gain as well as high speed. But the voltage swing is very low in this configuration which makes it improper to be used in low power circuits or where the supply voltage is low. Various techniques can be applied to increase the voltage swing of telescopic cascode OTA.

2.13.4 Regulated cascode OTA

This is also known as gain boosting OTA. This configuration helps to get more gain without compromising the voltage swing.

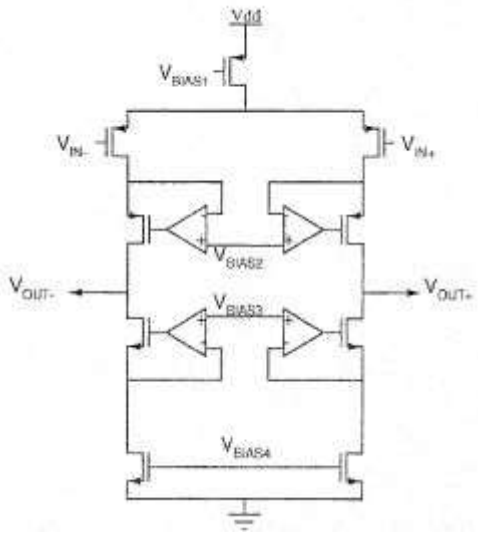


Fig 2.14: Regulated cascode OTA

This technique is introduced first by Eduard Sackinger and Walter Guggenbuhl. Again the extra amplifier circuit reduces the speed. Therefore it should be designed in such a way that the bandwidth of the entire configuration should not be affected.

2.13.5 Folded cascode OTA

It can be treated as an intermediate circuit of two stage OTA and telescopic cascode OTA. It is capable of taking low supply voltage and still can perform high output voltage swing.

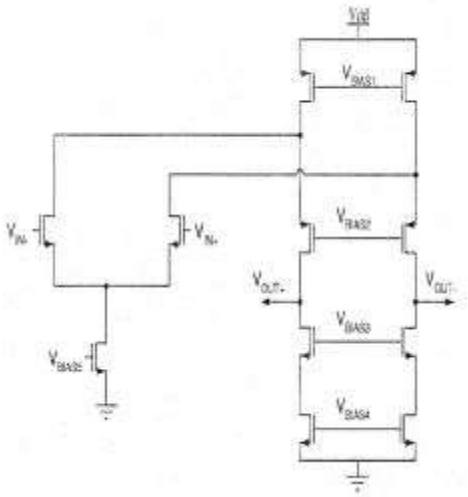


Fig 2.15: Folded cascode OTA

Gain of the folded cascode OTA is less than that of two stage OTA and also, the speed is less than that of telescopic cascode OTA.

2.14 Technique to Increase Gain of Op-Amp

Small size transistors are used frequently in high frequency modern analog circuits. Small size induces hot carrier effects along with channel-length modulation and the DC gain becomes limited. Scaling the devices down further reduces the gain.

Generally gain is increased in an op-amp by adding more stages or cascading transistors to enhance the output impedance. But these two techniques do not provide good frequency response and also, cascading alone confronts with voltage-headroom problem. Therefore, the idea is to separate the frequency response and gain of the amplifier and by increasing output impedance alone without affecting output swing or frequency response, we can get an increased amount of gain. This technique is very much compatible with A/D conversion application which is inevitable in Gm-C filter.

2.14.1 Normal Cascode Circuit

This is the basic technique used for getting higher gain from an amplifier. The general structure of this configuration is that the common source amplifier is followed by a common gate stage.

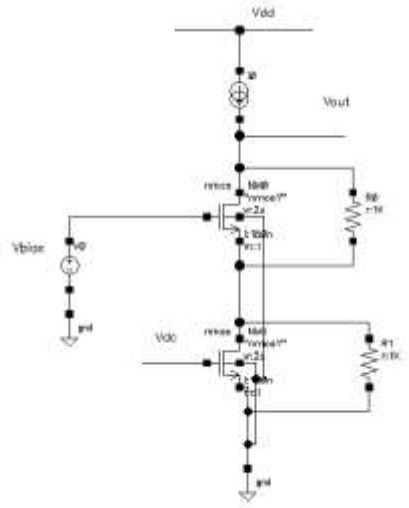


Fig 2.16: Normal cascode circuit biased by a current source

This type of architecture automatically increases the output impedance and reduces the input capacitance, thereby providing higher gain and higher frequency response respectively.

2.14.2 Regulated Cascode Circuit

Though the output impedance is more than the normal cascode configuration, the voltage range also increased with the help of regulated cascode amplifier.

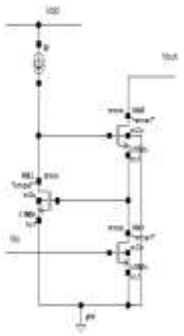


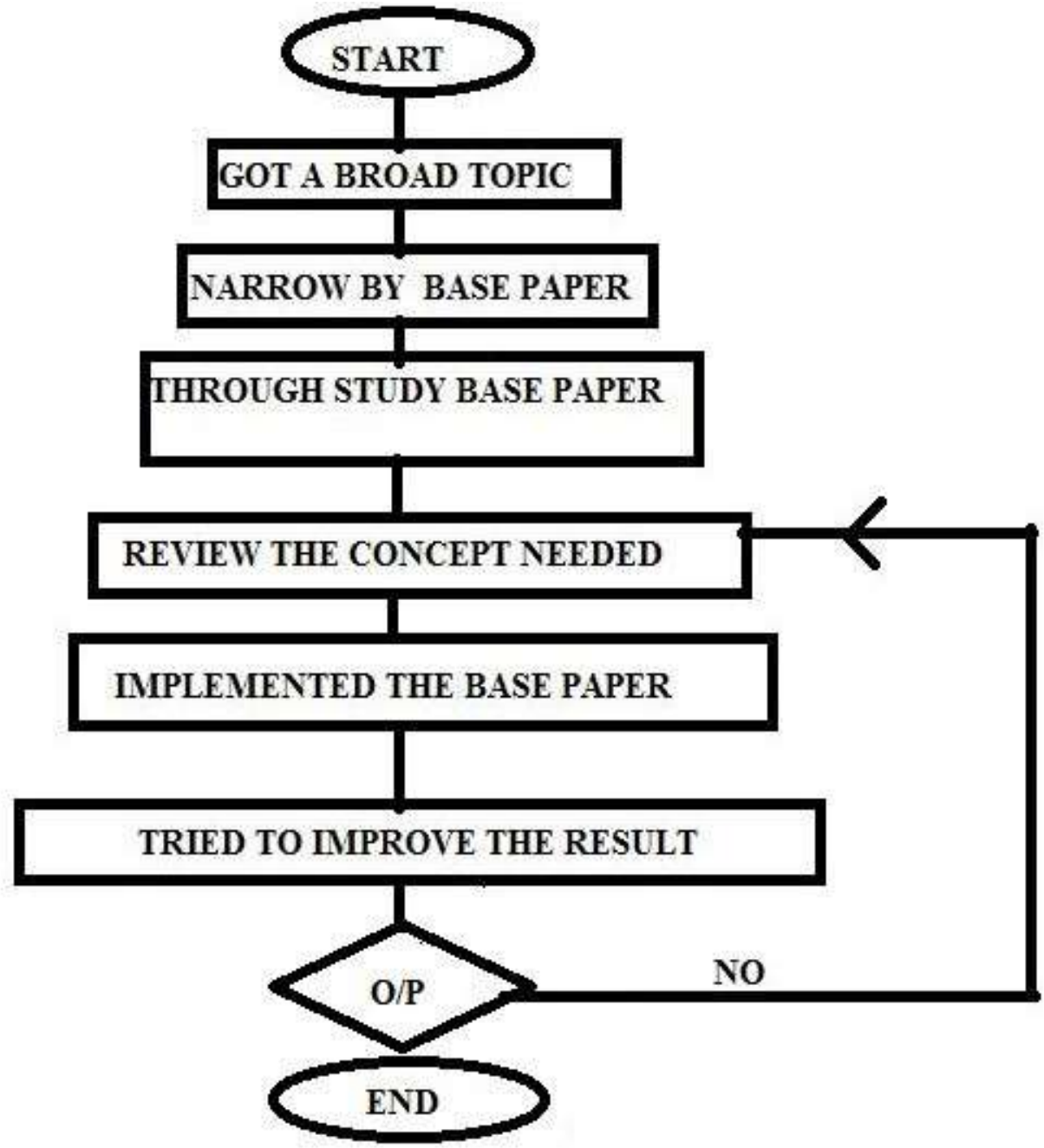
Fig 2.17: Regulated cascode amplifier

Input voltage is provided at the gate terminal of T_1. This results a drain current I_0 which flows in the source-drain path of T_1 and T_2 and this current ultimately

corresponds to the output current. The source-drain voltage must be kept stable to increase the output resistance. The I_0 current is fed through T_3 and fed back to the follower transistor T_2. This loop keeps the voltage of source-drain path stable providing high output impedance.

CHAPTER 3

RESEARCH METHODOLOGY



CHAPTER 4

MATERIALS, EQUIPMENTS AND EXPERIMENTAL SET-UP

4.1 Cadence virtuoso

The circuit we implement in analog or mixed signal applications are micro circuits. Even we cannot see the interconnections or components properly with our naked eye. In reality, we first design the circuit on semi-custom software and simulate it with various responses to check the correctness of the circuit. Simulation leads to a different field of analog electronics, "Testing". The software here in this research used for designing the circuit as a soft-copy of real hardware manufacturing is called as "Cadence Virtuoso". It is an Electronic Design Automation (EDA) found in the year of 1988 by the combine effort of SDA system and ECAD whose headquarter is situated in California. Cadence provides technologies to engineers across the world for full-custom and semi-custom design of ICs, S-O-Cs and printed circuit board. Among different platforms provided by Cadence such as: encounter, incisive, palladium series etc. virtuoso is one of the most important platform for designing ICs including schematic entry, behavioural modelling, circuit simulation, custom layout, physical verification, extraction and back-annotation which I have used for designing my concerned circuit of Gm-C filter.

4.2 My proceedings

Cadence virtuoso runs on Linux Red Hat Software. After opening the main window with linux software certain code is to be written by right clicking and opening new terminal to redirect the files for virtuoso placed in the computer. Then, the schematic main window is opened and circuit is to be created by adding a new library (DADUL) and attaching this library to a technical library of gpdk-180. Then, a new cell view is to be created (THESIS) under which the real design of the circuit is done. Finally, out of around 25 simulation options available in virtuoso platform, AC simulation is done for getting the frequency response of

the circuit. The circuit and the output results are saved and taken print-out by external hardware device to attach within the dissertation file.

4.2.1 Design of a two stage OP-AMP

The world of analog industry is always trending with more and more gain as the technology advances and of course higher gain is achieved in accordance of trade off with other transistor parameters. Expected high gain is not possible to avail through a single stage differential amplifier. Therefore, a 2 stage operational amplifier is created and simulated using cadence virtuoso.

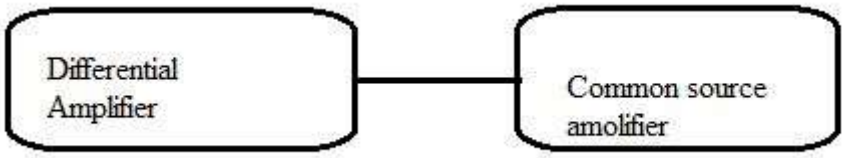


Fig 4.1: Basic two stage amplifier

A_1 is a simple differential amplifier which is expected to provide gain around 20dB – 40dB. But we are interested in more gain which can be accomplished by adding an extra amplifier to the differential amplifier. In this case, a simple common source amplifier is taken along with the present differential amplifier. Of course, we can take other types of amplifiers such as common drain or common gate or any other type of simple single stage amplifier. Now, the overall gain is calculated of this configuration of two stage operational amplifier.

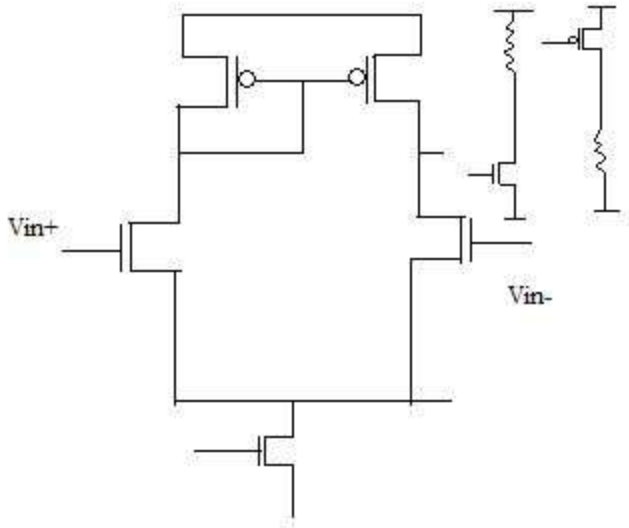


Fig 4.2: Connection of diff. amplifier to a common source amplifier

There are two types of configurations present as common source amplifier; using PMOS and NMOS along with a resistor load attached to the source end of the respective transistor. This resistor can be replaced by a current source which is further can be replaced by a transistor. We have chosen the PMOS configuration as output swing can be reduced or limited in the NMOS configuration. So the desired circuit will look like:

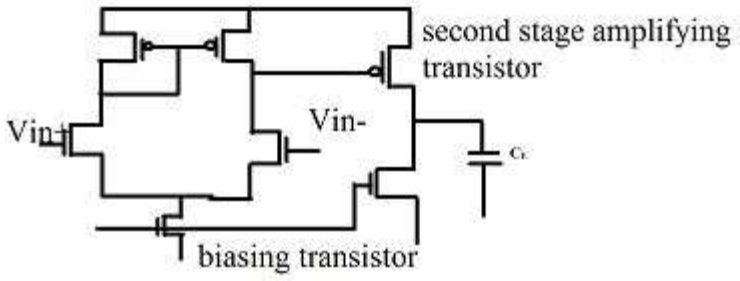


Fig4.3: Two stage operational amplifier

A capacitive load C_L is added at the output node of the second stage amplifier whose value can be given at the desired specifications later. The NMOS of the second stage amplifier is given the bias voltage at its gate input from the tail transistor of the differential amplifier. Input to the differential amplifier can be given at the differential input of two NMOS and the output of the differential

amplifier is provided as the input to the PMOS of common source amplifier. And, the final output is taken at the capacitive load, C_L.

Well, the given connection is not so easy and convenient and we cannot just connect the wires as shown in the figure. There is some practical problem while connecting two amplifiers to boost the gain.

As we all know that differential amplifier is a single pole system say, P_1. Because of the presence of only one pole we never worry about the phase and stability of the differential amplifier. There is only one RC component in a single stage differential amplifier which can be seen in its small signal model. The gain bandwidth product, GBW comes way after the position of the first pole, P_1 and there is very least chance of getting an un-stabilized characteristics from this amplifier. The point where the GBW lies or the gain curve crosses the 0dB line, gives a phase shift of 90^0 generally which is all beyond an acceptable value. At least 45^0 phase margin is considered as a good value but in real physical design 60^0 phase margin is required in most and a very good value for analog simulation.

But while connecting the two amplifiers, we introduce two RC components which ultimately produce two poles and the system becomes a two pole-system say, P_1 and P_2. This drastically reduces the stability of the system. The gain bandwidth product, GBW when comes after two poles, it becomes more prone towards instability performing a decay in gain by -20dB/decade and -40dB/decade respectively. The phase margin also suffers severely getting reduced from 180^0 to 0^0 by degradation in two slots such as 90^0 and 0^0. This problem needs to be addressed otherwise the motive behind the creation of two stage amplifier to get more gain will go in vein completely.

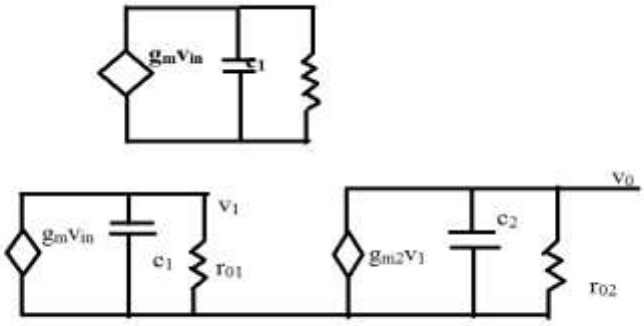


Fig 4.4: Small signal model of amplifier

Roughly,

$$P_1 = 1/r_{01}c_1 \quad \text{and} \quad P_2 = 1/r_{02}c_2$$

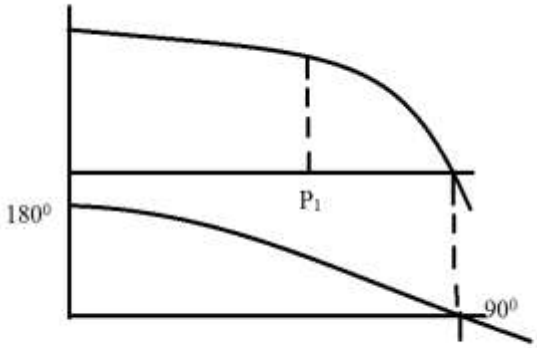


Fig 4.5: Gain and phase with single pole

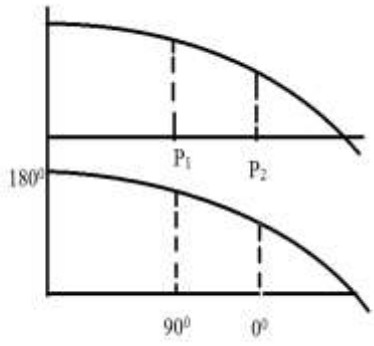


Fig 4.6: Gain and phase with double poles

To overcome this problem we try to make the system as a single pole system. Though, the statement contradicts the practical scenario, we can avail the luxury of a single pole system by considering a pole as a dominant pole and try to move the dominant pole towards the '0' axis. In this case, we consider pole, P_1 as the dominant pole and using various techniques we will try to move the pole, P_1 towards zero such that the gain curve will cross the 0dB before the second pole, P_2 appears. That means, the second pole will have eventually no effect or can say minimum effect over stability of the system because, there is no control of gain curve on stability after 0dB. All the techniques applied to move the dominant pole towards the left of the plane come under the category of 'compensation technique'. The detail of the compensation technique or method is discussed below.

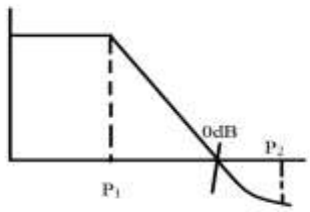


Fig 4.7: gain degradation because of second pole

An extra compensated capacitor, C needs to be added with the circuit to move the dominant pole towards the left of the plane. Adding a big capacitor is never a solution to the problem. Here, we take the help of 'Miller effect' and instead of adding a big capacitor, we can use a relatively very small value of capacitor yielding the same result which can be accomplished using the big capacitor. The small signal model of the circuit is now presented after inserting the compensated capacitor

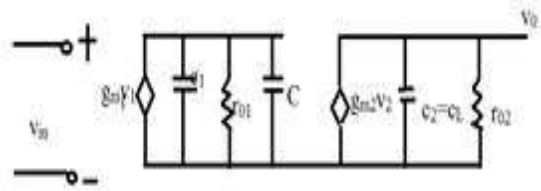


Fig 4.8: small signal model of two stage amplifier

It is clearly visible that there are two RC components present in the small signal model representing two poles of the system, P_1 and P_2. Form the figure we ca say that,

$$P_1 = 1/r_{01}\ (c_1+C)$$

This big capacitor, C can be replaced by a miller capacitor, C_c which relatively smaller than the previous one. But as per the definition of the miller effect the capacitor should be connected between the two outputs of the two stages. The possible circuit diagram, block representation diagram and small signal model diagram is presented below.

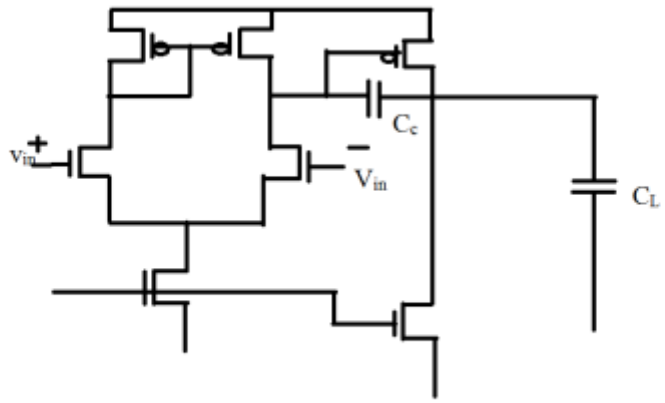


Fig 4.9: Two stage op-amp

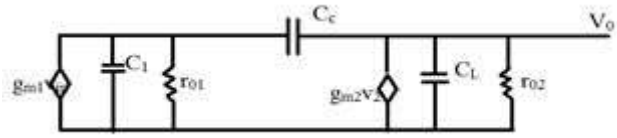


Fig 4.10: Small signal model with compensated capacitor

But we cannot just connect the miller capacitor in this way. There is still some limitations present in form of the pole splitting and zero positioning. Also at high frequency sometimes the C_c got short. Therefore, the manual calculation of the transfer function is done. First V_1/V_{in} is calculated followed by the calculation of V_{out}/V_1: ultimately the two terms are multiplied to get the result of V_{out}/V_{in} which is the transfer function of the system.

Taking node voltage equation of the first half of the small signal model,

$$V_1 = V_0 S C_c . R_1 – g_{m1}V_{in}R_1/1+S R_1(C_1+C_c) \quad (2.9\ a)$$

From the node equation of the second part of the circuit and value of V_1,

$$V_0/V_{in}=g_{m1}R_1.g_{m2}R_2(1- SC_c/g_{m2}) /$$
$$S^2[R_1R_2(C_1C_2+C_1C_c+C_2C_c)]+S[R_2(C_c+C_2)+R(C_c+C_1)+C_cg_{m2}R_1R_2]+1 \quad (2.9\ b)$$

But this big equation is definitely not suitable from the design perspective and to design an amplifier from this equation is really very difficult. Therefore, the equation is needed to be standardized first for the simplicity.

$$V_0/V_{in} = A_{DC} (1-S/Z) / (1+S/P_1) (1+S/P_2) \quad (2.10)$$

This can be further modified to,

$$V_0/V_{in} = A_{DC} (1- S/Z) / 1+s (1/P_1 + 1/P_2)+S^2(1/P_1P_2) \quad (2.11)$$

'Z' corresponds to zero of the system. P_1 and P_2 are the two poles and A_{DC} is the DC gain of the system. Since, P_2 is very small in comparison to the P_1 we can ignore the term related to P_2 carefully. This is because P_2 is far away from P_1. Accordingly, it is found that $1/P_1$ is the coefficient of S. Therefore,

$$P_1 = 1/g_{m2}R_2R_1C_c \quad (2.12)$$

$$P_2 = g_{m2}/C_2 \quad (2.13)$$

Also,

$$Z = g_{m2}/C_c \quad (2.14)$$

$$A_{DC} = g_{m1}R_1. g_{m2}R_2 \quad (2.15)$$

We have,

$$GBW = DC\ gain * P_1 = g_{m1}/C_c \quad (2.16)$$

As we all know that the phase margin should be at least greater than 45^0 and a good value of phase margin is considered above than 60^0 for the safety reasons. By calculating the angle of V_0/V_{in}, it is found that the condition for phase margin to be more than 60^0 is,

$$C_c \geq 2.2\ C_L \qquad (2.17)$$

Before, proceeding to the real design of amplifier some desired specifications need to be attached with the amplifier. As a designer we always expect some desired qualities to be maintained in the amplifier. Here, some specifications are pre-mentioned for the design to be carried out further.

Table 4.1: Pre design specifications for amplifier

DC gain	60dB
Slew rate	20v/usec
GBW and PM	30MHz and more than 60^0
Load capacitance	2pF
Power dissipation	Less than 300uW
ICMR+	1.6v
ICMR-	0.8v

We already have 180nm process. That means, the minimum length of a transistor in this process can be of 180nm. V_{DD} for this technology is 1.8v which can be found easily in the 180nm design kit. From the above specifications and by the help of "square law equation", the moderate or allowable sizes of the MOSFETs are found. GBW, maximum common mode range, slew rate and minimum common mode range play a vital role to get the descent sizes of MOSFETs of the two stage amplifier which is explained in the successive chapter with simulation diagram.

Some experimental findings are earned during the design process of the amplifier. Such as, very high biasing current limits the gain of the amplifier. Increasing the sizes of M_1 and M_2 increases the gain of the circuit. M_3 and M_4 control the maximum common mode range quite drastically and M_5 determines the value of minimum common mode range value. M_6 is the major cause for the second stage gain in the circuit. And, M_7 is actually a current source which is somewhat related to the gain. And, most importantly C_c has actually no effect on gain and the interesting thing is that the rumour takes the opposite angle of what is been said here.

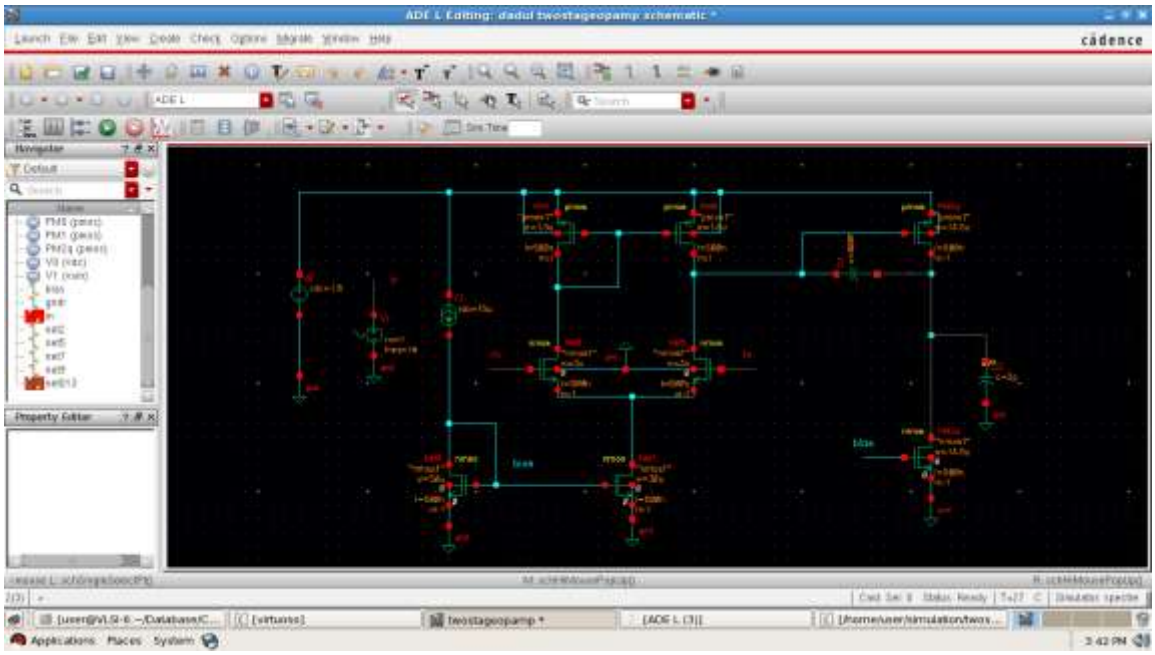


Fig 4.11: Schematic of two stage OP-AMP

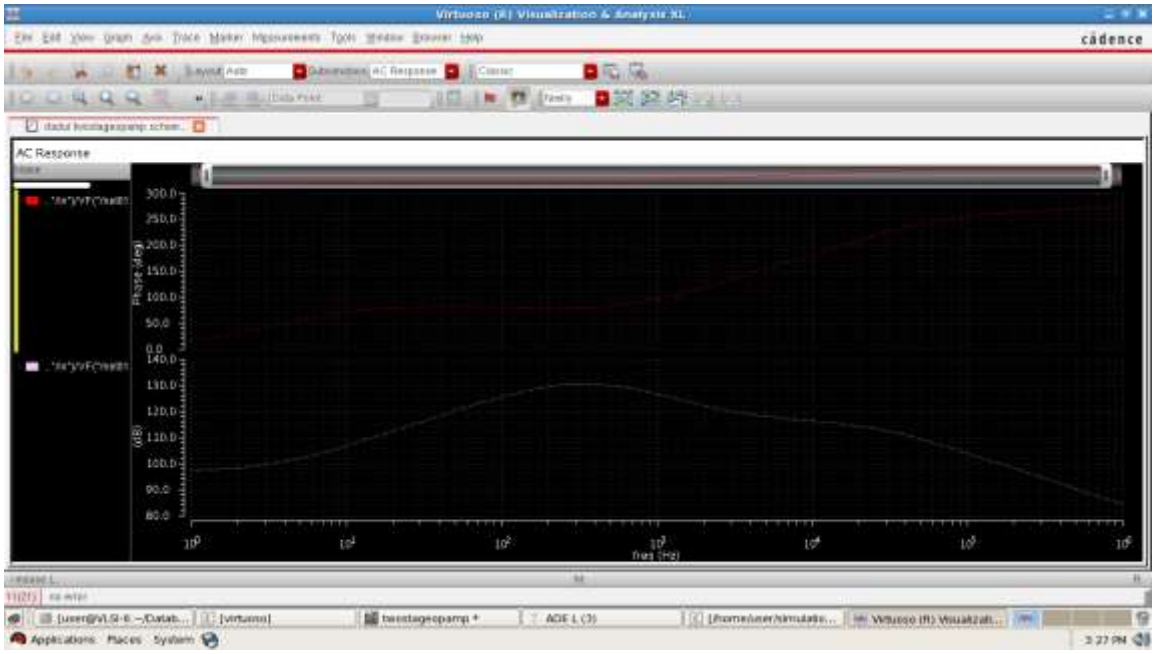


Fig 4.12: Gain and phase simulation of two stage amplifier

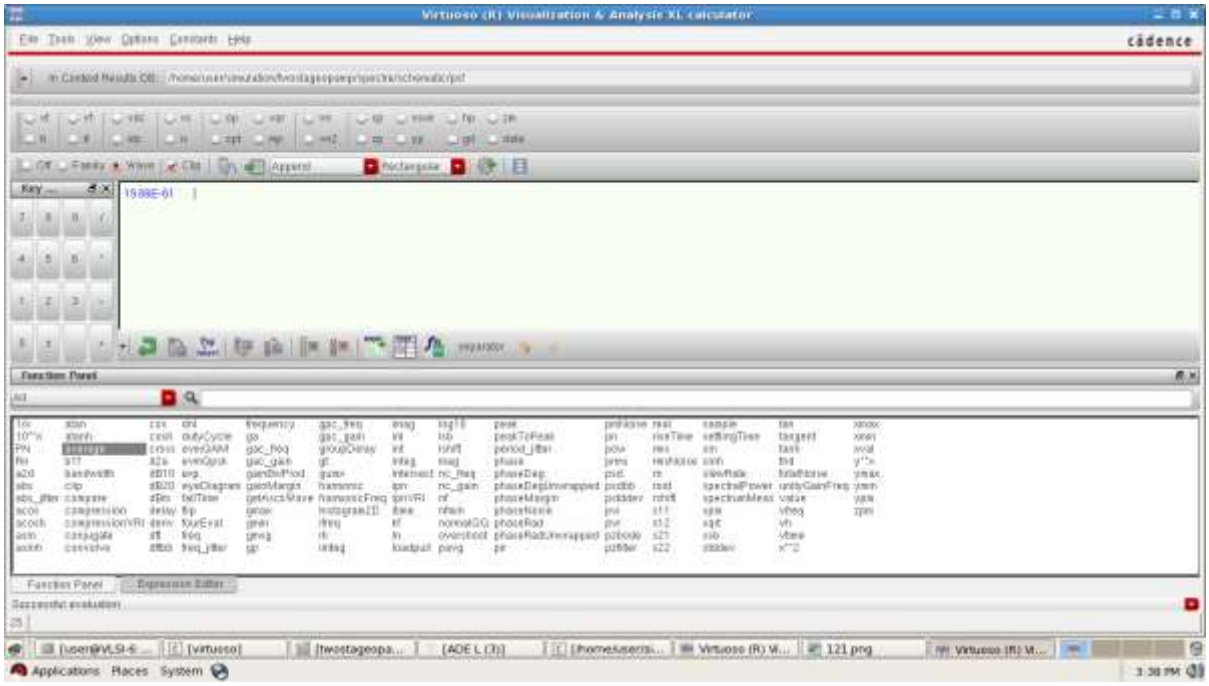


Fig 4.13: Power dissipation of OTA

4.2.2 Design of OTA using this two stage OP-AMP

There are two two-stage op-amps are connected in differential structure followed by a highly linear current multiplier to perform as an operational transconductance amplifier which will be best fit for our desired Gm-C filter.

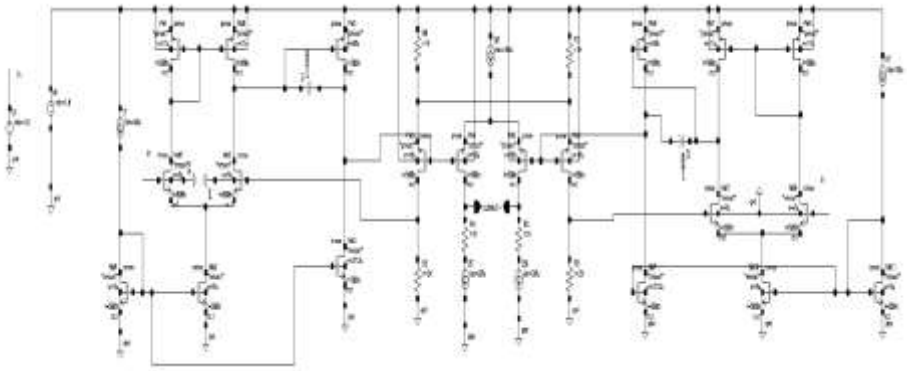


Fig 4.14: Transconductor schematic

The transconductor has a very wide tuning range. The translinear loop followed by the differential op-amps is acting as a current-mirror. This current mirror provides the wide tuning range. Feedback circuit equalizes the input voltage with the drain voltage of two outside transistors of the current mirror. Then, the current flowing through the two lower resistors will have a very linear relationship with the input voltages.

4.3 Previous works on proposed transconductor

Dr. Mohammed Ismail and his team of OHIO University have already done tremendous work on operational transconductance amplifier to be utilized in a low pass filter of wireless transceiver. Their proposed OTA is presented below along with simulation results.

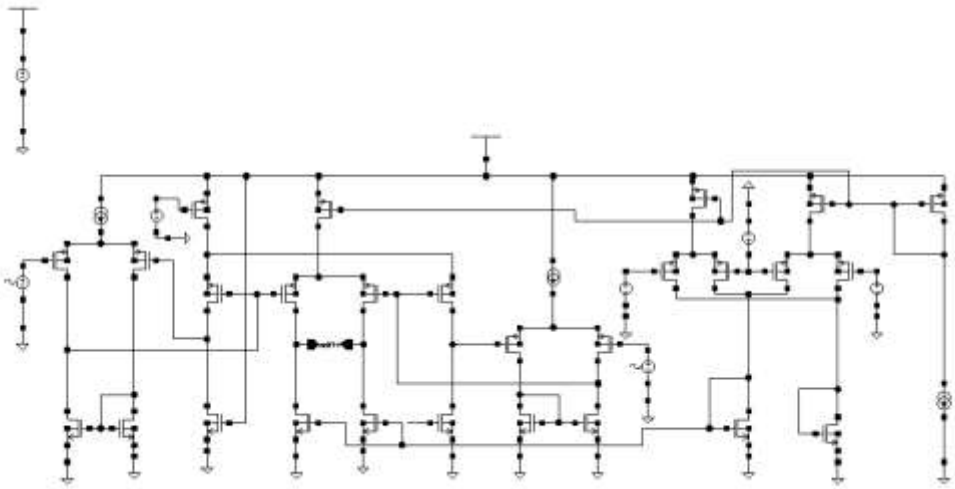


Fig 4.15: Base paper OTA

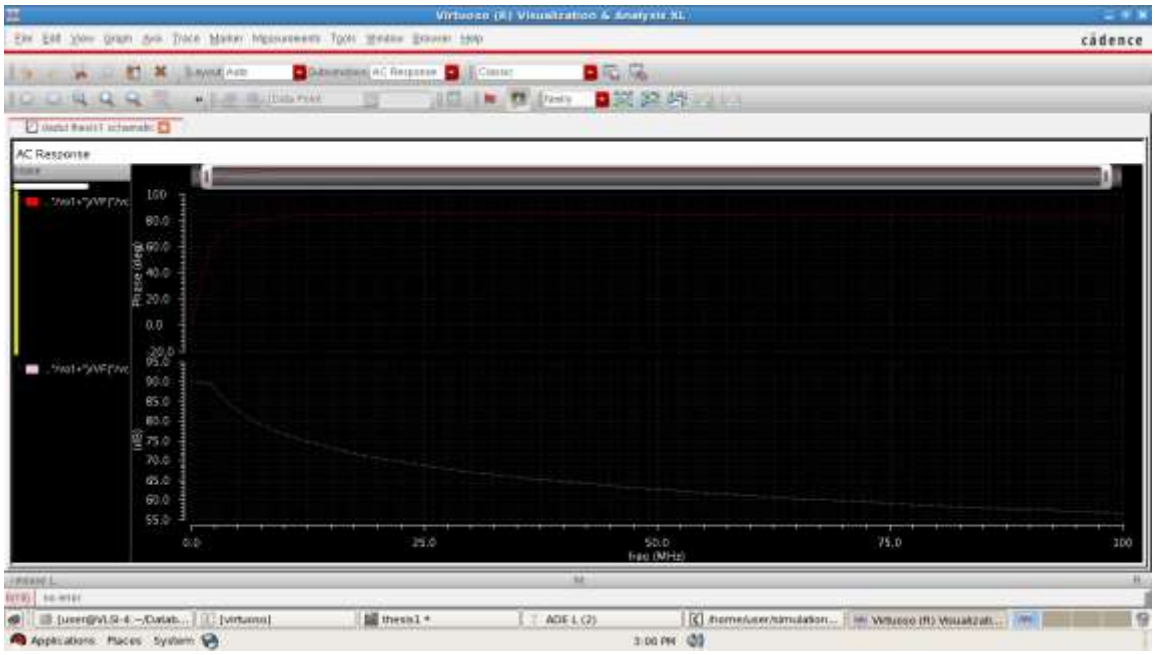


Fig 4.16: Simulation result of base paper

4.4 Comparison table between previous work and my work

Table 4.2: Comparison table

PREVIOUS WORK	PRESENT WORK
Gain: 80dB-90dB	Gain: >100dB
Phase: well above 60^0	Phase: well above 60^0
Frequency range: 0-20 MHz	Frequency range: 10-10^6 MHz

By replacing the CMFB circuit by a translinear loop we got more gain while phase margin is never a concern throughout this research as it always keeps the value more than $60^{0.}$ That means the system is stable throughout the operation. Feedback circuitry reduces the DC gain and we got rid of that problem by using a translinear loop acting as a current source.

CHAPTER 5

CONCLUSION AND FUTURE SCOPE

As the technology shrinks day by day perhaps this method used here to obtain high gain operational transconductance amplifier will not be accepted further to be used in a Gm-C filter which will be further used in a wireless transceiver. Channel length will go down so will go down the supply voltage. Low power and high speed operation may limit the gain. Therefore, advanced technology need to be implemented to obtain higher gain and wider tuning range. Some of the methods are briefly discussed here under the caption of "future scope" and can be researched further.

5.1 Design of gain boosted telescopic cascode amplifier

Some design specifications are provided prior to the design of the amplifier. Further edition is done to ensure proper operating region, stability and transistor sizing of the amplifier.

Table 5.1: Desired specifications for telescopic op-amp

Open loop gain,A_0	>85dB
Unity gain frequency	>80MHz
Phase margin	$>55^0$
Load capacitance	1pF
Supply voltage	1.8v
ICMR	0.8v - 1.6v
Output swing	0.8v – 1.6v
Power dissipation	<10mW

The benefits of using telescopic OP-AMP is that it can ensure high gain with certain manipulation in design parameters. And more over, telescopic Op-amps have the inherent property of providing high speed. Therefore, less compromise can be accommodated but using this type Op-amp over its performance parameters.

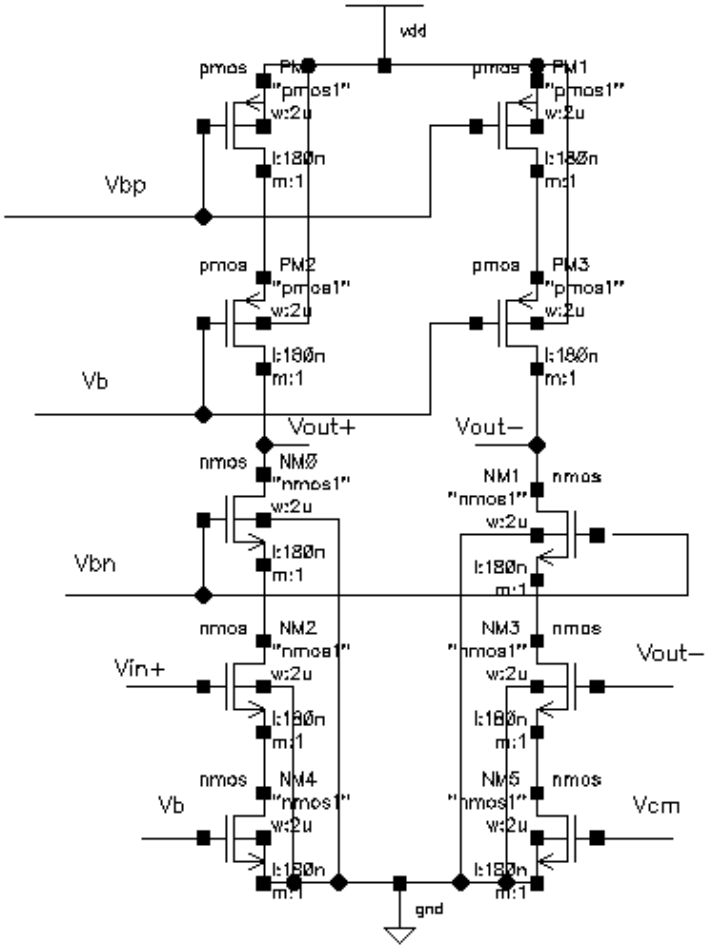


Fig 5.1: Telescopic OTA

Two NMOS are used at the lower side of the circuit to sense the differential voltage and the two should operate same operating region that is saturation region. Operating these transistors in triode region will make the OTA to be non-linear and also the DC gain will be reduced.

Common mode of the input is different from common mode of the output. This leads the input differential pair to be played under saturation region. Special attention should be provided when we use this Op-amp in bigger circuits. In bigger circuits generally, the output of the telescopic OTA is fed as an input of another OTA; that means common mode feedback circuit will be used to adjust the V_{cm} of the OTAs.

5.2 Fully differential telescopic amplifier

A fully differential telescopic amplifier is presented below.

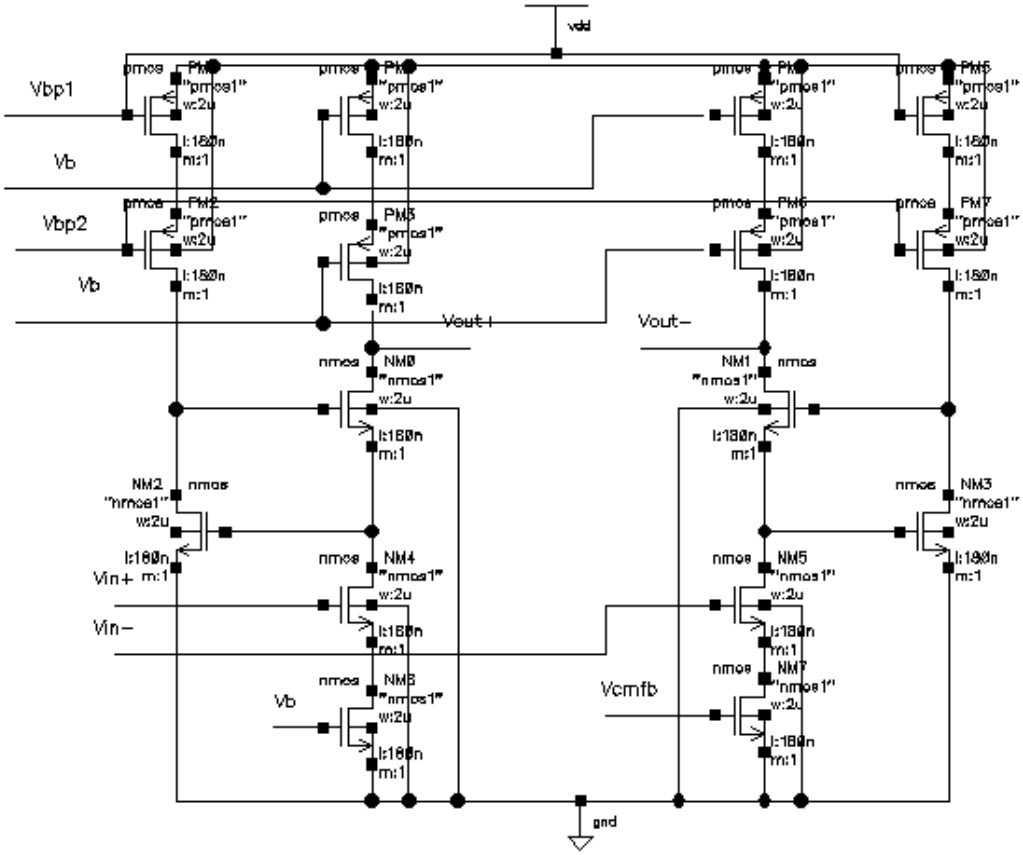


Fig 5.2: Fully differential telescopic amplifier

Two common source NMOS op-amps are used with cascode current loads. Output of these amplifiers is provided as the bias-voltage to another pair of NMOS transistors. Hence, the gain of these common source amplifiers is

multiplied with the gain of telescopic section shown above. Speed of the circuit is not affected so much because no additional gate is included in the signal path.

5.3 Wide swing cascode biased OTA

The wide swing configuration makes it a better option than the normal cascode OTA as the signal swing limitations do not prevail in this configuration.

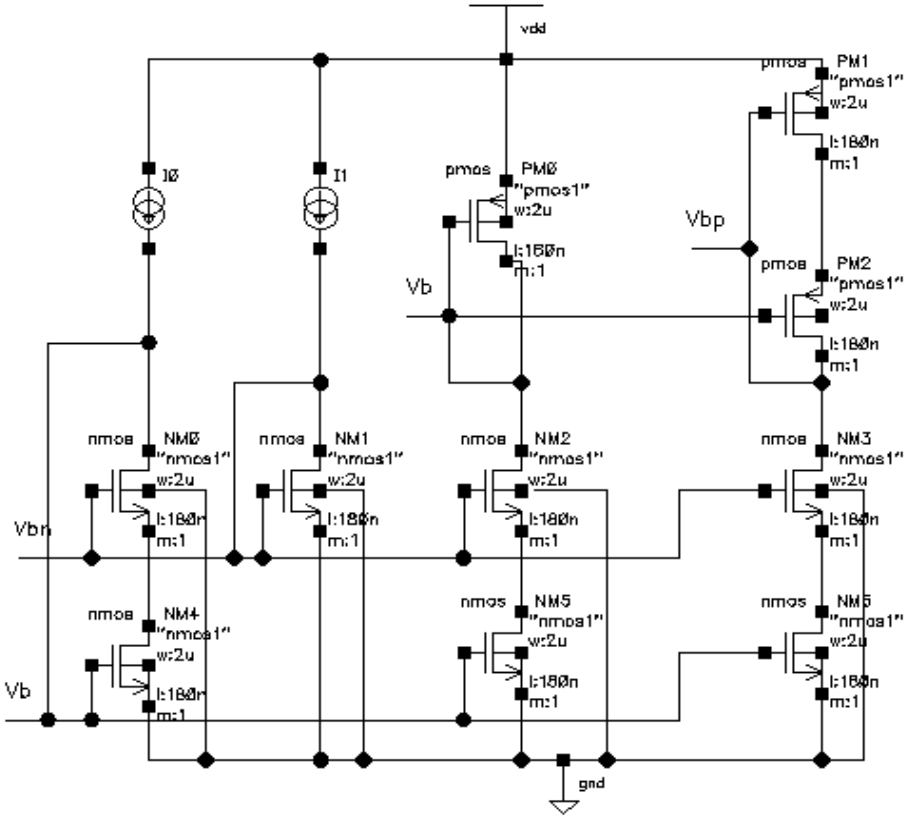


Fig 5.3: Wide swing cascode OTA

This configuration is based on very much popular WILSON CURRENT MIRROR technique. One transistor in the cascode structure acts as the current mirror while the other one basically acts as buffer. High biasing current can improve the tuning range of the amplifier but the very high values of these current sources can further be a hurdle on the path of tuning range as well as gain. Therefore, biasing current need to be taken carefully and 20u amp is used here in this 180nm process and 1.8v of supply voltage. Transistor sizes are chosen to make the operation in saturation region.

Population explosion with respect to limited resources forces engineers to work more over getting low power, low noise, low area, high performance integrated circuit with higher linearity and higher gain and speed etc. Therefore, scope of using CMOS technology is inevitable and will remain such till some new dynamic technology is invented. Of course, the output provided here is not satisfactory but implementing more cascaded version or inverting the position of PMOS and NMOS transistors or changing w/l ratio up to a adequate level may get more than desired output. Because of importance of wide frequency accommodation by a direct conversion filter, the further research work will have to be taken with greater sincerity and care. A sixth order configuration of Gm-C filter can be implemented for higher linearity and more wide tuning range. Success of this research study will bring a huge advantage to communication field and will be very much useful for mankind.

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