DISSERTATION-II REPORT

On

SIGMA-DELTA ADC FOR BIO-MEDICAL APPLICATIONS

Submitted in the partial fulfillment of the requirement for the award of degree

Masters of Technology

In

VLSI DESIGN

Submitted by

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ABSTRACT

A general biomedical device comprises energy source, analog-to-digital conversion (ADC), digital signal processing, and communication subsystem, each of which must be designed for Minimum energy consumption to adhere to the stringent energy constraint.

The ADC is a key building block in the sensing stage of the implantable biomedical devices. To lower the overall power consumption and allow full integration of a complete biomedical sensor interface, it is desirable to integrate the entire analog frontend, back-end ADC and digital processor in a single chip. While digital circuits benefit substantially from the technology scaling, it is becoming more and more difficult to meet the stringent requirements on linearity, dynamic range, and power-efficiency at lower supply voltages in traditional ADC architectures. This has recently initiated extensive investigations to develop low-voltage, low-power, high-resolution ADCs in nanometer CMOS technologies. Among different ADCs, the ΔΣ converter has shown to be most suitable for high-resolution and low-speed applications due to its high linearity feature.

This thesis investigates the design of high-resolution and power-efficient Sigma-delta ADC to attain the high and signal to noise ratio.

CERTIFICATE

Certified that this Dissertation-II Report entitled "**Sigma-Delta ADC for Bio-medical applications"** submitted by **Pavan Jamendar.M** having registration number **11310296,** student of Electronics and Communication Engineering Department, Lovely Professional University, Phagwara, Punjab in the partial fulfillment of the requirement for the award of Masters of Technology (VLSI Design Engineering) Degree of LPU, is a record of student's own study carried under my supervision and guidance.

This report has not been submitted to any other university or institution for the award of any degree.

Name of Project Supervisor & Signature
Designation

DECLARATION

I hereby certify that the work, which is being presented in the report entitled "SIGMA-DELTA ADC FOR BIO-MEDICAL APPLICATIONS" in partial fulfillment of the requirement for the award of the Degree of Masters of Technology submitted to the institution is an authentic record of my own work carried out during the period August 2014 to November 2014 under the supervision of Dr.Anita Kumari.

Pavan jamendar Muvvala

Date: December 2014

11310296 Signature of student

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Pavan Jamendar M

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LIST OF ABBREVITATIONS

ADC	Analog-to-Digital Converter
SAR	Successive-Approximation ADC
CIFF	Cascade of Integrator Feed Forward
SDM	Sigma-Delta Modulator
DSM	Delta-Sigma Modulator
CMOS	Complementary Metal-Oxide-Semiconductor
CT	Continuous Time
DT	Discrete Time
DC	Direct Current
Vdac	Voltage from DAC
DAC	Digital to Analog Converter
ECG	Electrocardiogram
EEG	Electroencephalogram
IC	Integrated Circuit
GBW	Gain Bandwidth Product
ENOB	Effective Number of bits
FOM	Figure of Merit
SR	Slew Rate
NTF	Noise Transfer Function
OSR	Oversampling Ratio

OTA	Operational Transconductance Amplifier
PSD	Power spectral Density
SC	Switched Capacitance
SOP	Switched op-amp
STF	Signal Transfer Function

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CHAPTER 1

INTRODUCTION

1.1 INTRODUCTION TO ADC

Analog to digital converter is a device which is used to convert an analog signal i.e. a continuous physical quantity (usually voltage and current parameters) in digital form or a digital number representing the analog quantity as magnitude or amplitude. The analog to digital conversion involves quantization and sampling a analog quantity which may also leads to small amount of errors. An ADC converts a continuous time analog signal and continuous amplitude analog signal to digital i.e. discrete time signal and discrete amplitude digital signal.

Analog refers to physical quantities that vary continuously instead of discretely. The physical phenomena typically involve analog signals. We have many examples like speed, temperature, pressure, voltage, etc. But microprocessors work with digital quantities, means the values which are taken from discrete domain. To interact analog systems with digital systems or digital systems with analog systems conversion is needed.

In the analog to digital converter the input vary from minimum to maximum value of volts or amperes. The output is a digital number that represents the input value. In the digital to analog converter the input that determine an output whose value changes in steps. These step changes are in volts or amperes. Analog to digital conversion techniques have become extremely important. In this a great deal of technical effort has gone to produce analog to digital converters. Which are accurate, fast, and cheap.

1.2 NYQUIST THEOREM

The amount of time required to sample the analog signal is known as sampling time .one ma think it is necessary to sample analog signal continuously without any gap between consecutive samples it turns to error in the signal.

To avoid these type of error we use the Nyquist theorem, it states that the sampling frequency Fsamp is slightl greater than maximum frequency of input signal Fmax from [2].

Fsamp > 2Fmax **eqn(1)**

1.3 WHY WE NEED CONVERTERS?

In modern automation world it is necessary to get data which is understandable by the computer. It is possible only when we converter the natural signal to digital the sensors also converter the signal in to system understandable language.
Ex: temperature can be convert b thermostat or b temperature sensor.

The electronic system, signal processing and storage performed in digital format for these ADC are required. In Cmos technology has the dramatically improve the system performance, in digital domain the unwanted interferes and noise will be reduced compared to analog domain. The data converters required the upstream of data or high sampling rate converters.
The ADC is required for the further high electronic systems like radio's software, image sensors, Bio-medical and wire-line communication and other applications. There are many ways to convert natural signal to bit stream. The bias value may produce zero quantity. It is

measured and removed by electrical network. This will null at zero the input signal ma not be linear with respect to the quantity being measured. Sometimes it may be logarithmic or exponential amplifier to correct the signal from non-linear nature a converter may takes into account

1.4 RESOLUTION

Number of bits used to represent the sampling or input signal is called resolution

Ex: we choose to digitize the input 8-bit that means we match the analog signal with 2^8=256 possible level. If ADC works properly then the digital estimation of analog input can be worst and be wrong by LSB. On average the error is half of these is called resolution.

1.5 QUANTIZATION ERROR

The mapping of a huge number of sets of input to smaller set by using different techniques such as rounding is known as Quantization.

In ADC the difference between analog and digitized value referred as quantization error or distortion. It is defined as –(1/2)LSB to +(1/2)LSB.

The signal to noise ratio for an ideal is defined as[2].

$$SNQR=20\log10(2Q) \qquad \text{eqn(2)}$$

Q is quantization bits

Quantization error is Qe=Efsr/(2^n-1)^2 eqn(3)

B increasing the no of bits results in the finger resolution and quantization error. Quantization error can be observed b continuously sampling a typr varying analog signal with ADC and converting back to DAC .the difference between the two signal is known as quantization noise. The root mean square of this signal is[2].

En=Efsr/(2nsqrt12) eqn(4)

En is cut in half

1.6 OTHER PARAMETERS

The ADC is required in the sensor for accurate and speed response .the sensor may suffer from response effect and also due to speed of response. So that it gives error signal also noise at the output signal. These output electrical signal values are different from actual signal values. These ADC may get different errors due tto quantization noise.

The factor required for the ADC are current source, comparator and error sources. The output impendence may be finite in non-ideal current source in such situation current will depend on output voltage. Because these produce non-linearity to the entire ADC, these will reduce non-linearity below the accepted level and impose by ADC resolution.

The comparator plays a major role in ADC its resolution must be smallest than ADC resolution with reasonable speed to get min delay of comparator this will effects the counter measure time.

These is one fact that input common mode voltage varies from different level of input sample.

1.7 TYPES OF ADC'S

Mainly the ADC are divided into two types.

1) Nyquist Rate ADC'S,

2) Oversampling ADC'S

Based on the application different ADC will be chose

Low-to-medium speed, High Accuracy	Medium-speed, Medium Accuracy	High Speed Low-to-medium Accuracy
Oversampling ADC	SAR(Successive Approximation)	Flash, Pipelined, Time interleaved

Table 1: Different A/D converter Architecture

Nyquist Rate ADC are

i) SAR(Sucessive-Approximation ADC)

ii) Flash ADC

iii) Pipelined ADC

i) SAR (Successive-Approximation ADC)

It iis one of the most popular ADC architecture. It will provide quick conversion time or for high accuracy with low power it can be operated.

It require a single comparator and large number of capacitors with switches and small amount digital control logic. It works on Binary search Algorithm.

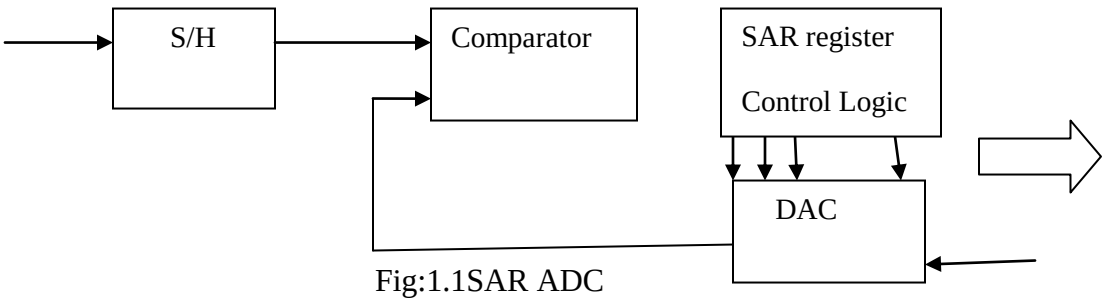

Fig:1.1SAR ADC

ADVANTAGES:

- It uses only one comparator.
- Low power consumption.

DISADVANTAGES**:**

- The DAC grows with the number of bits.
- They take as many cycles to convert the signal as the number of bits.
- The components mismatch in the DAC limits its linearity to around 12 bits.

ii) PIPELINED ADC

It is similarly to SAR ADC and algorithmic converter. It perform iterative search for digital code which reflects accurate input analog signal. These converter have separate analog stage dedicated for each iteration

Each clock cycle it operates on different input sample and hold it perform N iterations simultaneously. It is N-time faster than algorithmic converters. It is used when higher

speed is required compared to algorithmic converters' bit input samples re processed in parallel. There is N clock cycle latency for pipelined converters fig [2].

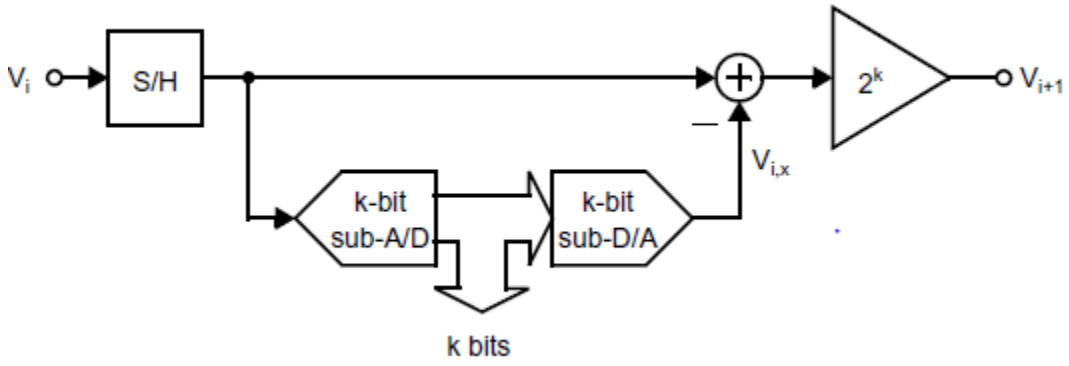

Fig-1.2 N-bit parallel pipelined ADC [2]

ADVANTAGES

- The number of stage will increases only with the number of bits.
- As fast as the Flash ADC

DISADVANTAGES

- High latency.
- An error introduced by doubling or subtraction operations passes to following stages**.**

iii) FLASH ADC

It is used for the realization of high speed converters. It required 2^N comparators in parallel, every comparator is connected with different node of resistor string. Every node connected to resistor string Vref which is greater than vin.

ADVANTAGES :

- Very fast,
- Converts instantly
- **DISADVANTAGES:**
- It doubles the size for each bit added to the representation .
- It consumes a lot of power

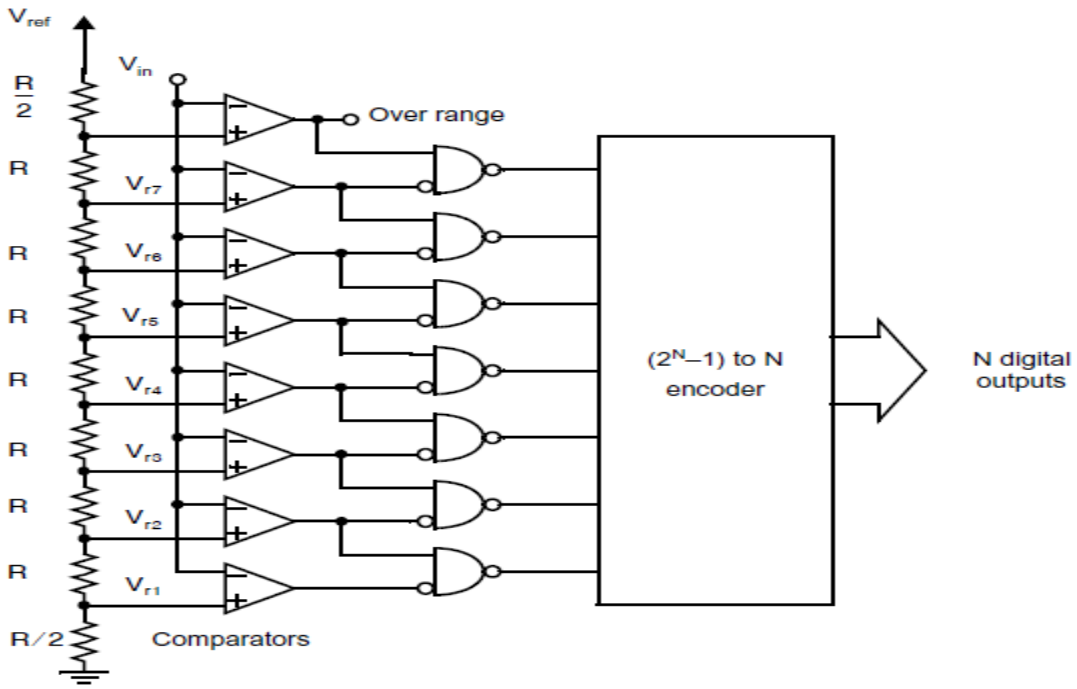

Fig -1.3 3-Bit Flash ADC [2]

2) OVERSAMPLING ADC

The sigma Delta ADC is most popular as the Oversampling ADC due to its oversampling property it's circuit is does not required of the anti-aliasing filter. The name oversampling came to the data converter due to its property it perform the sampling rate of the input signal more than the Nyquist rate frequency. Due to this property it does not required the low pass filter in the circuit.

The Sigma-Delta ADC is consists of the summing amplifier, integrator, comparator or quantizer, D Flip-flop or Decimation or digital filter and for the feedback path it required the DAC. In the higher order the Sigma-Delta ADC are more stably and gives the linear output due to its property of high resolution it mostly used in the Bio-medical applications.

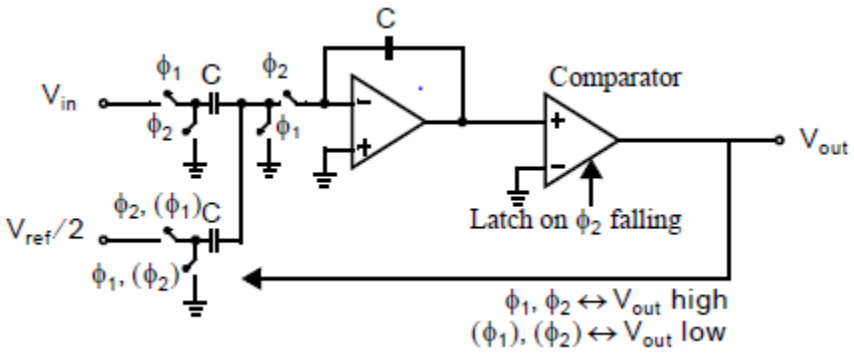

Fig-1.4 1-bit Sigma-Delta ADC [2]

ADVANTAGES

- Due to large oversampling the quantization noise spectral density is reduced.
- Very simple output.
- It allow the noise shaping.

DISADVANTAGES

- Requires the decimation filter in the end.
- Only useful in applications requiring low sampling rate, such as audio.

1.8 Types of Delta-sigma ADC

There are two types of Sigma-Delta ADC

1) Continuous Time Sigma-Delta ADC
2) Discrete Time Sigma-Delta ADC

Both the Continuous Time and the Discrete Time Sigma- Delta have the same building blocks. They are different based on the loop filter characteristics. Discrete Time ADC the loop filter is implemented with the Switched-Capacitor circuit and the Continuous Time loop filter is implemented with the RC or LC circuits.

Both the Continuous Time and the Discrete Time ADC takes the Continuous Time or Analog Signal and give the output Discrete Time Signal. In Discrete Time the input signal sampled by the modulator before the loop filter and the process of aliasing need for the anti aliasing Filter. The Discrete Time filters use the switched Capacitor input stage of the Filter. In the Continuous Time the Continuous Time signal is applied to the Filter without the need anti-aliasing Filter.

There are two type of structures are available in the sigma Delta ADC they are

1) Feed back Structure
2) Feed Forward Structure

Mostly based on the application where we are using the ADC depend on that the Structure will be chosen by the designer. The Continuous time ADC will be mostly used for the

communication purpose in the mobile communications, radar communications, for Audio Transmissions etc..,

While the Discreet Time and the feed forward is used in the applications of the Bio-applications which consumes the low power due to its structure as the order of the sigma delta ADC changes the structure also changes the structure of the ADC will also changes where the power consumption will change and the usage for the application will also changes based on the changes.

CHAPTER 2

SCOPE OF THE STUDY

2.1 INTRODUCTION

In the Bio-medical application ADC play a major role in many applications. Due to the high-resolution and the linearity of the signal with the added advantage low-power technique the sigma-Delta is well suited for the many applications not only in the Bio-medical applications but also in many other application the Sigma Delta ADC place a major role in audio amplifiers . data storages and in many.

At present the Bio-medical electronics in health care industry has gained the significant role. These ADC are becoming the wide spread using in diagnosis of diseases and in many other applications these are using like cardiac pacemakers, Image sensors, for the Cardiac Arrhythmia, to implants deafness or retinal implants for the blindness. These ADC also useful in the brain machine to interface for the paralysis.

Compared to other traditional ADC technique this sigma-delta is most useful in the Bio-medical applications. It is used to implantable device for detection of sensitive signals from the heart or Brain. These required the low power devices which is portable.

By integration of the Analog front end and Backend we can achieve the low power consumption with digital processor in the same chip.

In the Sigma-Delta ADC we can achieve thee linearity of the signal by using the higher order modulator with these type of modulators we will get the power efficacy at lower supply voltage. The integrator and the comparator plays a major role in sigma Delta ADC the first integrator will consume the much power to reduce these and to attain the low-power consumption the

switched capacitance technique for the integrator and the comparator will reduce the maximum power .To attain the more linearity and the low power here we used the Charge pump Integrator instead of the Switched capacitance integrator. By using the Charge pump integrator the power consummation of the circuit has been decreased and signal to Noise Ratio has been increased.

2.2 ULTRA-LOWPOWER DESIGN IMPORTANCE

In the bio-medical applications we required the portable and low power devices. Due to the low power the design can be operate for the long time without an recharge .The heat dissipation also important point to be consider

In few application like retinal after the implant of the sensor in the body we cannot rechargeable it even with the wireless charge or we cannot perform the operation to recharge the device always. so once the device is implanted it should work for many years,

CHAPTER 3

OBJECTIVES OF THE STUDY

The main object of this thesis is to design Sigma-Delta ADC for Bio-medical applications with high resolution low-power consumption with improved SNR

In sigma-delta ADC gain of the op-amp plays a important to get overall gain of the Sigma-Delta ADC so here we are using the single stage Operational Transconductance amplifier for the large gain of the ADC. The integrator is the main power consuming device so here by using the technique Switched Capacitance we reduce the power consumption of the circuit.

To design the low power Sigma-Delta ADC we have to reduce the power of the ever device using the different technique. By using the same technique for the comparator we can further reduce the power dissipation of the circuit.

By reducing the power of the ADC we can reduce the power consumption of any circuit which inherits these ADC Ex: In Bio-medical applications mostly these Sigma-Delta ADC are used to convert the signal in Cardiac Arrhythmia, or in any applications like to implants deafness or retinal implants for the blindness these we can't recharge every time or we can't charge it with wireless process also. For these for charging this equipment we can't perform the operation .By using the low power applications only we can make these to work for the long time after the implanting of the object these can be attain only b using the low power applications.

CHAPTER 4

LITERATURE REVIEW

Ichiro Fujimori et al. 2000[5] proposed a 16-bit 2.5 MHz output rate Analog-to-Digital converter for wire line communications and high-speed instrumentation has developed. A 2-1-1 cascaded Delta-Sigma modulator using 4-bit quantize in every stage makes all quantization noise negligible 8*OSR (over sampling ratio).The tone generated by multi bit DAC (Digital-to-Analog Converter) with data weighted averaging with bidirectional rotation.

The front-end sampling distortion is reduced by using the low-Threshold transistor in switched capacitance technique. This modulator achieves the 90db SNR (Signal-to-Noise Ratio) in 1.25 MHz bandwidth and 102-db SFDR with 270-mW power dissipation. This ADC successful integrator the decimation filter no SNR (Signal-to-Noise Ratio) degradation due to digital switching noise has been observed.

Gil-Cho et al. 2005 [7] proposed a 0.6v 2-2cascaded audio Delta-Sigma ADC(Analog-to-digital converter).By using a resistor based sampling technique to achieve high linearity and low-voltage operation without device subjecting to large terminal voltage. By reducing the sensitivity to op-amp (operational amplifier) distortion it enhanced the linearity b using the low-distortion feed-forward topology combined with non linear local feedback.

This modulator achieves 82-db Dynamic range and 81-db SNDR (Signal-to-Noise Distortion Ratio) with OSR of 64 b using a weighted audio-signal bandwidth. Power consumption of modulator is low 1mW from 0.6v supply. The overall linearity of the modulator is enhanced b applying low-distortion feed forward topology.

Min Gyu Kim et al. 2008 [3] proposed a new method using a combination of switched-RC technique and a floating switched capacitor double sampling configuration enabled low-voltage operation without clock boosting to improve the linearity a three level quantizer a simple dynamic element matching was used to improve linearity a three level quantizer a simple dynamic element matching was used to improve linearity. With this double-sampling technique we can double the OSR as compared to conventional design without extra power consumption and without increasing the clock frequency. The result of this technique is to achieve low-voltage low-power and high performance accuracy.

This prototype IC includes the op-amp with a low –voltage CMFB circuits a low voltage quantizer circuit and low power DEM for three-level quantizer

Youngcheol Chae et al. 2009 [6] this paper explains about the inverter based SC (Switched-Capacitance) Circuit and application to low-voltage low-power Delta-Sigma modulator. To implement a pacemaker cmos image sensor a three inverter-based Delta-Sigma modulator.

The modulator-I achieves 65db SNDR for 120 Hz bandwidth consuming 0.73uW with the supply voltage 1.5V

The modulator-II achieves 320-channel parallel ADC 65db SNDR for 8 kHz bandwidth consuming 5.6uW for each channel with1.2v supply.

The modulator-III achieves for an audio-codec achieves 81-db SNDR with 20 kHz bandwidth consuming 36uW and 0.7V power supply. This prototype achieves high power efficiency with same performance in particle applications.

Ali Agah et al. 2010 [8] proposed a calibration-free, high-resolution analog-to-digital converter designed for a Bioluminescence sensor array employs incremental sigma-delta modulator. The

resolution of the prospered modulator can be improved significantly by means to technique similar to extended counting. Two step process in which the residual error from a second-order incremental sigma-delta modulator is encoded using SAR ADC.

By maintaining a one-to-one mapping between in individual input and output samples. It is possible to enhance the static linearity and to enhance resolution.SAR ADC is used to digitize the residue of a second order incremental sigma-delta modulator.

Tao Wang et al. 2010 [1] proposed a low power switched capacitance integrator for high resolution delta-sigma ADC compared to conventional switched capacitance integrator. These achieve much low-power dissipation for the same noise specifications.

By using the third order delta-sigma modulator the effectiveness of the new integrator is compared with conventional integrator .The low power integrator was described which uses voltage multiplication.

Chien-Hung Kuo et al. 2010 [4] discussed about the low voltage fourth-ordered 2-2cascoded delta-sigma modulator using the double sampling switched-operational amplifier.

The SOP (Switched-Op-amp) is designed to reduce the power consummation of the modulator. In these paper two second order delta-sigma modulator with a cascaded integrator input feed forward structure to reduce the output of the first stage is directly connected to the second stage to simplify circuit design

The double-sampling switched op-amp based integrator is also adopted to reduce the applied clock frequency by half. The minimum requirement of slew Rate can be evaluated b supply voltage overdrive feedback factor and operating frequency which is helpful to the design of modulator. It is also validated from the result measurement results of a 1-v forth order delta-sigma modulator

CHAPTER 5

METHODOLOGY&PRESENT WORK

5.1 SIGMA-DELTA ADC

In the Sigma-Delta ADC the integrator plays a main role to improve the power and the linearity of the Signal. The First integrator used here will consume the more power when compared with the any module of the circuit so by replacing the Switched capacitance integrator with the Charge pump Integrator here we attain the low power and the High Signal to Noise ratio when compared with the pervious Switched Capacitance Circuit. The total circuit consists of the Summing Amplifier, Charge pump Integrator, and Quantizer.

1.Summing Amplifier:

The summing amplifier is designed by using the OTA(operational Transconductance Amplifier) which gives the more gain and low power. The summing amplifier which will do the summing of the two signal which will consists of the input and the feedback signal from the output of the quantizer. The circuit design is given below.

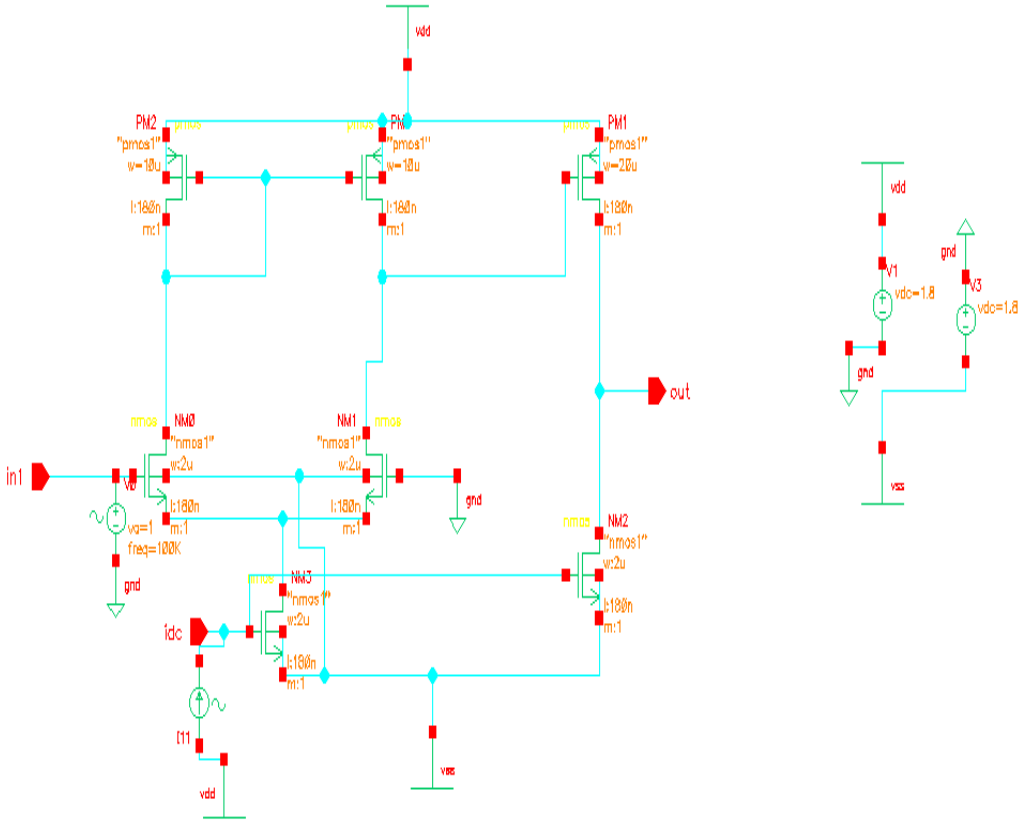

Fig:- 5.1 Operational Transconductance Amplifier

2.Charge pump Integrator:

The charge pump integrator which integrate the given signal and gives the amplified signal. The integrator here which will give the high power signal as the output with the help of the OTA in

the circuit. Here for the integrator we uses two clock signals for the switching activity to convert the analog signal into the discrete signal with some amplification of the signal.

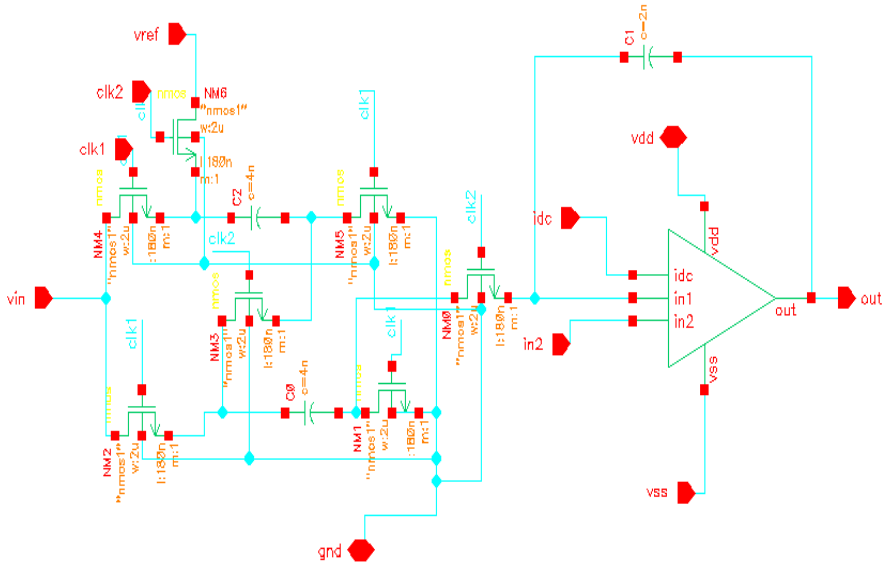

Fig:-5.2 Charge Pump Integrator

3. Quantizer

The quantizer is consists of the comparator and the latch the comparator which compare the signal with the reference voltage the latch which convert the signal into the level based in the sequence pattern. The circuit diagram of the Quantizer is below.

The comparator will consists of the two inputs the First input here is connected with the output of the Summing amplifier which is connected in the design after the 3rd Integrator n the feed forward structure.

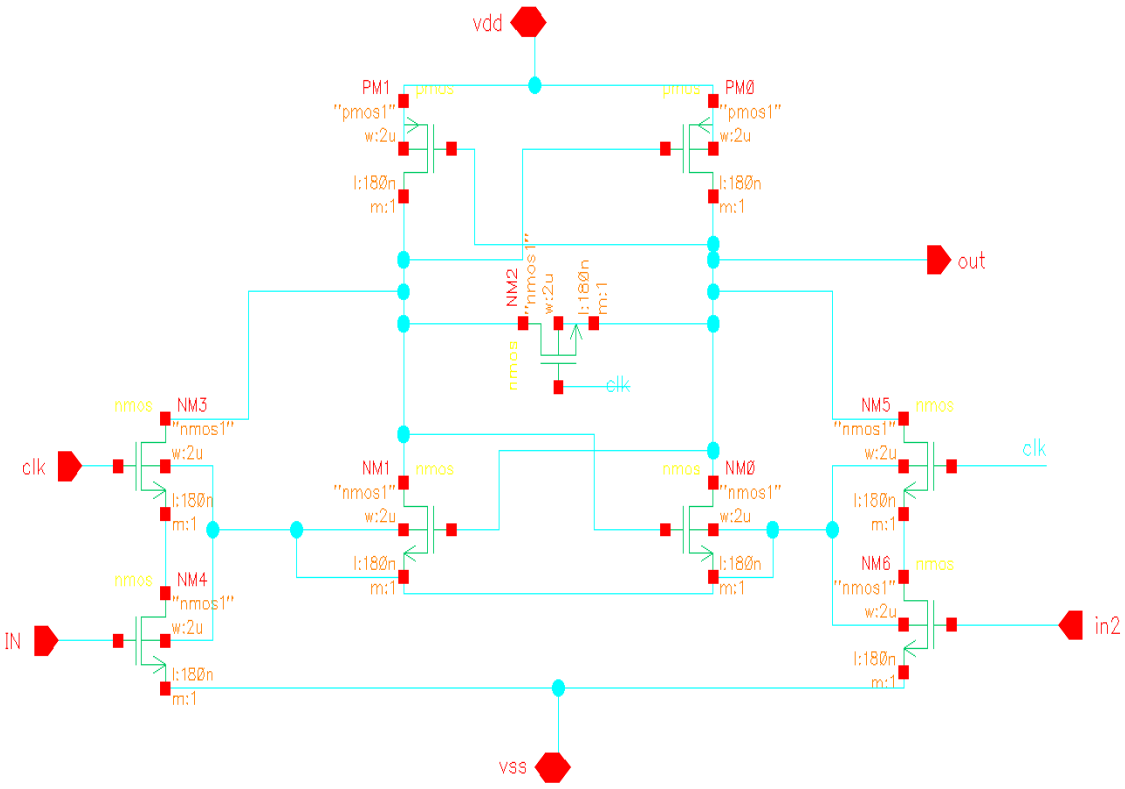

Fig:-5.3 Comparator

The D Latch the functionality of the D-Latch is same it is a level trigged here we are using the Latch for the reference of the clock and for the output signal.

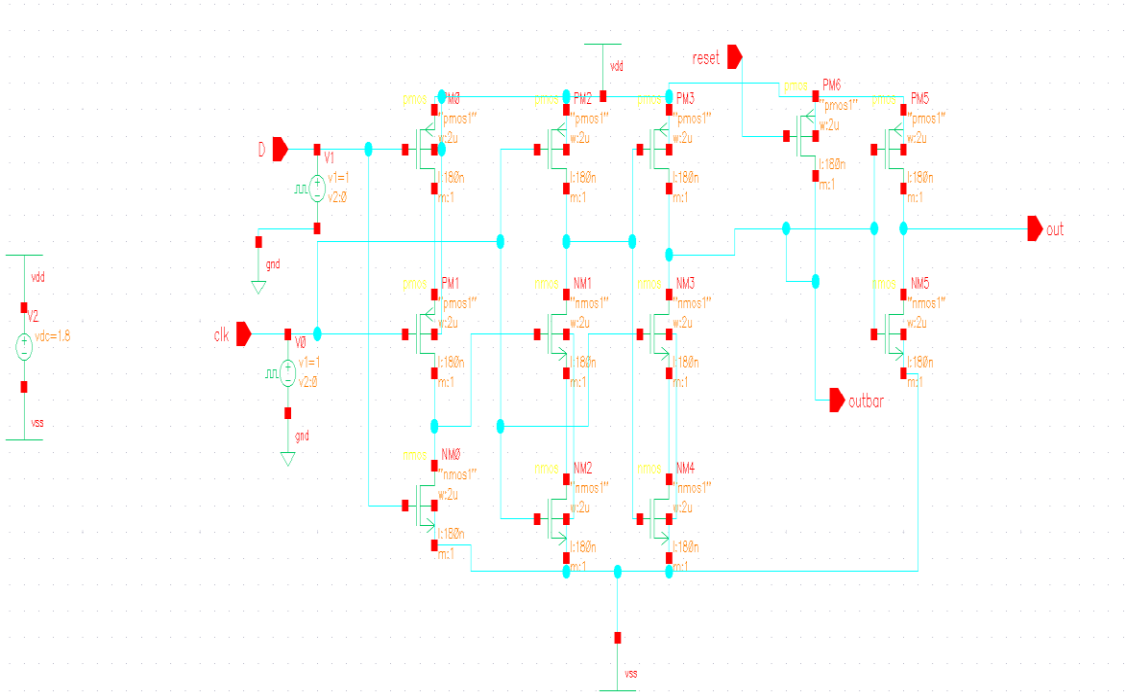

Fig:-5.4 D-Flip-Flop

4.Sigma-Delta ADC:

The Feed-Forward Structure of the Sigma delta ADC which the power consumtion is low when compared with the Feedback struccture the delay will be reduced the linearty of the output signal is increased and the signal to noise ratio of the signal also.

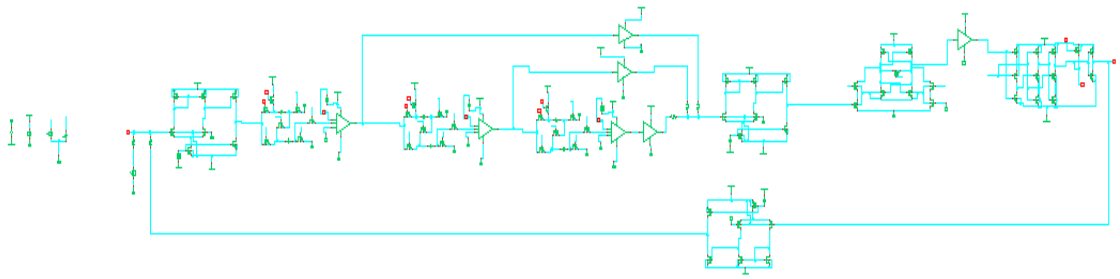

Fig:-5.5 FeedForward Sigma-Delta ADC

CHAPTER 6

RESULTS AND DISCUSSION

6.1 OUTPUTS:

OTA Output:

The figure which is below is the output of the OTA(operational Transconductance Amplifier).It shows the Transient Analysis and the gain of the OTA which is 45db.wwhiich will be operated at the frequency of thee 10M hz with the supply voltage of 1V .

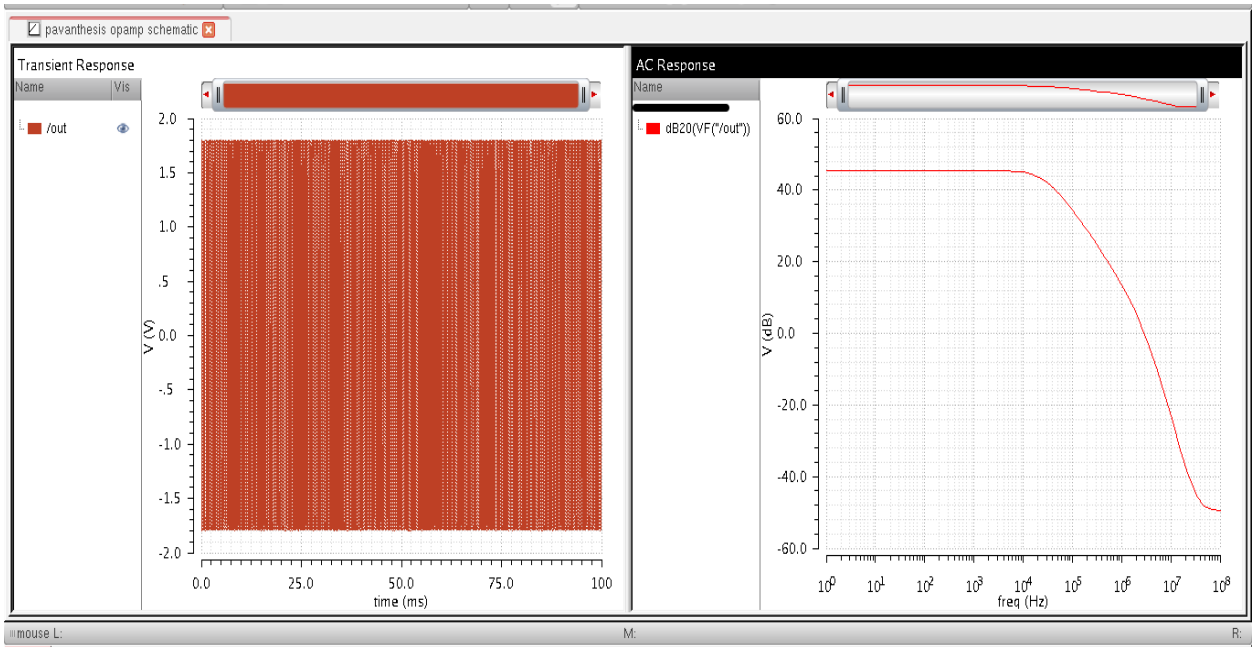

Fig: -6.1 output of operational Transconductance amplifier

Output of Integrator:

The integrator output which integrated the given sinussodal signal with the with the feed back and the second input is of theis which is connected to the ground has been integrated here and changed the signal into thedigital for due to the switches present in the input side of the integrator the output signal is also amplified due to the presence of the OTA in the integrator.

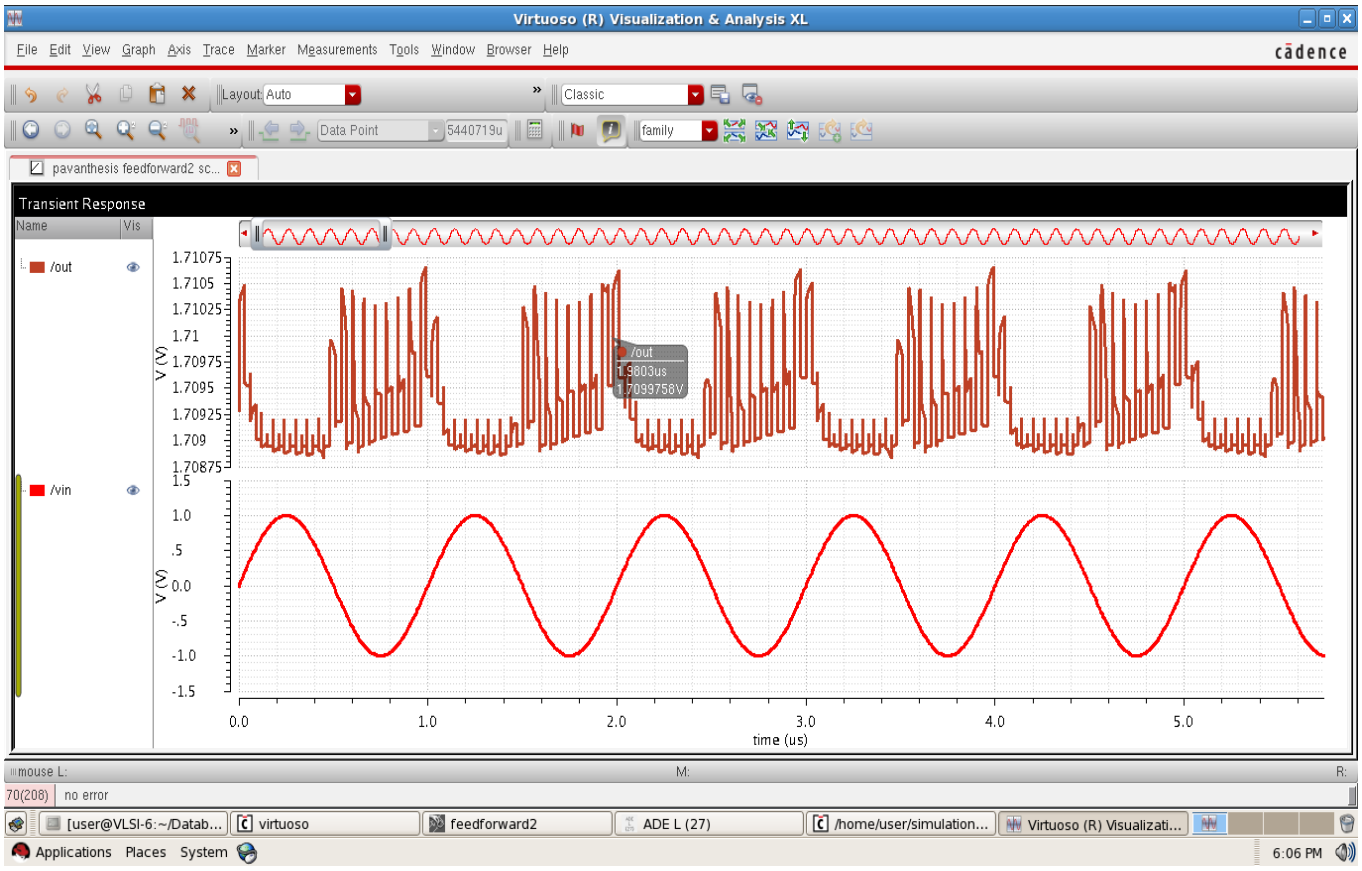

Fig:- 6.2output of low power charge pump switched capacitance integrator

Output of Comparator:

The output of the integrator will be given as the input for the comparator the comparator and the second input of the comparator is grounded which will compare the first input with the second input of the comparator to attenuated output without any glitches there and the amplified output.

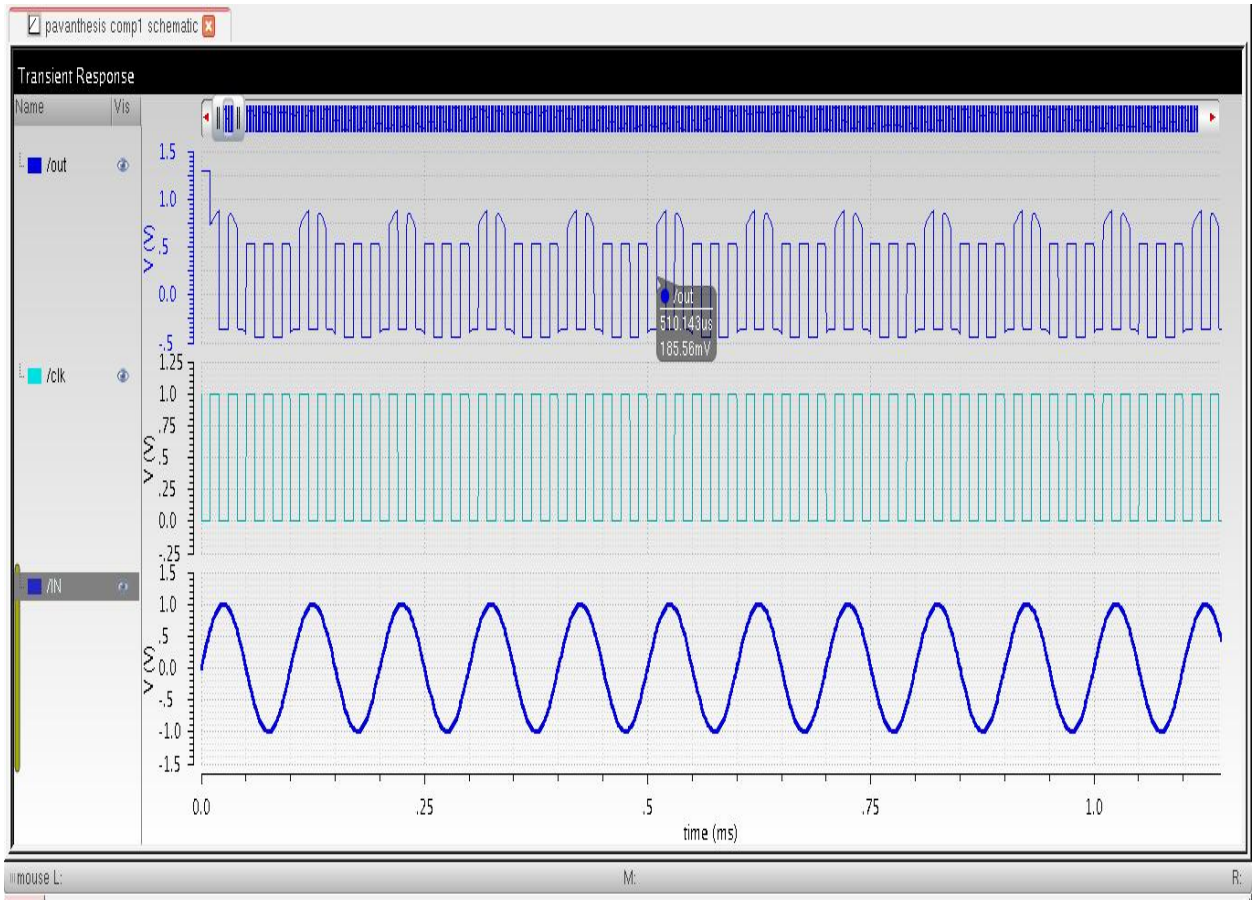

Fig:- 6.3output of comparator

Output Of D-Flip-flop:

The output of the D-Flip-flop which change the reference of the clock frequency. The D-Flp-flop which is well know as the delay Flip-flop

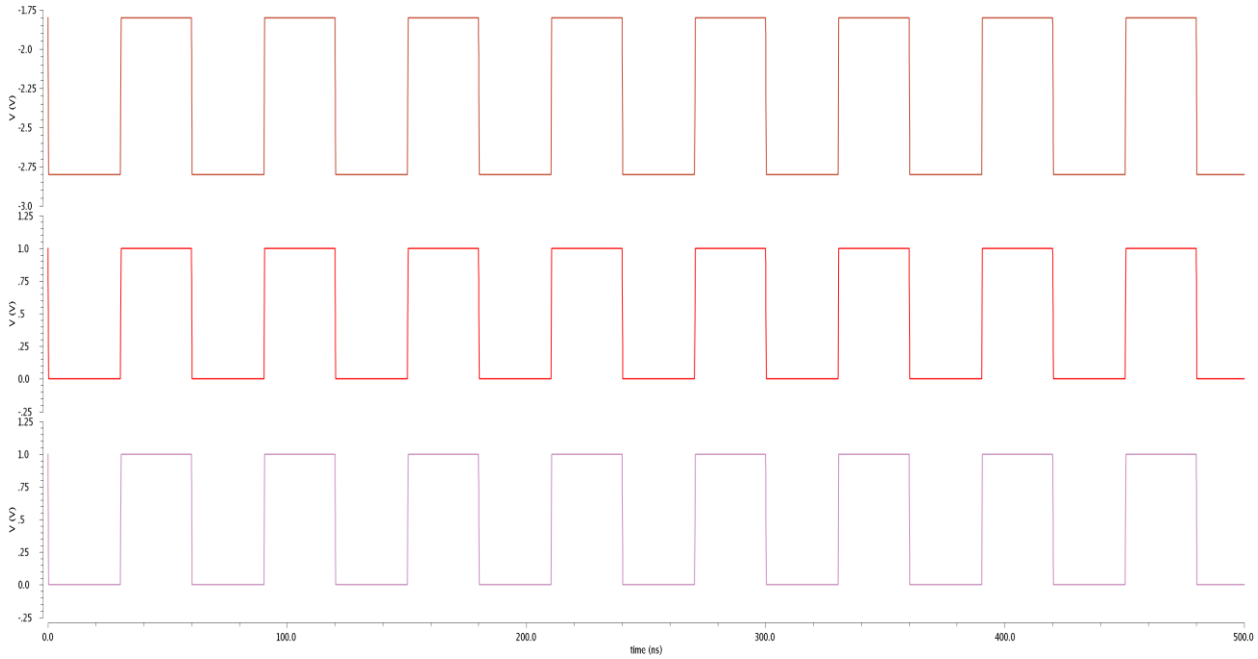

Fig:-6.4 Output of D-Flip-Flop

Output OF ADC:

This is the over all output of the feed forward Sigma Delta ADC which converted the given input signal into the Digital form with the low power consumption of 2mv and the sigal to noise ratio has been gained up to the 60db .

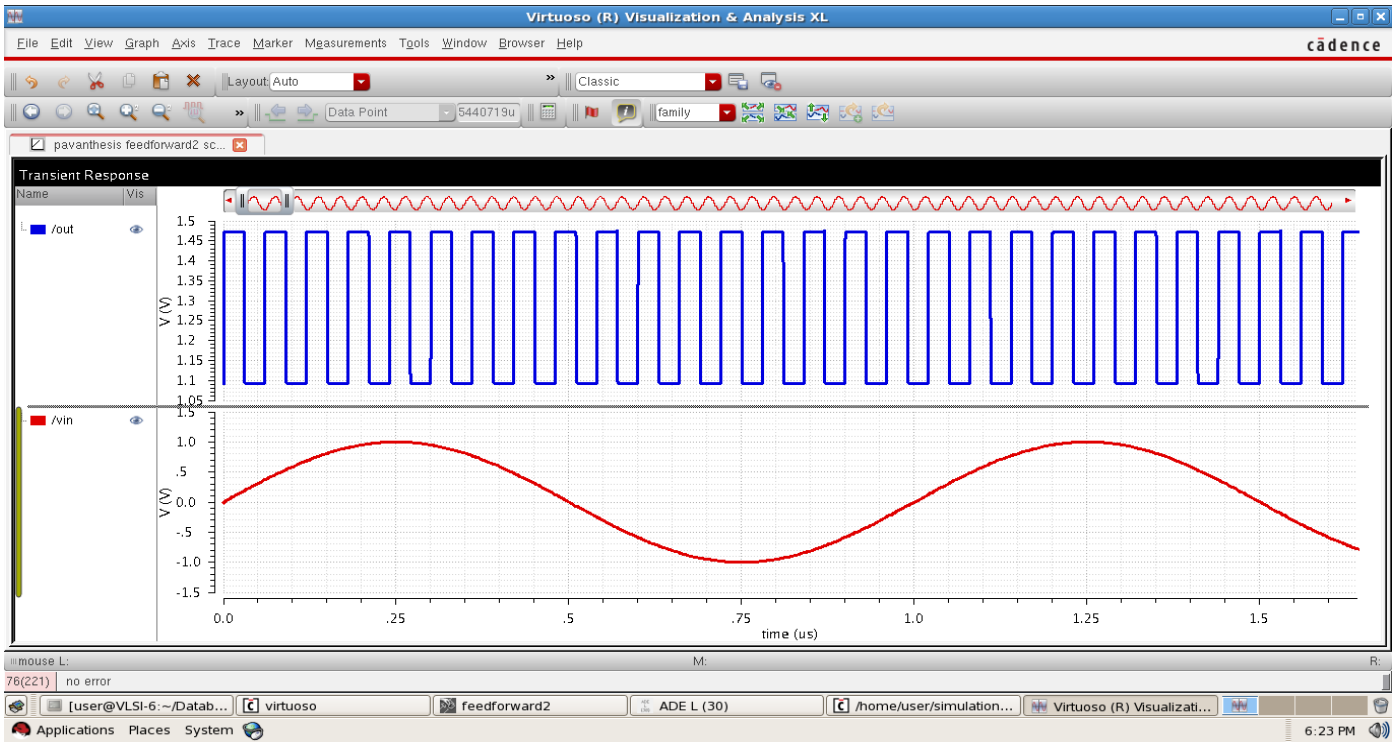

Fig:-6.5 Output Of 3rd order Sigma-Delta ADC

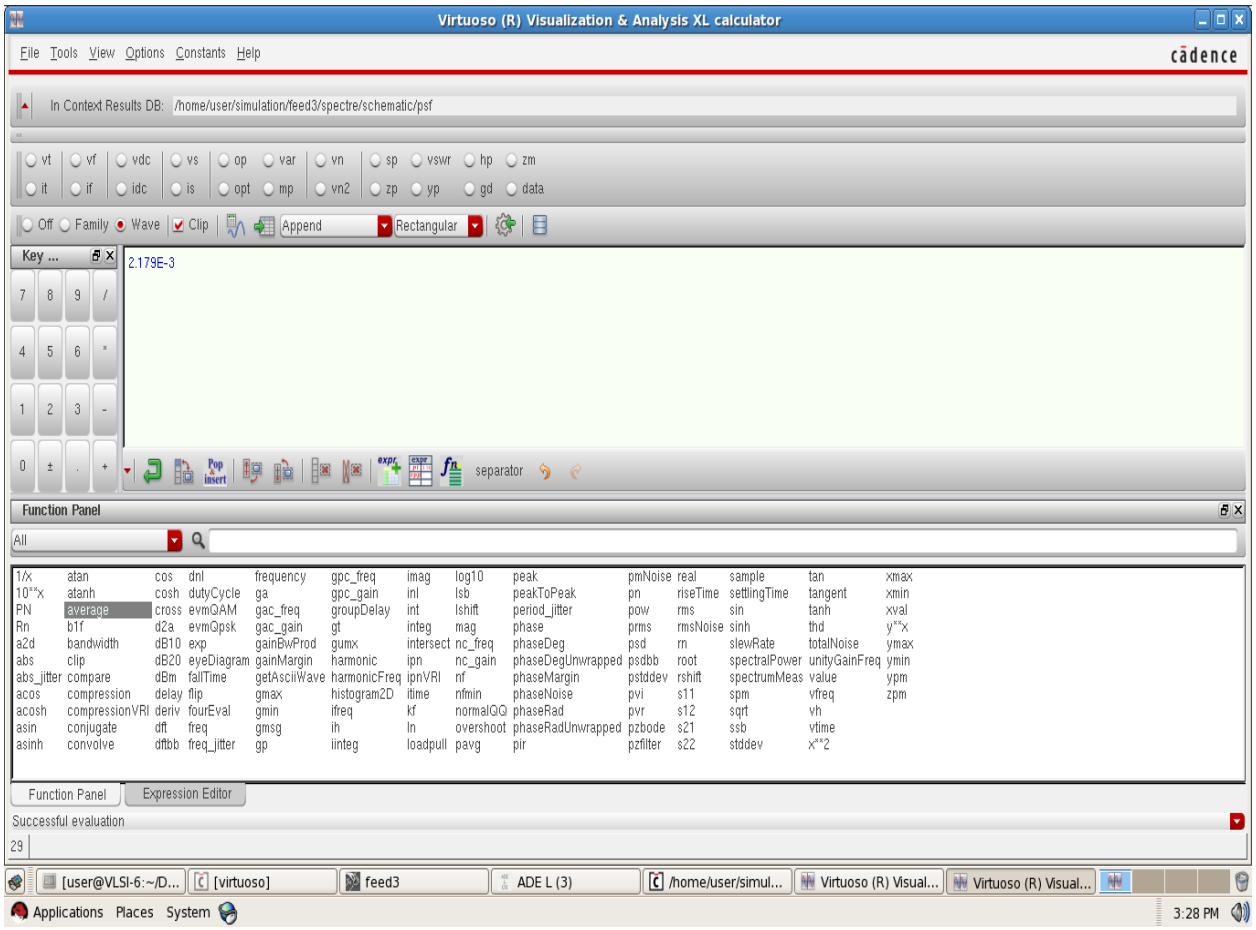

Fig:-6.6 Output Of 3rd order Sigma-Delta ADC power consumption

CHAPTER 7

CONCLUSION

Most Sigma-Delta ADC is most useful in many applications due to the oversampling property when compared with the other traditional ADC. So we are using these in the bio-medical applications.

In the discrete time delta sigma the OTA and the integrator are the main power consuming devices. To reduce the power consummation and to attain the high gain of the ADC we are using the OTA with technique switched capacitance op-amp and the switched capacitance integrator. In higher order the first integrator will consume the more power. By using the OTA instead of the op-amp we can attain large gain and the bandwidth. Even though there are many techniques like double sampling-Rc. With the help of the SC only we can attain low power dissipation.

Even by using the same technique for the comparator we can reduce more power consummation. For the multi bit (High resolution) we use the traditional ADC and the Decimation Filter or the digital filter.

The Sigma-Delta ADC with the Charge Pump Integrator consume the low power when compared with the Switched capacitance integrator and give the high signal to noise ratio which will be more useful for the Bio –Applications where low power and high linearity.

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