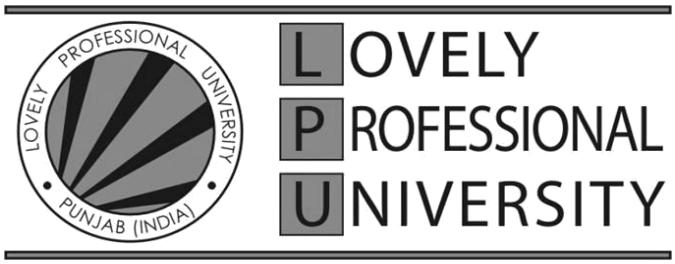

"DESIGN AND IMPLEMENTATION OF ANALOG ALL PASS FILTERS"

A Dissertation

Submitted

By

K .P. MANJUNATH
(11306922)

To

Department of Electronics and Communication Engineering

In partial fulfillment of the Requirement for the

Award of Degree of

MASTER OF TECHNOLOGY

IN

VLSI DESIGN

Under the guidance of

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Lovely Professional University
Phagwara-144402, Punjab (India)

(April 2015)

CERTIFICATE

This is to certify that **K.P.Manjunath** has completed M.tech dissertation titled **"DESIGN AND IMPLEMENTATION OF ANALOG ALL PASS FILTERS "**under my guidance and supervision. To the best of my Knowledge, the present work is the result of his original investigation and study. No part of the dissertation has ever been submitted for any other degree or diploma.

The dissertation is fit for the submission and the partial fulfilment of the conditions for the award of M.tech in VLSI Design.

Date:

Signature

TEJINDER SINGH
Assistant Professor
School of Electronics Engineering
Lovely Professional University
Date:

DECLARATION

I hereby declare that the Dissertation-II report entitled **"DESIGN AND IMPLEMENTATION OF ALL PASS FILTERS"**, is an authentic record of my own work carried out as the requirements for the award of degree of Master of Technology in VLSI Design at Lovely Professional University, Jalandhar under the guidance of **Mr. Tejinder Singh,** Assistant Professor, Department of Electronics and Communication Engineering, during January to May, 2015.

Dated:

K.P.MANJUNATH

(11306922)

Objective of the Dissertation-II is satisfactory / unsatisfactory

Examiner I **Examiner 2**

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This is a humble effort to express my sincere gratitude towards my mentor who has guided and helped me to explore the field of Analog Signal Processing, which is the base of my Dissertation undertaking.

Problem formulation is a major milestone for a student while working on Dissertation. As such this subject was a challenge for me and was an opportunity to prove my calibre. Being a beginner, I faced many problems, which would have frustrated me. I am highly grateful and obliged to my mentor.

It would not have been possible to see through the undertaken field of study without the guidance of Mr**. Tejinder Singh.** It was purely on the basis of his experience and knowledge that I am able to clear the theoretical and technical hurdles during the analyses and exploration of the selected field of study.

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ABSTRACT

The thesis focuses mainly on well efficient model of high frequency range, low power and high stability all pass filters. In vision of the modern communications there is a progressive development in the signal transmission techniques in sight of the contemporary methods arise to transference the signal from source to destination by means of the transmitters and receivers, as the par expansion of these systems is more, transreciever has to be replaced both and in designing such complex model a number of suitable considerations are come into account like filtering the signal and passing the signal form Hz to several GHz mainly for the RF, military application and also for wireless communications. To accomplish the task for building an effective such a novel design is required for the processing and passing the sustainable measured quantity without any loss of the information and its characteristics are to be analysed for the accuracy and efficiency.

In context of these a physical variable is needed for such type of realizations, and from these aspects an all pass filter design here provides all the features like gain, stability and phase, The implementation of the all pass filters is worked out with different methodologies and the selection of the topology for the high range frequencies are somewhat critical to validate. The models proposed accompanies the ideal characteristics of Analog all pass filter such as unity gain, high bandwidth and 180° phase shift over the band of frequencies with supressed noise and high efficiency.

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List of Abbreviations

1.	**AP**	All pass
2.	**TF**	Transfer Function
3.	**CM**	Current Mode
4.	**CT**	Continuous Time
5.	**VM**	voltage Mode
6.	**CFOA**	Current Feedback Op-amps
7.	**ASM**	Analytical Synthesis Method
8.	**DDCC**	Differential Difference Current Conveyors
9.	**DDCC**	Differential Difference Current Conveyors
10.	**CCII**	Second generation Current Conveyor
11.	**DXCCI**	Dual-X-Current Conveyor of second Generation
12.	**DVCC**	Differentials Voltage Current Conveyor
13.	**DOCCI**	Dual Output Current Conveyor

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CHAPTER-1

INTRODUCTION

At present in the trends of technology, in the context of signal transference Analog signal processing plays a crucial role in the communication for the signal processing. The possibility for choosing a physical variable, such that it effects mainly and each signal with a dense time and amplitude for the continuous processing cells. In the design of filter configuration in the past many topologies are mentioned to state the behaviour of the signal in the context of signal carrier.by taking all the stated models of all type of the filters an all pass filter is designed and implemented by taking all the feasible characteristics of a transistor with more efficient transmission. In this thesis the design of all pass filter design carries a different terminologies like compound transistor, Tran's linear loops and differential par combinations to perform the all desirable characteristics of a filter using an electronic precise function.

To estimate the behaviour of the filter mainly a transfer function is defined to form a well efficient model for the implementations. In the VLSI mainly a model proceeds with the features like low power low area with high efficiency but in analysing such precise factors the complex function is to derived and solved, here the filter is well implanted by taking account the filter function and realising it with necessary modifications and from the modified function the order and representation is made in all aspects. As the technology is advanced many filters are concluded with the advance tools with specific algorithms in these algorithms clearly mentions the function and the behaviour and comprises many analytical calculations and furthers refers a feedback to modify our design and move with the higher orders.

In an Analog signal processing first order electronic function has a wide range applications and signal generation in a network that is classified in the section of "filters". The term all pass filter evolves from the filter phenomenon where it is called as phase shifter and amplitude preserving feature which has its "former name" and the latter name called as frequency-dependent phase shifter. These two features combined together and gives a powerful electronic function which has extensive applications that ranges from the simple phase equalizer otherwise referred as phase shifter to more complex ones with signal generation of quadrature and multiphase outputs by this higher order filter functions are realised by the simple electronic function.

It gives an adequate view for these type of applications and implemented structures proceed with the plain computations. Some tasks are there in which entire electronic industry is most successful in aiming the required results for quite different category of tasks that corresponds to the technology with a continuously changing environment. To overcome these changes a flexible and rigid systems are designed for many applications mainly in the field of defence, communications, T.V broadcasting and bio-informatics and many Analog signal processing blocks.

In considerations to high-performance active elements, current-conveyor suits much better, such that the first order All-pass filter has a more prominent in the modern communications and in the field of instrumentation systems. It offers many desirable characteristics like High accuracy, Wide bandwidth and high slew rate in addition to this low voltage and low power implementations with current conveyors makes an ideal choice in Analog signal processing for modern applications

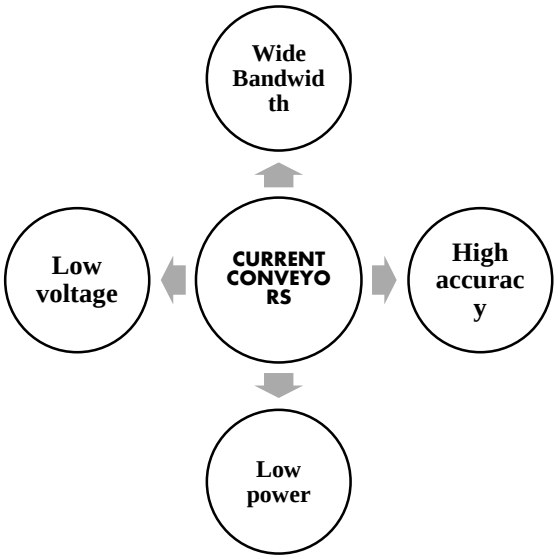

Figure 1.1 Current Conveyor usage in all pass filters

In the progress of the all pass filters the usage of the current conveyors are compulsory as it holds many useful applications in regards with supply voltage for the peculiar systems with High accuracy, where as its usage is mere in the fields of radio frequencies the design should be compatible with the noise and power consumptions.

CHAPTER-2

SCOPE OF THE STUDY

2.1 ANALOG IMPLEMENTATION:

In any works of implementation mainly VLSI circuits are considered as the best suitable regarding the implementation, especially in regard of size, power consumption size are concerned. By estimating all these parameters an Analog implementations are required to know how efficiently of small-area processing cells can be implemented in an opportunistic manner. With regard of the features of available components, with respect to the transistor that allows massively parallel architectures that are developed to carry out the collective processing on real-time signals. These architectures are derived from the systems which fulfil the requirements to develop a new proposals .In regard of my work an Analog implementation, seems to be an ideal medium to develop a new hypothesis

FILTERS

Filters are main necessary blocks in the communications for several applications for filtering and the removing the unwanted bands in the transferred signal and processed signal and the main role of the filter is to extracting the specified band of frequency and filter it in respect to noise and other primary specifications. In comparison to Analog filters with the digital filters the Analog filters adds some features in regard of frequency phase and gain, but in the design of the Analog filters the main perception is the topology selection and implementation with low supply voltage and low area, whereas in the Digital filters the chance of occurrence of the noise is less. So the design of the filters needs all the factors to withstand all the characteristics that affect the behaviour of the signal and the Filters function is to eliminate the random noise.

A.Digital -Filters:

In the concern of digital filers it holds mainly ADCs (Analog-Digital Converts) with programming software that is embedded in the microprocessors .Here the main lag will be following by the time constraints due to clock timings in the system and at peculiar points the power may increases due to delays. In view of some high performance devices mainly in FPGA and DSP processor kits a parallel architecture is made for filtering the input summations, but these are quite complex for the digital filters .so digital filters are to be specified with a clear cut in the timing constrains in which the clock cycle need to

operate in the precisely and the transference of the signal to next proceeding stage, in this a signal is filtered by the anti-aliasing filter to remove the glitches to the output.

B.Analog filters:

Analog filters are mainly operated with the frequency with the continuous amplitude and the time taken for the signal to proceed to the output .In the Analog circuits the AC response depends on the feeding supply and the crucial biasing conditions, as the input voltages with the determined frequency prepends the noise to the circuits, in concern to the high range, the frequency variations will be par greater and to overcome this the port should withstand high stability. Mainly these filters tenders gain to the system and phase alternations.

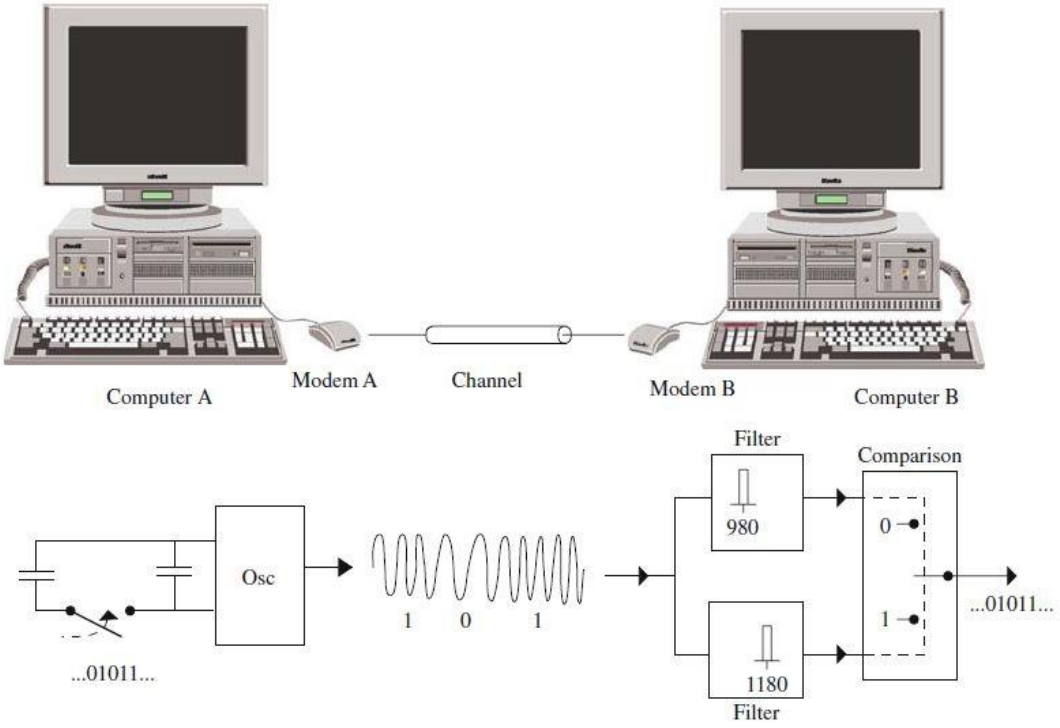

Fig 2.1 Computer-Computer communication by Filters

The figure 2.1 shows a simple Digital transmission system that suggests the Analog filters are main needs for data transmissions over the channels between two computers, to transmit the data the computer A sends the information to the Computer B in the form of ASCII symbols and the symbols need to be converted to 8-bit words.to transmit these bits over channel a referred phenomenon is needed like to carry the bits in a symbol a

physical quantity is much minimum, such that a signal like sinusoidal voltage by PSK(Phase shift Keying) technique, with two frequencies is sent. In the outturn the 0 represents 980Hz and the 1 is represented by the 1180Hz at the received frequency ,at the modem B we need two band pass filters to check the data received by matching with the amplitudes of the sinusoidal signal, so every transmission channel requires an Analog filter for the data conversion.so Analog filters play a lead role in data transfers at high rates in the context of the communication system that pursuits for signal conversion and retrieving the information from the output without loss of the signal carrier characteristics

2.2 TYPES OF FILTERS:

Filters are broadly classified in two types depending upon the distinct behaviour with input they are

- Component based
- Frequency Based

(i).Component based: on the component based they possess mainly **active filters** and **passive filters** utmost in which active filters pursues the resistors and capacitors, For the low frequency these components are placed in the filter design which holds attenuations that corresponds to the output in the passive filters are represented with the RC(Resistor-Capacitor)networks and LC(Inductor-Capacitor)networks.

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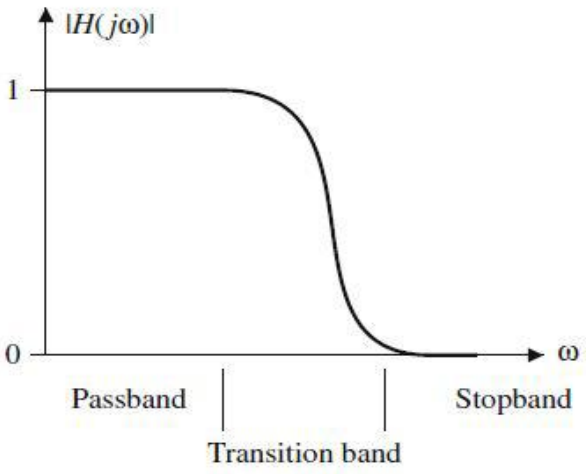


Figure 2.2 Low Pass Filter

(ii)Frequency Based: In respect to the frequency in the bands the filters that catches the respective bands are **low pass (LP)** filters that passes only low pass frequency and **high pass (HP)** to pass only the high frequencies for amplifiers and receivers. For particular applications in the transmitters the **band pass (BP)** to allow only respective bands and the **band stop (BS)** to supress the particular band of the signal. the frequency based filters are shown. In the frequency based filters the output is totally relay on the input with supply voltages, to construct these types of filters an express type of valuations are to be concerned with the desired frequency, gain and the phase change with proceeding to the input ,to accompany this we need to consider mainly with the bands in the frequency like transition band like to allow the particular band of the frequency for transition stop band to stop the particular bands and pass band to allow the band of frequencies. Three states in these types refers the peculiar type of filter.

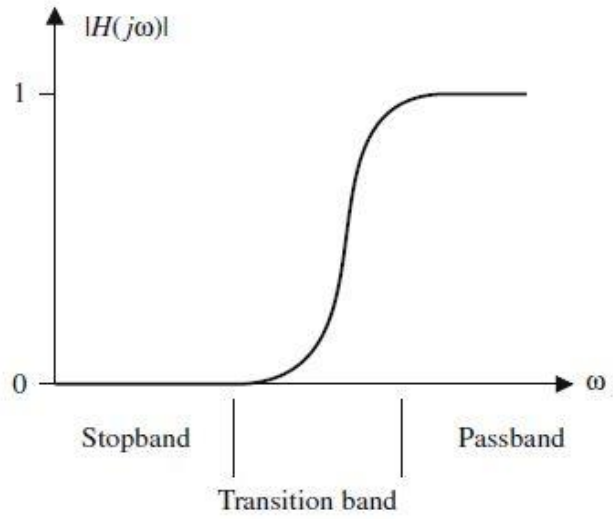


Figure 2.3 High Pass Filter

Majorly these frequency dependent filters are the chief processing blocks over gain control phase modulations and signal noise reductions to retrieve the specific information in the signal carriers and to modulate the input signal to the output.

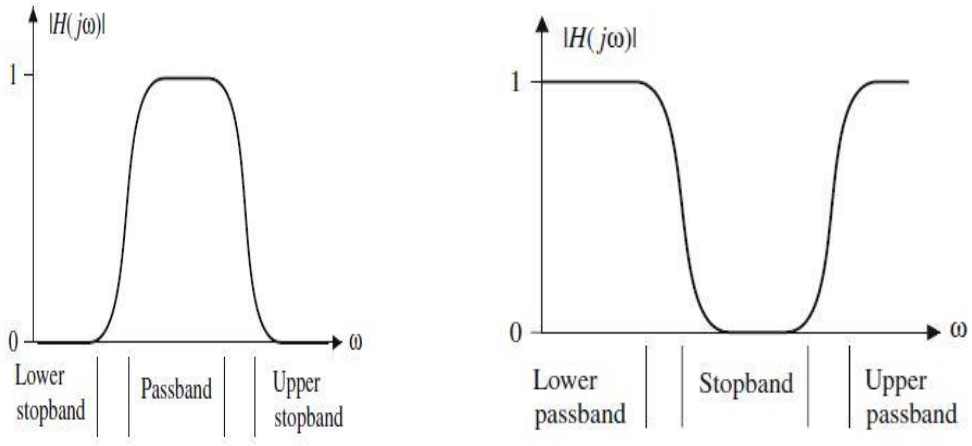


Figure 2.4 Band Pass and Band Stop Filters

2.3 WHY ALL PASS FILTER:

All pass filter is the major building block for many Analog signal processing systems and more attention is required to adopt this type. The most problem formulation in realising any filter design considerations the first concept we approach is the structural implementation with the expected output response. This work is a view of the design and implementations' by using the current conveyors namely **differential difference current conveyors (DDCC)** and the **fully differential current conveyors (FDCCII)** both which have the design constrains to implement , but in this regard the necessity is different so it requires special combination to construct the all pass filter circuit. In the designing of any filter type we approach with the design specification that the filter bank should process only specified frequency range and noted phase shifting's, in which for the low range appliances we infer the low pass filters and for high pass we move with high pass filters, but in the aspect of the all-pass filter designs a clear cut model is to be stated that it should fulfil all range of frequencies that comprises of both high and low range frequencies.

All-pass filters, otherwise called as the phase shifters are used in the processing block of the Analog signal operations, and in this all- pass filters are being a special cases for the filter transfer functions (TFs) Here it offers many advantages for the Analog filter designs. All-pass filters mentions a special case to cancel the unwanted sideband.

Zero and pole of the first-order all-pass filter are symmetrically located in relative to the imaginary axis, and real axis due to this location, and the transmission coefficient is seen

constant with respect to all the frequencies, and its phase shows with the frequency selectivity which has more usage . Multiple topologies of the All-pass filter are described so far to reach the noted considerations, and In that view various circuits are proposed and implemented, here the circuit carries CMOS transistors that use as the basic building blocks and plus-type second-generation current conveyors (CCII+s) composed of CMOS transistors because of low power. Considering many advantages All-pass filters are used as synthesize multiphase oscillators in the higher order filters which give wider bandwidth. In recent trends All-pass filters has many applications in the field of Radio-Engineering, defence, and wireless communications.

2.4ALL PASS FILTER DESCRIPTION:

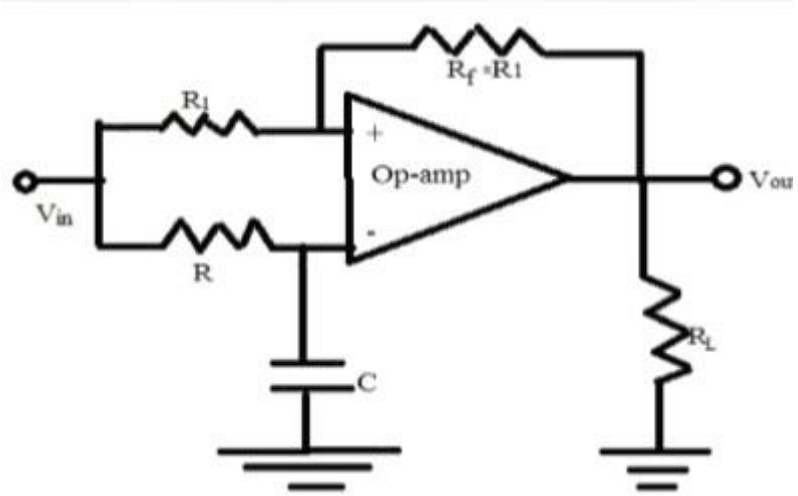


Fig 2.5 All Pass Filter schematic with op-amp

All pass filter is termed as signal processing filter in which it passes all the frequencies which are given at input and these frequencies are passed equally with gain and changes the phase relationship among various frequencies, here it operates by varying the phase shift as a function of input frequency, where the phase shift crosses 90° in which the input and output signals go into quadrature I.e. quarter wavelengths delay between these signals. These are generally used for compensating other undesired phase shift that occur in system, and it is mixed with an upshifted version signal of original signal for implementation of notch comb filter.

In All-pass filter it passes all the frequencies of all the input signals without attenuations where it gives predictable i.e. chosen phase shifts of different frequencies of all the input signals. The all-pass filters referred as delay equalizers and phase correctors

Circuit description:

Output voltage V_{out} for the above shown figure 2.5 is fined by using the superposition theorem

$$V_{out=-V_{in}}{}^{+}\left[\frac{-jX_C}{R-jX_c}\right]*2v_{in} \qquad (2.1)$$

Substitute -j$X_c = \frac{1}{2}лf_c$ in the above equation

$$V_{out} = \text{-V}_{in}\,(\text{-}1+\frac{2}{j2лf_c})$$

$$\frac{V_{out}}{V_{in}} = \frac{1-2лf_c}{1+2лf_c} \qquad (2.2)$$

Circuit parameters:

Here f = Frequency of a input signal given in the Hertz (Hz)

From the derived equations the amplitude is Vout/Vin = 1 i.e. unity from these | Vout | = | V_{in} | where it gives useful range frequencies and hence the phase shift between output and input as a function of frequency.

Output Response of the circuit:

All-pass the name itself defines that whatever the input frequency given to the system it allows all the allowable frequencies through it without distortions, at the output of the circuit is observed with respect to the input of the circuit with respect to the amplitude and time.

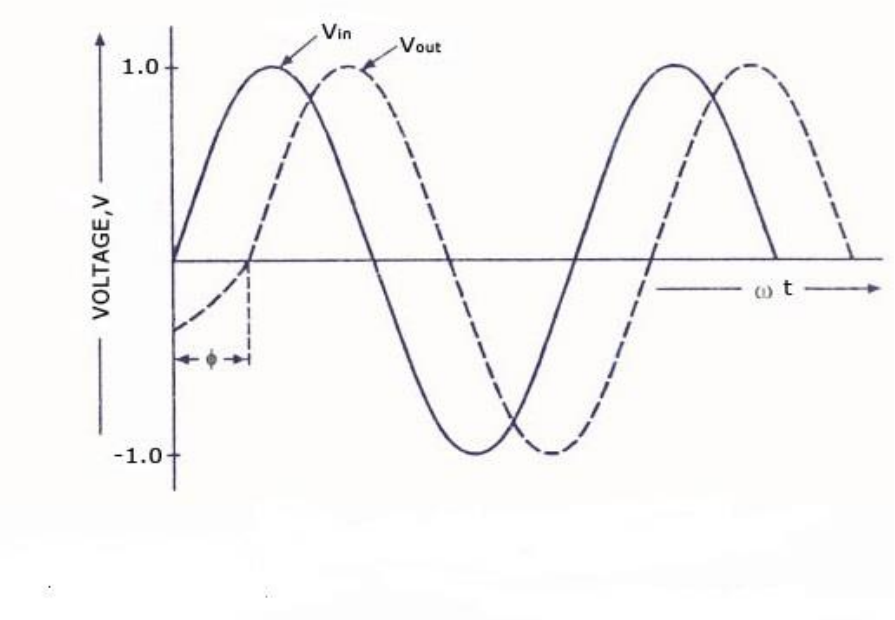


Fig 2.6 All Pass Filter output Response

V_{in} = input frequency voltage given at the input

V_{out} = output frequency voltage given at the output and Peak to peak voltage is 1

AC Response:

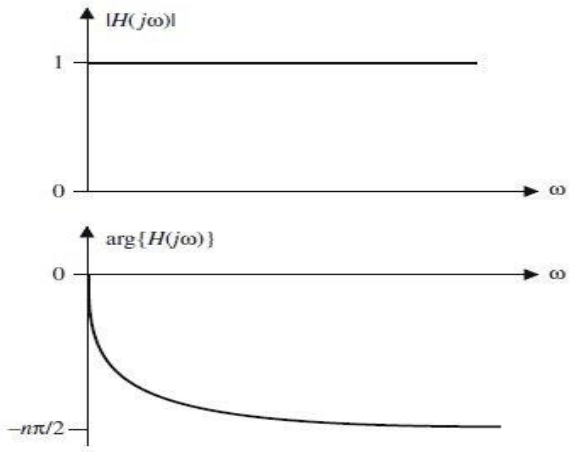


Figure 2.7 All Pass AC response

CHAPTER-3

REVIEW OF LITERATURE

✧ A.S.Sedra and Smith[1]

In this at first the current conveyors are discovered by the Sedra and Smith with realizing the stare space equations in the form of the matrix and satisfying the current and voltage equations mentioned in the matrix .To state these equations an Analog implementation is required to justify these equations and all pass filters are considered meets the constrains and in further development these are understood with the Wilson current mirrors for the applications for high range frequencies

✧ G.W.Roberts,et.al [2]

In the perspective of the al pass filters while considering the structures the model should be suitable for the IC realizations the models described in this paper fetches all the parameters that results in the chip design by connecting the passive elements to the ground.

✧ R.Senani.et al[3]

As the use of the current conveyors has increased in context of the high range applications. A new topologies are mentioned to with stand the signal carrier properties and to amplify and filter the signal with conversion a biquad filter is proposed with the KHN equivalent using the current conveyors.

✧ Shahram and Minaei[4]

As the topologies are refers with voltage mode (VM), current mode (CM) an all pass filter is proposed with an grounded capacitor, three resistors, and a single Current Follower (CF) with non-unity gain is presented. In comparison to the second-generation current conveyor-based current follower implementations employing large number of metal-oxide-semiconductor field effect transistors (MOSFETs), here the used CF is composed of only four MOSFETs. Hence, it is favourable for low-voltage low power circuit design. The APF was designed at pole frequency of 9.8 MHz with 112 μW power consumption using 90 nm CMOS process

- **S.J.G Gift[5]**

  All pass filters are realised by op-amps as they labels a simple design but in these due to feedback resistors the gain control is done but they infers a limitation in the limited gain bandwidth product and consumes more power where the load resistor and the feedback resistor values are normally high and resulting in low gain.

- **Ciecekoglu.et,al[6]**

  In modification with some topologies by using an single current conveyor a precise all pass filter is made in this the topology proceeds with the compound transistor a basic terminology in realising that pursues an pmos and nmos transistors majorly for the high range frequencies with high gain and the bandwidth .

- **I A Khan,et.al[7]**

  After the explicit designs of all pass filters .a number of modifications are done to the schematics of the current conveyors by considering the state space equations. The matrix representation of these equation refers to the port characteristics in which multiple port designs give more applications for mainly cascading networks.

- **M.Higashimura,et.al[8]**

  In the cascaded networks all pass filters are connected to give more gain and bandwidth for the networks while connecting in the cascading form there is change in the gain and this accompany the other parameters ,the models proposed in these presents a cascaded network without effecting the suitable features of an all pass filter

- **Lars Wan hammer[9]**

  The all pass filter has the several advantages mainly in the view of portable devices and it is used as the signal generator as the oscillator and the phase shifter for the signal carriers and the by the multi-port connections, in these various designs are mentioned like circulator, gyrator and the modulator, Analog signal processing mainly need all these types devices for data transmission with high efficiency.

- **Earkan Yuce[10]**

  In this all pass filter is implemented by the DXCCIdual-input-second generation current conveyor and in this DXCCI configuration holds two input and two

outputs with the intrinsic impedance is inserted at the output the connection of DXCCI is made with two capacitors and one two resistors resulting in the 800Mhz bandwidth with the coupling capacitors at the differential configuration.

- **Firat Yucel[11]**

Current conveyors suggests many applications like a oscillator for sinusoidal signal generation and here a new novel model of CCI is given as DOCCI(Dual-Output)current conveyor in which it is mixed of the trans linear loops and the compound transistors with the current mirror combination and to make an quadrature oscillator with converting whole into a block with cascading with a normal current conveyor .

- **Sudhanshu Maheshwari[12]**

In this a novel design is given by using a differential pair combination with the compound transistors, the differential pair is used to provide an efficient high impedance at the input ports and these impedances at the input port makes the system to withstand with the high frequencies and following the two combinations one combination with the resistor grounded and one combination with the capacitor grounded.

- **Emere Aslan[13]**

In this paper a new electronically tunable differential difference current conveyor is presented. The benefits of this new active element are demonstrated on tunable first-order voltage mode all-pass filter employing a resistor and a capacitor. In the proposed filter structure using single active and two passive elements no element-matching restriction is required. The theoretical results are verified with SPICE simulations using TSMC 0.35μm CMOS process parameters and with ±2.5v Supply voltages

- **Kamalesh kumar Singh[14]**

Here it provides a special voltage current conveyor which is differential voltage in which it gives a wide dynamic input range and is useful in the use of signal processing of voltage mode where it mentions most rigid popular technique that we realize in the cmos technology and its functions are clearly verified. , from the experimental results the novel design mentioned here provides a versatile Analog signal processing block with high range frequencies.

- **Mohammad,et.al[15]**

  Topology mentioned in this gives an ideal case of the current conveyor and considering this the passive elements are decided with the respect to the proposed model. In this the matching conditions for the passive elements are limited with respect to the β=1 and noting that poles and zeros of the CCII are finded by tracking the values by providing with volts which takes a more complexity.

- **PROPOSED MODEL**:

  Here we propose a new with model with all the considerations regard to the literature survey by analysing in the digital signal processing and calling that parameters' to implement in the Analog implementation by analysing the circuits with respect to the current conveyors .All the deigns in this thesis are implemented by the second generation current conveyor at first the design is implemented by the simple current conveyor or 1Ghz range and then for higher bandwidths and for higher by modification in the current conveyors DOXCCI,DVCCI and DOCCI blocks are implemented in the 180nm and 90nm CMOS technologies

CHAPTER-4

RESEARCH METHODOLOGY

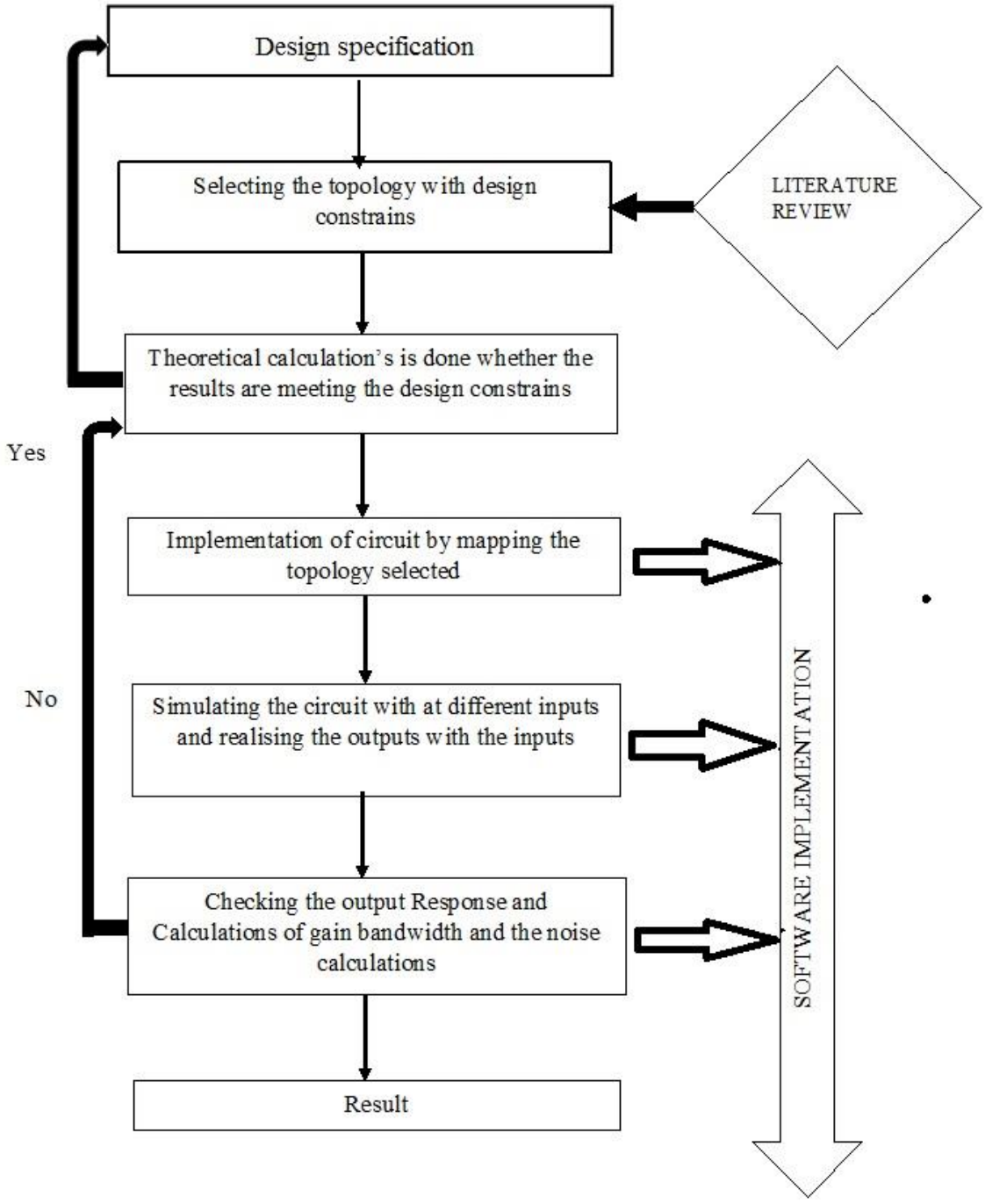


Fig 4.1 Research Methodology

Design specifications:

In any design methodology at first the design specifications' are to be noted like what should be the output of the circuit and input given to the circuit. Output response and phase response, power supply are to be decided. Here my design proceeds with the all-pass filter which it passes all the inputs and making magnitude constant.

Selecting the topology:

Here the topology is selected from the literature review and the design is to be made with the confined design constrains, here the topology which is selected which gives the better and desired result. As we are designing the all-pass filter the design specification consists of the frequency response should be constant, it should have wide bandwidth in range of GHz and the input voltage should be low.

Analytical calculations:

Here the theoretical calculations are done to the respective circuit by applying the possible conditions and verifying these calculations, we consider our design as all-pass where the magnitude of the all-pass is unity. We get the magnitude of all-pass is unity in Z-domain to implement this we choose as current conveyors because in the current conveyors by the port terminologies frequency response of the signal is to be constant and magnitude is unity As designing is made in the 180nm and 90nm technologies the process variations may be differ such that channel length is affected and some specific inputs are given to the circuit for achieving the low power and high stability.

Implementation:

The circuit is to be implemented in the Cadence virtuoso software, with the specified W/L ratios of the transistor. Depending upon the technology the circuit parameters are changed, circuit is to be simulated by choosing the input and output variables and the transient analysis and dc analysis is to be simulated by taking the supply voltage and bias current to the circuit we get the output with the respective input parameters.

Table 1 Technology parameters

PARAMETER	**180nm**	**90nm**
Supply voltage	**1.8v**	**1v**
Input frequency	0-1Ghz	0-10Ghz
Amplitude	100mv	100mv
Biasing voltages and current	Can't be defined	Can't be defined

The inputs are given according to the table 1 shown above

Output Responses:

Here the output response is much more important because as we are concerning the all pass filter in which it allows all the types of frequencies without distortion from the output only we decide that whether we met out design constrains and the following are the outputs we need to check

- ✧ Ac and Dc analysis
- ✧ Transient analysis
- ✧ Input Noise and Output Noise
- ✧ Noise Figure and Noise Factor
- ✧ Phase Noise and stability
- ✧ THD-thermal harmonic distortion
- ✧ Lissajous Patterns to locate the poles and zeros from Z smith and Y-smith graphs

Transient analysis: In the transient analysis the output is same as the input with the change in the phase and the transient time increases with decreases in the frequency and decreases at the high frequencies

AC analysis: From the ac analysis gain and bandwidth are calculated with respect to the input frequency and the supply voltage. Along the bandwidth unity gain is achieved with 180^0 phase shift.

Noise calculations: In the noise calculations input noise and output noise at the ports are determined with the load for several frequencies, the phase noises is calculated at output port to input port and the stability of the system defines the performance of the system over high range frequencies. In these mainly noise is affected from the Vdd and intrinsic capacitances of the transistor,

Lissajous Patterns: In the lissajous patterns the poles and zeros are plotted from the z-smith and the Y-smith graphs and from these graphs the poles and zeros of the system is known such that the system gives unity gain and it constant over the band of frequencies.

Power Calculations: The main concern in the Analog circuits are power calculations, as we proceed with the passive components to get high impedance the power may increase at a precise elements so the topology selection is to be result in less power and more extent low number of active components are used to decrease the power in the circuits and the values of the biasing voltages are to set more accurate that consumes low supply

Result: The desired result in which our design specifications are met in accordance with the all the design constrains.

CHAPTER-5

PROPOSED MODEL AND WORK DONE

PROPOSED MODEL OF ALL PASS FILTERS:

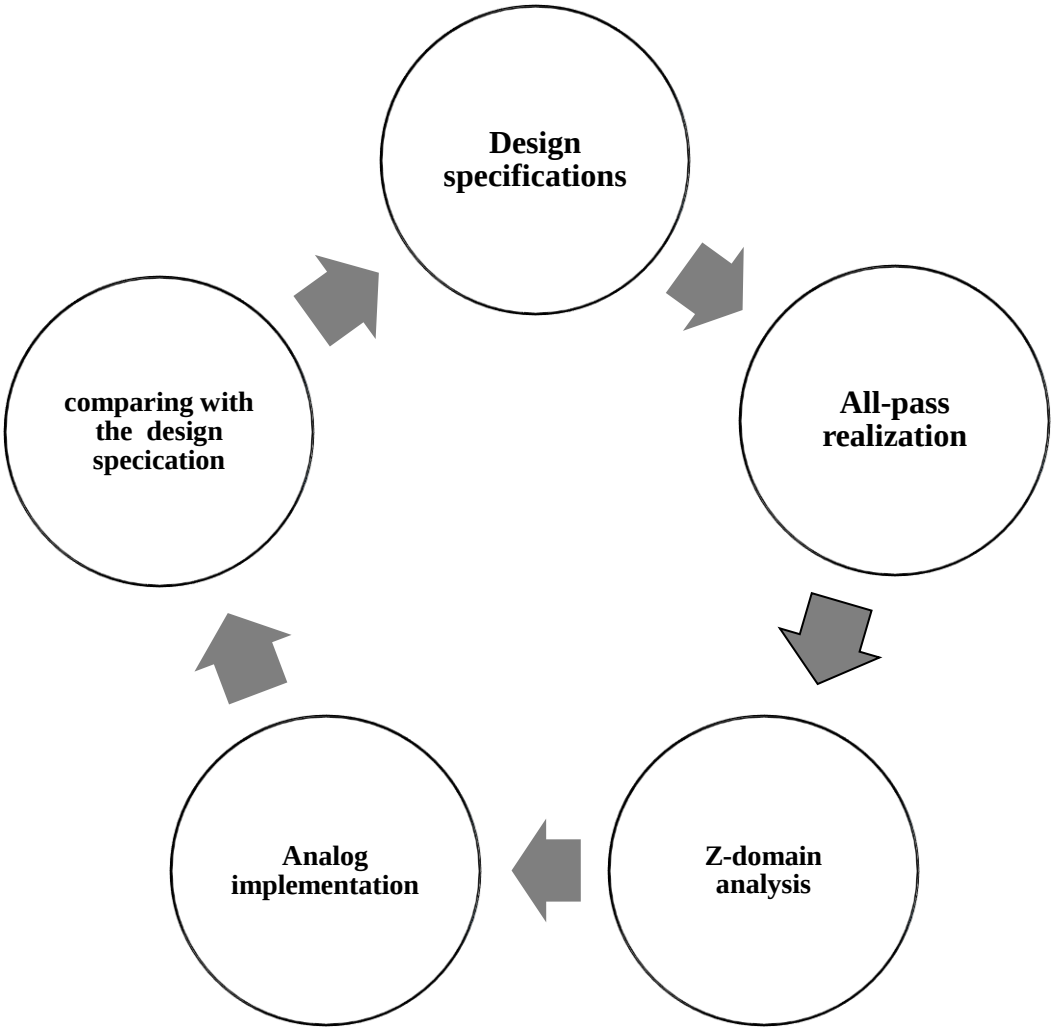


Fig 5.1 Proposed all pass realization

5.1ALL PASS FILTER REALIZATION:

The magnitude of frequency response is constant for an All-pass filter. All-pass filters are considered as IIR except for trivial filters. Now we start with a simple non-trivial all-pass filter by assuming unit frequency response.

$$H_{all}^{(k)}(Z) = \frac{z^{-1} - \alpha_k^*}{1 - \alpha_k z^{-1}} \qquad (5.1)$$

Here, the above expression represents an All-pass filter where, α_k represents the pole location. $|\alpha_k| < 1$ for the above expression.

All-pass filters can also be represented by cascade sections of it,

$$H_{all\,(k)}(Z) = \prod_{k=1}^{K} \frac{z^{-1} - \alpha_k^*}{1 - \alpha_k z^{-1}} \tag{5.2}$$

Let All-pass filter has real coefficient and there exist a conjugate root $\alpha*k$, for each complex root α_k. Therefore, an All-pass filter has a numerator polynomial having denominator polynomial coefficients conjugated and of reverse order.

$$H_{all}(Z) = \frac{z^{-k} - D^*(1/z^*)}{D(z)} \tag{5.3}$$

From Eq. (2), it is observed that any filter of the above form has a constant magnitude.

$$|Hall\,(\omega)|^2 = 1 \tag{5.4}$$

If α_k is expressed as $r_k e^{j\theta}k$ response for an all-pass section is

$$\begin{aligned} Arg\,[H_{all\,(k)}\,(\omega)] &= arg\,[e^{-j\omega} - \alpha_k^*] - arg\,[1-\alpha_k e^{-j\omega}] \\ &= arg\,[e^{-j\omega}] + arg\,[1-\alpha_k{}^* e^{-j\omega}] - arg\,[1-e^{-j\omega}] \\ &= -\omega - 2\tan^{-1}\left(\frac{r_k \sin(\omega-\theta_k}{1 - r_k\cos(\omega-\theta_k}\right) \end{aligned} \tag{5.5}$$

For $rk < 1$, the function inside the $\tan^{-1}$ (.)Denominator is positive which means the function is stable and causal All pass filter. The phase of $\tan^{-1}$ (.) function is limited by $\pm\pi/2$, as the numerator may change sign. As ω gets increased by 2π, the phase response decreases by 2π for each ALL-pass filter section. The total phase response is the sum of individual phases in each section. Therefore the overall phase decreases by 2лk with every 2л increase in ω which means monotonic.

$$Arg\,[H_{all\,(k)}\,(\omega)] = K\omega - 2\sum_{k=1}^{k} tan^{-1}\ \left(\frac{r_k \sin(\omega-\theta_k}{1 - r_k\cos(\omega-\theta_k}\right) \tag{5.6}$$

For an all-pass section, real roots have $\theta k = 0$, or $\theta k = \pm\pi$. For an overall all-pass filter with real coefficients, there are two sections that is one section with conjugate roots for each section of complex roots. These two sections are responsible to make the phase response of the overall All-pass filter with real coefficients, an anti-symmetric, with respect to $\omega = 0$.

5.2 Group Delay Response:

The group delay response of an All-pass filter can be determined from the below represented expression

$$\tau_{g\,(\omega)} = k + 2\sum_{k=1}^{k} \frac{r_k \sin(\omega-\theta_k) - r_k^2}{1 - 2r_k\cos(\omega-\theta_k) + r_k^2} \tag{5.7}$$

$$=\sum_{k=1}^{k}\frac{1-r_k^2}{1-2r_k\cos(\omega-\theta_k)+r_k^2} \quad (5.8)$$

In the second expression, we see that for $r_k < 1$, the group delay of an All-pass filter is always positive, as the above expression represents that the group delays the ratio of all positive coefficients. The group delay response of filter section has, denominator with minimum $\omega = \theta k$, which leads a peak in the response at that frequency. Positivity of the group delay means that the phase is monotonically moving downward as a function of frequency. So, as the phase decreases with increase in ω, the area of group delay response underlying the frequency 2π is $2\pi K$. Therefore we can frame that, the average group delay of an All-pass filter is K samples.

Magnitude System Response of an All-Pass Filter:

As the magnitude is constant, we generalize the result, we, we generalize the result, we consider the magnitude of $H_{all}(z)$ where z is not necessary

$$[H_{all}(k)(Z)]^2 = \frac{1-Re[\alpha_k^* Z]+|\alpha_k|^2\,|z|^2}{|z|^2-2Re[\alpha_k^* Z]+|\alpha_k|^2} \quad (5.9)$$

$$= \begin{cases} > 1 & |z| > 1 \\ 1 & |z| = 1 \\ < 1 & |z| < 1 \end{cases} \quad (5.10)$$

5.3 ALL-PASS DECOMPOSITION:

The first part of the figure shows the pole/zero configuration of a filter. This filter is actually maximum-phase, not with minimum phase. The filter can be represented as product of all-pass filter and minimum phase filter as shown in below figure. For the first impulse response of minimum phase filter, the gain is to be unity. The below figure also shows the frequency and impulse response of a minimum phase filter. The phase returns to zero at $\omega = \pi$, which means the phase response is not increasing with respect frequency. Therefore, the phase has both negative and positive slopes, which leads to group delay.

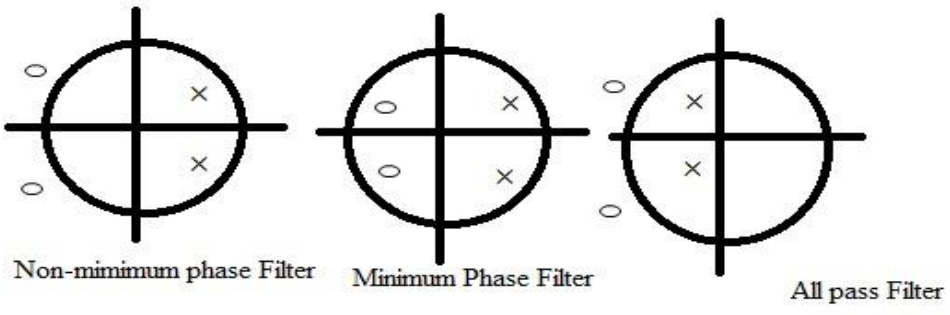


Fig.5.2 Location of poles and zeros in the z-plane

CHAPTER-6

IMPLEMENTATION OF PROPOSED WORK

6.1Analog realization with respect to the z-domain:

Z-domain realization:

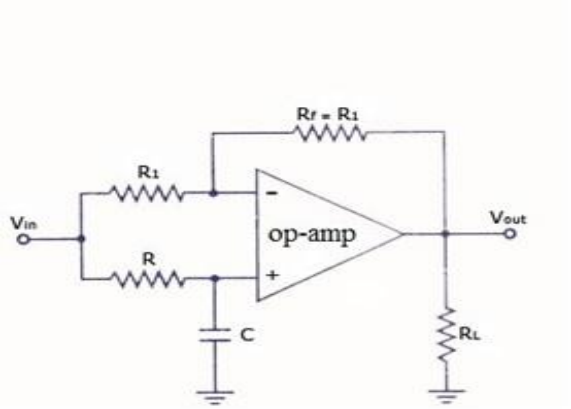


Fig 6.1 Z-Domain realization of the all-pass filter

All-pass refers to unity-gain across all frequencies where the output is taken with constant amplitude with phase shift

For unity gain:

Gain changes slowly from ⟶ inverting configuration {180° deg}

⟶ Non-inverting configuration {0° deg}

Transition between the inverting and Non-inverting given by the corner frequency f_c

$$f_c=\frac{1}{2\pi RC}$$

For an all-pass section:

Table 2 Centre frequency of an all pass filter

Frequency	**Configuration**	**Phase**	**Delay in wave**	**Operation/output**
$f<<f_c$	Inverting	-180^{θ}	Half cycle	c-opens and inverting path
$f=f_c$	-	-90^{θ}	Quarter cycle	c-shorts signal pass through in +ve path
$f>>f_c$	Non-inverting	0 deg	None	c-shorts non inverting path

For the positive path analyse each part separately negative input looks like standard inverting amplifier. V_{in} passes across R_1 and R .positive path looks like high pass filter and from resistor and capacitor for a non-inverting gain is defined by R_1 and R_f values

$$V_{out} = V_{in} - \frac{R1}{Rf} \quad (6.1)$$

$$V_{out} = \frac{V_{in} - R}{\left[\frac{R+1}{SC}\right] * \left[1 + \frac{R_1}{R_f}\right]} \quad (6.2)$$

$$V_{out} = \frac{V_{in-R}}{R_f + \left[\frac{1}{sc}\right] * [1 + \left(\frac{R_f}{R_1}\right)]} \quad (6.3)$$

For inputs V_{in} across R_1 and R set $\frac{Rf}{R1}$=1

By adding the outputs together with input

$$\frac{v_{out}}{v_{in}} = \frac{1-sRC}{1+RC} \quad (6.4)$$

$$H(s) = \frac{1-sRC}{1+RC} \quad (6.5)$$

Where H(s) is the transfer function of all pass filters

$$S=j\omega \text{ and } \omega=\frac{2л}{T}$$

Substitute the s and ω values in the in the H(s) then we get H(s) =1

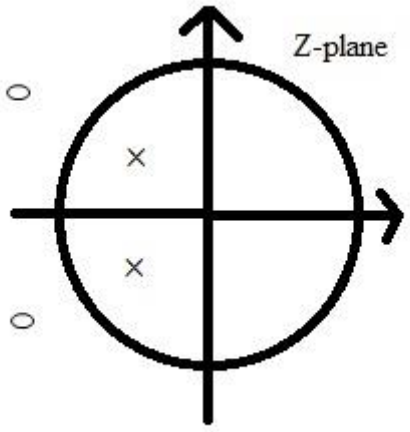


Fig 6.2 Z-plane showing the poles and zeros of the all-pass filter

Magnitude:

H(s) =1

Above equation represents all pass filter magnitude

H (jω) =1

For locating the poles and zeros: One pole is at $\frac{-1}{RC}$ and one zero at $\frac{1}{RC}$ and When we plot this in respect to the z-domain analysis we get plot the poles and zeros for an all- pas filter as shown above.

6.2 ANALOG IMPLEMENTATION:

From the Z-domain realization we get the design specifications of the all-pass filters where it has the properties derived from the z-plane, and to implement this in the Analog, a rich catalogue is required to provide all the parameters for the design. Then we proceed with the topologies required and the study relates with the review of an important Analog electronic function, in form of an all-pass filter's realization using current conveyor types and these are implementations can be realized using CADENCE 180nm and 90nm process technology and the 90nm technology for output results and simulations

- **CURRENT CONEYORS:**

In the concern of many high frequency range applications the current conveyor assists the fundamental blocks for processing the signal carriers and introduced in the year 1968 by Sedra and Smith. There is a more discussion in recent years, on current-mode circuits which play crucial role in Current-conveyors. Current conveyors has vast applications range from multifunction and universal filters, oscillators etc. Current conveyors gives a larger band-width and more suitable for low voltage applications. The current conveyors cannot use Op-Amps, because, the Operational amplifier has a poor performance when it is need with a current output. There is no feedback in the current conveyor, so it gives a high frequency behaviour when we compare to an Op-amp, because the gain bandwidth product limitation is not suitable for high frequency Op-amp.

Fig 6.3 Representing the simple current conveyor symbol

A current conveyor is a three port network. Block representation of current conveyor is given in figure. It has the wide range of properties like accuracy, Versatility in wide range

applications and high frequency range. .The Current conveyor has a very simple architecture with wide bandwidth and is capable to operate in low voltages. We have three generation types of current conveyor's are there, but we select second generation conveyor which meets our design specifications.

- First Generation Current conveyor, CCI.
- Second Generation Current conveyor, CCII.
- Third Generation Current conveyor, CCIII.

6.3. SECOND GENERATION CURRENT CONVEYOR (CCII):

The second generation current conveyor (CCII) is the most adaptable current-mode building block because if its high impedance input port which avoids load effect. The CCI has two low input impedance ports, but second generation CC has only one low input impedance port, which is required for our design. In CCI, the Y port is high input impedance port, from which no current flows, But in second generation CC, the Y port acts as voltage input with Z port as current output and X port as either current input or voltage output and hence this differs from first generation because, this current conveyor can be used to operate in both voltage and current modes. The second generation CC is again classified as two types.

- Positive current conveyor (CCII+) , in which the current magnitude of both X port and Z port is same
- Negative current conveyor (CCII-), in which the currents magnitudes are opposite for X and Z port.

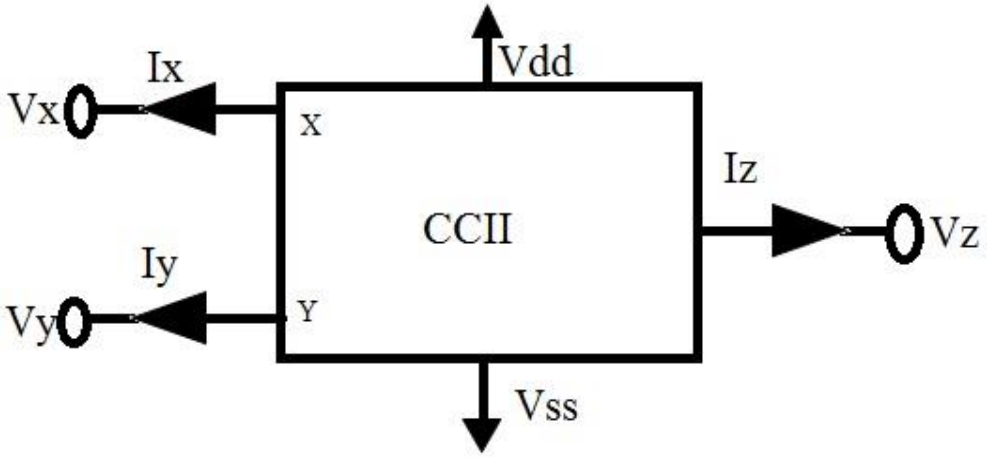


Fig 6.4 Representing the CCII symbol

The matrix representation of second generation CC is given by

$$\begin{bmatrix} I_x \\ V_x \\ I_z \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ I_X \\ V_Z \end{bmatrix} \quad (6.6)$$

The characteristic equations of the above CCII fig 6.4 symbol is given as

For CCII (+): $I_{Y=}0$, $V_X=V_Y$, $I_Z=I_X$ from port terminals of Z+

For CCII (-): $I_{Y=}0$, $V_X=V_Y$, $I_Z=-I_X$ from port terminals of Z-

For non-ideal case of CCII:

$$I_y=0 \quad (6.7)$$

$$V_X=V_y\ (1+\varepsilon_1) \quad (6.8)$$

$$I_X=I_y\ (1+\varepsilon_2) \text{ (where } \varepsilon \text{ denotes polarities)} \quad (6.9)$$

Analysis:

- Impedance is finite which is taken in to consideration of the circuit design. The voltage applied to node Y i.e.V_Y, and that voltage is gets replaced at the node X. and it is similar with the virtual short on an op-amp.
- When a current flows at node X, the same current flows into node Z and notation CCII+ denotes a positive Z at the output current conveyor (= +1) whereas CCII- gives a negative Z of the output current conveyor (= -1). And the terminal Y shows infinite input impedance.

Current conveyor circuit:

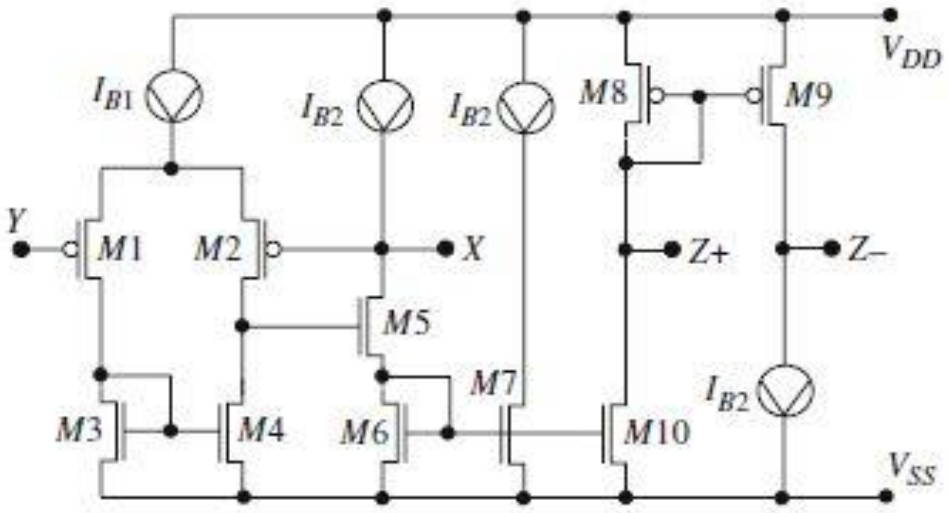


Fig 6.5 Representation of the CCII (+) circuit

The above schematic represents the second generation current conveyor with positive and negative types and it is combination of the compound transistor and the Trans linear loops, the schematic is made into the block as shown in the above section and the inputs are applied.

6.4 Dual-X-Second Generation Current conveyor:

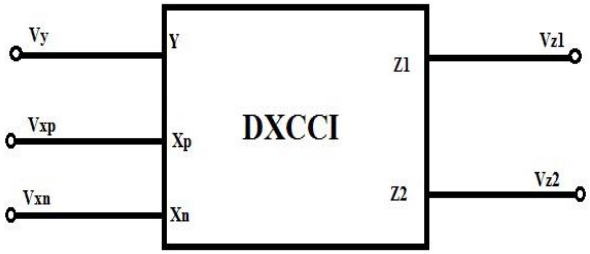


Fig 6.6 Block representation of Dual-x- second generation current conveyor

The above block gives a vision of an all pass model by the DXCC Dual-X-Current-Conveyor and the ports are set according to the impedances and the impedance match is made by the connection with the passive components. The values of the passive component is chosen by Monte-Carlo analysis for the respective frequencies, to get the precise gain without any change in the magnitude of the signal and from the voltage current relationship of the current conveyor in matrix method is given by the

$$\begin{bmatrix} I_Y \\ I_{Z1} \\ I_{Z2} \\ V_{XP} \\ V_{Xn} \end{bmatrix} = \begin{bmatrix} 0 & 0 & k_y & 0 & 0 \\ \alpha_1(s) & 0 & 0 & K_{Z1} & 0 \\ 0 & \alpha_2(s) & 0 & 0 & K_{Z2} \\ Z_{xp}(s) & 0 & \beta_1(s) & 0 & 0 \\ 0 & Z_{xn}(s) & -\beta_2(S) & 0 & 0 \end{bmatrix} = \begin{bmatrix} I_{xp} \\ I_{xn} \\ V_y \\ V_{z1} \\ V_{z2} \end{bmatrix} \qquad (6.10)$$

From the above matrix form the Transfer function is derived for the DXCCI ,and the currents at the ports Y and X is defined with the input supply and the resultant currents are given by the following equations such that in ideal case the behaviour of the terminals vary from ideal to practical and given as

$$I_y = 0 \text{ and } I_{z1} = I_{ZP,} \text{ and } \quad I_{Z2} = I_n \qquad (6.11)$$

With concern to the supply voltage the voltage at the output port Z1 and Z2 is due to the loads resistor and the voltage here defines the impedance exerted at the input and the voltages at this ports are given

$$V_{Z1}=V_{Y,}V_{Z2}= -V_Y \qquad (6.12)$$

DOXCCI proposed in this is operated in two modes, Voltage Mode (VM) and Current Mode (CM) and these modes of operations are given by proceeding with ports and to get unity gain and high bandwidth.

6.4.1Voltage Mode:

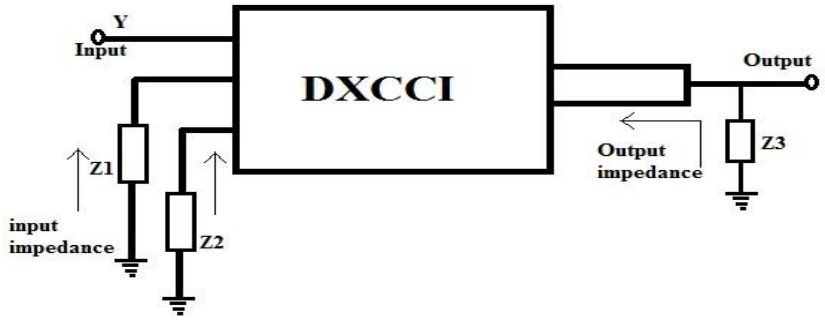


Fig 6.7 Voltage Mode of the D-X-CII

In the voltage mode of DXCII the unity gain is achieved by the change in the impedance followed by the Z1, Z2, Z3 values and in the voltage mode the inverting phase of the input frequency and voltage from the output to input is consider along with the impedance and these gives the gain and phase and

$$\frac{V_{out}}{V_{in}} = \frac{1-SCR}{1+SCR} \qquad (6.13)$$

The above equation infers the gain and the phase of the input frequency 180° i.e. inverted at the output and the inverting phase gives the phase shit of the amplitude alternations of the input signal represents

$$\phi\,(\omega) = -2\tan^{-1}(\omega CR) \qquad (6.14)$$

The overall impedance offered by the voltage mode DXCCI at the inverting of the phase and the change in phase makes the unity over the bandwidth and this results to allow any frequencies to the input and

$$\phi(\omega) = 180°\text{-}2\tan^{-1}(\omega CR) \qquad (6.15)$$

In the DVCC the main concern is the differential terminal in these the voltages are fed at the terminals the impedances that are fed at the port desires the precise impedance that is replica of the feeded input in this context t it constitutes both impedances and compares the supply impedances and the same impedance is inverted at the output port and in replica as the terminology accompanies the impedances the adequate amount of impedance required to get the desirable gain and to operate at high frequencies.

6.4.2 Current Mode (CM) of DXCCII:

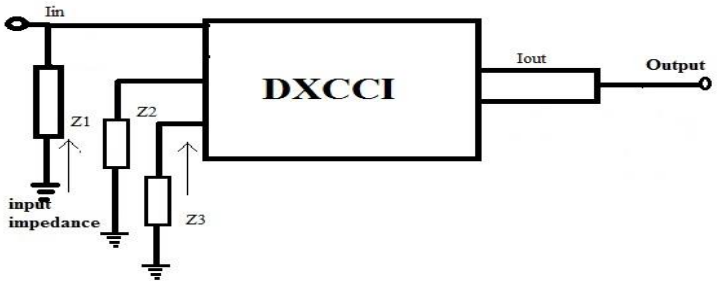


Fig 6.8Current Mode of the DXCCI

In the current mode of DXCCI it offers an non-inverting terminal from the configuration and by the impedances of the Z_1 Z_2 and the Z_3 is given by the $Z_1 =$ Z_2 and $Z_2 =$ $R_2 + 1/$ (cost), and in this mode at the input the passive component count varies due to maintain the stability of the block at high frequencies

$$\frac{I_{out}}{I_{in}} = \frac{R_3}{R_1} \times \frac{1-SC(R_1-R_2)}{(1+SCR_{2)}} \qquad (6.16)$$

The overall impedance and the vary in the resistance and in this mode there will be no phase changes

$$\frac{I_{out}}{I_{in}} = \frac{R_3}{R_2} \times \frac{(1-SCR_1)}{(1+SCR_1)} \qquad (6.17)$$

And from these two modes the unit gain and phase is resulted and the values of the transistor are set accordance with the process parameters and every transistor should operate in the saturation at V_{dd}

The following table represents the values of CMOS transistors of the DXCCI with all R and C values.

Table.6.1 DXCCI MOS CONFIGURATION

Mos transistor's	Width (µM)
M15.M16,M17,M1 M18,M19	2 u
M4.M5,M6,M9,M10,	0.999
M13,M11,M12,M14	1.54
M1,M2,M3,M8,M7	6.2

In the implementation of the DXCCI the L and C values are chosen to tune the circuits for operating at the high frequencies and LC network is connected with the cascaded stages and gives high bandwidth

$$X_C = \frac{1}{\omega C} \quad , \qquad X_L = \omega L \tag{6.18}$$

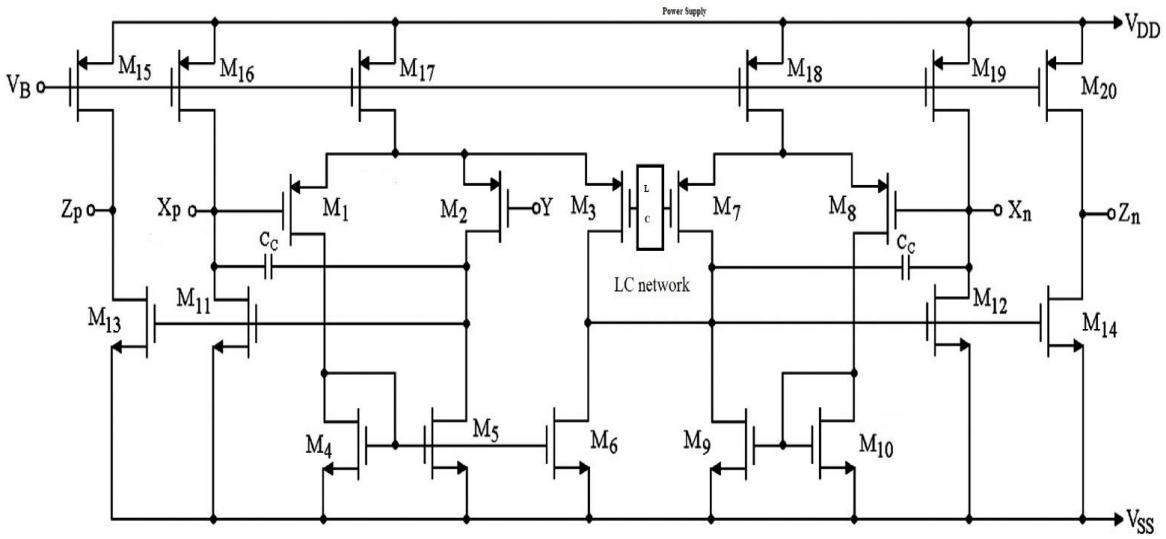


Fig 6.9 Schematic of DXCCI

Above schematics is the combination of the mixed translinar loop and the compound transistors are converted to the block as mentioned in the above section and output is verified at 1 GHz input frequency.

6.5 Differential-Voltage Current conveyor (DVCC):

The configuration proceed in this segment is Differential-Voltage-Current-Conveyor and in this same as the DXCCI but the topology constitutes of differential configuration in which terminal relations are

$$\begin{bmatrix} V_X \\ I_{Y1} \\ I_{Y2} \\ I_{Z+} \\ I_{Z-} \end{bmatrix} = \begin{bmatrix} 0 & 1 & -1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_{Y1} \\ V_{Y2} \\ V_{Z+} \\ V_{Z-} \end{bmatrix}$$

At the Y1 and Y2 input ports if we apply the input frequency it results in the high impedance and low impedance is proceeded at the output and the voltage at the terminal X accompanies the sum of inputs

$$\frac{V_2}{V_{in}} = -\frac{sCR-1}{sCR+1} \qquad (6.19)$$

Current proceeded towards the terminal X will be conveyed across the Z1 and Z2 follows the high impedance and these high impedance infers the matched impedance towards the ports of Y1, Y2 and has

$$\frac{V_2}{V_{in}} = -\frac{sCR-1}{sCR+1} \qquad (6.20)$$

Phase response of the output with respect to the input is 180° and the minimum phase shift is required

$$\phi(\omega) = -2\text{Tan}^{-1}(\omega CR) \qquad (6.21)$$

6.5.1 *DVCC block:*

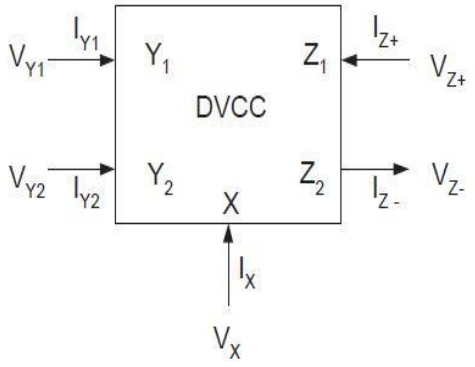


Fig 6.10 Symbol of DVCC

From the DVCC symbol it simplifies that it has the more port terminals to maximise more frequencies

$$\phi(\omega) = 180° - 2\text{Tan}^{-1}(\omega CR) \qquad (6.22)$$

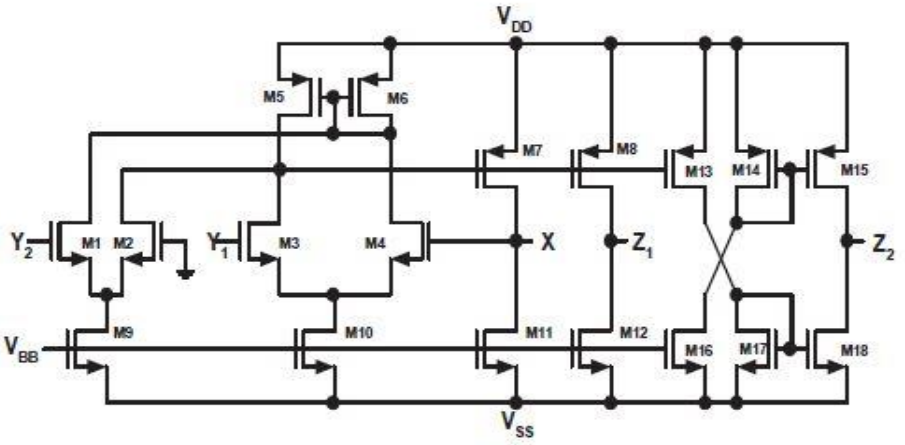


Fig 6.11 Schematics of DVCC

6.5.2 Proposed DVCC block of All Pass Filter:

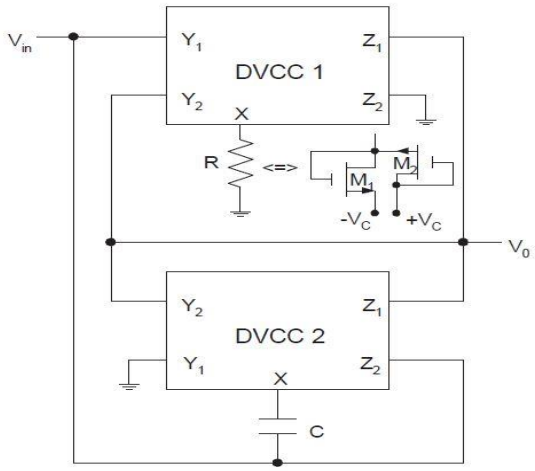


Fig 6.12 Proposed All Pass Filter Using DVCC

6.6. Dual Output Current Conveyor:

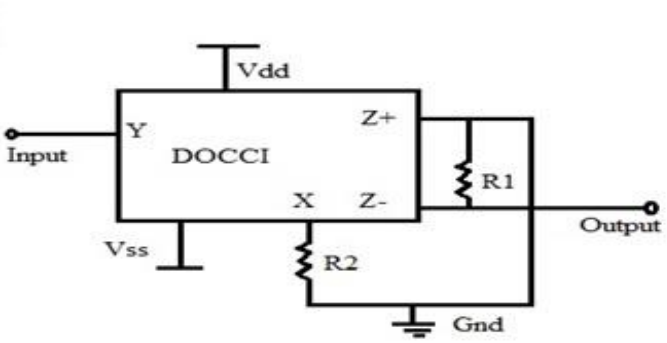


Fig 6.13 DOCCI Block

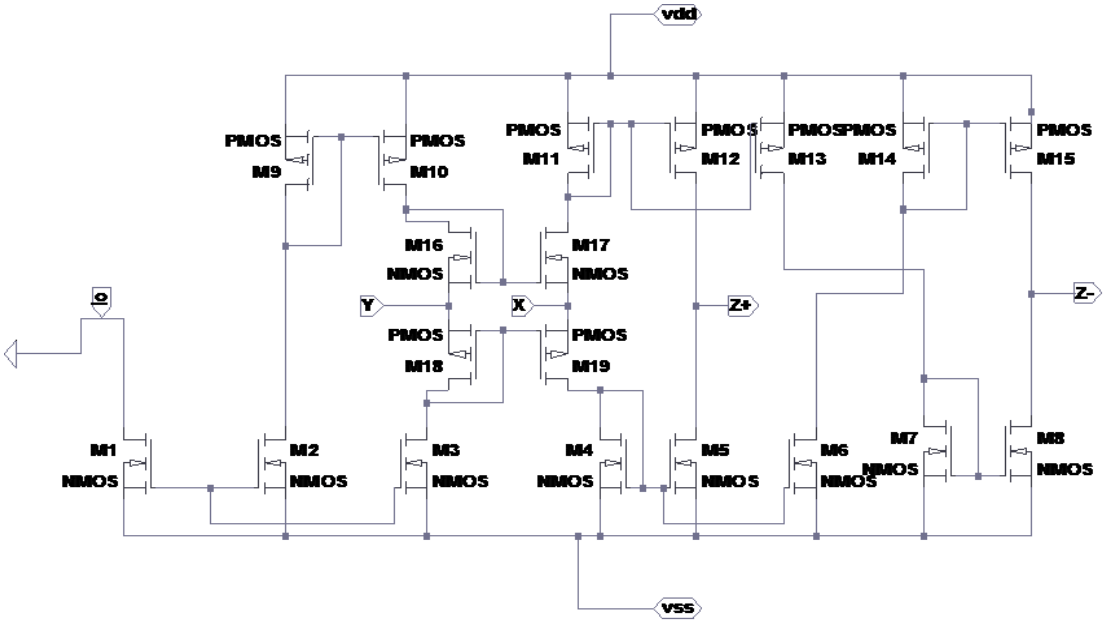


Fig 6.14 Schematic of DOCCI

6.7. Trans linear loop in current conveyors:

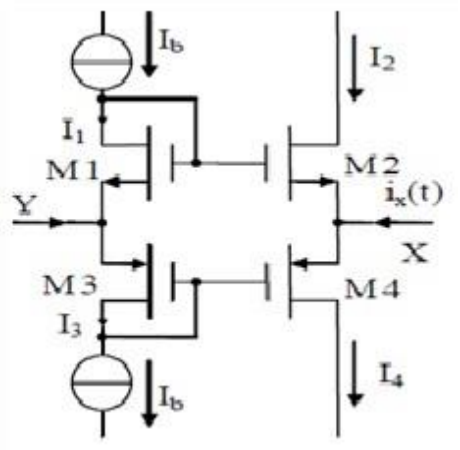


Fig 6.15: Representing the MOs Trans linear loop

Drain current and gate-source voltage meet the following conditions

$$I_d = {}^{K}/_{2}(V_{GS} - V_{th}) \qquad (6.23)$$

Where V_{GS} and the gate source voltage and k is given as $k=\mu_n C_{ox}$ (W/L) that is transconductances gain

W=width of the channel

L=length of the channel

V_T=thereshold voltage

For MOS transistors' in the Trans linear loop the relation is given and the voltages at the gate to source

$$V_{GS2} = V_{GS1} - V_{xy}$$

$$V_{GS4} = V_{GS3} - V_{xy}$$

From above equations we get the conditions as

$$V_{xy} = (4\frac{W_4}{L_4}\sqrt{\frac{k_p L_3 I_b}{W_3}})i_x(t) = R_x i_x(t) \qquad (6.24)$$

Voltage across terminal xy is given byV_{xy} and the above condition is correct only when

$$\frac{w_1}{L_1} = \frac{K_P}{K_n} * \frac{W_2}{L_2}, \qquad \frac{W_3}{L_3} = \frac{K_p}{K_n} * \frac{W_4}{L_4} \qquad (6.25)$$

Where $K_n K_p$ the transconductances coefficients for the NMOS and PMOS transistors, the parasitic resistance is given as Rx and the parasitic capacitance that is fed into it at x terminal acts as the input impedance to the circuit and it is inversely proportional to the square root of the biasing current of the circuit and these biasing current(I_b),but this offers restrictive condition regarding to the fabrication technology where for the IC implementations these accompanies a precise routing without effecting the transistor routing and in the trans linear loop the thickness of transistor is to be found, Considering this restrict condition we use a the MOS compound transistor

C**ompound Transistor:**

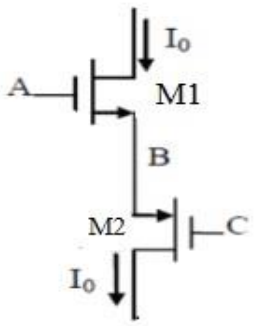


Fig 6.16 Compound transistor

The compound transistor shown above is the end to end connection of the pmos and nmos transistors as in the current mirrors it comprises only nmos transistors but in the

compound transistor it pursues both pmos and nmos transistors here by end to end connection the sources are connected and the drain

Currents of the pmos and nmos transistors are given by the

$$I_{d1} = I_0 = \frac{K_n}{2}(V_{GS1} - V_{th})^2$$
$$I_{d0} = I_0 = \frac{K_p}{2}(V_{GS2} - V_{th})^2$$

} drain currents of M1 and M2

From the above equations we get the

$$V_{GS1} - V_{GS2} - (V_{Tn} - |V_{tp}|) = (\frac{1}{\sqrt{K_n}} + \frac{1}{\sqrt{K_p}})\sqrt{2I0} \quad (6.26)$$

$$I_0 = \frac{1}{2}\frac{k_n k_p}{k_n + k_p} V_{GS1} - V_{GS2} - (V_{Tn} - |V_{tp}|^2 \quad (6.27)$$

By the order we get

$$V_{GSn} = V_{GS1} - V_{GS2} = V_A - V_C - (V_c - V_B) = V_A - V_C \quad (6.28)$$

$$V_{eff} = V_{Th} - |V_{Tp}| : K_{eff} = \frac{k_n k_p}{\sqrt{k_n} + \sqrt{k_p}} \quad (6.29)$$

At last we get the values as

$$I_0 = \frac{K_{eff}}{2}(V_{Gn} - V_{Teff})$$

CHAPTER-7

RESULTS AND DISCUSSION

DXCCI Schematics View:

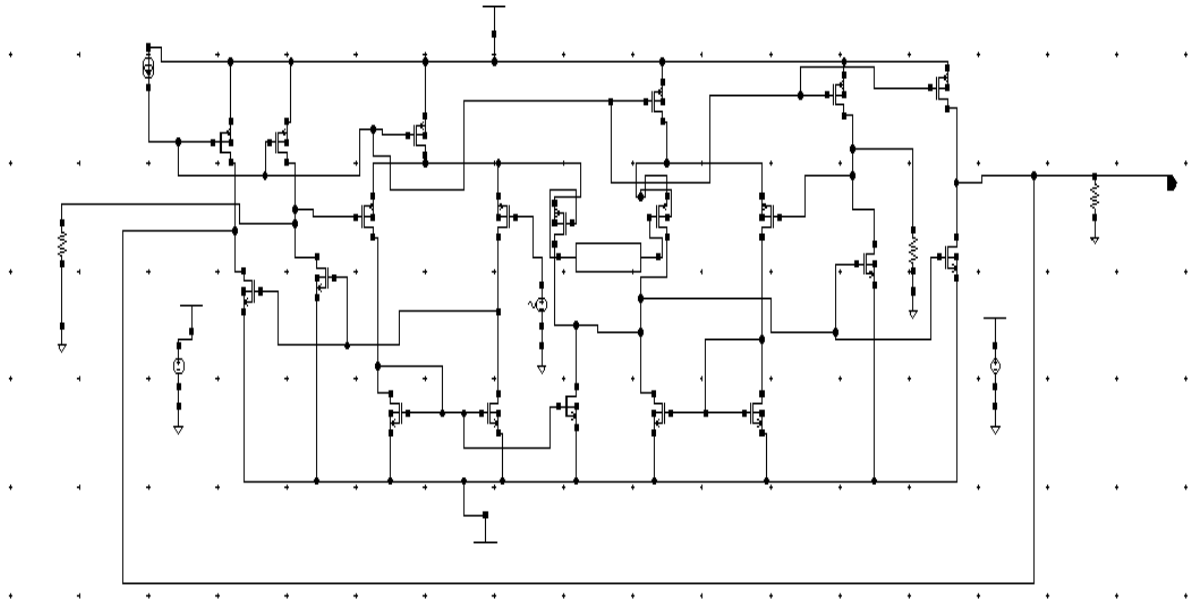
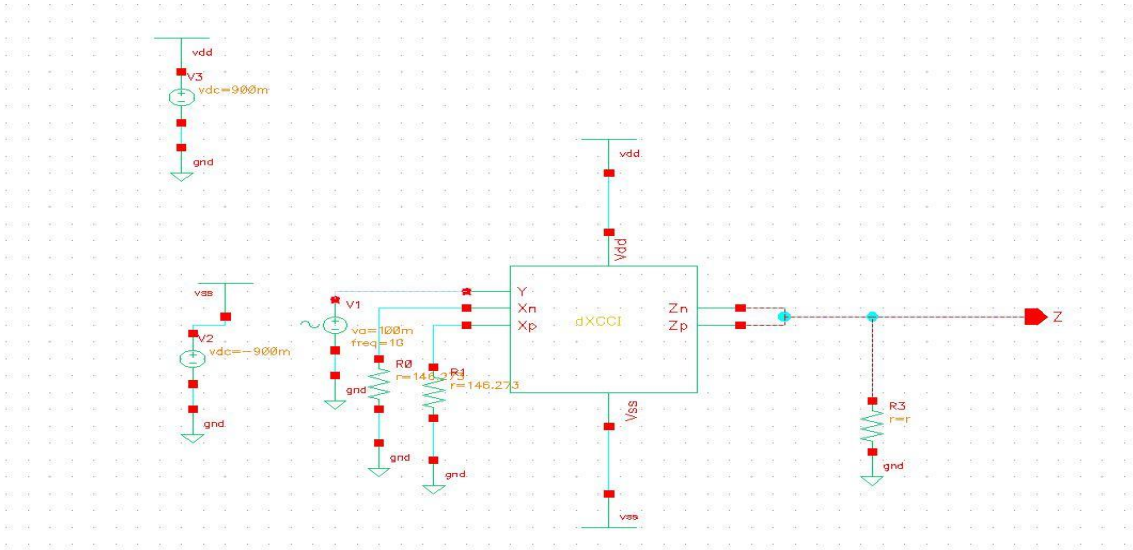


Fig7.1 D-X-CCI Schematic

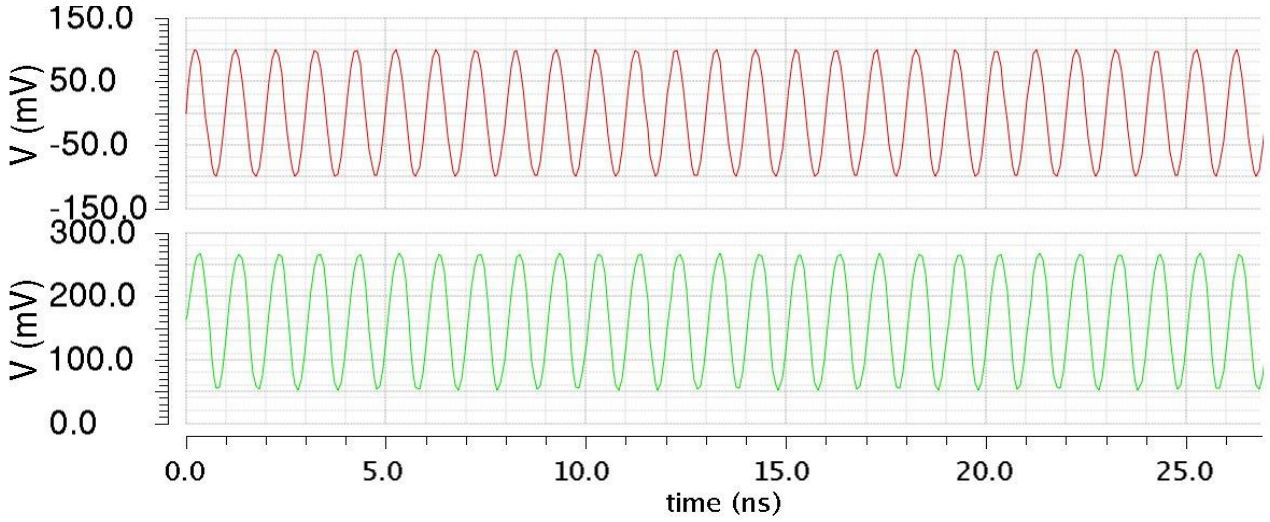
In the DOCCI at the inputs are given as

- Input supply voltage,500mv for V_{dd} and -500mv for V_{ss}
- Input Frequency 1Ghz
- Ac magnitude=100mvAC amplitude=100mv

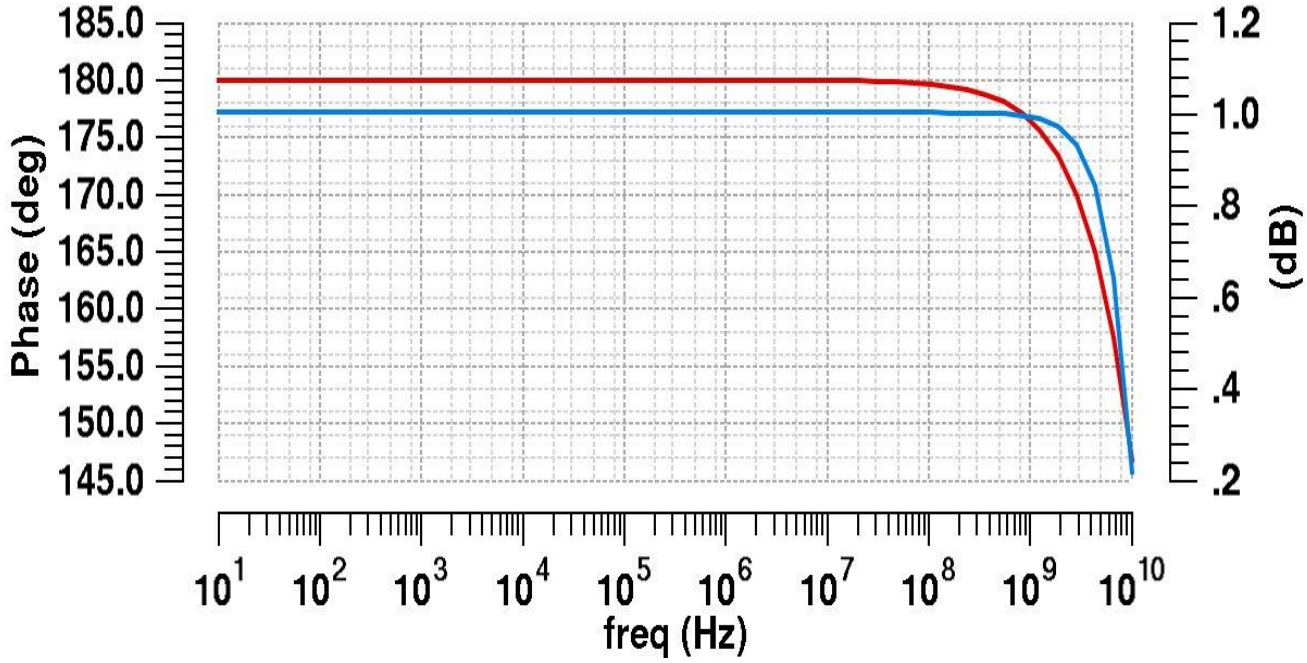
DXCCI Block:



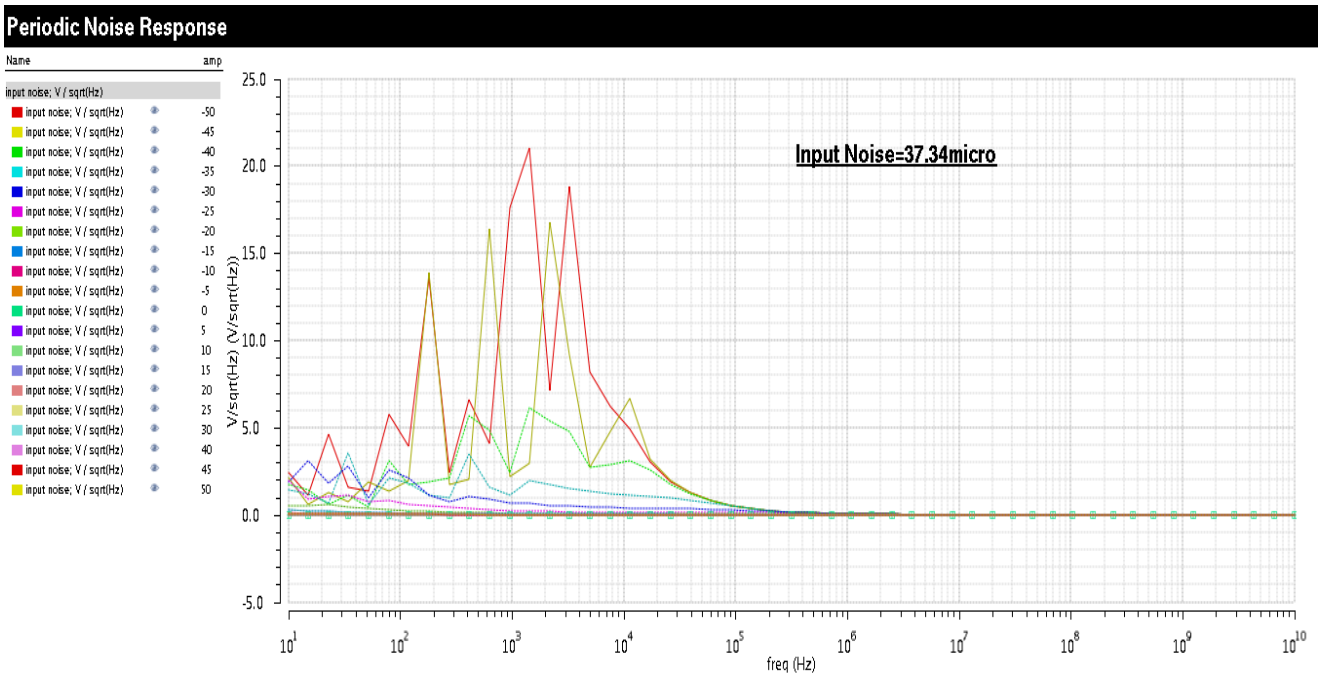
Transient Response of Proposed DXCCI:



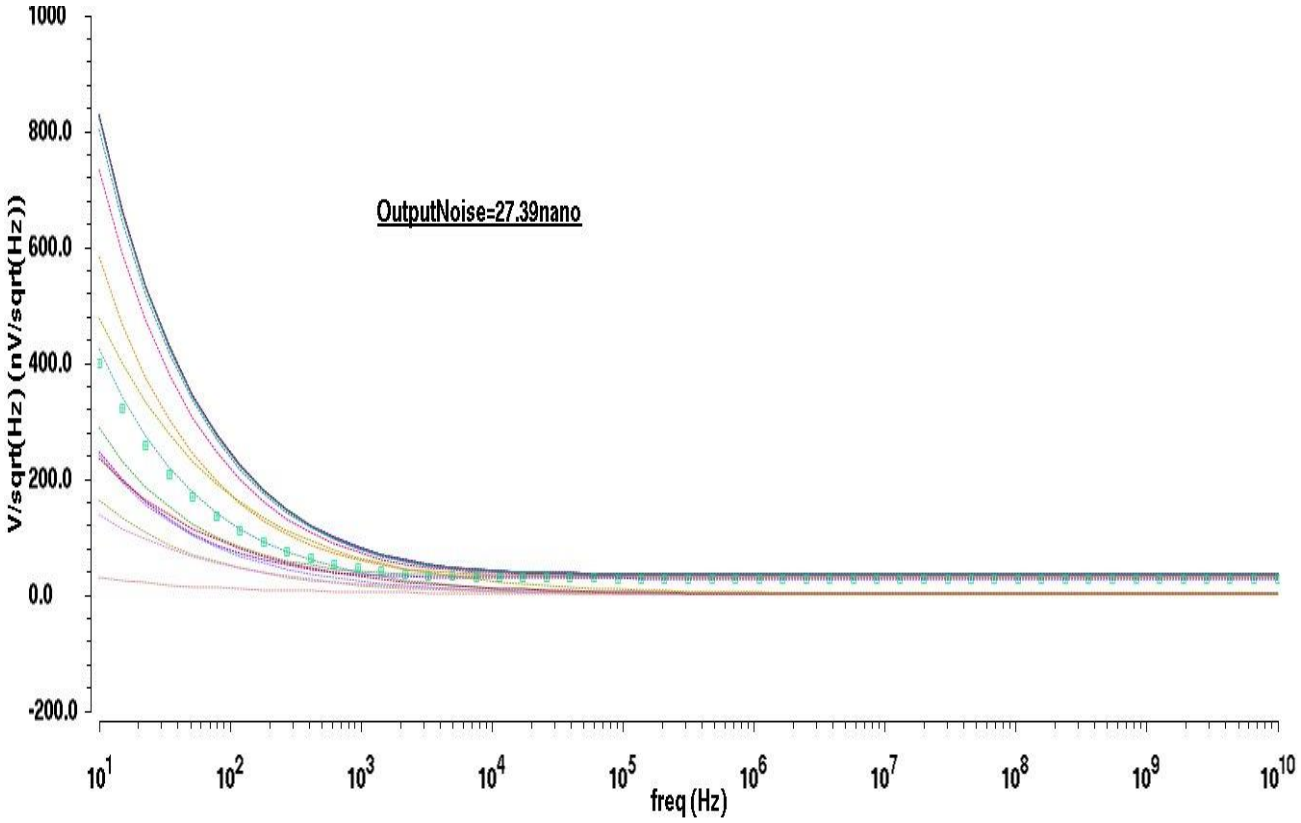
Gain and Phase Plot with respect to frequency of D-X-CCI:



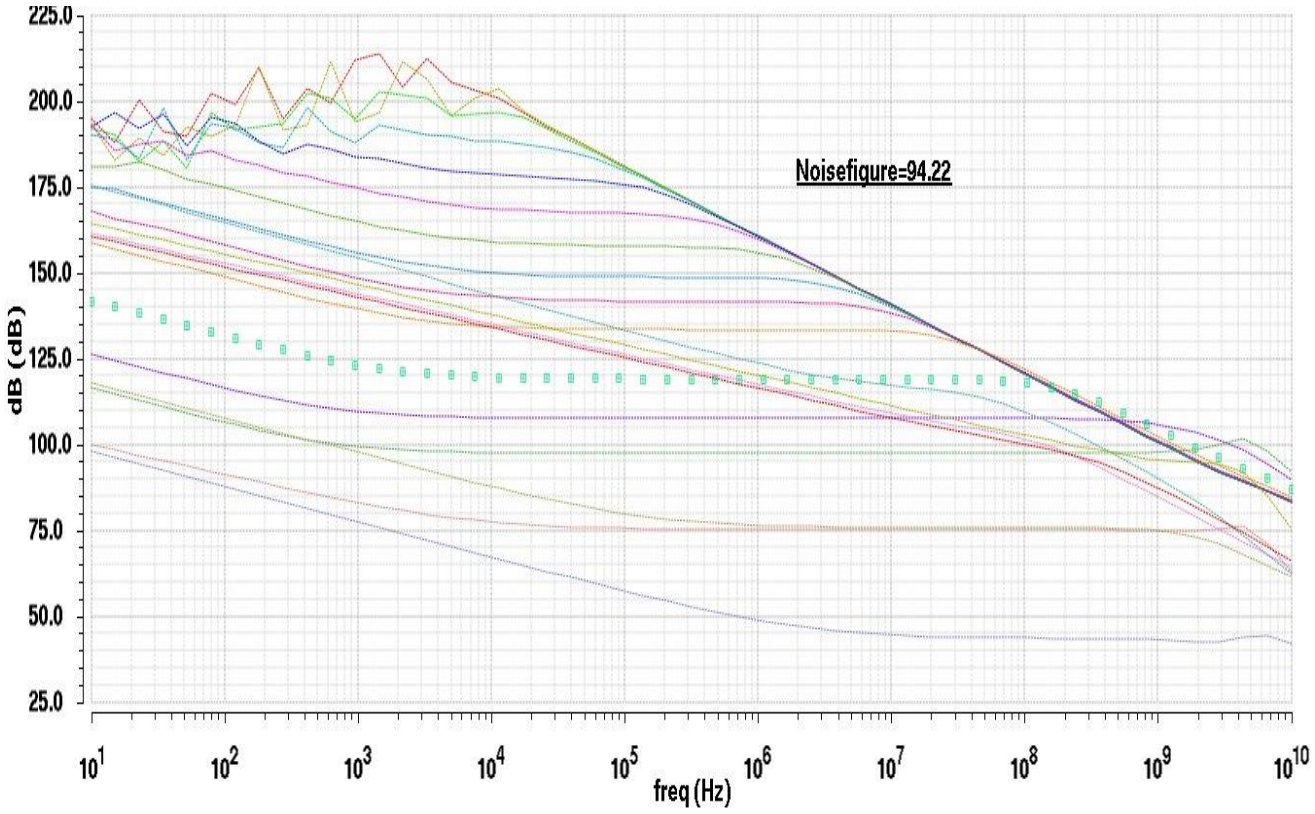
Input Noise Plot of DXCCI:



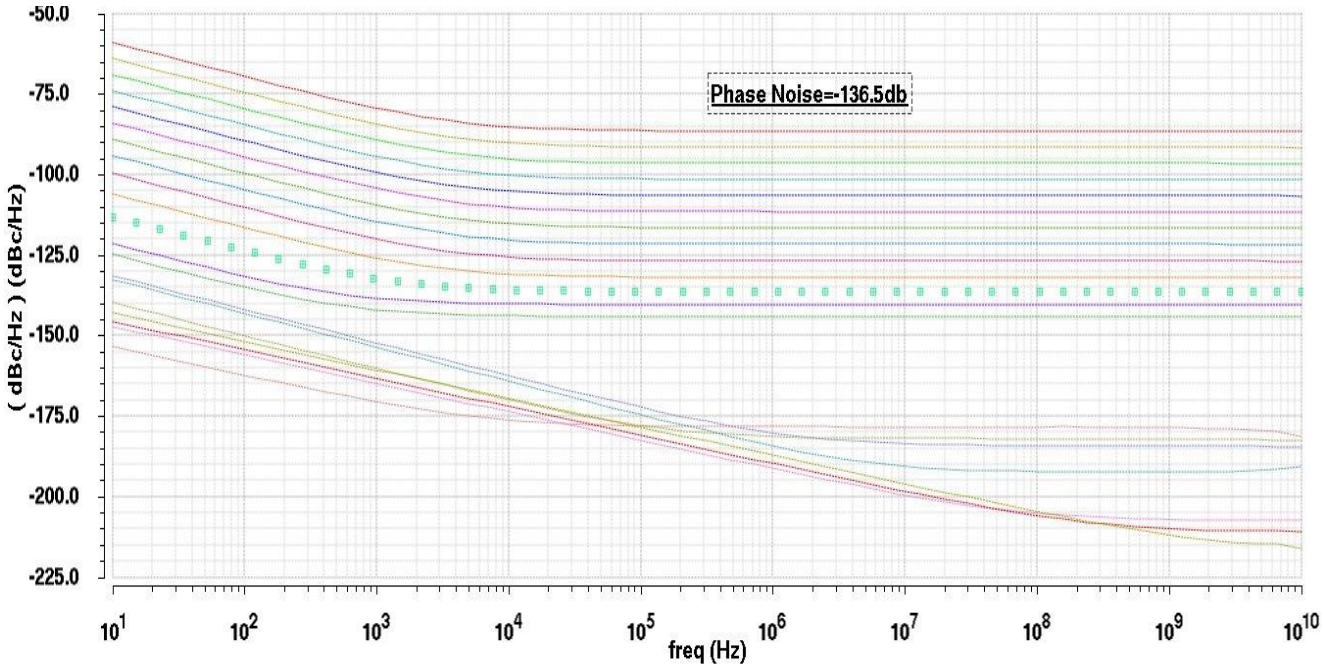
Output Noise Plot of D-X-CCI:



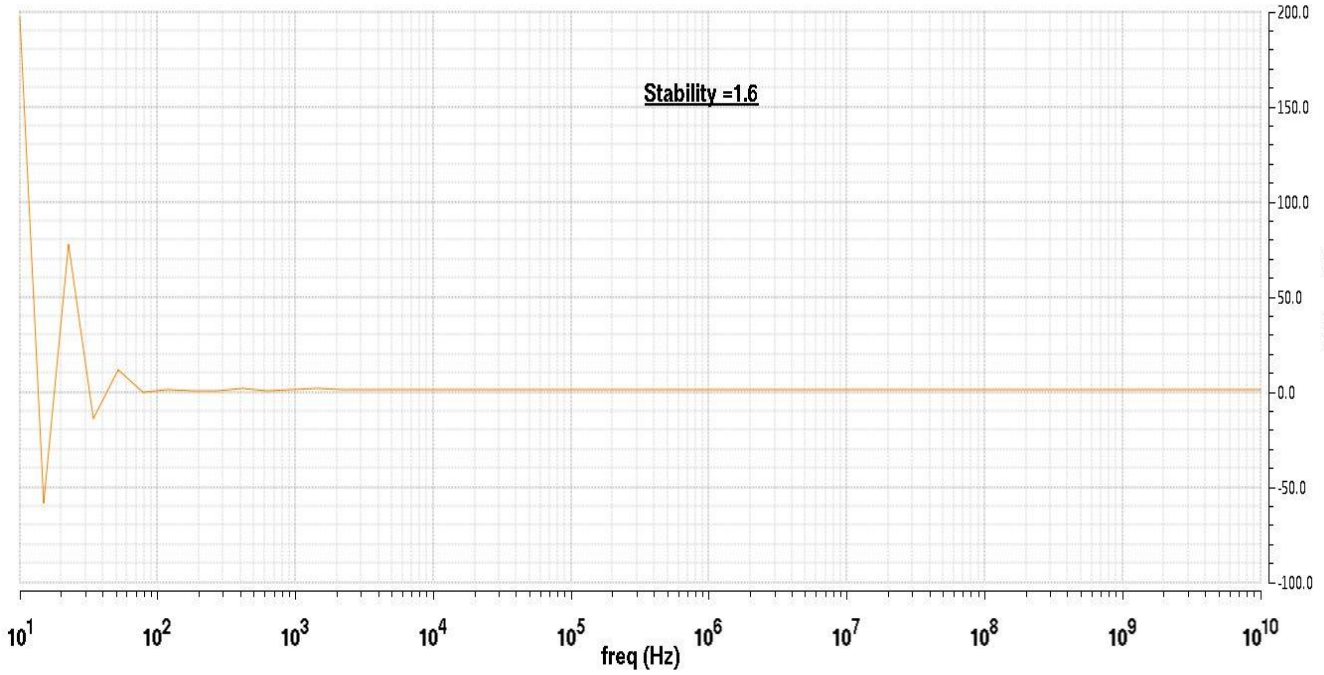
Noise Figure of DXCCI:



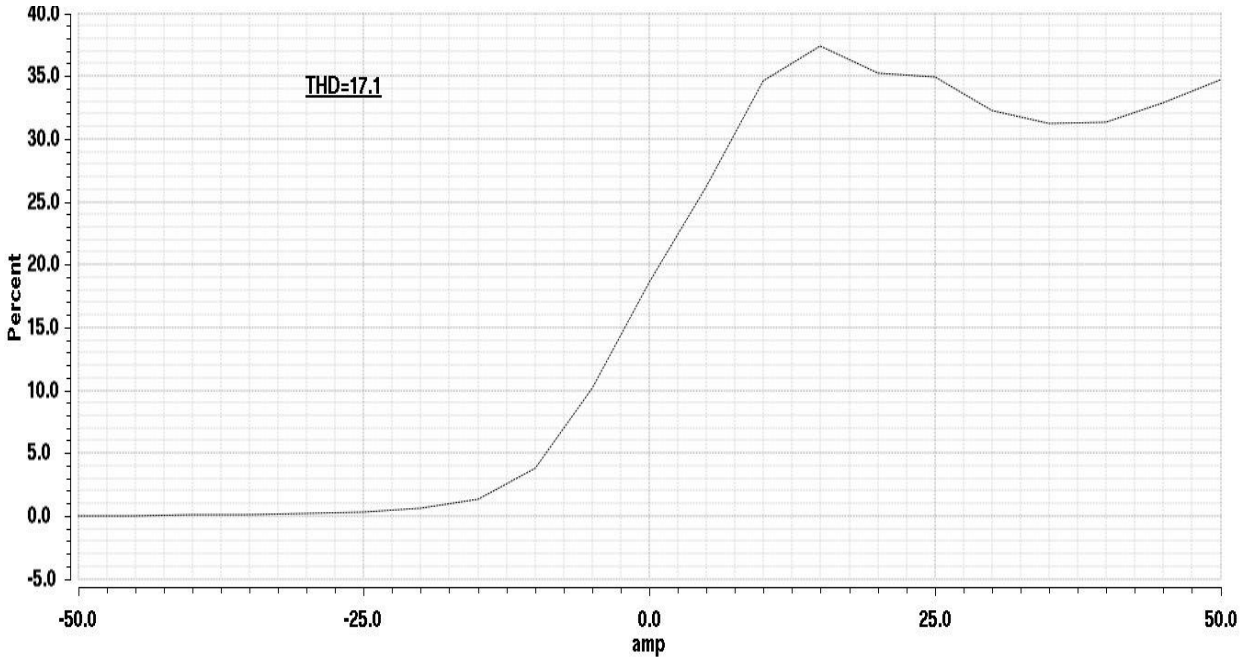
Phase Noise of DXCCI:



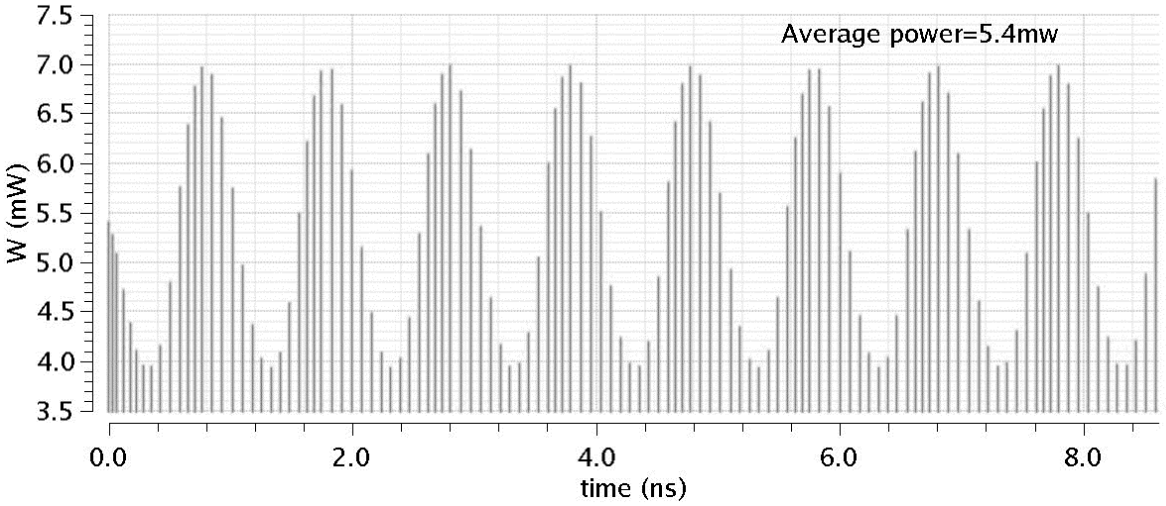
Stability of DXCCI:



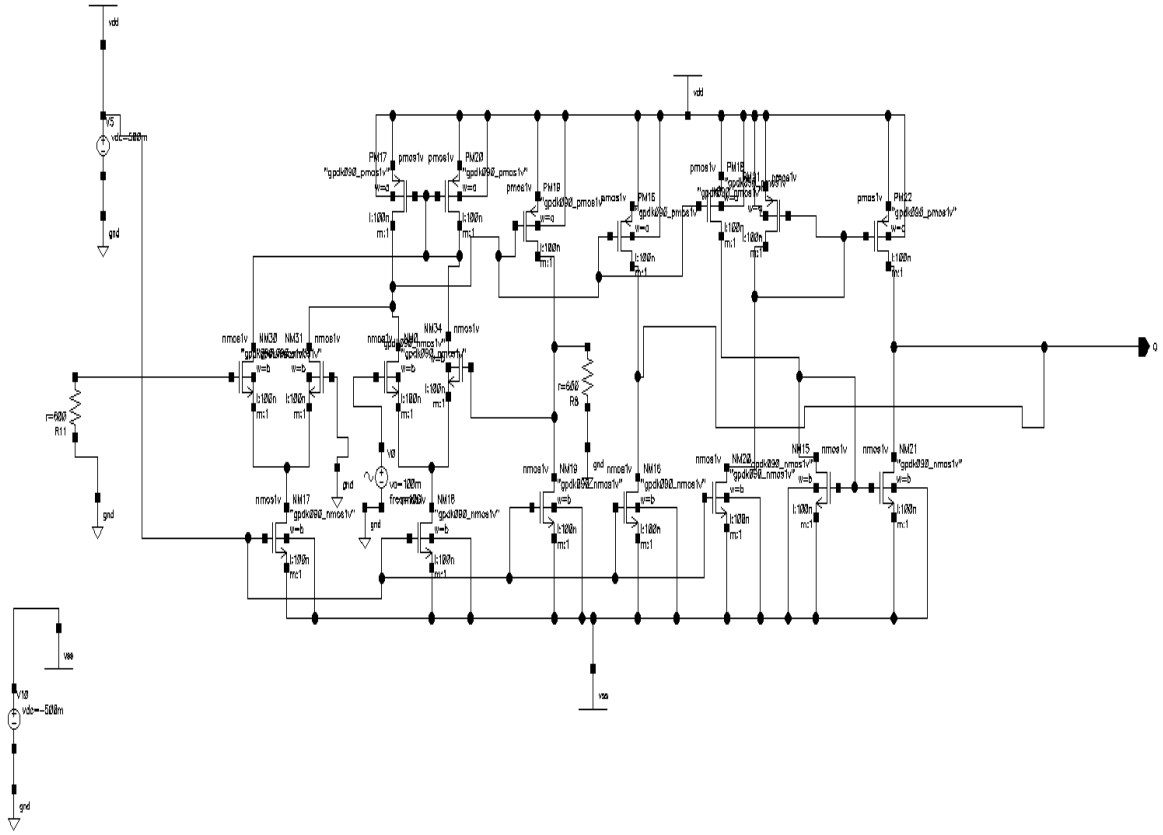
Total Harmonic Distortions of DXCCI:



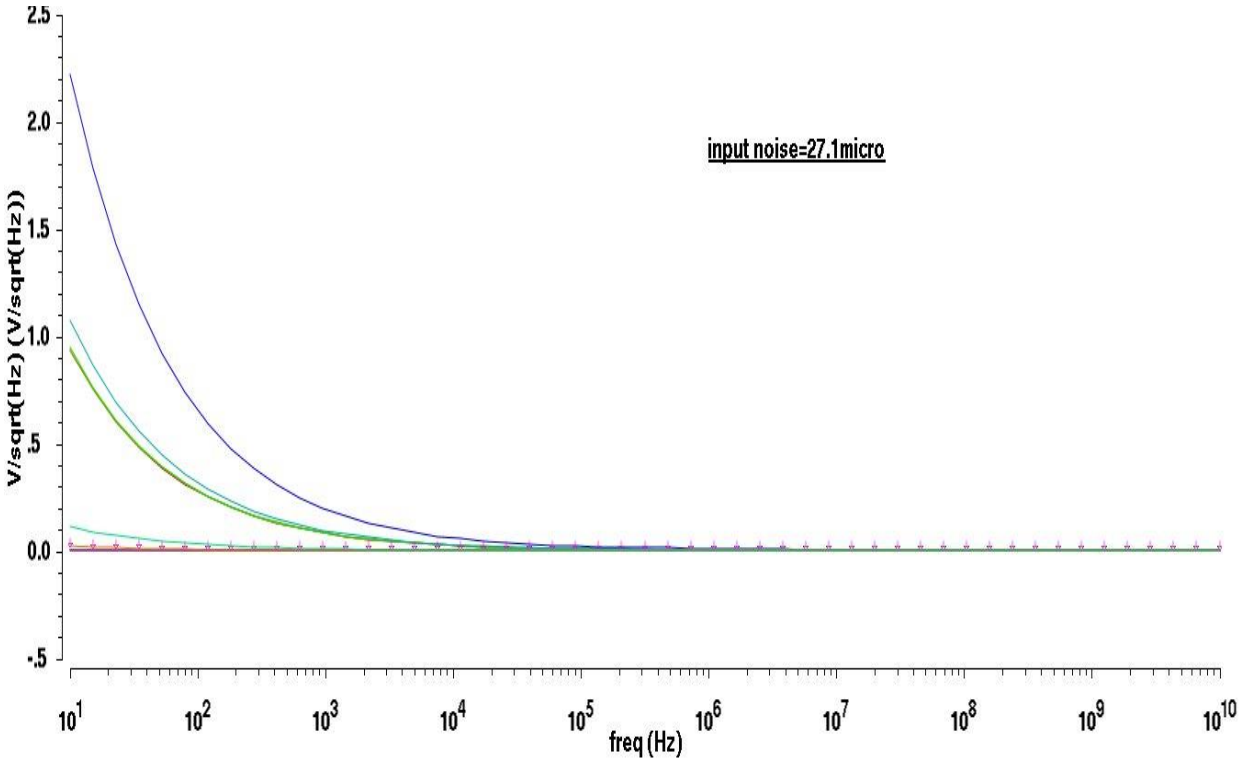
Power of D-X-CCI:



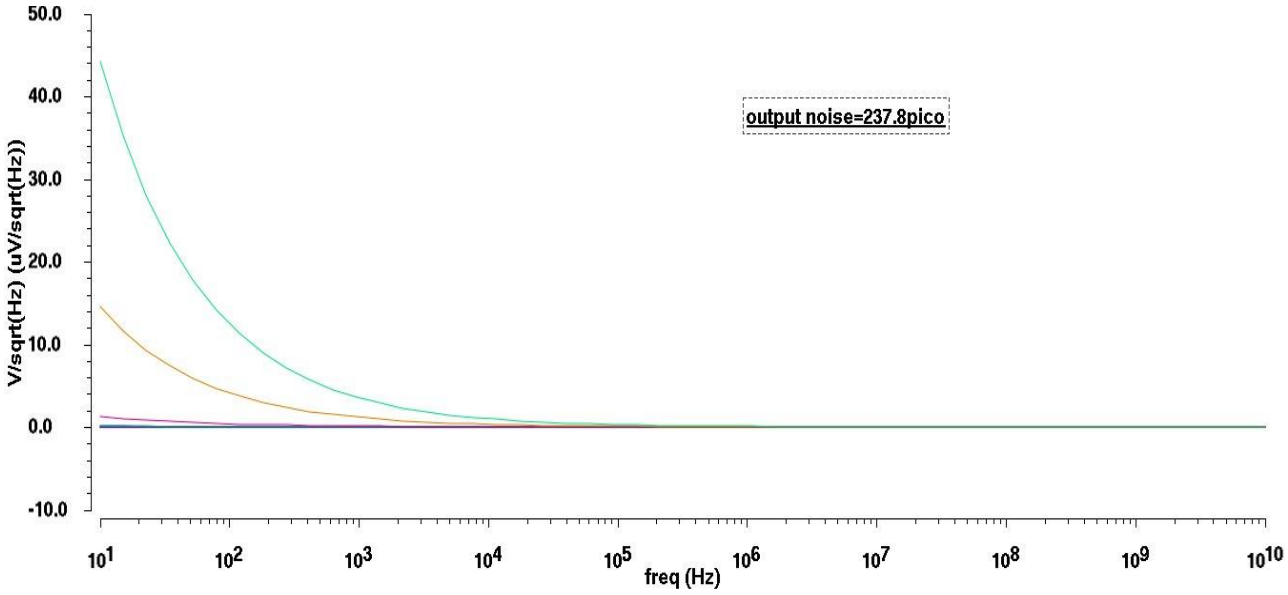
DVCC schematic:



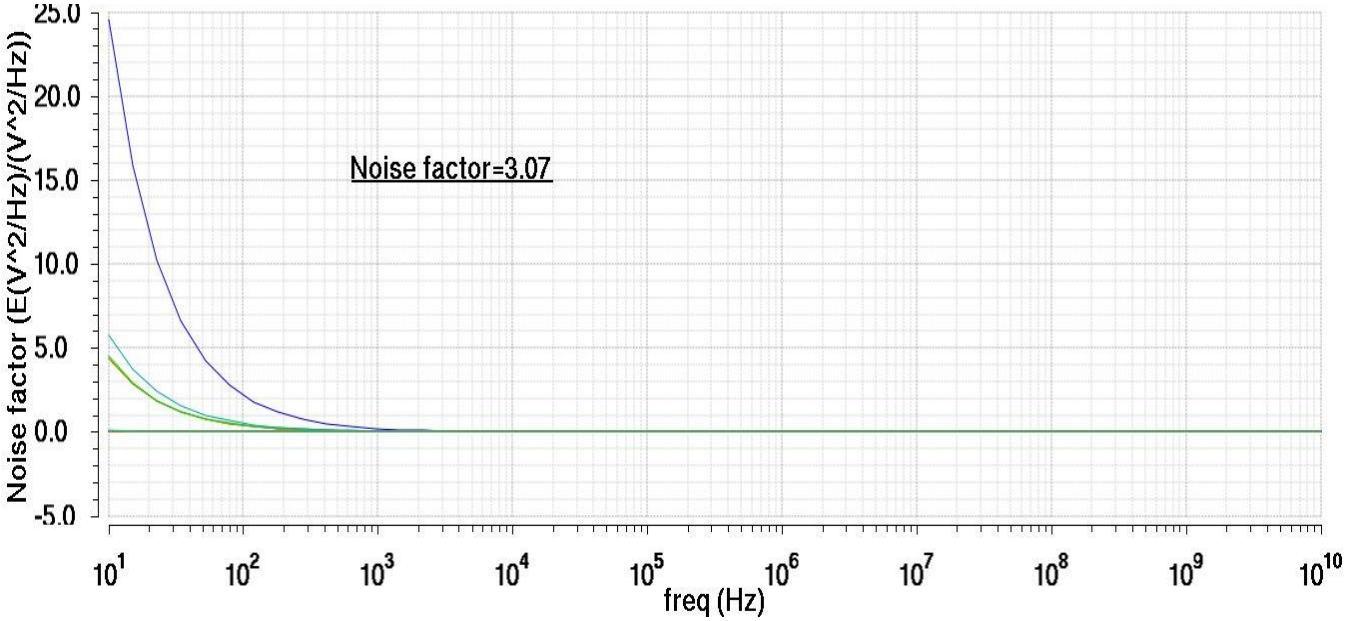
Input Noise of DVCC:



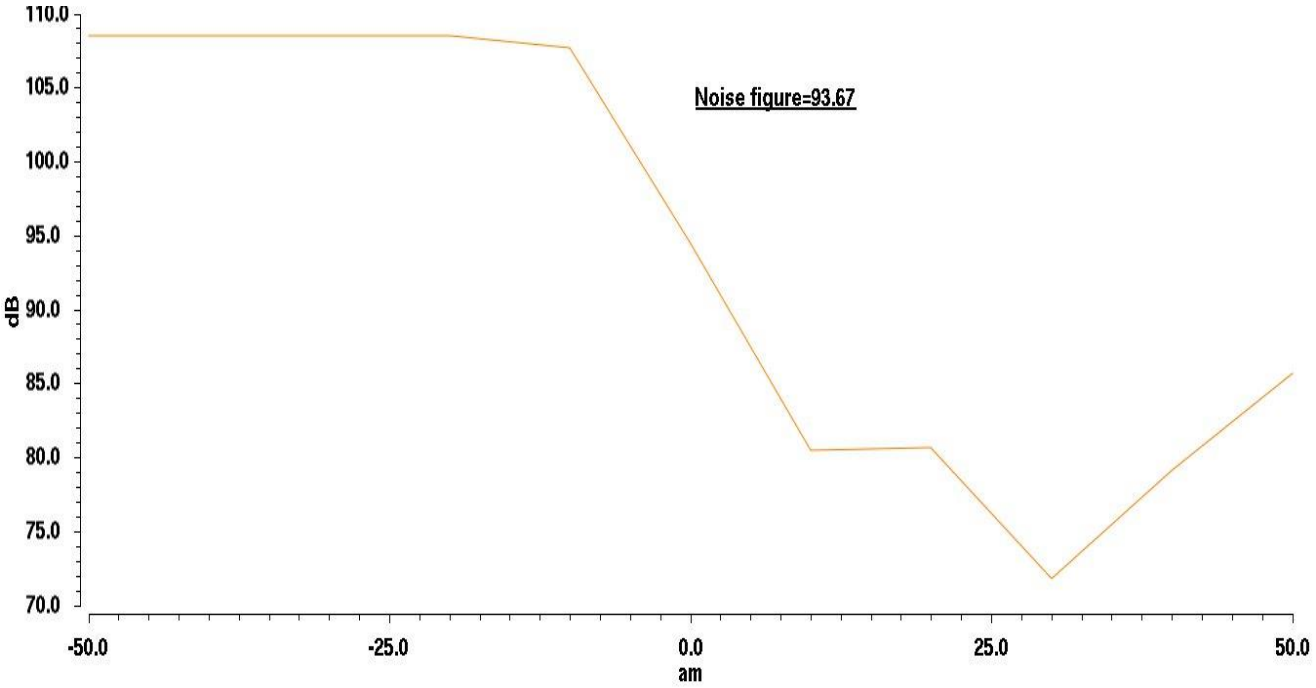
Output Noise of DVCC::



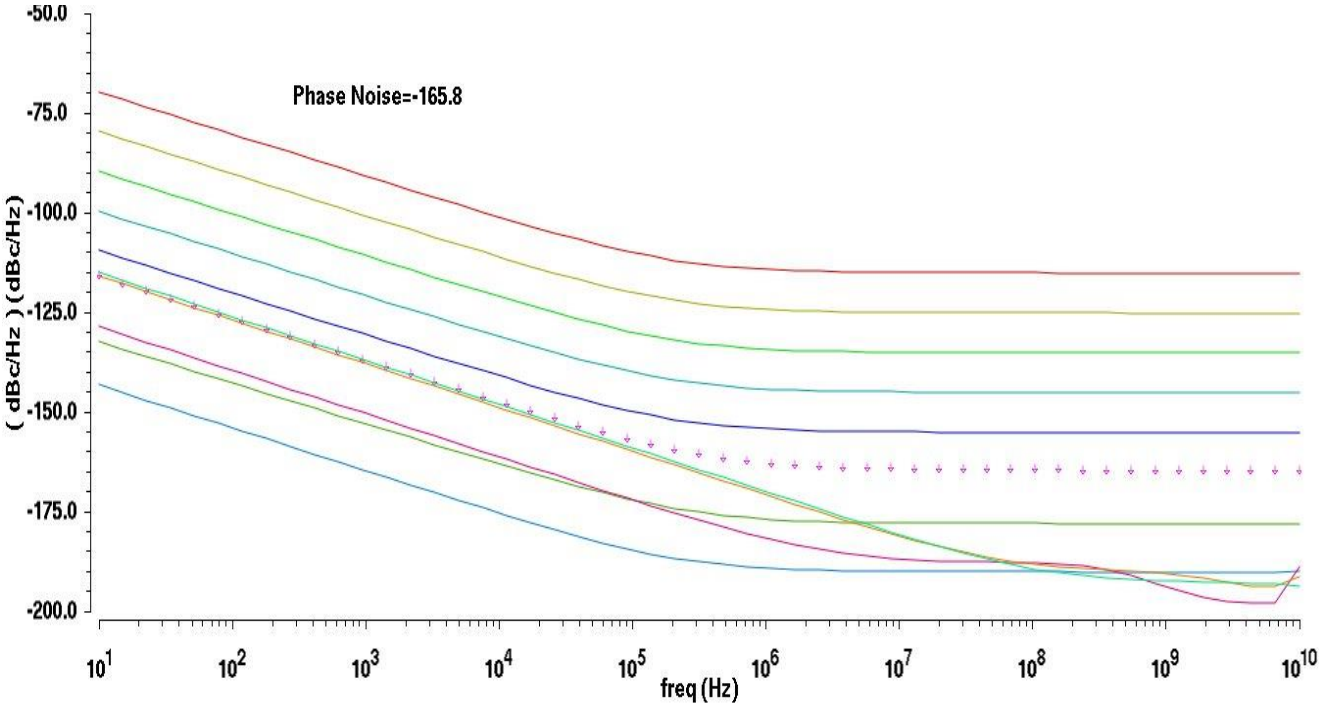
Noise Factor of DVCC::



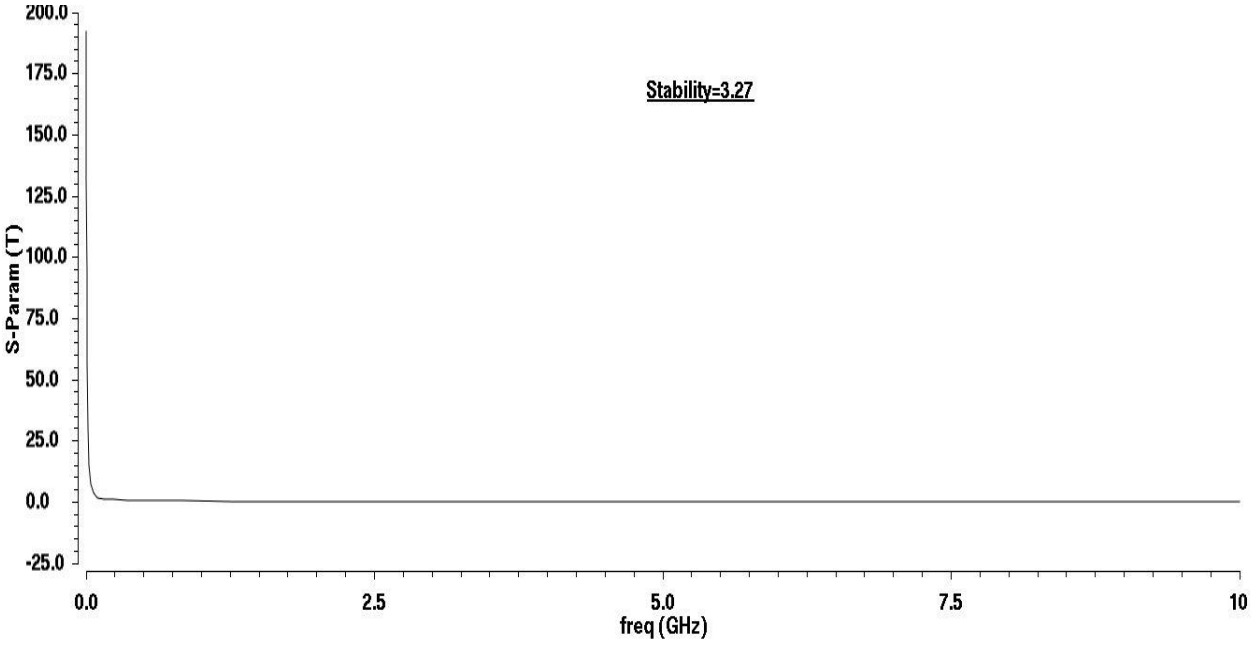
Noise Figure of DVCC::



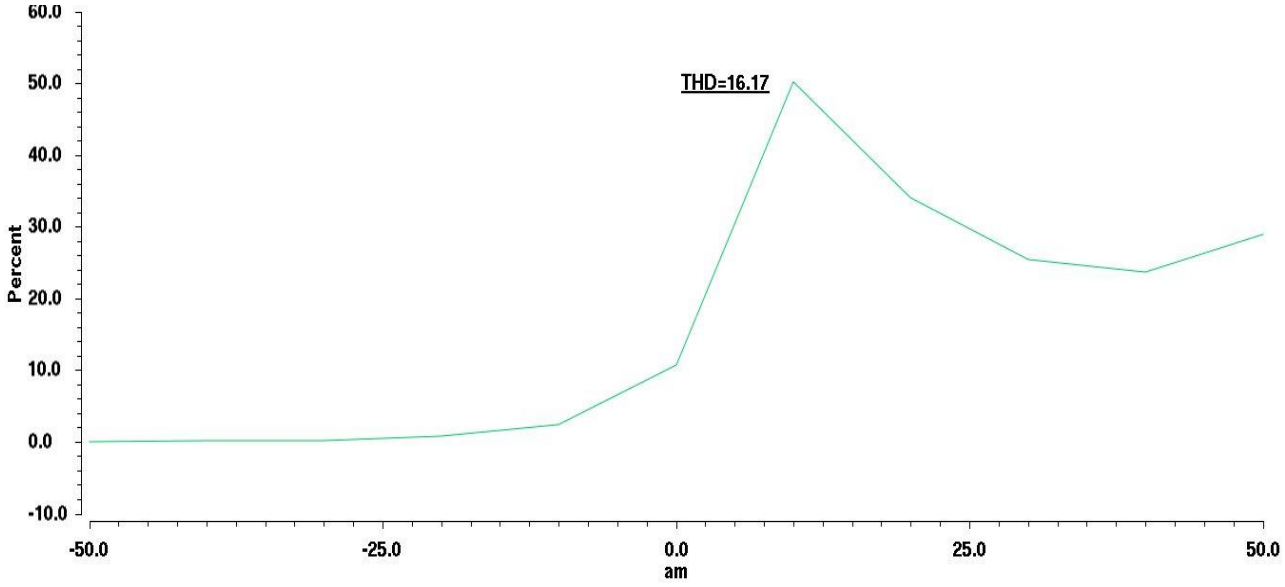
Phase Noise of DVCC::



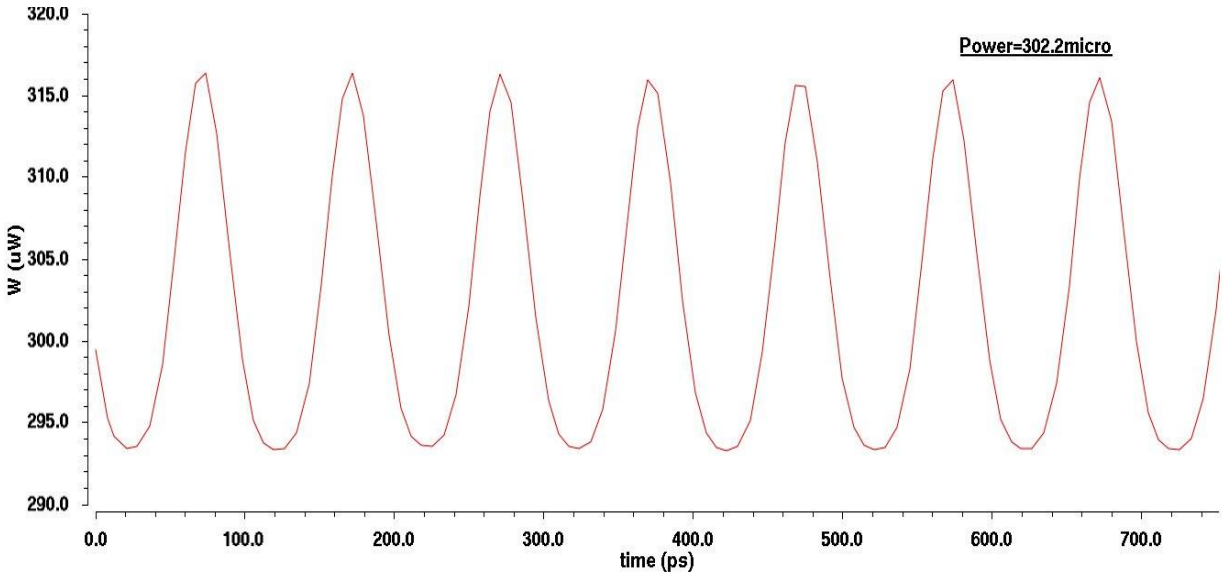
Stability of DVCC::



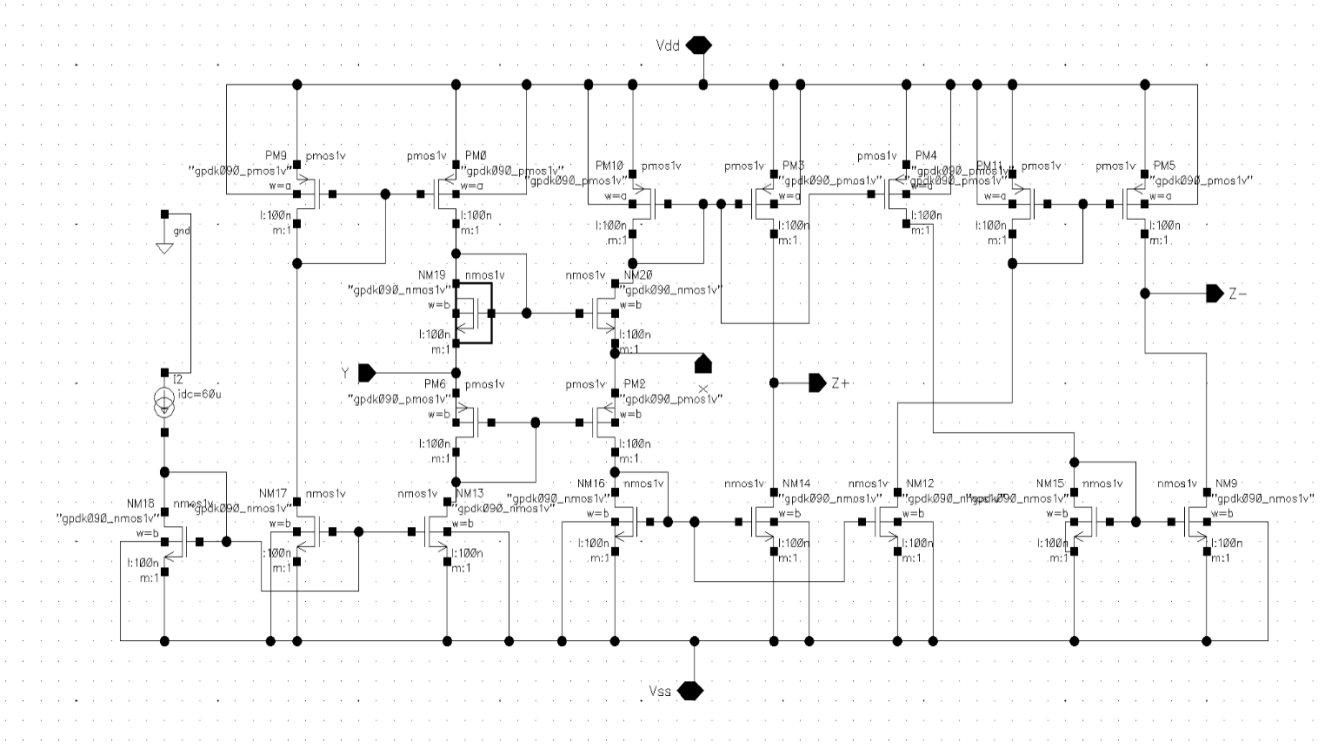
Total Harmonic Distortions of DVCC:



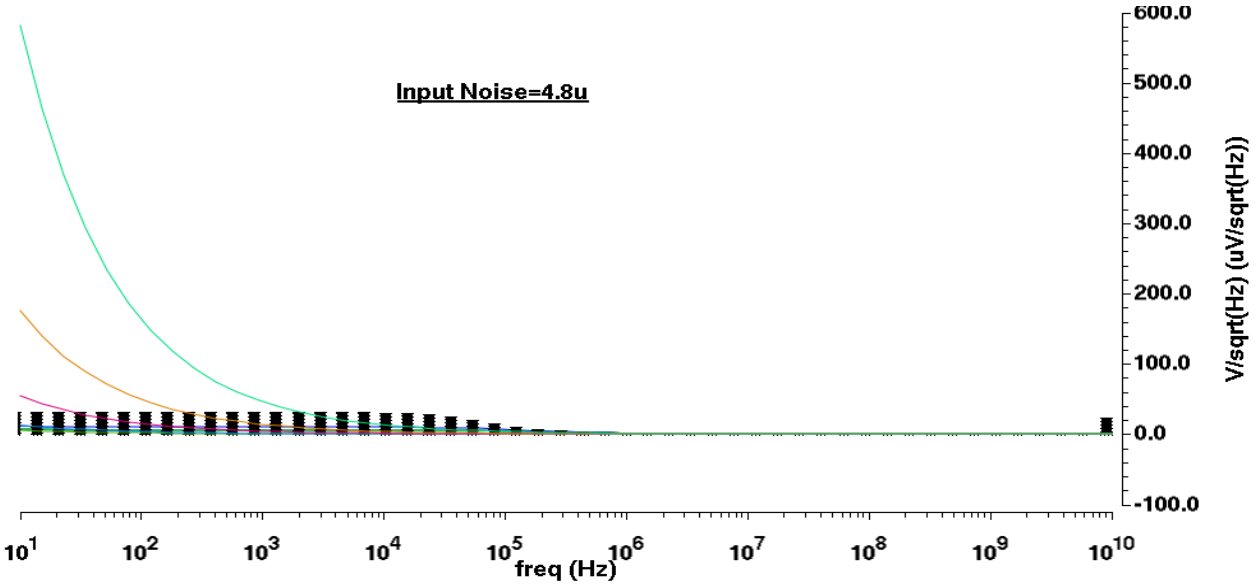
Power of DVCC:



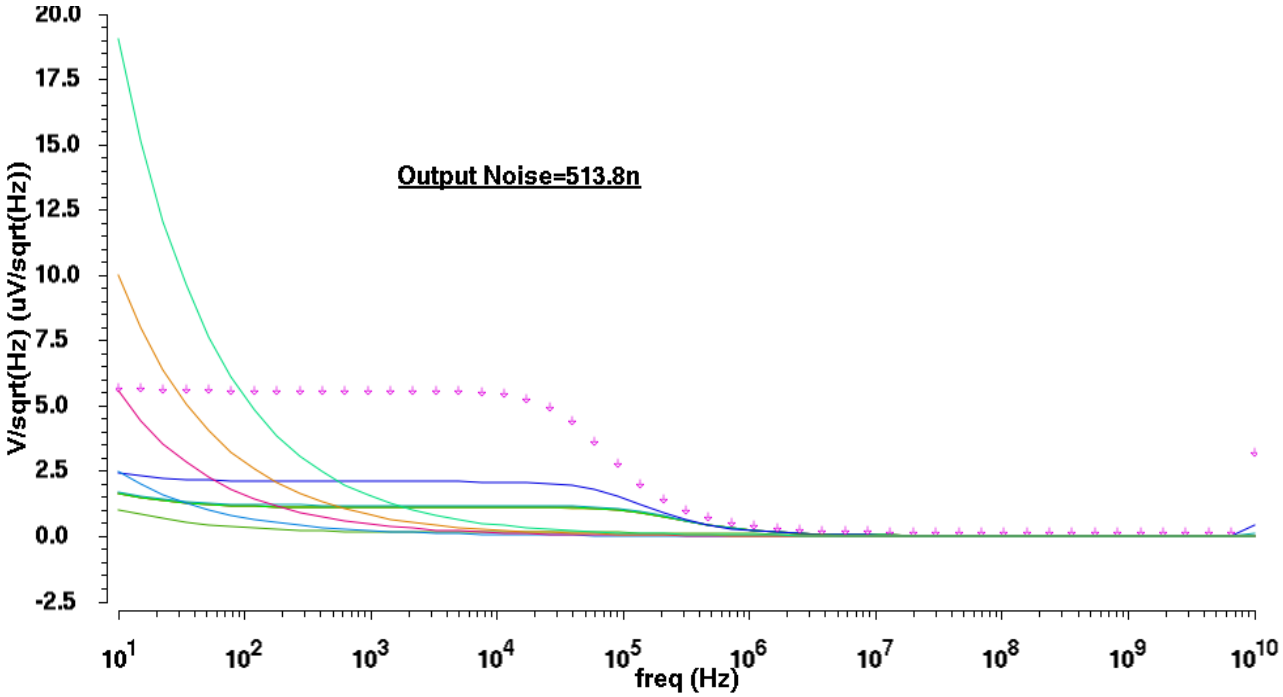
DOCCI schematic:



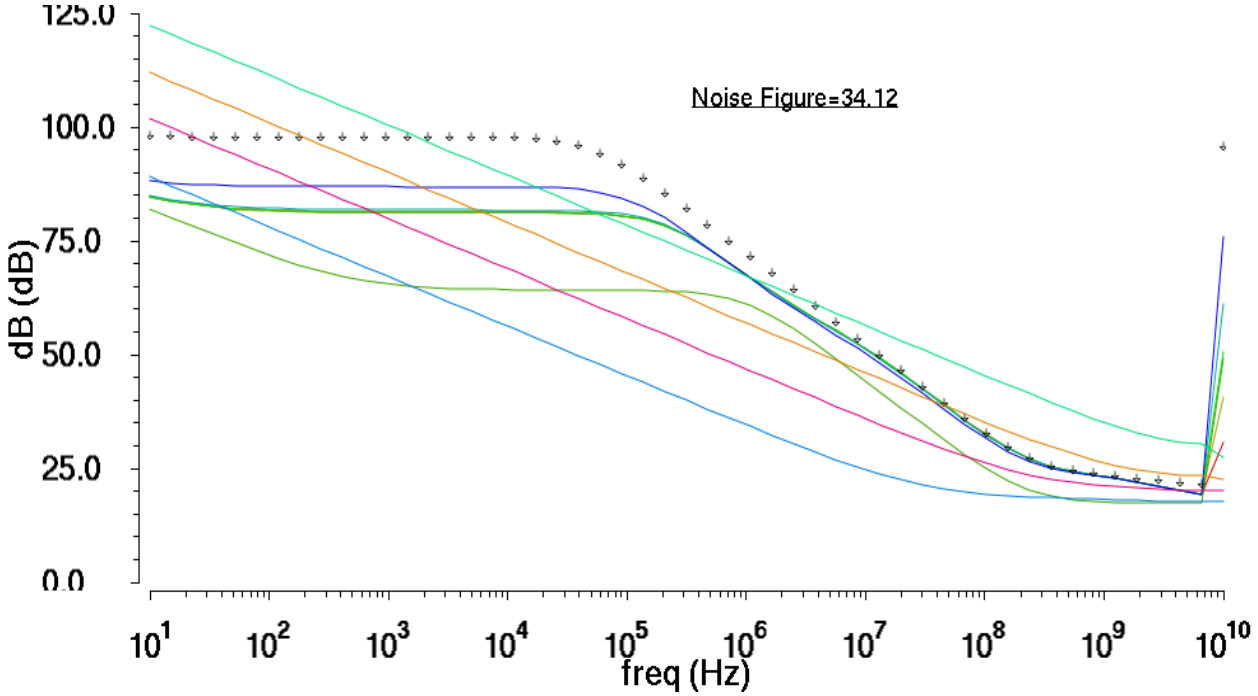
Input Noise of DOCCI :



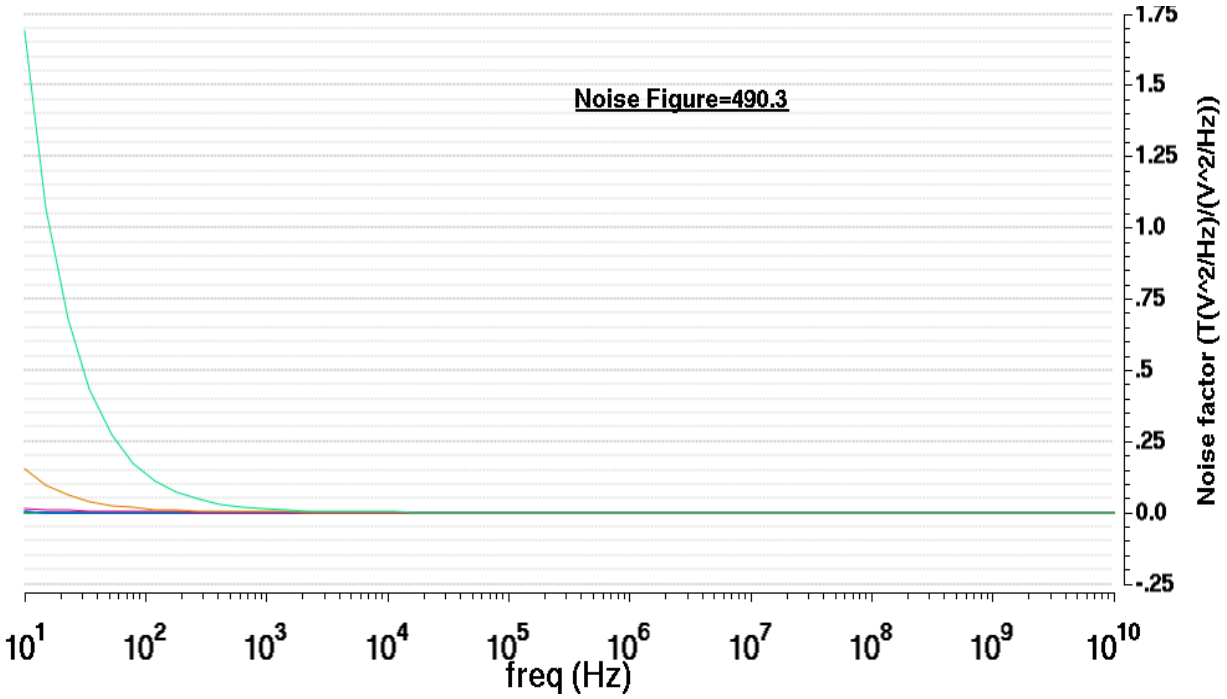
Output Noise of DOCCI:



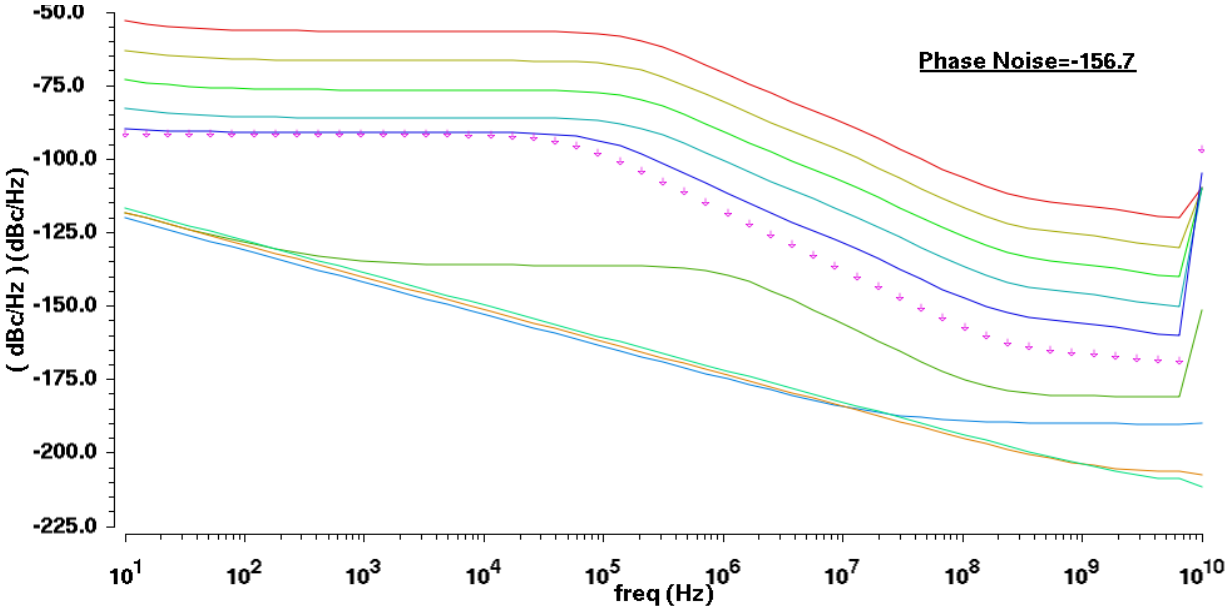
Noise Figure of DOCCI:



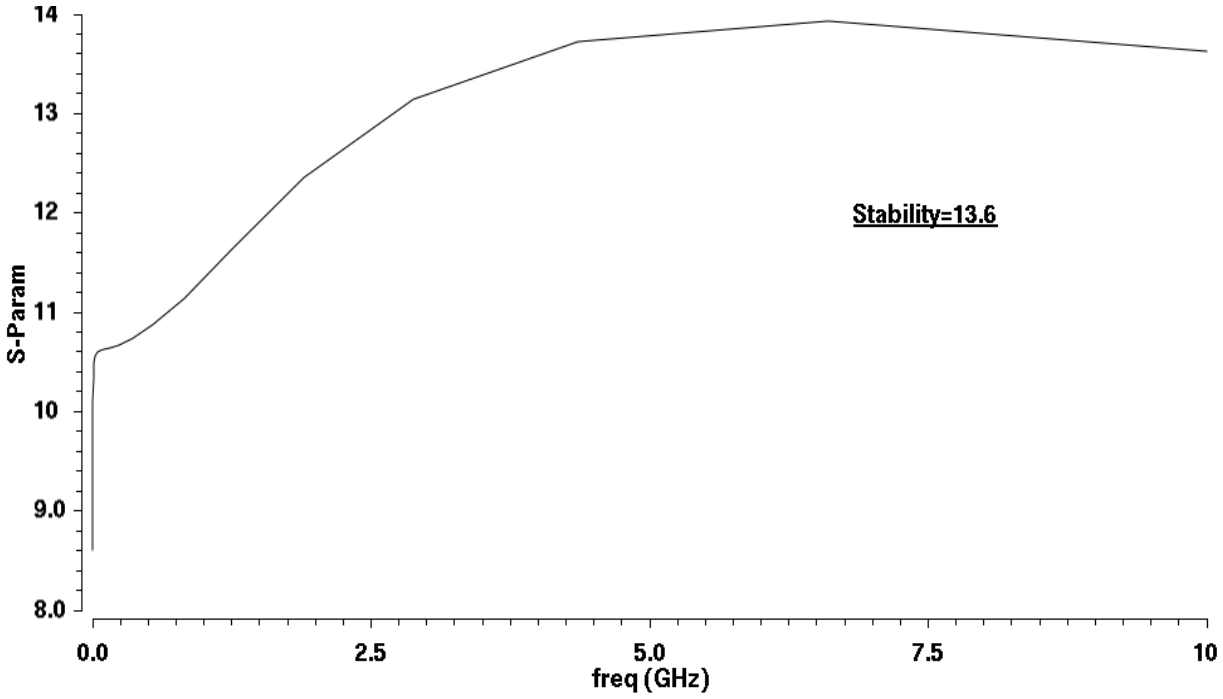
Noise Figure of DOCCI:



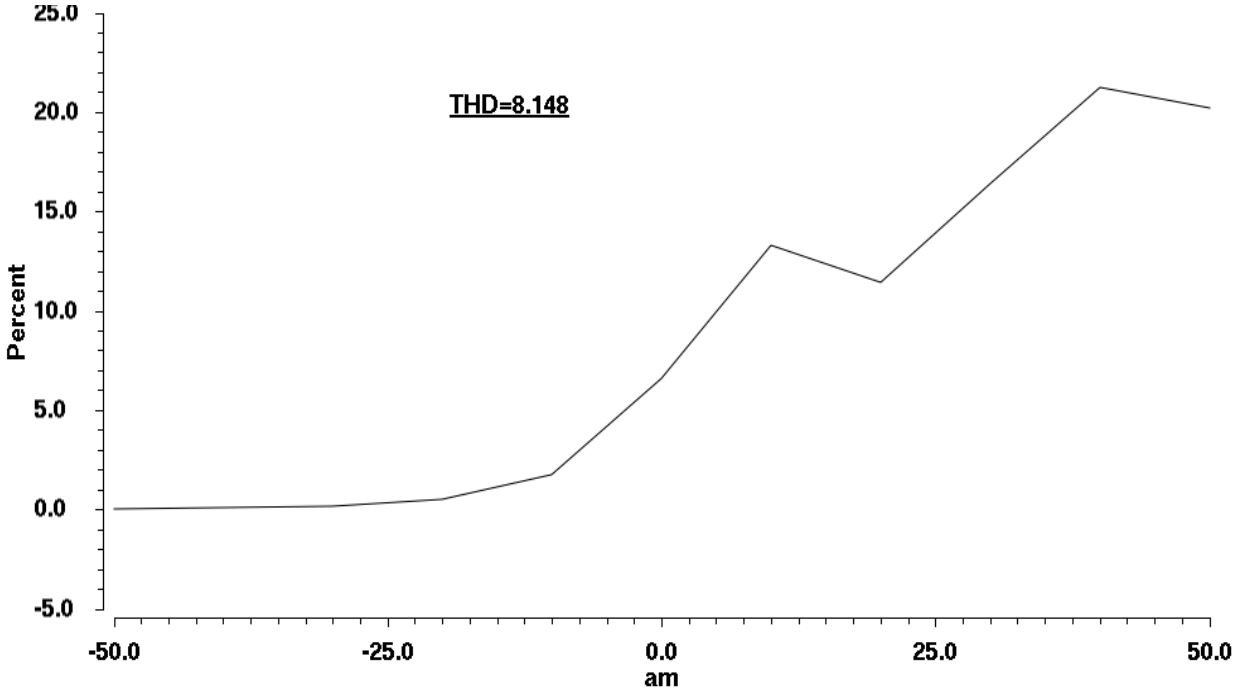
Phase Noise of DOCCI:



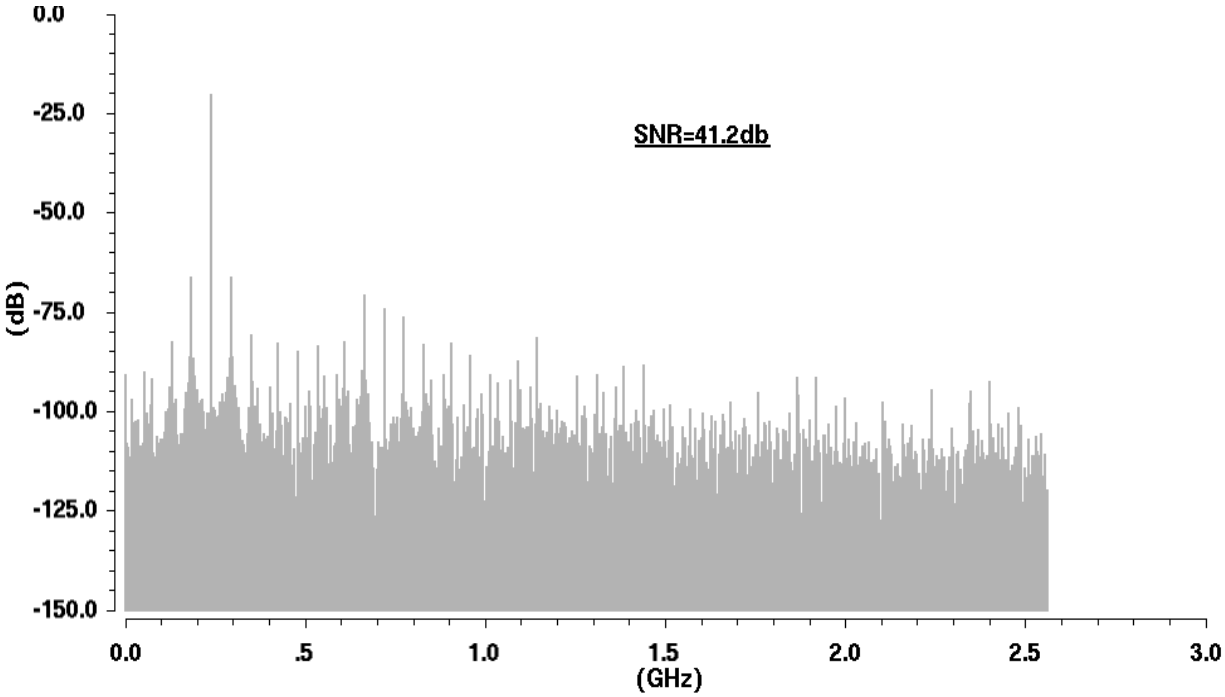
Stability of DOCCI:



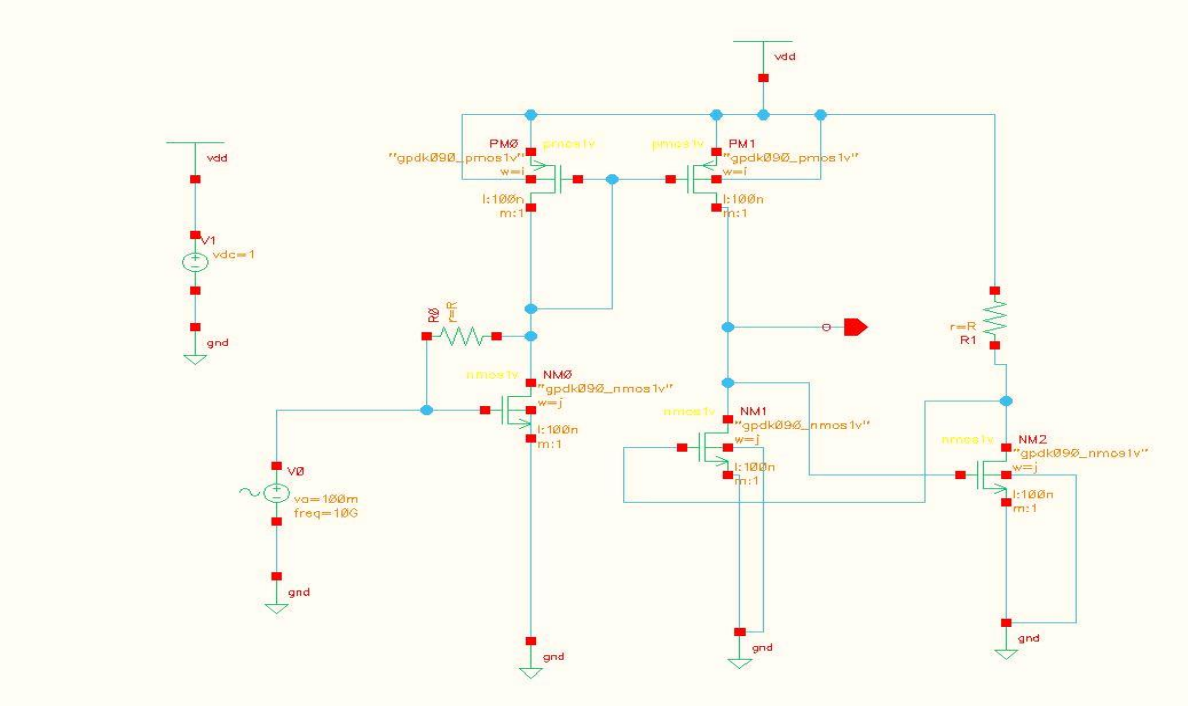
Total Harmonic Distortions of DOCCI:



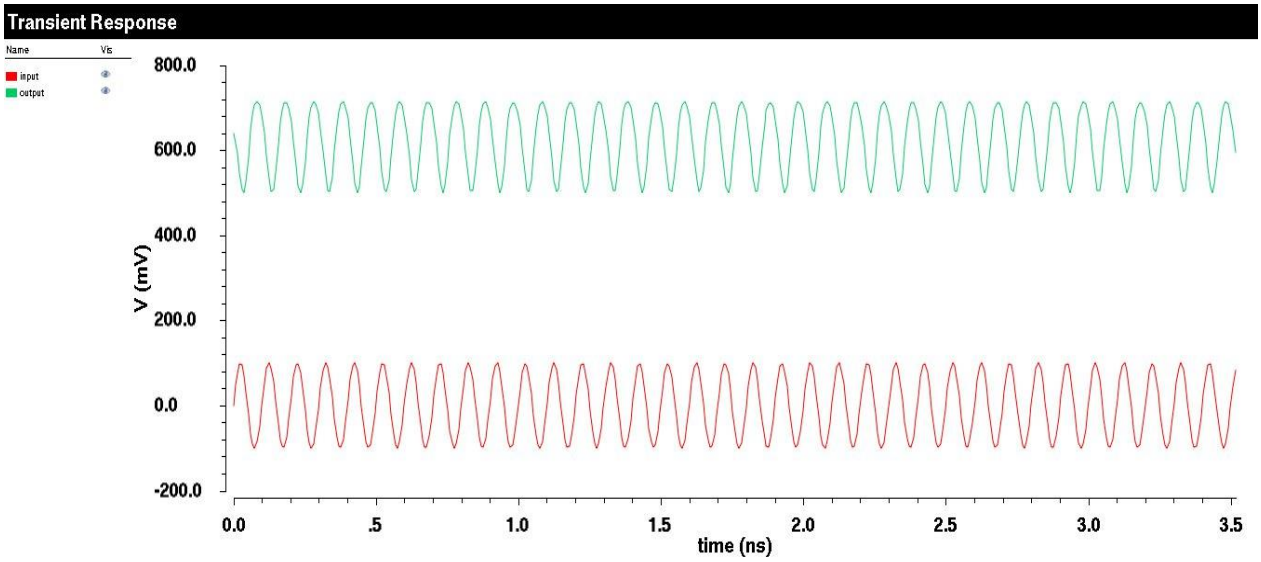
Signal-to-Noise Ratio of DOCCI:



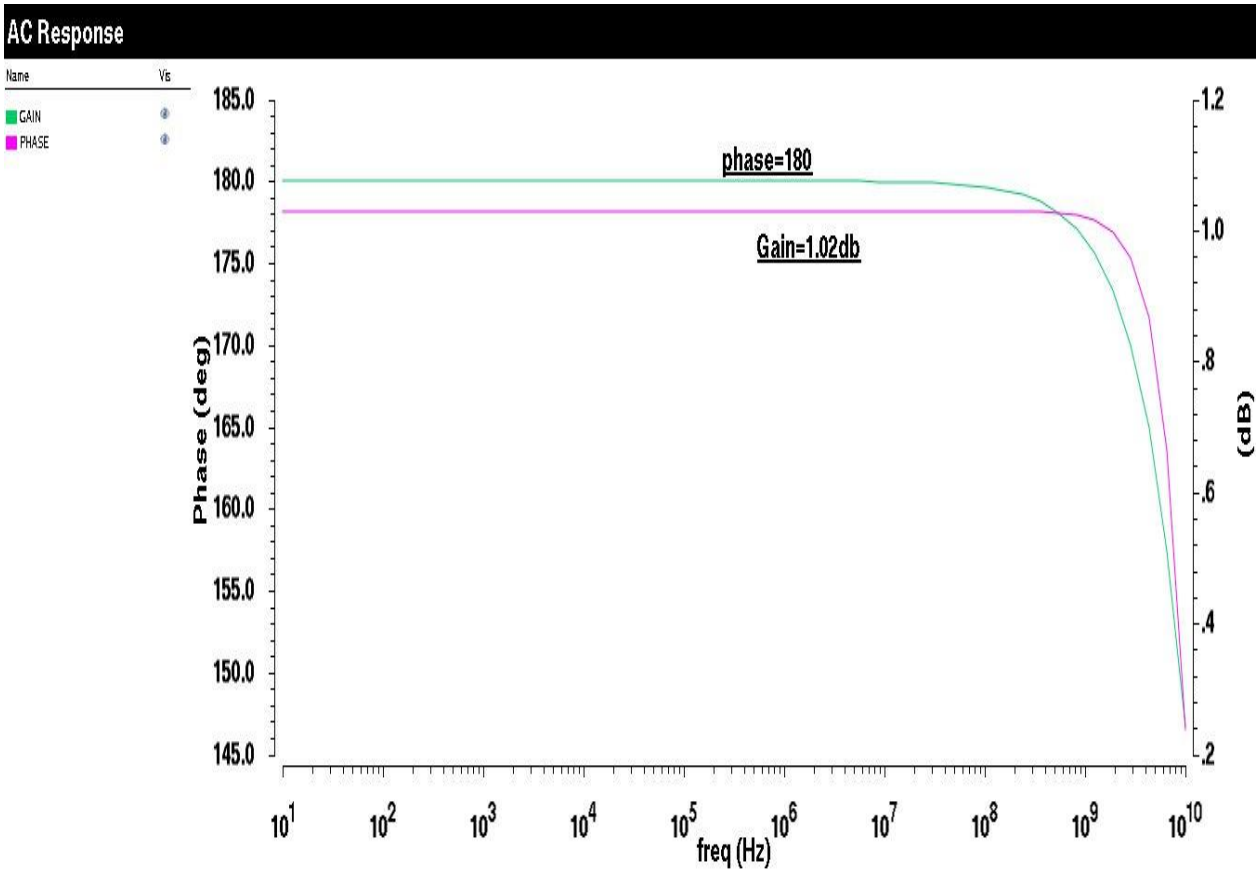
Five Transistor Proposed Model:



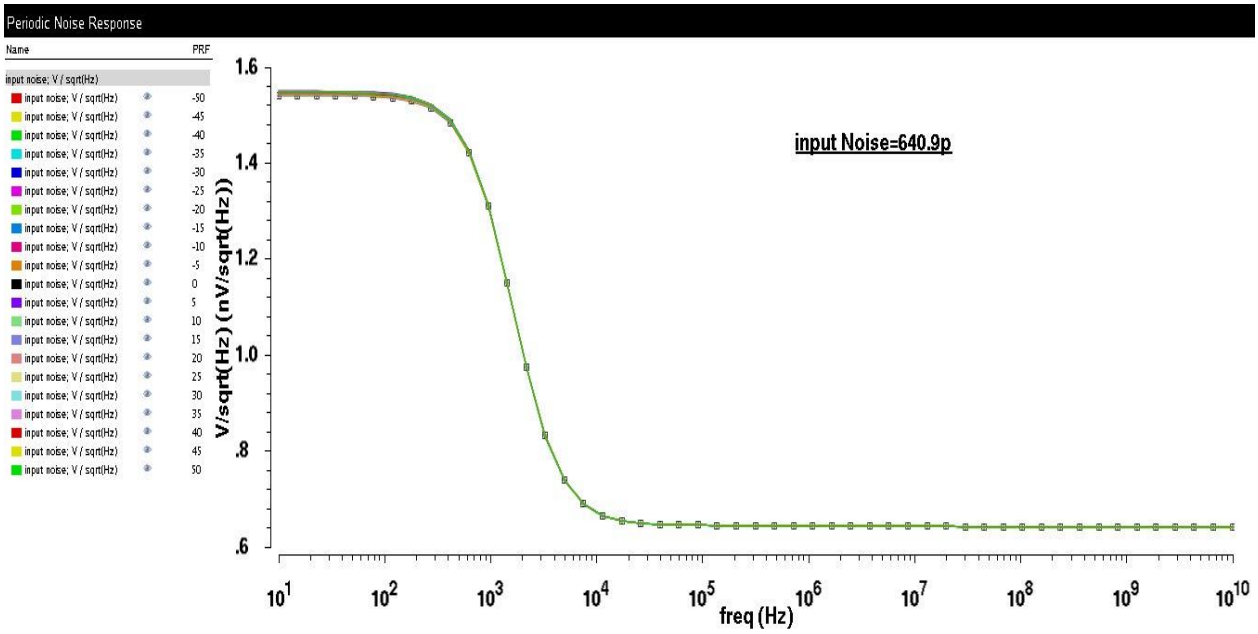
Transient Response of Five Transistor Model:



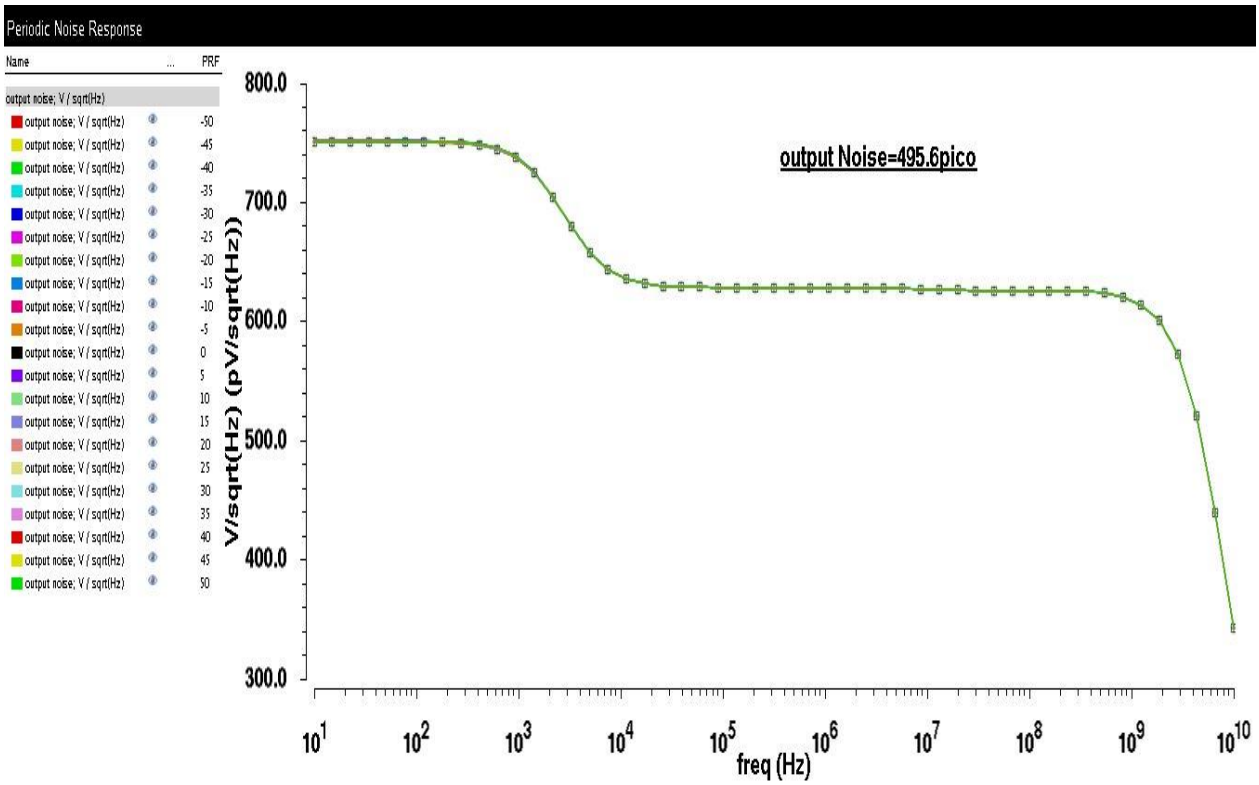
Gain and Phase Plot of Five Transistor Model:



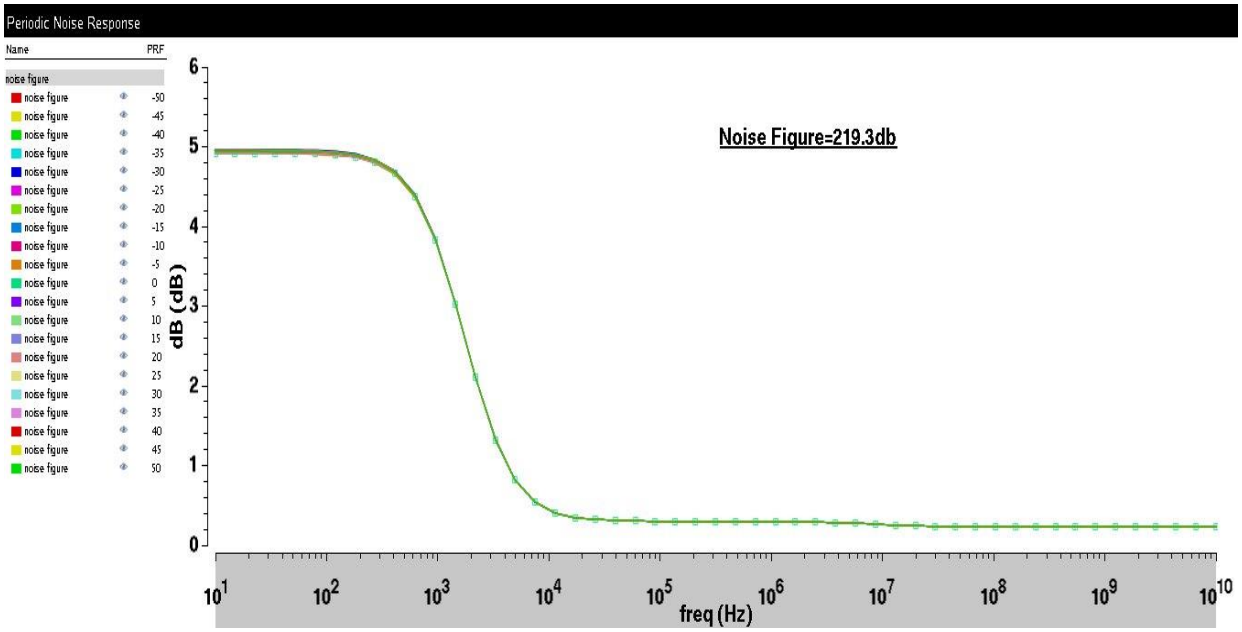
Input Noise of Five Transistor Model:



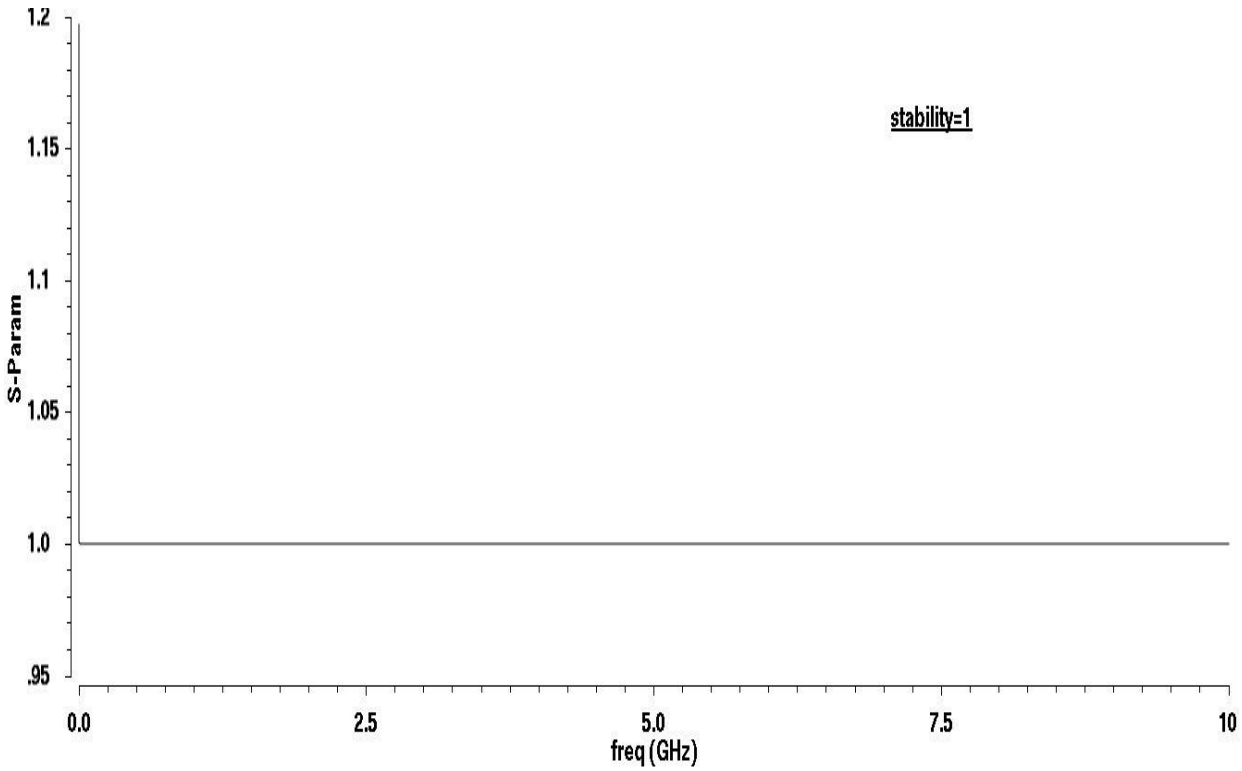
Output Noise of Five Transistor Model:



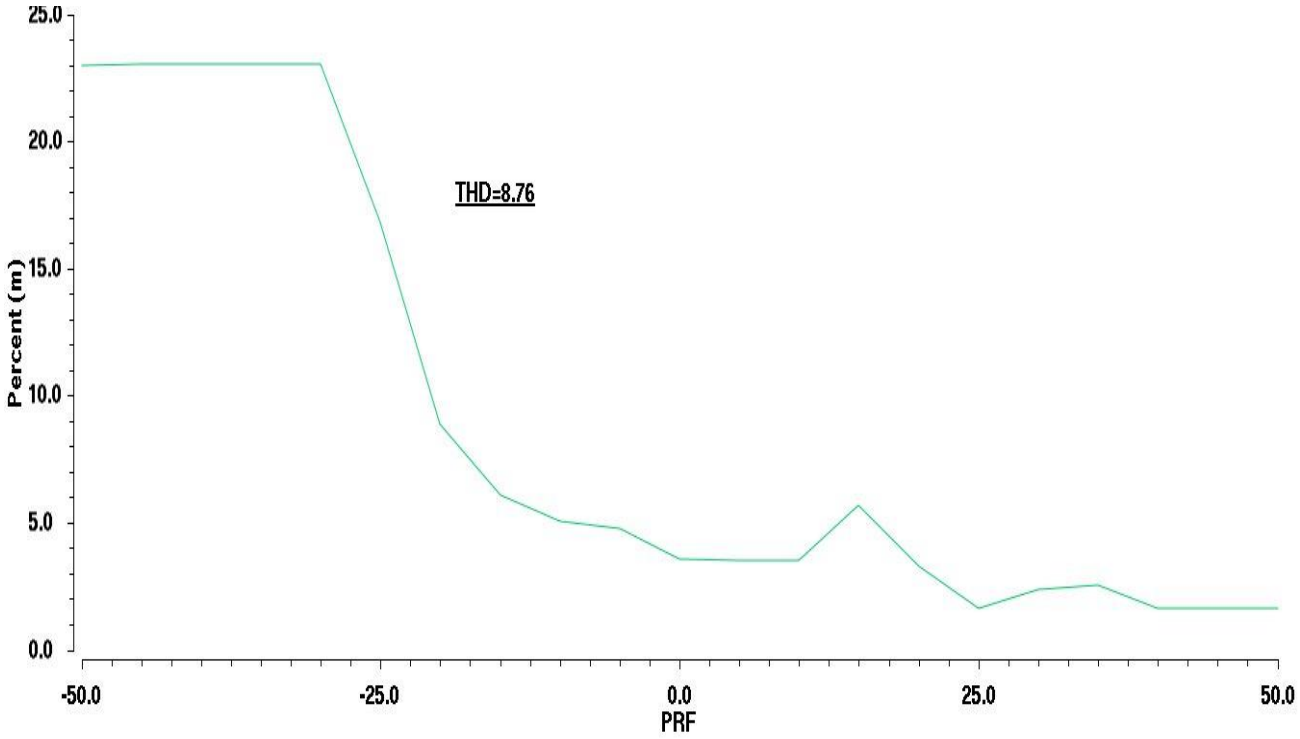
Noise Figure of Five Transistor Model:



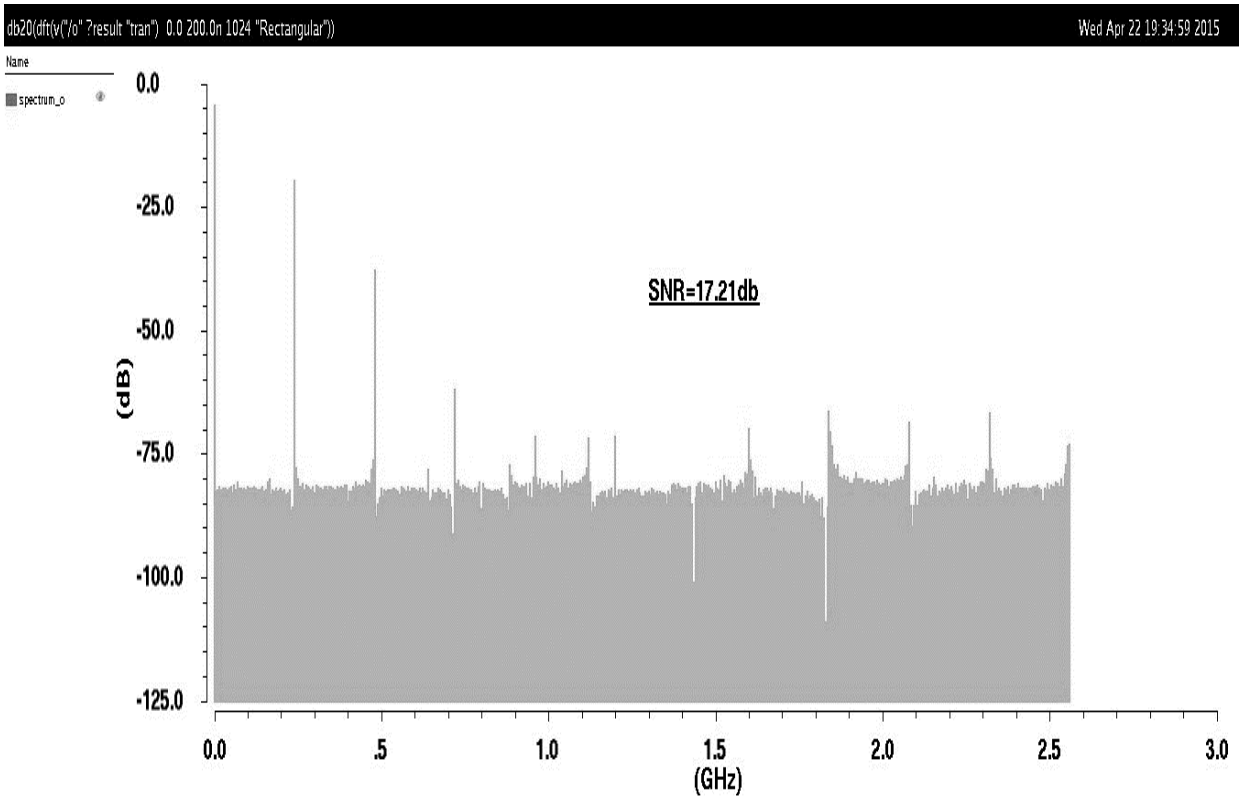
Stability of Five Transistor Model:



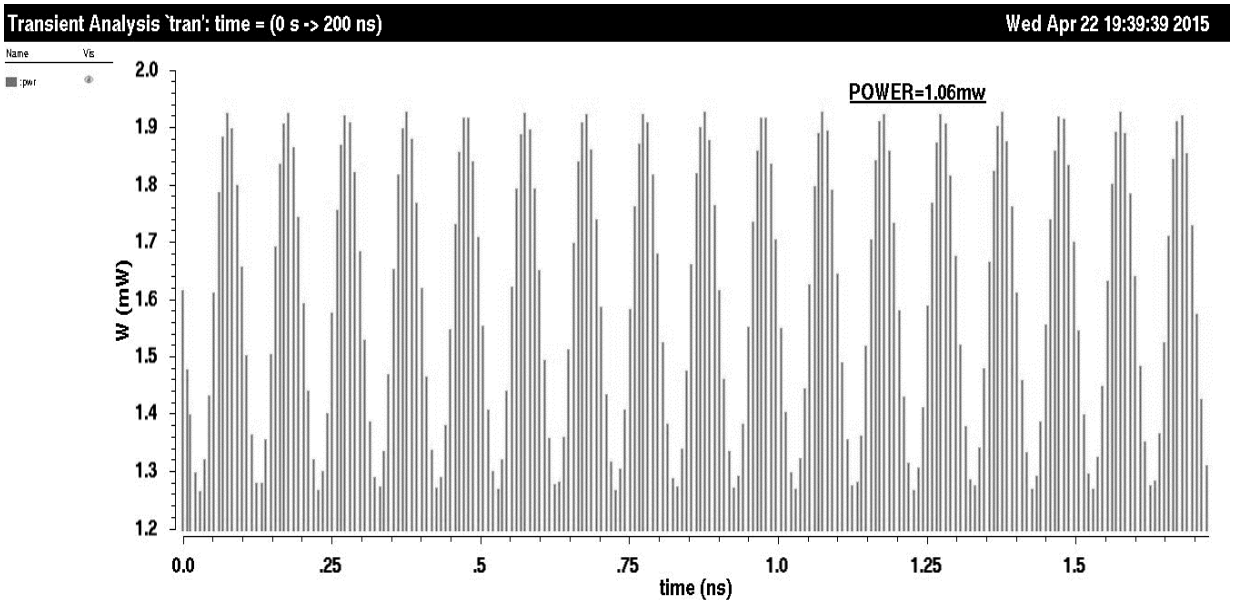
Total Harmonic Distortions of Five Transistor Model:



Signal-to-Noise Ratio of Five Transistor Model:



Power of Five Transistor Model:



Performance and Evaluation of all the proposed Models:

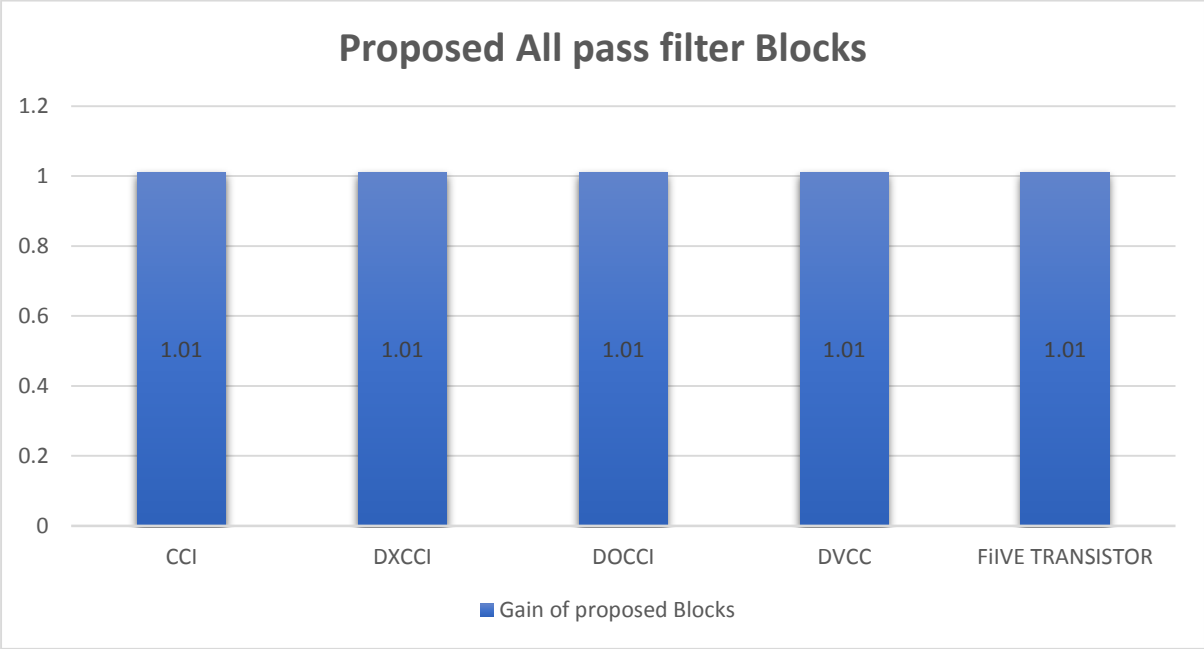
All Pass Block	Power (watts)	Input noise (dB)	Output noise (dB)	Noise Factor (dB)	Noise figure	Stability	THD (%)	Phase noise (dB)
CCI	1.5m	22.6p	555.6n	258.3	90.3M	6.9	7.45	-132.67
DXCCI	812.6u	4.8p	513.8n	490.3	490.3	13.6	8.148	-156.7
DVCC	302.2u	27.1p	237.8P	3.07	93.67	3.27	16.17	-165.8
DOCCI	5.4m	31.34p	27.39n	23.6	94.22	1.6	17.41	-136.5
Five Transistors Model	1.06m	640.9P	495.6P	16.23	219.3	2.4	8.76	-173.8

Table 7.1 Evaluation of proposed all pass filters

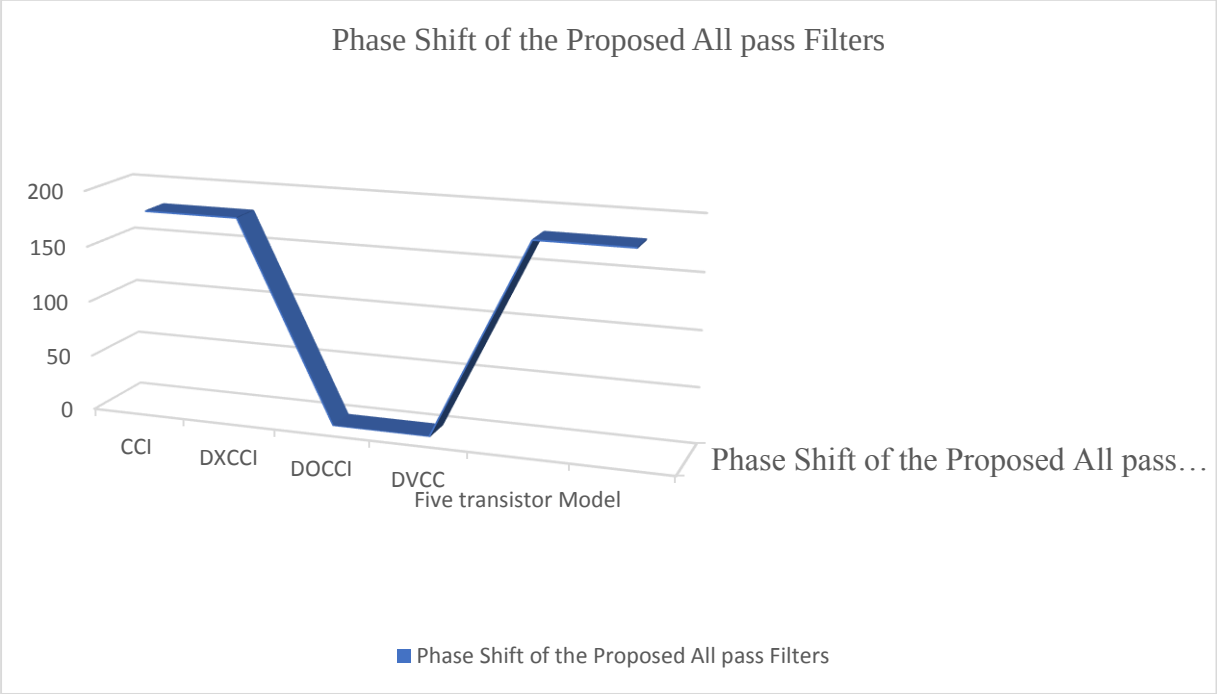
The above table shows the evaluation and performance of the proposed all pass filters as the unity gain and the phase shift of 180° is achieved over the 1Ghz bandwidth .To know its efficiency the noise parameters are calculated along with the load resistor added at the output and the its stability defines the withstand over the range of frequencies and to justify the noise parameters a set of 50range of frequencies are passed and its result is evaluated at the precise point. Its characteristics are represented in the pictorial graphs

- Input supply for Noise calculations
    1. 1v for Vdd
    2. 10Ghz band frequency
    3. 50mv peak-peak amplitude

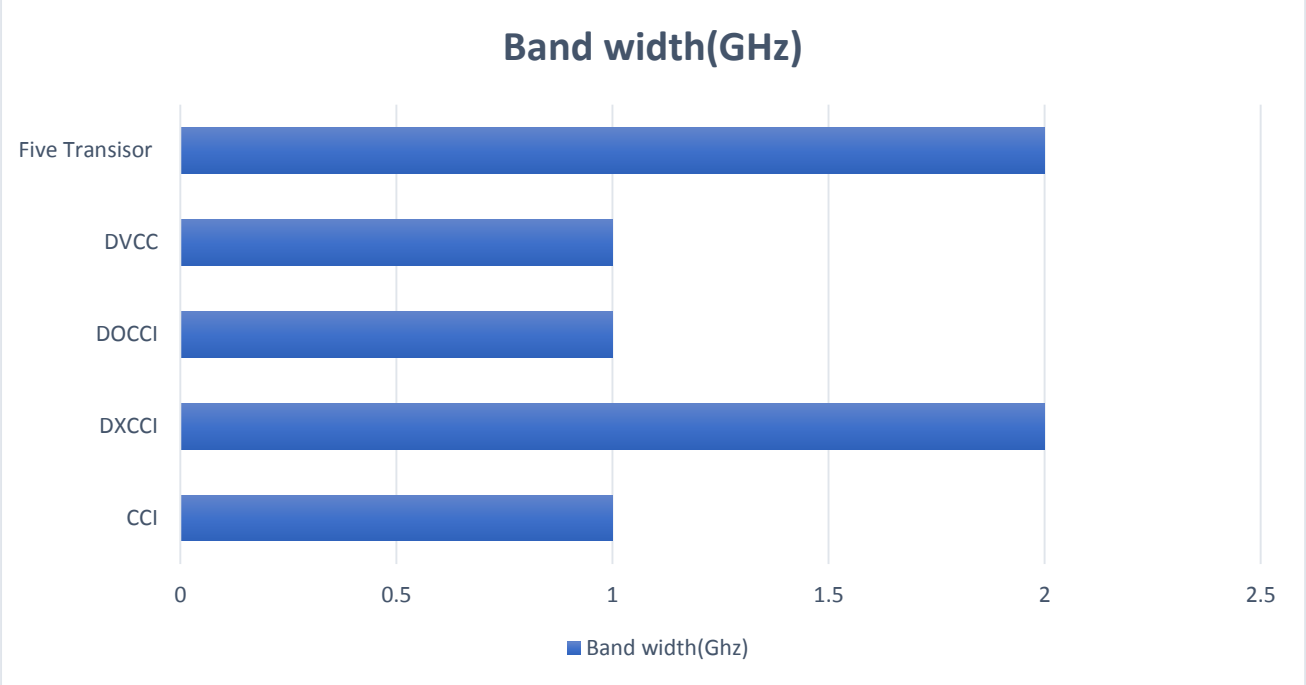
Gain of Proposed All pass filters:



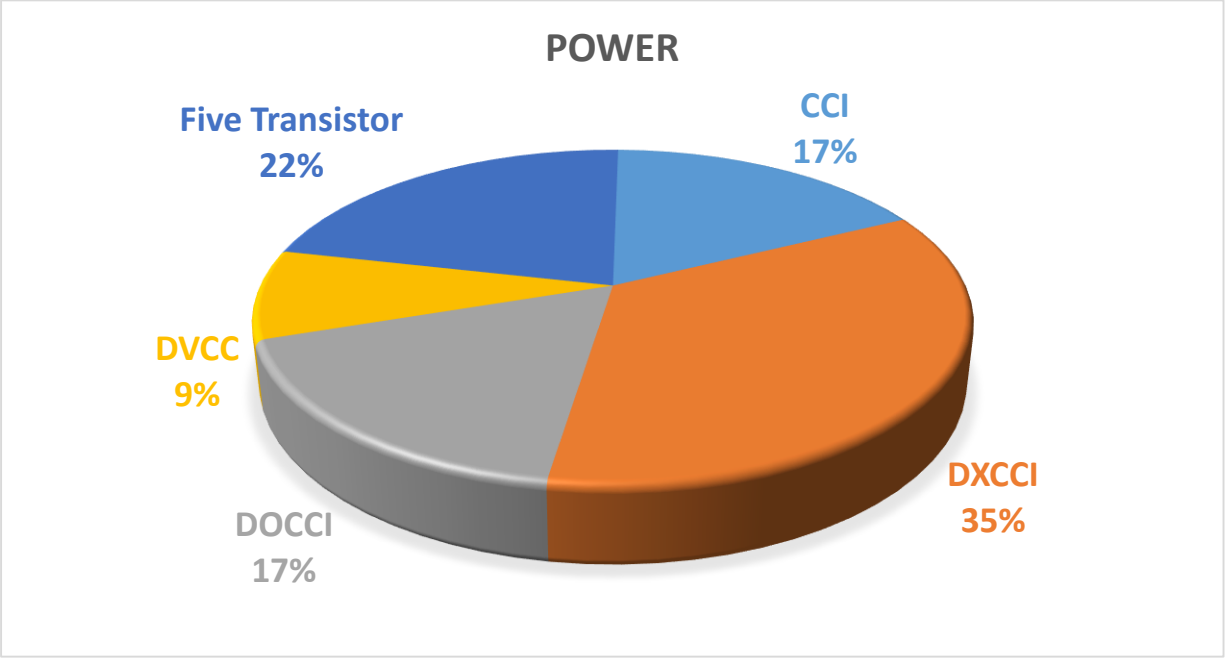
Phase shift Changes of the Proposed All Pass Filters:



Bandwidth of the Proposed All pass filter:



Power:



CHAPTER-8

CONCLUSION AND FUTURE SCOPE

The main aim of this work is to find an feasible solution for designing the all pass filters for transreciever and other electronic devices as it fuses an basic fundamental block for the signal transmission .instead of building different types of filters an all pass filter can be build up with high efficiency in all the parameters .As the par research is held with the Analog Signal processing the usage will the all pass filter merely increases and made incentives to conquer the new designs in regards of the all pass topologies. To make the efficient and accurate model its realizations is made in the Z-Domain and by the reference of the Z-domain realistic nature its equivalent nature behaviour is extracted in the form of the state space equations and with respect to the carrier signal properties the all pass circuit is implemented with desired outputs in all aspects. As the implementation involves in the CMOS process all the desirable characteristics in view of gain. Bandwidth, stability is realised and it eliminates some typical conditions in regard of fabrication and its usage will more for further generations.

As the technology advances in the field of communication for signal processing an efficient Radars and Antenna designs are mainly depend on the all pass filters.In the military applications mainly for the RF frequencies and for oscillators to generate signals, and ultra-high band transreciever the usage of all pass filters is more so there is demand of all pass designs in this field.

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