A

DISSERTATION-II REPORT

On

LINEAR TUNABLE TRANSCONDUCTOR

Submitted in the partial fulfilment of the requirement for the award of degree

Masters of Technology

In

VLSI

Submitted by

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Session: 2014-15 Parent Section: E2310

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SPECIALIZATION AREA: Analog VLSI Design **(pick from list of provided specialization areas by DAA)**

PROPOSED TOPICS

1. Design Transconductor with Linear Range & Tunning Capability using virtuoso
2. CMOS Domino Logic implementation for High performance Amplifiers.
3. Noise reduction in systems using VLSI Designs

Signature of Supervisor 15732

PAC Remarks:

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ABSTRACT

Operational Transconductance Amplifier (OTA) is a fundamental building block of analog circuits and systems. OTA has been used to implement many kinds of analog circuits such as; op amps, data converters, four-quadrant multipliers, mixers, modulators and continuous-time filters. Operational transconductance amplifiers (OTA) have been most significance block in analog circuits. The trend in modern wired as well as wireless communication system is to achieve higher data rates necessitating bandwidth and high linearity in analog front end circuits and analog filters. Moreover tunable transconductor are required for the compensation of environment parameter, specially temperature. Low voltage battery operated portable electronic gadgets are made to consume low power to give long life to its batteries. For this current mode circuits are preferred over voltage mode in analog signal processing. Transconductor amplifiers are recognized as fundamental building blocks of the analog frontend circuits, analog filters and oscillators [1-4]. In literature, several researchers have been reported linear Transconductor and its applications. OTA are widely used as active element in switched capacitor filter, data converter, and sample and hold circuits, or as buffer amplifier for driving large capacitive loads. OTA has fast setting response. In this report, the basic principle of linear transconductor has been addressed and some of the analog circuits based on transconductor are also investigated. Linear transconductor has essential for efficient realization. In Dissertation-II report multiple circuit techniques have been described to improve the linear characteristics of MOS transconductor.

ACKNOWLEDGEMENT

First of all, I would like to express my gratitude to **Mr. Sandeep Bansal** Assistant Professor, Electronics and Communication Engineering Department, **Lovely Professional University**, Phagwara for his gracious flawless efforts and forth right suggestions blended with an innate intelligent application have crowned my task with success. I am truly very fortunate to have the opportunity to work with him. I found this guidance to be extremely valuable.

I am also thankful to entire faculty and staff of Electronics and Communication Engineering Department and then friends who contributed directly or indirectly through there constructive criticism in evolution and preparation of this report work.

It is a pleasure to be associated with CADENCE Laboratory of **Lovely Professional University**, Phagwara and I would like to thanks the entire lab members.

I am thankful to **Mr. Sanjeev Kumar**, Research Scholar (LPU, Phagwara) who is always there at the need of hour and give me suggestion and inspiration in my tough time.

Last but not least I would like to thanks my all friends for their smile and friendship making the life at LPU University, Phagwara enjoyable and memorable. They rendered me enormous support during the whole tenure of my thesis work.

I extend my deepest gratitude to my Parents and Brother for their love, affection, encouragement and support.

CERTIFICATE

This is to certify that **ANKIT CHAUDHARY (11305703)** has completed objective formulation of his **Dissertation-II** entitled, **"Linear Tunable Transconductor"** under my guidance and supervision. To the best of my knowledge, the present work is the result of their original study and research. No part of the report has ever been submitted for any other degree at any University.

The project is fine for the submission and fulfillment of the conditions for the award of degree Masters of Technology.

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DECLARATION

I hereby declare that the **Dissertation-II** report entitled "**LINEAR TUNABLE TRANSCONDUCTOR** ", is an authentic record of my own work carried out as the requirements for the award of degree of **Master of Technology** in **VLSI Design** at **Lovely Professional University, Phagwara** under the guidance of **Mr. Sandeep Bansal**, Assistant Professor, Department of Electronics and Communication Engineering.

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It is certified that the above statement is correct to the best of my knowledge and belief.

Dated: **Mr. Sandeep Bansal**

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LIST OF SYMBOLS

Symbol	Name of Symbol
μ	Charge carrier mobility
C_{gs}	Gate Source capacitance
C_{gd}	Gate Drain capacitance
G_m	Transconductance
I_d	Drain current
K_p	PMOS transconductance parameter
K_n	NMOS transconductance parameter
V_{dd}	Positive supply
V_{ss}	Ground supply
V_{sat}	Saturation voltage
V_{th}	Threshold voltage
Vo	Output voltage
V_{tho}	Threshold voltage at $V_{sub}= 0$
ADSL	Asymmetrical Digital Subscriber Line
K	Boltzmann constant
L	Channel length
W	Channel width
C_{ox}	Normalized oxide capacitance
Z_{in}	Input Impedance
FVF	Flipped Voltage Follower

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Chapter 1 INTRODUCTION

1.1 INTRODUCTION

1.1.1 Introduction of Transconductor

The transconductor is a basic building block in analog circuit applications including continuous-time filters, data converters, variable gain amplifier and other interface circuits. Recently, they have also been used in continuous-time Bandpass sigma-delta modulators operating at IF frequencies and above. In many of these applications, the transconductor at the input determines the overall linearity performance of the system. As device sizes and power supply voltage are scaled down to achieve higher operating speeds and large scale integration, obtaining high linearity with reasonable signal levels becomes more challenging. The reason is that with modern CMOS technology, supply voltage decrease and many of the used linearization techniques where circuit grows vertically are often not feasible due to available reduced common mode range.

1.1.2 Symbol

Representation of transconductor based amplifier symbol is shown in Figure 1.1.

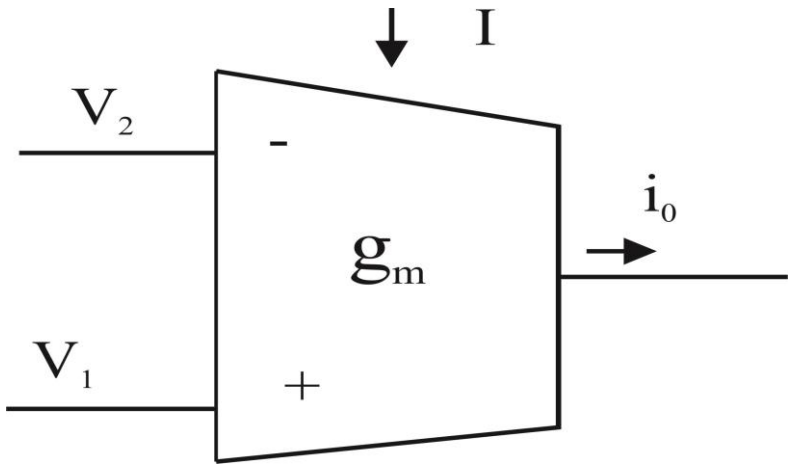

Figure 1.1 Symbol of Transconductor

Voltage V_1 and V_2 act as input and I_0 work as output. The gain of the block is represented by g_m [16].

1.1.3 Equivalent Model of Transconductor Based Amplifier

The equivalent model of transconductor based on high frequency model of MOS shown in Figure 1.2. In this model we are using some approximation related to high frequency parameter value [16]. Model of Transconductor is shown below in Figure 1.2.

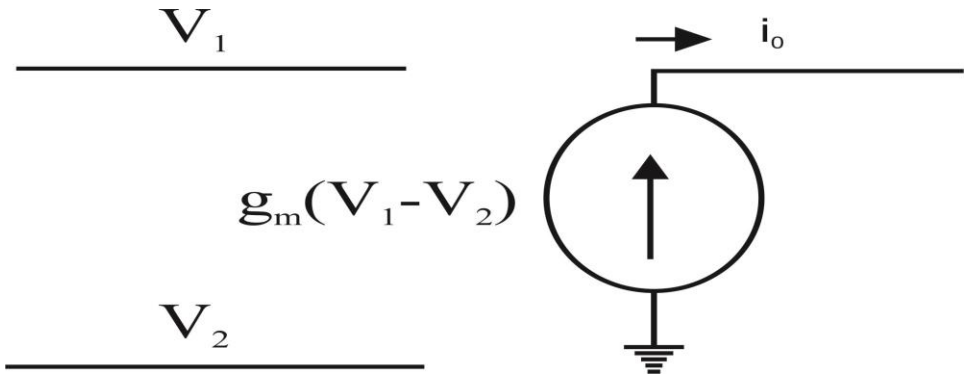

Figure 1.2 Equivalent Model of Transconductor Based Amplifier

There is a requirement of high transconductance and good controllability in high frequency continuous time filter and the used OTA filter should provide high transconductance and good controllability [6]. While RC filter provide constant cutoff frequency irrespective of input signal variation. The OTA is prerequisite good linearity in the entire range of input signal. Good linearity related to that OTA must have constant G_m, graph in his input limit [3]. The linearity during the voltage-to-current conversion should usually preserved because the linear range of transconductor govern the linearity of whole system.

Now a day the challenge is that the power supply and size of the device is scale down to achieve more speed because of this linearity create problem to achieve sufficient signal level [1]. Most of transconductor application system requires low noise and current consumption along with good linearity over a significant range. In transconductor due to differential structure even harmonics does not exit but odd harmonics play a vital role in the distortion of the output current [2].

1.1.4 Types of Linearization Techniques

- Source Degeneration (Either Resistor or MOS) [11]
- Cross Coupled Differential Pair [2]
- Adaptive Biasing [11, 31]

- Mobility Compensation Techniques[3]
- Shift Level Biasing [4]
- Input Signal Attenuation
- Transconductor Employing Body Effect [14]
- Transconductor Utilizing Squaring Circuit [35]
- Backgate Bias Techniques [24]
- Bias offset technique[4]

Source degeneration [1] give good linearity but there is a trade-off between supply voltage and common mode rejection ratio. The two source degenerated differential pair could be used to terminate harmonic distortion. The Pseudo- differential arrangements could accomplish good linearity because absence of tail current source [12, 13]. But these structures have poor common mode rejection ratio so we have to employ extra circuitry to achieve desired performance.

The main characteristic of a practical OTA are [16]:

- Limited linear input range
- Finite bandwidth
- Finite signal to noise ratio
- Finite output impedance

Analog filter designed using two methodologies [8, 30, 32]

- Discrete Time filter design
    - Switch Capacitor based filter design
    - Switch Current based filter design
- Continuous Time implementation

Continuous-time filters are required in many mixed signal systems, e. g. they are used for antialiasing purposes, before signals are sampled in order to be A/D converted or they are also used for smoothing purposes at the output of DACs. For the realization of filters in the hundred MHz frequency range the G_m-C-topology is the only technique to obtain filters with a high quality factor. However, due to the open-loop operation, G_m-C filters perform poorly as far as linearity is concerned. We have to linearize an operational transconductance amplifier (OTA)

in the way such that the current is defined only by one linear resistor. In order to maintain a high common-mode rejection ratio (CMRR) as well as a high power supply rejection ratio (PSRR), the topology is a fully differential structure. Due to sampling process we cannot use Switched Capacitor, Switched Current at higher frequency. Continuous time filter have a high speed as compare to discrete filter because absence of sampling process in Continuous filter.

There are three main procedures to implement filter [11].

- Active Resistive Capacitor Filter
- MOSFET-Capacitor Filter
- Transconductance (Gm)– Capacitor Filter

Active RC filter [6] use passive frequency element like as op-amp, resistor, capacitor, they provide worthy linearity but prerequisite large die area, tuning could accomplished by placing arrays of passive component.

MOSFET-C [5, 8] active filter has poor linearity because of non-linear behavior of CMOS transistor. Linearity could be increased by placing manifold Cross Combined transistor [7], and input active range is compact in demand to preserve the MOSFET in linear region. G_m-Capacitor configuration [8], [9] has stable frequency reaction in respect to active Resistor Capacitor, MOSFET- Capacitor, because of nonappearance of feedback to the active elements [37].G_m-Capacitor has poor linearity. But noise and linearity are in a tradeoff situation in this filter. There are different types of G_m-C filters are implemented now a days, such as first order, second order etc. With an improved version of Gm-c, its performance also increases [9].

1.2 BASIC PRINCIPLE

Although there are many techniques to implement a linear transconductor, a square-law function circuit, and a four-quadrant multiplier [9], [10], perhaps the simplest and most efficient way to do this, using the same basic circuit element, is to base the design on the principle of cross-coupling a matched MOS transistor pair with two identical dc floating-voltage sources as shown in Figure 1.3. The circuit exploits the ideal square-law behavior of the MOS transistor in the saturation region, given by the well-known expression

$$I_D = k_n \left(V_{GS} - V_T \right)^2 \tag{1.1}$$

The simplest way to implement the floating-voltage sources in Figure 1.3 is to use source followers. However, in order to obtain reasonable voltage sources with low output impedance, the source followers must have a large aspect ratio. Furthermore, since the source follower operates in class-A, the maximum current efficiency is limited to 25%. Different ways have been suggested for improvement. Both current feedback and voltage feedback have been used to reduce the output impedance of the voltage sources. However, such techniques greatly increase the circuit complexity and also reduce the operating speed.

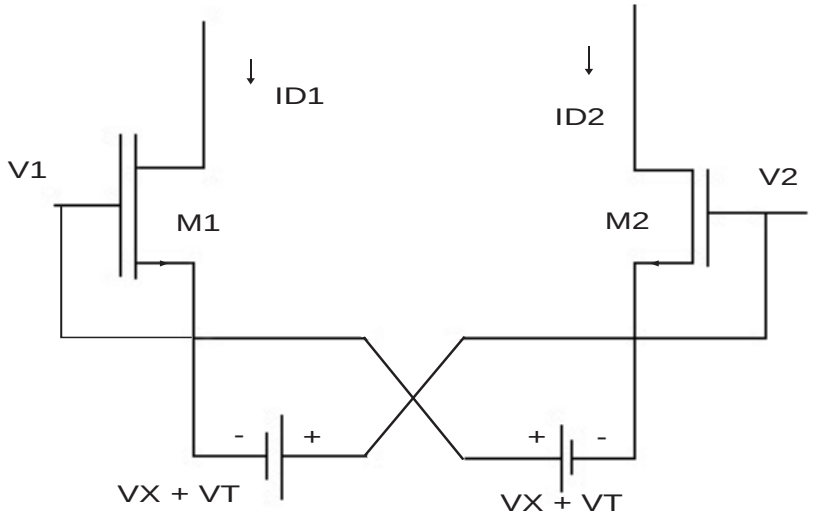

Figure 1.3 Straightforward Structure of Transconductor Circuit

In Figure 1.3 MOSFETs M_1 and M_2 both are biased to operate in saturation region. The drain currents I_{D1} and I_{D2} are expressed.

$$I_{D1} = k_n \left(V_{GS1} - V_T\right)^2 \tag{1.2}$$

$$I_{D2} = k_n \left(V_{GS2} - V_T\right)^2 \tag{1.3}$$

Where V_{GS} voltage difference between source to gate, V_T is the threshold voltage of CMOS gate. $k = 1/2\ \mu CoxW / L$ is transconductance factor, Where W means channel width, L is the channel length, μ is the charge carrier mobility, Cox is oxide capacitance. The threshold voltage V_T in equation (1.2), which leads non-linear terms to the squaring function, is abolished in Figure 1.3 by the annexation of the two dc floating-voltage sources of value $V_X + V_T$.

The circuit standard in Figure1.3 may be opportunely used to achieve a linear transconductor by subtracting the drain currents I_{D1}, I_{D2}. Using equations (1.2) and (1.3), the gate to source voltage of transistors M_1 and M_2 can be stated as:

$$V_{GS1} = V_{id} + V_T + VX \tag{1.4}$$

$$V_{GS2} = -V_{id} + V_T + VX \tag{1.5}$$

Where,

$$V_{id} = V_1 - V_2 \tag{1.6}$$

The uninvited V_T term which hosts non-linear terms to the squaring function. Source follower operates must have W/L large aspect ratio to completes low output impedance. The differential output current is then given by combining equations (1.4) and (1.5).

$$I_{D1} - I_{D2} = k\left[\left(V_{id} + V_x\right)^2 - \left(V_x - V_{id}\right)^2\right] \tag{1.7}$$

The threshold voltage V_T, is negated out and it is compact to

$$V_T\left(V_{SB}\right) = V_{TO} + \gamma\left(\sqrt{\left|2\varphi F\right| + V_{SB}} - \sqrt{\left|2\varphi F\right|}\right) \tag{1.8}$$

Which pronounces an impeccably transconductor. Given M_1, M_2 works in the saturation region, linear limit prolongs to these values of V_{id} where drain currents I_{D1} or I_{D2} converts to zero. From equations (1.1), (1.2), (1.3) and (1.4), it monitors that linear limit of transconductor is bounded by

$$V_X \leq V_{id} \leq V_X \tag{1.9}$$

The transconductance is then given by $4kV_X$ and may be varied electronically by varying bias voltage V_X [20].

Chapter 2 TERMINOLOGY

2.1 TERMINOLOGY

2.1.1 Transconductance

Transconductance is characteristic of electronic components. Conductance is the inverse of resistance, transconductance is the ratio of the current variation at to the voltage variation at the input. It is written as G_m. For direct current, transconductance is defined as follows [25].

$$G_m = \frac{\Delta I_0}{\Delta V_{id}} \tag{2.1}$$

2.1.2 Vacuum Tubes

Transconductance is defined as the change in the plate (anode)/cathode current divided by the corresponding change in the grid/cathode voltage, with a constant plate (anode)/cathode voltage. Typical values of G_m for a small-signal vacuum tube are 1 to 10mS. It is one of the three 'constants' of a vacuum tube, the other two being its gain μ and plate resistance R_p. The Van der Bijl equation defines their relation as follows [25].

$$G_m = \frac{\mu}{R_p} \tag{2.2}$$

2.1.3 Nonlinearity

Nonlinearity of a circuit means variation of the slope at input side and at output side. If incremental change at the input results in different incremental change at the output depending on the input dc level [15].

$$y(t) = a_1 x(t) + a_2 A^2 x(t)^2 + a_3 A^3 x(t)^3 + \ldots \tag{2.3}$$

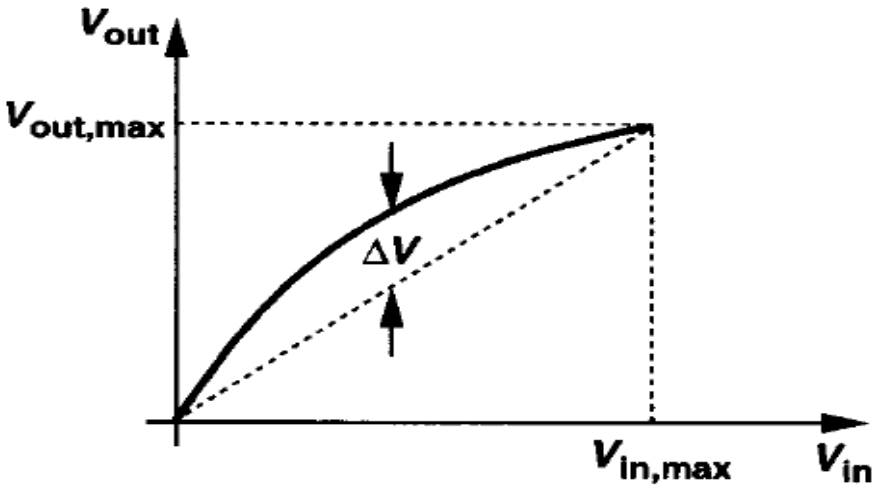

Figure 2.1 Definition of Nonlinearity

2.1.4 Harmonic Distortion

Harmonic distortion is a parameter of measuring nonlinearity in circuit. Harmonic distortion is undesirable in signal processing application [15].

$$y(t) = a_1 A\cos wt + a_2 A^2 \cos^2 wt + a_3 A^3 \cos^3 wt \tag{2.4}$$

Higher order terms yields higher harmonics.

2.1.5 Effects of negative feedback on nonlinearity

Negative feedback system improve the linearity of the circuits [15]. Circuit with feedback is shown Figure 2.2.

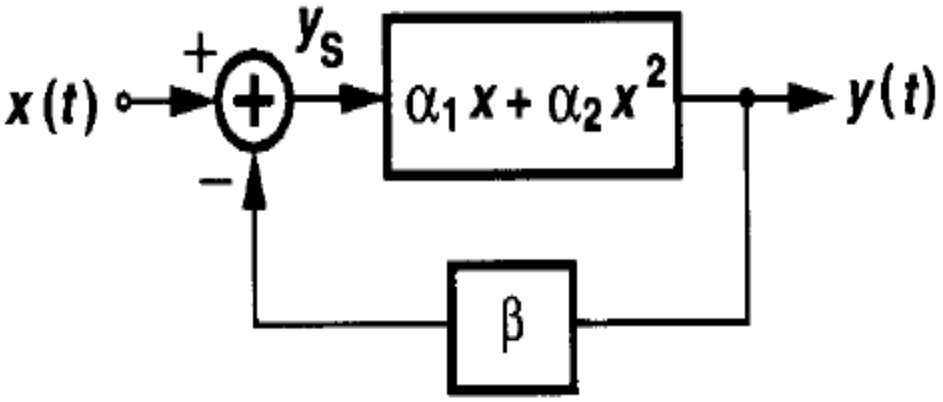

Figure 2.2 Circuit with Negative feedback

2.1.6 Capacitor Nonlinearity

Capacitor take some finite time constant to charge or discharge. Therefore capacitor introduce some nonlinearity into the circuit.

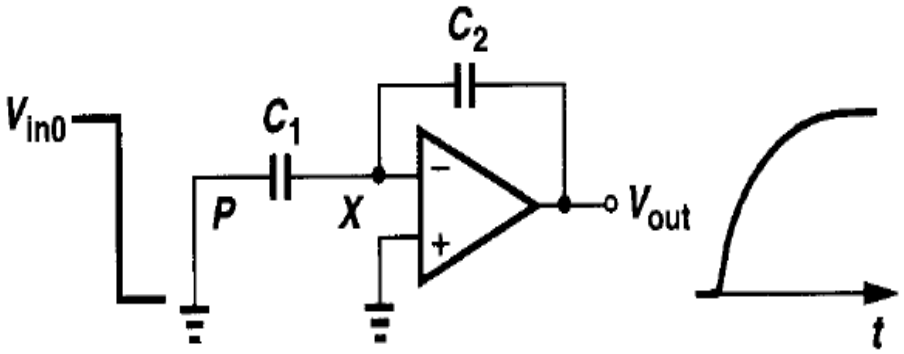

Figure 2.3 Capacitor Nonlinear Behavior

2.1.7 Second Order Effect

There are several second-order effects causing deviations from the ideal square-law behavior of MOSFET. The effect of mobility reduction and channel length modulation of the circuits will be considered. It will be shown that these effects cause the harmonic distortion of the current flowing through the circuit. Body effect is negligible because substrate of the transistor has been connected to the respective source. Second order effect play more accurate numerical result for the circuit performance, while current mirror and voltage follower are supposed to be ideal for simplicity sake. Second order effects will be studied for the linearization circuit. Voltage shifter V_T and the squaring circuit serve to provide an appropriate current for biasing linearization circuit, second order effects on these two circuits alter only the resistance value and cause no harmonic distortion of the resistor current [15].

2.1.8 Channel Length Modulation

Channel length modulation causes the drain current to be dependent on the drain voltage. This will cause mainly second and third order distortion components. The distortion due to channel length modulation can be reduced by increasing the channel length of the devices. For a MOSFET operating in the saturation region, the effective channel length is reduced as the inversion layer near the drain vanishes, while the channel-end voltage remains essentially constant and equal to V_{DS}.

2.1.9 Substrate Bias effect

In many digital circuit applications, on the other hand, the source potential of an nMOS transistor can be larger than the substrate potential, which results in a positive source-to-substrate voltage V_{SB} >0. In this case, the influence of the nonzero VSB upon the current characteristics must be accounted for. The voltage applied to the back contact affects the threshold voltage of a MOSFET. The voltage difference between the source and the bulk, VBS changes the width of the depletion layer and therefore also the voltage across the oxide due to the change of the charge in the depletion region. This results in a modified expression for the threshold voltage, as given by [15].

$$V_T(V_{SB}) = V_{TO} + \gamma(\sqrt{|2\varphi F| + V_{SB}} - \sqrt{|2\varphi F|}) \tag{2.5}$$

2.1.10 Noise

In general two types of noise are considered in case of CMOS circuit. Thermal noise, which is caused by the random motion of charge carriers at a temperature above absolute zero, does not depend on frequency of operation whereas flicker noise is associated with the carrier trap in semiconductors and decreases with increase in frequency.

Chapter 3 LITERATURE REVIEW

3.1 LINEARITY TECHNIQUES

3.1.1 Simple MOS Transfer

The simplest CMOS transconductor is a single CMOS differential tail-current pair, as shown in Figure 3.1. The differential input voltage is applied to the gate of the two input transistors and steers the tail current through the drain of the two transistors. Assuming saturation of strong inversion operation, the function transfer of this simple transconductor is given by: [11].

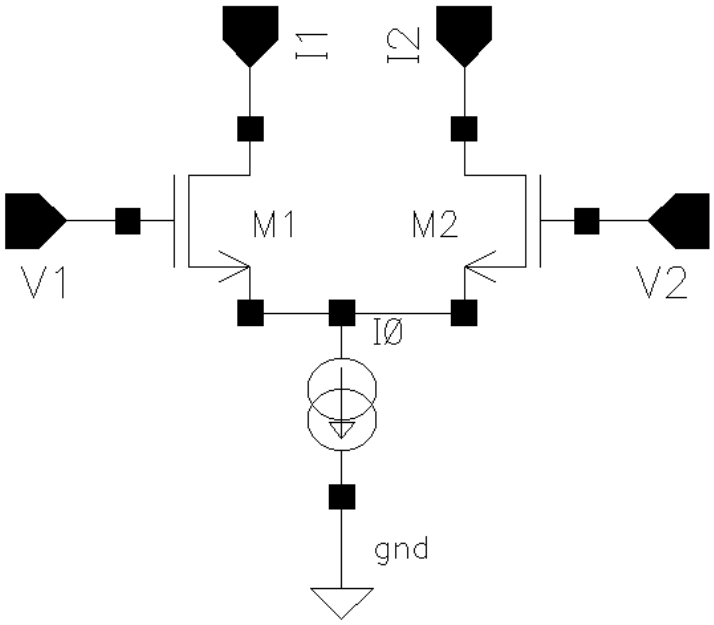

Figure 3.1 Basic Transconductor

The transfer function of this basic transconductor is specified as

$$I_{out} = I_1 - I_2 = G_{mo} V_{id} \sqrt{1 - \frac{\beta_{1,2}^2 V_{id}^2}{G_m^2}} \tag{3.1}$$

Where,

$$V_{id} = V_1 - V_2 \tag{3.2}$$

$$\beta_{1,2} = 1/2 \mu_0 C_{ox} \left(W / L \right) \tag{3.3}$$

$$G_{mo} = \sqrt{2I_{ss}\beta_{1,2}} \tag{3.4}$$

$\beta_{1,2}$ and G_{mo} are respectively transconductance ratio and transconductance of transistor $M_{1,2}$.

As V_{id} cross the certain value the entire polarization current pass through the one transistor and turned off the other transistor. The maximum value of the V_{id} is specified as

$$V_{id,\max} = \sqrt{2}\frac{Io}{Gmo} \tag{3.5}$$

From the above equation, it may be concluded that for a given biasing current I_o, the linear range can be extended by reducing the transconductance of the transistor M_1 and M_2.

A well-known technique to increase the linear range of the transconductor by transconductance reduction uses source degeneration resistors. The degeneration resistor increases the voltages at the source of the differential pair transistors, therefore reducing drain current. This is in the detriment of supply voltage and operating common mode range. Furthermore significant increase in linear range needs large resistor values, a commodity unavailable in many of today's CMOS technology [11]. Another method consists of replacing the degeneration resistor with two MOS transistors in the triode region, however the variation of the Transconductance remains significant because change of the polarization of the degeneration transistors (triode and saturation), according to the amplitude of differential input voltage.

3.1.2 Mobility Reduction Free Low Distortion OTA Using Backgate Bias Technique

In this paper author describe a low distortion CMOS OTA based upon Backgate Bias Techniques specially for circuits which have non saturation MOSFET as a voltage controlled current source. This structure is free from mobility reduction problem when it is realized using single well process. In this input signal is applied to either of drain terminal or gate terminals. When input signal is applied at gate terminal mobility reduction is occurred [24].

3.1.3 Multiple Input Floating Gate (MIFG) CMOS Technique

MIFG MOS is used in corresponding to the source coupled pair. The region of operation of MIFG MOS should be strong saturation operation [1]. The circuit is given below in Figure 3.2.

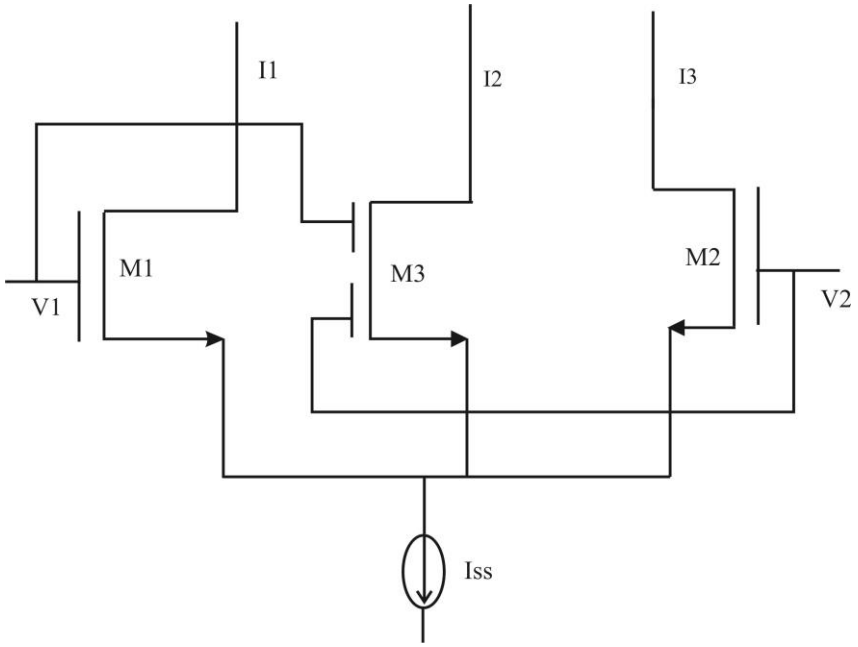

Figure 3.2 Multiple Input Floating Gate Based MOS Transconductor

Transfer function of this circuit is specified below

$$I_{out} = \left(\frac{2\beta_{1,2}}{1+\frac{\beta_3}{\beta 1,2}} \right) \left(\sqrt{1-\frac{\beta_{1,2} V_{id}^2}{G_{mo}^2}} \right) V_{id} \tag{3.6}$$

$$I_{out} = \frac{G_{mo}}{A} V_{id} \left(\sqrt{1-\frac{\beta_{1,2}^2 V_{id}^2}{G_{mo}^2}} \right) \tag{3.7}$$

Where, A is specified as geometrical size of M_2 and $M_{1,2}$.

$$A = \sqrt{1+\frac{\beta_3}{2\beta 1,2}} \tag{3.8}$$

The MIFG MOS circuit simulated in a double poly .8µm CMOS technology. Voltage supply is 3V and the bias current 10A, and size of transistor $M_{1,2}$ to (W/L)2,1 = (10µm/4µm). The maximum linearity was achieved for (W/L) = (88µm/4µm). We see that the linearity directly depend upon the value of A. Higher the value of A higher will be linearity. So for good linearity value of A should be as large as possible [1].

3.1.4 Attenuated Resistor Degenerated Differential Pair (ARDP) Technique

This linearization method employ an attenuator monitored by source degenerated operational transconductance amplifier. Degeneration may be two type either it can use a MOS or resistor in triode range of operation [2]. The circuit of OTA (ARDP) is given below in Figure 3.3.

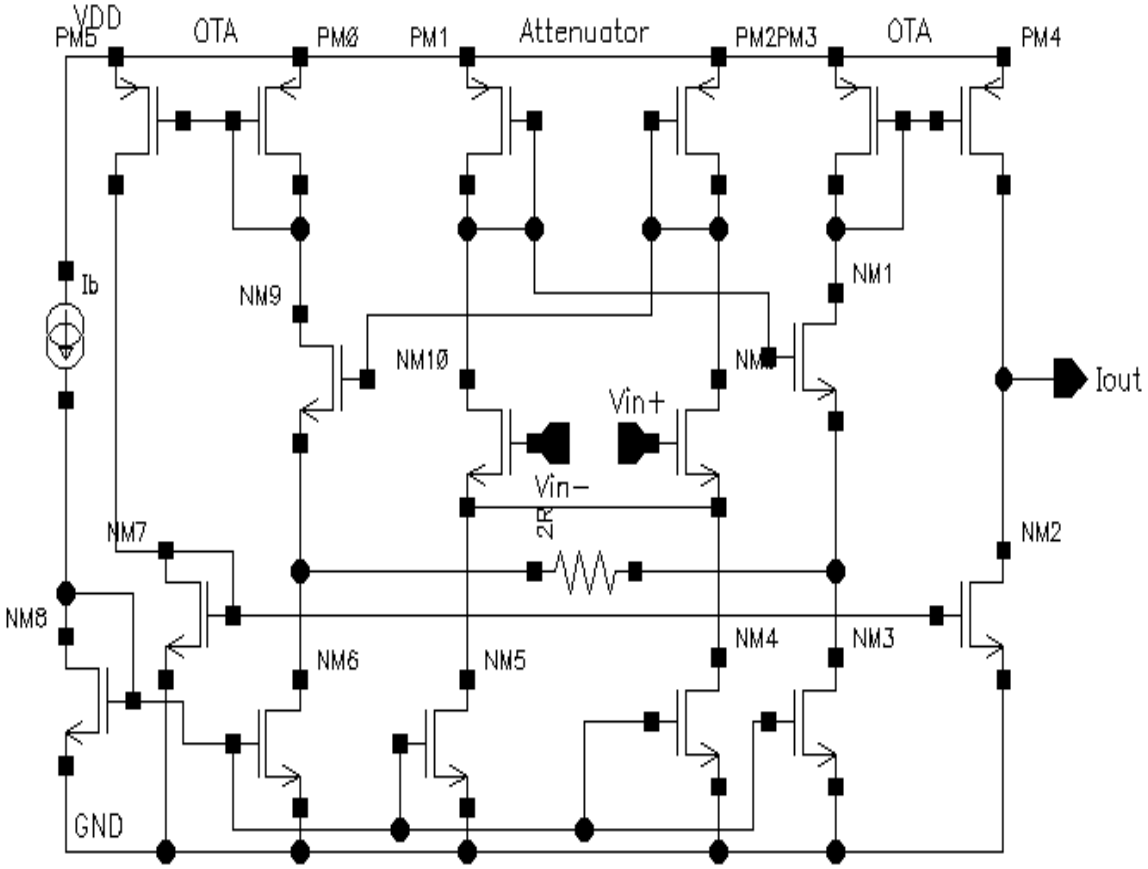

Figure 3.3 Attenuated Resistor Degenerated Differential Pair Approach Based Transconductor

The attenuator fundamentally the differential attenuator with diode coupled PMOS load Transistors. In this circuit attenuator output work as an input for source degenerated OTA [2].

$$I_1 = \frac{I_b}{2} + \frac{1}{2}\sqrt{2\beta_n I_b} * \mathrm{V}_{id} - \frac{1}{8}\sqrt{2\beta_n I_b}(\beta_n / I_b) * \mathrm{V}_{id}^3 \tag{3.9}$$

$$I_2 = \frac{I_b}{2} - \frac{1}{2}\sqrt{2\beta_n I_b} * \mathrm{V}_{id} + \frac{1}{8}\sqrt{2\beta_n I_b}(\beta_n / I_b) * \mathrm{V}_{id}^3 \tag{3.10}$$

$$\Delta V_g = V_{g3} - V_{g4} = \sqrt{\frac{I_1}{\beta_p}} - \sqrt{\frac{I_2}{\beta_p}} \tag{3.11}$$

$$V_g = \frac{V_{id}}{\sqrt{m}} \tag{3.12}$$

$$m = \frac{\beta_p}{\beta_n} = \left(\frac{\mu_p}{\mu_n}\right)\left\{\frac{(W/L)_{p3,4}}{(\mathrm{W}/L)_{n1,2}}\right\} \tag{3.13}$$

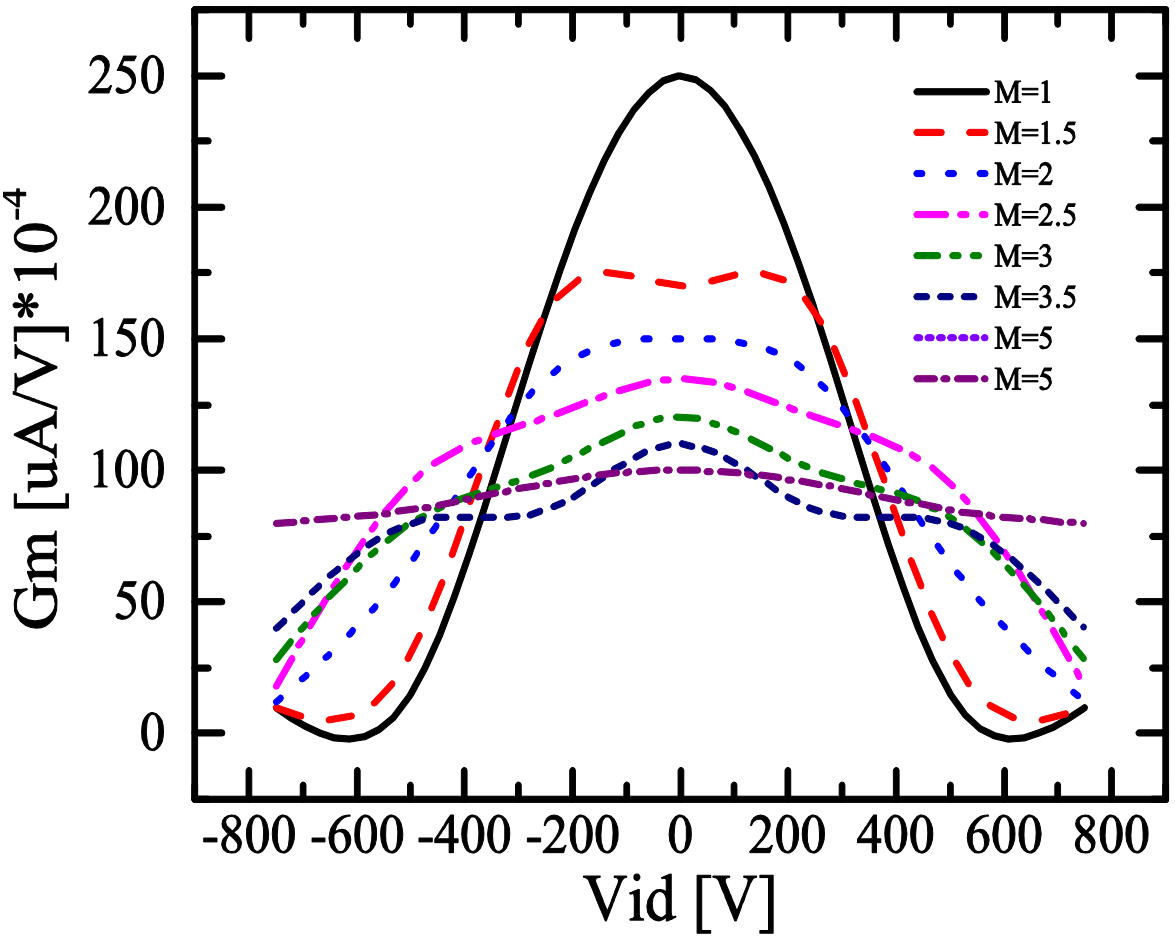

Figure 3.4 Transconductance Characteristics

m is the ratio of transconductance parameter of load transistors to that of input transistors and termed as attenuation factor Some non-linearity is still exit because of mobility degradation, idealities problem of transistor, second order effects.

At this instant this differential voltage is given at input of resistor degenerated OTA. The output current of this OTA is given below

$$I_0 = \frac{\sqrt{2\beta_n I_b}}{\sqrt{m}(1+N)} * V_{id} - \frac{1}{4m^{\frac{3}{2}}(1+N)^{\frac{5}{2}}} \sqrt{2\beta_n I_b}(\beta_n / I_b) * V_{id}^3 \tag{3.14}$$

$$G_m^{'} = \frac{\sqrt{2\beta_n I_b}}{\sqrt{m}(1+N)} \tag{3.15}$$

$$HD_3^{'} = \frac{1}{32} \frac{V_{id}^2}{m(1+N)^2 (V_{GS} - V_{th})^2} \tag{3.16}$$

It is clear that if the value of m will increase than the harmonic distortion will be decrease as well as increase the value of linear range. But there is limitation on the value of m, we can not increase the value of m after certain limit. Higher value of m decrease the voltage swing at the output and force the load transistor enter into subthreshold region [2].

This circuit was implemented under .18µm CMOS technology under 1.8V power supply. It shows the common mode rejection ratio (CMRR), power supply rejection ratio (PSRR) -60 dB and -58 dB respectively. Input noise spectral noise density 70nV for 10 MHz frequency. In this -70dB HD3 is attained for 600mV with a linear range of 1.2V peak to peak for 1% transconductance [2].

3.1.5 A Novel CMOS OTA Based on Mobility Compensation Procedure

To remove the mobility effect Coban and Allen provide a configuration in which they practice of parallel grouping of linear and saturation devices [3]. Even though the circuit indications a worthy linearity, circuit input range was not adequate for application such as video application circuit. Then a new approach makes use of triode and subthreshold region transistor. Mobility compensation techniques based circuit is given below in Figure 3.5.

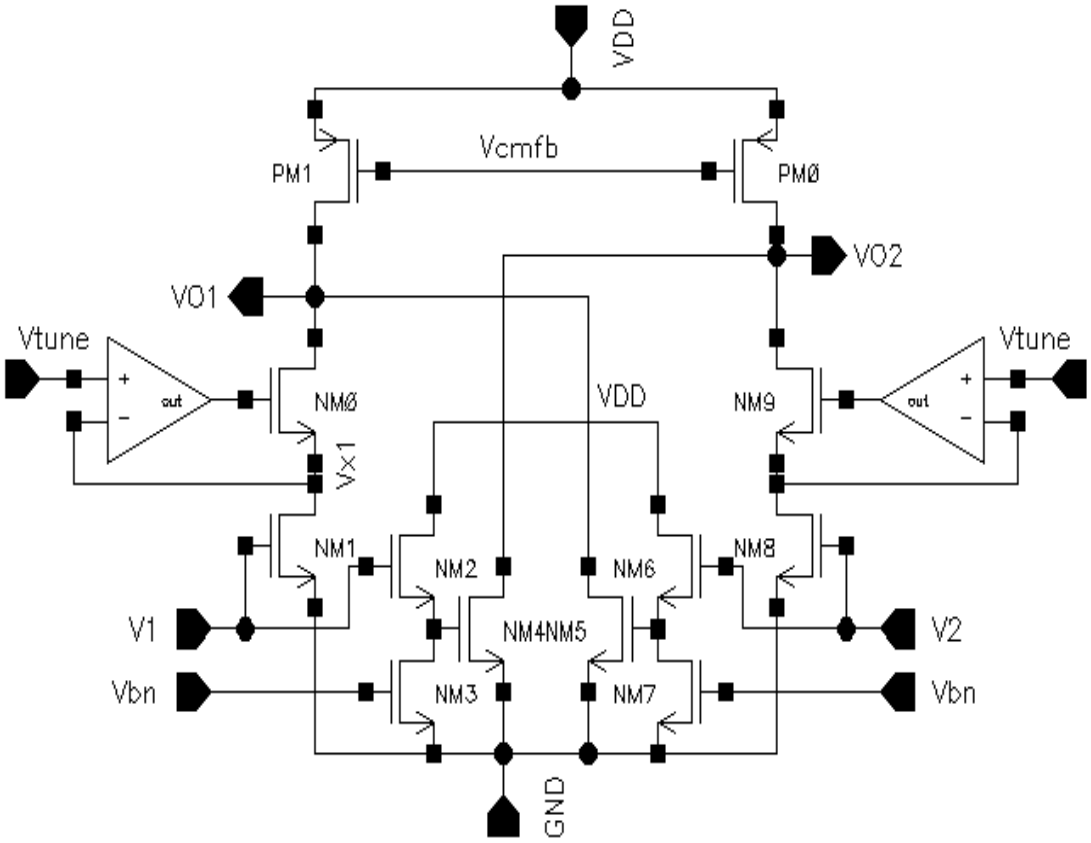

Figure 3.5 Mobility compensation based OTA

Transistor M_{N3} and M_{N4} operate in subthreshold region. Source follower consisting the transistor M_{N7} - M_{N10} command M_{N3} - M_{N4} to drive in subthreshold region. Third order harmonics terms of linear and subthreshold region has reverse signs. Parallel arrangement of linear and subthreshold region transconductor could cancel harmonics term with an appropriate aspect ratio and can rise the linearity. The output current is specified as

$$I_{out} = I_1 - I_2 = (I_{mn1} - I_{mn2}) + (I_{mn3} - I_{mn4}) \tag{3.17}$$

The drain current in M_{N3} and M_{N4} given as

$$\mathrm{I}_{mn3} = \beta_3 V_t^2 (\eta - 1)\, \mathrm{e}^{(V_{GS3} - V_{THN})/\eta v_t} \left(1 - e^{-V_{DS3}/\mathrm{V}_t}\right) \tag{3.18}$$

$$\mathrm{I}_{mn4} = \beta_4 V_t^2 (\eta - 1)\, \mathrm{e}^{(V_{GS4} - V_{THN})/\eta v_t} \left(1 - e^{-V_{DS4}/\mathrm{V}_t}\right) \tag{3.19}$$

The triode region G_m is deviated to the positive sign whereas the subthreshold G_m have negative sign, with parallel arrangement of these two Gm we acquire the over-all G_m having

an improved linearity and a broader input limit for a given error limit. Subsequently the input operating limit of OTA is exaggerated by V_B and A_{vsf} these twofold design parameter should be wisely selected to promise $M_{N3,}$ M_{N4} to operate in the subthreshold region.

If V_B has too large the gate source voltage of M_{N3}, M_{N4} are excessively large, transistor dimension to conserve the compensation capability should be enlarged to a disagreeable value. For large A_v as the input increase, there exit the region that M_{N3} M_{N4} modify his operation subthreshold region to saturation region and OTA has lost his compensation capability.

Here the source follower circuits play an important role to determine the optimum value of A_{vsf} and V_B. The circuit suffers Gm fluctuation due to process parameter mismatch.

This circuit has ± 0.5% G_m deviation in the wide input range of ± 0.8V. The THD is under -60dB. A ninth order Bessel filter for a DVD read channel equalizer using this OTA was simulated with 0.35-µm n-well CMOS process. This circuit indicate the cutoff frequency of 8-MHz and group delay ripple is less then ±2.1% over the range from .5fc to 2fc. Filter use about 65mW power under at 3.3V supply [3].

3.1.6 Transconductor Using Body Effect for Low Frequency Application

In this techniques problem of narrow input range of the transconductor in medical devices, which has low frequency can be eliminated by an improved local-feedback MOS transconductor operating in subthreshold region utilizing body effect. Newton Raphson and Downhill Simplex method is used in the designing of this transconductor [14,29].

The biological signal frequency is several hundred hertz and the magnitude is 1µV to 100mV [9]. For the low frequency application the time constant values should be higher. For a 100Hz frequency transconductor should be less than 1µS.

Nonlinearity can be compensated by change the threshold voltage with the help of body voltage. Threshold voltage is given as

$$V_{th} = V_{tho} + V_{OFF} + \gamma\left(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F}\right) \tag{3.20}$$

$$\Delta V_{th} = \gamma\left(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F}\right) \tag{3.21}$$

V_{th} ,V_{OFF} , γ, V_{SB} , ΔV_{th} are the threshold voltage of a transistor operating in strong inversion region, when V_{SB}=0 , the offset threshold voltage of a transistor operating in subthreshold region, body effect coefficient, the fermi-potential the source bulk voltage, and the variation of the threshold by body effect respectively. If the value of V_{SB} is decrease then the value of drain current will be increase. The diagram is given below in Figure 3.6.

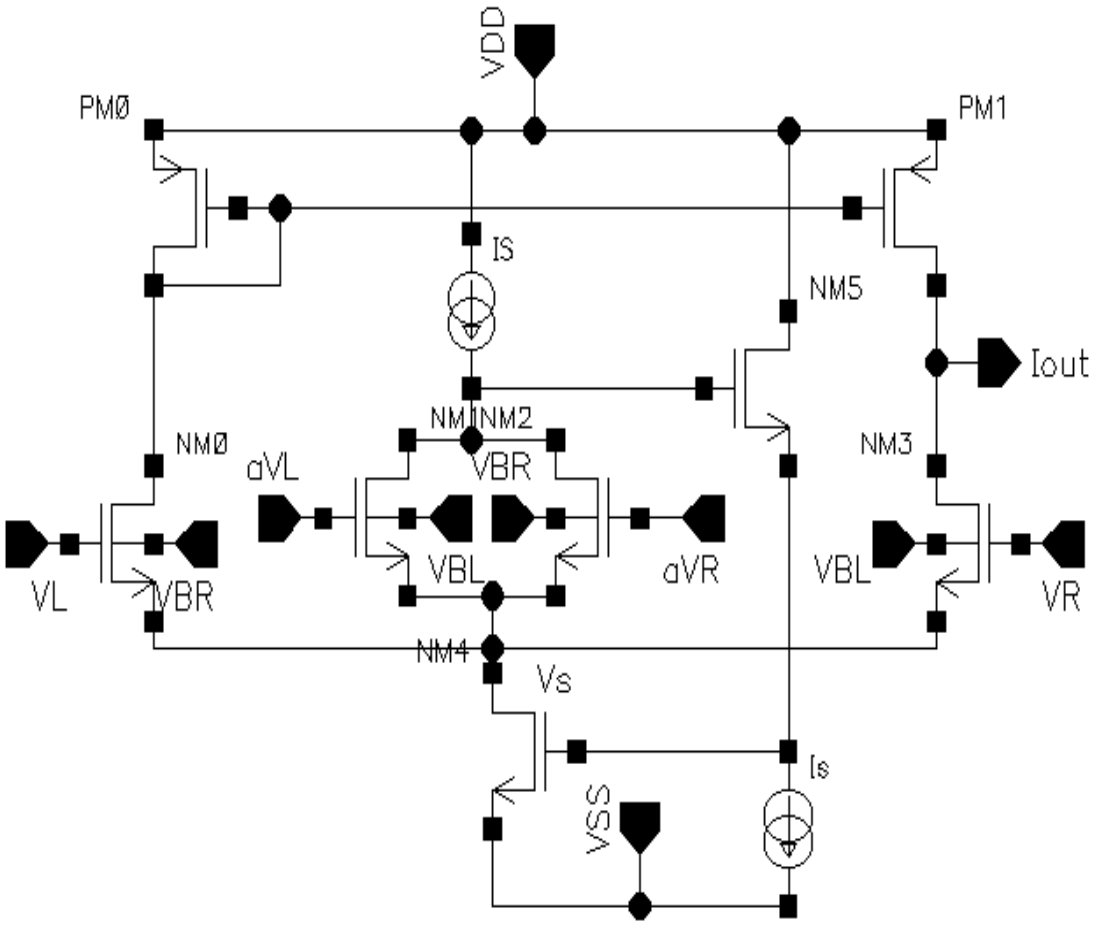

Figure 3.6 Low Transconductance Circuit Using Body Effect

To reduce the nonlinearity of the improved LFB OTA the common source voltage VBL and VBR of the active voltage divider are used for the bulk voltage of the proposed transconductor [14].

In the simulation of this circuit design .18µm BSIMS model is used. The supply voltage is ±.9V. The THD around -40dB for input voltage magnitude 170mV and the frequency of input voltage 100Hz. Power consumption at Gm = 1µS is 682nW [14].

3.1.7 Squaring Circuit Based Linear Transconductor

This technique based circuit is able to tune by adjusting the bias voltage. This circuit shows the significant application for highly linear continuous time filter [35].

Voltage tunable transconductor linearization method based on a bias offset technique which provide a high linearity and consume low power. The circuit diagram is given below in Figure 3.7.

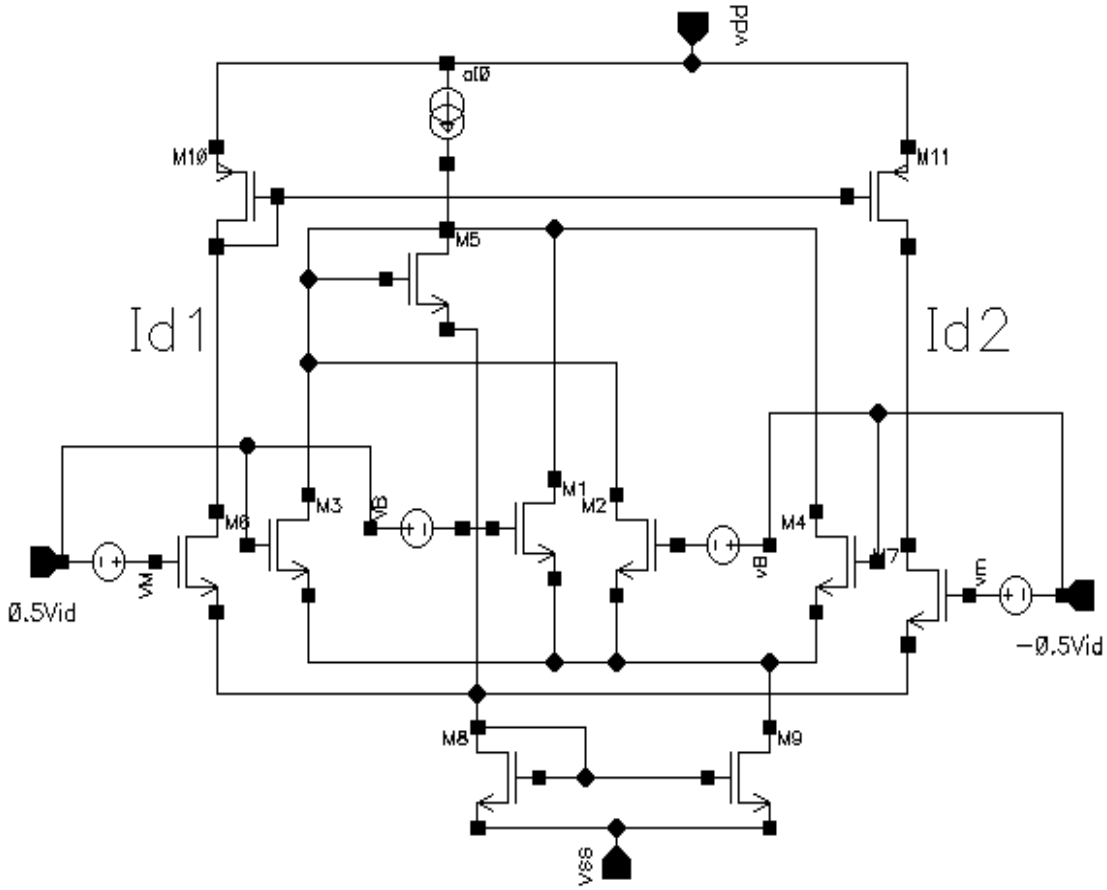

Figure 3.7 Linear Transconductor Using Bias Offset Scheme

Transistor $M_6 – M_7$ form the differential pair, while transistor M_1- M_4 constitute the bias offset transconductor. This squaring circuit provide the input independent bias current to differential pair in such a different way that M_5 and a current sink I_0 are used to level shift the summed the drain current of I_L and I_R from vertex A to vertex B. The drain current of the transistor M_6 and M_7 are i_{d1} and i_{d2} is expressed as.

$$I_{D1} = K_n\left(-\frac{Vid}{2} + V_M - V_S - V_T\right)^2 \tag{3.22}$$

$$V_S = -\frac{1}{2}\sqrt{\frac{I_{SS}}{K_n} - V_{id}^2 - V_B^2} - \frac{V_B}{2} - V_T \tag{3.23}$$

The saturation condition of transistor is

$$V_{id} > 2\left(-V_M + V_S^{'} + V_T\right) \tag{3.24}$$

$$V_{id} < 2\left(V_M - V_S^{'} - V_T\right) \tag{3.25}$$

Where,

V_T is the threshold voltage of n- channel MOS transistor.

$$V_M \cong V_S^{'} + V_T \tag{3.26}$$

$$I_{SS} = K_N V_{id}^2 + 4I_o \tag{3.27}$$

$$I_{SS} = \frac{1}{4}K_N V_{id}^2 + I_o \tag{3.28}$$

Putting equation (3.28) in equation (3.23)

$$V_S = -\frac{1}{2}\sqrt{\frac{K_N V_{id}^2 + 4I_o}{K_n} - V_{id}^2 - V_B^2} - \frac{V_B}{2} - V_T \tag{3.29}$$

$$V_S = -\frac{1}{2}\sqrt{\frac{4I_o}{K_n} - V_B^2} - \frac{V_B}{2} - V_T \tag{3.30}$$

Now equation show that V_S is independent of V_{id} and show the linear characteristics.

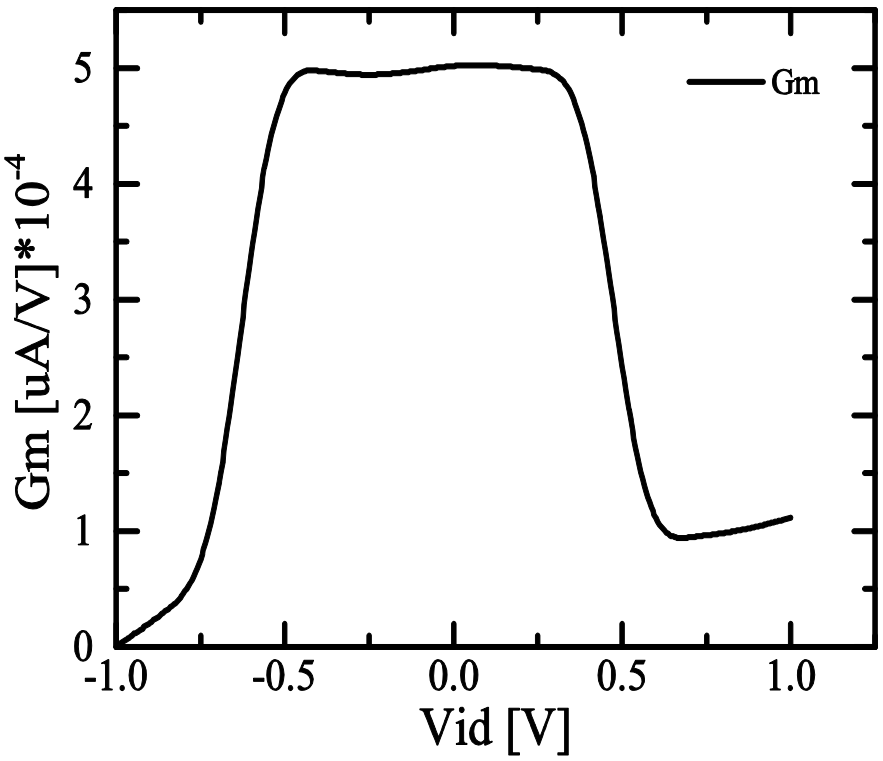

Figure 3.8 Transconductance Characteristics

The circuit is implemented in Cadence VIRTUOSO atmosphere of UMC .18µm CMOS method machinery operated with 27^0C with V_T = .523V.The DC voltage gain is 5.29 dB and the bandwidth of 1.69 GHz. The linear range within -62V to .54V [35].

3.2 Source Degeneration and Adaptive Biasing

3.2.1 CMOS Transconductor with Resistive Source Degeneration

In Resistive Source Degeneration techniques V-I characteristic for MOS transistor in the saturation region and the second order effect ignored for straightforwardness [11]. The circuit diagram of resistive source degeneration based transconductor is shown below in Figure 3.9.

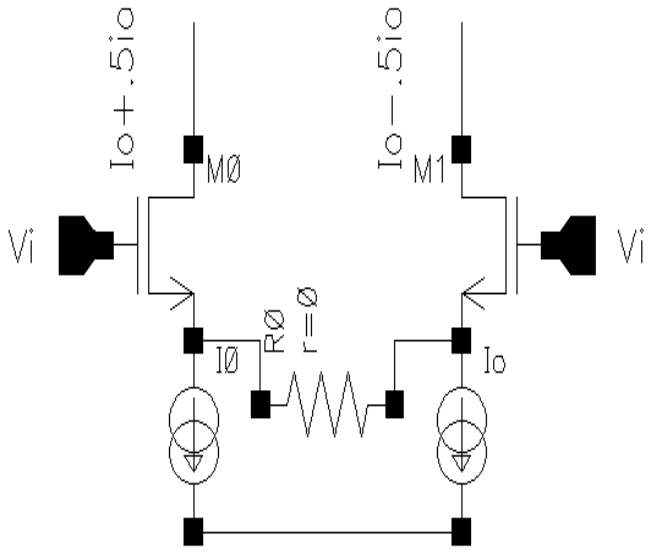

Figure 3.9 CMOS Transconductor Based On Degeneration Resistor

Drain current of the circuit given by

$$I_D = \frac{\beta}{2}\left(V_{gs} - V_t\right)^2 \tag{3.31}$$

In this circuit better linearity achieved for large gate to source voltage but for low gate to source voltage this gives poor linearity. We can solve this problem by using degeneration resistor but this will require large value of resistor to attain an extensive linear input limit. Given method removes tuning capability because this value is decided with the help of resistor.

3.2.2 Source Degeneration Method Based CMOS Transistor

In this techniques substitute resistor with two CMOS transistor working in the linear region of operation [11].

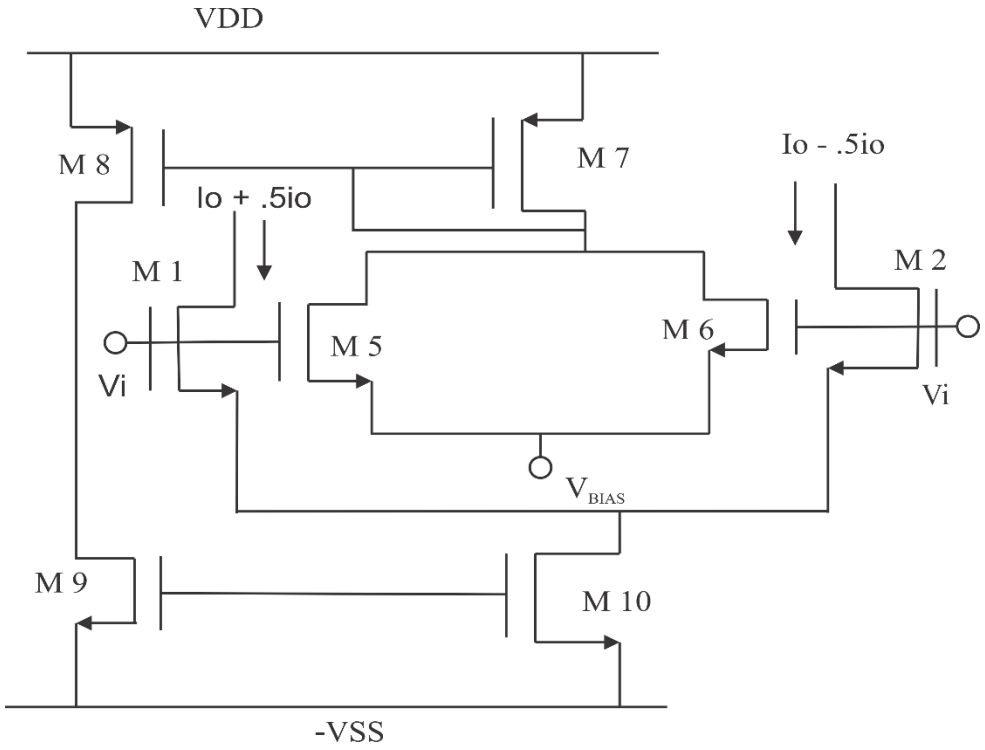

Figure 3.10 Source Degeneration Method Based MOS Transistor

Here M_1-M_2, M_3-M_4 should be perfectly matched and neglect second order effect. Transfer characteristic of this circuit is given is given as:

$$I_o = \frac{\sqrt{2\beta_1 I_o}}{a} V_i \sqrt{1 - \frac{\beta_1 V_i^2}{a^2 I_o}} \tag{3.32}$$

Where,

$$a = 1 + \frac{\beta_1}{4\beta_3} \tag{3.33}$$

Non-linear value below the square root have to made far lesser compare to unity and improved linearity and we can obtain superior input dynamic limit.

3.2.3 Adaptively Biased MOS Transistor

In this technique a tail current having an input reliant on quadratic component for terminate the nonlinear term only when

$$I_o = I^{'}_o + \frac{\beta V_i^2}{8} \tag{3.34}$$

According to technique nonlinear transfer characteristic (3.31) should transform into linear ones, tail current I_o must have the same value

$$I_o = I^{'}_o + \frac{\beta_1 V_i^2}{8a^2} \tag{3.35}$$

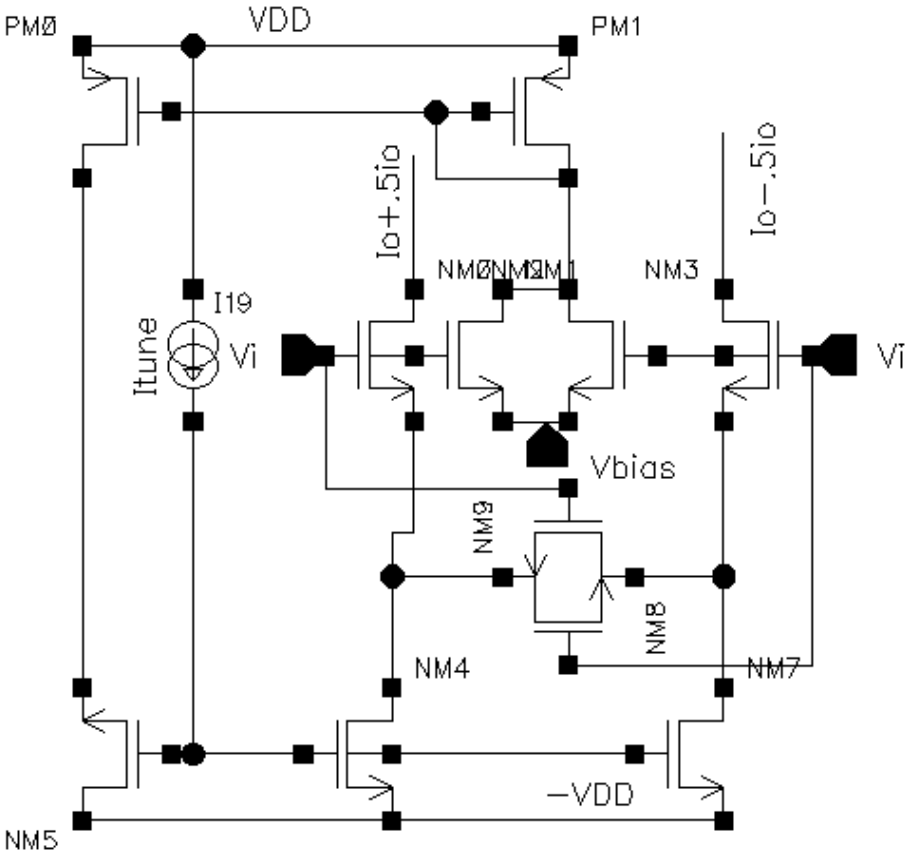

Figure 3.11 MOS transconductor based on Source Degeneration and Adaptive Biasing

The transfer characteristic converts linear and it is specified by

$$I_o = \frac{\sqrt{2\beta I_o}}{a} V_i \tag{3.36}$$

The adaptive bias current is given as

$$I_o = I_{tune} + \beta_5 \left(V_{GS5} - VT^2 \right) + \frac{\beta_5 V_i^2}{4} \tag{3.37}$$

$$I_o = I_o + \frac{\beta_5 V_i^2}{4} \tag{3.38}$$

Now compare the equation (3.38) (3.36), the transconductance coefficient of squaring circuit must be

$$\beta_5 = \beta_6 = \frac{\beta_1}{2a^2} \tag{3.39}$$

Since β_5 is lesser than β_1, the dc factor of current produced by the squaring circuit is minor to bias differential pair.

Consequently we require an external I_{TUNE} circuit to tune transconductor. This circuit is implemented in .35µm CMOS under a single voltage supply of 3.3V [11]. The entire transconductor dissipates 1mW for G_m=40µS and 5-MHz bandwidth [11]. The circuit shows the good linearity for fully balanced as well as unbalanced output.

3.3 TUNING

Filter based upon resonant loops. Any system contain poles and zeros. Poles may be dominant one or may be non-dominant. Ideally we want that our system should be single pole system means only one pole should be dominant and rest of the pole should be non-dominant. The frequency response and system stability depend upon the dominant pole. But practically we cannot neglect the effect of non-dominant pole. Due to non-dominant pole there is excessive phase in circuit, fortunately the resonant frequency have small sensitivity toward these effects. Most of automatic tuning is achieved phase locked loops [15].

There are two main method for tuning

- Voltage Controlled Oscillator
- Voltage Controlled Bandpass Filter

3.3.1 Voltage Controlled Oscillator

The block diagram for this procedure is given below in Figure 3.12.

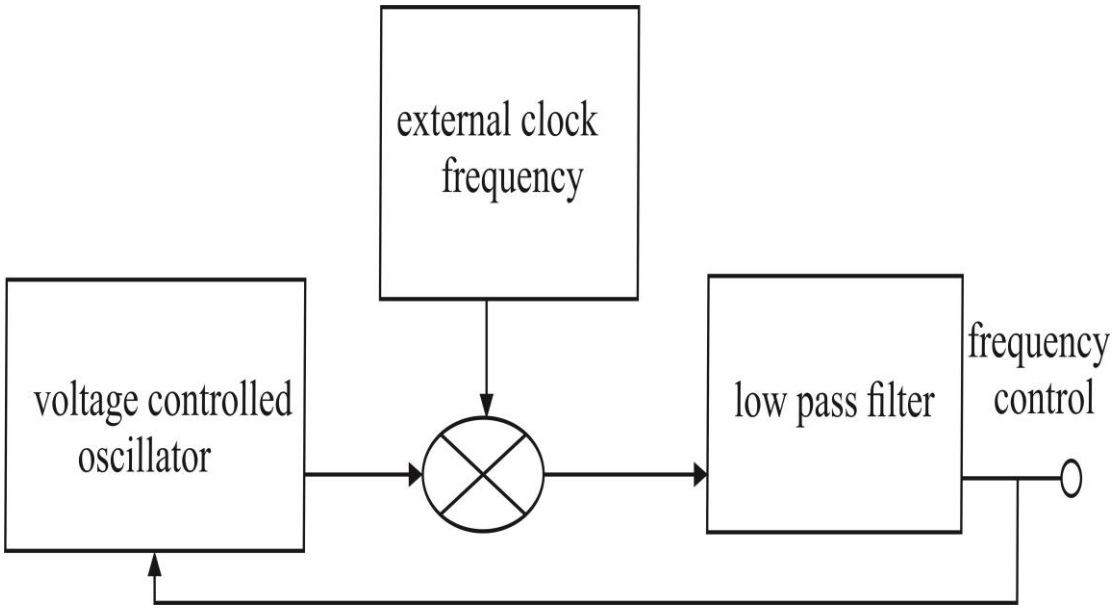

Figure 3.12 Voltage Controlled Oscillator (VCO)

3.3.2 Voltage Controlled Bandpass Filter

The block diagram representation of VCF is given blow in Figure 3.13.

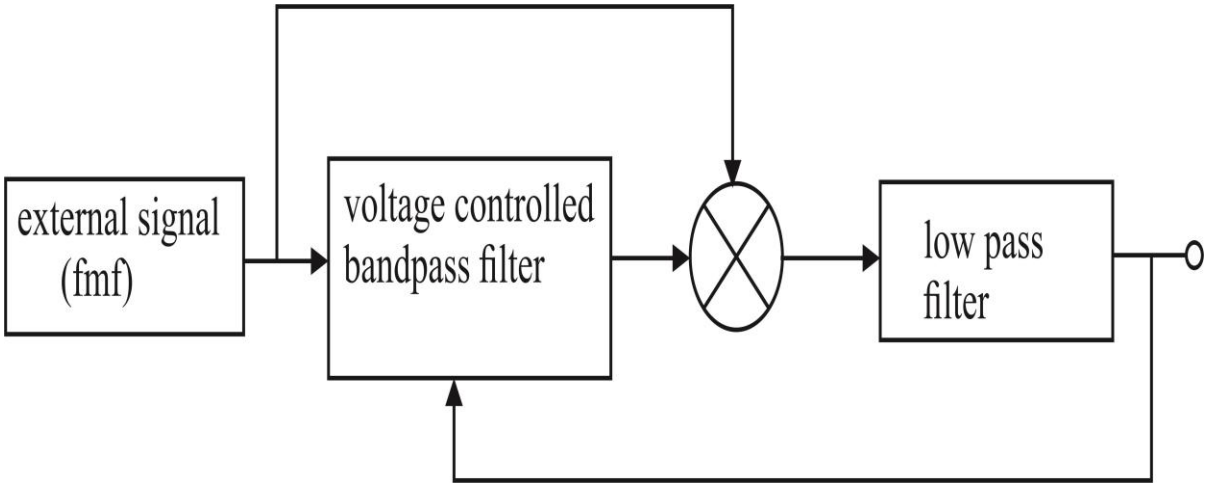

Figure 3.13 Voltage Controlled Bandpass Filter (VCF)

Low Voltage Linear Transconductor with Tuning Capability.

3.3.3 Tuning Technique Based Circuit

The technique presented by **Vijaya Bhaduria [23]** use the concept of bias offset voltage to tune the circuit and bias current of cross combined differential amplifier is accustomed to reduce third order harmonic distortion [34, 36]. The block level representation of technique is shown below in Figure 3.14.

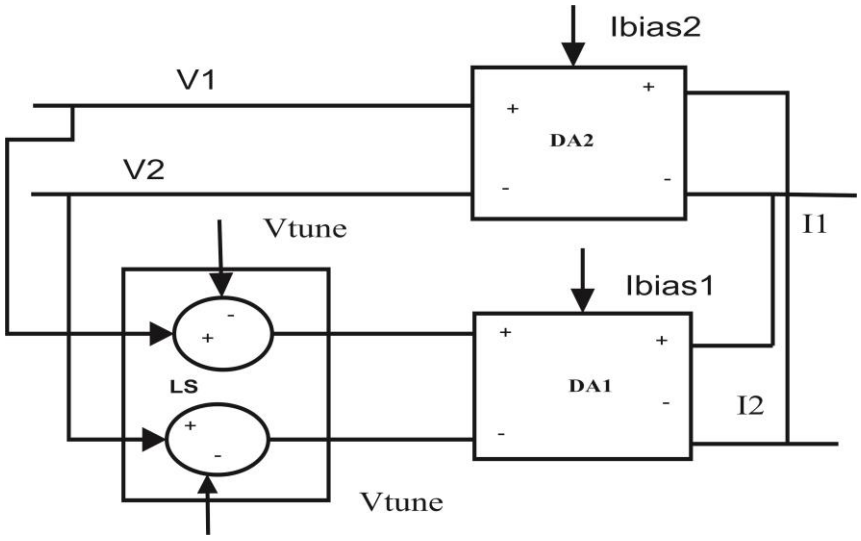

Figure 3.14 Low Voltage Linear Transconductor with Tuning Capability

It consist two differential amplifier (DA) one of them is used as compensatory differential amplifier (D_{A2}) and other work as normal differential amplifier (D_{A1}). The output of D_{A1} and D_{A2} are cross coupled. A two level shifter is used to connect input D_{A1} to D_{A2}. In this approach G_m is tune with the help of level shifter. We can offset the gate input of D_{A1} by altering tuning voltage applied at level shifter and G_M tuned to desired value [23].

The circuit is simulated in cadence .18µm virtuoso process technology. Bias current I_{bias1} is 240µA and I_{bias2} is 30µA. Vtune is varied from 1.2V to .6V and the step size is 0.1V. Transconductor show tuning within 310 to 100µS at tuning voltage varied from 1.2V to .6V. Harmonic distortion is -30 dB at tuning voltage of 0.9V.

Chapter 4 SCOPE OF STUDY

SCOPE OF THE STUDY

Centered on the literature review the following scope of the study of linear transconductor and analog circuits design based on transconductor application have been listed as

Different practices have been recommended to improve the linearity of the transconductor but in low-voltage applications the non-linearity problems exist in many transconductor circuits. Researchers have reported Total harmonic distortion (THD) of the transconductance circuits, but there is a possibility to reduce this factor to the lower values. For the use of the linear transconductor in the designing of Gm-C filters, the there is a tradeoff between bandwidth and intrinsic gain when selecting MOS drain current, inversion level and channel length. In previous years the more attention of research is given to improve the linearity of the transconductor. But very less importance is given to the noise analysis of the transconductance. If we introduced linearization methods there will be appear extra nodes in circuit generating parasitic poles and zeros and hence there is degradation at high frequency application.

Chapter 5 OBJECTIVE OF STUDY

OBJECTIVE OF THE STUDY

The main objective to design the tunable transconductor is that tunable transconductor is required for the tune-ability of Q factor of filters and center frequency. And helps to compensate the fabrication tolerances and the environmental parameters, especially temperature. There is a requirement of high transconductance and good controllability in higher frequency continuous time filter and the used OTA filter should provide high transconductance and good controllability. Good linearity related to that OTA must have constant Gm, graph in his input limit [3]. The linearity during the voltage-to-current conversion should usually preserved because the linear range of transconductor govern the linearity of whole system. Now a day the challenge is that the power supply and size of the device is scale down to achieve more speed because of this linearity create problem to achieve sufficient signal level [1]. Most of transconductor application system requires low noise and current consumption along with good linearity over a significant range. In transconductor due to differential structure even harmonics does not exit but odd harmonics play a vital role in the distortion of the output current [2]. In literature, several researchers have been reported linear Transconductor and its applications. OTA are widely used as active element in switched capacitor filter, data converter, and sample and hold circuits, or as buffer amplifier for driving large capacitive loads. OTA has fast setting response. In this report, the basic principle of linear transconductor has been addressed and some of the analog circuits based on transconductor are also investigated. The objectives of the thesis work is proposed as

1. To improve the linearity of the transconductor for low voltage operations.
2. To reduce the total harmonic distortion (THD) of the linear transconductor.
3. To develop transconductor circuit based applications such as multipliers and squarer.
4. To improve the noise performance of the linear transconductor circuits.
5. Design the transconductor for low voltage environment and for low power application circuits.
6. Second order effect (mobility effect, channel length effect, body effect) free transconductor circuit.

Chapter 6 RESEARCH METHODOLOGY

RESEARCH METHODOLOGY

The research methodology adopted for the present research work is as follows

- Identification of the issues and challenges regarding the linearity and tune-ability of the circuits.
- Comparison of the existing analog transconductor circuits.
- Understanding the complete tool package used to design the analog circuits.
- Understanding the various types of analysis used in analog circuits.
- Designing a new tunable.
- Simulations for the proposed circuit and compare it with other exiting circuit.

Chapter 7 SIMULATION AND RESULTS

7.1 SIMULATION AND RESULTS

7.1.1 Low Voltage Linear Transconductor with Tuning Capability.

This circuit have two differential amplifier. One is used for normal operation of differential operation other one is used for compensation for harmonic distortion. And the output of these two amplifier is cross coupled. Transistor N_0 and N_1 form the level shifter. Tunable voltage is controlled with the help of level shifter. In this circuit two bias current is used for biasing of these two differential amplifier.

7.1.2 Schematic Diagram

Schematic diagram of this technique is presented below on Figure 6.1.

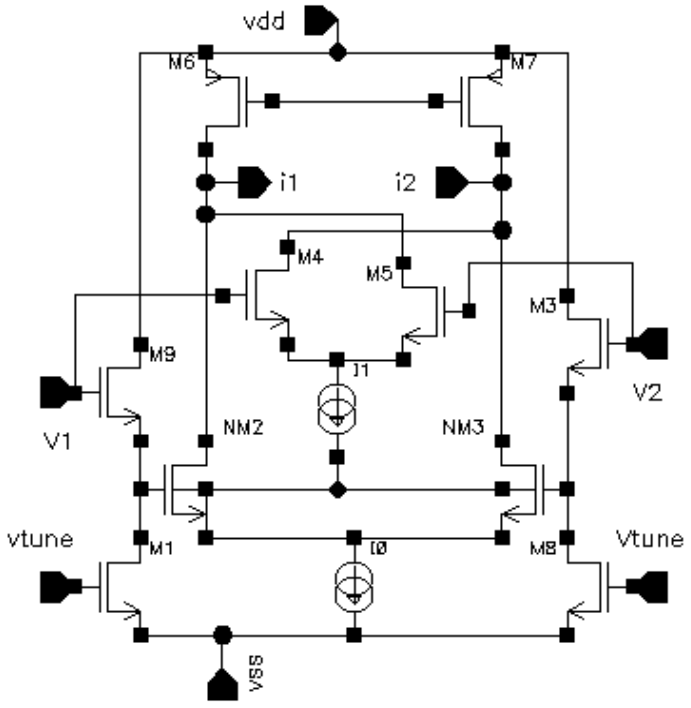

Figure 7.1 Schematic Representation of Linear Transconductance

7.1.3 Functional Description of Circuit

It consist two differential amplifier (D_A) one of them is used as compensatory differential amplifier (D_{A2}) and other work as normal differential amplifier (D_{A1}) [23]. The output of D_{A1} and D_{A2} are cross coupled. A two level shifter is used to connect input D_{A1} to D_{A2}. In this approach Gm is tune with the help of level shifter. We can offset the gate input of D_{A1} by altering tuning voltage applied at level shifter and G_M tuned to desired value. Some relation regarding the W/L ratio of these two bias current is given below.

$$\frac{I_{bias1}}{I_{bias2}} = \left\{ \frac{W2/L2}{W5/L5} \right\}^3 \tag{6.1}$$

And the gain of transconductance is given below

$$G_m = \frac{\Delta I_0}{\Delta V_{id}} \tag{6.2}$$

The I_0 current and input differential voltage is calculated for different Tuning voltage.

The drain current of PMOS and the difference of input voltage at a given tuning voltage is require to check whether all the transistor is working in a proper operating region or not.

All the transistor related to differential amplifier should working in saturation region. And the PMOS should be operated in linear region and the main use of PMOS is a working like a resistor.

$$\beta_{23} = \beta_{54} \tag{6.3}$$

Tuning voltage signal is applied at applied the input of both the level shifter. We have to provide a proper input signal which cause the level shifter CMOS transistor and main differential signal into saturation region [26- 28]. We have to choose proper width to length ratio so that working of transistor into saturation is ensure. For this condition the transistor dimension should follow this condition

$$\beta_{23} = \beta_{54} \tag{6.4}$$

7.1.4 Analysis of Drain Current and Transconductance at V_{tune} .6V

Circuit parameter is calculated when V_{tune} voltage is fixed at .6V. And the other voltage is variable to generate differential input voltage. For each differential voltage value of I_1 and I_2 is calculated and value of transconductance is calculated. Maximum value of G_m is $5.3(10^{-4}S)$ and minimum value is $1.7(10^{-4}S)$.

Table 7.1 Circuit Parameters for V_{tune} .6V

V_{tune} = .6V					
V_2(V)	V_1(V)	V_{id}(V)	I_2(µA)	I_1(µA)	Gm (10^{-4}S)
1	0	-1	208.99	31.00	1.7
1.4	.6	-.8	209.99	30.0	2.2
1.2	.6	-.6	209.9	30.0	2.9
1	.6	-.4	206.63	33.36	4.3
.8	.6	-.2	173.023	66.97	5.3
.7	.6	-.1	143.07	96.92	4.6
.6	.7	.1	96.92	143.92	4.6
.6	.8	.2	66.97	173.023	5.3
.6	1	.4	33.36	206.63	4.3
.6	1.2	.6	30.0	209.9	2.9
.6	1.4	.8	30.0	209.07	2.2
0	1	1	31	208.99	1.7

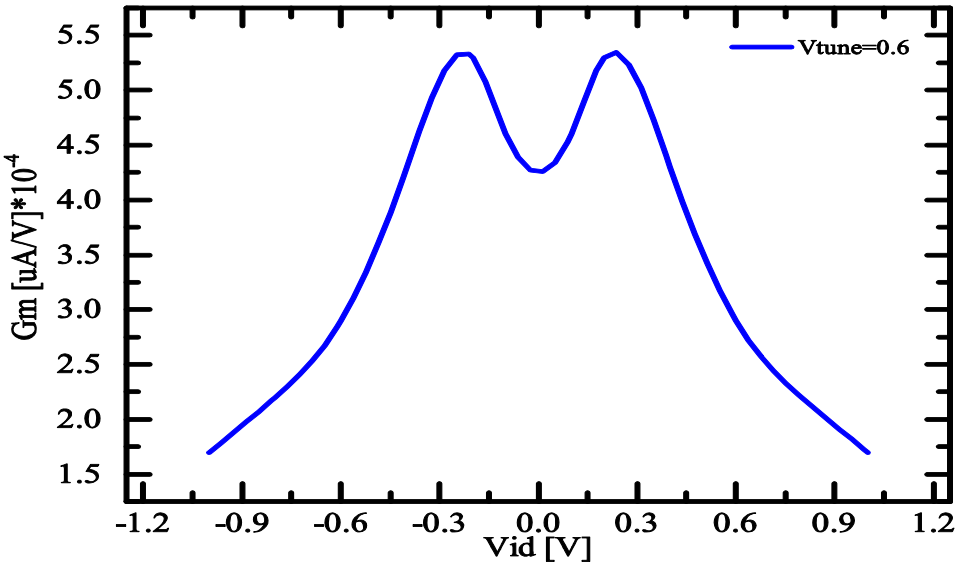

Figure 7.2 Differential Input Signal (V_{id}) vs Transconductance at V_{tune} .6V

7.1.5 Analysis of Drain Current and Transconductance at V_{tune} .7V

Circuit parameter is calculated when V_{tune} voltage is fixed at .7V. And the other voltage is variable to generate differential input voltage. For each differential voltage value of I_1 and I_2 is calculated and value of transconductance is calculated. Maximum value of G_m is $4.9(10^{-4}S)$ and minimum value is $1.7(10^{-4}S)$.

Table 7.2 Circuit Parameters for V_{tune} .7V

V_{tune} = .7V					
V_2(V)	V_1(V)	V_{id}(V)	I_2(µA)	I_1(µA)	$G_m(10^{-4}S)$
1.8	.8	-1	205	34.782	1.7
1	.2	-.8	205.217	34.782	2.13
1.2	.6	-.6	209.721	30.27	2.99
1	.6	-.4	201.4	38.58	4.0
.9	.7	-.2	169.161	70.83	4.9
.8	.7	-.1	140.38	99.61	4.0
.7	.8	.1	99.61	140.38	4.0

.7	.9	.2	70.83	169.161	4.9
.6	1	.4	38.58	201.4	4.0
.6	1.2	.6	30.27	209.721	2.99
.2	1	.8	34.782	20.217	2.13
.8	1.8	1	34.782	205	1.7

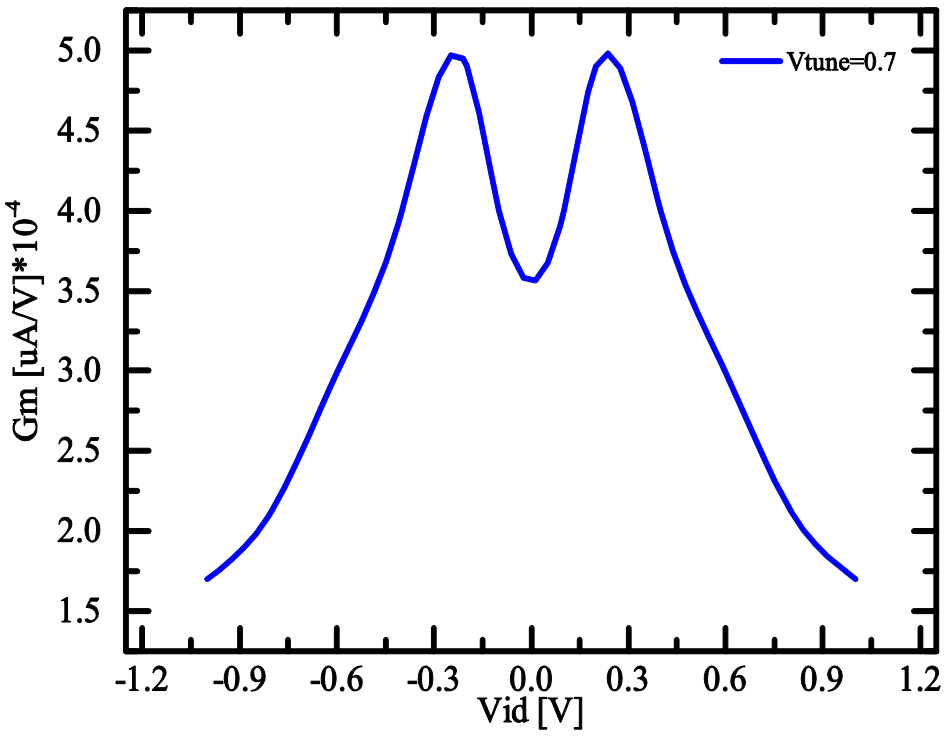

Figure 7.3 Differential Input Signal (V_{id}) vs Transconductance at V_{tune} .7V

7.1.6 Analysis of Drain Current and Transconductance at V_{tune} .8V

Circuit parameter is calculated when V_{tune} voltage is fixed at .8V. And the other voltage is variable to generate differential input voltage. For each differential voltage value of I_1 and I_2 is calculated and value of G_m is calculated. Maximum value of G_m is $4.53(10^{-4}S)$ and minimum value is $1.8(10^{-4}S)$.

Table 7.3 Circuit Parameters for V_{tune} .8V

V_{tune} = .8V					
V_2(V)	V_1(V)	V_{id}(V)	I_2(µA)	I_1(µA)	$G_m(10^{-4}S)$
1.8	.8	-1	210	30	1.8
1.8	1	-.8	209.9	30.7	2.25
1.1	.5	-.6	205.636	34.36	2.85
1	.6	-.4	190.633	49.36	3.53
1	.8	-.2	165.257	74.742	4.52
.9	.8	-.1	138.4	101.598	3.68
.8	.9	.1	101.598	138.4	3.68
.8	1	.2	74.742	165.257	4.52
.6	1	.4	49.36	190.633	3.53
.5	1.1	.6	34.36	205.636	2.85
1	1.8	.8	30.7	209.9	2.25
.8	1	1	30	210	1.8

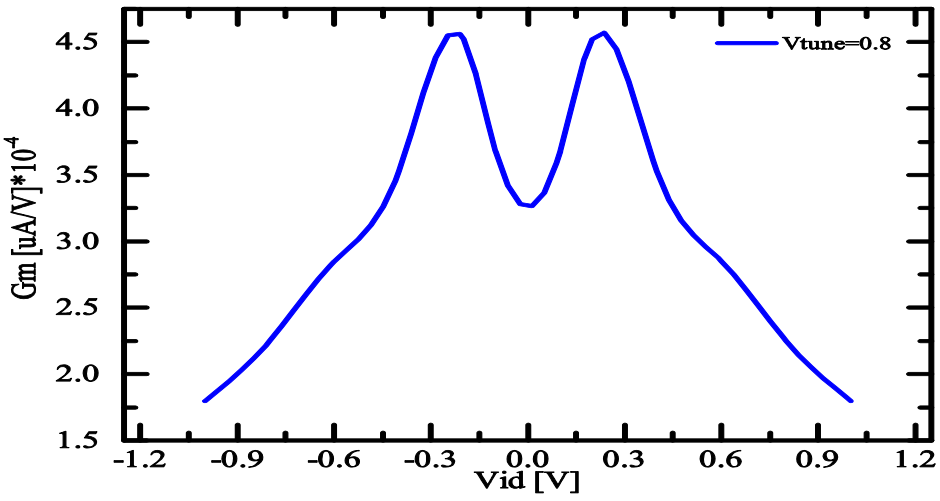

Figure 7.4 Differential Input Signal (V_{id}) vs Transconductance at V_{tune} .8V

7.1.7 Analysis of Drain Current and Transconductance at V_{tune} .9V

Circuit parameter is calculated when V_{tune} voltage is fixed at .9V. And the other voltage is variable to generate differential input voltage. For each differential voltage value of I_1 and I_2 is calculated and value of transconductance is calculated. Maximum value of G_m is $4.2(10^{-4}S)$ and minimum value is $1.8(10^{-4}S)$.

Table 7.4 Circuit Parameters for V_{tune} .9V

V_{tune} = .9V					
V_2(V)	V_1(V)	V_{id}(V)	I_2(µA)	I_1(µA)	$G_m(10^{-4}S)$
1.8	.8	-1	210	30	1.8
1.8	1	-.8	210	30.01	2.25
1.4	.8	-.6	204.935	35.01	2.813
1.2	.8	-.4	197.268	42.731	3.816
1.2	1	-.2	168.58	71.411	4.85
1.1	1	-.1	141.207	98.79	4.2
1	1.1	.1	98.79	141.207	4.2
1	1.2	.2	71.79	168.58	4.85
.8	1.2	.4	42.731	197.268	3.86
.8	1.4	.6	35.06	204.935	2.813
1	1.8	.8	30.01	210	2.25
.8	1.8	1	30	210	1.8

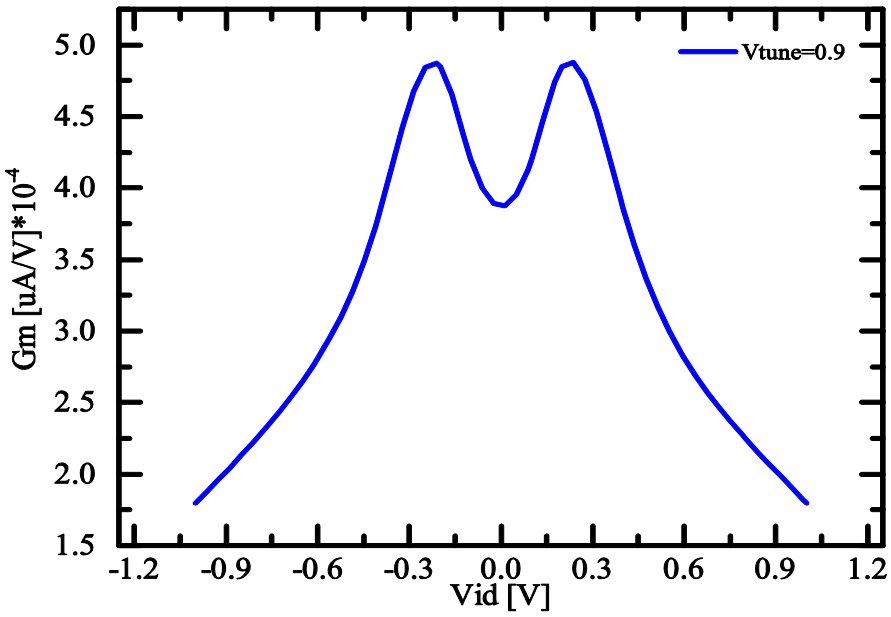

Figure 7.5 Differential Input Signal (V_{id}) Vs Transconductance at V_{tune} .9V

7.1.8 Analysis of Drain Current and Transconductance at V_{tune} 1V

Circuit parameter is calculated when V_{tune} voltage is fixed at 1V. And the other voltage is variable to generate differential input voltage. For each differential voltage value of I_1 and I_2 is calculated and value of G_m is calculated. Maximum value of G_m is 4.07(10^{-4}S) and minimum value is 1.79(10^{-4}S).

Table 7.5 Circuit Parameters for V_{tune} 1V

V_{tune} = 1V					
V_2(V)	V_1(V)	V_{id}(V)	I_2(µA)	I_1(µA)	G_m(10^{-4}S)
1.8	.8	-1	209.99	30	1.79
1.8	1	-.8	209.97	30.07	2.24
1.8	1.2	-.6	209.87	34.63	2.99
1.6	1.2	-.4	205.36	34.63	4.26
1.3	1.1	-.2	165.08	74.91	4.50
1.2	1.1	-.1	139.153	100.84	3.8

1.1	1.2	.1	100.84	139.153	3.8
1.1	1.3	.2	74.91	165.08	4.50
1.2	1.6	.4	34.63	205.36	4.26
1.2	1.8	.6	30.12	209.87	2.99
1	1.8	.8	30.0076	209.00	2.24
.8	1.8	1	30	209.9	1.79

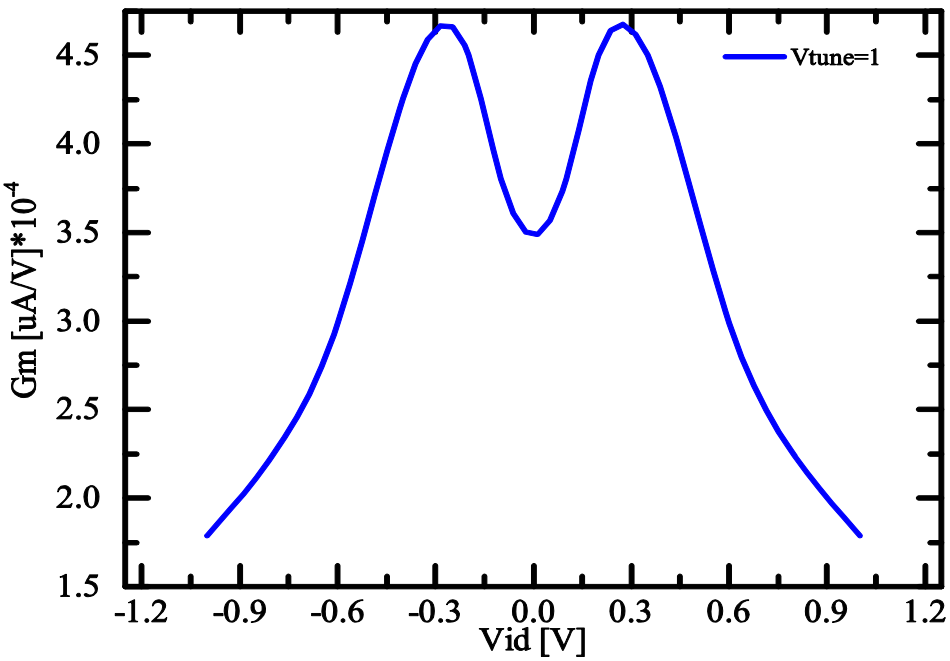

Figure 7.6 Differential Input Signal (V_{id}) Vs Transconductance at V_{tune} 1V

7.1.9 Analysis of Drain Current and Transconductance at V_{tune} 1.1V

Circuit parameter is calculated when V_{tune} voltage is fixed at .6V. And the other voltage is variable to generate differential input voltage. For each differential voltage value of I_1 and I_2 is calculated and value of transconductance is calculated. Maximum value of G_m is $5.3(10^{-4}S)$ and minimum value is $1.79(10^{-4}S)$.

Table 7.6 Circuit Parameters for V_{tune} 1.1V

V_{tune} = 1.1V					
V_1(V)	V_2(V)	V_{id}(V)	I_2(µA)	I_1(µA)	$G_m(10^{-4}S)$
1.8	.8	-1	209.99	30.03	1.79
.8	1.8	1	30.03	209.99	1.79
1.8	1	.8	209.95	30.5	2.24
1	1.8	-.8	30.5	209.95	2.24
1.8	1.2	.6	209.66	30.3	2.98
1.2	1.8	-.6	30.3	209.66	2.98
1.6	1.4	.4	201.55	38.44	4.07
1.2	1.6	-.4	38.44	201.55	4.07
1.6	1.4	.2	171.57	68.4	5.15
1.4	1.6	-.2	68.4	171.57	5.15
1.5	1.4	.1	143.758	96.24	4.75
1.4	1.5	-.1	96.24	143.758	4.75

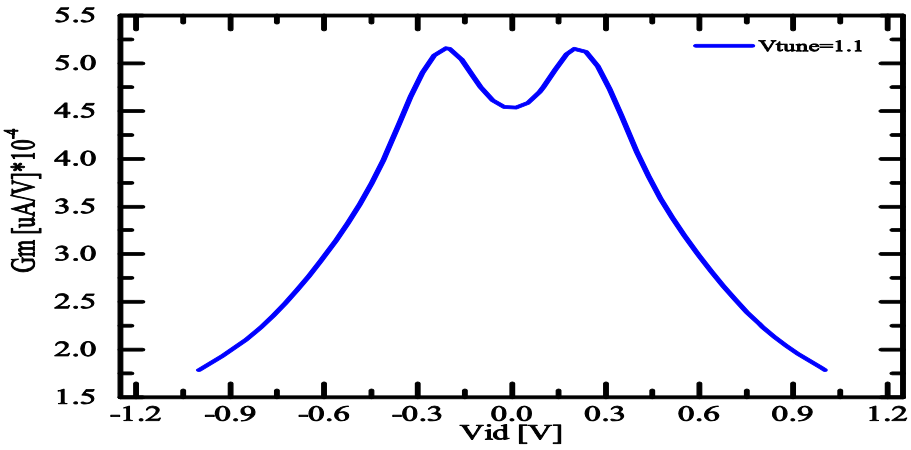

Figure 7.7 Differential Input Signal (V_{id}) Vs Transconductance at V_{tune} 1.1

7.1.10 Analysis of Drain Current and Transconductance at V_{tune} 1.2V

Circuit parameter is calculated when V_{tune} voltage is fixed at 1.2V. And the other voltage is variable to generate differential input voltage. For each differential voltage value of I_1 and I_2 is calculated and value of G_m is calculated. Maximum value of G_m is $2.56(10^{-4}S)$ and minimum value is $1.6(10^{-4}S)$.

Table 7.7 Circuit Parameters for V_{tune} 1.2V

V_{tune} = 1.2V					
V_1(V)	V_2(V)	V_{id}(V)	I_2(µA)	I_1(µA)	$G_m(10^{-4}S)$
1.3	.3	1	200.10	39.89	1.6
.3	1.3	-1	39.89	200.10	1.6
1.3	.5	.8	199.62	40.379	1.9
.5	1.3	-.8	40.379	199.62	1.9
1.3	.7	.6	199.62	40.379	2.6
.7	1.3	-.6	40.62	199.62	2.6
1.2	.8	.4	172.344	76.65	2.61
.8	1.2	-.4	76.344	172.344	2.61
1.2	1	.2	145.68	94.31	2.56
1	1.2	-.2	94.31	145.31	2.56
1.2	1.1	.1	131.185	108.81	2.23
1.1	1.2	-.1	108.81	131.185	2.23

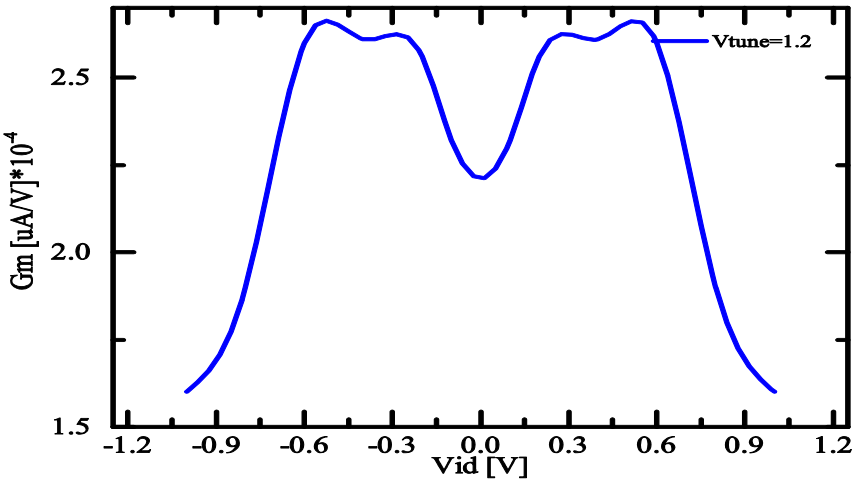

Figure 7.8 Differential Input Signal (V_{id}) Vs Transconductance at V_{tune} 1.2

Figure 6.9 shown below gives the complete behavior of the circuit for variable V_{tune} from .6V to 1.2V. And show how the transconductance will change, if there is a change in V_{tune} voltage and change in input differential voltage.

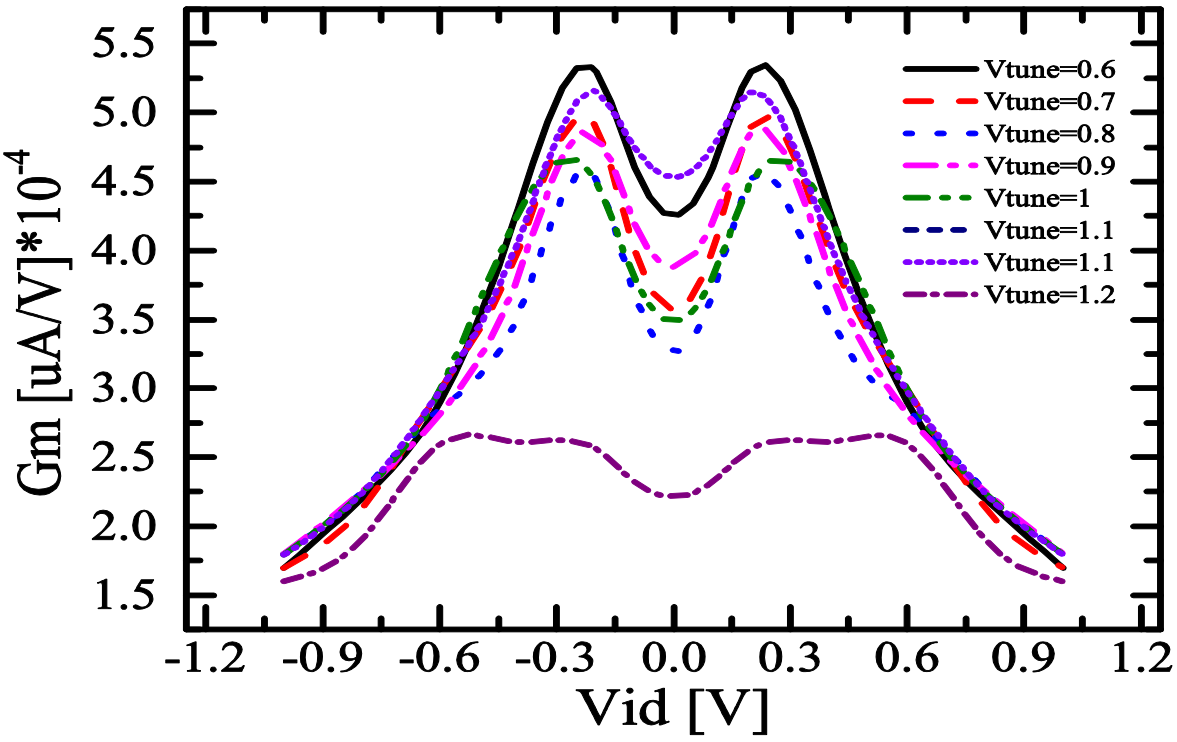

Figure 7.9 Differential Input Signal (V_{id}) vs Transconductance at variable V_{tune}

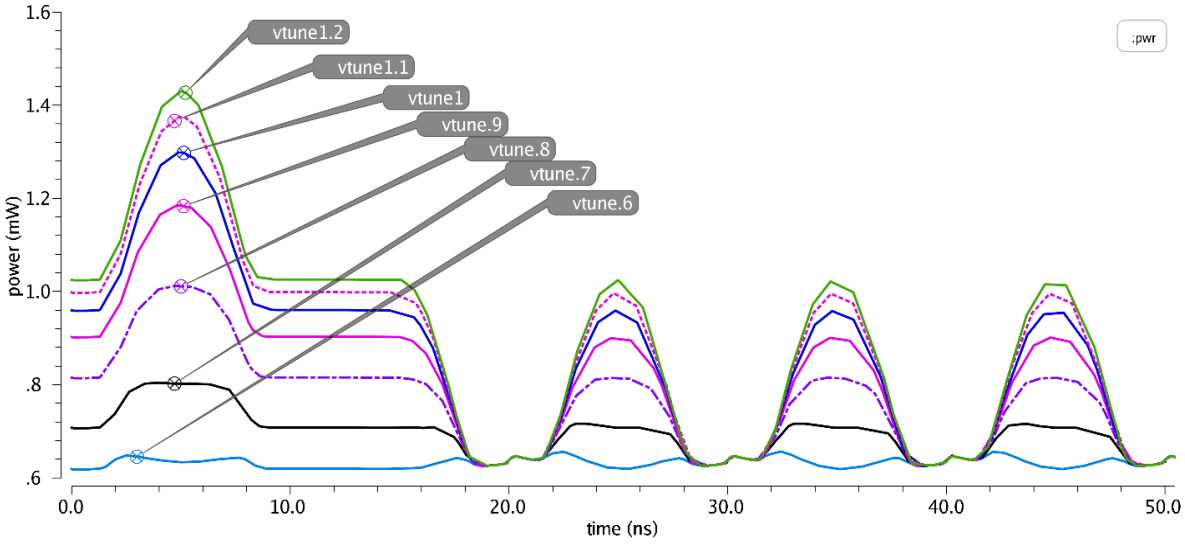

Figure 7.10 Power Consumption of the circuit for different V_{tune} Voltage.

The circuit is simulated in cadence .18um virtuoso process technology. Bias current I_{bias1} is 240µA and I_{bias2} is 30µA. V_{tune} is varied from 1.2V to .6V and the step size is 0.1V. Transconductor show tuning within 515µS to 160µS at tuning voltage varied from 1.2V to .6V. From the circuit analysis we found that the circuit is symmetric because all the transconductance graph is follow even symmetric property. All the value of transconductance for V_1 input and V_2 input is same. Here we plot the magnitude of transconductance with respect to differential input signal.

7.2 CMOS High-Frequency and Low-Voltage Tunable Positive Transconductor with an Improved Linearization Technique

The performance of transconductor is improved by giving them of programmability. A common approaches is use transistors operating in linear operating region as variable resistors. Several linearization methods have been established to solve the difficult of the high distortion introduced in topologies based on linear MOS transistors [22].

The given structure is centered on pseudo differential class-A CMOS inverter amplifiers with active load. The advantages of using this configuration, against others like auto polarized [29] or RGC (Regulated-Cascode) [20-21], are the lower supply voltage and the greater bandwidths. A NMOS transistor operating in the linear operating region, M_{N3}, is used as a variable resistor placed in the second stage, thus obtaining a highly linear and voltage tunable transconductor

with extensive bandwidth capable of low voltage operation. Both [16] and [18] understand an extensive summary of the theory and the implementations of given circuit in Figure 6.11.

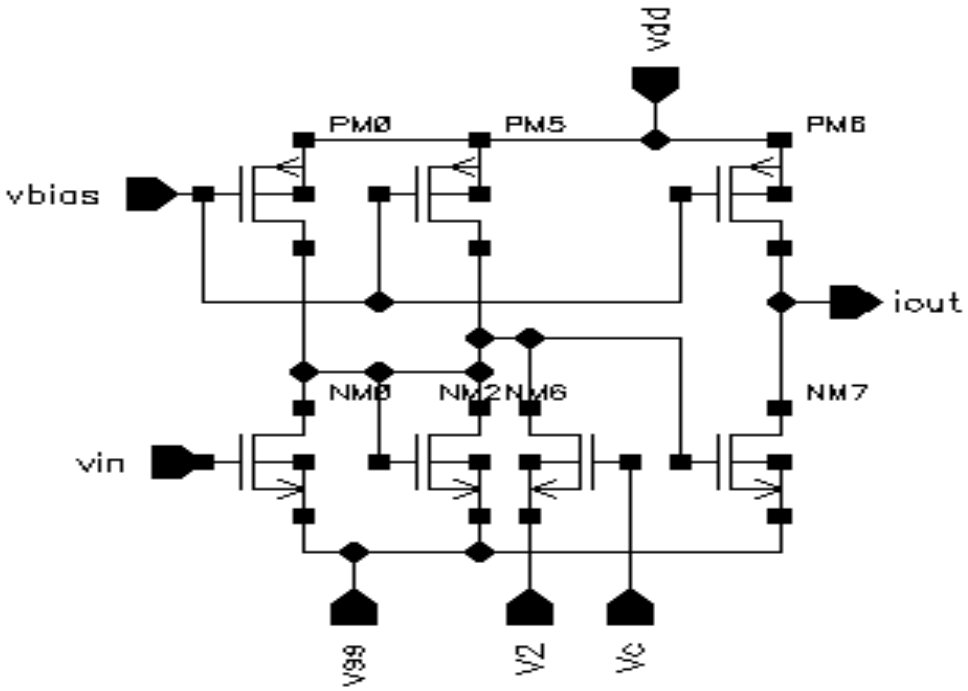

Figure 7.11 Positive Tunable Transconductor

The input voltage and output current relation is given as

$$i_o = \left[\frac{2I_{BIAS}}{V_c - 2V_{thN}} \right] V_{in} \tag{6.5}$$

The transconductance of the circuit, G_m, given in the equation (6.5) and its value can be controlled by changing the value of V_c. In the measurement conditions, were considered both input and output capacitors and line resistors whose values are 1pF and 50Ω respectively.

The transconductance as a function of the input voltage amplitude (V_{in}) is depicted in Figure 6.12 for different V_C values.

Table 7.8 Transconductance as a function of controlling voltage V_c

V_{in}(mV)	V_c = 1.10v Gm(10^{-4}S)	V_c=1.03V Gm(10^{-4}S)	V_c=.95V Gm(10^{-4}S)	V_c=.88V Gm(10^{-4}S)	V_c=.80V Gm(10^{-4}S)
-0.3	0.751	0.851	0.901	1.000	1.121
-0.25	0.755	0.855	0.915	1.011	1.143
-0.20	0.761	0.861	0.921	1.012	1.151
-0.15	0.765	0.865	0.925	1.013	1.158
-0.10	0.771	0.871	0.911	1.021	1.161
0.00	0.776	0.876	0.926	1.031	1.165
0.10	0.771	0.871	0.911	1.021	1.161
0.15	0.765	0.865	0.925	1.013	1.158
0.20	0.761	0.861	0.921	1.012	1.151
0.25	0.755	0.855	0.915	1.011	1.143
0.30	0.751	0.851	0.901	1.000	1.121

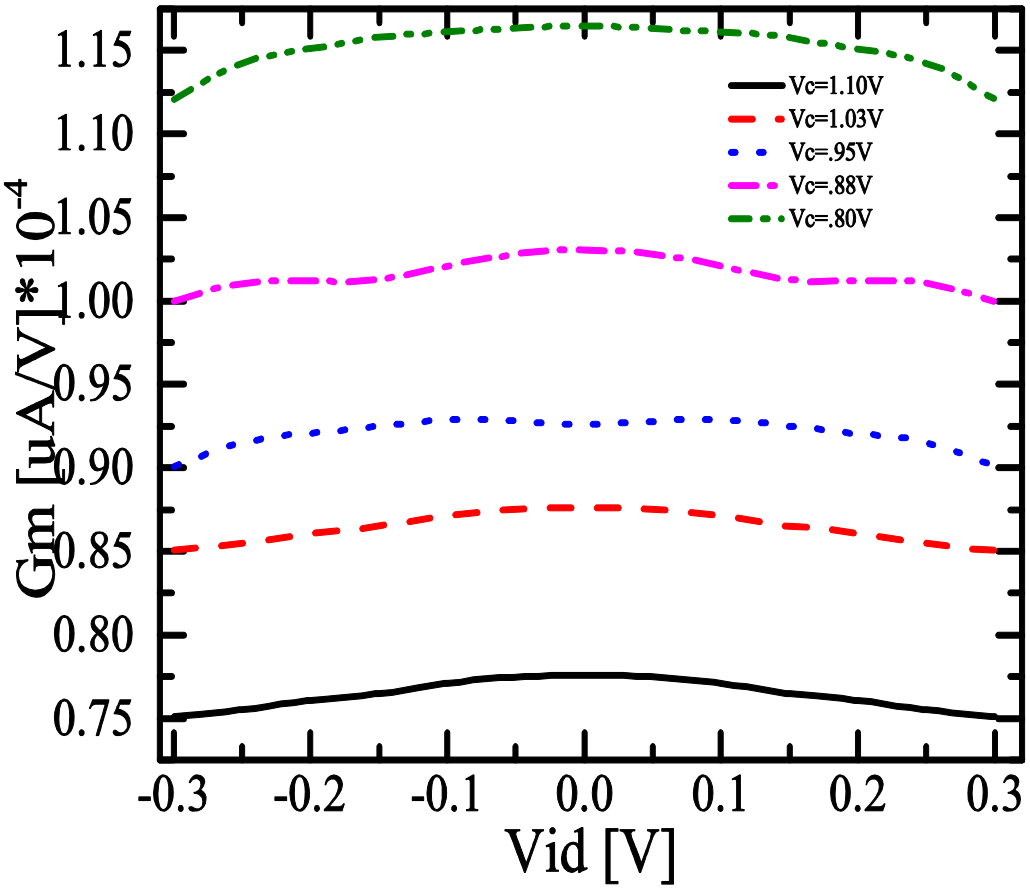

Figure 7.12 Transconductance as a function of controlling voltage Vc

Table 7.9 Bandwidth and Transconductance as a function of Vc

V_c(V)	G_m(mS)	Bandwidth(GHz)
0.80	1.165	2.10
0.85	1.031	2.15
0.90	0.956	2.19
0.95	0.926	2.22
1.00	0.874	2.25
1.05	0.834	2.28
1.10	0.776	2.30

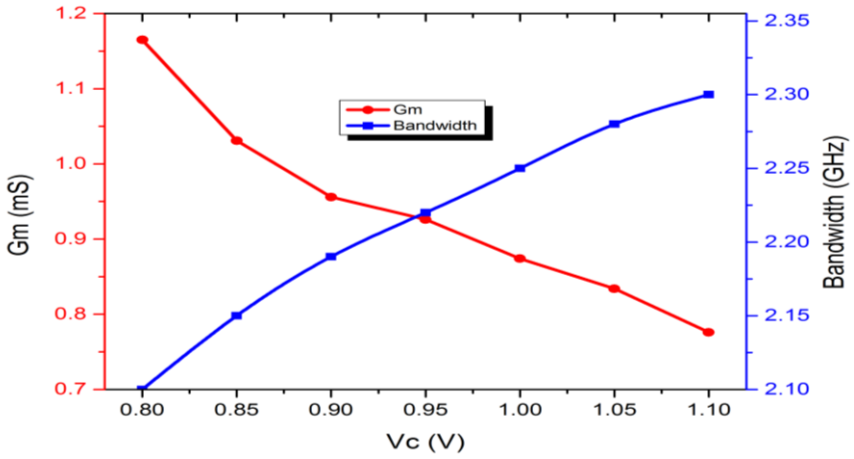

Figure 7.13 Bandwidth and Transconductance as a function of Vc

This system based on class A inverter amplifier work on 2.2V supply voltage and it consume 12mW. Circuit is simulated using .35µm CMOS technology. 750µS transconductance is achieved using this configuration.

7.3 Proposed Tunable Transconductor with High Linearity

In this technique circuit is built with the help of two differential amplifier, one differential amplifier is used for obtained desired transconductance value, known as gain differential amplifier, and other is used for compensation of harmonic distortion present in the circuit, known as compensation differential amplifier. Tune-ability is obtained using the bias offset at the gate of differential amplifier [29]. Compensation is controlled with the help of bias current such that the operating region of level shifter transistor is strong inversion region. It consist of gain amplifier and compensation amplifier with their output are cross coupled. Input are connected to differential amplifier with the help of a pair of level shifter.

7.3.1 Schematic diagram

Circuit diagram of this technique is given below in Figure 6.14.

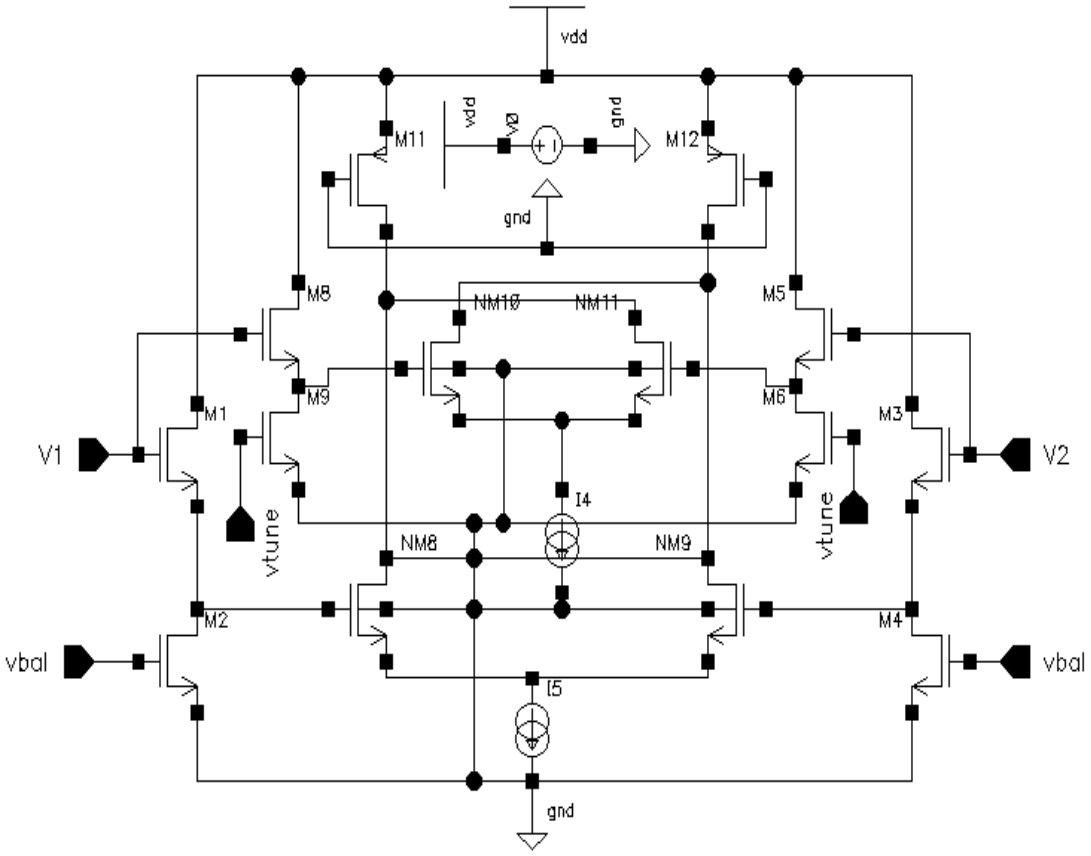

Figure 7.14 Tunable Transconductor with High Linearity

7.3.2 Functional details

Thus Gm can be tuned by varying V_{tune} and it increases as

$$G_m = \frac{\Delta I_0}{\Delta V_{id}} \tag{6.5}$$

V_{tune} decreases. Tuning voltage, V_{tune} is varied from 0.5 V to 1.0 V in steps of 0.1 V. The lower value (0.5 V) is kept slightly higher than the threshold voltage of input transistors N_{M2} and N_{M4} of L_{S1} to keep them in strong inversion region. Circuit parameter is calculated when V_{tune} voltage is fixed at .9V. And the other voltage is variable to generate differential input voltage. For each differential voltage value of I_1 and I_2 is calculated and value of transconductance is calculated. Maximum value of G_m is $4.2(10^{-4}S)$ and minimum value is $1.8(10^{-4}S)$.

7.3.3 Analysis of Drain Current, Transconductance & Power Consumption for V_{tune} .5V

Table 7.10 Drain current and Transconductance for V_{tune} .5V

V_1(V)	V_2(V)	V_{id}((V)	I_1(μA)	I_2(μA)	$G_m(10^{-4}S)$
-0.8	0.4	-1	52.17	52.09	0.08
-0.4	0.4	-.08	56.82	47.54	0.11
-0.2	0.4	-0.6	56.82	47.45	0.15
1.15	1.55	-0.4	91.76	12.23	2.13
1	1.2	-0.2	83.74	20.29	3.17
0.4	0.5	-0.1	64.26	40	2.42
0.5	0.4	0.1	40	64.26	2.42
1.2	1	0.2	20.29	83.74	3.17
1.55	1.15	0.4	12.23	91.76	2.13
0.4	-0.2	0.6	47.45	56.82	0.15
0.4	-0.4	0.8	47.54	56.82	0.11
0.2	-0.8	1	52.09	52.17	0.08

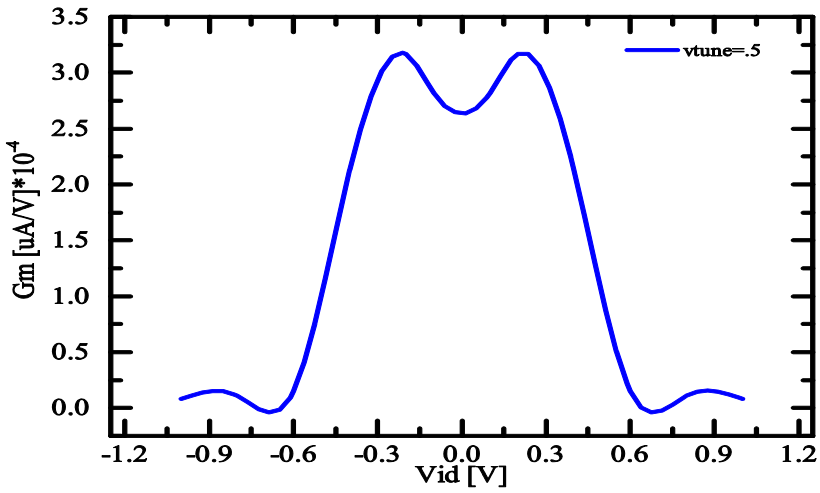

Figure 7.15 Transconductance (G_m) Vs differential signal input (v_{id}) at V_{tune} .5V

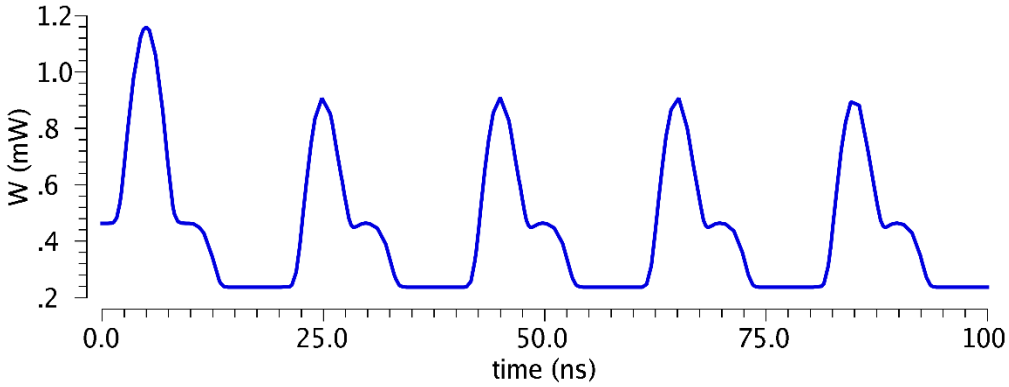

Figure 7.16 Power Consumption at V_{tune} .5V

7.3.4 Analysis of Drain Current, Transconductance & power consumption for V_{tune} .6V

Circuit parameter is calculated when V_{tune} voltage is fixed at .6V. And the other voltage is variable to generate differential input voltage. For each differential voltage value of I_1 and I_2 is calculated and value of transconductance is calculated. Maximum value of G_m is $4.2(10^{-4}S)$ and minimum value is $1.8(10^{-4}S)$.

Table 7.11 Drain current and Transconductance for V_{tune} .6V

V_1(V)	V_2(V)	V_{id}((V)	I_1(µA)	I_2(µA)	$G_m(10^{-4}S)$
-.650	.350	-1	53.02	51.25	0.01
1	1.8	-.8	54.51	49.76	.05
-.05	.55	-.6	67.09	37.16	.49
.8	1.2	-.4	91.71	12.32	1.98
1	1.2	-.2	83.47	20.57	3.15
.4	.5	-.1	113.657	92.532	2.10
.5	.4	.1	92.532	113.657	2.10
1.2	1	.2	20.57	83.47	3.15
1.2	.8	.4	12.32	91.71	1.98
.55	.05	.6	37.16	67.09	.49
1.8	1	.8	49.76	54.51	.05
.350	-.650	1	51.25	53.02	.01

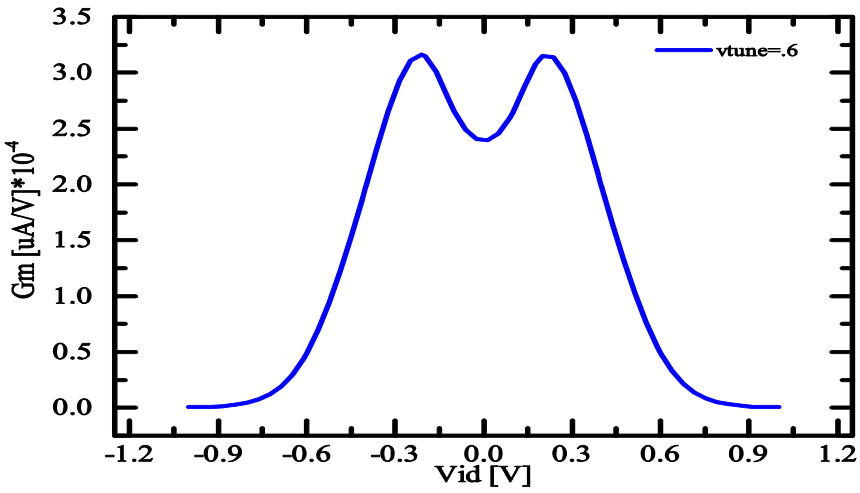

Figure 7.17 Transconductance (G_m) Vs differential signal input (V_{id}) at V_{tune} .6V

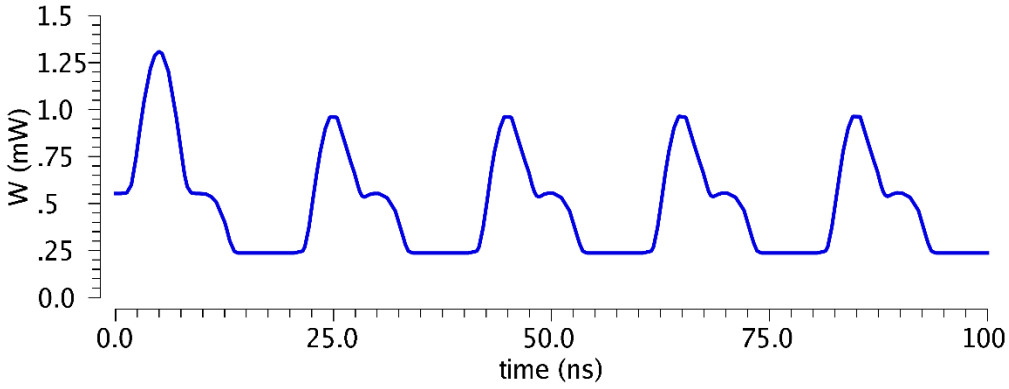

Figure 7.18 Power consumption at V_{tune} .6V

7.3.5 Analysis of Drain Current, Transconductance & Power Consumption for V_{tune} .7V

Circuit parameter is calculated when V_{tune} voltage is fixed at .7V. And the other voltage is variable to generate differential input voltage. For each differential voltage value of I_1 and I_2 is calculated and value of transconductance is calculated. Maximum value of G_m is $4.2(10^{-4}S)$ and minimum value is $1.8(10^{-4}S)$.

Table 7.12 Drain current and Transconductance for V_{tune} .7V

V_1(V)	V_2(V)	V_{id}((V)	I_1(µA)	I_2(µA)	$G_m(10^{-4}S)$
-.08	0.2	-1	52.14	52.12	0.02
-.01	0.7	-.08	77.79	26.43	0.06
-0.2	0.4	-0.6	53.77	50.57	0.5
0.4	0.8	-0.4	85.68	18.49	1.67
0.8	1	-0.2	82.74	21.37	3.0
0.65	0.55	-0.1	39.35	64.90	2.55
0.55	0.65	0.1	64.90	39.50	2.55
1	0.8	0.2	21.37	82.74	3.0
0.8	0.4	0.4	18.49	85.68	1.67
0.4	-0.2	0.6	50.57	53.77	0.5
0.7	-0.1	0.8	26.43	77.79	0.06
0.2	-0.8	1	52.12	52.14	0.02

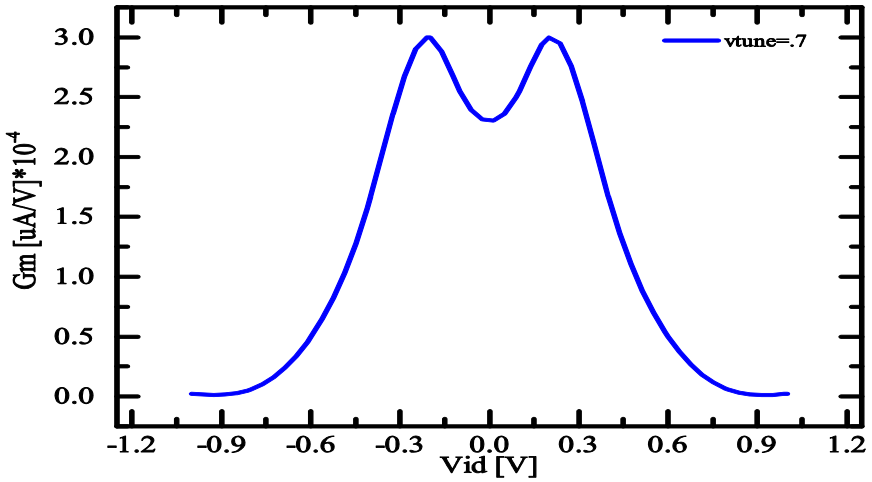

Figure 7.19 Transconductance (G_m) Vs differential signal input (V_{id}) at V_{tune} .7V

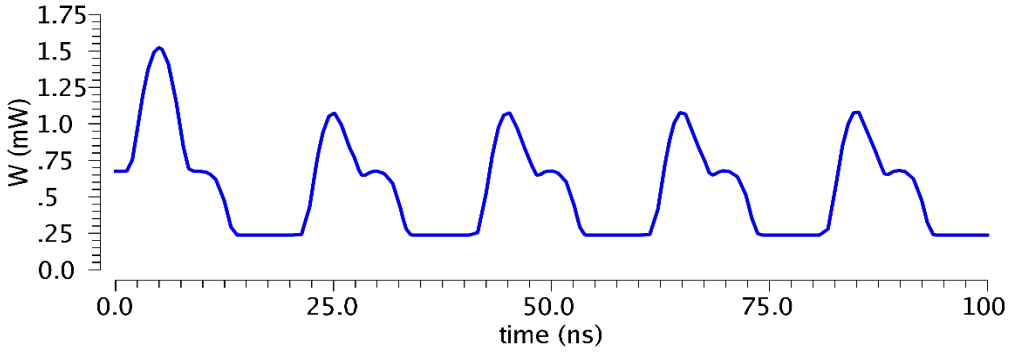

Figure 7.20 Power consumption at V_{tune} .7V

7.3.6 Analysis of Drain Current, Transconductance & Power Consumption for V_{tune} .8V

Circuit parameter is calculated when V_{tune} voltage is fixed at .8V. And the other voltage is variable to generate differential input voltage. For each differential voltage value of I_1 and I_2 is calculated and value of transconductance is calculated. Maximum value of G_m is $4.2(10^{-4}S)$ and minimum value is $1.8(10^{-4}S)$.

Table 7.13 Drain current and Transconductance for V_{tune} .8V

V_1(V)	V_2(V)	V_{id}((V)	I_1(µA)	I_2(µA)	$G_m(10^{-4}S)$
-0.60	0.40	-1.0	53.32	50.94	0.02
-0.25	0.55	-.08	60.60	43.66	0.2
0.60	1.20	-0.6	91.93	12.13	1.33
1.00	1.40	-0.4	91.52	12.51	1.97
0.80	1.00	-0.2	78.40	25.73	2.63
0.75	0.85	-0.1	62.48	41.64	2.0
0.85	0.75	0.1	41.64	62.48	2.0
1.00	0.80	0.2	25.73	78.40	2.63
1.40	1.00	0.4	12.51	91.52	1.97
1.20	0.60	0.6	12.13	91.93	1.33
0.55	-0.25	0.8	43.66	60.60	0.2
0.40	-0.60	1.0	50.94	53.32	0.02

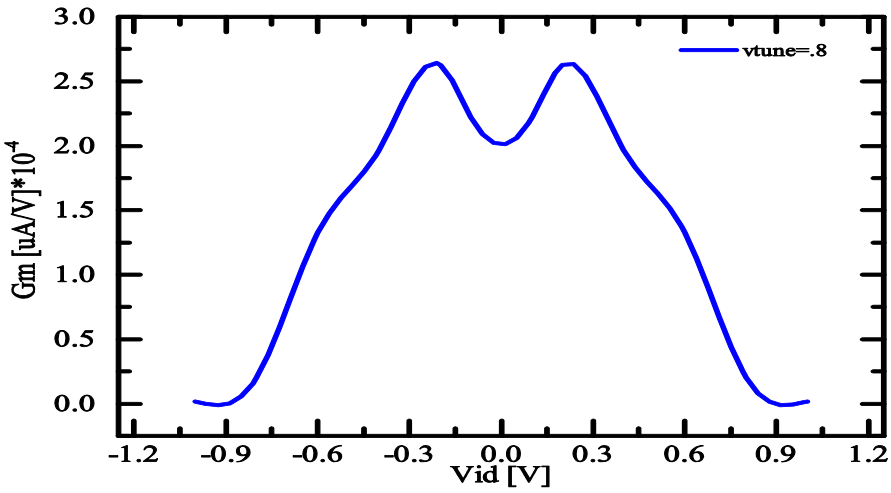

Figure 7.21 Transconductance (G_m) Vs differential signal input (V_{id}) at V_{tune} .8V

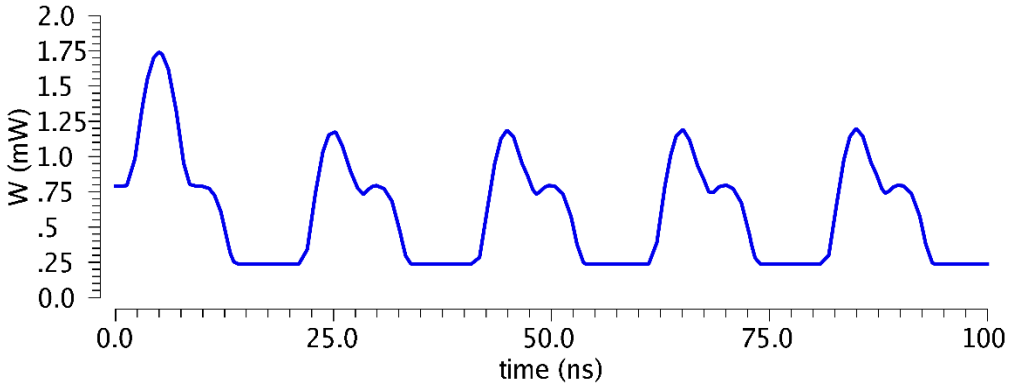

Figure 7.22 Power consumption at V_{tune} .8V

7.3.7 Analysis of Drain Current, Transconductance & Power Consumption for V_{tune} .9V

Circuit parameter is calculated when V_{tune} voltage is fixed at .9V. And the other voltage is variable to generate differential input voltage. For each differential voltage value of I_1 and I_2 is calculated and value of transconductance is calculated. Maximum value of Gm is 4.2(10^{-4}S) and minimum value is 1.8(10^{-4}S).

Table 7.14 Drain current and Transconductance for V_{tune} .9V

V_1(V)	V_2(V)	V_{id}((V)	I_1(µA)	I_2(µA)	G_m(10^{-4}S)
-0.6	0.4	-1.0	53.11	51.16	0.01
-0.1	0.7	-.08	69.98	34.26	0.44
0.6	1.2	-0.6	91.60	12.47	1.33
1.0	1.4	-0.4	91.16	12.87	1.95

0.8	1.0	-0.2	73.65	30.51	2.15
0.85	0.95	-0.1	61.15	42.96	1.81
0.95	0.85	0.1	42.96	61.15	1.81
1.0	0.8	0.2	30.51	73.65	2.15
1.4	1.0	0.4	12.87	91.16	1.95
1.2	0.6	0.6	12.47	91.60	1.33
.7	-0.1	0.8	34.26	69.98	0.44
.4	-0.6	1.0	51.16	53.11	0.01

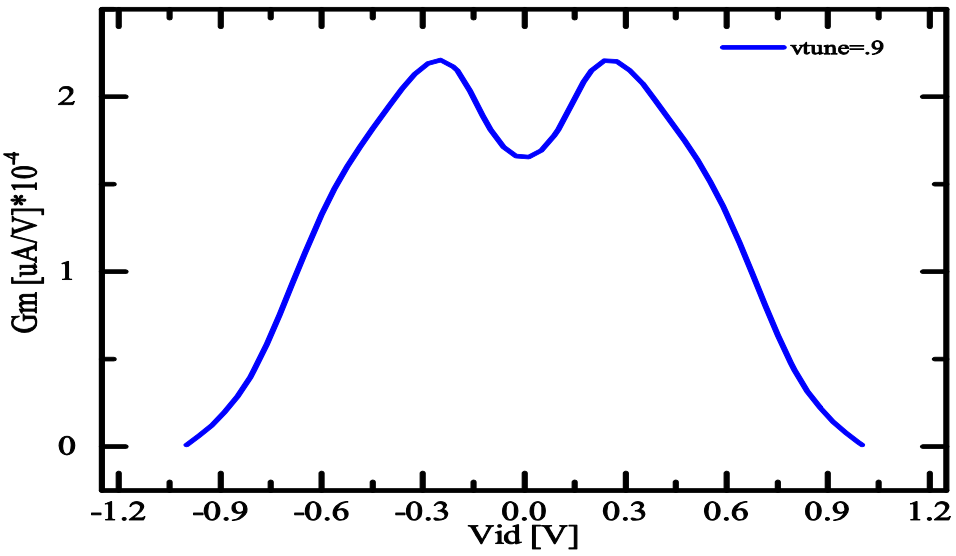

Figure 7.23 Transconductance (G_m) Vs differential signal input (V_{id}) at V_{tune} .9V

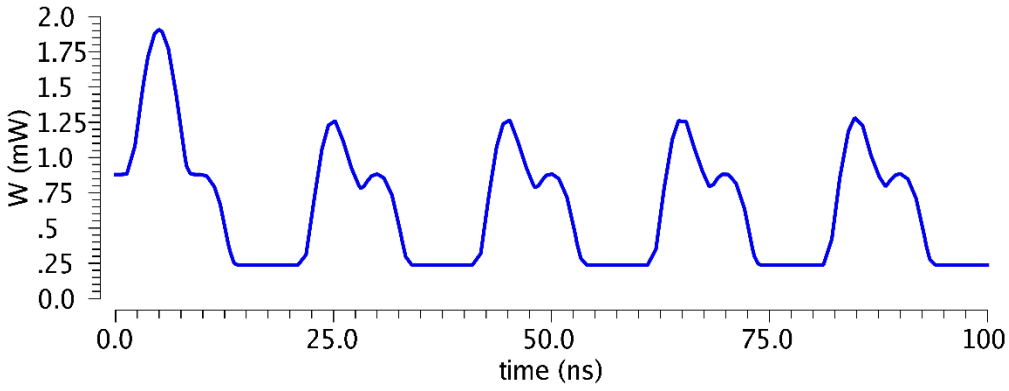

Figure 7.24 Power consumption at V_{tune} .9V

7.3.8 Analysis of Drain Current, Transconductance & Power Consumption for V_{tune} 1V

Circuit parameter is calculated when V_{tune} voltage is fixed at 1V. And the other voltage is variable to generate differential input voltage. For each differential voltage value of I_1 and I_2 is calculated and value of transconductance is calculated. Maximum value of G_m is $4.2(10^{-4}S)$ and minimum value is $1.8(10^{-4}S)$.

Table 7.15 Drain current and Transconductance for V_{tune} 1V

V_1(V)	V_2(V)	V_{id}((V)	I_1(µA)	I_2(µA)	$G_m(10^{-4}S)$
-.05	0.5	-1.0	55.91	30.36	0.25
0.8	1.0	-.08	86.70	17.44	0.8
1.2	1.8	-0.6	91.99	12.02	1.33
0.55	0.95	-0.4	80.87	23.30	1.43
0.8	1.0	-0.2	70.09	34.09	1.8
0.7	0.8	-0.1	58.13	46.11	1.20
0.8	0.7	0.1	46.11	58.13	1.20
1.0	0.8	0.2	34.09	70.09	1.80
0.95	0.55	0.4	23.30	80.87	1.43
1.8	1.2	0.6	12.02	91.99	1.33
1.0	0.8	0.8	17.44	86.70	0.8
0.5	-0.5	1.0	30.36	55.91	0.25

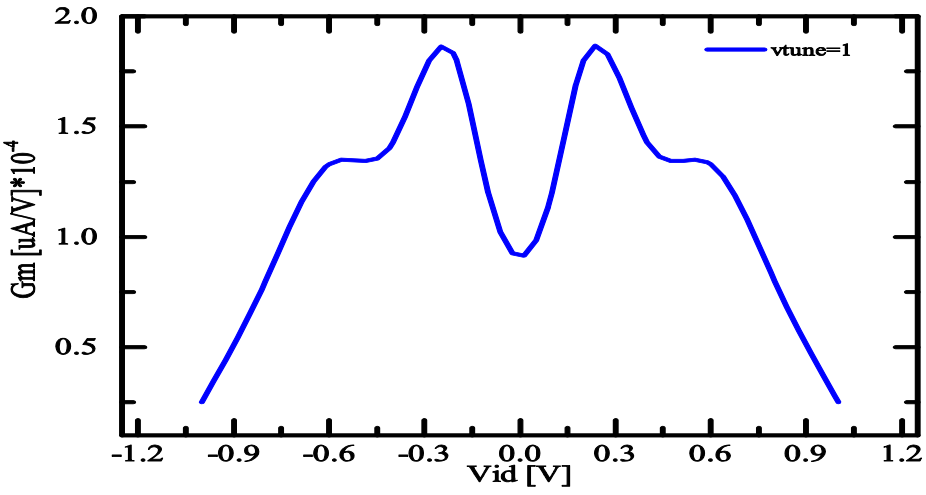

Figure 7.25 Transconductance (G_m) Vs differential signal input (V_{id}) at V_{tune} 1V

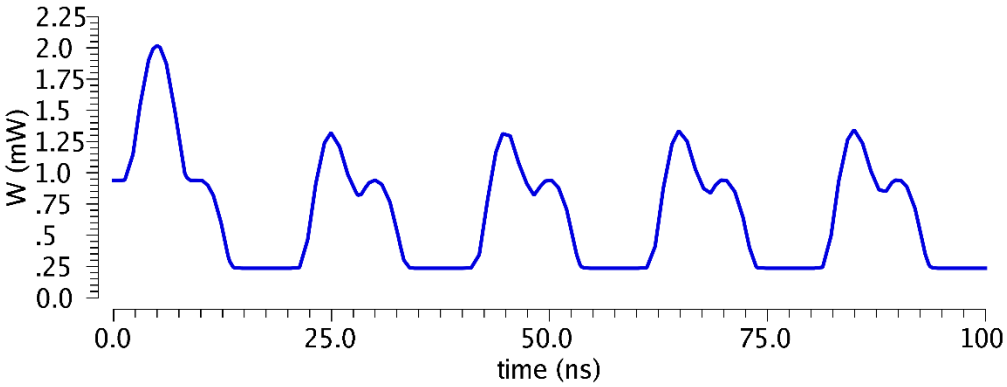

Figure 7.26 Power consumption at V_{tune} 1V

Figure 6.27 shown below gives the complete behavior of the circuit for variable Vtune from .5V to 1V. And show how the transconductance will change, if there is a change in V_{tune} voltage and change in input differential voltage.

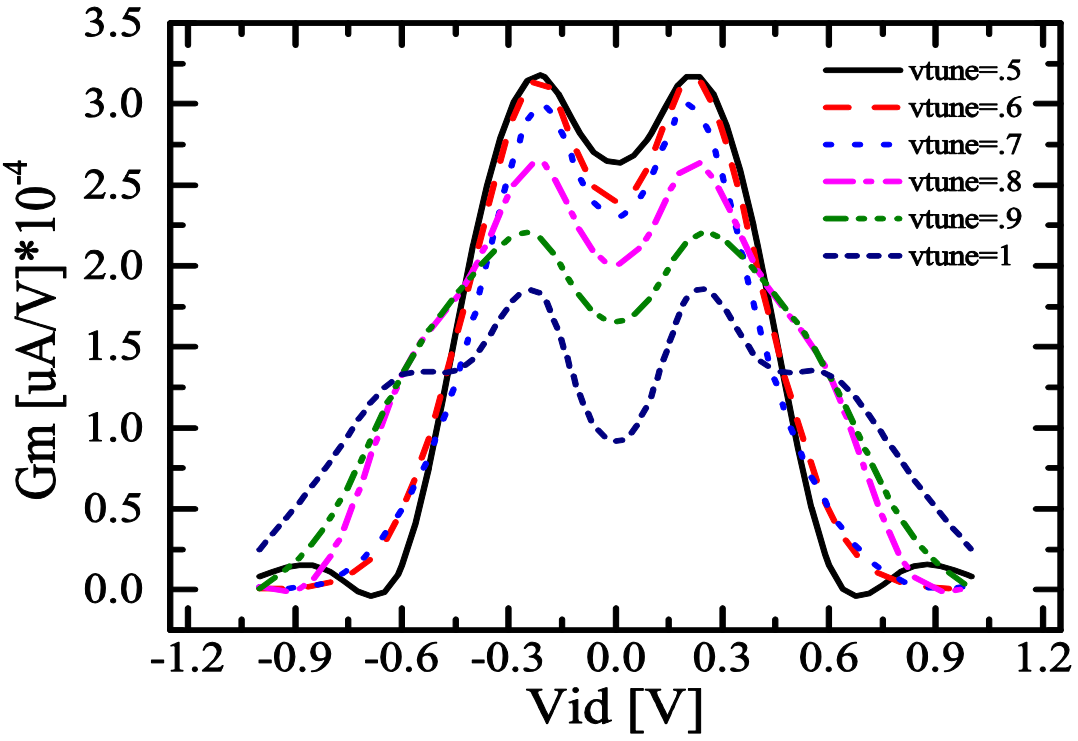

Figure 7.27 Transconductance (G_m) vs differential signal input (V_{id}) at different values of V_{tune}

Figure 6.28 show the relationship between transconductance and tuning voltage for zero input differential voltage. Transconductance value decrease as the tuning voltage magnitude increase.

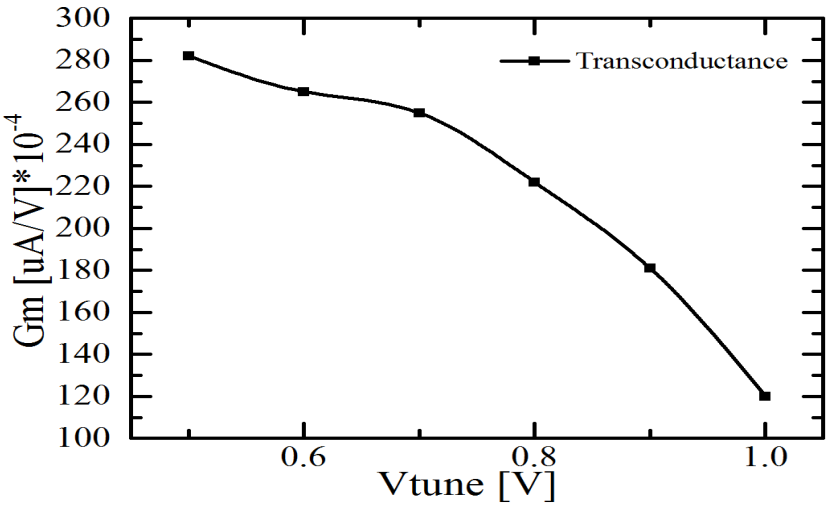

Figure 7.28 Transconductance (G_m) Vs tuning voltage (V_{tune}) at V_{id} = 0V

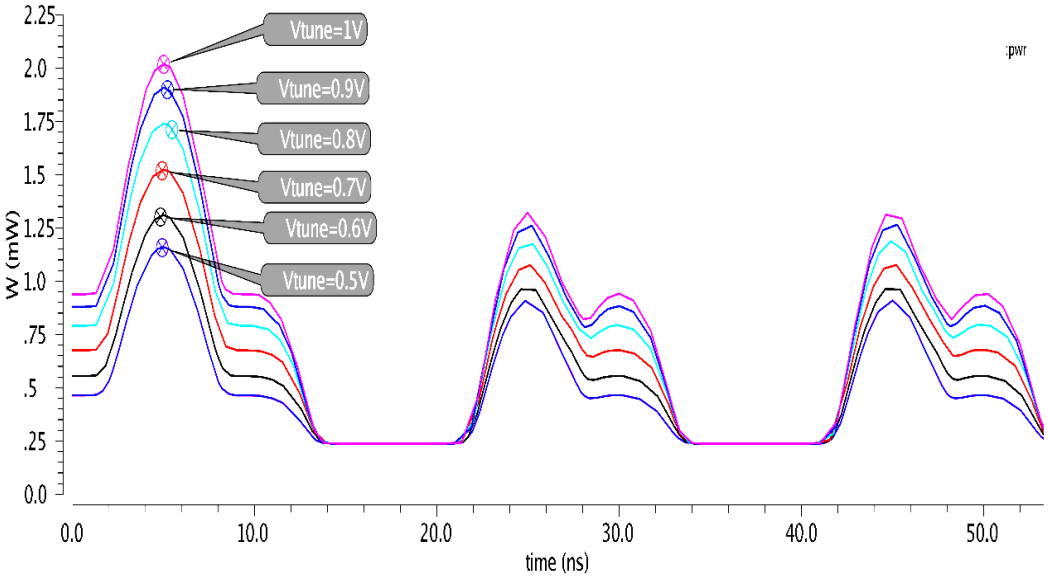

Figure 7.29 Power consumption for different tuning voltage

Chapter 8 RESULTS AND FUTURE SCOPE

RESULTS AND FUTURE SCOPE

The transconductor is simulated in Cadence VIRTUOSO environment using UMC 0.18µm CMOS process technology operated at 1.8V and 27^{o}C. V_{bal}, I_{bias1} and I_{bias2} are kept at 0.8V (greater than V_{th} of N_{M1} and N_{M7}), 92µA and 12µA, respectively. From the circuit analysis we found that the circuit is symmetric because all the transconductance graph is follow even symmetric property. All the value of transconductance for V_1 input and V_2 input is same. Here we plot the magnitude of transconductance with respect to differential input signal. System based on class A inverter amplifier work on 2.2V supply voltage is and it consume 12mW. Circuit is simulated using .35µm CMOS technology. 751µS transconductance is achieved using this configuration. The circuit is simulated in cadence .18µm VIRTUOSO process technology. Bias current I_{bias1} is 240µm and I_{bias2} is 30µm. Vtune is varied from 1.2V to .6V and the step size is 0.1V. Transconductor show tuning within 515µS to 160µS at tuning voltage varied from 1.2V to .6V. The results shown good linearity and tune-ability. The circuit can be used in the design of CMOS continuous time filter. The performance of the circuit can be improved by employing some temperature compensation technique. Although many efficient tuning strategies have been investigated, most of them are not efficient above 100MHz. Also, most of the linearization scheme introduce parasitic poles, reducing their frequency response. It is very challenging for frequencies of around few gigahertz. Mismatches between the input transistors or the mirror transistors causes a DC imbalance between the current, and produces the non-annulations of the even harmonics in the output current, in spite of the differential structure. These effects can be reduced by avoiding minimum-length devices and using common centroid geometry techniques wherever device matching is required.

Techniques	**Supply voltage**	**THD/HD3**	**Process**	**Power consumption**	**Linar range (Vpp)**
MFG MOS	3V	-	.18µm	-	.8V
ARDP	1.8V	-7dB	.18µm	-	1.2V
Mobility Compensation	3.3V	-6dB	35µm	65mW	.8V
Source degeneration Adaptive biasing	3.3V	-	.35µm	1mW	1V
Body effect	.9V	-40dB	.18µm	10mW	100mV
Class A CMOS inverter	2.2V	-70dB	.35µm	12mW	
Tunable high linearity	1.8V	-51dB	.18µm	1.4mW	1Vp-p
Proposed tunable circuit	1.8V		. 18µm	2.1mW	1Vp-p

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