REDUCTION OF SWITCHES IN MULTI-LEVEL INVERTER

DISSERTATION-II

Submitted in partial fulfillment of the
Requirement for the award of the
Degree of

MASTER OF TECHNOLOGY
IN
ELECTRICAL ENGINEERING

By

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MAY 2017

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This is to certify that the Thesis titled **"REDUCTION OF SWITCHES IN MULTI-LEVEL INVERTER"** that is being submitted by **DASARI VENKATA MANIKANTA** is in partial fulfillment of the requirements for the award of MASTER OF TECHNOLOGY DEGREE, is a record of bonafide work done under my /our guidance. The contents of this Thesis, in full or in parts, have neither been taken from any other source nor have been submitted to any other Institute or University for award of any degree or diploma and the same is certified.

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Examiner I **Examiner II**

ACKNOWLEDGEMENT

First and foremost, I am deeply indebted to my mentor **"Mr R.K.SHARMA"** whose inspiration has been unfailingly available to me at all stages of this work. This has fueled my enthusiasm even further and encouraged me to boldly step into what was a totally dark and unexplored expanse before for me. I express my warm thanks to our H.O.S. **Mr. Bhupinder Verma** and my mentor **Mr. R. K. Sharma** for his support and guidance. Moreover, I also want to thank Electrical Department Assistant Professors at Lovely Professional University, special thanks to my senior **B. Prathap Reddy** and my classmate **Gurpreet singh,** all the people who provided me with the facilities being required and conductive conditions for my Dissertation-II.

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This is to certify that **DASARI VENKATA MANIKANTA** bearing Registration no. **11206190** has completed objective formulation of thesis titled, **"REDUCTION OF SWITCHES IN MULTI-LEVEL INVERTER"** under my guidance and supervision. To the best of my knowledge, the present work is the result of her original investigation and study. No part of the thesis has ever been submitted for any other degree at any University.

The thesis is fit for submission and the partial fulfillment of the conditions for the award of Dissertation-II.

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DECLARATION

I, **DASARI VENKATA MANIKANTA**, student of **Masters of Technology** under **School of Electronics and Electrical Engineering** of Lovely Professional University, Punjab, hereby declare that all the information furnished in this thesis report is based on my own intensive research and is genuine.

This thesis does to the best of my knowledge, contain part of my work which has been submitted for the award of my degree either of this university or any other university with proper citation.

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ABSTRACT

The interest in development of newer topologies of multilevel inverter has been increasing rapidly in past few years. Recently introduced topologies achieve higher number of output voltage steps with reduced number of switches, DC voltage sources, voltage stress across switches and losses as compared with the conventional topologies. In this study, a new structure of symmetrical multilevel inverter is enhanced. The enhanced structure offers reduced number of controlled switches, power diodes and DC sources as compared with classical and recently proposed topologies in the literature. Reduction of switch count and DC voltage sources reduces the size, cost, complexity and enhances overall performance. Enhanced topology is capable of producing 7, 9 and 11 levels of output voltage with seven switches only. Moreover, significant reduction in voltage stress across the switches can be achieved. A comparative analysis of enhanced topology with the conventional topology and recently published topologies has been made in terms of controlled switches, power diodes, driver circuit requirement, DC voltage sources and blocking voltage. Multi-carrier pulse-width modulation strategy is adopted for generating the switching pulses. Simulation study of the enhanced topology has been carried out using Mat lab/Simulink.

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LIST OF ABBREVIATION

MLI	Multi-Level Inverter
DCMLI	Diode braced multilevel inverter
CCMLI	Capacitor cinched multilevel inverter
PWM	Pulse Width Modulation Technique
CSI	current source inverter
CHMLI	Cascaded H-Bridge multi-level inverter
SPWM	Single Pulse Width Modulation technique
VSI	Voltage Source Inverter
THD	Total Harmonic Destruction
NPCMI	Neutral-Point-Clamped MLI
VS	Voltage source
DC	Direct Current
IGBT	Insulated-Gate Bipolar Transistor

Chapter 1

Introduction

Research background

Basic idea of Classical inverters

Overview of multilevel inverters

Overview of capacitors

Scope of study

Dissertation objectives

Dissertation outline

1.1 Research Background:

Day by day the demand of high power is increasing for all the industrial applications. Because of this reason many researches are going on from last three decades, and many new structures and new conventional topologies has been proposed. The basic aim of this thesis is improve the quality the output and reduce the number of switching devices and dc sources (Batteries), I was simulated and designed a seventeen level inverter which can produces 17-levels in the output with very less THD and dv/dt ratio. This chapter gives a basic overview of conventional and emerging topologies of multilevel inverters with their operations, limitations, advantages and disadvantages.

In the present situation Multi-level inverters are expanding their advantage on account of the accompanying reasons; high power appraisals, enhanced symphonious execution, quality yield i.e. nearer to sine wave, , and diminished electromagnetic obstruction (EMI) impact i.e. Conceivable with the assistance of different dc-levels that are blend of the yield voltage waveform. Few of the modern applications and electrical engine drives require the high power (i.e. megawatt level) and high voltage level. We can't utilize one semiconductor switch specifically for the level of medium and high range voltages. To determine these issues another idea was presented for high voltage and high power applications i.e. multilevel converters. Presently a days, Multilevel inverters have been used in medium and high power applications, for example, modern engine drives, footing, adaptable AC transmission framework (FACTS), electric vehicle applications, drive frameworks, et cetera.

The primary point of the multilevel inverter is to utilize the power semiconductor switches in arrangement association, keeping in mind the end goal to minimize the voltage weight on every switch and with utilization of less number of dc sources to get yield voltage with all the more no of levels. In multi-level inverters we are utilizing batteries, Capacitors, power devices, and reusable vitality sources as dc sources. The rating of every switch depends on the dc voltage source exhibit in the multilevel inverter.

The multilevel inverters are creating littler regular mode (CM) voltage, in this way minimizing the weight on the engine metal balls. Likewise multilevel inverters having a few downsides alongside the points of interest. The primary disadvantage is to utilize the quantity of semiconductor switches are increasingly and each switch needs singular door drive circuit. Additionally the establishment cost is expanded. These

systems and new topologies are talked about in the writing survey. The real sorts of multi-level inverters are diode-cinched, flying-capacitor sort, H-connect fell sort inverters with various dc sources and P2 multi-level converter. These sorts are unmistakably portrayed in figure 1.1.

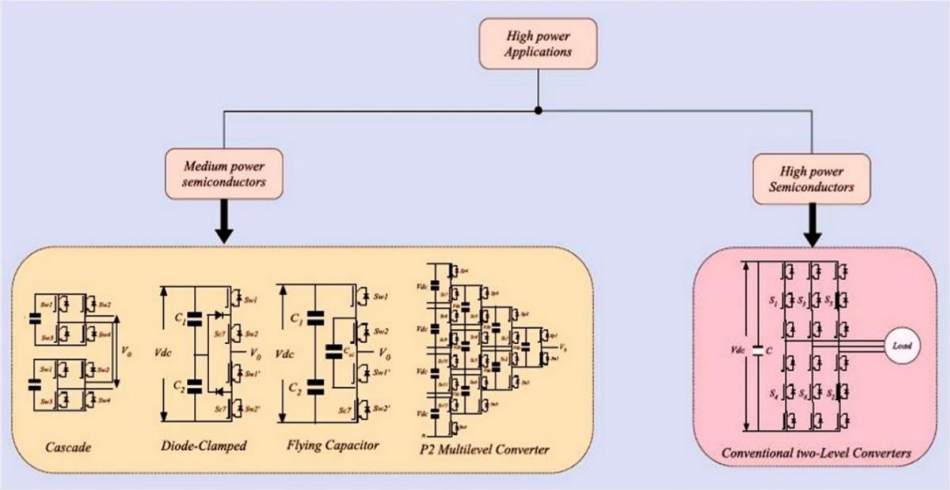


Fig. 1.1 Classic two-level power converters versus most common multilevel power converters

There are many number of regulation procedures and control techniques are presented for multi-level inverters, as are single heartbeat balance, specific consonant disposal, sinusoidal PWM, space vector beat width balance, trapezoidal adjustment, principal recurrence exchanging. These multilevel inverters are utilized as a part of UPSs, ASDs, high voltage transmission, FACTS, VAR compensators and footing reason.

1.2 Basic idea of Classical inverters (Two-level inverters)

Presently a days there is intense rivalry between the utilization of established power converters with high-control semiconductors and proposed converters with medium-control semiconductors. In past, the traditional two-level inverters are just the choice for medium-voltage and high-voltage applications. In any case, in now a days, multi-level converters with medium-control semiconductor gadgets are the opposition for traditional power converters utilizing high-control semiconductor gadgets i.e. which are under constant improvement and are not develop. Despite the fact that, two-level converters are ideal for low-control applications and some medium-control applications, however they are neglected to satisfy the prerequisites of high-voltage and mechanical applications. Established inverters are having taking after disadvantages:

(a) The aggregate DC input voltage showed up over every switch when that is in off position. Because of this reason high appraisals of individual switches required.
(b) Because of the two-level yield voltage enormous minor departure from the heap this can impacts the engine protection.
(c) Snubber circuits are required.
(d) Output of this sort of converters having more symphonious mutilation at exchanging recurrence. Also, the rest of the downside depicted in a table 1.1, which is obviously clarifies the why we are inclining toward multi-level inverters.

Table 1.1 Comparison of classical two level inverters with multilevel inverters

Classic two-level Inverter	**Multi-level Inverter**
Not applicable for high-voltage and medium-voltage applications.	Applicable for high-voltage and medium-voltage applications.
In this high values of switching frequencies are used so that Switching losses are high.	In this low values of frequencies are used so that switching losses are less.
The no. of levels in the output voltage are two, so that THD value is high i.e. 48%.	The no. of levels in the output voltage are high, so that THD value is less. THD value depends on no. of levels in output and type of topology i.e. less than 10%.
Switching stresses across the devices are more.	Switching stresses across the devices are less.
Because of the high dv/dt problem the EMI of the system also high.	But in this very low dv/dt value so that the EMI from the system is very low.
Designing and control of this type is simple	Designing and control of this type is somewhat complex if the no. of will increases.
Cost is less but efficiency also less.	Cost is comparatively high but this give better efficiency.

1.3 Overview of multilevel inverters

The littlest number in multilevel converter topologies is having three voltage levels. As a result of the bi-directional switches, the multilevel converters can work in

both inverter and rectifier modes. When all is said in done multi-level inverters comprises exhibit of force semiconductor gadgets and capacitors (voltage sources), which delivers a yield with more number of steps. The replacement of the power semiconductor switches gives the total of the capacitor-voltages to get high scope of voltages at the yield side, while the power semiconductors need to withstand just decreased voltages. The fundamental prerequisite of multilevel inverters, is to create yield is nearer to sinusoidal wave with low and less voltage push (dv/dt). Another necessity lies in enhancing the power taking care of capacity of force converters. The voltage levels in the yield, is constrained as a result of the voltage-irregularity issues crosswise over capacitors, voltage clasping gadgets, circuit many-sided quality, plan of the controller, capital and support costs.

1.3.1 Concept of multi-level

The essential outline of single stage leg of inverters with a few number of levels, for which the operation of the power semiconductors is spoken to by a perfect switch with various positions appeared in Figure 1.2. The ordinary two-level inverter gives the yield voltage of two levels as per the negative terminal of the capacitor, while the three-level inverter creates three levels of voltages in yield, and the nine-level multi-level inverter gives nine levels in yield which are plainly appeared in the figure 1.2. Consider n is the no. of levels of the yield stage voltage w.r.t the negative terminal of the inverter, then the no. of levels in the yield voltage crosswise over two periods of the heap is

$$m = 2n + 1 \quad \text{---------- (1)}$$

And for a 3-phase load in wye connection, the no. of levels in phase voltage are

$$p = 2m + 1 \quad \text{---------- (2)}$$

1.3.2 Classifications of Multi-level inverters By and large medium voltage range is considered in the power ventures from 2.3 to 6.6 kV and high-control in the scope of 1–100 MW. Presently a days inverters are assumes real part in all high-voltage and medium-voltage drives, FACTS controllers and framework associated frameworks like PV cell and wind vitality frameworks. From the writing overview, we will presume that multi-level inverters are best decision for Medium voltage and high-voltage

applications.

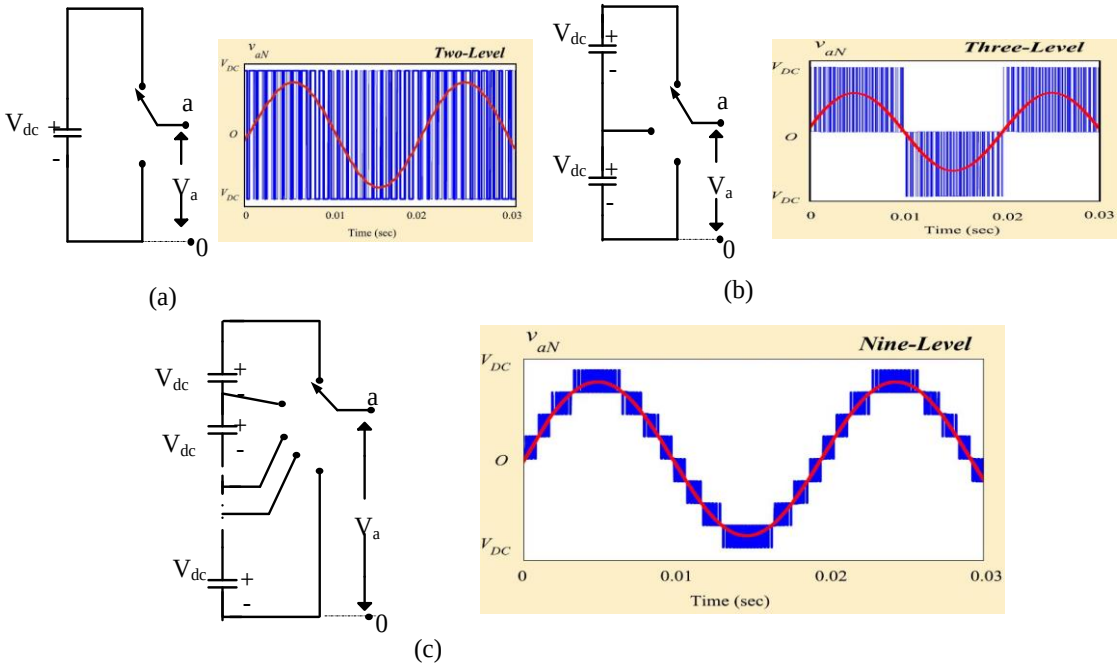


Figure 1.2.Single phase leg of an inverter with (a) two levels, (b) three levels (c) n levels (nine-levels).

The characterization display in figure 1.3 gives the immediate air conditioning to air conditioning converters and current source converters (CSC), which are in a matter of seconds the principle aggressive to multi-level converters; predominantly the heap commutated inverters (LCIs) and cycloconverter are utilized for high-control, high torque, and low speed applications, and the PWM current source inverter (CSI) are utilized for high power and variable-speed drives. Despite the fact that every one of these sorts of converters are capacity to meet high-power and medium-control request, we won't favored as a result of their confinements and downsides i.e. multifaceted nature, size, cost and proficiency.

1.3.3 Conventional types Multi-level inverter topologies

The quantity of levels increments to interminability, the THD of yield scopes to zero. The voltage levels in the yield are restricted in light of the voltage-unevenness issues crosswise over capacitors, voltage cinching gadgets, circuit intricacy and outline of the controller, capital and support costs. Diode braced multilevel inverter (DCMLI) in [1], capacitor cinched multilevel inverter (CCMLI) in [9] and fell H-Bridge multi-level inverter (CHMLI) in [9]-[183 are the three unmistakable fundamental multilevel inverters.

The principal Neutral-point multilevel inverter topology is presented by A. Nabae in 1980 [1]. In 1992 Maynard and Foch are presented the flying capacitor-cinched multilevel inverter topology and the fell H connect topologies were presented in 1990's.

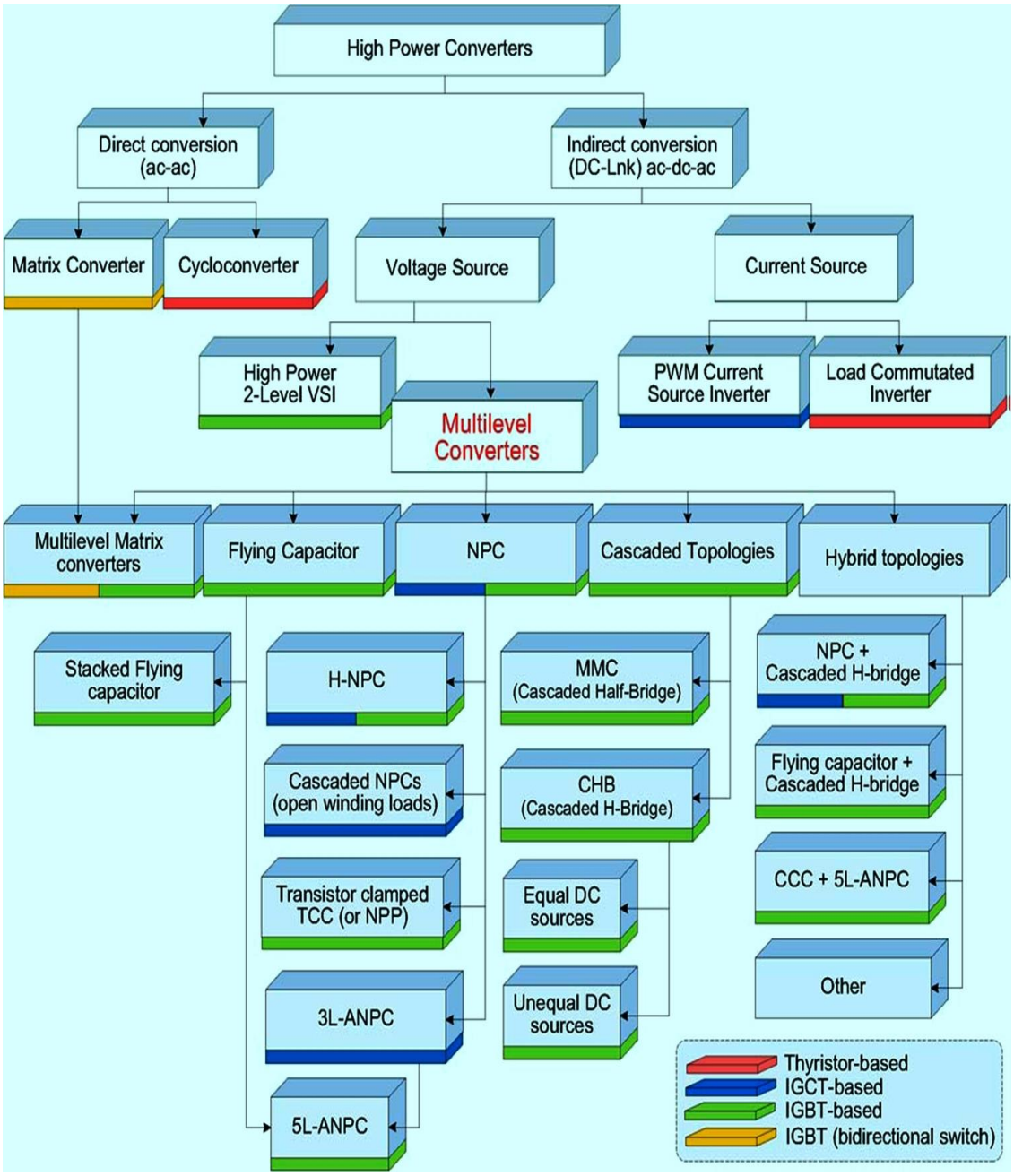


Fig 1.3 Classification of high-power multi-level inverters.

1.3.3. a. Diode-Clamped Multilevel Inverter

Diode clasped sort of inverter is the usually utilizing multilevel topology is the, keeping in mind the end goal to accomplish ventures in the yield voltage the diode is utilizing as the bracing gadget to clip the dc transport voltage. The three-level diode cinched inverter is having two sets of switches, two capacitors and two diodes. The diodes are utilized for giving the mid-point voltage and every switch sets worked in complimentary mode. In three-level inverter the normal dc transport, which is sub separated into the three levels by these combine of two capacitors. The arrangement association of DC capacitors (i.e. C1 and C2) partitions input dc transport voltage into three voltage levels. Every exchanging gadget is having the voltage worry crosswise over of Vdc through the clipping diodes D1 and D2.The aggregate info dc connect voltage is expected as Vdc and mid-point is controlled at half of the information voltage, over the every capacitor voltage is Vdc/2. For the three level diode clipped inverter, i.e. three unique sorts of conceivable states which can apply for the semi square case voltage of yield voltage waveform likewise to info DC connect capacitors voltages. Figure 1.4 portrays the circuit for a diode-cinched inverter for a three level and a five-level inverter.

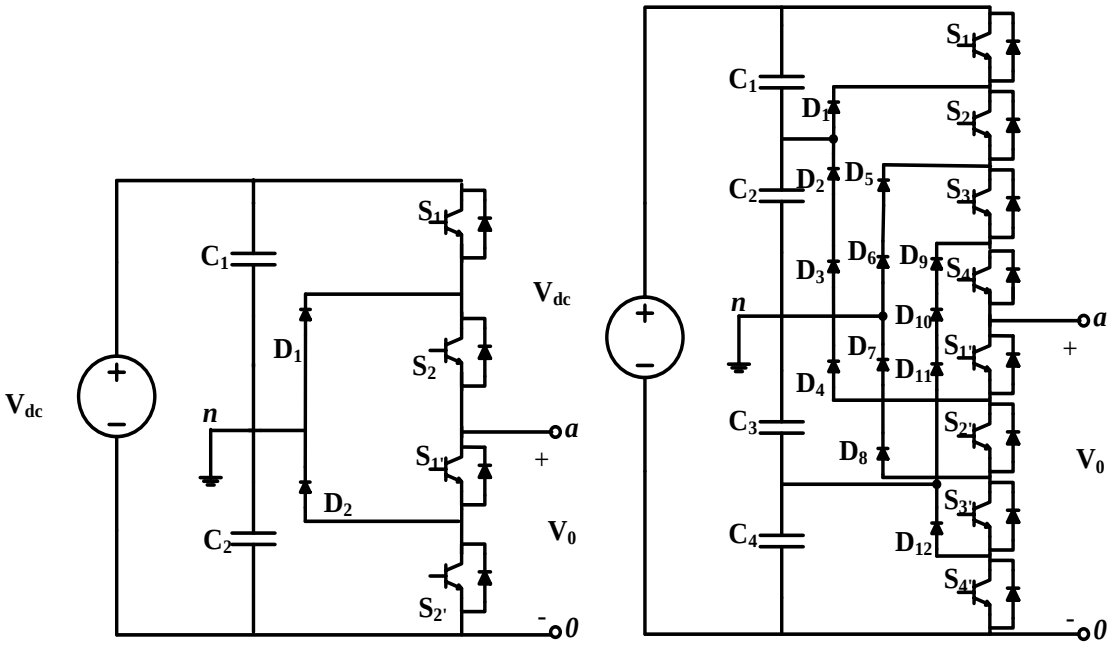


Fig 1.4 .Single leg of Diode-clamped bridge inverter (a) 3-level inverter, (b) 5-level inverter

For the three level diode clipped inverter, whenever two switches are in on position and for the five level diode cinched inverter, whenever there is a gathering of four switches are in position and comparatively for any level of inverter. When all is said in done each leg introduce in P level diode clipped inverter having 2(P-1) exchanging gadgets, (P-1) dc transport capacitors, (P-1) * (P-2) clasping diodes.

By augmenting the no. of voltage levels the way of the yield voltage is upgraded and the voltage waveform ends up being nearer to sinusoidal waveform. Be that as it may, for high voltage level inverters the capacitor voltage adjusting is the significant trouble. Right when P is satisfactorily high, the no. of diodes and the no. of exchanging gadgets will assemble and make the structure (framework) unfeasible to execute. On the off chance that we will utilize sinusoidal PWM for controlling the inverter, the diode switch recuperation of these clasping diodes transforms into the huge design challenge

.i) Operation of DCMLI

Figure 1.4 (a) demonstrates a three-level diode-clamped inverter. Basically three level inverter, where the dc link comprises of two capacitors, C1, C2. For dc-link voltage V_{dc}, the voltage over every capacitor is $V_{dc}/2$ and voltage stress every switching device will be restricted to one capacitor voltage level $V_{dc}/2$ through clamping diodes. To clarify how the stepped wave (stair case) voltage is integrated, the neutral-point n is considered as the common reference point for the output voltage. There are three switching possibilities to integrate three-level voltages over *a* and *0*.

Conducting switches for 3-level operation,

- $V_{a0} = V_{dc}$, S1 and S2.
- $V_{a0} = V_{dc}/2$, S2 and S1′.
- $V_{a0} = 0$, S1’ and S2’ and the remaining switches in the each level are in off state.

Figure 1.4 (b) represents the five-level diode-clamped converter. In which the dc link is having four capacitors i.e. C1, C2, C3, and C4. For dc-bus voltage V_{dc}, the voltage over each capacitor is $V_{dc}/4$ and the stress on each switching device will be constrained to single capacitor voltage level $V_{dc}/4$ through clamping diodes.

Conducting switches for the 5-level operation

- $V_{a0} = V_{dc}$, S1, S2, S3, and S4.
- $V_{a0} = 3V_{dc}/4$, S1’, S2, S3 and S4.
- $V_{a0} = V_{dc}/2$, S3, S4, S1′ and S2′.

- $V_{a0} = V_{dc}/4$, S4, S1′, S2′ and S3′.
- $V_{a0} = 0$, S1′, S2′, S3′ and S4′. And the remaining devices are in off position in every level in above five combinations.

ii) Advantages:

1. Method of Control is simple.
2. Efficiency of this type of inverter is high due to all devices are triggered at fundamental frequency.

iii) Disadvantages:

This structure can be summed up, and the standards utilized as a part of the essential 3-level topology can be stretched out for use in topologies with any number of levels. Nonetheless, for pragmatic this topology has a few specialized difficulties that muddle its application for high power converter applications. i.e.

1. Need of quick recuperation bracing diodes that must be skilled to handle the full load present and high switch recuperation stresses.
2. On the off chance that the no. of levels are expanded, then the expanded voltage stretch equivalent to Vdc (n-1)/n.
3. All the more no. of bracing diodes are required when levels are expanded.

This raises the unpredictability to unwavering quality, outline and cost parameters. Despite the fact that the 3-level diode braced converter works well at high p.f loads, these topologies with more levels are utilized for static VAR remuneration circuits.

1.3.3. b. Flying Capacitor Structure

The structure of this inverter is same as that of the diode braced inverter except for that instead of using clipping diodes, this inverter uses capacitors set up of diodes. The flying capacitor incorporates arrangement plan of capacitor braced trading cells. This topology has a venturing stepping stool structure of dc capacitors, where the voltage on each capacitor fluctuates from that of the accompanying capacitor. The voltage expansion between two adjacent capacitor legs gives the degree of the voltage levels in the yield waveform. Figure 1.4 exhibits the three-level and five-level capacitor cinched inverters independently.

i) Operation of FCMLI

Figure 1.5 represents the central building block of a phase leg flying capacitor inverter. Figure 1.5(a) describes a three-level capacitor-clamped inverter. Basically three level inverter, where the dc link comprises of two capacitors, C1, C2. For dc-link voltage V_{dc}, the voltage over every capacitor is $V_{dc}/2$.

For 3-level operation,

- For the level of voltage $V_{a0}=V_{dc}$, S1 and S2 are ON.
- For the level of voltage $V_{a0}= V_{dc}/2$, the possible two combinations are,
    a. S1 and S1'are ON.
    b. S2 and S2' are ON.
- For the level of voltage Va0= 0, S1' and S2' are ON.

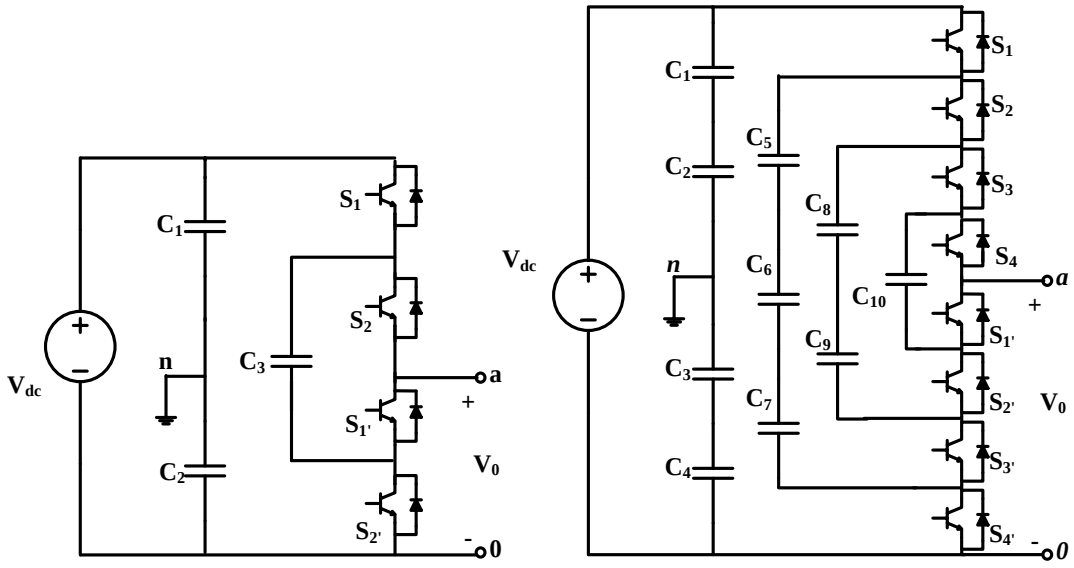


Fig 1.5 Capacitor-clamped multilevel inverter topologies (a) 3-level inverter (b) 5- level inverter.

From the Figure 1.5 (b), the voltage of the five-level flying capacitor phase-leg *a* output according to the reference point 0, V_{a0}, can be determined by these below mentioned switching possibilities.

- For the level of voltage $V_{a0} = V_{dc}$, S1, S2, S3 and S4 are ON.
- For the level of voltage $V_{a0} = 3V_{dc}/4$, the possible four combinations are,
    a) Turn on the devices S1, S2, S3 and S1'.
    b) Turn on the devices S2, S3, S4 and S4'.
    c) Turn on the devices S1, S4, S3 and S3'.

d) Turn on the devices S1, S2, S4 and S2'.

- For the level of voltage $V_{a0}= V_{dc}/2$, the possible six combinations are,
  a) Turn on the devices S1, S2, S2' and S1'.
  b) Turn on the devices S3, S4, S3' and S4'.
  c) Turn on the devices S1, S3, S3' and S1'.
  d) Turn on the devices S1, S4, S2' and S3'.
  e) Turn on the devices S2, S4, S2' and S4'.
  f) Turn on the devices S2, S3, S4' and S1'.
- For the level of voltage $Va0= V_{dc}/4$, the possible four combinations are,
  a) Turn on the devices S1, S1', S2' and S3'.
  b) Turn on the devices S4, S2', S3'and S4'.
  c) Turn on the devices S3, S1', S3' and S4'.
  d) Turn on the devices S2, S1', S2' and S4'.
- For the level of voltage Va0= 0, S1', S2', S3' and S4' are ON.

In general, the capacitors with negative signs are in charging mode, while those with positive sign are in discharging mode. By choosing appropriate combinations of capacitor, it is conceivable to adjust the charge of capacitor (Q). Like as diode-clamped MLI, the capacitor-clamped MLI also needs more no. of high rated capacitors to clamp the dc-link voltage. Given that the voltage rating of every capacitor utilized is the same as that of the fundamental power switch, for n- level flying capacitor converter is requires a sum of (n-1)*(n-2)/2 clamping capacitors for every phase leg also (n-1) primary dc-link capacitors.

ii) Advantages:

1. Clamping diode problems, which are present in the diode clamped multilevel converter are eliminated.

2) Additionally, this type of topology reduces the dv/dt stress across the power semiconductor devices by creating more no. of switching states which are help full for balancing the capacitor voltages.

iii) Disadvantages:

1. The control of this type of inverter is complicated and switching losses are high fo real- power transmission.
2. Excessive no. of capacitors required for when the no. of levels are more.

Also there is a chance, large rms currents will flows in these capacitors. There is a potential for parasitic resonance between decoupling capacitors.

1.3.3. c. Cascaded H-Bridge multilevel inverter

The Cascaded H-Bridge multi-level inverter (CHMLI) has been used in an extensive variety of uses in present days. With its modularity and adaptability, the CHMLI demonstrates prevalence in high power and high voltage applications, particularly series and shunt connected FACTS controllers. The CHMLI gives its output voltage almost sinusoidal output voltage waveforms by joining numerous isolated (disengaged) voltage levels. The dc connection supply for every full bridge converter is given independently, and this is commonly accomplished utilizing diode rectifiers encouraged from the isolated secondary windings of a three-phase transformer.

i) Operation of CMI

The cascaded multi-level converter topology is depends on the series arrangement of single-phase full bridge inverters with more number of dc links. A single phase full bridge (H-bridge) converter is capable to produce 3 different output voltage levels i.e. $+V_{dc}$, 0 and $- V_{dc}$. Each leg present in H-Bridge have two possible conducting states, to avoid dc-link capacitor short-circuit. Figure 1.6 demonstrates the converter circuits for 5-level and 9-level cascaded multi-level inverters. The output phase voltage is analysed by summing of the output voltages of the all bridges. Consider for a 5-level cascaded inverter in which each single-phase full-bridge inverter produces three voltages at the output. There are three switching possibilities to integrate three-level voltages over *a* and *0*.

For the 5-level operation

- $V_{a0}= 2V_{dc}$, S1, S4, S1'and S4' are ON.
- $V_{a0}= V_{dc}$, the two possible combinations are

a) Turn on the devices S1, S4, S1'and S3'.

b) Turn on the devices S1, S3, S1'and S4'.

- $V_{a0} = 0$, the two possible combinations are
    a) Turn on the devices S1, S3, S1'and S3'.
    b) Turn on the devices S2, S4, S2'and S4'.
- $V_{a0}= -V_{dc}$, the two possible combinations are
    a) Turn on the devices S2, S3, S1'and S3'.
    b) Turn on the devices S2', S3', S1 and S3.

- V_{a0}= -2V_{dc}, S2, S3, S2’ and S3’ are ON.

And the remaining switches are in off position in every combination. The staircase output voltage waveform is approximately nearer to sinusoidal, even no need of filter requirement. And figure 2.8 (b) describes the 9-level cascaded H-Bridge MLI, which is formed by either cascading the two 5-level CHMLIs or four single H-Bridges.

ii) Advantages:

• This topology is simple and easy to control.

• The number of capacitors and other semiconductor devices are very less compare to other type of topologies.

iii) Disadvantages:

• It requires separate DC-links or capacitors (batteries) for each module.

• Cost and complexity will increases for high level inverters because of the separate dc sources.

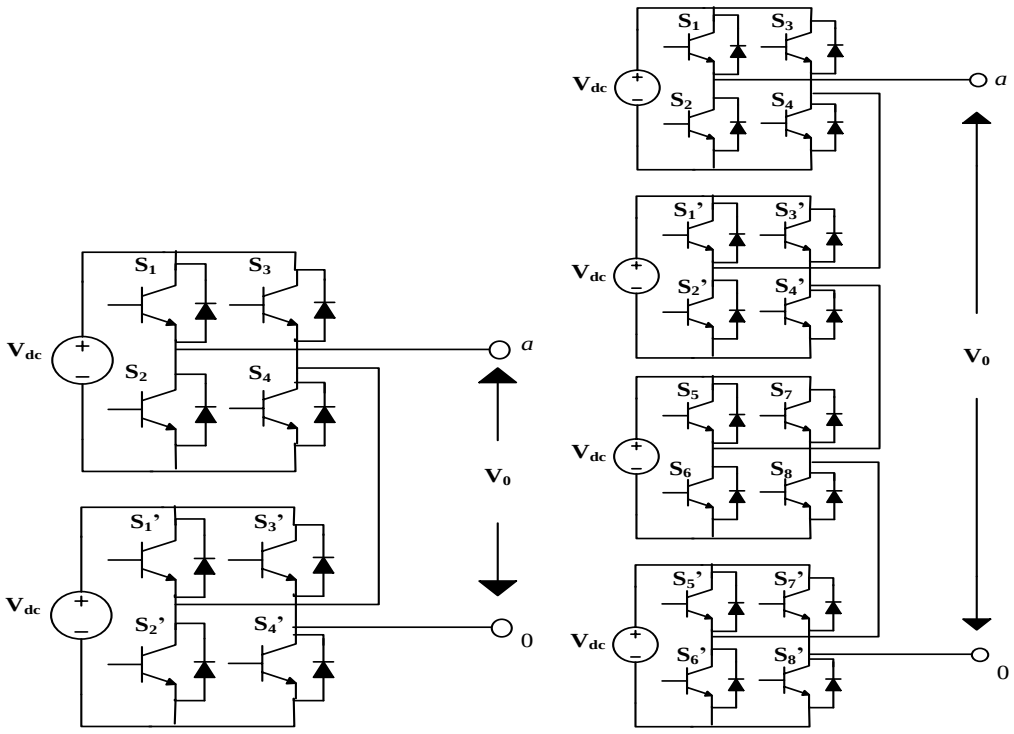


Fig 1.6 Cascaded multi-level topology (a) 5-level (b) 9- level operation

1.3.4. Advantages of multilevel inverters

Now a days, multilevel inverter has numerous merits over a conventional two-level converter that uses high switching frequency pulse width modulation (PWM). The major features of a multilevel converter can be briefly summarized as follows.

1. Staircase waveform quality: Multilevel inverters are generating the output voltages with very low harmonic distortion, and also can minimize the dv/dt stresses; therefore electromagnetic interference (EMI) issues are also minimized.
2. Common-mode (CM) voltage: Multilevel inverters generate smaller CM voltage; due to this reason, the stresses in the bearings of a motor connected to a multilevel motor drive can be minimized.
3. Input current: Multilevel inverters are draws the input current with lower harmonic distortion.
4. Switching frequency: Multilevel inverters are operates at both high switching frequency and fundamental switching frequency.
5. They can be functioned at lower switching frequency.
6. Without increasing power rating of switches we are increasing the number of levels in the output voltage also we can use for high power applications. Multilevel inverters are also having some disadvantages. They require more number of power semiconductor switches. Since we are smaller voltage rating switches can be used in a multilevel converter, each and every switch requires a respective gate driving circuit. This result the whole system will be more complex and costly.

1.3.5. Emerging multilevel inverter topologies:

a) Mixed-Level Hybrid Multilevel Cells –

In high-power and high-voltage application, we can supplant the H-Bridge in a fell multi-level inverter with diode-cinched or capacitor-braced multi-level inverters. The principle go for doing as such is to diminish the quantity of independent dc sources. The 9-level fell H-connect inverter show in figure 1.6 (b) shaped by 4 isolate dc hotspots for one stage leg and 12 requires for a 3-stage inverter. On the off chance that a three-level diode-clipped or capacitor-braced inverter present set up of one H-Bridge, the level in voltage level are multiplied for every module. So that for getting a similar nine levels of voltage for every stage, just two separate dc sources are required for one stage leg and six required for a 3-stage inverter. Figure 1.7 portrays the different developing Topologies of Multilevel Inverters.

b) Asymmetric Hybrid Multilevel Cells –

In the past, the output voltage levels of the cascade inverter cells equal each other. But in this type we will use different voltage levels for different H-bridges of cascaded multilevel inverter, which generates more number of levels with less number of cascaded H-bridges. And the circuit can be known as Asymmetric hybrid multilevel inverter. The topology present in the figure 1.7 we will generate seven levels in the output with two separate dc sources i.e. one with V_{dc}, and the second one with 2 V_{dc}. The advantage of this type of asymmetric hybrid multi-level cells are, which can produces more no. of levels in the output voltage, so that harmonic contents will reduces with less no. of sources and H-Bridge cells .

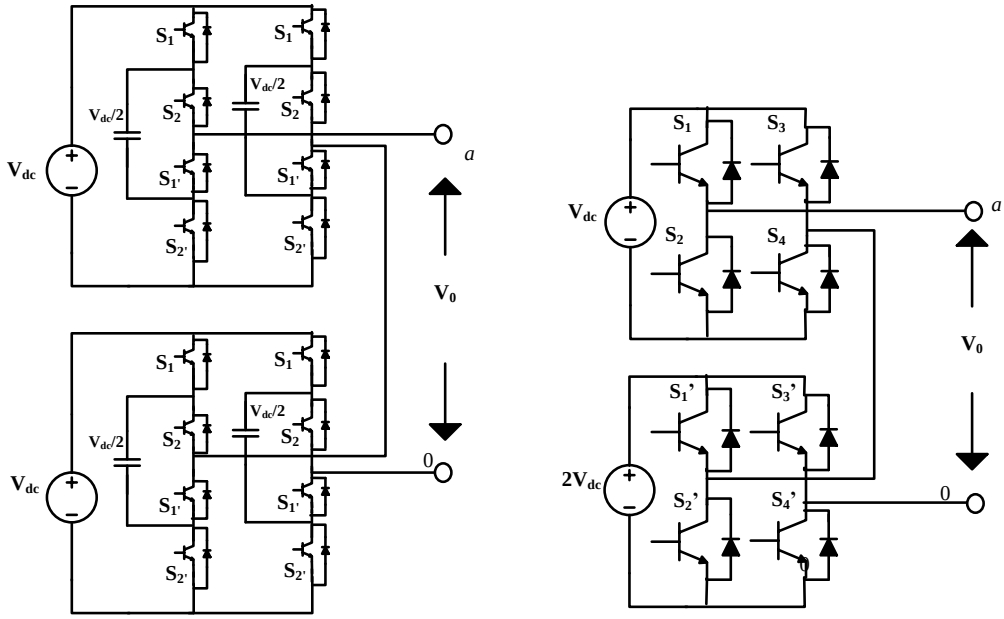


Fig. 1.7 Emerging multi-level inverters: (a) Mixed-level hybrid type, (b) Asymmetrical type

2.8.3. Soft Switched Multilevel Inverters –

The basic use of implementing soft switching techniques are minimize the switching losses, improve the fundamental component of output voltage and improve quality of output for various multi-level inverter topologies. Although zero-current switching (ZCS) is possible, in the previous papers proposed the zero-voltage-switching techniques with auxiliary resonant commutated pole (ARCP), zero-voltage transition (ZVT) with coupled inductor, and their possible combinations.

1.3.6 Applications of multilevel inverters:

Now a day's multi-level converters are the best option for medium-voltage and high-power applications. In general multi-level inverter can be implemented in various manner like DCMLI, FCMLI, or CHMLI, each of them have their advantages,

disadvantages and limitations. Although conventional cascaded H-Bridge multi-level inverter (CHMLI) suffers with separate capacitors (batteries) but the applications of conventional CHMLI's are high. This topology emerges in following applications like and reactive power compensation, STATCOM, traction, LNG plants, electric vehicle drives, renewable energy conversion, UPSs and magnetic resonance imaging etc. The cascaded multi-level inverter (CHMLI) emerging as the best choice, in the liquid natural gas (LNG) plants. In this plants CHMLIs can minimize the maintenance effect in the production cycle, increases the mean time between failures and, at the same time, minimizing the maintenance work period. This can be explains in form of figure 1.8.

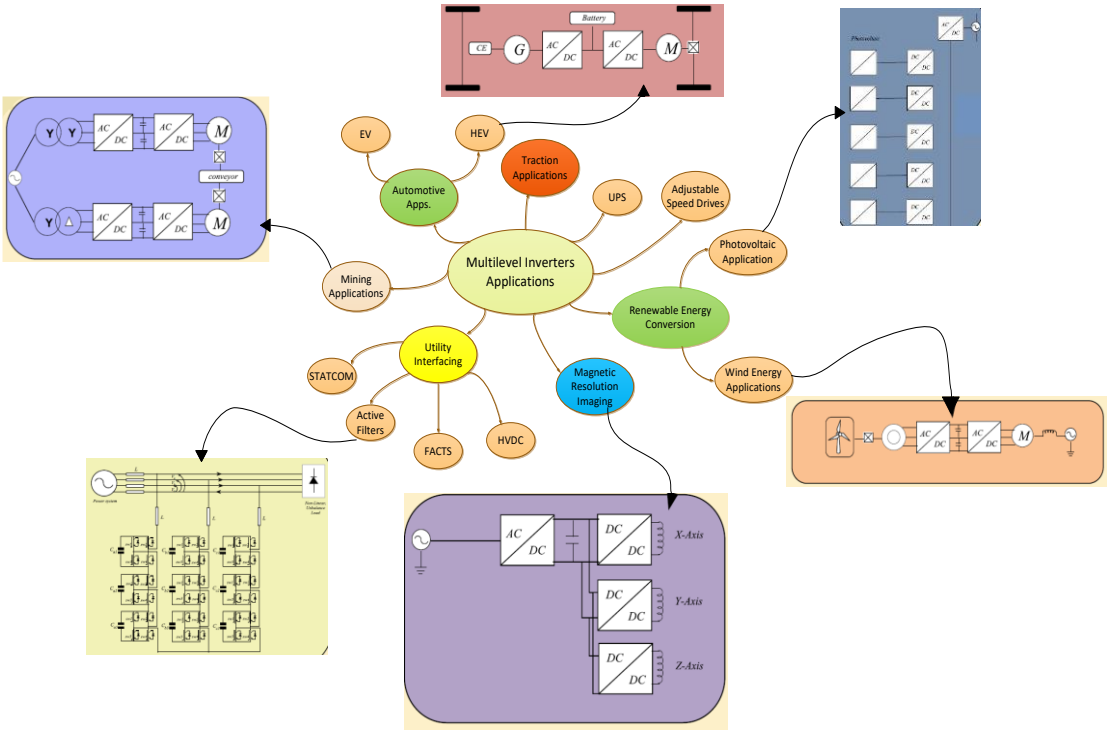


Fig. 1.8 Applications of multilevel inverters

Especially, the DCMLI and FCMLI are used in pumps, fans, and rolling mills, UPSs, electric vehicle drives, HVDC transmission and traction etc. Because of the single source these two types became popular in medium-power applications. And they can't fulfil the demand of high-power due the high switching losses and more number of power semiconductor devices used.

1.4 Scope of study

Multilevel inverters are power electronic systems which produce a suitable AC output voltage waveform from many dc voltages as inputs. Multilevel inverters have several features in comparison with the traditional two-level voltage inverters such as smaller output voltage level, better electromagnetic compatibility, lower harmonic

components and lower switching losses. The conventional full bridge inverter output voltage or streams are of 0 or Vdc voltage. They are named as two-level inverter. Keeping in mind the end goal to acquire a subjective yield voltage and current with lessened measure of swell substance, there is a need of high bearer recurrence alongside various heartbeat width tweak (PWM) methods. However In high-control applications these routine square wave inverters have certain limits like leading misfortunes and gadget evaluations. In cutting edge years, Multilevel inverters have been used in medium and high power applications, for example, adaptable AC transmission framework (FACTS), mechanical engine drives, footing electric vehicle applications, drive frameworks etc.

In this proposition, a novel cross breed multi-level inverter is framed by a three-level flying capacitor inverter and fell H-connect models with drifting capacitors has been displayed, which is producing seventeen levels of yield voltage (shaft voltage). Furthermore, this half and half inverter can produce a more strides of voltage levels with decreased number of switches, door driver circuits and diodes as contrast with customary multilevel inverter. Another element of this inverter is its capacity to create the voltages from a solitary dc-interface control supply which empowers consecutive operation of converter.

The yield voltage waveform is very nearly a sine wave with least symphonious esteem, enhancing the execution of the drive exhibited in this theory as the quantity of voltage levels increments. The work depicted in this postulation produces distinctive voltage levels by exchanging the heap current through capacitors. Here, by taking the excess states for a similar shaft voltage, the bearing of load current through the capacitor can be changed.

Every one of the capacitors introduce in this cross breed inverter circuit can be adjusted at the same time by utilizing one of the post voltage mixes. The proposed inverter with more number of levels can enhance control quality, bring down exchanging misfortunes and deliver top notch voltage waveforms. Also at all heap control variables and adjustment records the proposed strategy can be worked. This topology has low basic mode voltage variety and dv/dt stretch. Additionally this inverter is full for receptive power remuneration.

Extra preferred standpoint of this proposed half breed inverter is if any of the H-spans not worked (i.e. blamed), this inverter can at present be worked with

diminished number of levels of yield at full load. This kind of inverter is for the most part utilized as a part of mechanical engine drives marine impetus and footing.

1.5 Dissertation objectives

The main objectives of my thesis are:

- In this thesis enhanced multi-level inverter, which is formed by a seven semi-conductor switches, ten diodes, capacitors and two dc sources. And that can able to generate the nine levels of output voltage (pole voltage).
- Observe the performance of the enhanced inverter at various modulation index and at all power factor.
- Implement the enhanced inverter work under all critical conditions like if any one of the semi-conductor switch is not functioned (i.e. faulted).
- Implement the three-phase structure for controlling the induction motors and observe the performance at various power factors and various modulation index values.
- Design a proto-type of nine level multi-level inverter and verify the results with various switching techniques.

1.6 Dissertation outline

In this dissertation, in order verify the effectiveness and performance of the cascaded type of hybrid multilevel inverter formed by floating capacitors the following five chapters are proposed:

Chapter 1: Gives the basic idea about multi-level inverters and merits of multi-level inverters over classical two-level inverters are discussed. Further this chapter gives the description of all traditional multi-level inverters and their applications are demonstrated.

Chapter 2: In this chapter literature reviews are discussed. This chapter gives basic overview all conventional topologies and their merits, demerits and control techniques. Main aim of this contribution is identify the problems in the traditional converter topologies.

Chapter 3: This chapter discusses the operation of enhanced multi-level inverter and with their switching states for nine level output with its simulation results.

Chapter 4: This chapter gives the all simulation results of implemented nine level inverter topology.

Chapter 2

Literature reviews

Introduction

Overview of previous papers

Summary

2.1 Research motivation

At present there is extreme rivalry between the utilization of high voltage semiconductors in exemplary power converter topologies and new converter topologies utilizing medium voltage gadgets. Presently a days, industry has started to request higher power hardware, which now achieves the megawatt level. Controlled air conditioning drives in the megawatt range are normally associated with the medium-voltage organize. Today, it is difficult to associate a solitary power semiconductor change specifically to medium voltage networks (2.3, 3.3, 4.16, or 6.9 kV). Thus, I was intrigued to do my proposal on this multilevel inverters.

2.2 overview of previous papers

I was concentrated numerous diaries and gathering papers, articles identified with my point and few of those papers are underneath.

Akira Nabae, Isao Takahashi, and Hirofumi Akagi (1981)

The Basic idea of multilevel inverter was initially presented by Nabae [1]. In this paper another unbiased point-clasped (NPC-PWM) inverter created by utilizing beat width adjustment (PWM) method. This inverter yield having less consonant substance as contrasted and the routine inverters. Here components of every single ordinary inverter are researched tentatively and diagnostically. This NPC-PWM inverter is enhances the proficiency of drive framework, including engine effectiveness, and it is ideal for an extensive variety of variable-speed drive frameworks. This paper likewise gives the similar investigation of every single customary inverter, including two level inverters, and a few constraints and issue additionally discussed.In option, this inverter is best for an air conditioner engine drive framework.

Ronald Marusarz (1989)

In this papers creators proposed another idea of exchanged capacitor multilevel inverter without inductors or transformers in [2]. Creators are presented another topology for delivering the low-consonant, 60 Hz recurrence. They displayed another inverter, which gives the sinusoidal 110 V, AC yield from a 24 Vdc source. The new circuit structure permits a similar power MOSFETS which consecutively charge a bank of capacitors to likewise integrate the stair-case sine wave estimation. They introduces the Fourier examination of the impacts of force MOSFET on state resistance and exchanging day and age upon a 1 KW demonstrate.

Varsha Singh,Raipur Raipur,S Gupta, et al.[5] Implemented a Hybrid cascade multilevel inverter (HCMLI)for increasing power quality of MLI by less number of switches and sources. In MLI power quality increased by increasing number of level in output wave form. But, in MLI levels are increased then semiconductor devices, DC sources, cost and complexity increased. HCMLI is overcomes the above problems. HCMLI is combination of module (positive voltage levels) and H-bridge (negative and zero voltage levels).

Young-Seok Kim, Beom-Seok Seo, et al. [6] clarified a dynamic exchanging attributes of every power semiconductor gadgets and a few issues of MLI like voltage unbalance between DC-interface capacitors and over voltages over the exchanging gadgets. The above specify issues taken and they proposed another MLI with PWM inverter. They demonstrates the investigation of new three level inverter.

Nashiren Farzilah Mailah, Sh. Sakinah Tuan Othman, et al. [7] clarified that THD (Total Harmonic Distortion) was diminished by expanding voltage level in yield wave. For clarification they done five level Neutral-Point-Clamped MLI MATLAB reenactment plan and three level NPCMI MATLAB outline and looked at both THD values.

Nakul Thombre, Ratika Singh Rawat, et al. [8] proposed an outline of 21 level fell cost proficiency inverter with less switches and dc hotspots for decreasing semiconductor switches and dc sources.

S. Lai and F.Z. Peng, et al. [9] Established two-level converters are ideal for low-control applications and some medium-control applications, yet they are neglected to satisfy the necessities of high-voltage and modern applications. In light of this reason Multi-level converters are developing as another choice of force converter alternatives for high-control applications. The creators in [9] given an essential thought of multilevel inverters into diode cinched multilevel inverter, flying capacitor multilevel inverter and fell H-connect inverter and their working rule, components, impediments and applications . In this paper the creators are disclosed the methods to comprehend the voltage awkwardness between various levels introduce in both diode-cinched and capacitor braced converters. Utilizing static VAR generator as an application creator infers that each of the three setups of multilevel inverters can be connected without issue of voltage unbalancing between the levels.

J. Rodriguez', J. Pontt2, S.Kouro, et al. [10] presents the use of Direct Torque Control in an acceptance engine, utilizing a multilevel fell inverter with isolated DC sources. The control technique works with forced exchanging recurrence, enhancing torque conduct. The paper concentrates the hypothetical ideas identified with this technique, similar to vector determination, state factors estimation and compensation time count. What's more, this work presents comes about for a 3 and 11-level inverter nourished drive, from which it can be valued that the expansion of levels of the heap voltage decreases the torque swell.

K.Gobinath, S.Mahendran, et al. [11] executed the Selective Harmonic Elimination Stepped Waveform technique and plan MLI with less number of switches. By utilizing SHESW strategy take out the lower arrange sounds. Utilizing MATLAB recreation comes about THD esteem contrasted and standard THD esteem.

Poh Chiang Loh, Donald Grahame Holmes, et al. [12] Multilevel inverter that produce more than two levels of voltage to get the yield nearer to sine wave and less twisted air conditioning to dc, dc to air conditioning, and dc to dc control transformation, have pulled in numerous patrons. In paper [12] Peng and Fang Zheng are proposed a summed up model of multi-level converter with self-voltage adjusting. From this summed up inverter topology we can infer the customary unbiased point diode clipped and flying capacitor multilevel inverters. Likewise this summed up multi-level converter topology gives another multilevel structure that can control the every dc-voltage level naturally with no help from other converter structures circuits. Numerous new multilevel converter topologies can be gets from this proposed summed up multilevel inverter structure. Additionally some application cases of the summed up multilevel converter are likewise introduced in this paper

Gopal Mondal, K. Gopakumar, et al. [13] The energy here is in using a single DC power source to build up a three stage five-level fell multilevel inverter to be used as a drive for a Permanent magnet footing engine. In [13] the five-level inverter involves a standard three-leg inverter (one leg for each stage) and a H-Bridge in game plan with each inverter leg, which use a capacitor as a DC source. It is exhibited that one can in the meantime keep up the direction of the capacitor voltage while creating an Output voltage waveform which is 25% more than that delivered using a standard three-leg inverter independent from anyone else.

Mariusz Malinowski, K. Gopakumar, et al. [14] At this moment, multilevel inverters have transformed into a create advancement and are in all cases found in medium-voltage moreover, high-control mechanical methodology. From the most recent three decades multi-level inverters are expanding their advantage due to the accompanying reasons; high power appraisals, enhanced consonant execution, quality yield i.e. nearer to sine wave, and lessened electromagnetic obstruction (EMI) impact i.e. Conceivable with the assistance of various dc-levels that are combination of the yield voltage waveform. The point of [14] is to gathering and audit these late topologies of multilevel inverters. This is the primary paper gives a brief thought of settled multi-level inverters emphatically situated to their present state in modern applications. Likewise they examined about the rising structures of multilevel inverters.

Saketh Dogga, Sumanth Kumar A.V, et al. [15] demonstrates that number of yield voltage expanded then THD values diminished. The correlation was appeared in this paper with seven-level inverter. Outline nine level inverter with just six switches and less DC-sources. Connected PWM strategy on 9-level single stage inverter. The outcome was appeared in MATLAB recreation

José Rodríguez, Jih-Sheng Lai, et al. [16] state that different topologies of MLI, sinusoidal pulse width module technique, space vector modelling technique, applications of MLI and every topology of inverter.

Ebrahim Babaei, et al. [17] obtained 53-level single phase inverter using 22 IGBT"s, and standing voltage of 500.5V and 24 IGBT"s using 49-level inverter with standing voltage of 1007.2V.

Youhei Hinago, and Hirotaka Koizumi, et al. [18] It comprises of a H-connect and an inverter which yields multilevel voltage by exchanging the dc voltage sources in arrangement and in parallel. The proposed inverter can yield more quantities of voltage levels in a similar number of exchanging gadgets by utilizing this transformation. The quantity of door driving circuits is decreased, which prompts to the diminishment of the size and power utilization in the driving circuits. The aggregate consonant of the yield waveform is additionally lessened. The proposed inverter is driven by the half breed regulation strategy. In this paper, the circuit arrangement, hypothetical operation, Fourier investigation, reproduction comes about with MATLAB/SIMULINK, and test results are appeared.

Pablo Lezana, José Rodríguez, and Diego A. et al. [19] Multilevel converters are an extremely intriguing option for medium and high power drives. One of the more

adaptable topologies of this sort is the fell multicell converter. This paper proposes the utilization of a solitary stage diminished cell appropriate for fell multilevel converters. This cell utilizes a diminished singlephase dynamic rectifier at the info and a H-connect inverter at the yield side. This topology introduces a decent execution, viably controlling the waveform of the information current and of the yield voltage and permitting operation in the motoring and regenerative mode. The outcomes displayed in this paper affirm that this medium voltage inverter viably wipes out low recurrence input current sounds at the essential side of the transformer and works without issues in regenerative mode.

Prof. Dr. P. K. Sataya Moorthy , et al. [20] Inspected topology of fell multilevel inverter utilizing a decreased number of switches is proposed. The new topology has the benefit of diminished number gadgets contrasted with customary setups and can be reached out to any number of levels. This topology brings about lessening of establishment zone, cost, computational time and has effortlessness of control framework. This structure comprises of arrangement associated submultilevel inverter squares. The GA procedure finds the ideal arrangement set of exchanging edges.

Divya Subramanian, Rebiya Rasheed, et al. [21] executed a nine level inverter utilizing 8 switches, 4 dc sources and 8 diodes and demonstrates the resultant wave in MATLAB reproduction configuration yield.

Varsha Sahu, Shraddha Kaushik, et al. [22] outline a model for new five level diode braced multi-level inverter with less number of switches and diodes. In these sort converters, each of the data sources and yields can single-stage air conditioning, or multiphase air conditioning; dc, that is the reason, they are valuable in dc to dc, dc to air conditioning, air conditioning to dc, or air conditioning to air conditioning power transformation frameworks. The fractional full converters (delicate exchanging air conditioning join widespread power converters) are solid, minimized, and longer lifetime as contrast with other customary converters. In any case, traditional converters needs more number of switches, which is unpredictable to control. This paper proposed a novel altered approach, which can additionally minimizes the no. of switches without changing the working standard. This proposed converter, which is called as ultrasparse air conditioning join buck–boost converter, minimizes the no. of changes from 24 to 16, in a 3-stage air conditioning to air conditioning case, and diminishes the no. of changes from 20 to 10, in a dc to 3-stage air conditioning structure. This ultrasparse

converters are adoptable to frameworks with unidirectional stream of current and power, i.e. photograph voltaic cells (PV cells) and wind control era frameworks.

2.3 Summary

From the above exchange, I was watched the accompanying issues like diode cinched and flying capacitor multilevel inverters are having more number of exchanging gadgets, diodes additionally more capacitors. Also, these two inverters experiences the voltage unbalancing of capacitors and rating of the gadgets. Most ideal sort of multilevel inverter is fell sort, since it has less no of exchanging gadgets furthermore less number of capacitors and diodes.

Real trouble of this fell inverter is need of various dc sources. My point is to produce the more number of levels with less number of switches and dc sources. That is the reason I was actualized a proto kind of fell 17-level exchanged capacitor inverter, which creates the seventeen levels by utilizing two sources, sixteen switches and six capacitors. After that i propose another seven level single stage crossover inverter, which produces the seventeen levels (shaft voltage) from a solitary dc source.

Chapter 3

Enhanced Multi-level Inverter Topology
(9 Level & 11 Level H-Bridge)

Enhanced H-Bridge Inverter

Summary

3. 1 Enhanced H-Bridge Inverter:

3.1.1 Introduction

In this thesis Multi-level inverter has been enhanced, which is formed by a seven semi-conductor switches, ten diodes, capacitors and two dc sources. Which is generating nine levels and 11 level of output voltage (pole voltage) from a two dc power supply. And this inverter can generate a more steps of voltage levels with reduced number of switches, gate driver circuits and diodes as compare to conventional multilevel inverter. The enhanced inverter with more number of levels can improve power quality, lower switching losses and produce high quality voltage waveforms.

3.1.2 Power circuit topology

The basic structure of enhanced inverter is shown figure 3.1. Two dc voltage sources (VS1 and VS2) along with two capacitors C1 and C2. The voltages of capacitors C1 and C2 are maintained at a voltage level of $V_{dc}/2$ and $V_{dc}/2$ respectively. This enhanced topology consists of seven semi-conductor switches S1, S2, S3, S4, S5, S6 and S7. S7 works as four quadrant switch along with four diodes D7, D8, D9 and D10.

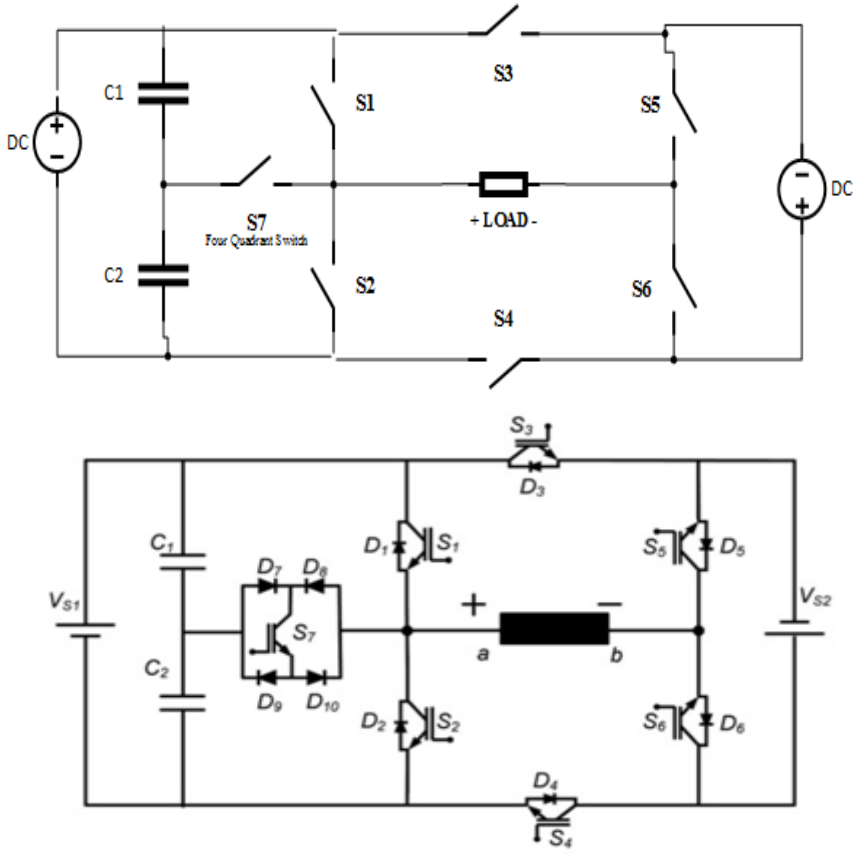


Fig. 3.1 Basic structure of enhanced multi-level inverter

When the two DC sources i.e.VS1 and VS2 are equal then it considered as symmetrical multi-level inverter otherwise asymmetrical multi-level inverter. By maintain voltage levels of the DC sources (VS1 and VS2) we can maintain output voltage levels. When VS1 and VS2 DC voltage sources are equal then output voltage can be nine levels, VS1= (2/3)*VS2 then output voltage will be 11 level.

Table 3.1. Various switching combinations with conducting diodes

S. No.	Output voltage levels	ON state switches	Conducting Diodes
1	1	S_4, S_7	D_6, D_7, D_{10}
2	2	S_4, S_5	D_2
3	3	S_4, S_5, S_7	D_7, D_{10}
4	4	S_1, S_4, S_5	-
5	0	S_1, S_3, S_5	-
6	-1	S_3, S_7	D_5, D_8, D_9
7	-2	S_3, S_6	D_7
8	-3	S_3, S_6, S_7	D_8, D_9
9	-4	S_2, S_3, S_6	-

Table 3.2. Output voltage levels if VS1=VS2=2V

S.No.	Voltage levels	If VS1=VS2=2V	Output voltage
1	**2V**	**2*2**	**4V**
2	**3V/2**	**(3*2)/2 = 6/2**	**3V**
3	**V**	**2**	**2V**
4	**V/2**	**2/2**	**1V**
5	**0**	**0**	**0**
6	**-V/2**	**-2/2**	**-1V**
7	**-V**	**-2**	**-2V**
8	**-3V/2**	**-(3*2)/2 = 6/2**	**-3V**
9	**-2V**	**-2*2**	**-4V**

The steps to synthesize the output voltage levels of 9level H-bridge inverter are as follows:

a) For V_0 = 1V level output:

The output voltage V_o = 1V is possible by two switching combinations, which are clearly mentioned in the Table 3.1. These two switching states are required for balancing the capacitor C_2 and its voltage to a prescribed value of 1V. S_4, S_7 switches are 'ON' and D_7, D_{10} are conducting.

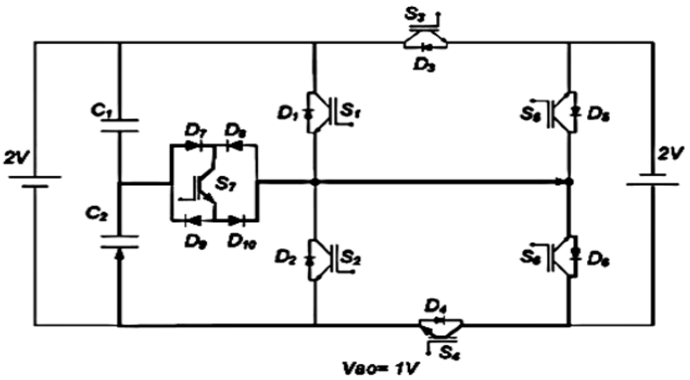


Fig. 3.2 switching combinations for the voltage of V_o = 1V

b) For V_0 = 2V level output:

The output voltage V_o = 2V is possible by two switching combinations, which are clearly mentioned in the Table 3.1. These two switching states are required for balancing the capacitors and its voltage to a prescribed value of 2V. S_4, S_5 switches are 'ON' and diode D_2 is conducting.

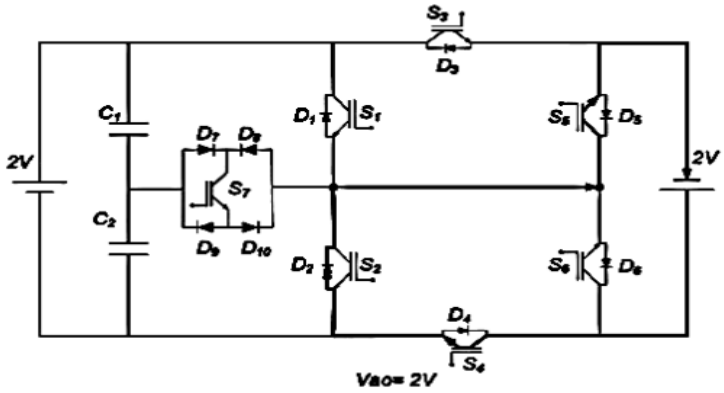


Fig. 3.3 switching combinations for the voltage of V_o = 2V

c) For V_0 = 3V level output:

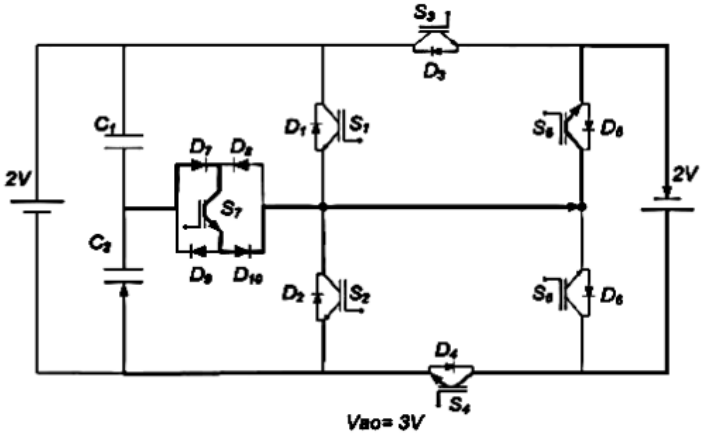


Fig. 3.4 switching combinations for the voltage of V_o = 3V

The output voltage V_o = 3V is possible by three switching combinations, which are clearly mentioned in the Table 3.1. These three switching states are required for balancing the capacitors and its voltage to a prescribed value of 3V. S_4, S_7, S_5 switches are 'ON' and D_7, D_{10} are conducting.

d) For V_0 = 4V level output:

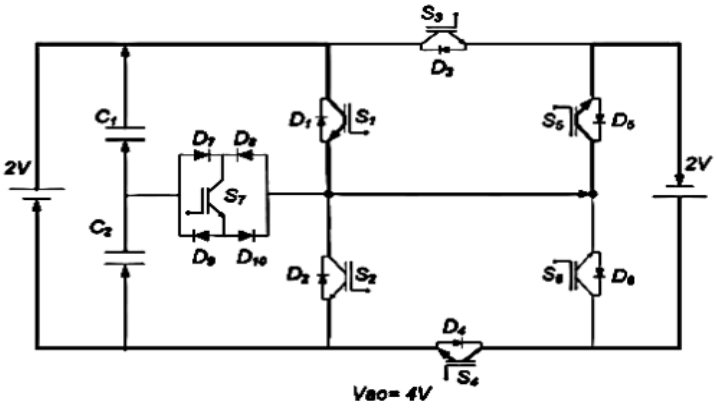


Fig. 3.5 switching combinations for the voltage of V_o = 4V

The output voltage V_o = 4V is possible by three switching combinations, which are clearly mentioned in the Table 3.1. These three switching states are required for balancing the capacitors and its voltage to a prescribed value of 4V. Switches S_1, S_4, S_5 are 'ON'

e) For V_0 = -1V level output:

The output voltage V_o = -1V is possible by two switching combinations, which are clearly mentioned in the Table 3.1. These two switching states are required for balancing the capacitors and its voltage to a prescribed value of -1V.Switches S_3, S_7 are 'ON' and D_5, D_8, D_9 are conducting.

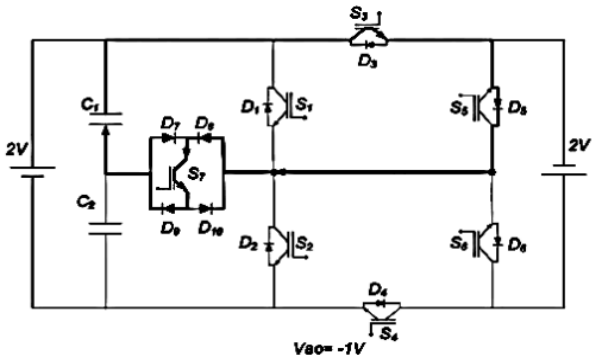


Fig. 3.6 switching combinations for the voltage of V_o = -1V

f) For V_0 = -2V level output:

The output voltage V_o = -2V is possible by two switching combinations, which are clearly mentioned in the Table 3.1. These three switching states are required for balancing the capacitors and its voltage to a prescribed value of -2V. Switches S_3, S_6 are 'ON' and D_1 is conducting.

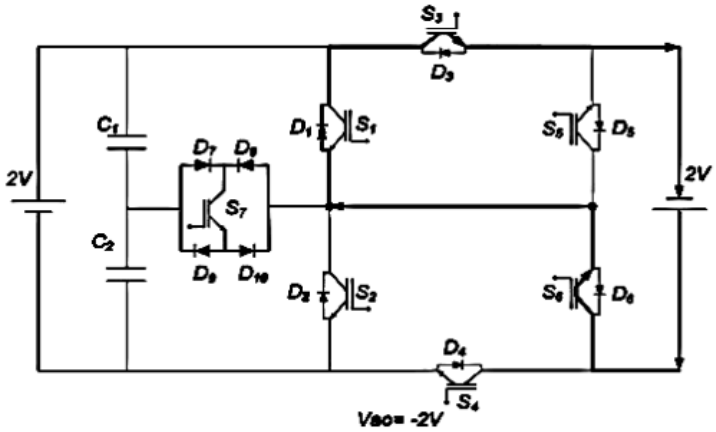


Fig. 3.7 switching combinations for the voltage of V_o = -2V

g) For V_0 = -3V level output:

The output voltage V_o = -3V is possible by three switching combinations, which are clearly mentioned in the Table 3.1. These three switching states are required for balancing the capacitors and its voltage to a prescribed value of -3V. Switches S_3, S_6, S_7 are 'ON' and D_9, D_{10} are conducting.

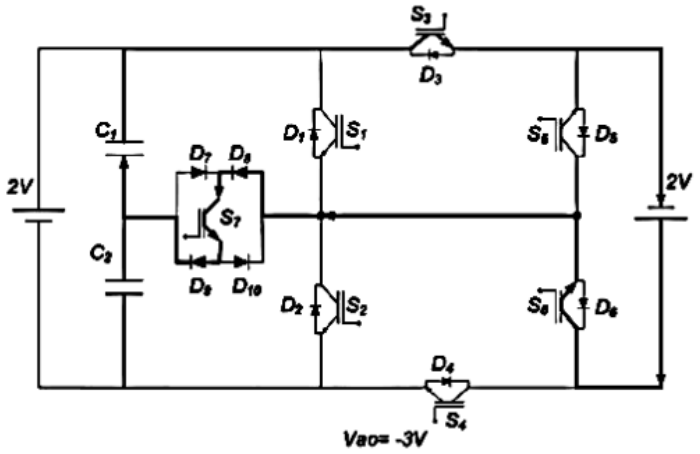


Fig. 3.8 switching combinations for the voltage of V_o = -3V

h) For V_0 = -4V level output:

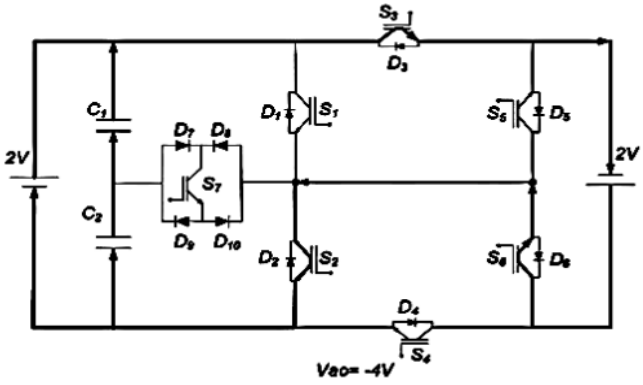


Fig. 3.9 switching combinations for the voltage of V_o = -4V

The output voltage V_o = -4V is possible by three switching combinations, which are clearly mentioned in the Table 3.1. These three switching states are required for balancing the capacitors and its voltage to a prescribed value of 3V.Switches S_2, S_6, S_3 are 'ON'.

3.2 Simulation model for 9 level H-Bridge:

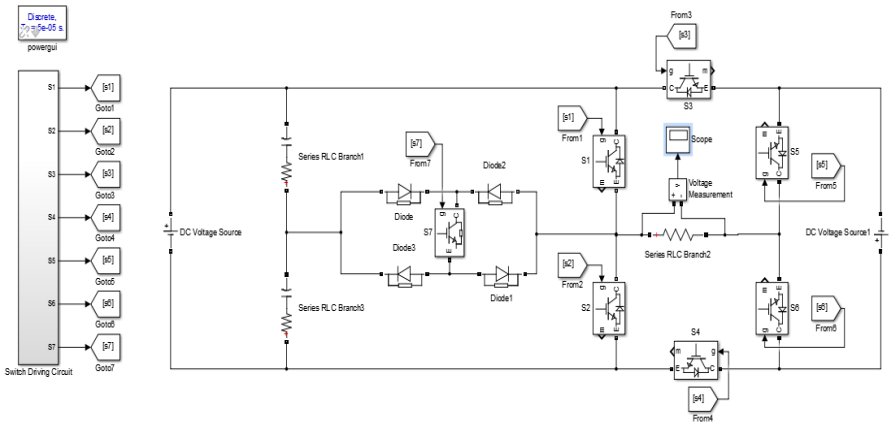


Fig. 3.10 Simulation model for enhanced multi-level inverter

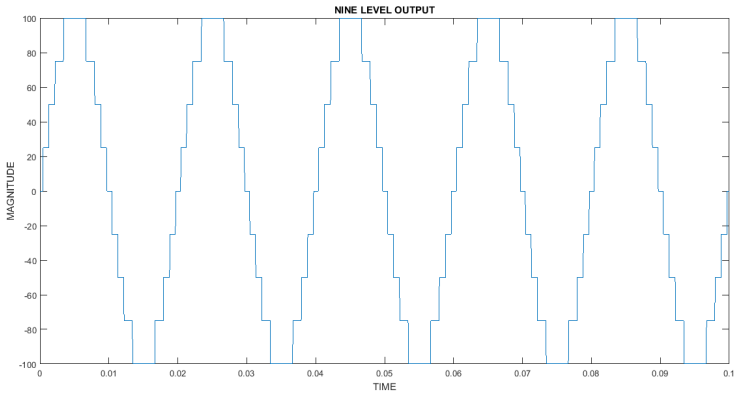


Fig. 3.11 Output waveform for 9 level H-bridge inverter

Table 3.3. Various switching combinations with conducting diodes

S. No.	Output voltage levels	ON state switches
1	5V/3	S_1, S_4, S_5
2	5V/6	S_4, S_5, S_7
3	2V/3	S_2, S_4, S_5
4	V	S_1, S_4, S_6
5	V/2	S_4, S_7, S_6
6	0	S_1, S_3, S_5
7	-V/2	S_3, S_5, S_7
8	-V	S_2, S_3, S_5
9	-2V/3	S_1, S_3, S_6
10	-5V/6	S_3, S_6, S_7
11	-5V/3	S_2, S_3, S_6

The steps to synthesize the output voltage levels of 11level H-bridge inverter are as follows:

a) For V_0 = 0V level output:

The output voltage V_o = 0V is possible by three switching combinations, which are clearly mentioned in the Table 3.3. These three switching states are required for balancing value of 0V. S_1, S_3, S_5 switches are 'ON'

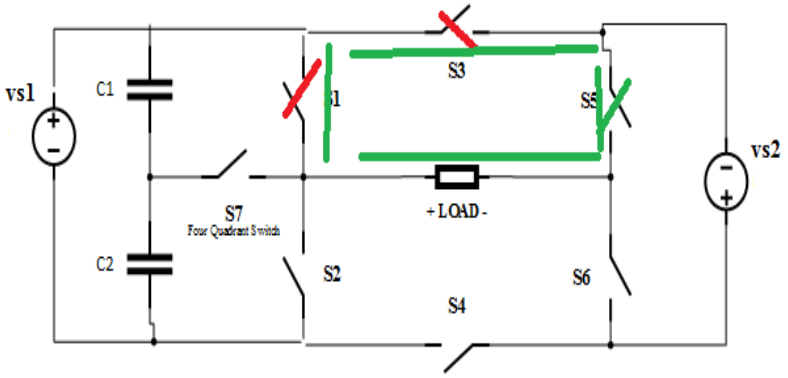


Fig. 3.12 switching combinations for the voltage of V_o = 0

b) For V_0 = V/2 level output:

The output voltage V_o = V/2 is possible by three switching combinations, which are clearly mentioned in the Table 3.3. These three switching states are required for balancing the capacitor C_2 and its voltage to a prescribed value of V/2. S_4,S_6,S_7switches are 'ON'.

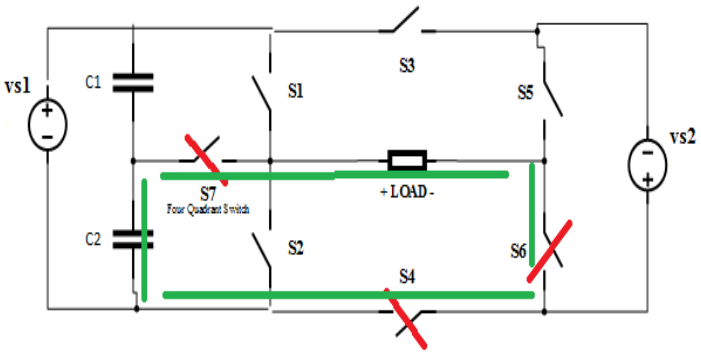


Fig. 3.13 switching combinations for the voltage of $V_o = V/2$

c) For $V_0 = V$ level output:

The output voltage $V_o = 1V$ is possible by three switching combinations, which are clearly mentioned in the Table 3.3. These three switching states are required for balancing the VS1 and its voltage to a prescribed value of 1V. S_4, S_1, S_6 switches are 'ON'.

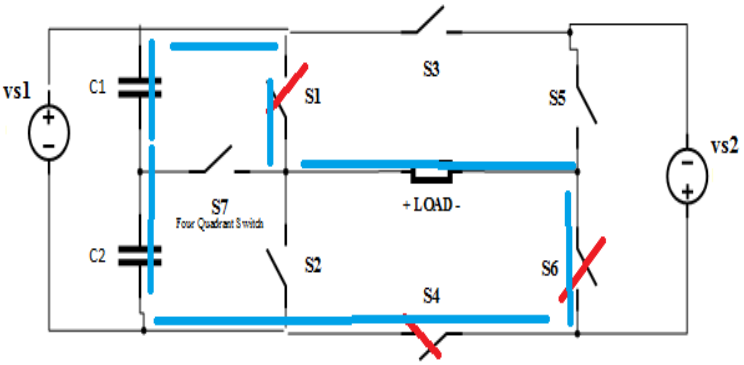


Fig. 3.14 switching combinations for the voltage of $V_o = V$

d) For $V_0 = 2V/3$ level output:

The output voltage $V_o = 2V/3$ is possible by three switching combinations, which are clearly mentioned in the Table 3.3. These three switching states are required for balancing the VS2 and its voltage to a prescribed value of 2V/3. S_2, S_5, S_4 switches are 'ON'.

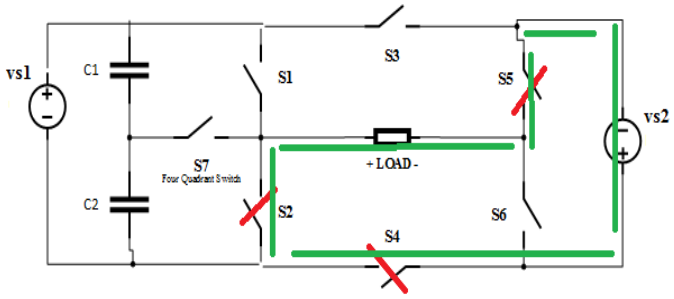


Fig. 3.15 switching combinations for the voltage of $V_o = 2V/3$

e) For V_0 = 5V/6 level output:

The output voltage V_o = 5V/6 is possible by three switching combinations, which are clearly mentioned in the Table 3.3. These three switching states are required for balancing the capacitor C_2 and VS2 source its voltages to a prescribed value of 5V/6. S_4, S_5, S_7 switches are 'ON'.

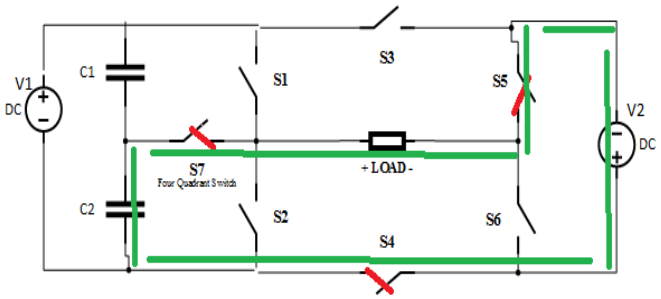


Fig. 3.16 switching combinations for the voltage of V_o = 5V/6

f) For V_0 = 5V/3 level output:

The output voltage V_o = 5V/3 is possible by three switching combinations, which are clearly mentioned in the Table 3.3. These three switching states are required for balancing the VS1 and VS2 its voltages to a prescribed value of 5V/3. S_4, S_5, S_1 switches are 'ON'.

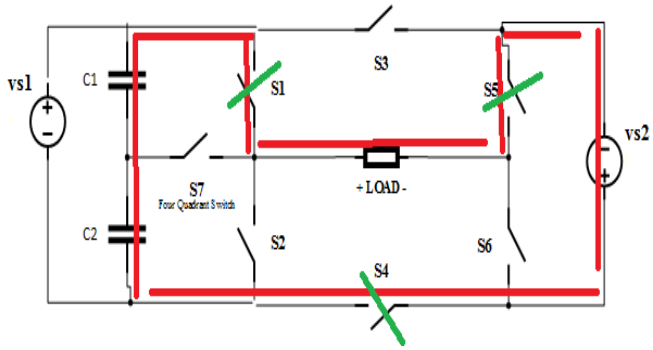


Fig. 3.17 switching combinations for the voltage of V_o = 5V/3

g) For V_0 = -V/2 level output:

The output voltage V_o = -V/2 is possible by three switching combinations, which are clearly mentioned in the Table 3.3. These three switching states are required for balancing the capacitor C_1 and its voltage to a prescribed value of -V/2. S_3, S_5, S_7 switches are 'ON'.

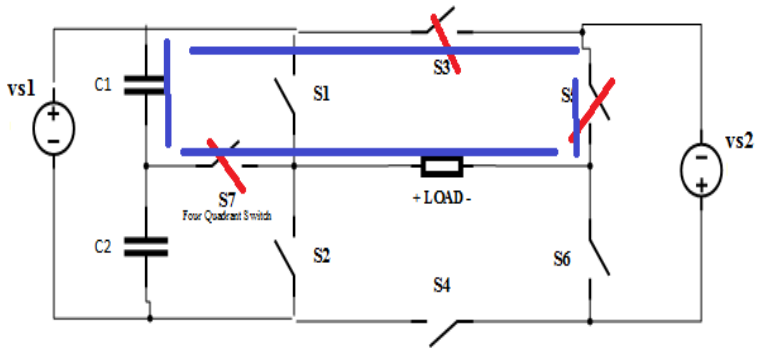


Fig. 3.18 switching combinations for the voltage of V_o = -V/2

h) For V_0 = -V level output:

The output voltage V_o = -1V is possible by three switching combinations, which are clearly mentioned in the Table 3.3. These three switching states are required for balancing the VS1 and its voltage to a prescribed value of -1V. S_2, S_3, S_5 switches are 'ON'.

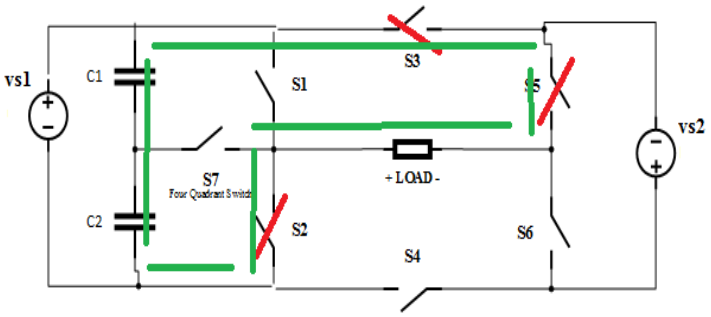


Fig. 3.19 switching combinations for the voltage of V_o = -V

i) For V_0 = -2V/3 level output:

The output voltage V_o = -2V/3 is possible by three switching combinations, which are clearly mentioned in the Table 3.3. These three switching states are required for balancing the VS2 and its voltage to a prescribed value of -2V/3. S_1, S_3, S_6 switches are 'ON'.

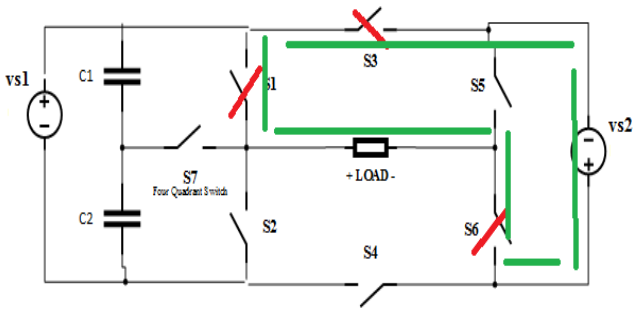


Fig. 3.20 switching combinations for the voltage of V_o = -2V/3

j) For V_0 = -5V/6 level output:

The output voltage V_o = -5V/6 is possible by three switching combinations, which are clearly mentioned in the Table 3.3. These three switching states are required for balancing the capacitor C_2 and VS2 its voltages to a prescribed value of -5V/6. S_3, S_6, S_7 switches are 'ON'.

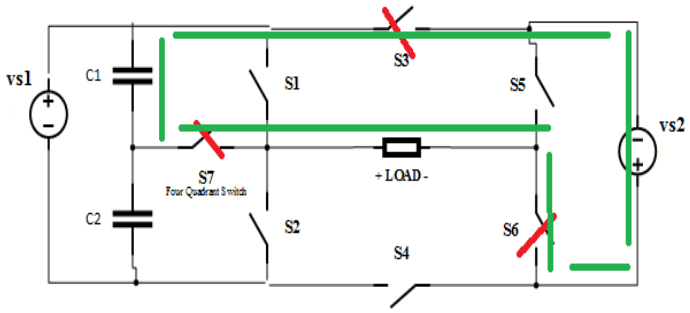


Fig. 3.21 switching combinations for the voltage of V_o = -5V/6

k) For V_0 = -5V/3 level output:

The output voltage V_o = -5V/3 is possible by three switching combinations, which are clearly mentioned in the Table 3.3. These three switching states are required for balancing the VS1 and VS2 its voltageS to a prescribed value of -5V/3. S_2, S_3, S_6 switches are 'ON'.

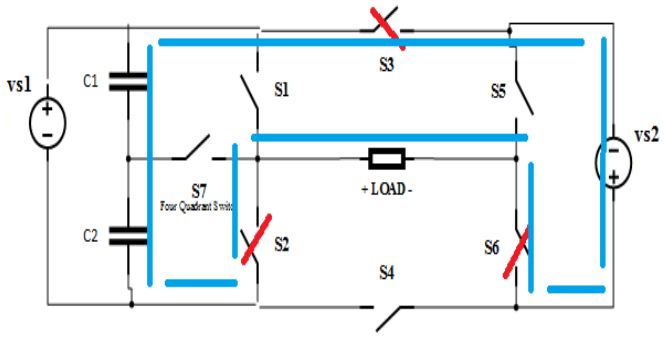


Fig. 3.22 switching combinations for the voltage of V_o = -5V/3

3.4 Simulation model for 11 level H-Bridge:

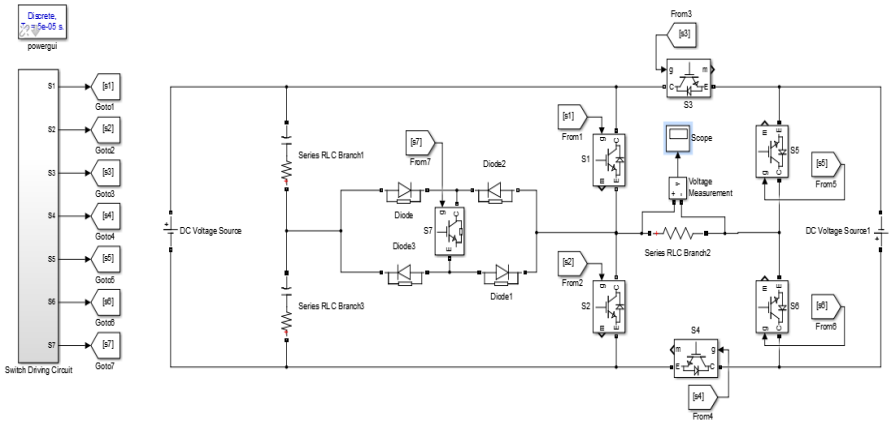


Fig. 3.23 Simulation model for enhanced multi-level inverter

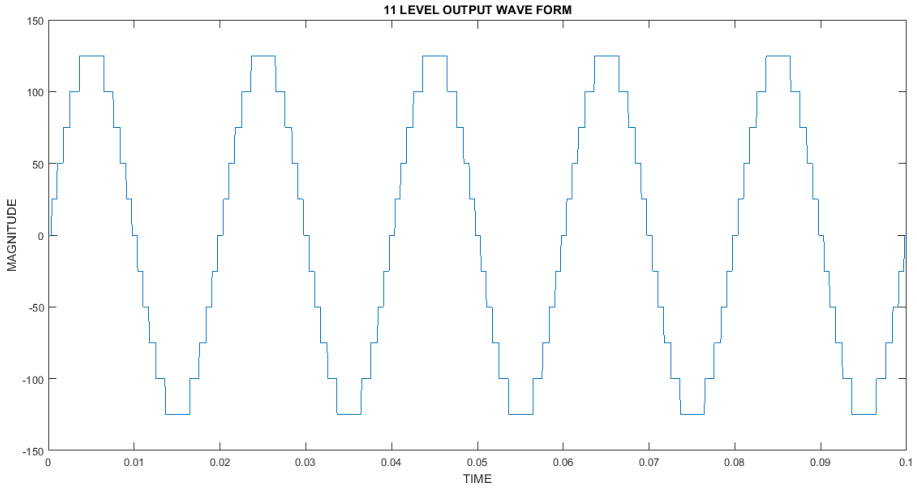


Fig. 3.24 Output waveform for 11 level H-bridge inverter

3.5 Summary

This chapter has enhanced multi-level inverter presented, which can generate the multilevel voltages in output with a two dc-sources. This enhanced multi-level inverter contains seven switches and diodes, in which one of the switches in this circuit works as an auxiliary switch. In this chapter the methodology and switching circuits are explained.

Chapter 4

Simulation Model And Output Wave Forms

Introduction

Simulation results

Hardware Progress

Summary

4.1 Introduction

In this chapter we can observe the effectiveness and performance of the enhanced 9-level inverter topology by using MATLAB/SIMULINK version. R2015a. Simulink software is a modern design tool that allows scientists and engineers to rapidly and easily build the any type of models.

4.2 Simulation results of enhanced multi-level inverter:

MATLAB/ Simulink R2015a environment is used to study the desired objective of this work. Figure shows the 9Level H-bridge and 11Level H-bridge single phase inverter simulation circuit along with its voltage waveforms. The inverter is having two supply sources as DC with a magnitude of 50V each source for 9 level H-Bridge and VS1=50V, VS2=75 because (VS1= [2/3] *VS2) for 11level H-Bridge. The switches are IGBT's with internal diodes and having internal resistance of 1m Ω. are used.

4.2.1 Simulation Model for 9 level H-Bridge:

Figure 4.1 shows the 9 level H-bridge inverter simulation model with two dc source and two capacitors. The two capacitors present in the topology are charged to voltage of $V_{dc}/2$, V_{dc} /2 respectively. The inverter is having two supply sources as DC with a magnitude of V_{dc} =50V each. A load which have been taken as the R load (R = 100Ω) for simulation purpose. The switches are IGBT's with internal diodes and having internal resistance of 1m Ω.

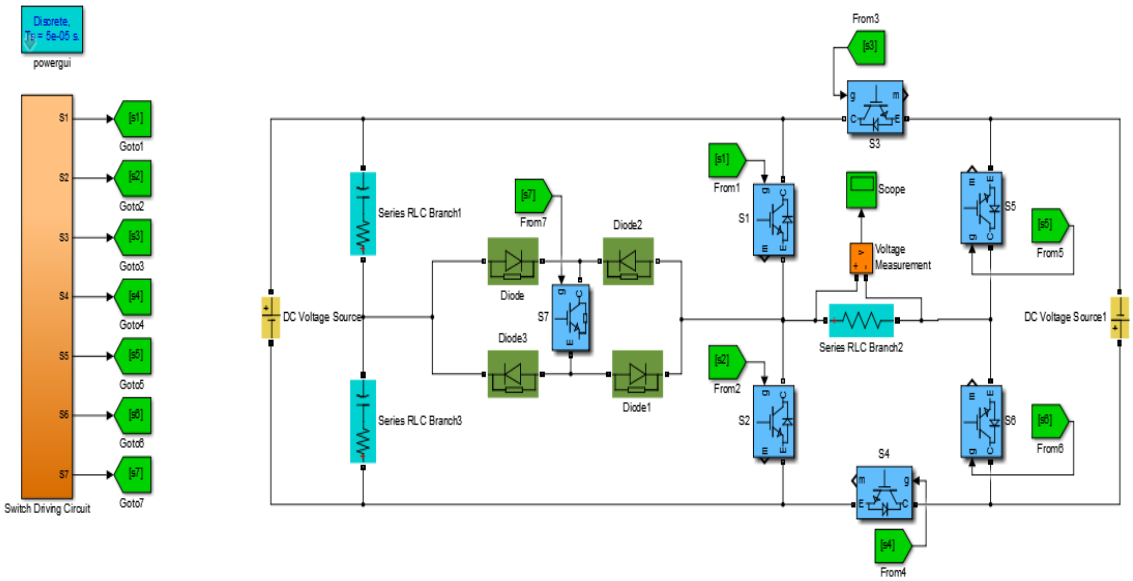


Fig. 4.1 Simulation model of 9 level H-Bridge inverter with two dc source.

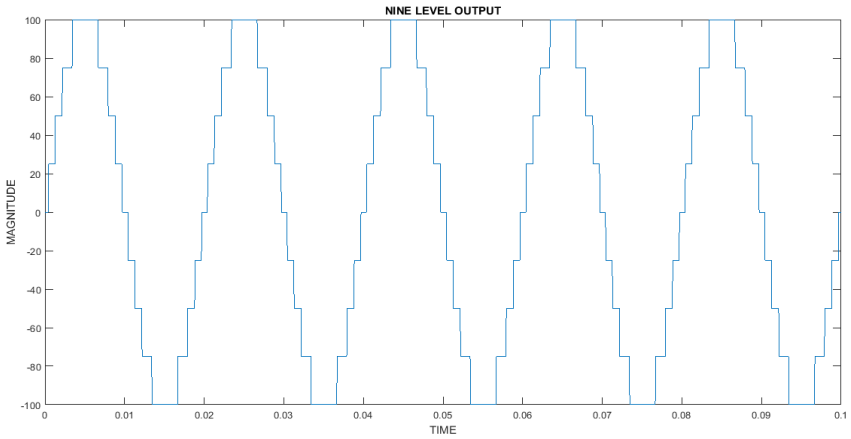


Fig. 4.2 Output voltage wave forms of 9-level inverter by using two dc sources with R load.

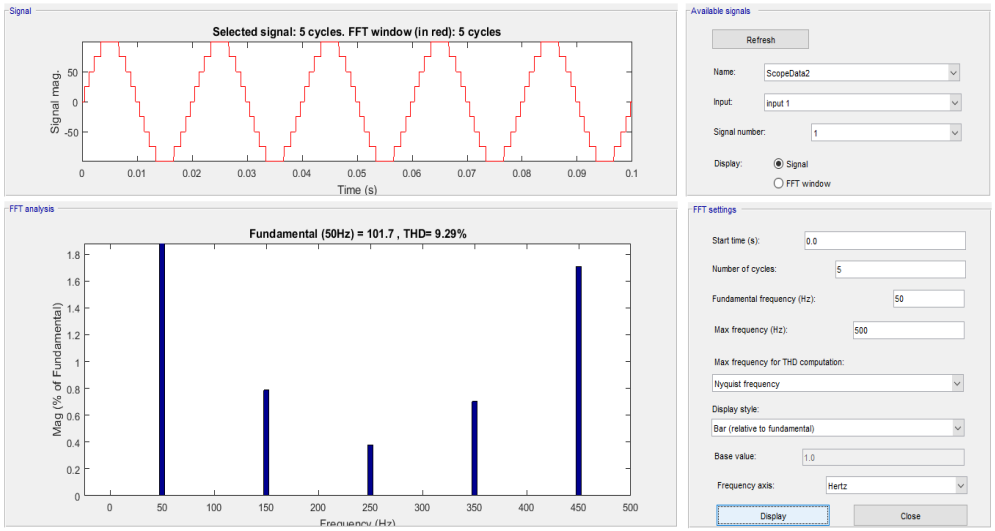


Fig. 4.3 Output voltage THD spectrum for 9 level H-Bridge inverter by using two dc source with R load.

Figure 4.2 shows the output voltage waveforms of enhanced multi-level inverter and its THD spectrum shown in figure 4.3. The fundamental peak value of output is V_{peak} =101.7V. Here the load is pure resistive(R=100Ω) is used. So that both voltage current are having same wave shape.. Also the THD spectrum for output voltage is same and value is 9.29%.

4.2.2 Simulation Model for 11 level H-Bridge:

Figure 4.1 shows the 11 level H-bridge inverter simulation model with two dc source and two capacitors. The two capacitors present in the topology are charged to voltage of $V_{dc}/2$, V_{dc} /2 respectively. The inverter is having two supply sources as DC with a magnitude of VS1=50V and VS2=75V. A load which have been taken as the R

load (R = 100Ω) for simulation purpose. The switches are IGBT's with internal diodes and having internal resistance of 1m Ω.

4.2.2 Simulation Model for 9level H-bridge

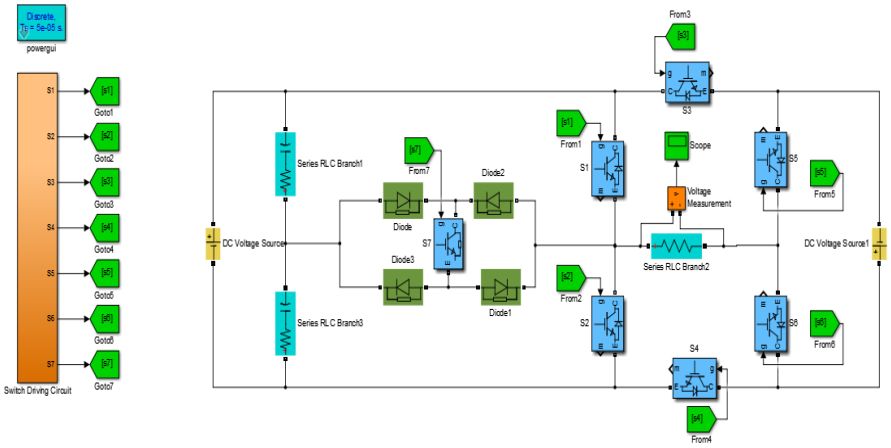


Fig. 4.4 Simulation model of 11 level H-Bridge inverter with two dc source.

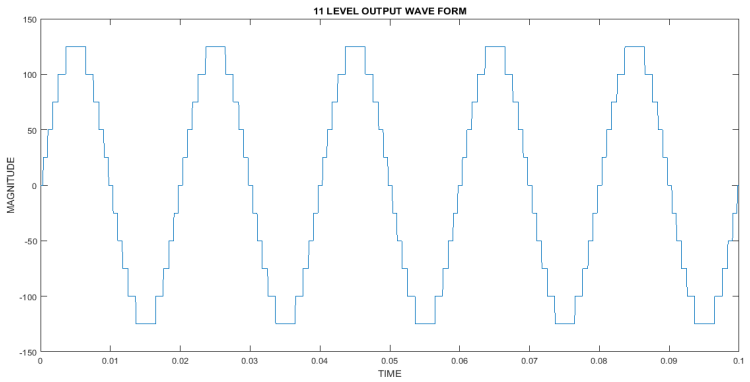


Fig. 4.5 Output voltage wave forms of 11-level inverter by using two dc sources with R load

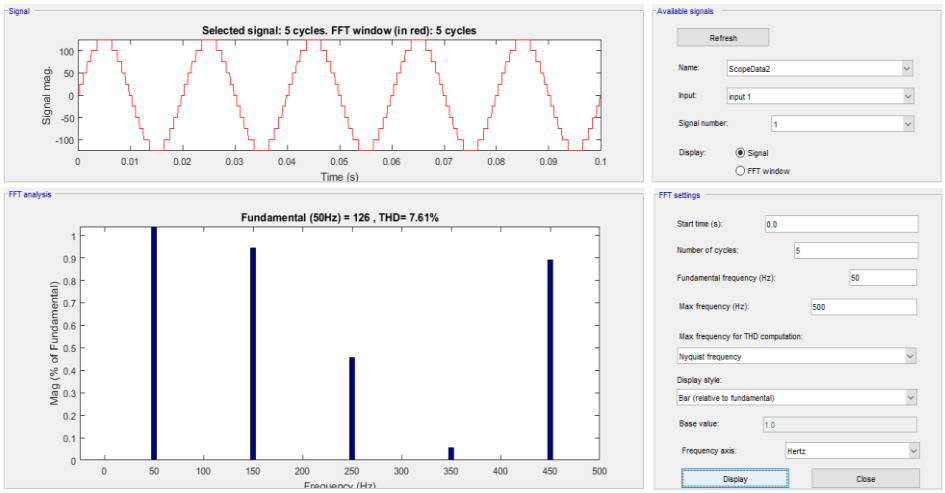


Fig. 4.6 Output voltage THD spectrum for 11level H-Bridge inverter by using two dc source with R load.

Figure 4.2 shows the output voltage waveforms of enhanced multi-level inverter and its THD spectrum shown in figure 4.3. The fundamental peak value of output is V_{peak} =101.7V. Here the load is pure resistive(R=100Ω) is used. So that both voltage current is having same wave shape. Also the THD spectrum for output voltage is same and value is 7.61%.

4.2.3 Simulation model for Gate Pulses:

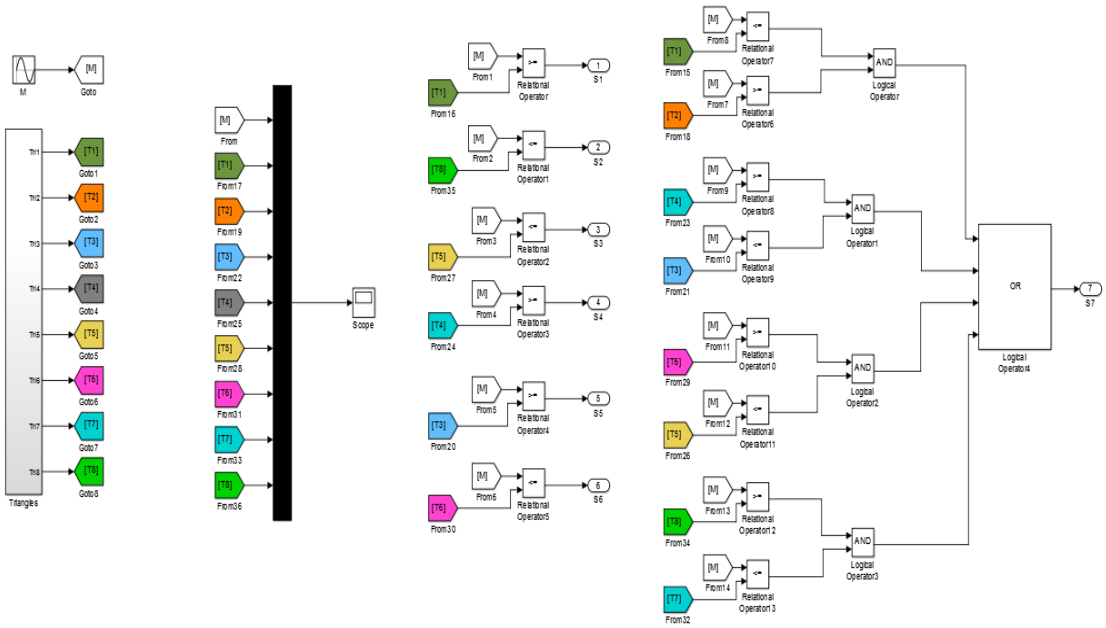
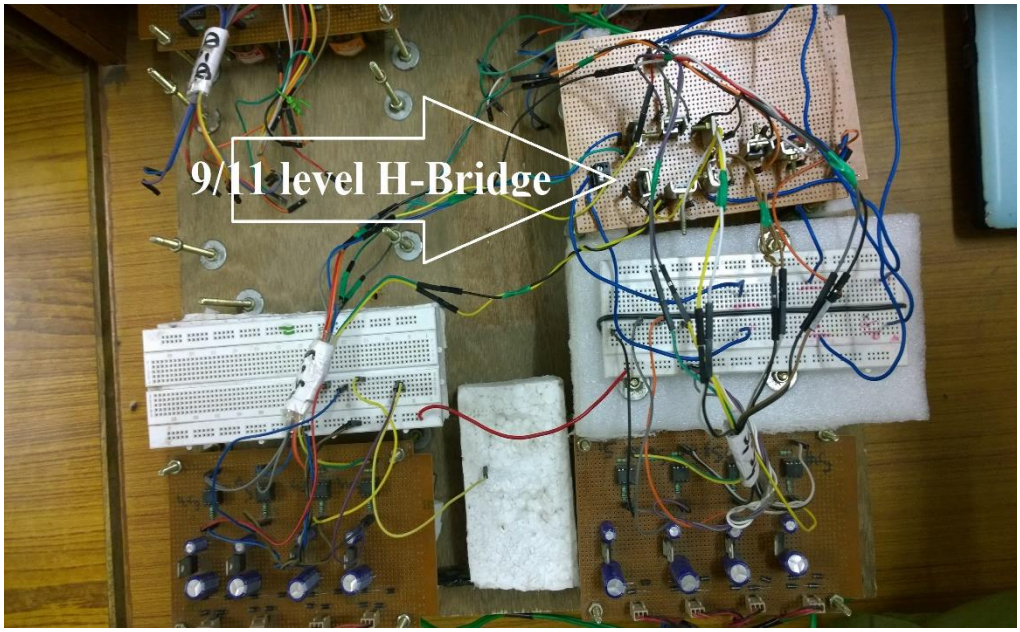


Fig. 4.4 Simulation model for PWM technique to produce gate pulse

In this work, the Sinusoidal PWM and square wave technique are used to control the enhanced inverter. The Sinusoidal PWM technique can minimize the harmonics along with the control of inverter output voltage. The requirement of filter will be minimized as the higher order harmonics can be eliminated easily with SPWM. The diodes are used in this power circuit are having same value of R_{on}, R_s as IGBT modules.

4.2.4. Hardware Progress:

The 9/11 level H-Bridge is implemented by using eight IRF840N MOSFET modules. In eight MOSFET 2 switches are for four quadrant switch implementation. Arduino Mega 2560 is used for generating the triggering signals for all MOSFETs.



9/11 level H-Bridge Inverter Hardware

4.3 Summary

In this chapter effectiveness and operation of the 9level and 11level H-Bridge inverter topology is investigated by using MATLAB R2015a.

Advantages: less cost, small size, less switching losses and high value of fundamental component, easy to control

Chapter 5

Conclusion

Conclusion

Scope for Future work: Hardware output texting of 9/11 level H-bridge inverter and hardware implementation of cascaded 11level H-Bridge inverter which produces 21 level output from a two dc-sources.

5.1 Conclusion

In recent years, industry has begun to demand higher power equipment, which now reaches the megawatt level. Although, two-level converters are preferable for low-power applications and some medium-power applications, but they are failed to fulfil the requirements of high-voltage and industrial applications. Because of this reason many researches are going on from last three decades, and many new structures and new conventional topologies has been proposed. The main challenge is Voltage balancing which will arise both in Diode-clamped and Capacitor-clamped inverters. Cascaded H-Bridge inverters are mainly used in high voltage and high power motor drives because of their quality output with minimum amount of harmonic content, and less number of devices. But this CHMLI requires separate dc sources every H-Bridge. It increases inverter cost and complexity.

In this thesis Multi-level inverter has been enhanced, which is formed by a seven semi-conductor switches, ten diodes, capacitors and two dc sources. Which is generating nine levels of output voltage (pole voltage) from a two dc power supply. And this inverter can generate a more steps of voltage levels with reduced number of switches, gate driver circuits and diodes as compare to conventional multilevel inverter. The enhanced inverter with more number of levels can improve power quality, lower switching losses and produce high quality voltage waveforms.

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