A New Single Phase Multilevel Inverter Topology with Reduced Number of Switches

DISSERTATION-II

Submitted in partial fulfillment of the

Requirement for the award of the

Degree of

MASTER OF TECHNOLOGY

IN

ELECTRICAL ENGINEERING

By

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MAY 2017

CERTIFICATE

This is to certify that the Thesis titled **"A New Single Phase Multilevel Topology with Reduced Number of Switches"** that is being submitted by **GURPREET SINGH** is in partial fulfillment of the requirements for the award of MASTER OF TECHNOLOGY DEGREE, is a record of bonafide work done under my /our guidance. The contents of this Thesis, in full or in parts, have neither been taken from any other source nor have been submitted to any other Institute or University for award of any degree or diploma and the same is certified.

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E x a m i n e r   I   **E x a m i n e r   I I**

ACKNOWLEDGEMENT

First and foremost, I am deeply indebted to my mentor **"NIRAJ KISHORE"** whose inspiration has been unfailingly available to me at all stages of this work. This has fueled my enthusiasm even further and encouraged me to boldly step into what was a totally dark and unexplored expanse before for me. I would like to thank for my teachers for his efforts, who was always ready with a positive comment, whether it was an off-hand comment to encourage us or constructive piece of criticism. In course of present work, it has been our privilege to receive help and assistance of my friends. I take great pleasure in acknowledge my debt to them. At last but not the least I want to thank my parents who appreciated me regard this work and motivate me.

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This is to certify that **GURPREET SINGH** bearing Registration no. **11201011** has completed objective formulation of thesis titled, **"A New Single Phase Multilevel Topology with Reduced Number of Switches"** under my guidance and supervision. To the best of my knowledge, the present work is the result of her original investigation and study. No part of the thesis has ever been submitted for any other degree at any University.

The thesis is fit for submission and the partial fulfillment of the conditions for the award of Dissertation-II.

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<u>DECLARATION</u>

I, **GURPREET SINGH**, student of **Masters of Technology** under **School of Electronics and Electrical Engineering** of Lovely Professional University, Punjab, hereby declare that all the information furnished in this thesis report is based on my own intensive research and is genuine.

This thesis does to the best of my knowledge, contain part of my work which has been submitted for the award of my degree either of this university or any other university with proper citation.

Date :   Signature and Name of the student

Registration No. : 11201011   GURPREET SINGH

ABSTRACT

The ever-increasing reliance on electronic devices which utilize AC power highlights the problems associated with the unexpected loss of power from the electrical grid. In places where the electrical infrastructure is not well-developed, brown-outs can prove fatal when electronic medical instruments become unusable. Recently introduced topologies achieve higher number of output voltage steps and less harmonics with reducing the number of switches, DC voltage sources and losses as compared to conventional topologies. The improved topology offers reduced number of switches, low voltage imbalances and Dc sources. Through this topology, size and cost reduces and it enhances the overall performance. Improved topology is capable to produce 31 and 63 levels (peak to peak) of output voltage with twelve and fourteen switches only. A comparative analysis with conventional topology is done in terms of switches used, DC sources used, diodes and in terms of output quality and THD obtained. Simulation of topology is done in MATLAB 2009 Simulink model.

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LIST OF ABBREVIATIONS

MLI   Multi-Level Inverter

PWM   Pulse Width Modulation

DC   Direct Current

AC   Alternating Current

IGBT   Insulated Gate Bipolar Transistor

MOSFET   Metal Oxide Semi-conductor Field Effect Transistor

Hz   Hertz

UPS   Uninterruptible Power Supply

SMPS   Switched Mode Power Supply

HVDC   High Voltage Direct Current

HVAC   High Voltage Alternating Current

DTC   Direct Torque Control

VAR   Volt-Ampere Reactive

THD   Total Harmonic Distortion

Chapter 1

Introduction

The concept of inverter

Why power conversion

IGBT vs MOSFET

Types of inverter

Problem statement

Introduction to Multilevel inverter

Multilevel Inverter Topologies

Modulation Strategy

1.1 The concept of inverter

An inverter is an electronic device or equipment that gives alternating current (AC) from direct current (DC). We use power semiconductor devices to control, convert and condition electrical power output. Inverters comes in different sizes. They can be as small as 150 watts in power, or can be as large as 1 megawatt (10 lakh watt). Inverter can be entirely made up of electronic components or may be a combination of mechanical equipment (rotatory equipment) and electronic devices. Now a day, most of the inverters are static inverters and do not use any moving parts in the conversion procedure.

1.2 Why power conversion

Electricity is distributed to consumers in the form of alternating current because AC voltage can be stepped up or stepped down using a transformer. By stepping up the voltage level, power can be transmitted over the power lines to a very long distance with less losses because as the voltage increases, the current through the line decreases and hence, there are less heating losses and conductor size required will be thinner. At consumer level, voltage can be stepped down to a safer level using transformers. So, whole of the electric power system is built around alternating current and not direct current. The adoption of AC power has created trend where mostly all the devices use AC power from the power outlet. But, AC power is not always available and there can be a situation where mobility and simplicity gives batteries a great advantage in portable applications.

Inverters are used because batteries cannot store alternating current and can only provide direct current and we don't have DC transformers as transformers works only on alternating current i.e. sinusoidal waveforms. Also, there can be mismatch between power supply available and power supply requirements of load especially when we have frequency mismatch. In different countries and areas, different power supply is available:

❖ Main voltage
   220V, 50Hz, 1-phase
   400V, 50Hz, 3-phase
   110V, 60Hz, 1-phase

115V, 400Hz, 3-phase
- ❖ Stored energy in batteries
    DC voltage – 12V, 24V, 48V etc.

Previously, inverters were only used in some main power application, which tends to be large scale and expensive, but now a days, inverters are small compulsory electronic device, on which our many electronic device depends.

1.3 IGBT vs Power MOSFET

Whenever there is a design choice of any power electronic equipment, a choice has to be made between two main types of switching devices readily available. They are insulated gate bipolar transistor or IGBT which is used in very high power applications, but relatively low frequencies, and the other one being the power MOSFET, which is very similar to regular MOSFET, but designed for handling relatively large voltages and currents through it.

Power MOSFET s came in 1970's. Power MOSFET s has very high switching frequency capability as compared to IGBT, ranging in few MHz. They are voltage controlled device and not current controlled and have a positive temperature co-efficient, thus stopping thermal runaway. On state losses of MOSFETs are very low because of low on state resistance. The MOSFET also have a body diode, which can be good or bad thing depending on the application, particularly useful in situations with limited freewheeling currents. MOSFET s do not have current tail power losses, which makes them more efficient than IGBTs. They do not have as much capability for high voltage and currents as IGBT and tend to be used at voltages lower than 250V and power rating less than 500W. MOSFET s are ideally used for low voltage but high frequency applications like in Uninterruptible Power Supply (UPS), Switched Mode Power Supply (SMPS), and battery charging circuits etc.

Then, there came IGBTs in 1980s, which is a cross between bipolar transistor and MOSFET. IGBT has switching n and conduction characteristics much similar to that of a bipolar transistor but is voltage controlled device like MOSFET. IGBT tend to be very

useful in very high in power applications. In the year 2003, Mitsubishi Electric introduced dual IGBT modules with a rated current of 100A to 1000A, employing the CSTBT – IGBT technology. This technology has reduced the static and switching losses and is capable of switching at a frequency of 50 KHz. IGBT tend to be used in very high power application and high voltage levels, generally above 600V. They are able to handle high amounts of currents and able to output greater than 5Kw. IGBT have negative temperature co-efficient, which could lead to thermal runaway and also, paralleling of them is hard to achieve. They are able to operate properly above 100° Celsius. IGBT don't have body diode, which may be helpful in some situations. One major disadvantage of IGBT is that, it still has comparatively large tail current. IGBTs are generally used in applications like Motor speed control, Uninterruptible Power supplies of power higher than 5Kw, welding, lighting etc.

MOSFETs are great choice in:

❖ High frequency applications (>200KHz)
❖ Wide line or load variations
❖ Long duty cycles
❖ Low voltage applications with greater efficiency (<250V)
❖ Low output power (<500W)

IGBTs are preferred in applications in these conditions:

❖ Low duty cycle
❖ Low to medium frequency (<25KHz)
❖ Narrow or small line or load variations
❖ High voltage applications (>1000V)
❖ High output power

The 9.5-Watt IGBT losses are higher than the 7-Watt MOSFET losses at room temperature. So, MOSFETs have lower losses and hence higher efficiency. Comparison of voltage and operating frequency of MOSFET and IGBT is given below in fig 1.1:
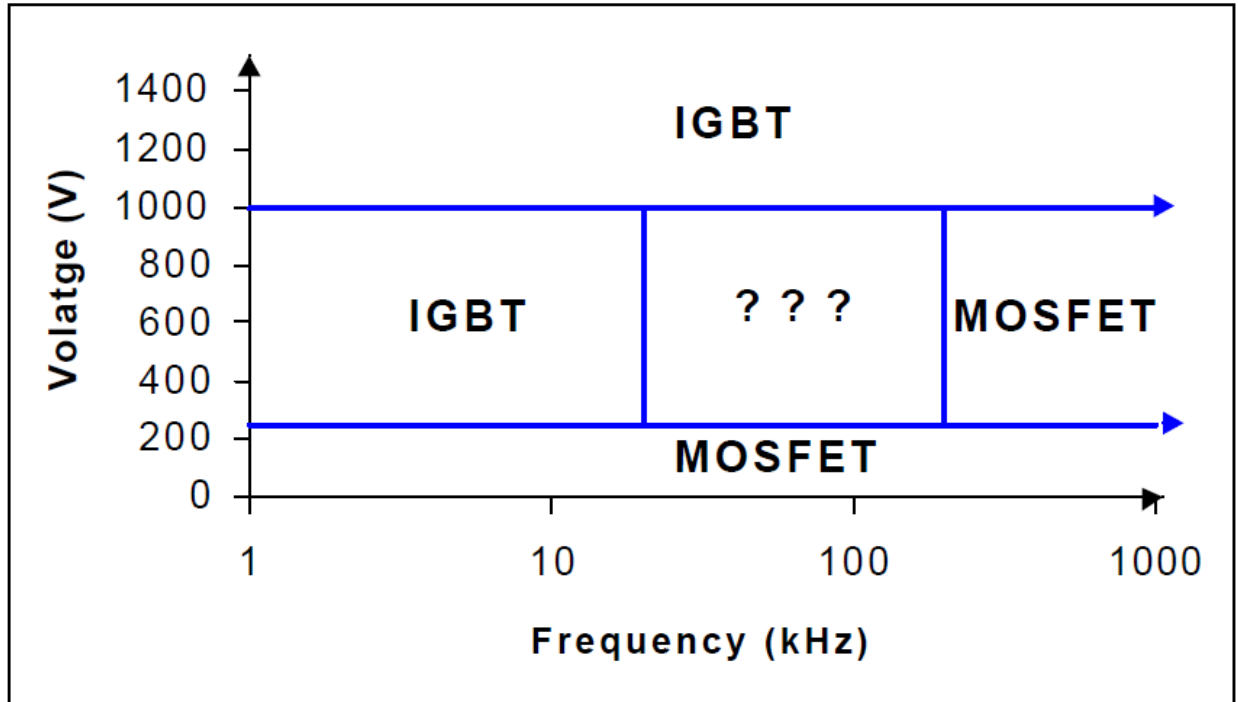
Fig 1.1 Where MOSFETs and IGBTs are preferred

1.4 Types of inverter

Inverters are broadly classified into three types which are available in market according to their output waveform: square wave, modified -sine wave and pure sine wave. Off-the-shelf or stand-alone inverters are most of the time either square wave or modified-sine wave inverters. This is because they are less costly to manufacture and output delivered is the same average voltage to the load. Pure sine wave inverters give pure sine wave as the name suggest and offers more accuracy and gives less harmonics in their output waveform and deliver power with less power losses and less heat generation, as such they are appropriate for delicate electronic devices which rely on precise timing and delicate loads like computers etc. but, tend to be more complex in design and are most costly.

1.4.1 Square wave inverter

It is the simplest type of inverter, which converts dc voltage into shifting AC signal, but the output is not pure AC and it is square wave. Their construction includes an on/off switch as shown in fig. they are limited to a very few uses and will run simple things like universal motors without a problem and is best suited for low-sensitivity applications such as lighting and heating, but not much else. Square wave inverters are seldom seen anymore. The output of square wave is shown in fig 1.2.
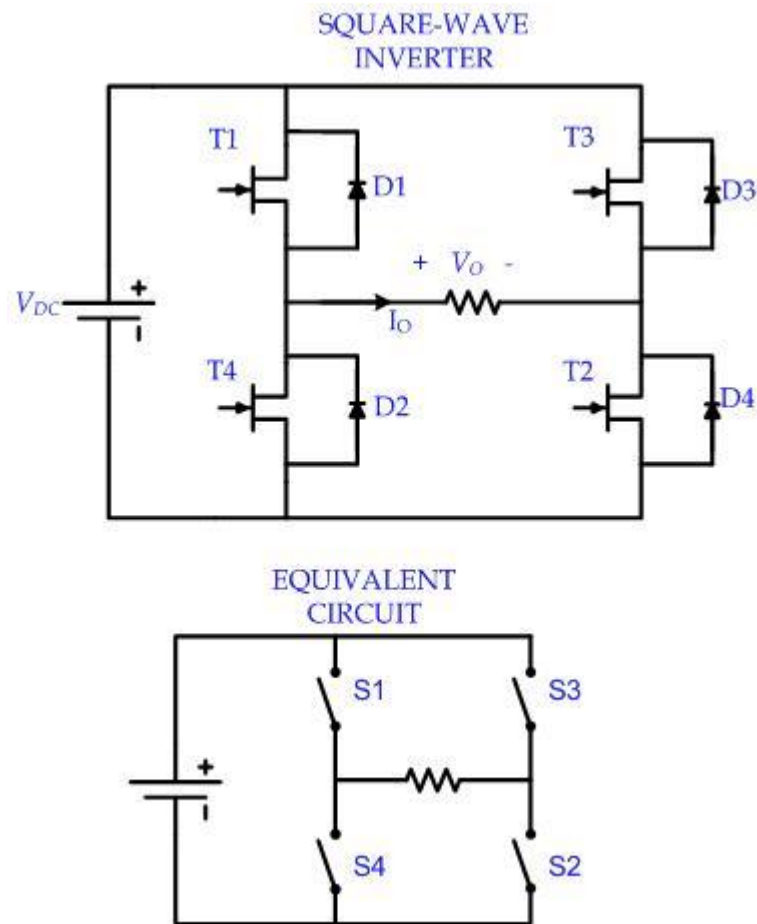

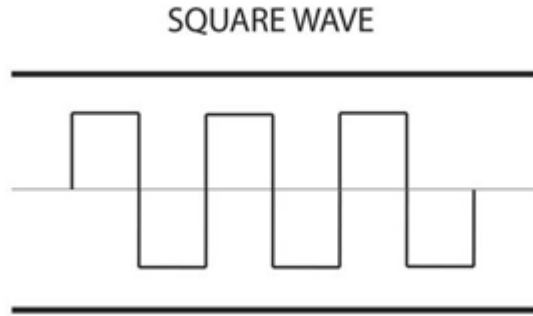Fig 1.2(a) circuit diagram of square wave inverter

SQUARE WAVE

Fig 1.2(b) output of square wave inverter

1.4.2 Modified square wave inverter

A modified square wave inverter has a waveform resembling to square wave, but with an extra step or so. There are three voltage levels in the output waveform, high, low and zero with a dead time zone between the high and low pulses and this results in three level waveform with equal intervals of zero volts; peak positive volts; zero volts; peak negative volts and then zero volts. This reduces the voltage stress across the switches. This type of inverter works fine with most equipment like incandescent light bulbs and switch-mode power supply but can produce heating of main transformer depending upon its rating, although the efficiency will be reduced. Motors will be using about 20% more power. Some fluorescent lights will not operate as desired and as bright and may buzz or make annoying noises. Appliances like electronic clock or digital times may become asynchronous and loose time. Modified square wave output waveform is given in fig 1.3.
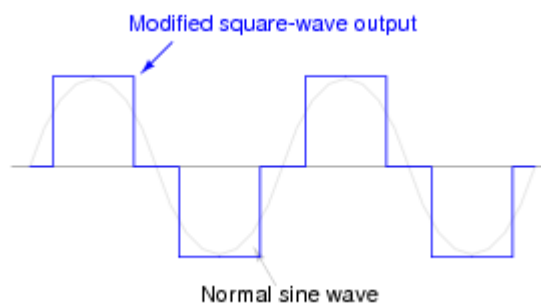

Fig 1.3 output of modified square wave inverter

1.4.3 Sine wave inverters

It is the best source of alternating current out of three types of inverters. It produces multiple step sinusoidal AC waveform with output of much less distortion than the modified sine wave inverter. A true sine wave for high power applications is produced by rotatory electrical machines such diesel generators, DC motors coupled with AC generators. But their cost is too much and due to rotating parts, they require maintenance as such they cannot be used for low power applications, backup supply applications etc. their output waveform is shown in fig 1.4.
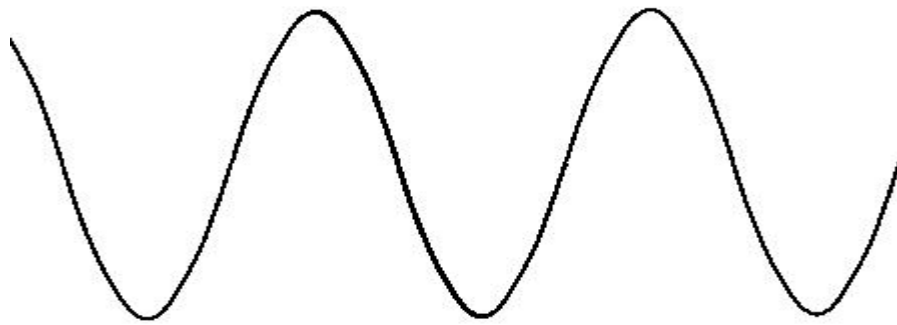
Fig 1.4 output of sine wave inverter

1.5 Problem statement

Developing countries often have limited access to electrical power with poorly developed electrical grid and electrical network is not widely spread throughout the country. Also, brownouts are commonplace and any fault or transient can result in damage of medical equipment etc. Uninterruptible Power Supplies (UPS) can provide temporary remedy to this problem in the developing countries, but due to lack of power or the places where there is no reach of grid connection, either small power plant has to be installed, but this requires time and costs more money and also transporting fuel can be a problem in remote area. So, government emphases on using local renewable energy resources which does not harm the environment and also produces no greenhouse gasses and leaves no or low carbon footprint.

Solar panels or wind turbines can be used in this context as power is generated and used in same area, there is no dependence on grid and also transportation of electricity and its associated losses are reduced. But they are highly unreliable and depends on various factors like daytime, season, wind speed and direction and others. Solar panels produce DC voltage and commercial units works on AC power, due to which there is a requirement of DC to AC converter or inverter having good quality output for various purposes like lighting, cooking, medical aids, refrigeration etc. Wind turbines can give variable output depending on the speed and direction of the wind and so, its output power fluctuates. So, there is the requirement of AC to DC converter to convert variable AC output to fixed DC and smooth the DC output and again convert back to AC through use of inverters.

1.6 Introduction to Multilevel Inverters

Concept of Multilevel Inverters

Conventional two-level inverter is used to get AC output voltage waveform from DC voltage. It can only generate to different levels. A lot of harmonics is produced in the voltage output through this inverter. They are generally switched with PWM, but it also creates Electromagnetic Interference (EMI) that produces humming noise in radio communication, and high dv/dt across the switch. Also, switching losses of the switch increases which causes heating of the switch, produces hotspots and reduces lifespan of the switch.

Instead of using only two levels, several voltage levels are added to each other and this creates smoother stepped waveform similar to sine wave but with reduced dv/dt across the switch and low harmonic distortion. Also, switching is greatly reduced compared to PWM technique, such that they can be used for medium to high power applications. But as the voltage levels increases, both cost and components (diodes, switches, capacitors etc.) increases but we get very clean and near sinusoidal output.

According to the available data, the first multilevel inverter was designed in 1975 and it was a cascade inverter with diodes blocking the source. This inverter was later derived into the diode clamped multilevel inverter also known as neutral clamped multilevel inverter.

1.7 Multilevel Inverter Topologies

1.7.1 Diode Clamped/Neutral Point clamped multilevel Inverter

This inverter is based on the concept to use diode and provide multiple voltage levels by the use of capacitors which are connected in series across the battery or DC source. Diode helps in reducing the stress on switches by transferring limited amount of voltage. The maximum output voltage that is obtained using neutral point clamped multilevel inverter is half of the DC source or battery and this is the main drawback of this inverter.

The following fig 1.5 shows the 5-level (0 to peak) diode clamped Multilevel inverter. Voltage V_{dc} is divided into four capacitors such that across on capacitor, there is a voltage drop of Vdc /4.

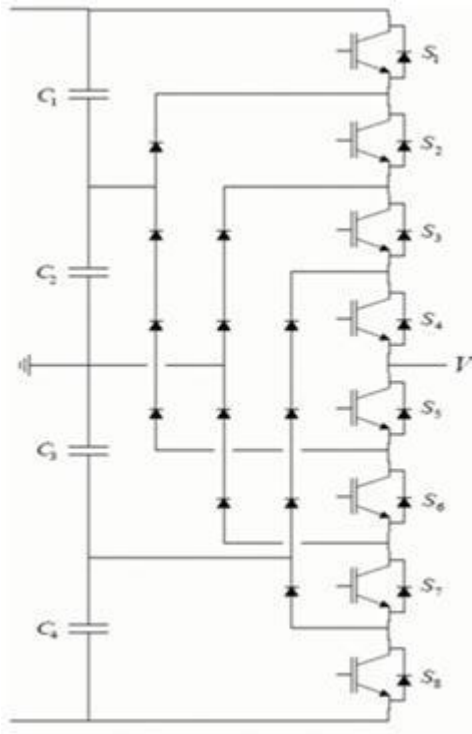Fig 1.5 5-level diode clamped inverter

When the switches s1, s2, s3 and s4 are turned on, we get V_{dc} output voltage. If the switches s2, s3, s4 and s5 are turned on, we get 3 V_{dc}/4 as an output. If switches s3, s4, s5 and s6 are turned on, V_{dc}/2 output is obtained. On turning the switches s4, s5, s6 and s7, we get V_{dc}/4 output voltage. Similar s the case for negative switches.

As capacitors are used in this inverter, capacitor voltage balancing is a major issue such that it is restricted to three or at most five levels only.

Table1.1: Component count of diode-clamped Multilevel inverter

Voltage Level m (0 to peak)	Active Switches 6(m-1)	Clamping Diodes 3(m-1)(m-2)	DC Capacitors (m-1)
3	12	6	2
4	18	18	3
5	24	36	4
6	30	60	5
7	36	90	6

Application areas of Neutral Point clamped multilevel Inverter

- ❖ Static VAR compensation
- ❖ Variable speed motor drives
- ❖ High voltage system interconnections
- ❖ HVDC and HVAC transmission lines

1.7.2 Flying Capacitors Multilevel Inverter

This type of inverter is based on use of capacitors, but clamping diodes are not required in this inverter. The maximum output that is obtained from this type of inverter is half of the DC source or battery and this is their main disadvantage. Through this inverter, we can control both active and reactive power flow.

The following fig 1.6 shows the 5-level (0 to peak) flying capacitor Multilevel inverter. When the switches s1, s2, s3 and s4 are turns on, we get output as Vdc. To get 3 Vdc/4, switches s1, s2, s3 and s1' needs to be turned on. For Vdc/2 voltage output, s1, s2, s2' and s1' are turned on. If switches s1, s1', s2' and s3' are turned on, we get Vdc/4 as the output voltage.
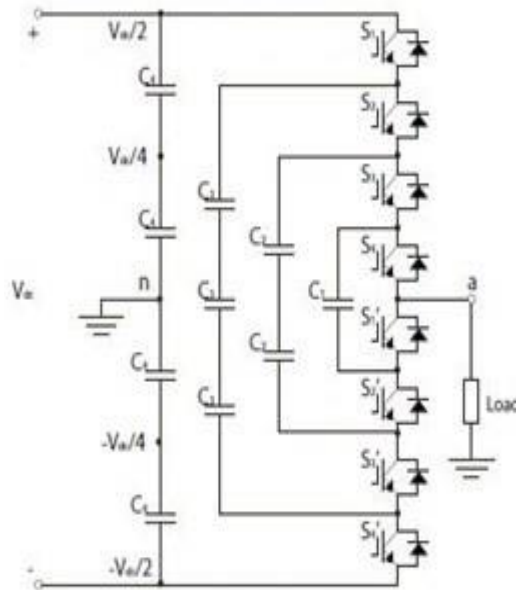
Fig 1.6 5-level flying capacitor multilevel inverter

Table1.2: Component count of flying capacitor Multilevel inverter

Voltage Level m (0 to peak)	Active Switches 6(m-1)	Clamping Diodes	DC Capacitors $(m-1)+3*(\sum_{k-1}^{m-2} k)$
3	12	0	5
4	18	0	12
5	24	0	22
6	30	0	35
7	36	0	51

Applications of Flying Capacitors Multilevel Inverter

❖ Induction motor control using DTC (Direct Torque Control) circuit

❖ Static var generation

❖ Converters with Harmonic distortion capability

1.7.3 Cascaded H-Bridge Multilevel Inverter

The cascaded H-bride multi-level inverter is to use capacitors and switches and requires less number of components in each level. This topology consists of series of power conversion cells and power can be easily scaled. The combination of capacitors and switches pair is called an H-bridge and gives the separate input DC voltage for each H-bridge. It consists of H-bridge cells and each cell can provide the three different voltages like zero, positive DC and negative DC voltages. One of the advantages of this type of multi-level inverter is that it needs less number of components compared with diode clamped and flying capacitor inverters. The price and weight of the inverter are less than those of the two inverters. Soft-switching is possible by the some of the new switching methods.

The following fig 1.7 shows the 5-level (peak to peak) cascaded H-bridge Multilevel inverter. When the switches s1, s4, s1' and s4' are turns on, we get output as 2Vdc. To get Vdc, switches s1, s4, s1' and s3' needs to be turned on. For -Vdc voltage output, s2, s3, s1' and s3' are turned on. If switches s2, s3, s2' and s3' are turned on, we get -2Vdc as the output voltage.
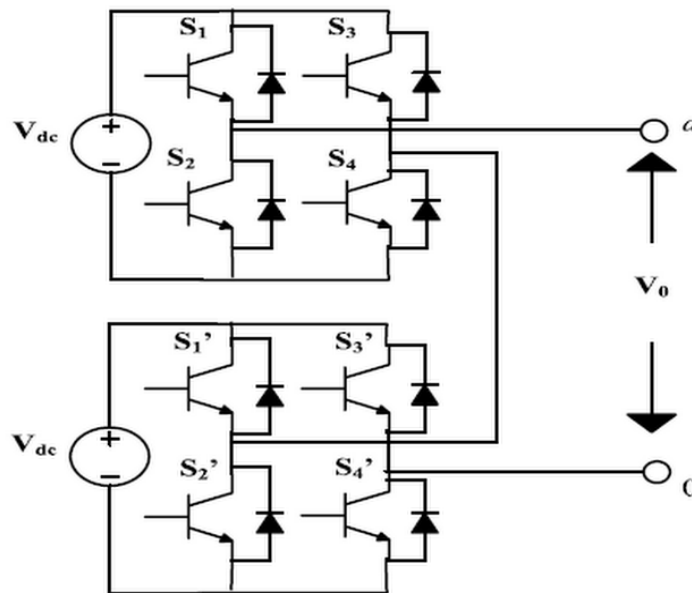

Fig 1.7 5-level cascaded H-bridge multilevel inverter

Multilevel cascade inverters are used to eliminate the bulky transformer required in case of conventional multi-phase inverters, clamping diodes required in case of diode clamped inverters and flying capacitors required in case of flying capacitor inverters. But these require large number of isolated voltages to supply each cell.

Table 1.3: Component count of cascaded H-bridge Multilevel inverter

Voltage Level m (0 to peak)	Active Switches 6(m-1)	Clamping Diodes	DC Sources
3	12	0	3
5	24	0	6
7	36	0	9
9	48	0	12

Applications of Cascaded H-Bridge Multilevel Inverter

- Motor drives
- Active filters
- Electric vehicle drives
- DC power source utilization
- Power factor compensators
- Back to back frequency link systems
- Interfacing with renewable energy resources.
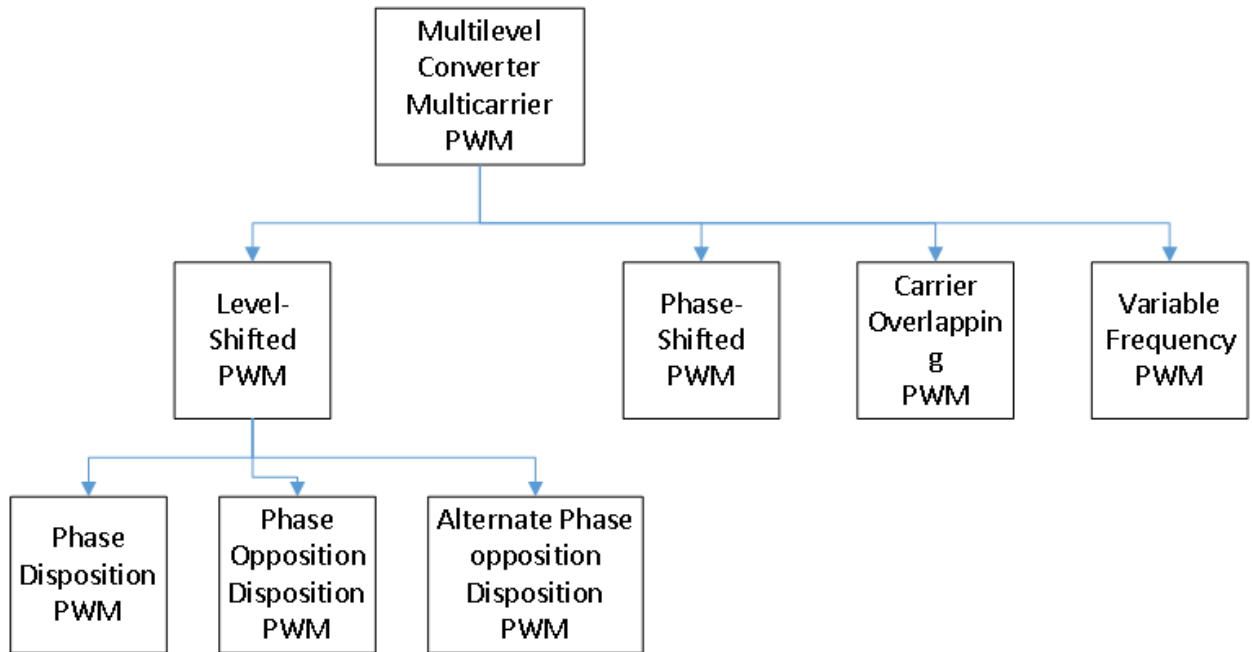
1.8 Modulation strategy

Fig1.8 Different Modulation strategies

Multicarrier PWM techniques entail the natural sampling of a single modulating or reference waveform generally being sinusoidal same as that of output frequency of the inversion system, by the use of several carries wave typically being triangular waveforms ranging in frequencies of few to several kilo hertz. There are different PWM strategies and are discussed below:

1.8.1 Phase Disposition PWM (PD)

This type of technique requires each of (m-1) carries waveforms for m level waveform, but all carries waveforms are in same phase to one another as shown in the fig 1.9(a) . The carrier wave is compared with the reference wave to produce the desired output phase voltage level. If the reference signal is higher than carrier wave, the PWM output is high (or 1) and if the reference signal is lower than carrier wave, the PWM output is low (or 0).
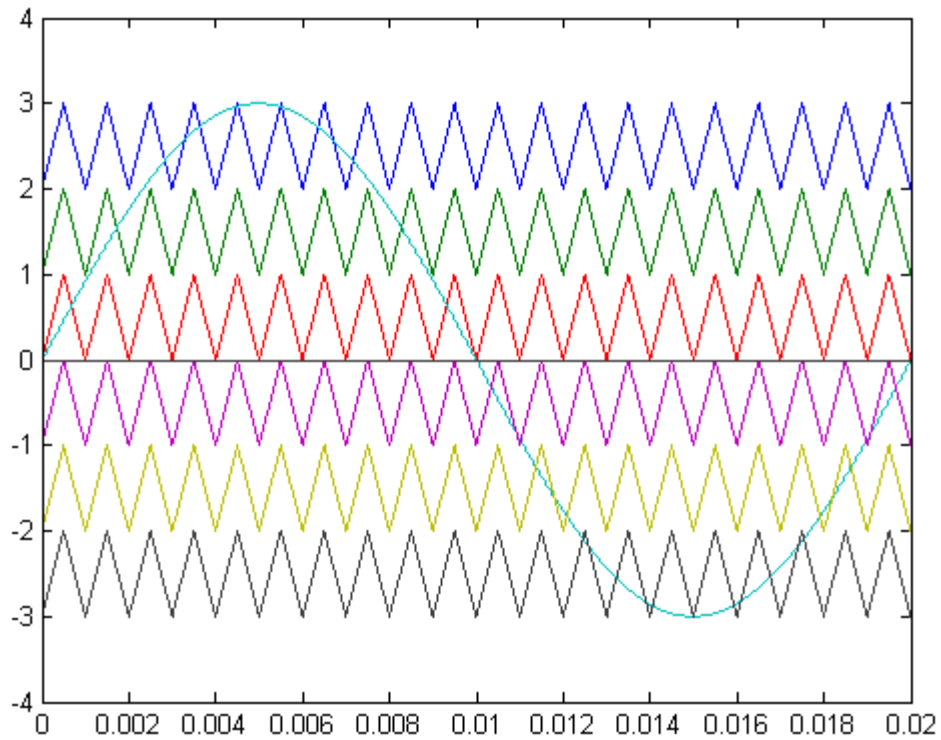
Fig1.9(a) Phase Disposition PWM

1.8.2 Phase Opposition Disposition PWM (POD)

In this technique, the carries waveforms above the zero reference are all in same phase and the carries waveforms that are below zero reference are 180^0 phase shifted between the ones above and the ones below respectively. The dominant harmonics are located around the carries frequency.
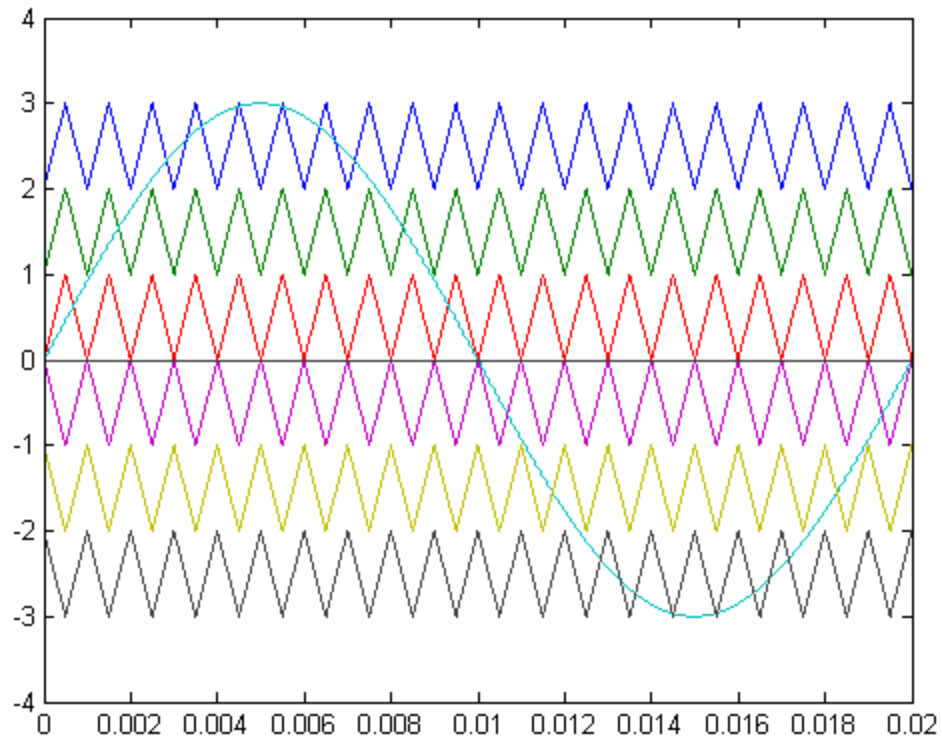
Fig 1.9(b) Phase Opposition Disposition PWM

1.8.3 Alternative Phase Opposition Disposition PWM (APOD)

This type of technique requires (m-1) carries waveforms for m level phase waveform and in this, every carrier wave is out of phase with its neighbor carrier waveform by 180^0. In this, the most dominant harmonics are centered as sidebands around the carries frequency and no harmonics occur at carries frequency. APOD technique is given in fig 1.9(c) .
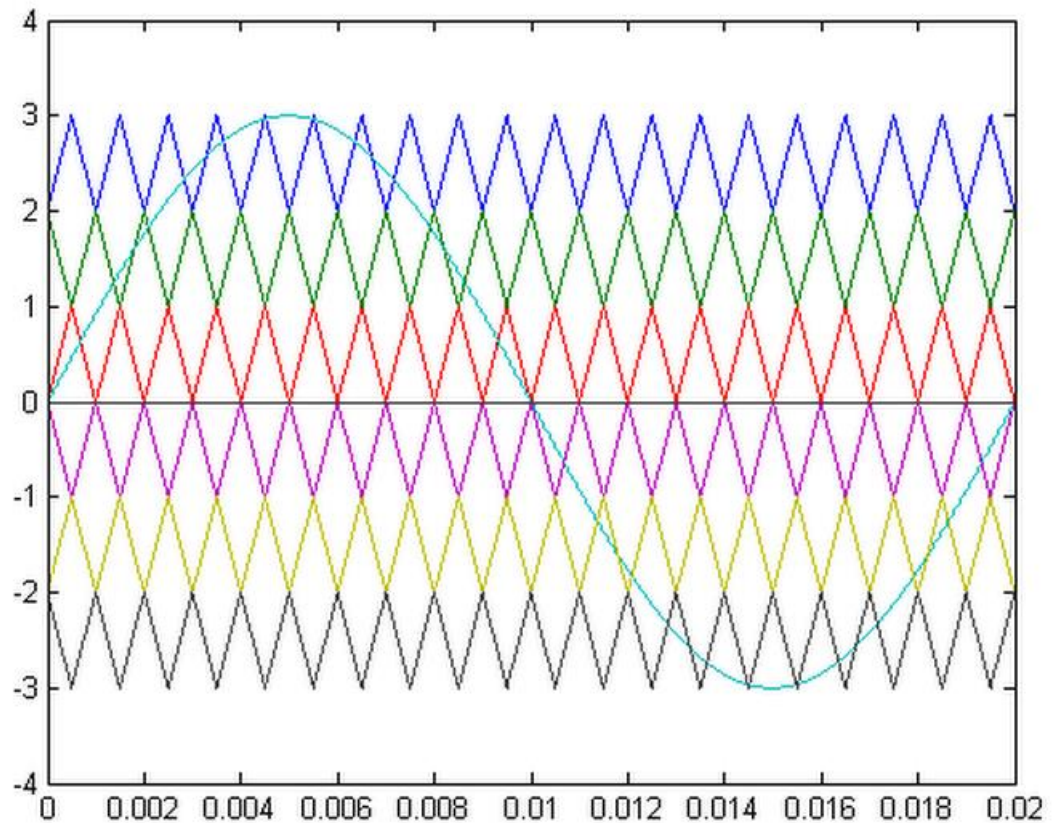
Fig 1.9(c) Alternative Phase Opposition Disposition PWM

1.8.4 Phase Shifted PWM (PS PWM)

This technique is also called hybrid PWM technique and is used to generate the stepped multilevel output voltage waveform with lower % THD. Multilevel inverter with m levels requires (m-1) triangular carriers. All the triangular carriers have same frequency and have same peak to peak amplitude. The two carriers above zero have 180^0 phase shift between them. The same is true for the two carriers below the zero. In case, the number of converter levels is higher, the carrier waves are phase shifted accordingly, that is 120^0 for a 7-level system and 90^0 for a 9-level system and so on. The dominant harmonics are concentrated around multiples of (m-1)/2 of the carrier wave frequency.
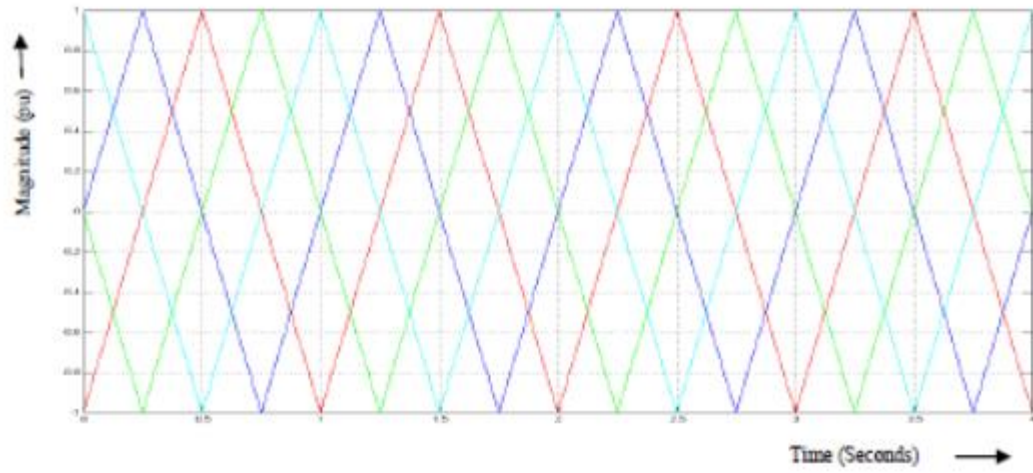
Fig 1.9(d) Phase Shifted PWM

Chapter 2

Literature Review

Saeed Ouni, Mohammad Reza Zolghadri, et al.

IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, VOL. 64, NO. 4, APRIL 2017.

In this paper, the author has focused on improvement of fault performance of cascaded H-bridge inverter by decreasing the common mode voltage. In this, an algorithm has been proposed and modified technique is proposed for the calculation of reference phase inverter voltage under faulty conditions. The simulation and experimental results are in accordance to the proposed solutions as compared to existing methods in different cases.

Krishna Kumar Gupta, Alekh Ranjan*, et al.*

IEEE TRANSACTIONS ON POWER ELECTRONICS, VOL. 31, NO. 1, JANUARY 2016

This paper presents comparison of various multilevel topologies in terms of switches used, number of sources and the various challenges which arises when an attempt is made to reduce the device count. It gives comparison of topologies, both in terms of qualitative and quantitative parameters.

Raghavendra Reddy Karasani, Vijay Bhanuji Borghate, et al.

IEEE TRANSACTIONS ON POWER ELECTRONICS, VOL. 32, NO. 2, FEB 2017

This paper presents a three-phase hybrid cascaded multilevel inverter derived from modified H bridge. The basic operation of the proposed cascaded hybrid topology is compared and explained. The topology has resulted in reduction of number of switches, voltage stress across the switch, converter cost and installation cost. The comparison and analysis is done with flying capacitor and cascaded H-bridge inverter. It can be interfaced with PV-connected system.

Soumyadeep Ray, Sushree Subhadarsini

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering, Vol. 2, Issue 9, September 2013

The performance of PV system using boost converter where switching is controlled by MPPT technique. It is connected by multilevel inverter. Paper gives the study and design of PV system connected to MLI. It uses cascaded multilevel inverter with reducing THD and discussing boost converter.

S.Subalakshmi, A.Mangaiyarkarasi, et al.

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering Vol. 3, Issue 11, November 2014

This paper provides information about using modified sinusoidal PWM (MSPWM) technique and using inductor coupled to make 5 level inverter. It uses multiple DC sources and various capacitors used in existing inverters are eliminated to reduce the problem of voltage balancing. The complete MATLAB simulation with results are given and verified in the paper.

BindeShwar Singh , Nupur MIittal, et al.

International Journal of Reviews in Computing, Vol. 10, july 31, 2012

The aim of this paper is to analyze the various topologies used in multilevel inverter and various techniques for driving the gate of the IGBT/MOSFET, in order to reduce the harmonics mainly dominant 3 harmonic. The most important topologies like diode-clamped inverter, capacitor-clamped and cascaded multilevel with a separate dc sources are discussed.

Haiwen Liu, Leon M. Tolbert, et al.

Hybrid cascaded multilevel inverter with PWM method is presented and output wave is analyzed and experimentally validated and tested using hardware. Simulated and hardware output are in accordance with the proposed idea.

Boris Reznikov, Milan Srndovic, et al.

IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, VOL. 63, NO. 6, JUNE 2016

This paper aims at addressing the calculation of THD of a single phase multilevel inverter. Along with strict mathematical solutions, simple accurate Bessel function approximation and hyperbolic average trend one are suggested. The formulas clearly reveal a single-phase PWM inverter current THD dependence on modulation index for an arbitrary voltage level count and are easily modified to cover grid-connected cases.

C. Bharatiraja, Harshavardhan Reddy, et al.

International Journal of Power Electronics and Drive System (IJPEDS), Vol. 7, No. 2, June 2016,

This paper proposes a new Asymmetrical multilevel inverter topology with reduced number of switches. This topology is superior to the existing multilevel inverter (MLI) configurations in terms of lower total harmonic distortion (THD) value and lower cost. The proposed topology uses a novel pulse width modulation (PWM) technique to control the gating pulses. It is simulated in MATLAB Simulink and the results are validated through FPGA spartan 3 based hardware. It produces 7 level output. The circuit complexity is drastically reduced and it is suitable for medium and high power applications. THD for the output is quite low when compared with the conventional inverter.

Young-Seok Kim, Beom-Seok Seo, et al.

In this paper, author clarified a dynamic exchanging attributes of every power semiconductor gadgets and a few issues of MLI like voltage unbalance between DC-interface capacitors and over voltages over the exchanging gadgets. The above specify issues taken and they proposed another MLI with PWM inverter. They demonstrates the investigation of new three level inverter.

Poh Chiang Loh, Donald Grahame Holmes, et al.

Multilevel inverter that produce more than two levels of voltage to get the yield nearer to sine wave and less twisted air conditioning to dc, dc to air conditioning, and dc to dc control transformation, have pulled in numerous patrons. In paper [12] Peng and Fang Zheng are proposed a summed up model of multi-level converter with self-voltage adjusting. From this summed up inverter topology we can infer the customary unbiased point diode clipped and flying capacitor multilevel inverters. Likewise this summed up multi-level converter topology gives another multilevel structure that can control the every dc-voltage level naturally with no help from other converter structures circuits. Numerous new multilevel converter topologies can be gets from this proposed summed up multilevel inverter structure. Additionally some application cases of the summed up multilevel converter are likewise introduced in this paper.

Youhei Hinago, and Hirotaka Koizumi, et al.

It comprises of a H-connect and an inverter which yields multilevel voltage by exchanging the dc voltage sources in arrangement and in parallel. The proposed inverter can yield more quantities of voltage levels in a similar number of exchanging gadgets by utilizing this transformation. The quantity of door driving circuits is decreased, which prompts to the

diminishment of the size and power utilization in the driving circuits. The aggregate consonant of the yield waveform is additionally lessened. The proposed inverter is driven by the half breed regulation strategy. In this paper, the circuit arrangement, hypothetical operation, Fourier investigation, reproduction comes about with MATLAB/SIMULINK, and test results are appeared.

Prof. Dr. P. K. Sataya Moorthy , et al.

Inspected topology of fell multilevel inverter utilizing a decreased number of switches is proposed. The new topology has the benefit of diminished number gadgets contrasted with customary setups and can be reached out to any number of levels. This topology brings about lessening of establishment zone, cost, computational time and has effortlessness of control framework. This structure comprises of arrangement associated submultilevel inverter squares. The GA procedure finds the ideal arrangement set of exchanging edges.

Varsha Sahu, Shraddha Kaushik, et al.

It outline a model for new five level diode braced multi-level inverter with less number of switches and diodes. In these sort converters, each of the data sources and yields can single-stage air conditioning, or multiphase air conditioning; dc, that is the reason, they are valuable in dc to dc, dc to air conditioning, air conditioning to dc, or air conditioning to air conditioning power transformation frameworks. The fractional full converters (delicate exchanging air conditioning join widespread power converters) are solid, minimized, and longer lifetime as contrast with other customary converters. In any case, traditional converters need more number of switches, which is unpredictable to control. This paper proposed a novel altered approach, which can additionally minimize the no. of switches without changing the working standard. This proposed converter, which is called as ultrasparse air conditioning join buck–boost converter, minimizes the no. of changes from 24 to 16, in a 3-stage air conditioning to air conditioning case, and diminishes the no. of changes from 20 to 10, in a dc to 3-stage air conditioning structure. This ultrasparse converters are adoptable to frameworks with unidirectional stream of current and power, i.e. photograph voltaic cells (PV cells) and wind control era frameworks.

Chapter 3

Enhanced MLI Topology

Problem formulation

Research motivation

Objectives

Multilevel Inverter Design

3.1 Problem formulation

In this section, some problems are formulated while designing the multilevel inverter and to improve various characteristics like number of steps, voltage balancing, total harmonic distortion etc. and various challenges faced by existing and proposed techniques.

3.2 Research Motivation

Renewable energy has become gained much importance in the recent years and there is a lot of research and potential in renewable energy sources especially in solar panel and wind energy generation systems and their connectivity with grid. They are no longer operated as isolated and for low power applications but now they are grid connected and with increased proportion of electrical energy generation from them. The output of either renewable energy source is dependent on various factors and are uncontrolled and needs to be connected to grid and requires pure sine wave having very less total harmonic distortion, voltage imbalance and frequency mismatch. This thesis aims at design of multi-level inverter and applying various techniques and design to eliminate the harmonics. The selection of type of multilevel inverter and the topology used plays an important role in its performance. The main motive is to reduce cost of inverter for economic benefits and to make it affordable to be used in various places by reducing the number of switches used and the number of isolated DC sources required.

3.3 Objectives

The approach to the proposed multilevel inverter can be briefly summarized below:

1. To design an improved topology of inverter in MATLAB (Simulink) for reduced harmonics.
2. To design gate driver circuit and logic for driving IGBT/MOSFET.
3. To reduce the total number of semiconductor switches used so as to reduce the overall cost of inverter.
4. To reduce the total number of voltage source required for operation.
5. To compare the performance of inverter in terms of total harmonic distortion (THD), and voltage imbalance that occurs.

So, most of the problems above said can be eliminated or reduced by below mentioned methodologies.

3.4 Multilevel Inverter Design

In order to reduce the THD of the output voltage, new topology has been designed. 31 level (peak to peak) and 63 level (peak to peak) inverter has been discussed following:
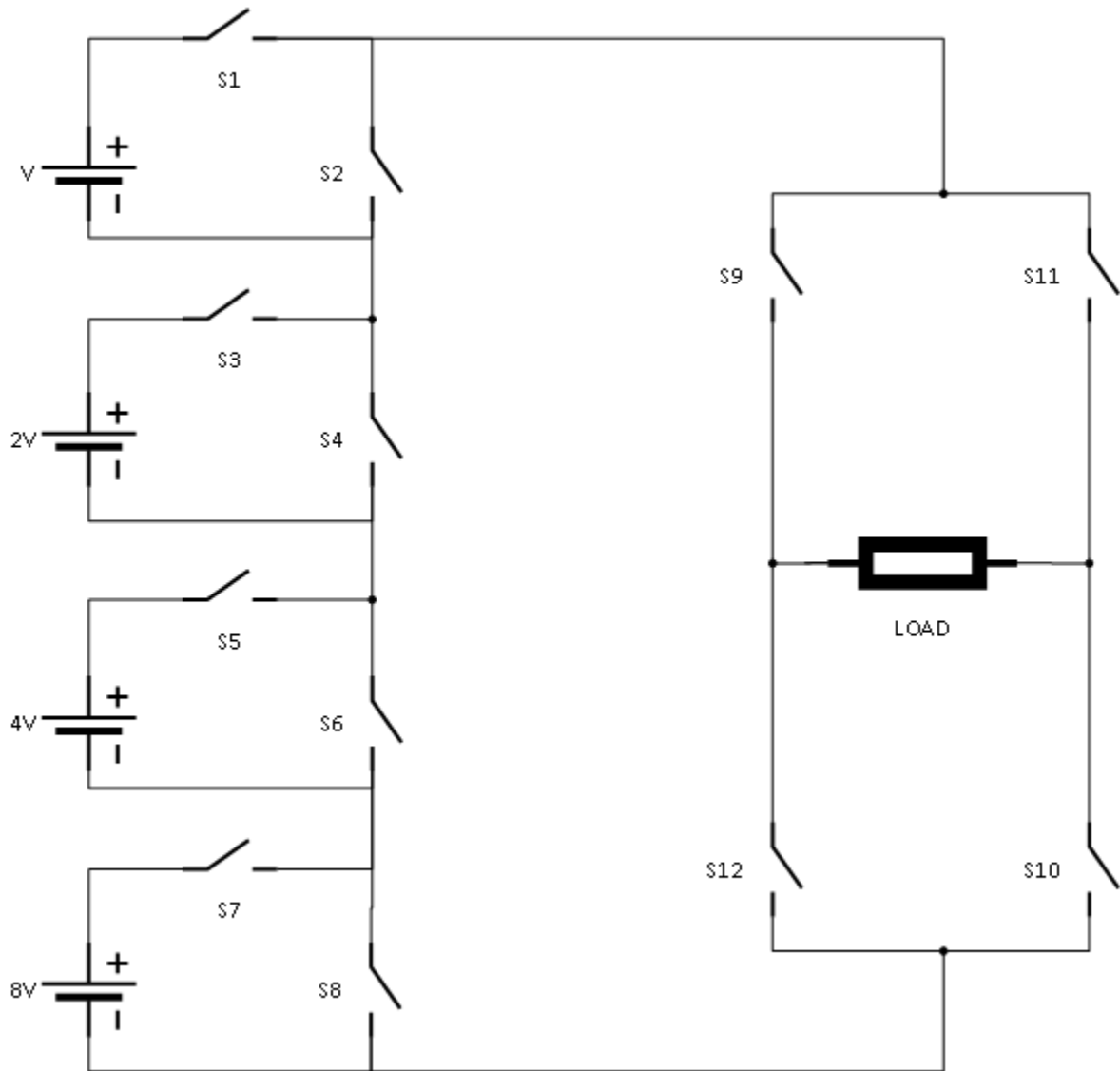
The 31-level configuration

Fig 3.1 Basic structure of 31-level inverter

This configuration produces single phase 31 level output of voltage by using only 12 switches and four DC sources at input side. A single DC source outputs only two voltage levels either 0 or V. as the number of voltage source goes on increasing, the output levels increases. One part in this configuration is called level generation part and it is responsible

for level generation. It uses 8 switches named s1, s2, s3, s4, s5, s6, s7 and s8. The other part is known as polarity generation and it is responsible for generating correct polarity of the output voltage. It uses switches named s9, s10, s11 and s12. Switches s1 to s8 is used to connect four DC sources to load, one at a times or in series combination according to the voltage level required. The DC voltage is split into each cell and these are connected in series and desired number of level can be achieved by series connection of sources with the help of switches.

Operation of the improved topology

Operation of the topology with 31 level MLI with asymmetrical cascaded configuration can be explained with the help of fig and its switching sequence in fig . When the switches s1, s3, s5 and s7 are turned "on", the output voltage will be "180 V" (i.e., level 15). The output voltage will be "168 V" (i.e., level 14) when switches s3, s5, and s7 are turned "on". When the switches s1, s5 and s7 are turned "on", the output voltage will be "156 V" (i.e., level 13). When the switches s5 and s7 are turned "on", the output voltage will be "144 V" (i.e., level 12). When the switches s1, s3 and s7 are turned "on", the output voltage will be "132 V" (i.e., level 11). When the switches s3 and s7 are turned "on", the output voltage will be "120 V" (i.e., level 10). When the switches s1 and s7 are turned "on", the output voltage will be "108 V" (i.e., level 9). When the switches s7 are turned "on", the output voltage will be "96 V" (i.e., level 8). When the switches s1, s3 and s5 are turned "on", the output voltage will be "84 V" (i.e., level 7). When the switches s3 and s5 are turned "on", the output voltage will be "72 V" (i.e., level 6). When the switches s1 and s5 are turned "on", the output voltage will be "60 V" (i.e., level 5). When the switches s5 are turned "on", the output voltage will be "48 V" (i.e., level 4). When the switches s1 and s3 are turned "on", the output voltage will be "36 V" (i.e., level 3). When the switches s3 are turned "on", the output voltage will be "24 V" (i.e., level 2). When the switches s1 are turned "on", the output voltage will be "12 V" (i.e., level 1). When the switches s2, s,4, s6 and s8 are turned "on", the output voltage is zero (i.e., 0 level).
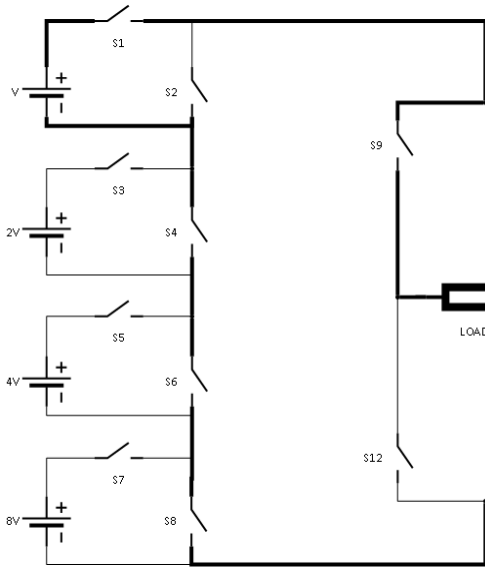
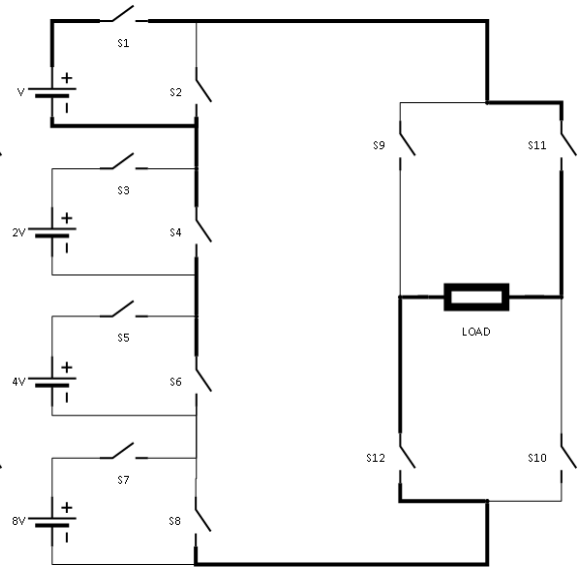Fig 3.2(a) Level 1   Fig 3.2(b) Level-1
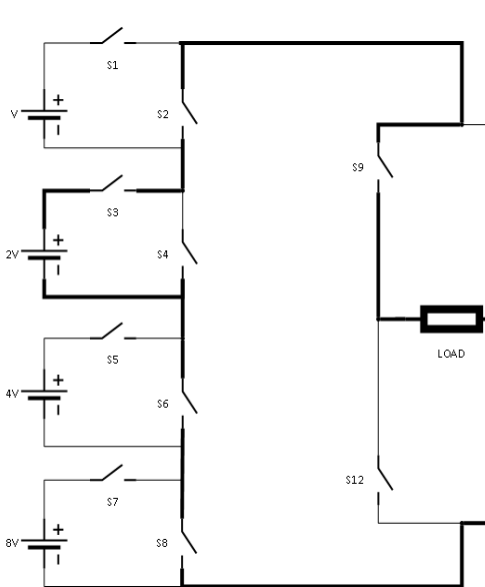

Fig 3.2(c) Level 2   Fig 3.2(d) Level-2
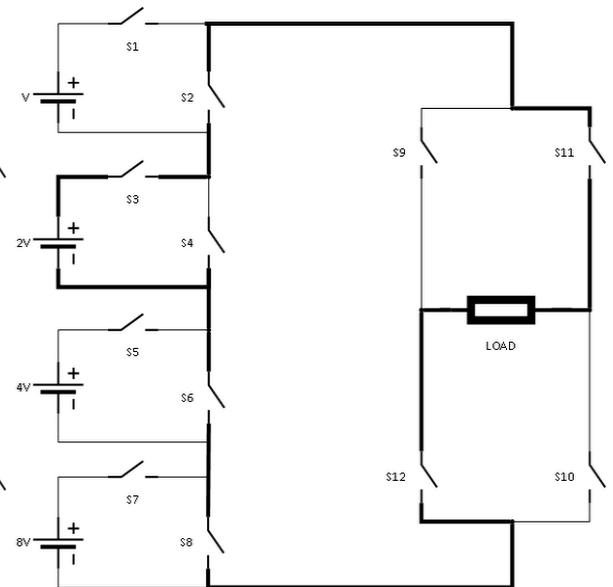
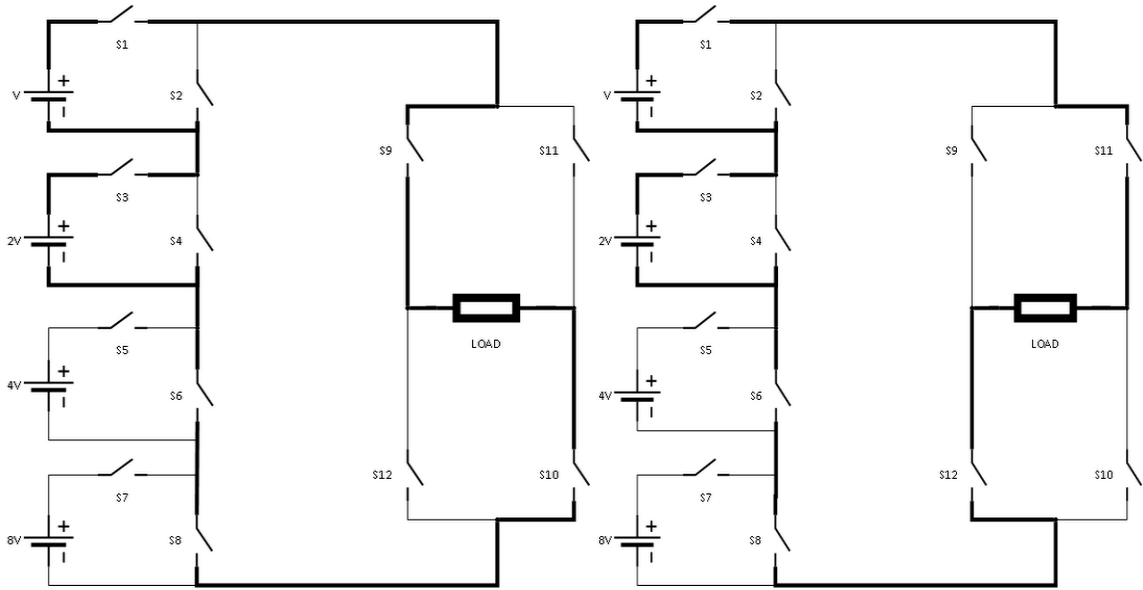Fig 3.2(e) Level 3   Fig 3.2(f) Level-3
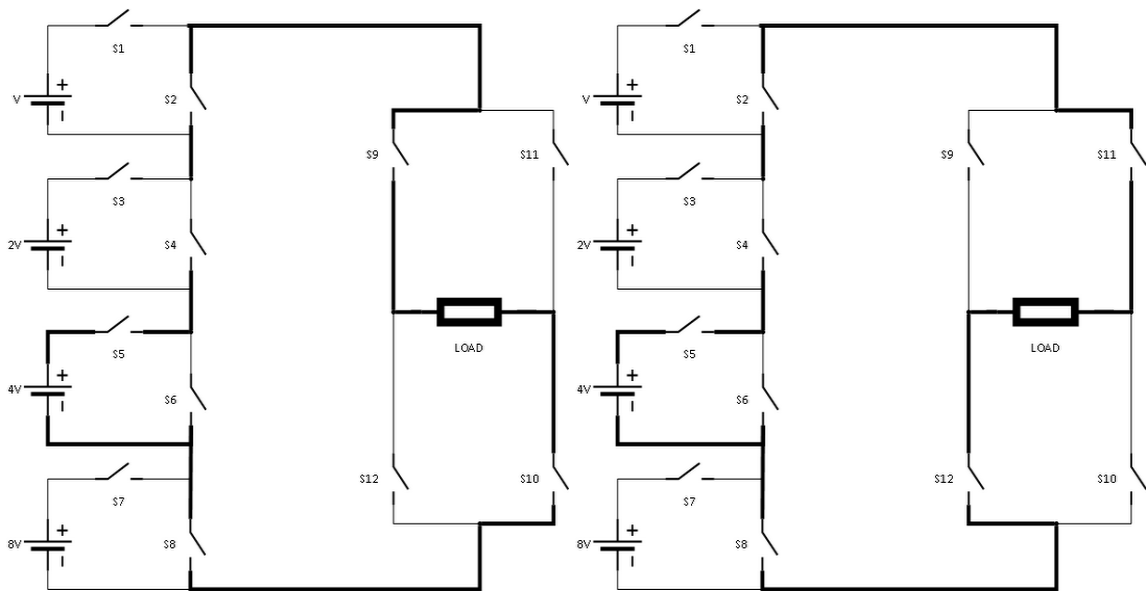

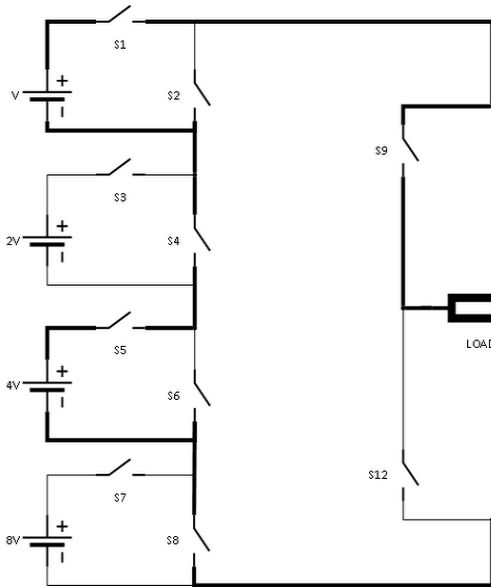Fig 3.2(g) Level 4   Fig 3.2(h) Level-4
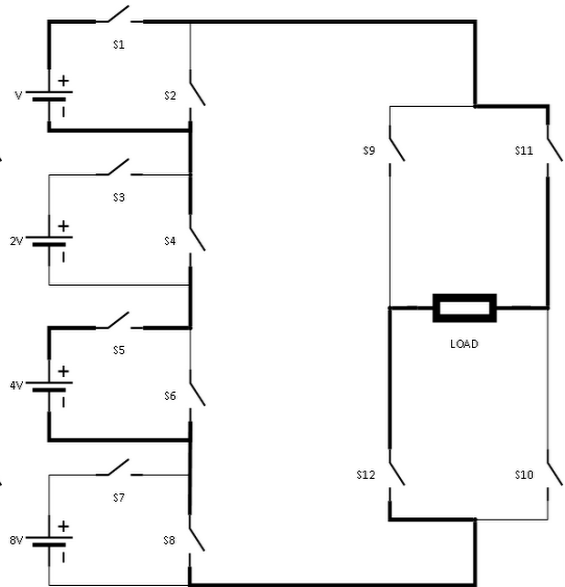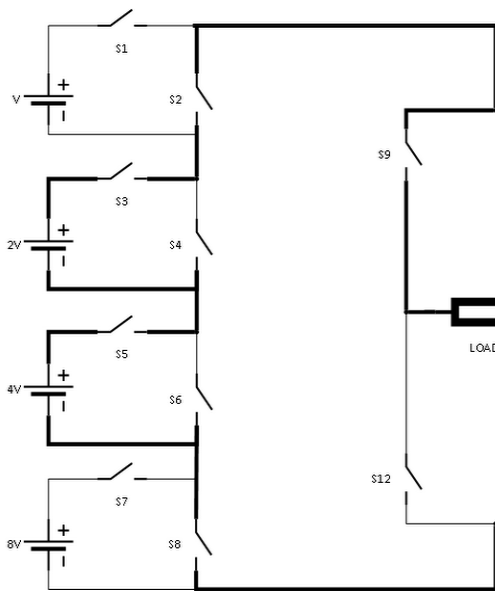
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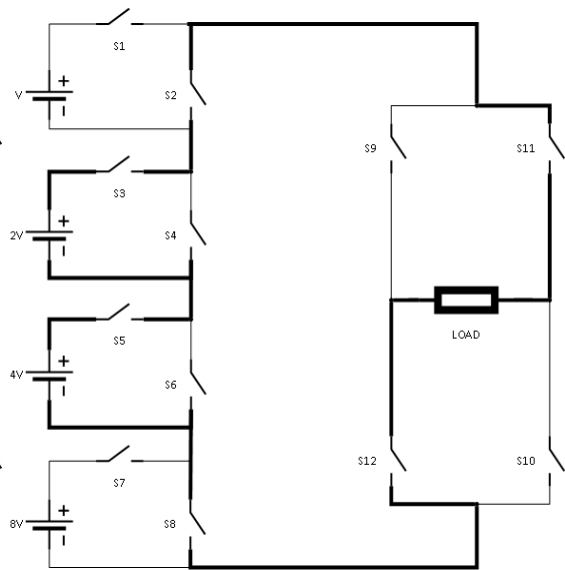

Fig 3.2(j) Level-5
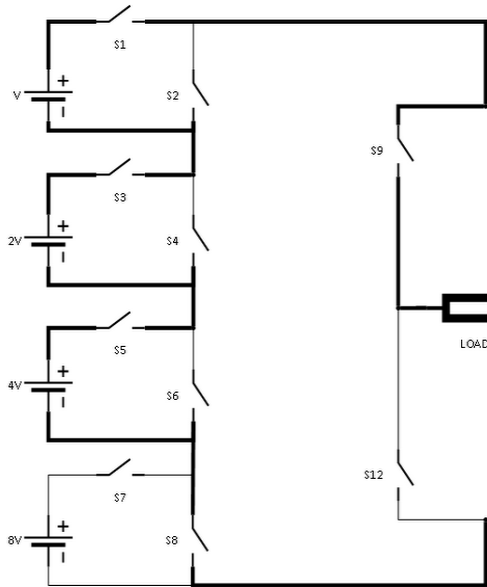

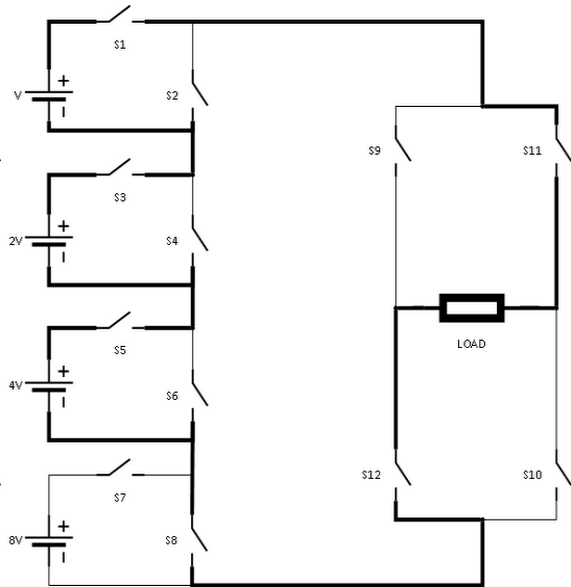
Fig 3.2(k) Level 6

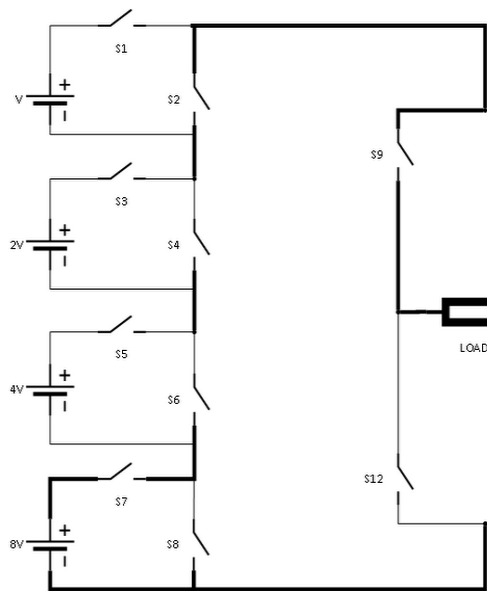Fig 3.2(l) Level-6

Fig 3.2(m) Level 7
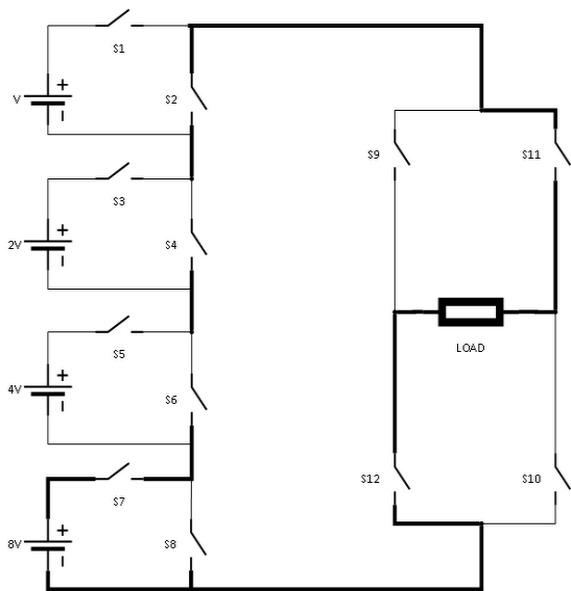

Fig 3.2(n) Level-7

Fig 3.2(o) Level 8

Fig 3.2(p) Level-8
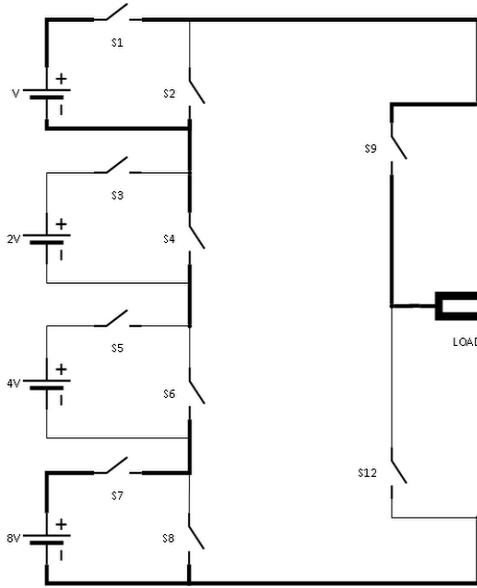
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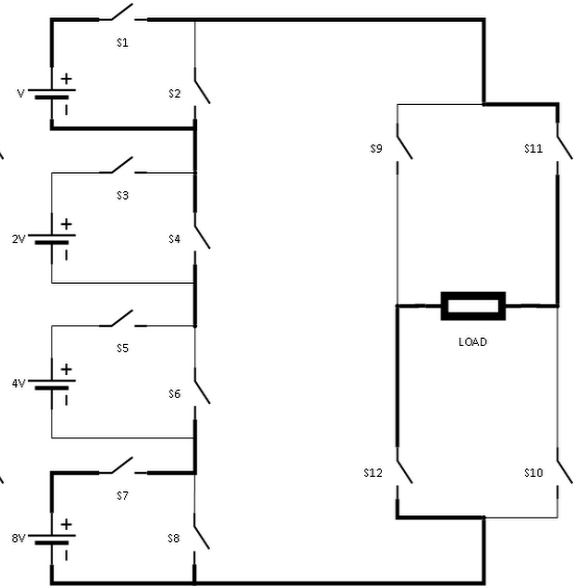
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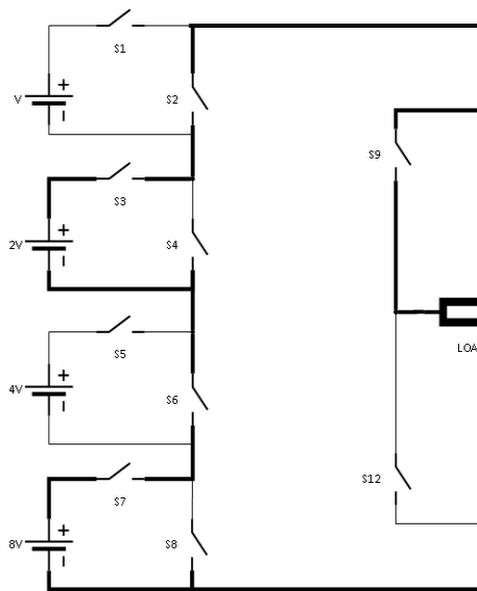
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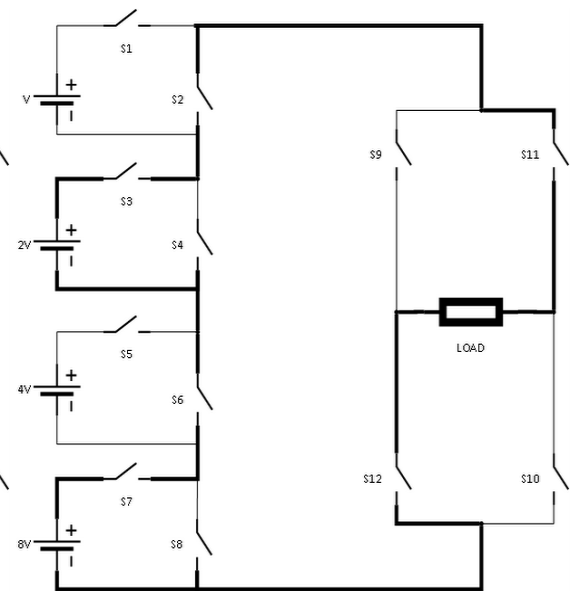
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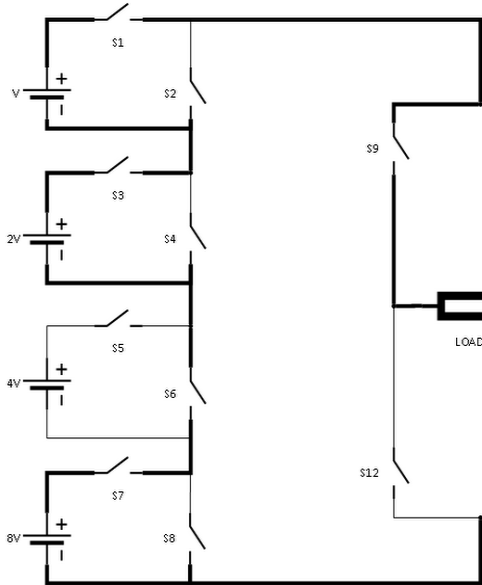
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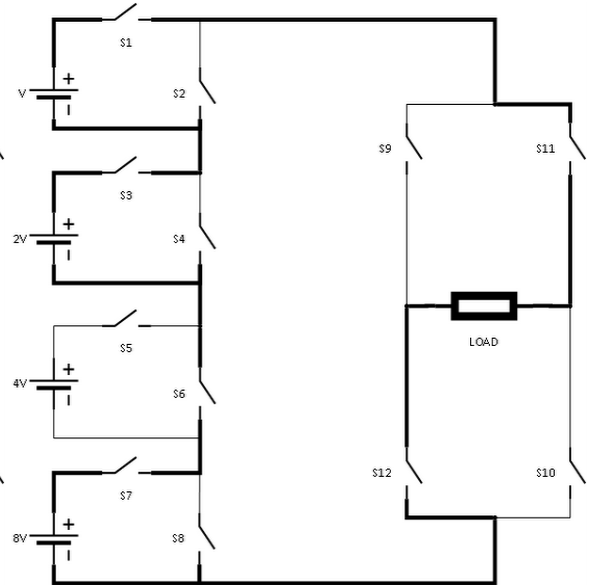
Fig 3.2(v) Level-11
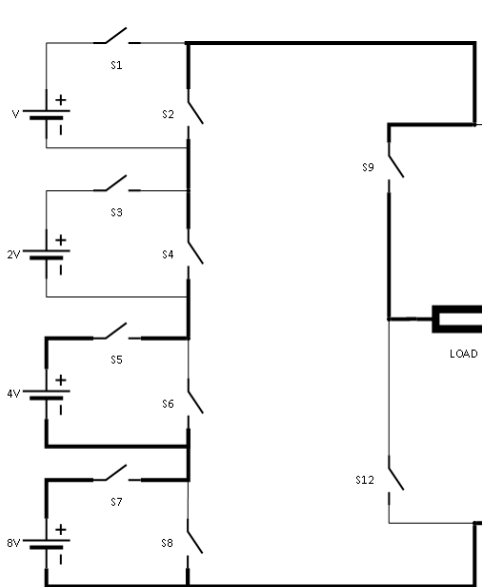
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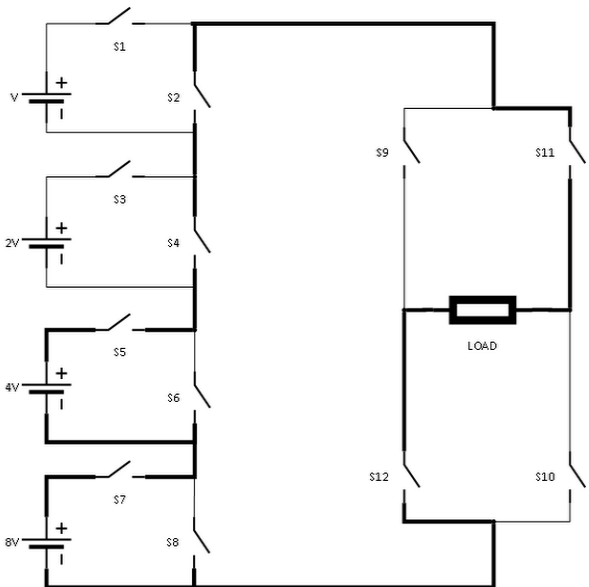
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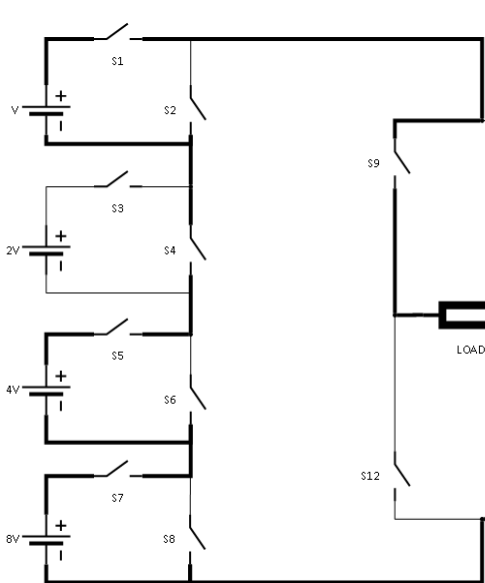
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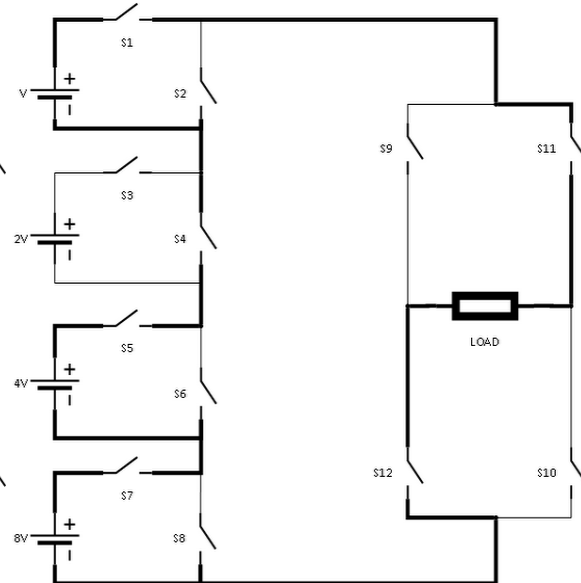
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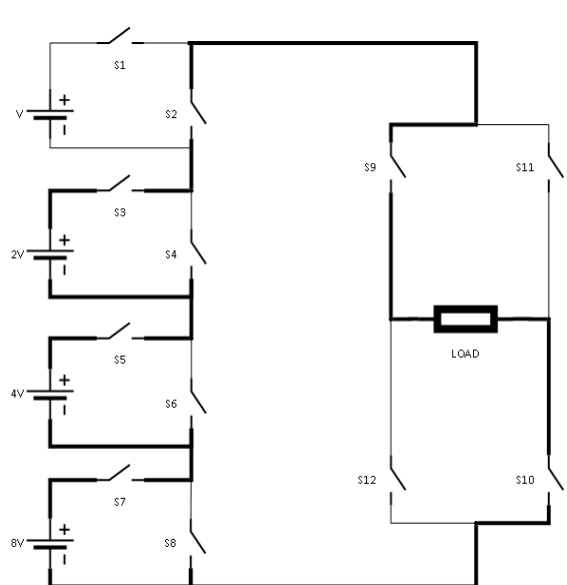
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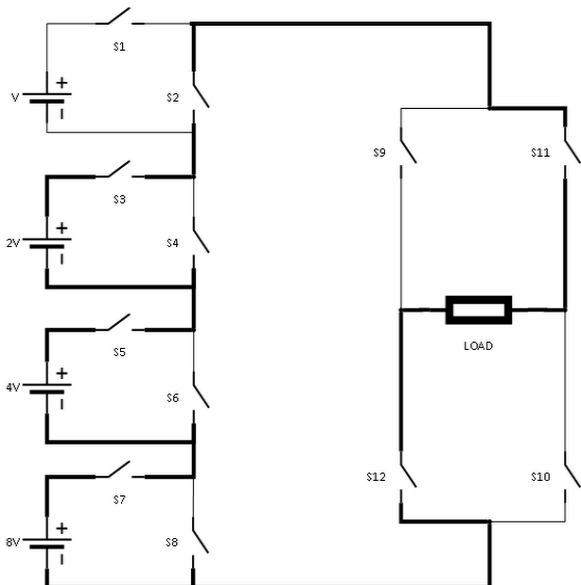
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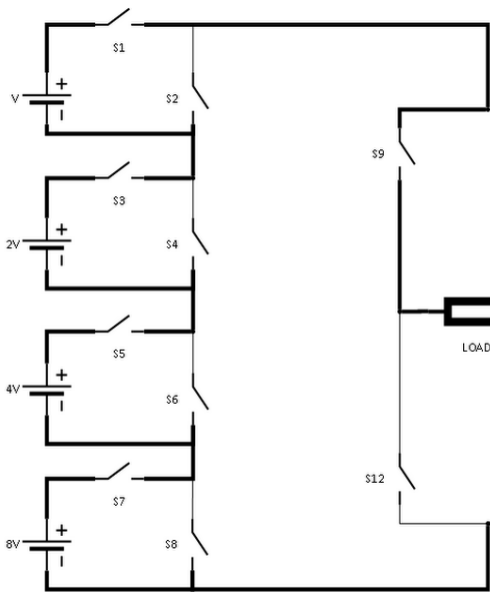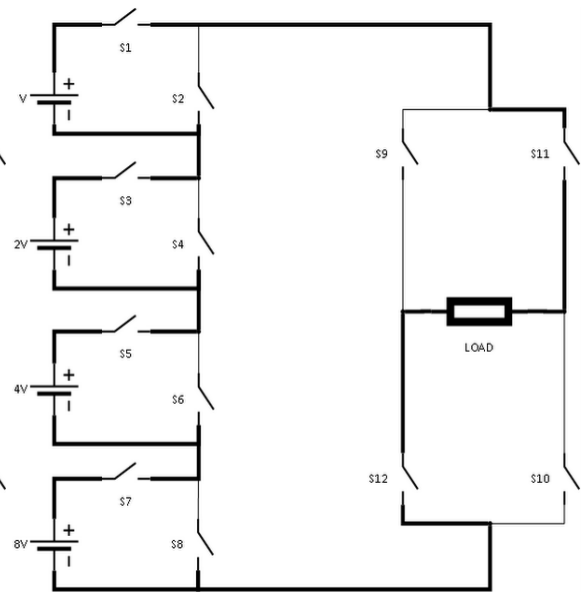
Fig 3.2(a3) Level 15   Fig 3.2(a4) Level-15
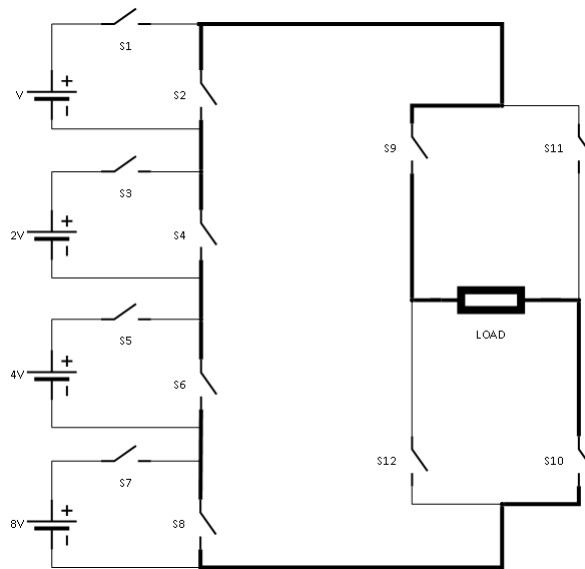
Fig(a5) Level 0

Switches s9, s10, s11 and s12 are complementary switches and are used for voltage reversal. When s9 and s10 are together turned "on", positive half cycle (level: +1,+2,+3 and so on) is obtained whereas when s11 and s12 are together turns "on", negative half cycle (level: -1,-2,-3 and so on) is obtained across the load connected.

Table 3.1: Switching sequence of 31-level inverter

Voltage Level	SWITCHING STATE												Output Voltage
	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	
+15	1	0	1	0	1	0	1	0	1	1	0	0	180 V
+14	0	1	1	0	1	0	1	0	1	1	0	0	168 V
+13	1	0	0	1	1	0	1	0	1	1	0	0	156 V
+12	0	1	0	1	1	0	1	0	1	1	0	0	144 V
+11	1	0	1	0	0	1	1	0	1	1	0	0	132 V
+10	0	1	1	0	0	1	1	0	1	1	0	0	120 V
+9	1	0	0	1	0	1	1	0	1	1	0	0	108 V
+8	0	1	0	1	0	1	1	0	1	1	0	0	96 V
+7	1	0	1	0	1	0	0	1	1	1	0	0	84 V
+6	0	1	1	0	1	0	0	1	1	1	0	0	72 V
+5	1	0	0	1	1	0	0	1	1	1	0	0	60 V
+4	0	1	0	1	1	0	0	1	1	1	0	0	48 V
+3	1	0	1	0	0	1	0	1	1	1	0	0	36 V
+2	0	1	1	0	0	1	0	1	1	1	0	0	24 V
+1	1	0	0	1	0	1	0	1	1	1	0	0	12 V
0	0	1	0	1	0	1	0	1	1	1	0	0	0 V
-1	1	0	0	1	0	1	0	1	0	0	1	1	-12 V
-2	0	1	1	0	0	1	0	1	0	0	1	1	-24 V
-3	1	0	1	0	0	1	0	1	0	0	1	1	-36 V
-4	0	1	0	1	1	0	0	1	0	0	1	1	-48 V
-5	1	0	0	1	1	0	0	1	0	0	1	1	-60 V
-6	0	1	1	0	1	0	0	1	0	0	1	1	-72 V
-7	1	0	1	0	1	0	0	1	0	0	1	1	-84 V
-8	0	1	0	1	0	1	1	0	0	0	1	1	-96 V
-9	1	0	0	1	0	1	1	0	0	0	1	1	-108 V
-10	0	1	1	0	0	1	1	0	0	0	1	1	-120 V
-11	1	0	1	0	0	1	1	0	0	0	1	1	-132 V

-12	0	1	0	1	1	0	1	0	0	0	1	1	-144 V
-13	1	0	0	1	1	0	1	0	0	0	1	1	-156 V
-14	0	1	1	0	1	0	1	0	0	0	1	1	-168 V
-15	1	0	1	0	1	0	1	0	0	0	1	1	-180 V

The 63-level (peak to peak) inverter configuration is given in fig:

Fig 3.3 Basic structure of 63-level inverter

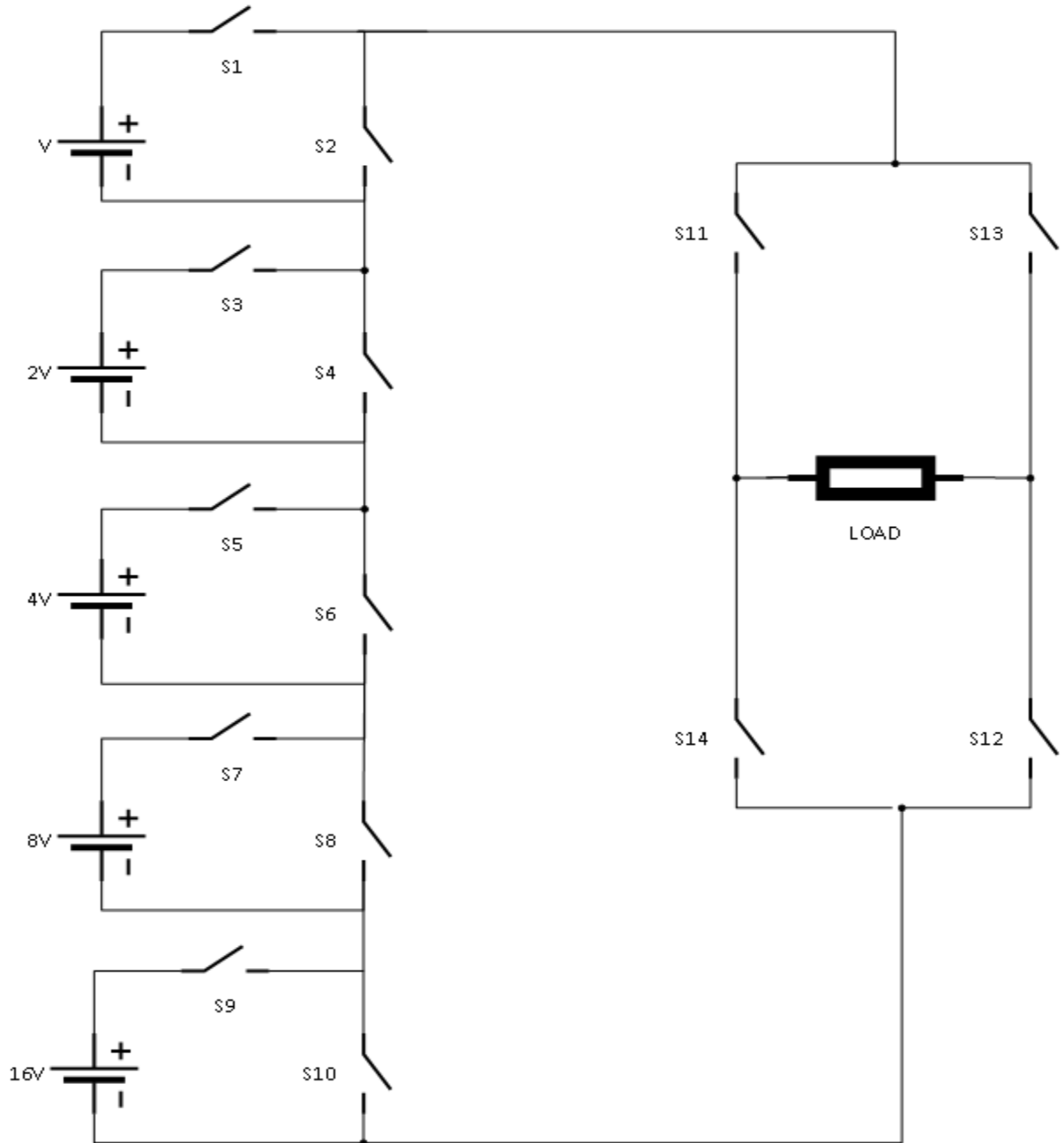This configuration produces single phase 63 level output of voltage by using only 14 switches and five DC sources at input side. With just increase of only one source and two switches, the output levels and the output voltage greatly increases. One part in this configuration is called level generation part and it is responsible for level generation. It uses 10 switches named s1, s2, s3, s4, s5, s6, s7, s8, s9 and s10. The other part is known as polarity generation and it is responsible for generating correct polarity of the output voltage. It uses switches named s11, s12, s13 and s14. Switches s1 to s10 is used to connect five DC sources to load, one at a times or in series combination according to the voltage level required.

Operation of the improved topology

Operation of the topology with 63 level MLI with asymmetrical cascaded configuration can be easily explained with the help of fig 3.3 and its switching sequence in Table 3.1 . When the switches s1, s3, s5, s7 and s9 are turned "on", the output voltage will be "372 V" (i.e., level 31). The output voltage will be "360 V" (i.e., level 30) when switches s3, s5, s7 and s9 are turned "on". When the switches s1, s5, s7 and s9 are turned "on", the output voltage will be "348 V" (i.e., level 29). When the switches s5, s7 and s9 are turned "on", the output voltage will be "336 V" (i.e., level 28). When the switches s1, s3, s7 and s9 are turned "on", the output voltage will be "324 V" (i.e., level 27). When the switches s3, s7 and s9 are turned "on", the output voltage will be "312 V" (i.e., level 26). When the switches s1, s7 and s9 are turned "on", the output voltage will be "300 V" (i.e., level 25). When the switches s7 and s9 are turned "on", the output voltage will be "288 V" (i.e., level 24). When the switches s1, s3, s5 and s9 are turned "on", the output voltage will be "276 V" (i.e., level 23). When the switches s3, s5 and s9 are turned "on", the output voltage will be "264 V" (i.e., level 22). When the switches s1, s3 and s9 are turned "on", the output voltage will be "252 V" (i.e., level 21). When the switches s5 and s9 are turned "on", the output voltage will be "240 V" (i.e., level 20). When the switches s1, s3 and s9 are turned "on", the output voltage will be "228 V" (i.e., level 19). When the switches s3 and s9 are turned "on", the output voltage will be "216 V" (i.e., level 18). When the switches s1 and s9 are turned "on", the output voltage will be "204 V" (i.e., level 17). When the switches

s9 are turned "on", the output voltage will be "192 V" (i.e., 16 level). When the switches s1, s3, s5 and s7 are turned "on", the output voltage will be "180 V" (i.e., level 15). When the switches s3, s5 and s7 are turned "on", the output voltage will be "168 V" (i.e., level 14). When the switches s1, s5 and s7 are turned "on", the output voltage will be "156 V" (i.e., level 13). When the switches s5 and s7 are turned "on", the output voltage will be "144 V" (i.e., level 12). When the switches s1, s3 and s7 are turned "on", the output voltage will be "132 V" (i.e., level 11). When the switches s3 and s7 are turned "on", the output voltage will be "120 V" (i.e., level 10). When the switches s1 and s7 are turned "on", the output voltage will be "108 V" (i.e., level 9). When the switches s1, s3 and s9 are turned "on", the output voltage will be "96 V" (i.e., level 8). When the switches s1, s3 and s5 are turned "on", the output voltage will be "84 V" (i.e., level 7). When the switches s3 and s5 are turned "on", the output voltage will be "72 V" (i.e., level 6). When the switches s1 and s5 are turned "on", the output voltage will be "60 V" (i.e., level 5). When the switches s5 are turned "on", the output voltage will be "48 V" (i.e., level 4). When the switches s1 and s3 are turned "on", the output voltage will be "36 V" (i.e., level 3). When the switches s3 are turned "on", the output voltage will be "24 V" (i.e., level 2). When the switches s1 are turned "on", the output voltage will be "12 V" (i.e., level 1). When the switches s2, s,4, s6 and s8 are turned "on", the output voltage is zero (i.e., 0 level).
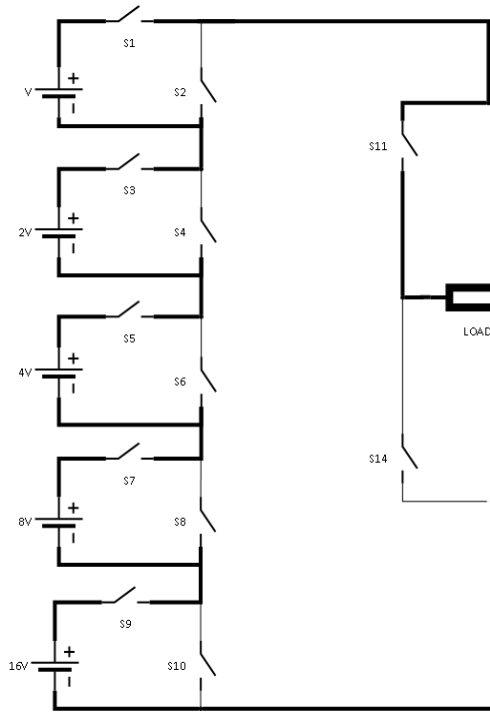
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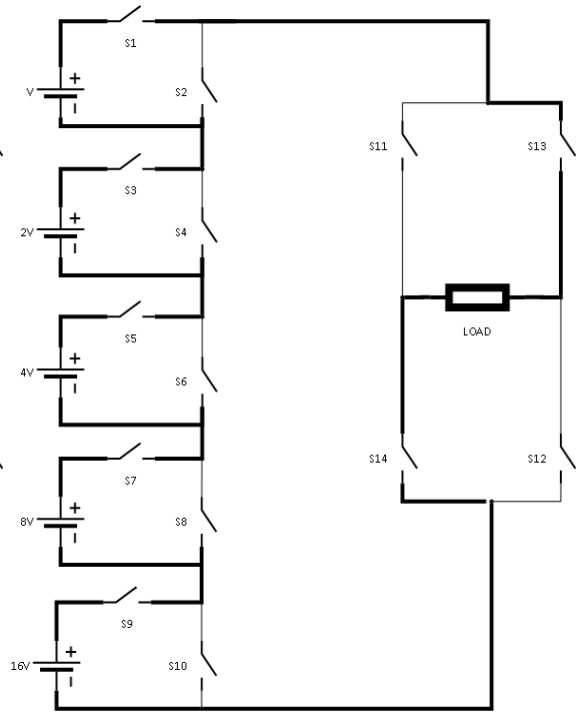
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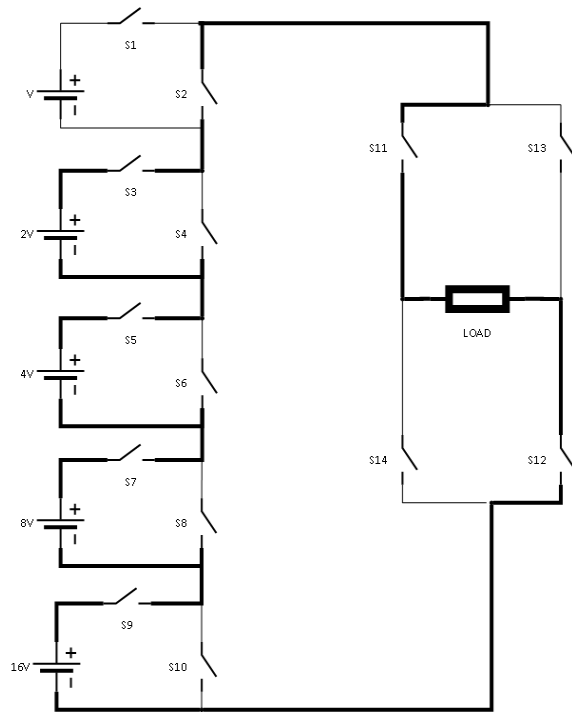
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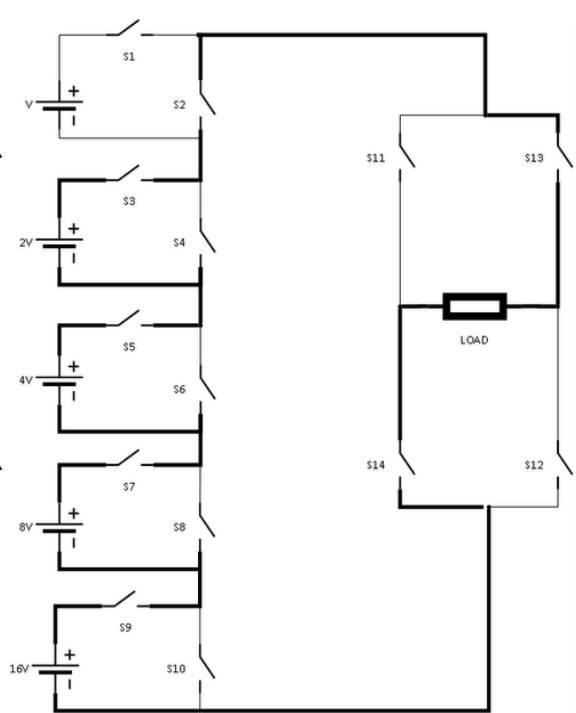
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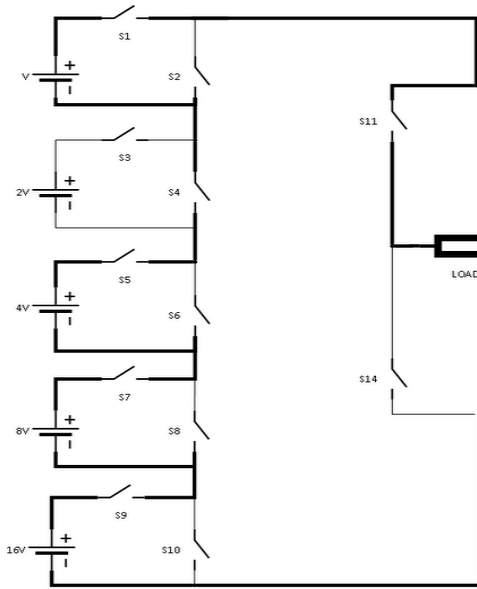
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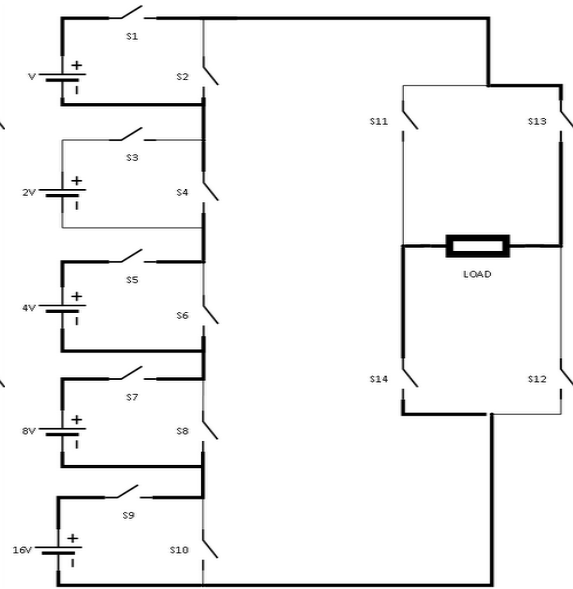
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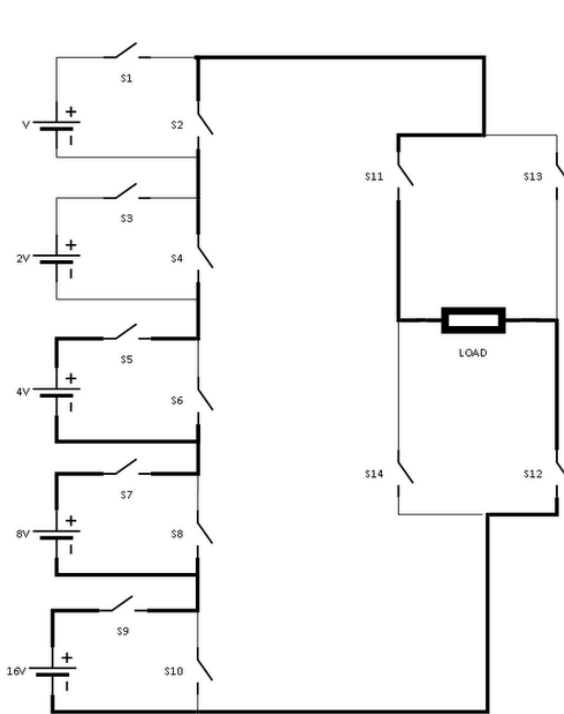
Fig 3.4(g) Level 28
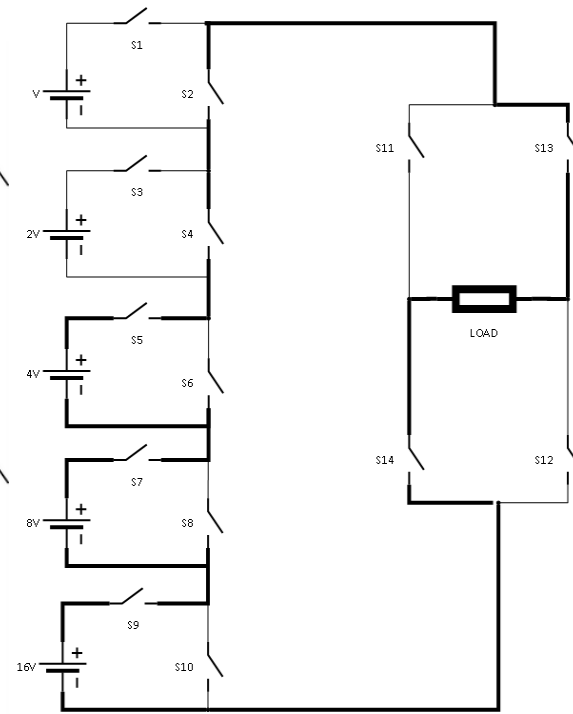
Fig 3.4(h) Level-28
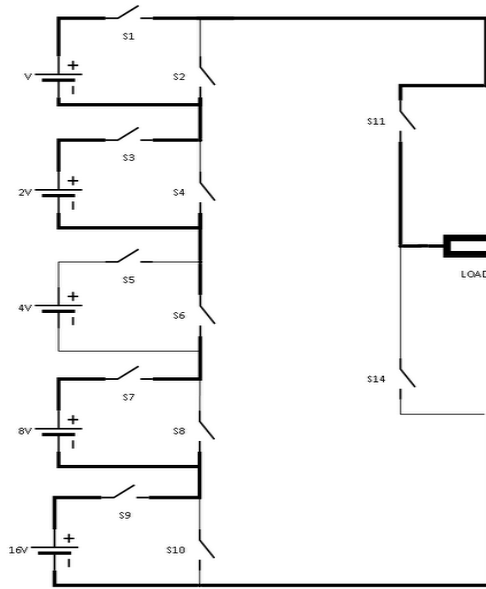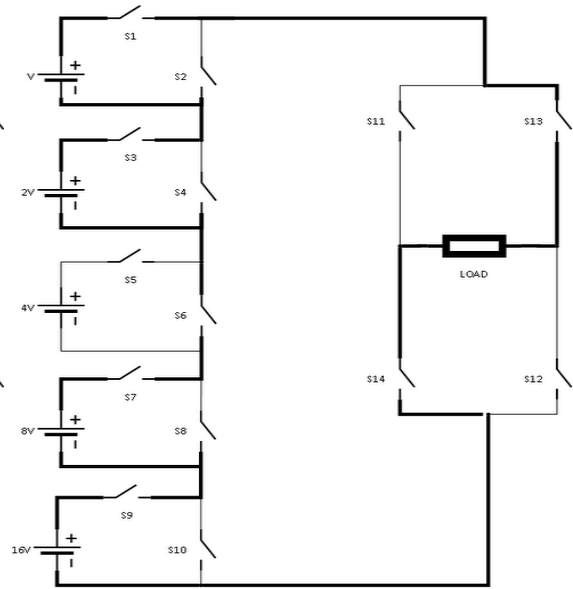
Fig 3.4(i) Level 27   Fig 3.4(j) Level-27

Switches s10, s11, s13 and s14 are complementary switches and are used for voltage reversal. When s11 and s12 are together turned "on", positive half cycle (level: +1,+2,+3 and so on) is obtained whereas when s13 and s14 are together turns "on", negative half cycle (level: -1,-2,-3 and so on) is obtained across the load connected.

Table 3.1: Switching sequence of 63-level inverter

Voltage Level	SWITCHING STATE														Output Voltage
	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	
+31	1	0	1	0	1	0	1	0	1	0	1	1	0	0	372 V
+30	0	1	1	0	1	0	1	0	1	0	1	1	0	0	360 V
+29	1	0	0	1	1	0	1	0	1	0	1	1	0	0	348 V
+28	0	1	0	1	1	0	1	0	1	0	1	1	0	0	336 V

+27	1	0	1	0	0	1	1	0	1	0	1	1	0	0	324 V
+26	0	1	1	0	0	1	1	0	1	0	1	1	0	0	312 V
+25	1	0	0	1	0	1	1	0	1	0	1	1	0	0	300 V
+24	0	1	0	1	0	1	1	0	1	0	1	1	0	0	288 V
+23	1	0	1	0	1	0	0	1	1	0	1	1	0	0	276 V
+22	0	1	1	0	1	0	0	1	1	0	1	1	0	0	264 V
+21	1	0	0	1	1	0	0	1	1	0	1	1	0	0	252 V
+20	0	1	0	1	1	0	0	1	1	0	1	1	0	0	240 V
+19	1	0	1	0	0	1	0	1	1	0	1	1	0	0	228 V
+18	0	1	1	0	0	1	0	1	1	0	1	1	0	0	216 V
+17	1	0	0	1	0	1	0	1	1	0	1	1	0	0	204 V
+16	0	1	0	1	0	1	0	1	1	0	1	1	0	0	192 V
+15	1	0	1	0	1	0	1	0	0	1	1	1	0	0	180 V
+14	0	1	1	0	1	0	1	0	0	1	1	1	0	0	168 V
+13	1	0	0	1	1	0	1	0	0	1	1	1	0	0	156 V
+12	0	1	0	1	1	0	1	0	0	1	1	1	0	0	144 V
+11	1	0	1	0	0	1	1	0	0	1	1	1	0	0	132 V
+10	0	1	1	0	0	1	1	0	0	1	1	1	0	0	120 V
+9	1	0	0	1	0	1	1	0	0	1	1	1	0	0	108 V
+8	0	1	0	1	0	1	1	0	0	1	1	1	0	0	96 V
+7	1	0	1	0	1	0	0	1	0	1	1	1	0	0	84 V
+6	0	1	1	0	1	0	0	1	0	1	1	1	0	0	72 V
+5	1	0	0	1	1	0	0	1	0	1	1	1	0	0	60 V
+4	0	1	0	1	1	0	0	1	0	1	1	1	0	0	48 V
+3	1	0	1	0	0	1	0	1	0	1	1	1	0	0	36 V
+2	0	1	1	0	0	1	0	1	0	1	1	1	0	0	24 V
+1	1	0	0	1	0	1	0	1	0	1	1	1	0	0	12 V
0	0	1	0	1	0	1	0	1	0	1	1	1	0	0	0 V
-1	1	0	0	1	0	1	0	1	0	1	0	0	1	1	-12 V
-2	0	1	1	0	0	1	0	1	0	1	0	0	1	1	-24 V

-3	1	0	1	0	0	1	0	1	0	1	0	0	1	1	-36 V
-4	0	1	0	1	1	0	0	1	0	1	0	0	1	1	-48 V
-5	1	0	0	1	1	0	0	1	0	1	0	0	1	1	-60 V
-6	0	1	1	0	1	0	0	1	0	1	0	0	1	1	-72 V
-7	1	0	1	0	1	0	0	1	0	1	0	0	1	1	-84 V
-8	0	1	0	1	0	1	1	0	0	1	0	0	1	1	-96 V
-9	1	0	0	1	0	1	1	0	0	1	0	0	1	1	-108 V
-10	0	1	1	0	0	1	1	0	0	1	0	0	1	1	-120 V
-11	1	0	1	0	0	1	1	0	0	1	0	0	1	1	-132 V
-12	0	1	0	1	1	0	1	0	0	1	0	0	1	1	-144 V
-13	1	0	0	1	1	0	1	0	0	1	0	0	1	1	-156 V
-14	0	1	1	0	1	0	1	0	0	1	0	0	1	1	-168 V
-15	1	0	1	0	1	0	1	0	0	1	0	0	1	1	-180 V
-16	0	1	0	1	0	1	0	1	1	0	0	0	1	1	-192 V
-17	1	0	0	1	0	1	0	1	1	0	0	0	1	1	-204 v
-18	0	1	1	0	0	1	0	1	1	0	0	0	1	1	-216 V
-19	1	0	1	0	0	1	0	1	1	0	0	0	1	1	-228 V
-20	0	1	0	1	1	0	0	1	1	0	0	0	1	1	-240 V
-21	1	0	0	1	1	0	0	1	1	0	0	0	1	1	-252 V
-22	0	1	1	0	1	0	0	1	1	0	0	0	1	1	-264 V
-23	1	0	1	0	1	0	0	1	1	0	0	0	1	1	-276 V
-24	0	1	0	1	0	1	1	0	1	0	0	0	1	1	-288 V
-25	1	0	0	1	0	1	1	0	1	0	0	0	1	1	-300 V
-26	0	1	1	0	0	1	1	0	1	0	0	0	1	1	-312 V
-27	1	0	1	0	0	1	1	0	1	0	0	0	1	1	-324 V
-28	0	1	0	1	1	0	1	0	1	0	0	0	1	1	-336 V
-29	1	0	0	1	1	0	1	0	1	0	0	0	1	1	-348 V
-30	0	1	1	0	1	0	1	0	1	0	0	0	1	1	-360 V
-31	1	0	1	0	1	0	1	0	1	0	0	0	1	1	-372 V

Chapter 4

Results and Discussion

All the simulations are done in MATLAB R2009. The results of both the configurations are shown below:

MATLAB Simulink model of 31 level (peak to peak) inverter is shown below in fig 4.1:
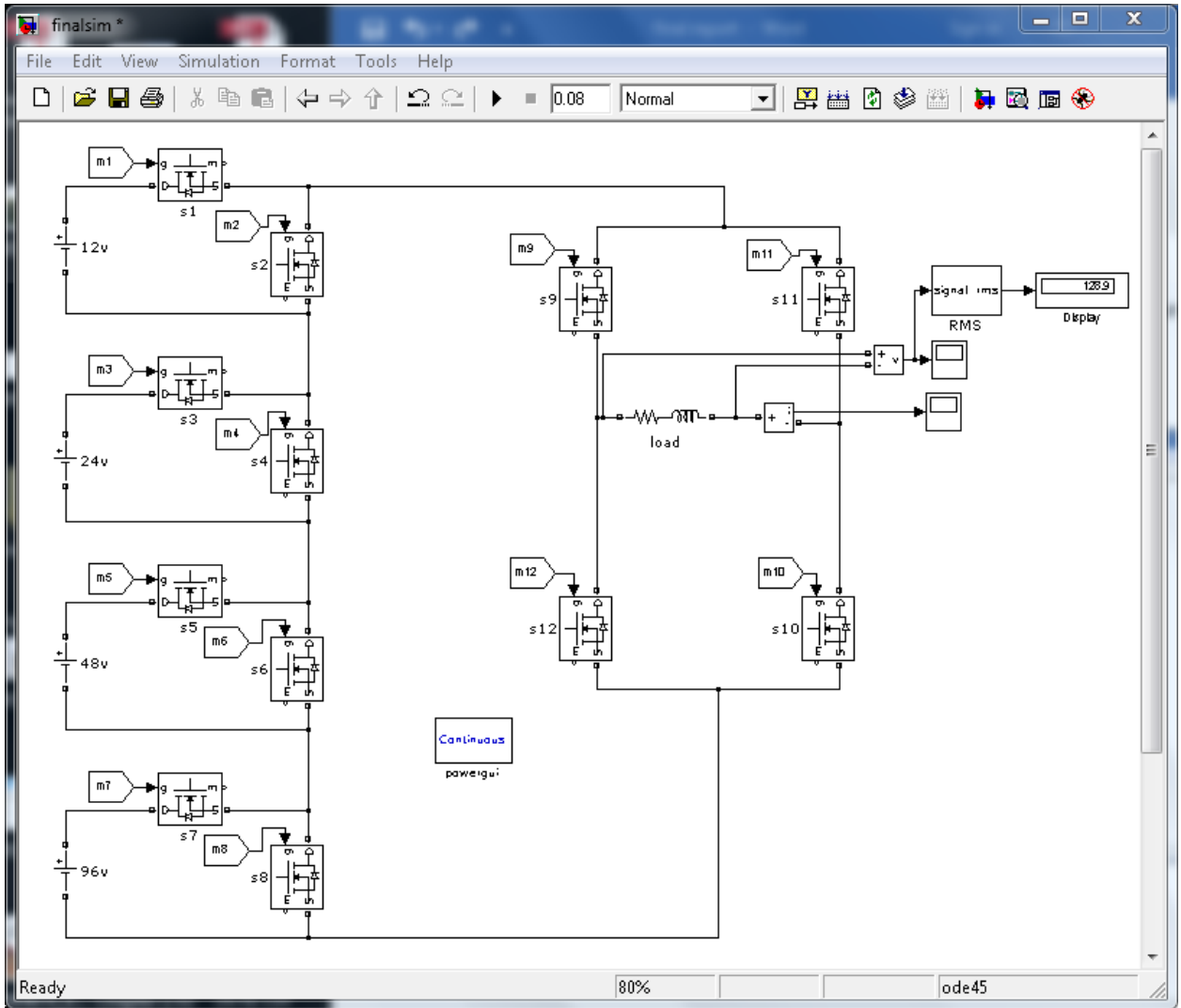

Fig 4.1 MATLAB Simulink model of 31-level inverter

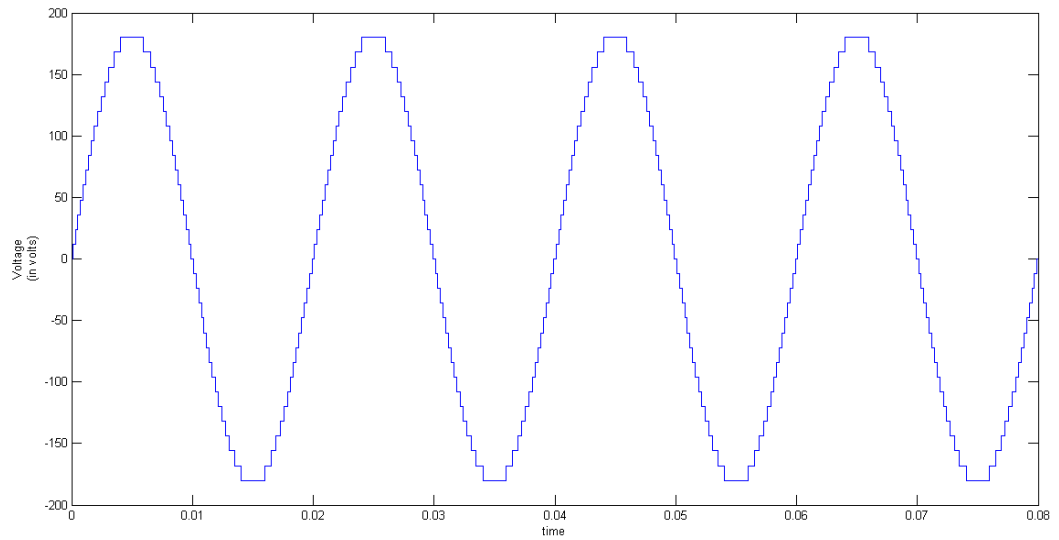The output voltage of 31 level (peak to peak) inverter with four DC voltage source is given below.

Fig 4.2 Voltage output waveform of 31-level inverter

The RMS value of output voltage is 128.9 volt and the peak value of voltage is 182.2 volt. The Total harmonic distortion present in output waveform is 2.52% which can be analyzed by FFT analysis which is shown below.
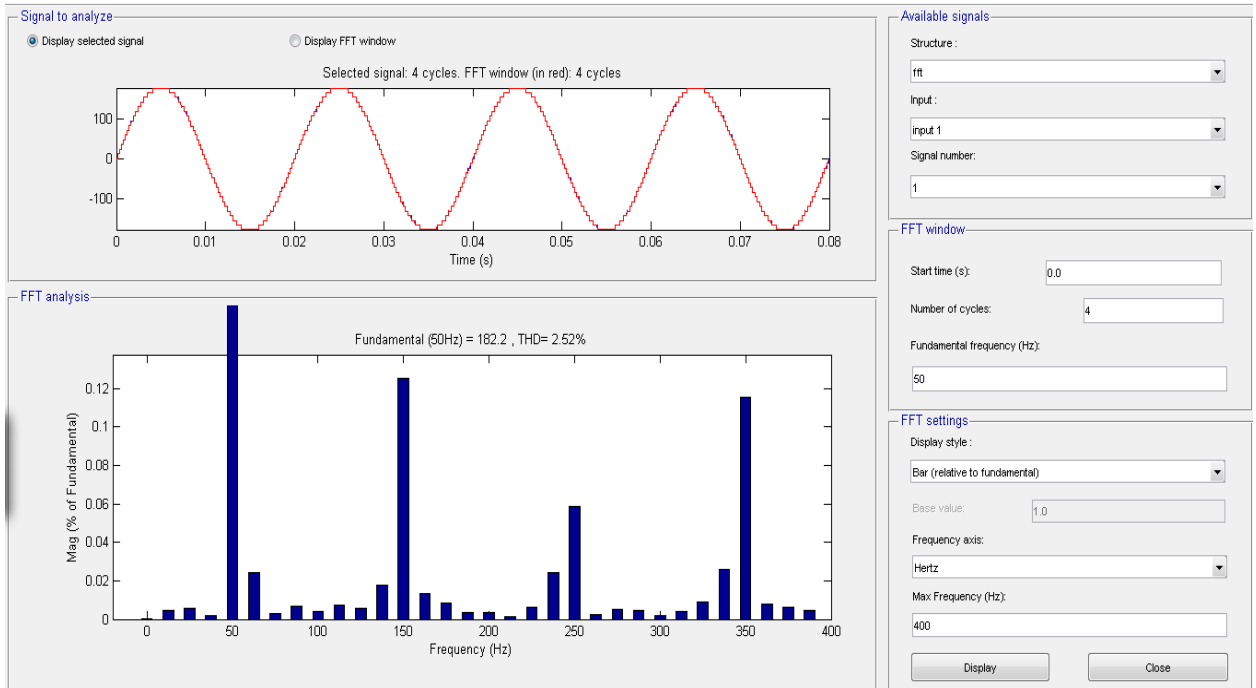

Fig 4.3 FFT analysis of 31-level output

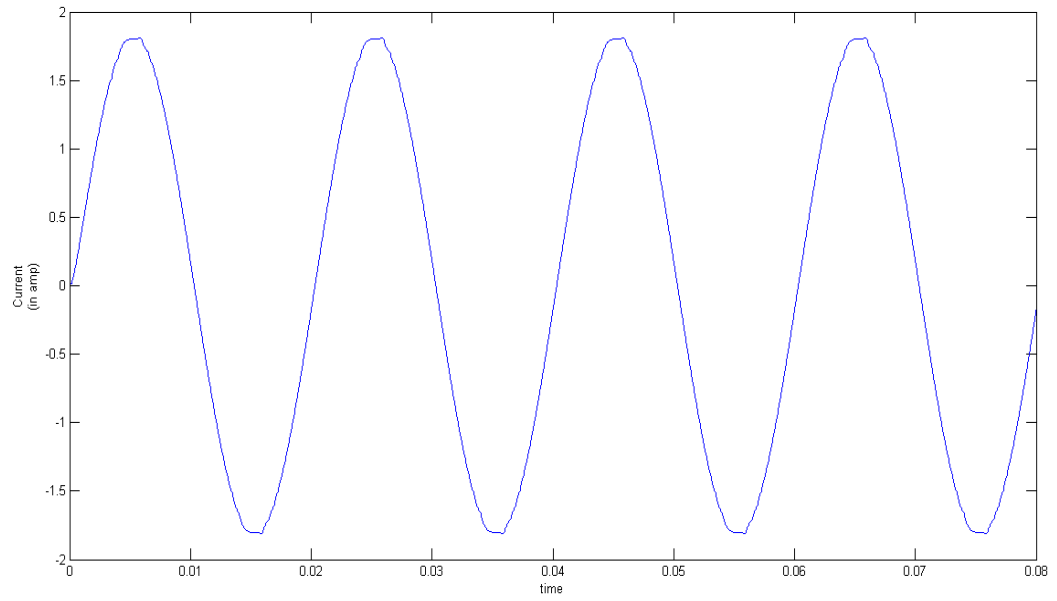Fundamental frequency is 50 hertz. Current waveform is given in fig.

Fig 4.4 Current output waveform of 31-level inverter

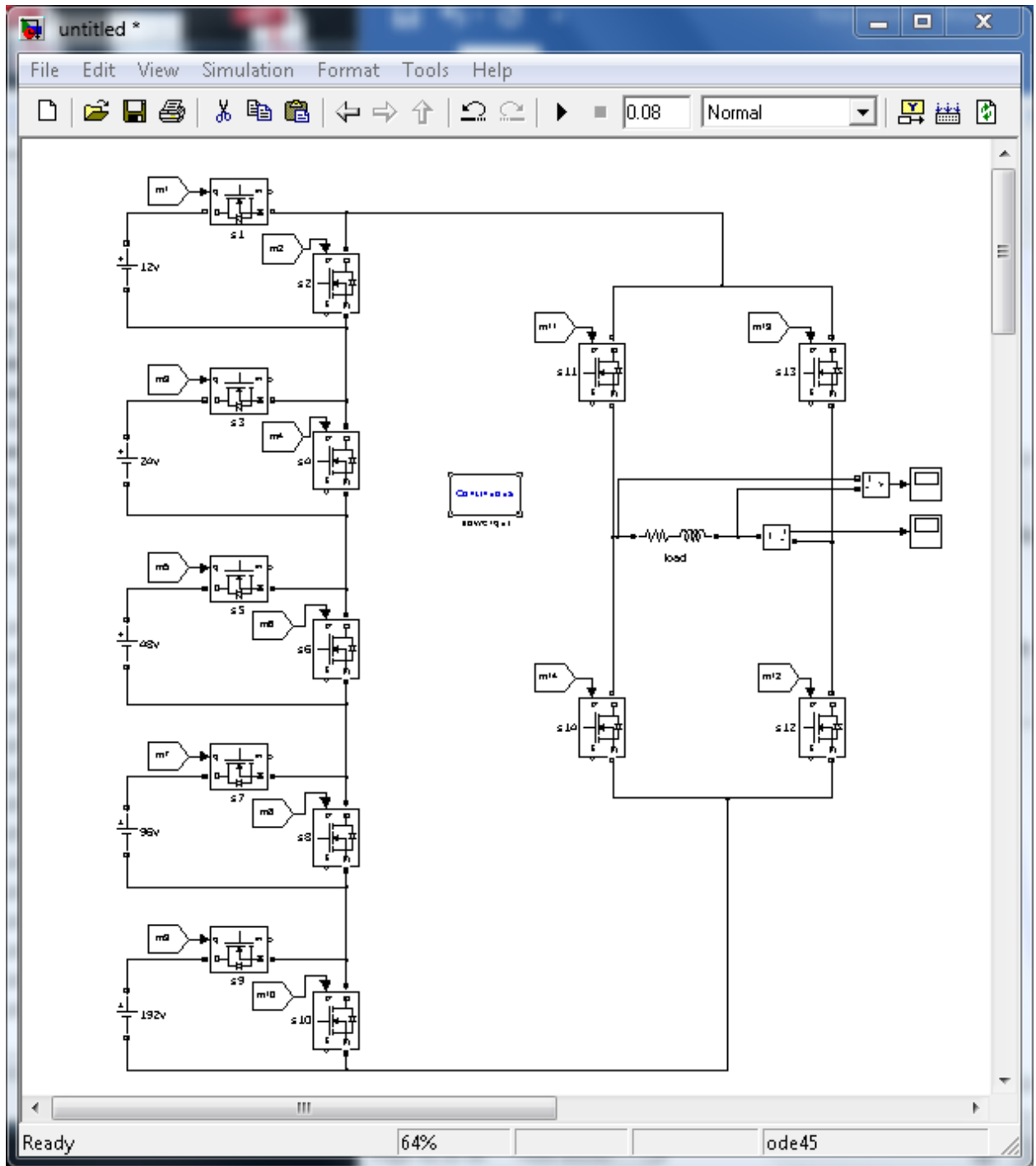MATLAB Simulink model of 63 level inverter is shown below in fig 4.5:

Fig 4.5 MATLAB Simulink model of 31-level inverter

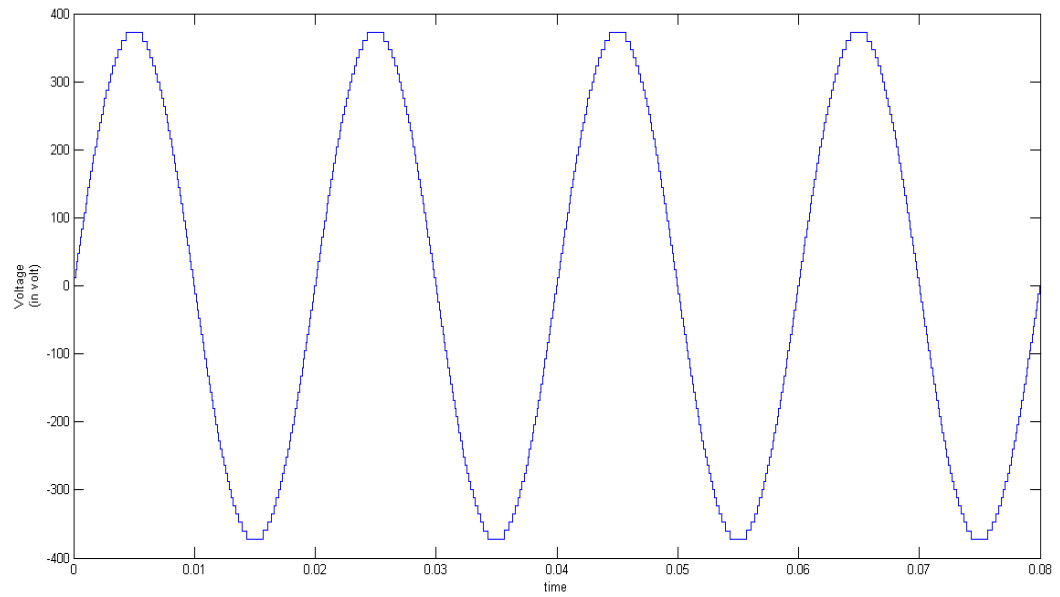The output voltage of 63 level (peak to peak) inverter with five DC voltage source is given below.

Fig 4.6 Voltage output waveform of 63-level inverter

The RMS value of output voltage is 264.7 volt and the peak value of voltage is 374.3 volt. The Total harmonic distortion present in output waveform is 1.26% which can be analyzed by FFT analysis which is shown below.
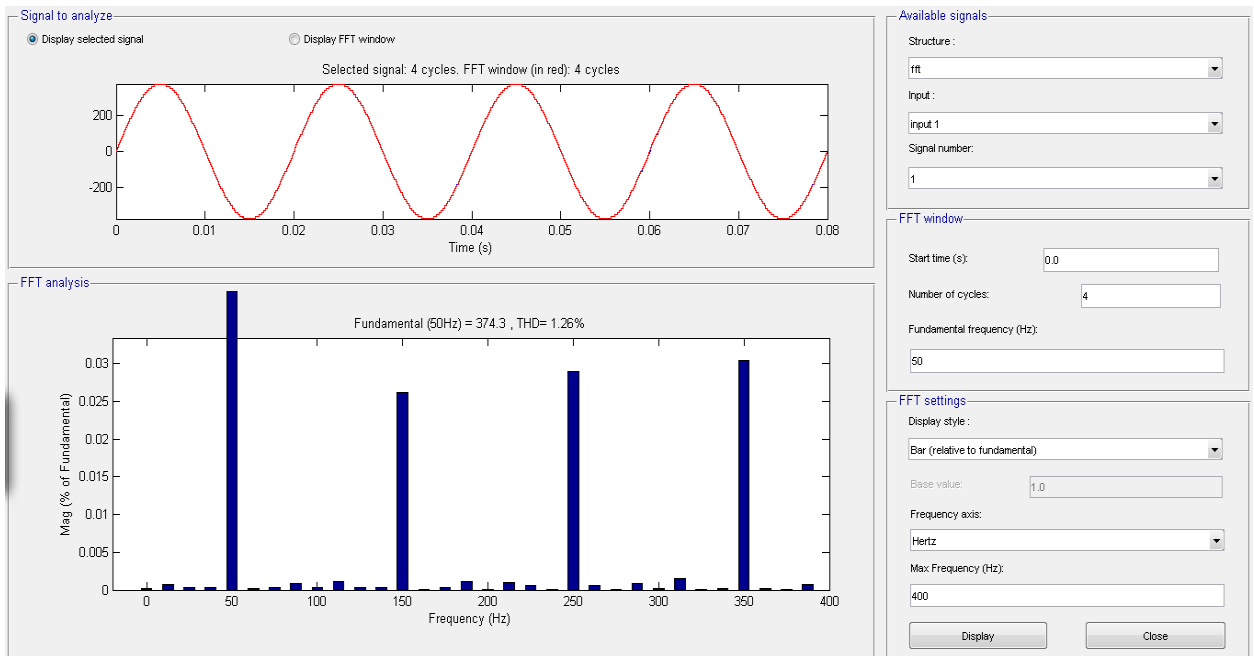

Fig 4.7 FFT analysis of 63-level output

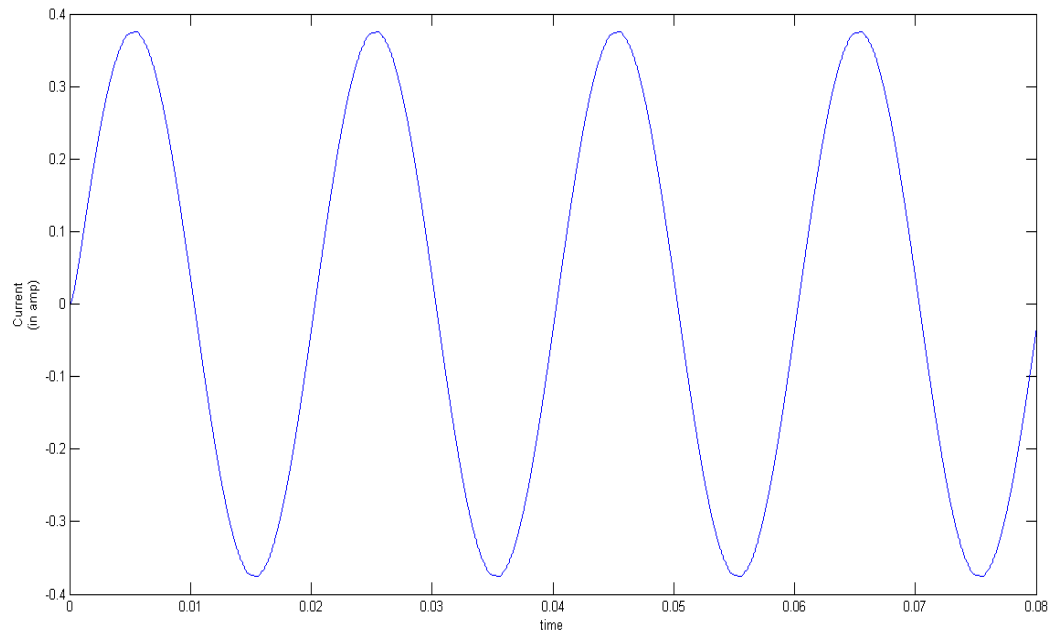Fundamental frequency is 50 hertz. Current waveform is given in fig 4.8.

Fig 4.8 Current output waveform of 31-level inverter

Chapter 5

Conclusion and Future Scope

Conclusion and future scope

This thesis is aimed at designing a multilevel inverter with reduction of switches as well as sources. It aims at controlling EMI (electromagnetic interference), reduces voltage stress and dv/dt across the switches and also reducing the THD drastically. This configuration can be compared with three types of multilevel inverter and this type is more suited for medium and high power applications.

For a conventional cascaded H-bridge single-phase 31-level inverter, it uses 60 switches with 15 DC isolated sources, whereas the proposed topology uses only 12 switches with 4 DC isolated sources.

The results are found to be very satisfactory and encouraging and in future, algorithm and soft switching can be designed and tested. Soft switching can further reduce the switching losses and heating of switches can be reduced. This can be very helpful in high power applications where lots of energy can be saved and heating can be reduced so that there will be smaller heat sink required and active cooling can be fully avoided.

Also, the same system can be designed for three phase system and can be analyzed.

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