THESIS REPORT

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DESIGN OF X-BAND CMOS VCO FOR RADAR APPLICATIONS

Submitted by

Nancy

Registration No.:11010286

Programme – M. Tech (ECE)

Under the Guidance of

Tejinder Singh

UID 17324

Designation- Asst. Professor

Discipline of ECE

Lovely School of Science and Technology

Lovely Professional University, Phagwara

To God and to my Family

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School of: Technology & Science

DISSERTATION TOPIC APPROVAL PERFORMA

Name of the Student: Nancy

Registration No: 11010286

Batch: 2010-2015

Roll No: RE0008B57

Session: 2014-2015

Parent Section: E2012

Details of Supervisor:

Designation: Assistant Professor

Name: Tejinder

Qualification: M-Tech

UID: 17324

Research Experience: 2 years

SPECIALIZATION AREA: Analog VLSI Design (pick from list of provided specialization areas by DAA)

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Signature of Supervisor: 09/10/14

PAC Remarks:

Approved

Signature: MG

Date:

APPROVAL OF PAC CHAIRPERSON:

*Supervisor should finally encircle one topic out of three proposed topics and put up for approval before Project Approval Committee (PAC)

*Original copy of this format after PAC approval will be retained by the student and must be attached in the Project/Dissertation final report.

*One copy to be submitted to Supervisor.

CERTIFICATE

I hereby certify that the work, which is being presented in the report, entitled on **"DESIGN OF X-Band CMOS VCO for RADAR applications",** in partial fulfilment of the requirement for the award of the Degree of Bachelor of Technology submitted to the **LOVELY PROFESSIONAL UNIVERSITY, Jalandhar**; is an authentic record of Nancy (11010286).

Date: 2nd May'15

Signature of student:

Nancy (11010286)

This is to certify that the above statement made by the candidate is correct to the best of my knowledge.

Mr. Tejinder Singh(17324)
Designation – Asst. Professor
School: Lovely School of Technology and Sciences
Lovely Professional University
Phagwara, Punjab
Date: 2nd May,2015

DECLARATION

I, Nancy, student of B.Tech +M.Tech (Dual Degree) under ECE Discipline at Lovely Professional University, Punjab, hereby declare that all the information furnished in this thesis report is based on our own intensive work and is genuine. This report is not copied and also not taken from anywhere.

Date: 2nd May, 2015

Signature:

Nancy (11010286)

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Gratitude cannot be seen or expressed. It can only be felt in heart and is beyond description. Often words are inadequate to serve as a model of expression of one's feeling, specially the sense of indebtedness and gratitude to all those who help us in our duty.

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We want to formally acknowledge my sincerest gratitude to all Lovely Professional University for providing a platform for designing and analyzing in CADENCE lab in completing this research.

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Abstract

In communication engineering, the X-band frequency range is 7 to 11.2GHz but in the RADAR engineering, the range of frequency which is specified by IEEE is 8.0 to 12.0GHz. X-band (8-12GHz) is widely used in applications of RADAR. Radar system operates in a wide range of transmitted frequencies. If the transmitted frequency is higher, the accuracy of radar system is better. X-band frequency is used for monitoring weather, air traffic control, defense tracking and detection of vehicle speed. X-band is also widely used for military applications like airborne radar and for maritime civil and military navigation radars.

Voltage controlled oscillators(VCOs) are used in application that require the generation of high frequency signals, e.g. in communications or sensor system such as radar. A good VCO should have low phase noise, wide tuning range, high frequency swing and low power consumption. The low phase noise and wide tuning range are the most crucial parameter in designing of VCO. A CMOS voltage-controlled-oscillator (VCO) can be designed with two main topologies: the ring VCO and the LC VCO. The LC VCOs have low phase noise much better than ring VCOs with low power consumption but with small tuning range. The phase-noise of LC VCO oscillators depend on the quality factor of inductor. Thus, the addition of high quality inductors to a CMOS process results in increasing cost and also the complexity of chip. Thus, in LC VCO, a large layout area is needed.

On the other hand, ring VCO results in low power consumption and less complexity with small chip area due to no use of on-chip inductors as required in LC VCOs.

Ring VCOs also provides multiple output phases and wide tuning range (>50%) as compared to that of tuning range of LC VCOs (10-20%) but having a poor phase noise. Therefore, some processing steps are required for improving phase-noise characteristic of ring VCO.

In this work, design of ring VCO using 90nm CMOS technology with 1V low power supply to obtain X- band frequency range ($f_{osc} \approx 10GHz$) with low power (1-5 mW), high tuning range (8-12GHz) and low phase noise (-90 to -130 dBc/Hz from 1MHz to 100MHz offset) is presented.

CHAPTER 1

INTRODUCTION

1.1 OSCILLATORS

Oscillator is the main block of many electronic devices such as PLL, frequency synthesizer. The different oscillator topologies and their performance parameters are required for various applications ranging from generation of clock in microprocessors to carrier synthesis in frequency synthesizer in radar systems.

1.1.1 General Considerations

An oscillator produces a sinusoidal periodic output in the form of voltage. The primary aim of an oscillator is to generate a waveform with constant peak amplitude swing with specific frequency and to maintain the same waveform within certain limit of amplitude and frequency. The requirements for an oscillator are as follows:

a) It must provide necessary gain for the signal.

b) To sustain oscillations, a sufficient regenerative feedback is required.

c) To maintain the desired output frequency, a frequency-determining device is needed.

To sustain oscillation, an oscillator must satisfy two conditions as follows:

$$|H(jw)| \geq 1 \tag{1.1}$$

$$\angle H(jw) = 180^{\circ}. \tag{1.2}$$

If a negative-feedback circuit has a loop gain and satisfying above mentioned two conditions, then circuit may oscillate at w_0 and these above mentioned two conditions are known as "**Barkhausen conditions**".

There is a phase shift of 180° or a total phase shift of 360°. Due to negative-feedback loop there is an 180° phase shift and there is another 180° phase shift which is frequency-dependent phase shift which shows that feedback signal enhances the original signal.

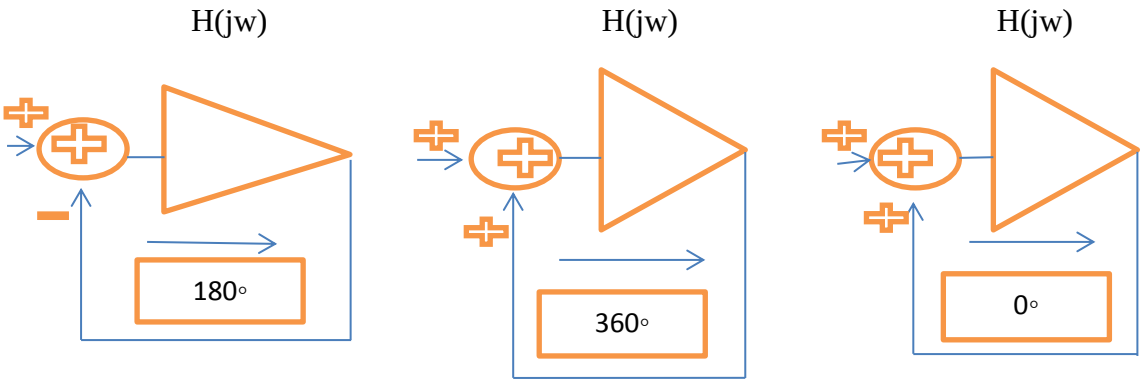


Fig 1.1: Various oscillatory feedback systems.

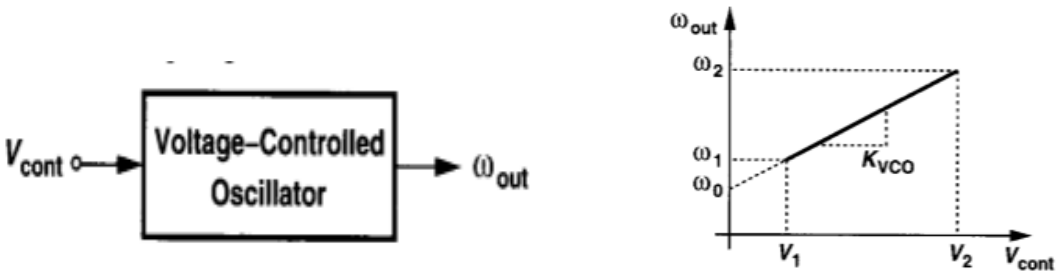
1.2 Voltage-Controlled Oscillators

An ideal VCO is a circuit whose output frequency is a linear with control voltage

$$w_{out}=w_0+K_{vco}\ V_{ctrl}. \quad (1.3)$$

where w_0 is the frequency when $V_{ctrl}=0$ and K_{vco} is the gain of VCO.

The range to be tuned of VCO is the achievable range i.e. w_2-w_1 as shown in Fig.1.2 (b) [20]:



(a) (b)

Fig 1.2 (a) VCO blocks (b) Characteristic of VCO [2]

1.2.1 Important Performance Parameters of VCOs [26]:

1. **Centre Frequency**: The center frequency is determined by the environment in which the VCO is used such as CMOS VCOs achieve center frequencies +10GHz.
2. **Tuning Range**: The desired tuning range can be achieved by two parameters:
   a) Variation in center frequency of the VCO with process and temperature.
   b) The frequency range desired for the application required.

The center frequency of VCO may vary by a factor of two at the extremes of temperature and process, thus it is sufficient to maintain a wide (≥2*) tuning range so that the VCO output frequency be driven to desired value. The variation in phase and frequency output keeping the effect of noise on control line is an important factor. The noise in the output frequency is proportional to gain of VCO K_{vco} for a given noise amplitude. The VCO gain must be minimized to minimize the effect of noise on V_{ctrl} which conflict with the required tuning range. The range of V_{ctrl} is from 0 to VDD i.e V_1 to V_2 and tuning range from w_1 to w_2 as shown in Fig1.2 (b), [26] the gain of VCO K_{vco} must satisfy:

$$K_{vco} \geq (w_2 - w_1)/(V_2 - V_1) \quad (1.4)$$

Thus, the gain of VCO increase with decreasing voltage supply but its making oscillator much sensitive toward noise.

3. **Tuning Linearity**: Due to gain of VCO K_{vco} is not constant, the tuning characteristics of VCO exhibits non-linearity which further degrades application in which it is used. Thus, it is desirable to minimize the variation of Kvco with tuning range and in actual, oscillator exhibit a high gain in mid of tuning range and a low gain at extremes.

4. **Output Amplitude**: It is desired to achieve high swing output oscillation amplitude which results in less sensitive to noise but there is trade-off between output amplitude with power dissipation, supply voltage and the tuning range.
5. **Power Dissipation**: There occurs a trade-off between power dissipated, speed and noise of VCO.
6. **Supply and Common-Mode Rejection**: As VCOs are sensitive to noise if designed in single-ended form and it is not easy to design oscillators with high noise immunity. Thus, it is preferable to design oscillators with differential path for both oscillation signal and control line.
7. **Output Signal Purity**: The output waveform is not periodic even with constant control voltage. The output phase and frequency get affected by electronic noise in oscillator and supply noise.

1.2.2 Comparison of Ring and LC VCO

LC VCOs have low phase noise much better than ring VCOs with low power consumption but with small tuning range. The phase-noise of LC VCO oscillators depend on the quality factor of inductor. Thus, the addition of high quality inductors to a CMOS process results in increasing cost and also the complexity of chip. Thus, in LC VCO, a large layout area is needed.

Ring VCO results in low power consumption and less complex in addition with small chip area due to no use of on-chip inductors that required in LC VCOs. Ring VCOs also provides multiple output phases and wide tuning range (>50%) as compared to that of tuning range of LC VCOs (10-20%) which is low but with poor phase noise.

1.3 Scope of the study

As the technology increases, the VCO with its comprising features with respect to the technology needed for various applications ranging from clock generation in microprocessors to frequency synthesizers for radar and other systems. Thus, it is not always needed to use LC networks for high-frequency VCO [1]. By changing the various parameters of ring VCO, it is possible to achieve high-frequency with good phase-noise as well. Thus, with different ring architectures as designed sand proposed meet the desired specifications as per requirement with high-frequency operation, wide tuning range, and low power with low phase-noise also.

1.4 Objective of the study

X-band VCO would be designed using base differential architecture with low phase noise and wide tuning range using 90nm CMOS technology with 1V low supply voltage to obtain X-band frequency range (8-12 GHz) with low power (1-5 mW), high tuning range and low phase noise (-90 to -130 dBc/Hz from 1MHz to 100MHz offset).

CHAPTER 2

CMOS RING VCO

2.1 Ring Oscillators Basics

A ring oscillator consists of a number of stages in a closed loop by connecting output to input. The most basic ring oscillator is single-ended inverter chain consists of odd number of stages. The frequency of oscillation of ring VCO is given as [14]:

$$F_{osc}=1/(2*N*t_d) \quad (2.1)$$

where t_d is the propagation delay of single stage.

The transfer function of N-stage ring oscillator is:

$$H(s) = A_1(s).A_2(s).A_3(s).\ldots\ldots A_N(s) \quad (2.2)$$

where $A_1(s)$, $A_2(s)$, $A_3(s)$ and $A_N(s)$ are the s-domain transfer function of individual delay stages. The gain of delay stages are identical so

$$H(s) = A^N(s) \quad (2.3)$$

where N is the number of stages.

According to Barkhausen condition, the total phase shift should be a multiple of $2\prod$ and magnitude should be equal to unity. The oscillation criterion is as follows:

$$\angle H(jw_0) = 2\prod/N \quad (2.4)$$

$$|H(jw_0)|^N = 1 \quad (2.5)$$

Finally, the oscillation frequency is given as:

$$w_0=\tan(\theta)/RC \quad (2.6)$$

This reduces to $\sqrt{3}/RC$ for 3-stage ring VCO and $1/RC$ for 4-stage ring VCO. Therefore, the gain requirement of a 3-stage ring VCO is $g_mR\geq 2$ and $g_mR\geq\sqrt{2}$ for 4-stage ring VCO.

2.1.1 Single-ended Ring VCO:

The most widely used single-ended ring oscillator is CMOS inverter that consists of an NMOS transistor and a PMOS transistor.

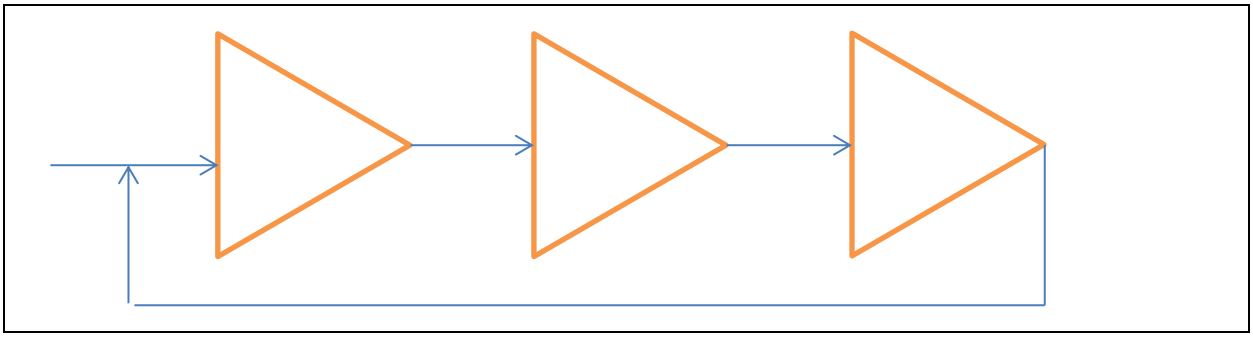


Fig. 2.1: 3-stage Single-ended Ring VCO

There are different ways to tune the frequency by changing the load which can be either resistor or capacitor and also by tail current by control voltage as in [19]. These ring VCOs are simple and easy to design but more susceptible to noise.

2.1.2 Differential Ring VCO:

The differential topology is preferred over single-ended and mostly used in most of the applications due to its differential output reject noises such as common-mode noise, power-supply noise and so on.

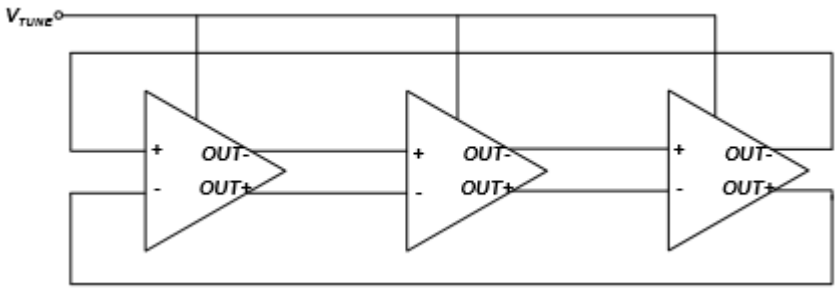


Fig.2.2 (a): 3-stage Differential Ring VCO [13].

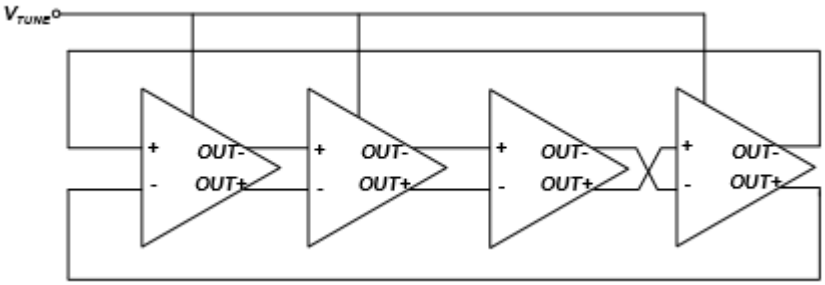


Fig. 2.2 (b): 4-stage Differential Ring VCO [13]

CHAPTER 3

LITERATURE REVIEW

Today ICs and SoCs, mixed signal circuit has significantly increased from 10 to 20% to 50% or more due to increased needs for mobility, higher performance and integration of interfaces in devices. The design of high performance VCOs has been one of the active areas of research. **A good VCO must have low phase noise, less power consumption, high tuning range with small area of chip.** An ideal oscillator output frequency must be linearly dependent on its control voltage. Radar synthesizers have more stringent noise and are used as the reference of timing between the transmitted and received signals of the radar. Thus, a CMOS ring VCO with low phase-noise and high tuning range is designed. The design of ring oscillator using delay stages becomes much more beneficial as compared to other monolithic oscillators. Thus, designing ring VCO in such a way to improve the performance as speed of operation and noise performance.

S. Vandna et al. (2012) [12] In this paper, the design and analysis of ring oscillator in 45nm technology is presented. In 9-stage single-ended ring oscillator, the phase-noise is reduced and power consumption is also reduced by 18.9% but there is also ***reduction in operating frequency from 5.63GHz to 341MHz*** at same supply voltage and due to ***use of 9-stages, the delay increases as the number of stages increases.***

M K Mandal et al. (2010) [14] In this paper, the structure and operating principle of ring oscillator have been described. The limitations of conventional ring oscillator and techniques to overcome these limitations have been mentioned. Some modified ring structures such as negative skewed delay ring oscillator, multi-feedback ring oscillator and coupled ring oscillators are described for high frequency oscillations.

R.K.Sarin et al. (2012) [19] In this paper, the conventional ring oscillator is modified in which the charging and discharging time is reduced by improving tail current. The first delay stage is of CMOS NAND gate and the others two delay stages are of CMOS inverters. The output frequency increases by reduction in propagation delay by reducing charging and discharging time of output node capacitance of the delay cell.

The design results in tuning range 0.958-4.43GHz, 0.226mW power and -94.51dBc/Hz @1MHz. This modified conventional ring oscillator is not much more immune to noise as compared to differential-ring oscillators.

Moh. Ashraf et al. (2013) [13] In this paper, the design of high performance ring VCOs are analyzed. The differential VCO cell provide better oscillation and noise performance due to their current mode logic which provides fast oscillation frequency and differential noise rejection than the single-ended. PFETs load in differential pair produces a large tuning range in addition the output of VCO cell drives only another gate to achieve maximum frequency has been reported by ***S. Docking and M. Sachdev*** but suffering with two drawbacks of dc offset problem and small swing at low control voltage problem. The proposed ring VCO helps in obtaining large tuning range and acceptable phase-noise. The tuning range increases linearly with V_{out} .

J.K.Panigrahi et al. (2010) [3] In this paper, the differential VCO is presented with improved phase noise and tuning range as compared to previous ones. The proposed schematic delay cell in consists of positive feedback for VCO oscillation and two diode-connected PMOS load and one PMOS load whose input is control voltage for frequency tuning of VCRO. The two delay blocks are used for minimization of power consumption and phase noise. To achieve high frequency of operation, the transconductane to capacitance (g_m/C) ratio be increased by using NMOS transistor as input pairs and by varying the transconductance of diode-connected PMOS, the wide tuning range is achieved.

Phase noise of ring VCO infers that the delay cell provide faster slew rate (short rise/fall time) and full switching capability achieves better phase noise. The ***frequency tuning range is improved by 12% and power consumption is less but the phase noise of VCO is high***. The ***phase noise can be improved by increase in number of stages which result in improvement of 6dB with three stages over two*** and its ***tuning range is also improved by 2%*** but at the ***expense of increasing in area of chip*** and also ***increase in power consumption*** from 9.61mW to 14.43mW. The output frequency of the VCO is 1.22-3.22GHz with 62.11% tuning range with -90.01dBc/Hz @ 600 kHz offset.

L. Xuemei et al. (2013) [6] In this paper, a large tuning range ring VCO is designed based on a DCVL delay cell which consists of a differential pair of NMOS transistor with a cross-coupled load PMOS transistor, along with two PMOS transistors who change the flow of current of output node. By the power supply and controlled voltage, the oscillation frequency is changed.

The maximum frequency is obtained with largest power supply and lowest controlled voltage while the minimum frequency is obtained with lowest power supply. With the help of controlled voltage, the phase noise is changed and it becomes better when the controlled voltage is higher. The maximum frequency of oscillation of this ring VCO is 6.9GHz with tuning range of 75MHz to 6.9GHz but with worse phase noise of 101.1dBc/Hz @ 10MHz offset. This ***differential VCO results in wide tuning range with less power consumption but also results in worse phase noise***.

L. Xuemei et al. (2013) [4] In this paper, the proposed circuit is same as the previous one mentioned in [6] and redesign to improve its phase noise performance. By changing delay time, the frequency be controlled by changing charging-discharging and RC time constant of delay cell. The frequency of oscillation can be tuned by varying the control voltage. The ***phase noise of proposed ring VCO*** in [4] ***is independent of the number of delay stages*** and it ***depends on oscillation frequency***, the charging and discharging of output node and the transconductance of NMOS transistors. Thus, ***the same VCO circuit is used resulting in 5.287GHz oscillation frequency with 15.1mw power using 3-stages and -97.93dBc/Hz phase noise @ 1MHz offset with 0.00175mm^2 core areas.*** As compared to previous one, this ***VCO results in good phase noise, less area but at the expense of power consumption***.

L. Hai Qi et al. (2008) [20] The multi-loop topology is introduced in this paper in differential ring oscillator which improves oscillator frequency with much good phase noise. A sub-feedback loop is created to increase the operation frequency of ring VCO and it is a fast loop compared to the normal loop. A delay stage for ring VCO with multi-loop technique is by using push-pull inverter as the secondary input in its delay cell [20]. This proposed ring VCO results in improvement in frequency of 17% as compared to conventional. To boost the oscillation frequency and also for the improvement in phase noise performance, a push-pull inverter is added to the delay cell. The proposed oscillator speed gets improved at the cost of lower swing amplitude and results tuning range from 6.24-7.04GHz with 72mW power and -107.7dBc/Hz @ 10MHz from 6.26GHz.

A. Yalcin et al. (2004) [1] This paper presents the design of a 14GHz ring VCO with in-phase/quadrature (I/Q) in a standard 0.18-µm CMOS process. A four stage multiple-pass ring oscillator is designed with frequency doublers for high frequencies. The delay cell with cross-coupled FETs is used for increasing the switching speed and to improve noise parameters.

The main purpose is to reduce the delay of the cells below the smallest delay that must be possible in ring oscillators which is going to be achieved by addition of secondary inputs S+ and S-, to every stage of the oscillator and switching these earlier than the primary inputs during the operation.

A. Yalcin et al. (2004) [5] This paper presented the design of three and nine-stage VCO in TSMC 0.18-µm CMOS technology with oscillation frequency up to 5.9 GHz. The circuits use a multiple-pass loop architecture. Measurements show that the oscillators have linear frequency-voltage characteristics over a wide tuning range, with the three- and nine-stage rings resulting in frequency ranges of 5.16–5.93 GHz and 1.1–1.86 GHz, respectively. The measured phase noise of the nine-stage ring oscillator was -105.5 dBc/Hz at a 1-MHz offset from a 1.81-GHz center frequency, whereas the value for the three-stage ring VCO was simulated to be -99.5 dBc/Hz at a 1-MHz offset from a 5.79-GHz center frequency.

CHAPTER 4

RESEARCH METHODOLOGY

4.1 Experimental Setup

Cadence: Virtuoso Analog Design Environment

Cadence is an Electronic Design Automation (EDA) environment which allows different applications and tools to integrate into a single framework and also support all the stages of IC design and verification from a single environment. These tools support different fabrication technologies.

Cadence Virtuoso Schematic Editor: It provides a complete design and constraint composition environment for front-to-back analog, custom-digital, RF, and mixed-signal designs.

4.2 Design Methodology

The design study has to be done step by step as follows:

- Firstly, the study has to be done on the research topic. Then the different architectures designed need to be studied and analyzed with their pros and cons.

- Hand analysis has to be done as per desired specifications required to design for proposed architecture.

- After hand calculations, determining various parameters such as transistor size, control voltage and others, then the design will be implemented on the software as required.

- Results be compared with hand analysis to determine any error and then again the proposed design is implemented with proper analysis.

The flow chart to illustrate design methodology is as follows:

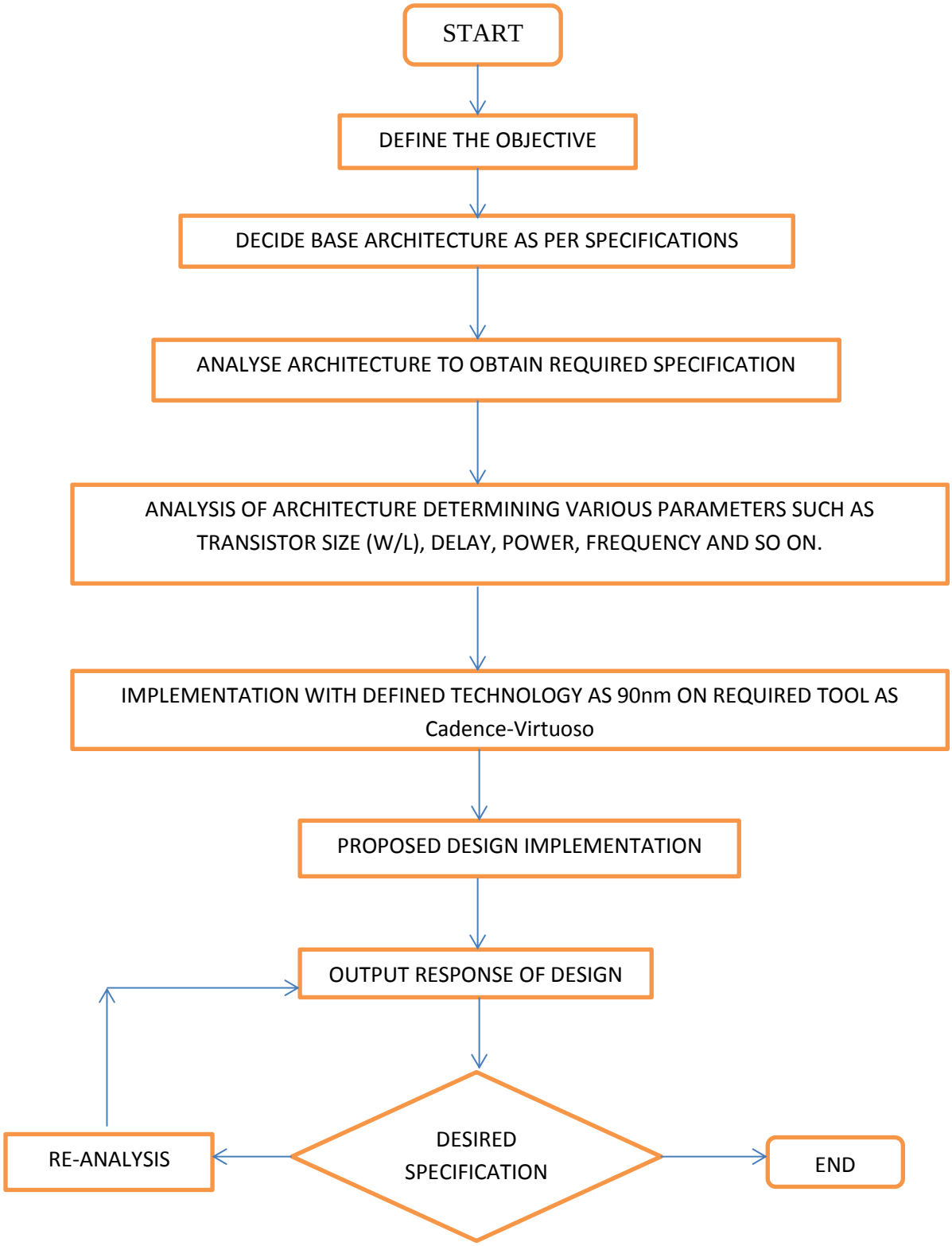


Fig. 4.1: Flowchart of design methodology

As in designing ring VCO, the multi-loop architecture is proposed to reduce the smallest delay possible in a delay stage.

Design Considerations:

The desired specifications for 3-stage multi-pass ring oscillator are as follows:

Table 1.1: Desired specification of multi-pass oscillator for 90nm technology

Desired Specifications:	
f_{osc}	≈ 10GHz
Power	1-5 mW
phase noise(@ 600KHz to 1MHz offset)	(-90 to -130 dBc/Hz

The frequency of oscillation of ring VCO is given as [19]:

$$F_{osc} = 1/N(t_{rise}+t_{fall}) \quad (4.1)$$

Where N is the number of stages, t_{rise} is the rise time and t_{fall} is the fall time.

If $t_{rise} = t_{fall} = t_{d,}$ then

$$F_{osc} = 1/2Nt_d \quad (4.2)$$

For desired frequency, the propagation delay is calculated.

There is a trade-off between frequency and number of stages and delay. Increase in number of stages increases propagation delay. Thus, the number of stages N should be less reducing delay increase frequency.

The average power of ring oscillator is given as [19]:

$$P_{avg} = C_{load}*V_{dd}^{2}*F_{osc} \quad (4.3)$$

where C_{load} is the load capacitance.

For a given desired frequency of oscillation and power supply and for desired power, the load capacitance can be calculated.

And the power of ring oscillator is also given as:

$$P_{avg} = N*V_{dd}^{2}*I_{avg}$$

As the delay and load capacitance be determined, the width of PMOS and NMOS be calculated as follows [19]:

$$\left(\frac{W}{L}\right)_n = \frac{C_{load}}{\tau\,\mu_n\,C_{ox}\left(V_{DD}-V_{t,n}\right)}\left[\frac{2\,V_{t,n}}{V_{DD}-V_{t,n}} + \ln\left(\frac{4\left(V_{DD}-V_{t,n}\right)}{V_{DD}} - 1\right)\right] \quad (4.4)$$

$$\left(\frac{W}{L}\right)_p = \frac{C_{load}}{\tau\,\mu_p\,C_{ox}\left(V_{DD}-|V_{t,p}|\right)}\left[\frac{2\,|V_{t,p}|}{V_{DD}-|V_{t,p}|} + \ln\left(\frac{4\left(V_{DD}-|V_{t,p}|\right)}{V_{DD}} - 1\right)\right] \quad (4.5)$$

Thus, the transistor sizes can be determined so that the desired frequency with desired specifications can be achieved for the base ring voltage-controlled oscillator.

4.3 Expected Outcome

The proposed design is designed by delay stage of multiple loop differential architecture to obtain desired specification for X-band ring VCO for radar applications with low phase noise and wide tuning range using 90nm CMOS technology

The desired specifications are as follows:

Table 1.2: Desired specifications for ring VCO

DESIRED SPECIFICATIONS	
CMOS technology	90nm
Power supply (V)	1
Oscillation frequency (GHz)	≈10
Tuning Range (GHz)	8-12
Power (mW)	1-5
Phase Noise (dBc/Hz from 1MHz to 100MHz offset)	-90 to -130

CHAPTER 5

PROPOSED RING VCO ARCHITECTURE

The simple basic ring oscillator is the CMOS inverter delay stages. The schematic of 3-stage CMOS inverter ring oscillator is shown in Fig.5.1.

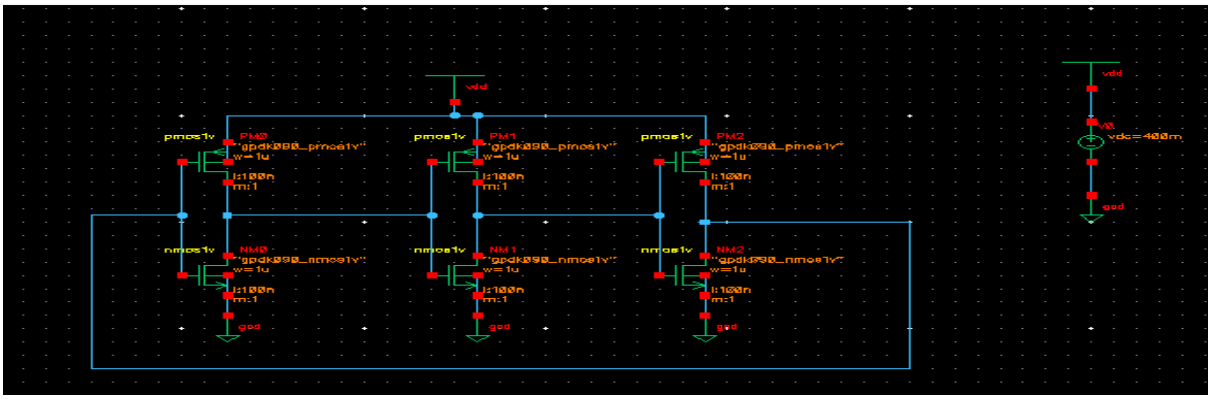


Fig. 5.1: Schematic of 3-stage CMOS ring oscillator.

It is designed just by simple CMOS inverter whose output act as an input to next delay stage and final stage output is feedback to input of first stage. The width of PMOS is twice the width of NMOS for proper operation.

Further, to achieve the tuning range of VCO, the PMOS with varying gate voltage is connected in parallel with PMOS of CMOS inverter in a delay stage. The desired tuning range can be achieved by varying the width of the PMOS PM4. The gate voltage of PM4 is varied from 0-1 V.

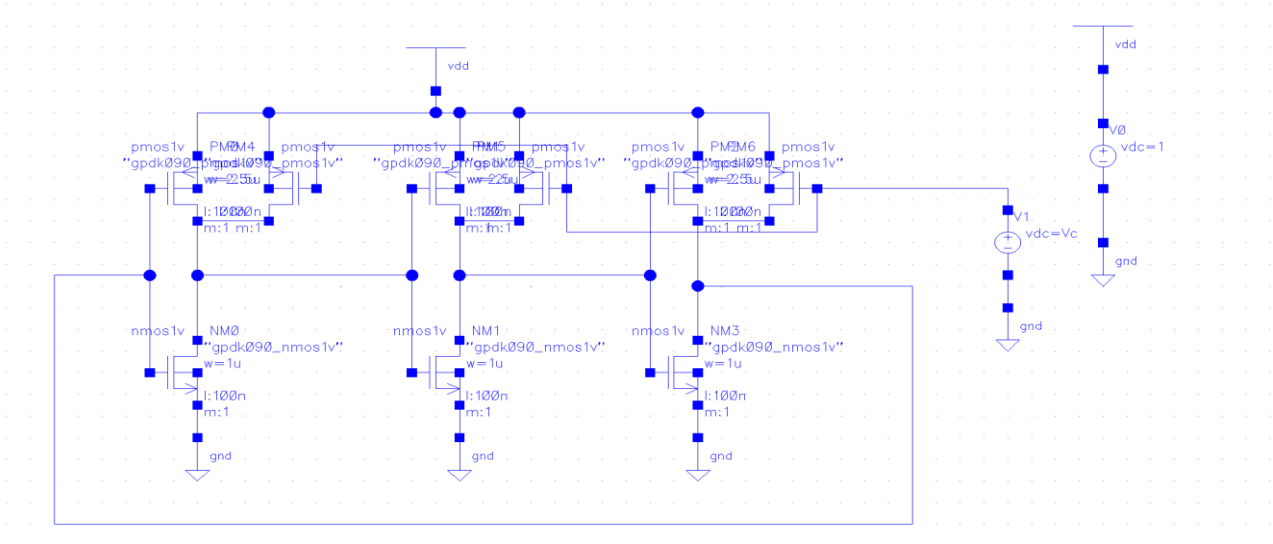


Fig. 5.2: 3-stage Single-ended ring VCO.

An inductive load is induced as shown in Fig. 5.3 to improve the phase-noise characteristic of VCO. The transistor NMOS NM10 and PMOS PM1 forms the input pair and PMOS PM4 act as a load to control the operating range of frequency with NMOS NM5 as an inductive load which provides higher frequency of oscillation with better phase noise. The width of inductive load must be set to minimum width of the technology and the width of PMOS load PM4 should be greater than PMOS PM1.

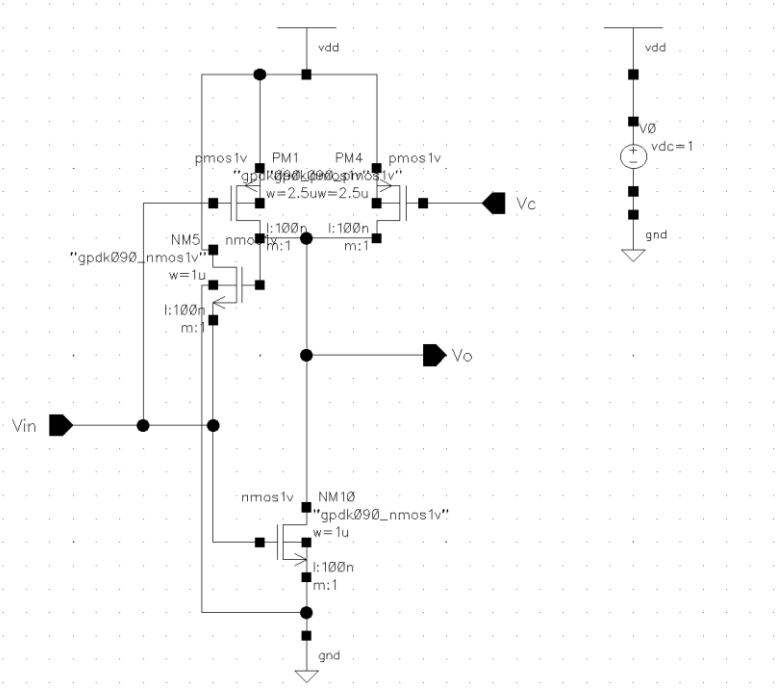


Fig. 5.3: Single-ended VCO with inductive load delay cell.

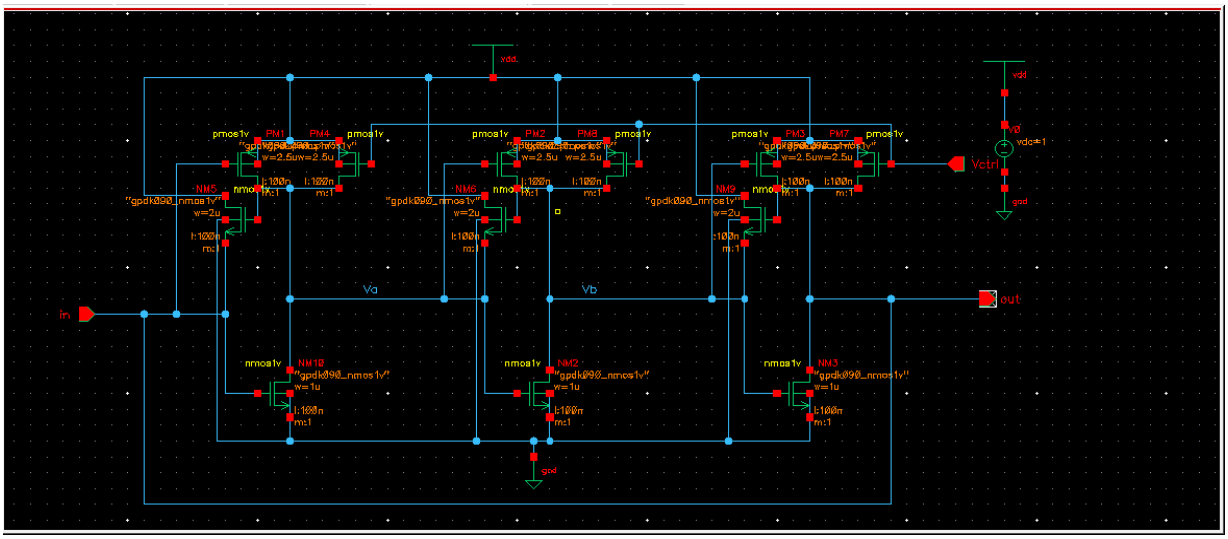


Fig. 5.4: 3-stage Single-ended ring VCO with inductive load.

As the differential topology is preferred over single-ended due to common-mode noise rejection and others. Thus, the same single-ended topology is converted into differential one for better results. The single-ended ring VCO with inductive load results better than single-ended with PMOS load is discussed in next chapter. So, the differential with multiple loop architecture is designed in 90nm technology as shown in Fig. 5.5. The wider tuning can be achieved by differential topology.

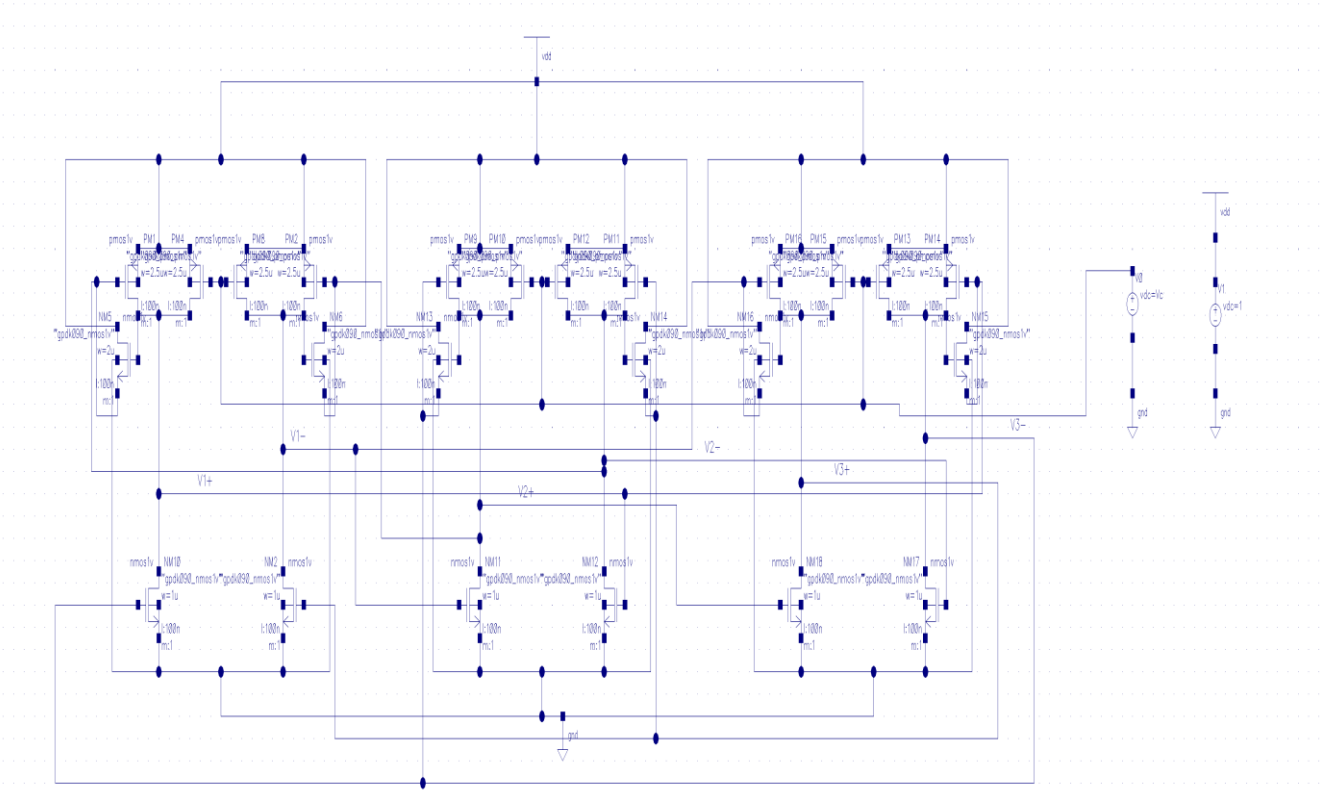


Fig. 5.5: 3-stage Differential ring VCO with inductive load.

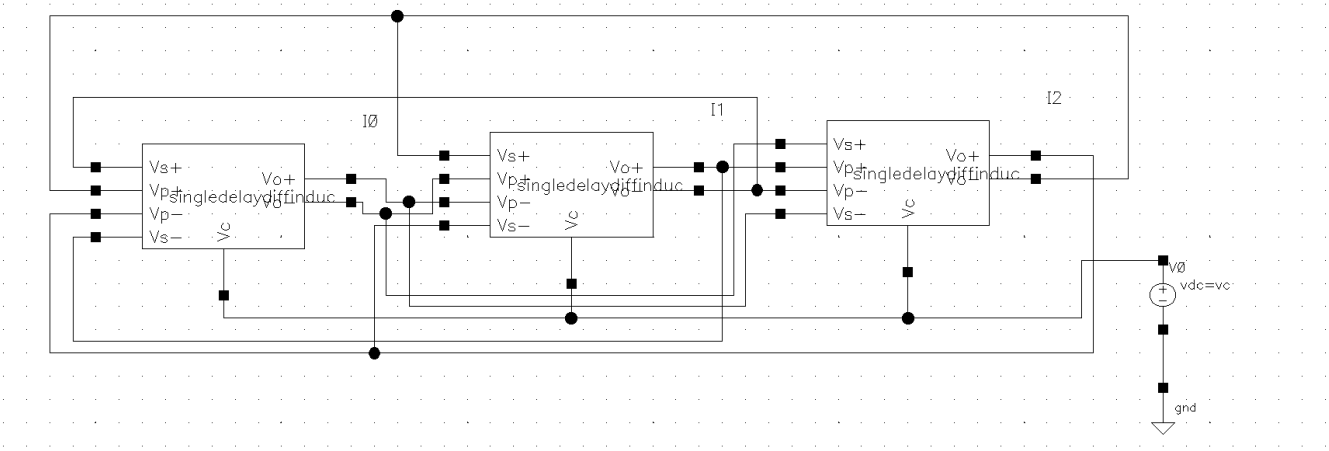


Fig. 5.6: Block diagram of 3-stage Differential ring VCO with inductive load.

5.1 Proposed 3-stage multi-loop CMOS ring VCO additional PMOS load

The previous differential architecture results in wider tuning range with low power dissipation and good phase noise. Thus, an additional PMOS load is connected to achieve the desirable tuning range. This additional PMOS load is always ON because gate of this PMOS is connected to ground. This also results in wider tuning range but adjusting the width of both PMOS load, X-band tuning range can be achieved with low power dissipation than previous one. The schematic of 3-stage proposed differential ring VCO is shown in Fig.5.7.

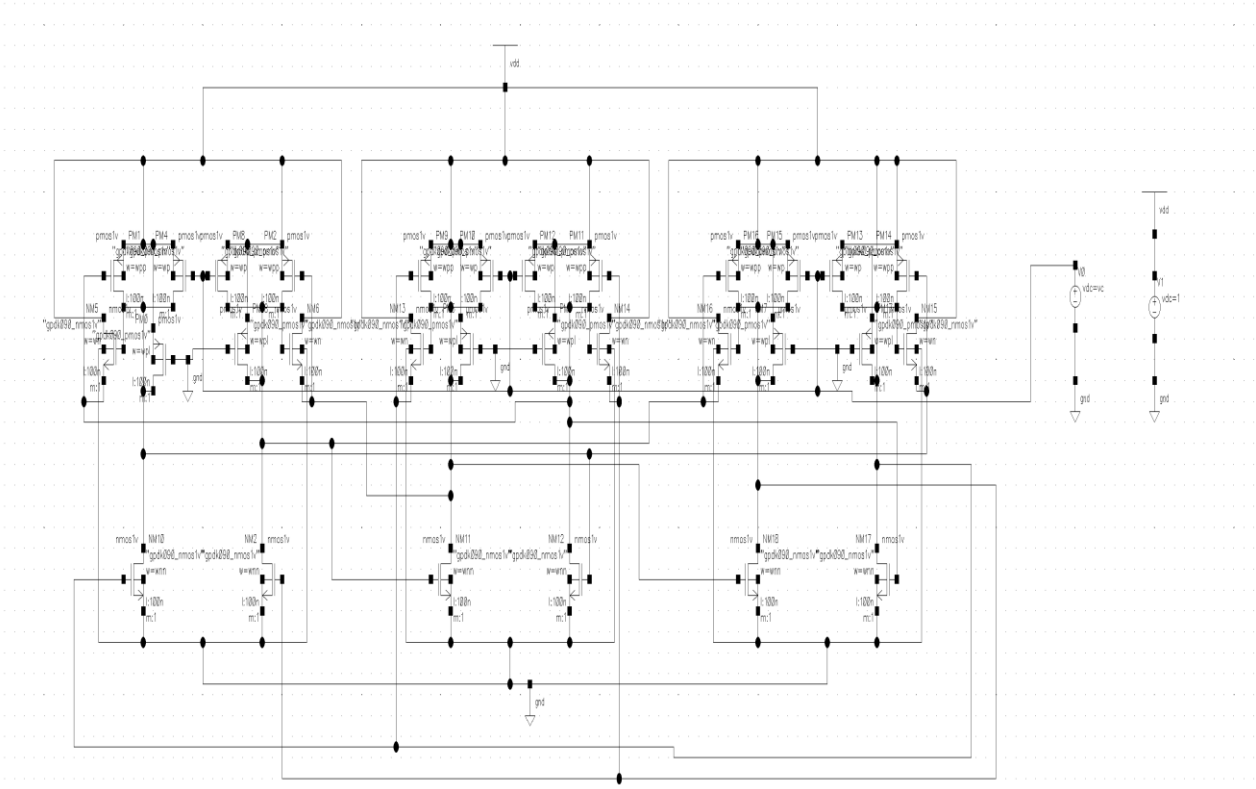


Fig. 5.7: 3-stage Proposed Differential Ring VCO.

For wider tuning range, the size of secondary input pair PMOS and additional PMOS load connected to ground should be of minimum feature size while the size of PMOS load with varying control voltage should be greater than all other.

The differential topology reduces the number of stages for higher frequency of oscillation.

5.2 Modified 3-stage proposed multi-loop CMOS ring VCO

The phase noise characteristic of proposed VCO is quite good but if we connect additional PMOS load with a varying bias voltage and not with ground. This architecture helps in improving phase noise performance but with the expense of increase in power dissipation.

The size of both the additional PMOS load with varying gate voltage determines the tuning range of VCO. The schematic of 3-stage modified proposed differential ring VCO is shown in Fig. 5.8.

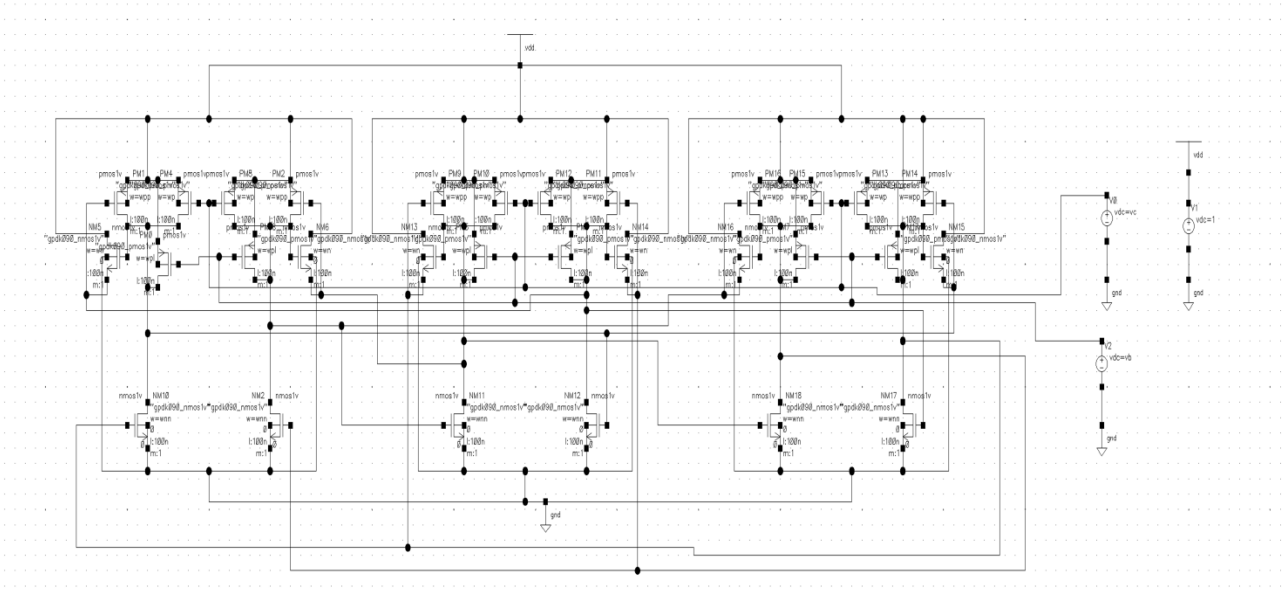


Fig. 5.8: Modified 3-stage Proposed Multi-loop Differential Ring VCO.

CHAPTER 6

RESULTS AND DISCUSSION

6.1 Experimental Work

6.1.1 CMOS inverter ring oscillator

Schematic of a single delay cell:

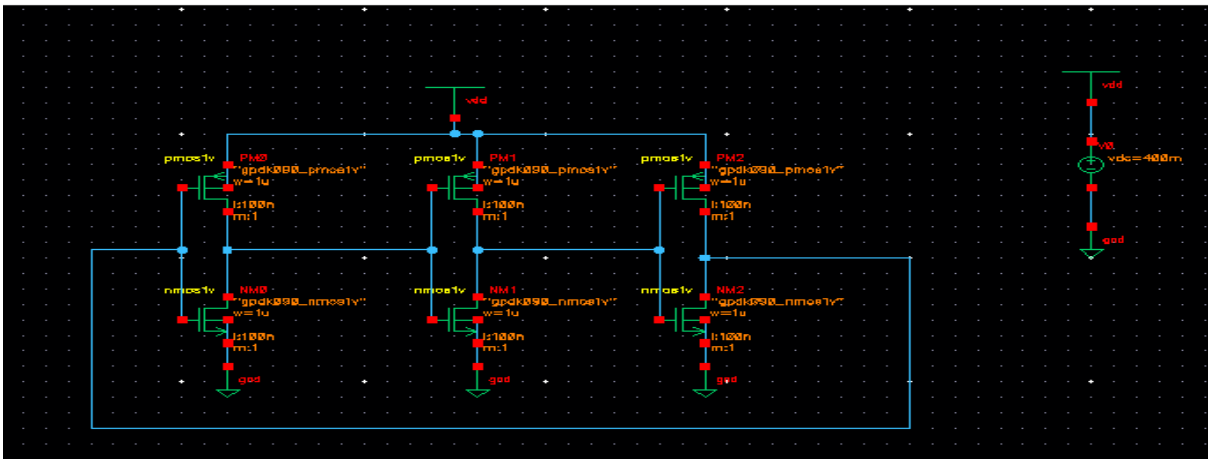


Fig. 6.1: Schematic of 3-stage CMOS inverter ring oscillator.

The transient response of 3-stage CMOS inverter ring oscillator for 0.4 supply voltage is shown in Fig. 6.1(a).

The frequency of oscillation is 1.24GHz.

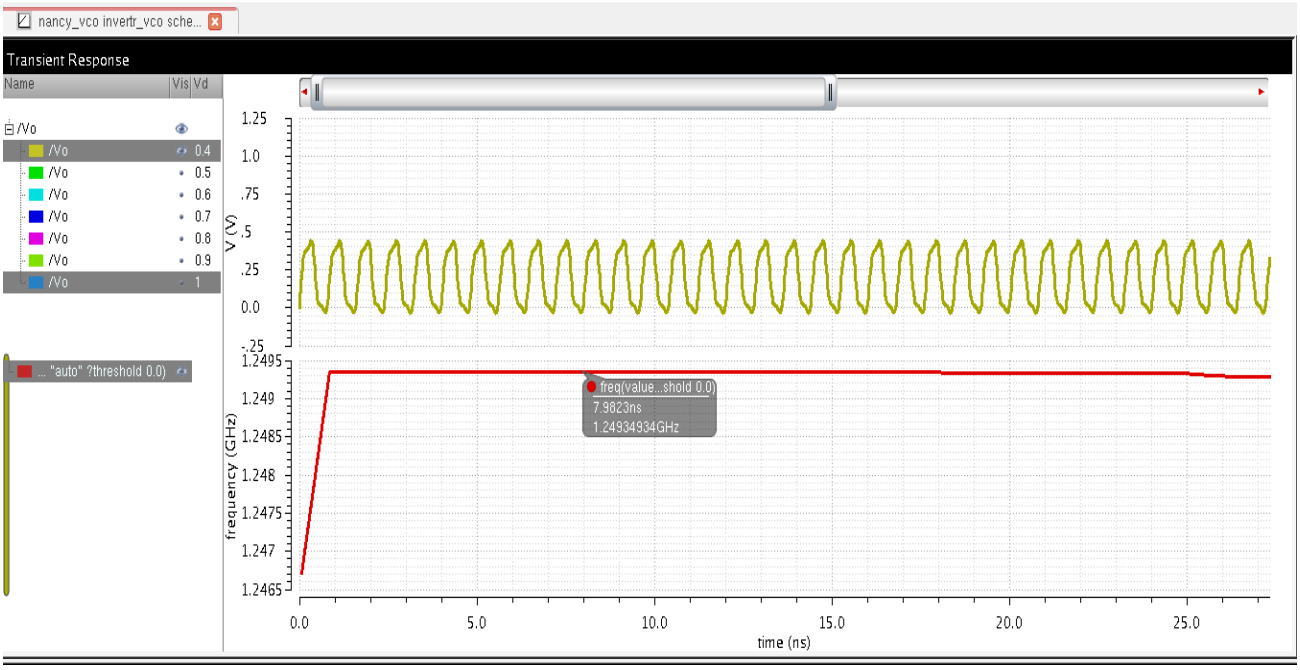


Fig. 6.1(a): Transient response of 3-stage CMOS inverter ring oscillator for 0.4 $V_{dd.}$

The transient response of 3-stage CMOS inverter ring oscillator for 0.5 supply voltage is shown in Fig. 6.1(b).

The frequency of oscillation is 3.02GHz.

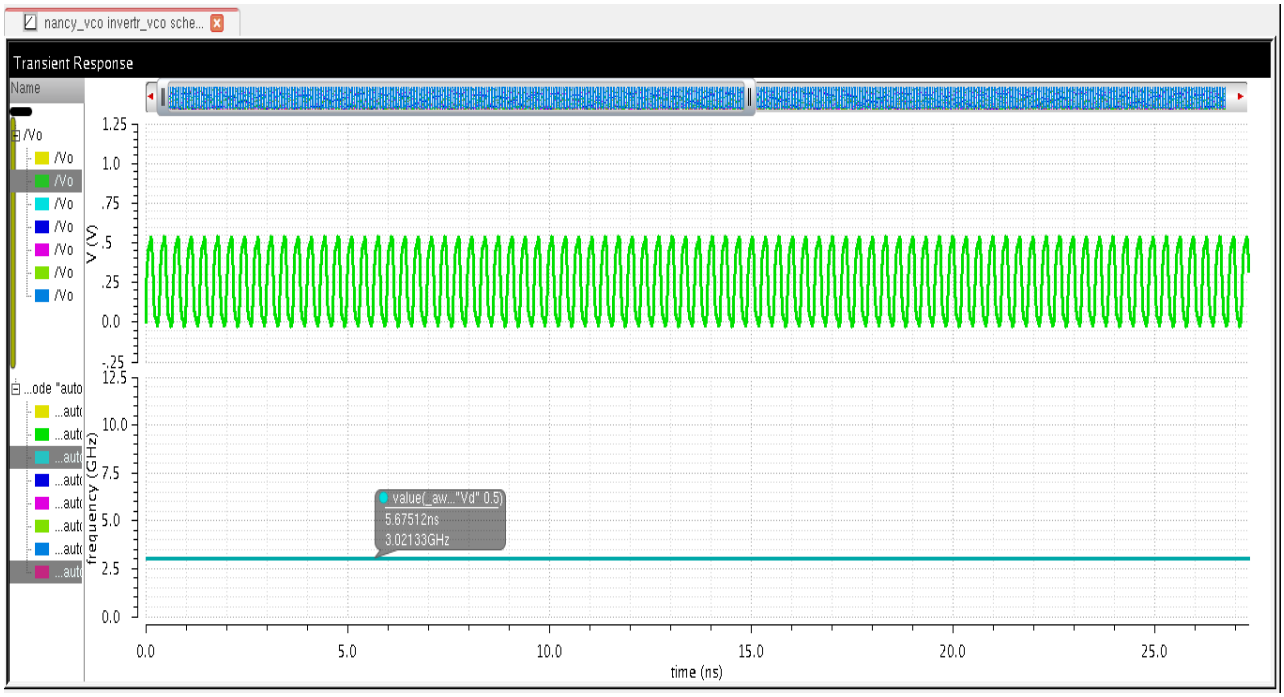


Fig. 6.1(b) Transient response of 3-stage CMOS inverter ring oscillator for 0.5 V_{dd}.

The transient response of 3-stage CMOS inverter ring oscillator for 0.6 supply voltage is shown in Fig. 6.1(c).

The frequency of oscillation is 5.05GHz.

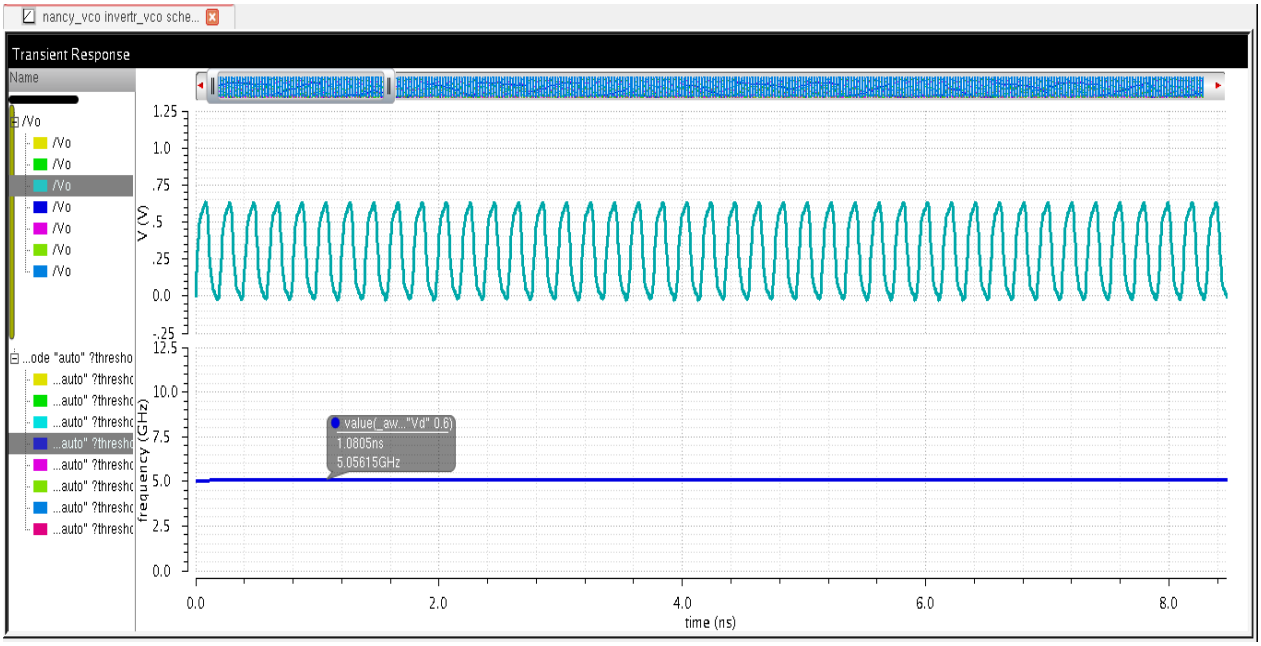


Fig. 6.1(c) Transient response of 3-stage CMOS inverter ring oscillator for 0.6 V_{dd}.

The transient response of 3-stage CMOS inverter ring oscillator for 0.7 supply voltage is shown in Fig. 6.1(d). The frequency of oscillation is 7.07GHz.

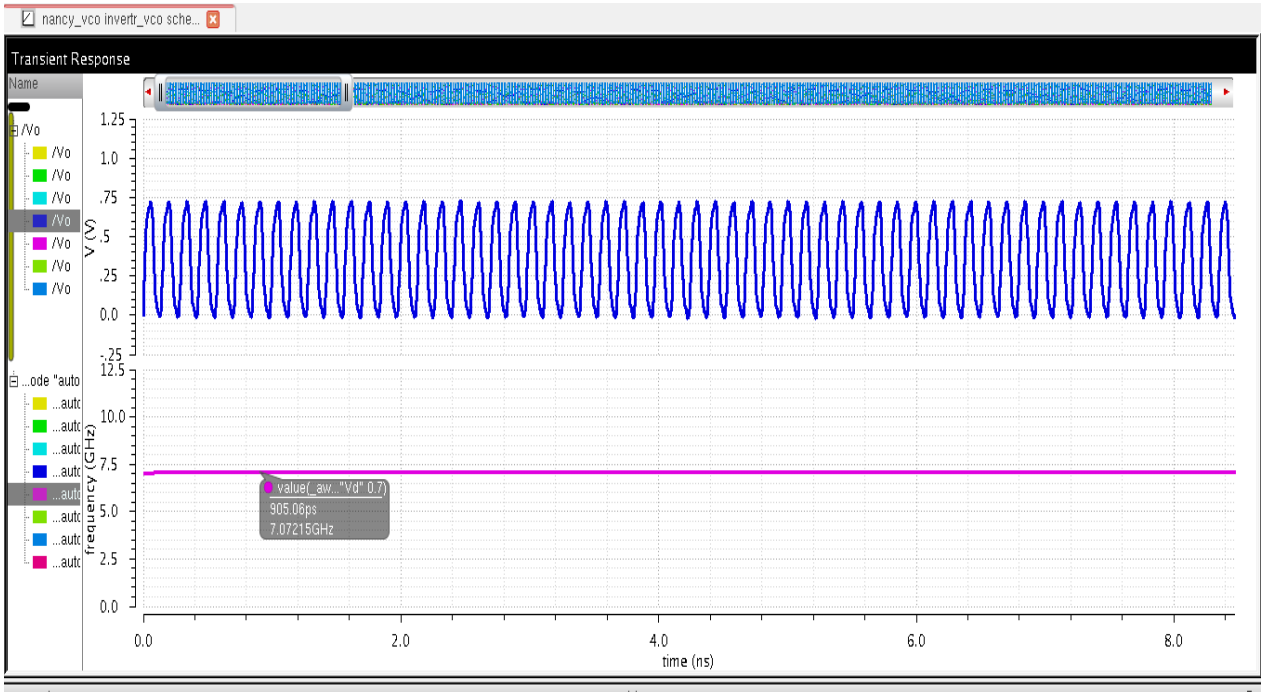


Fig. 6.1(d) Transient response of 3-stage CMOS inverter ring oscillator for 0.7 V_{dd}.

The transient response of 3-stage CMOS inverter ring oscillator for 0.8 supply voltage is shown in Fig. 6.1(e). The frequency of oscillation is 8.971GHz.

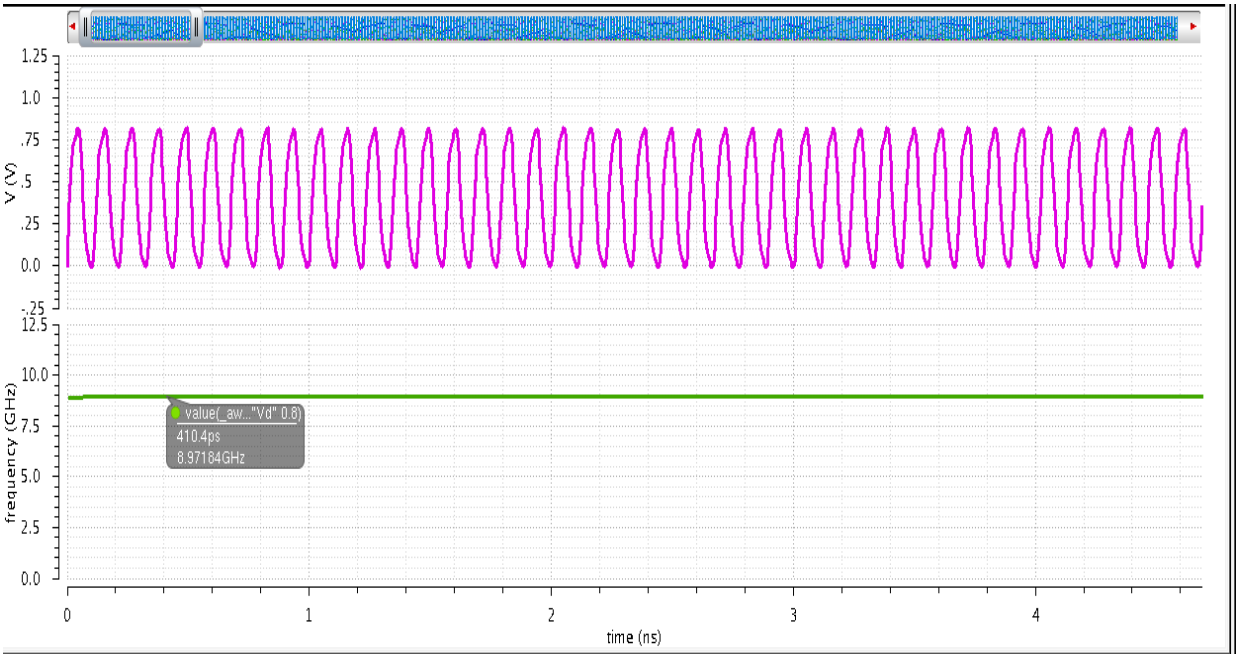


Fig. 6.1(e) Transient response of 3-stage CMOS inverter ring oscillator for 0.8 V_{dd}.

The transient response of 3-stage CMOS inverter ring oscillator for 0.9 supply voltage is shown in Fig. 6.1(f).

The frequency of oscillation is 10.724GHz.

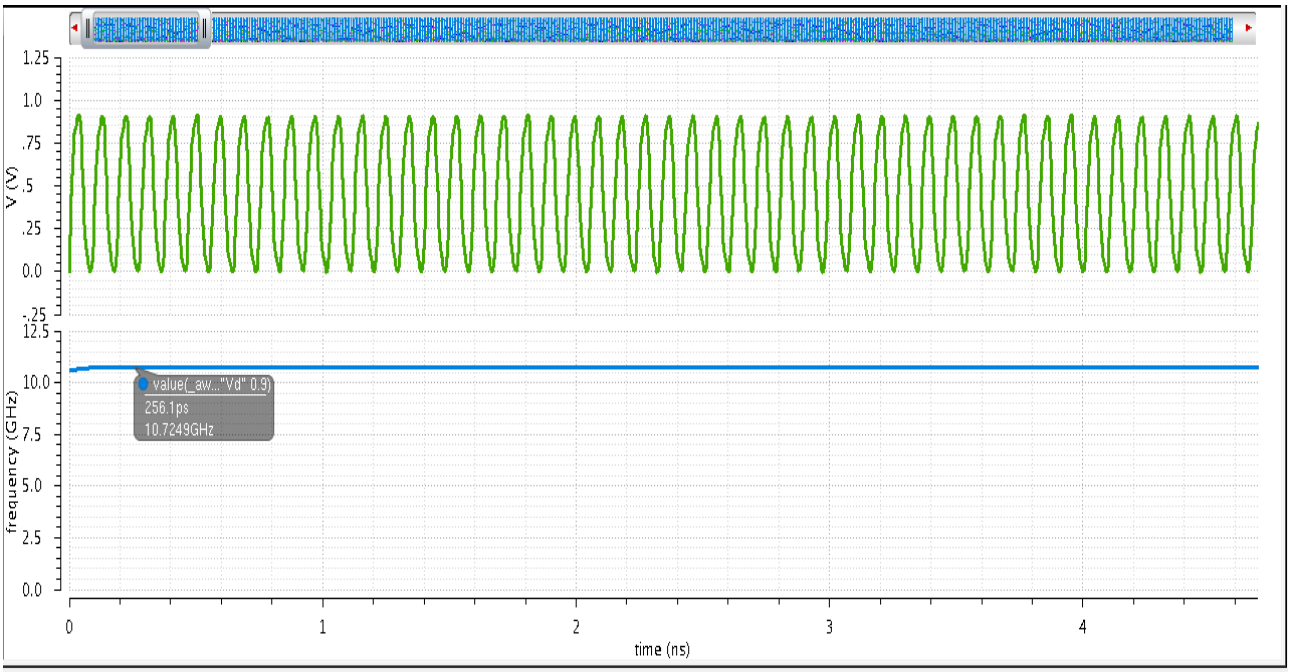


Fig. 6.1(f) Transient response of 3-stage CMOS inverter ring oscillator for 0.9 V_{dd}.

The transient response of 3-stage CMOS inverter ring oscillator for 1 supply voltage is shown in Fig. 6.1(g).

The frequency of oscillation is 12.325GHz.

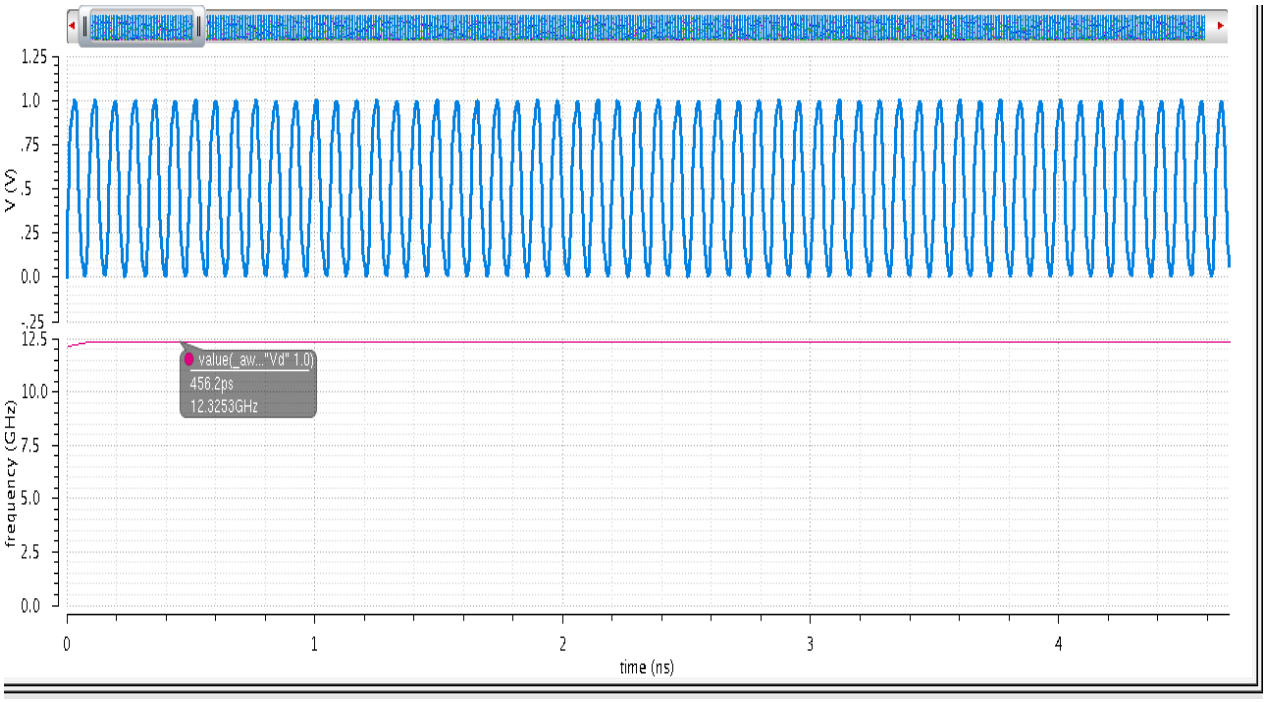


Fig. 6.1(g) Transient response of 3-stage CMOS inverter ring oscillator for 1 V_{dd}.

The power response of 3-stage CMOS inverter ring oscillator for 0.9 supply voltage is shown in Fig. 6.1(h) which is 267.14µW.

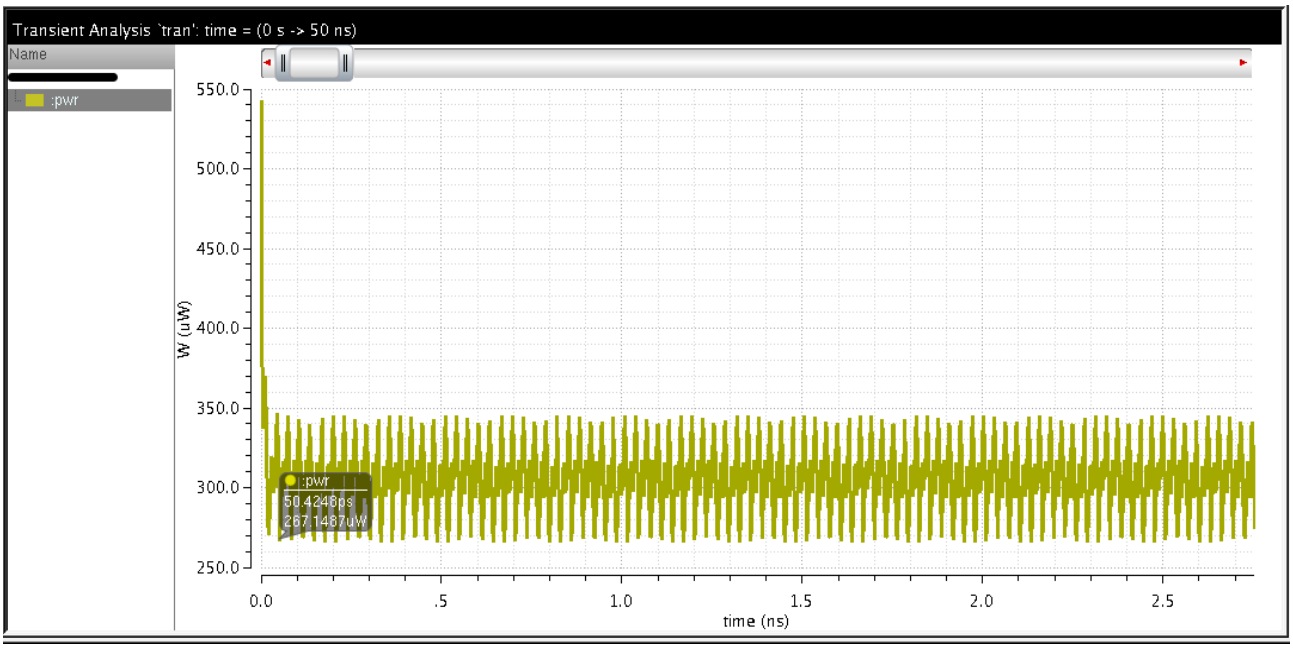


Fig. 6.1(h): Power response of 3-stage CMOS inverter ring oscillator for 0.9 supply voltage.

The periodic steady state response of 3-stage CMOS inverter ring oscillator for 0.9 supply voltage is shown in Fig. 6.1(i).

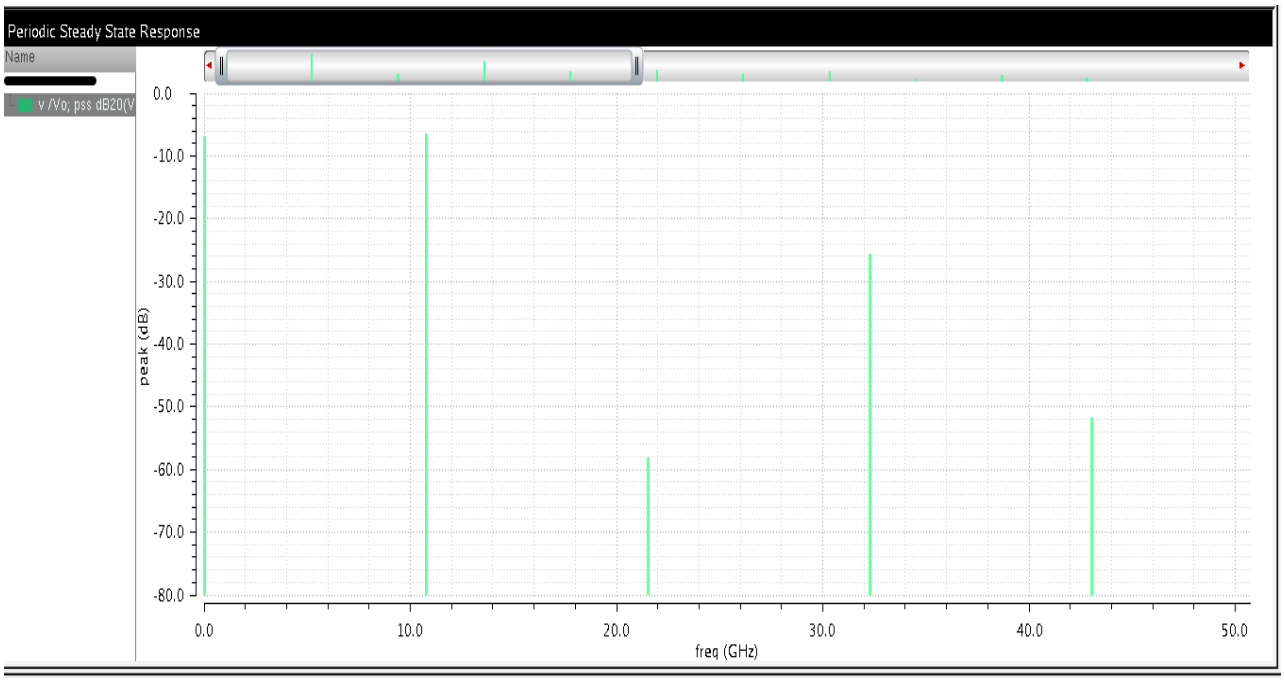


Fig. 6.1(i): Periodic Steady State response of 3-stage CMOS inverter ring oscillator for 0.9 V_{dd}.

The phase noise response of 3-stage CMOS inverter ring oscillator for 0.9 supply voltage is shown in Fig. 6.1(j) which is -98.03dBc/Hz.

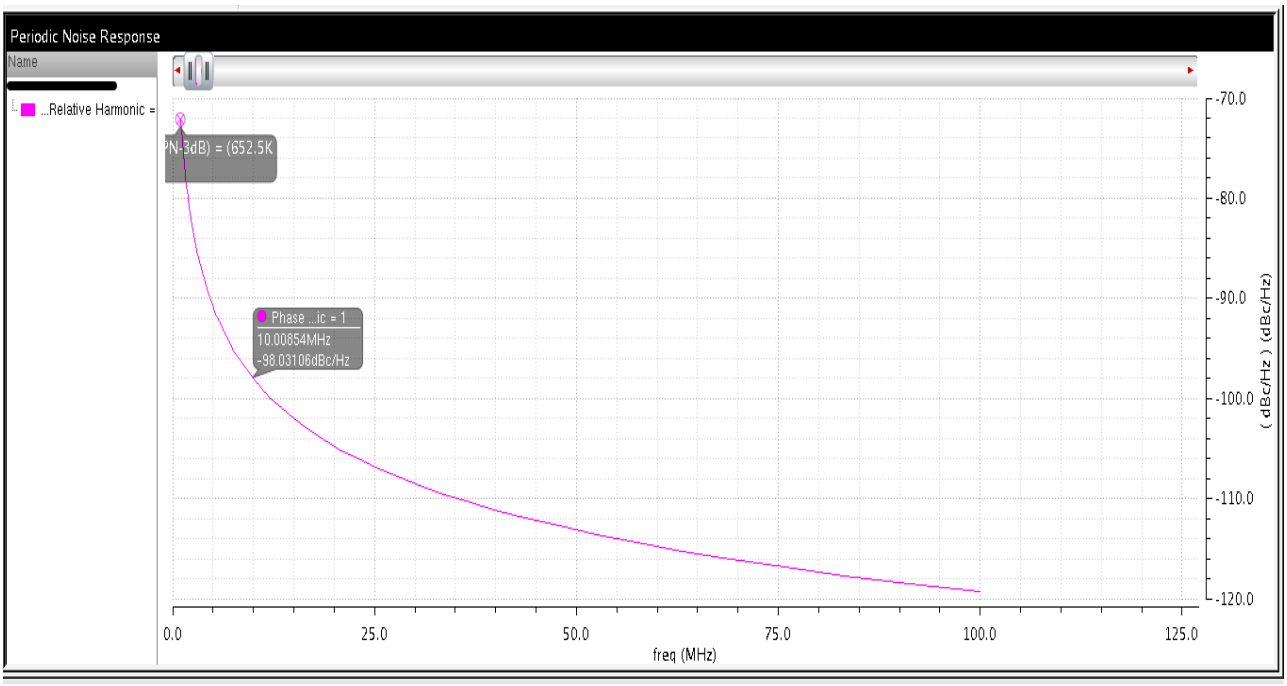


Fig. 6.1(j): Phase noise response of 3-stage CMOS inverter ring oscillator for 0.9 V_{dd}.

The performance table of CMOS inverter ring oscillator is tabulated in Table 1.3.

Table 1.3: Performance of CMOS inverter ring oscillator.

Power Supply (V)	Oscillation Frequency (GHz)	Power (µW)	Phase noise (dBc/Hz) @ 10MHz offset
0.4	1.24	9.31	
0.5	3.02	23.53	-98.61
0.6	5.05	60.55	-98.60
0.7	7.07	106.05	-98.33
0.8	8.971	172.74	-98.26
0.9	10.724	267.14	-98.05
1	12.325	393.97	-97.76

6.1.2 3-stage Single-ended CMOS ring VCO with PMOS load

The schematic with varying PMOS load is shown in Fig. 6.2(a) and 6.2(b):

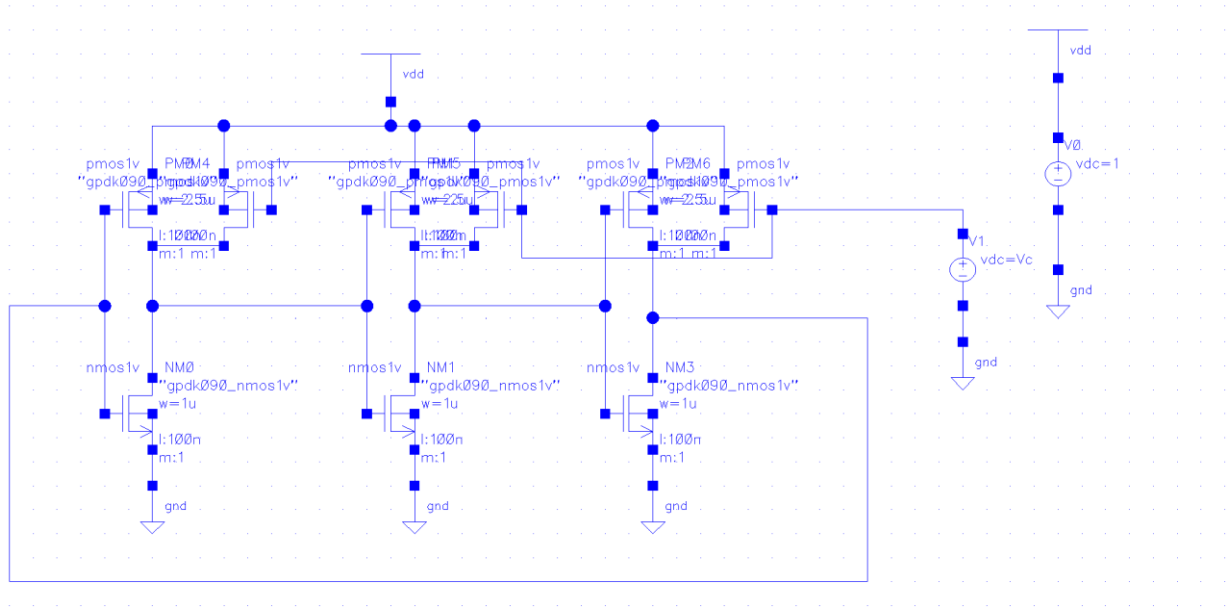


Fig. 6.2(a): Schematic of 3-stage single0ended ring VCO with varying PMOS load.

The transient response of single-ended with varying PMOS load is shown in Fig. 6.2(b):

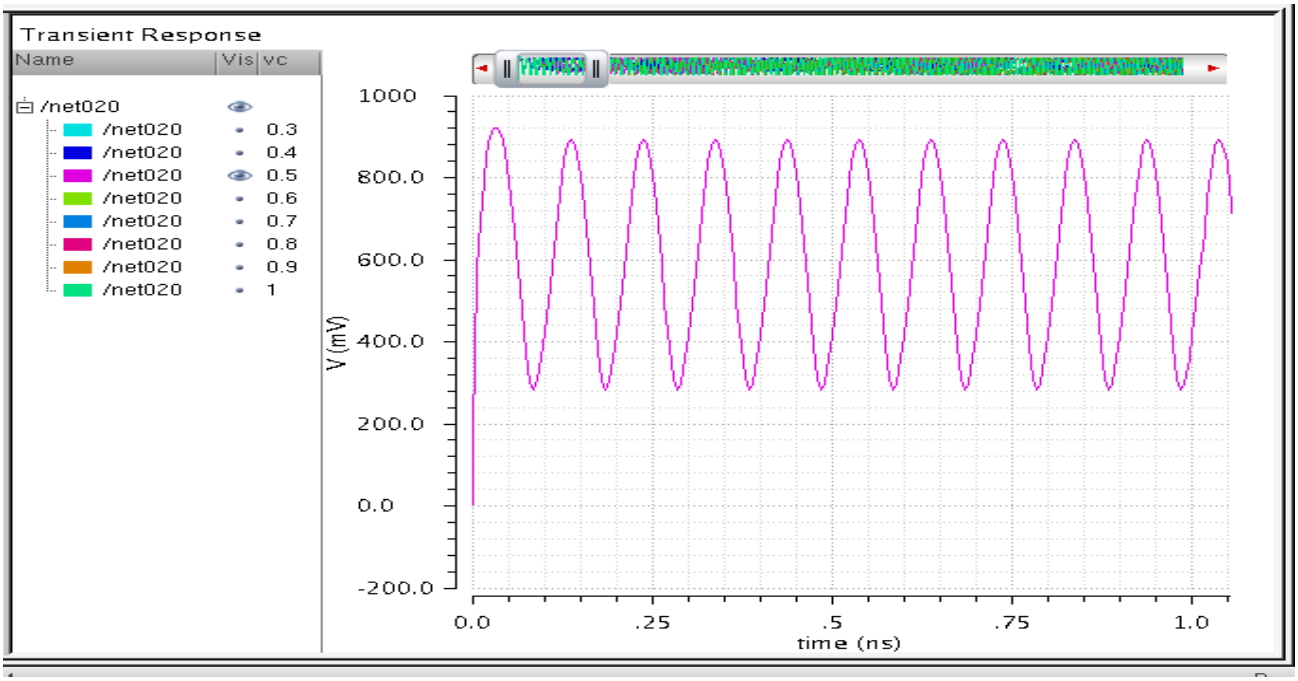


Fig. 6.2(b): Transient response of single-ended with varying PMOS load.

The transient response of single-ended with varying PMOS load with frequency of 9.85GHz in Fig. 6.2(c).

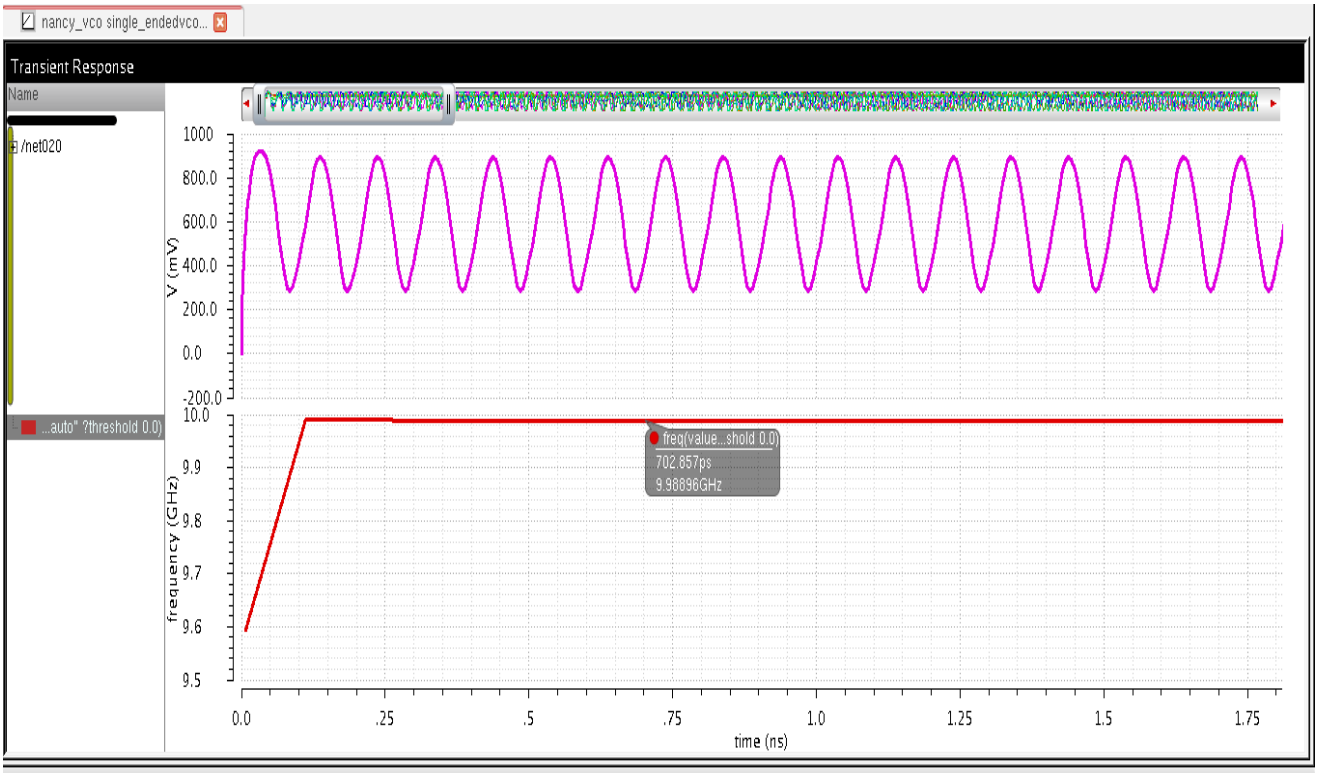


Fig. 6.2(c): Transient response of single-ended with varying PMOS load.

The phase noise response of single-ended with varying PMOS load with frequency of oscillation 9.85GHz is -87.689dBc/Hz with 0.04mW power dissipation

The performance table of CMOS ring VCO with PMOS load is tabulated in Table 1.4.

Table 1.4: Performance of CMOS ring VCO with PMOS load.

Control Voltage (V)	Frequency (GHz)	Power (µW)	Phase Noise (dBc/Hz) @ 10MHz offset
0.2	11.34	70	
0.3	10.77		
0.4	10.25		
0.5	9.85	40.10	-87.689
0.6	9.60		
0.7	9.52		
0.8	9.52		
0.9	9.52		
1	9.52	34	

6.1.3 3-stage Single-ended CMOS ring VCO with inductive load

The schematic of single-ended ring VCO with inductive load with oscillation frequency 9.989GHz is shown in Fig.6.3(a):

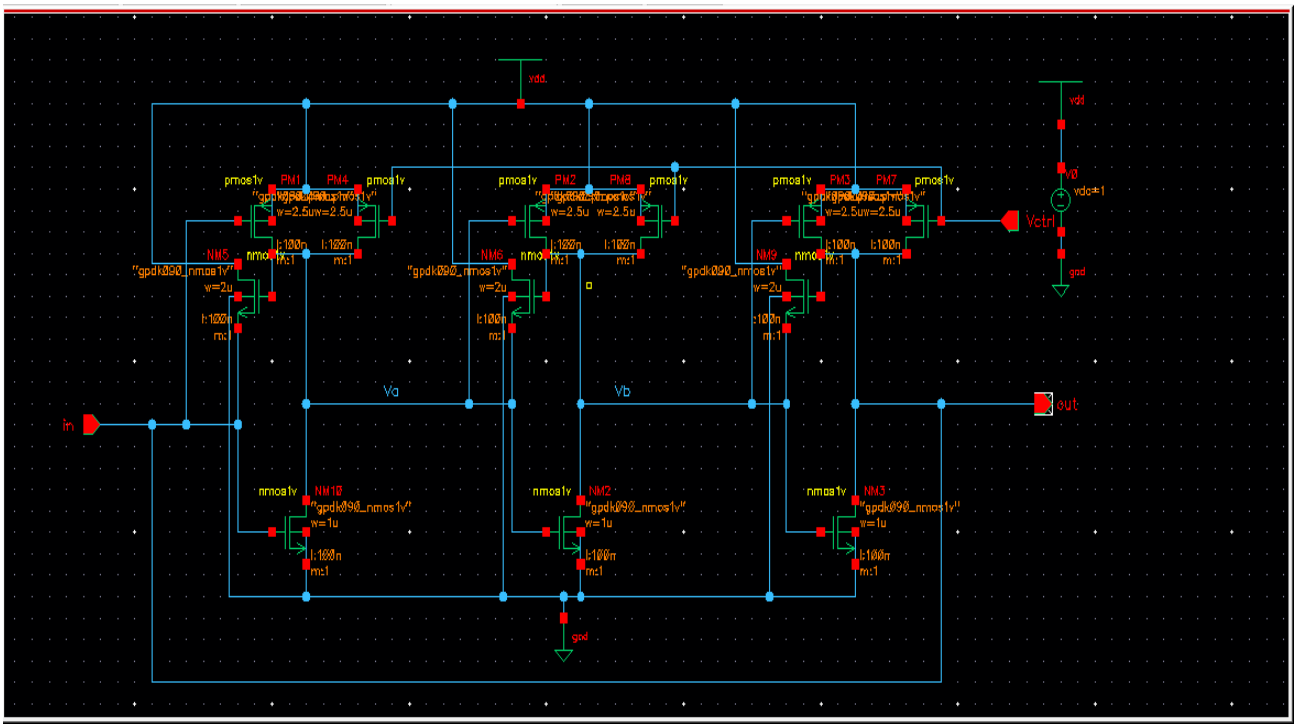


Fig. 6.3(a): Schematic of 3-stage single-ended ring VCO with inductive load.

The power response of 3-stage single-ended ring VCO with inductive load results in 0.677mW is shown in Fig. 6.3(b):

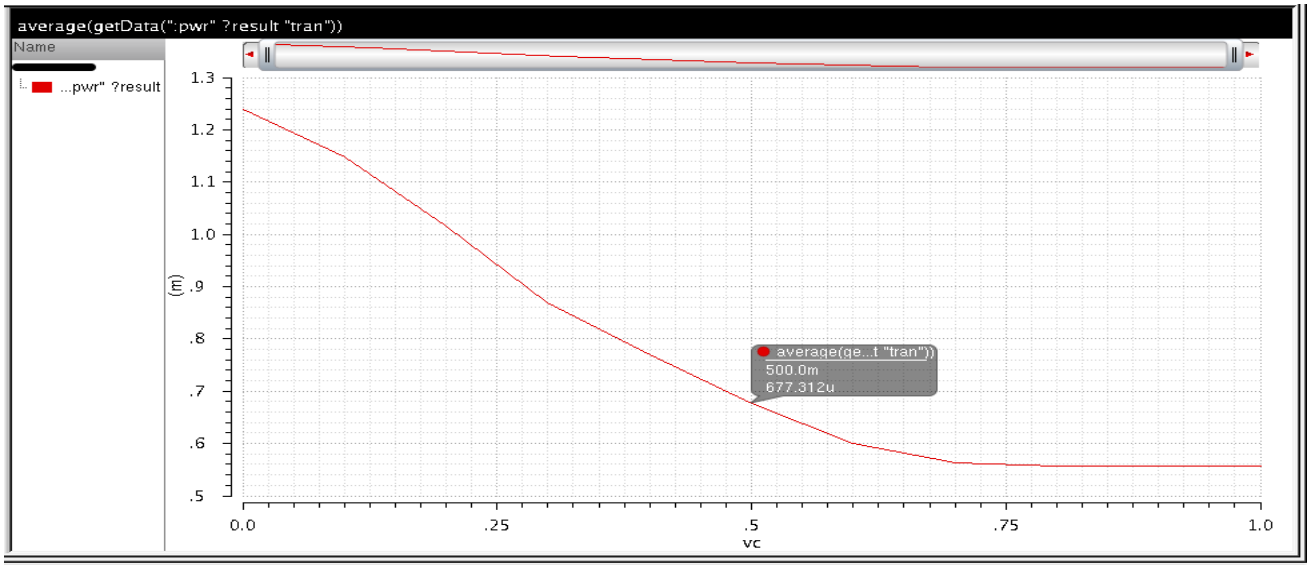


Fig. 6.3 (b): Power response of 3-stage single-ended ring VCO with inductive load.

The phase noise response is -97.436dBc/Hz @ 10MHz offset from center frequency is shown in Fig. 6.3(c).

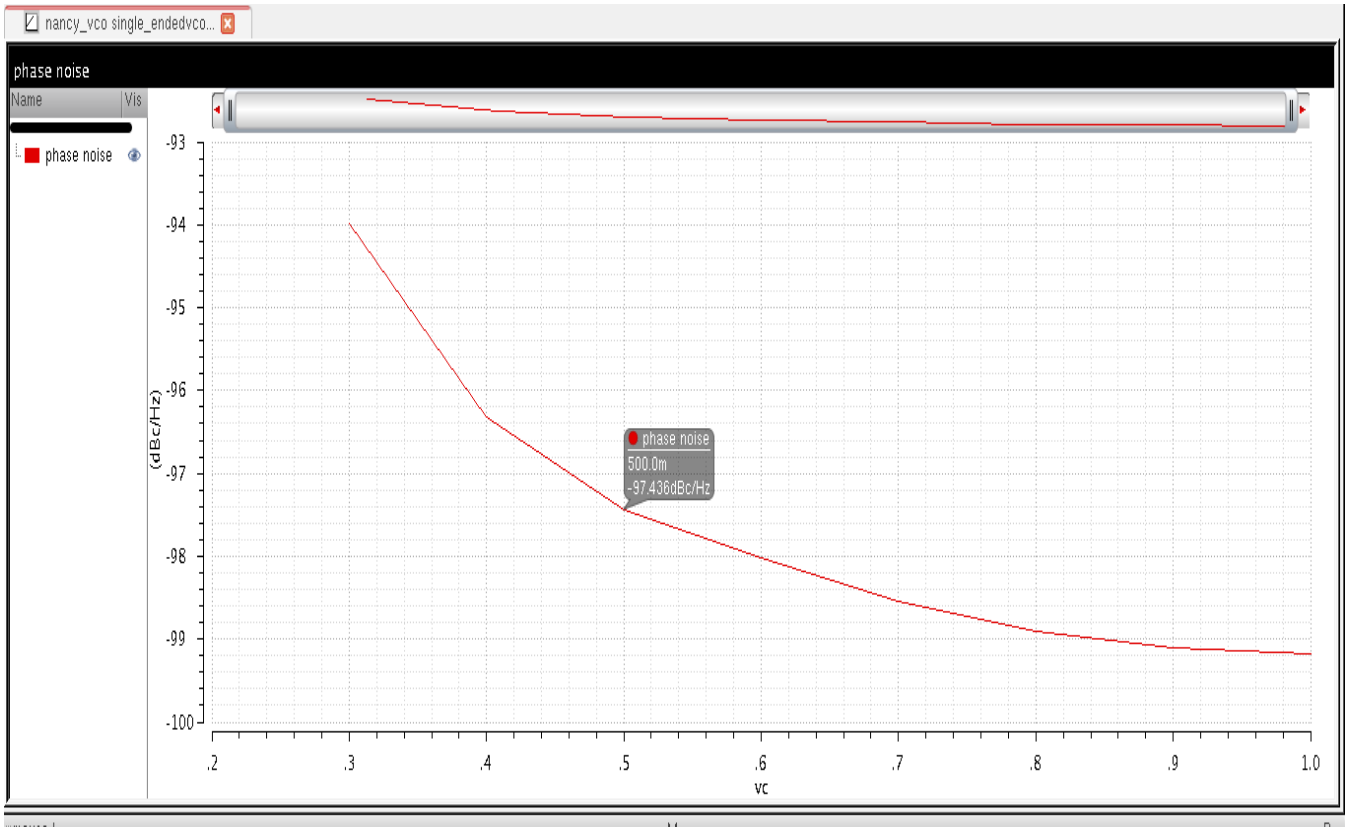


Fig. 6.3(c): Phase noise response of 3-stage single-ended ring VCO with inductive load.

The performance table of CMOS ring VCO with inductive load is tabulated in Table 1.5.

Table 1.5: Performance of CMOS ring VCO with inductive load.

Control Voltage (V)	Frequency (GHz)	Power (µW)	Phase Noise (dBc/Hz) @ 10MHz offset
0.3	8.84		
0.4	9.58		
0.5	9.989	677.3	-97.436
0.6	10.19		
0.7	10.24		
0.8	10.26		
0.9	10.26		
1	10.26		

6.1.4 3-stage multi-loop CMOS ring VCO with inductive load

The block diagram of 3-stage differential multi-loop ring VCO with inductive load is shown in 6.4(a):

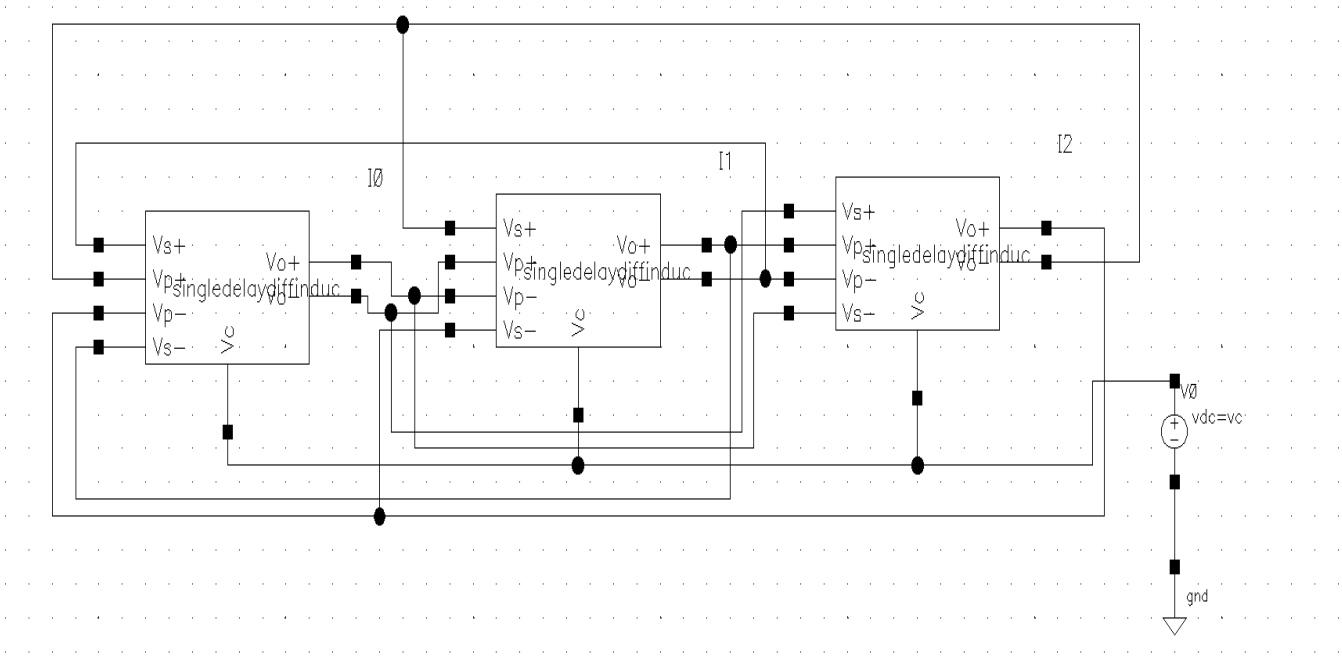


Fig. 6.4 (a): Block diagram of 3-stage differential multi-loop ring VCO with inductive load.

The frequency of oscillation is 10.40GHz.

The power response which is 1.5mW is shown in Fig. 6.4(b).

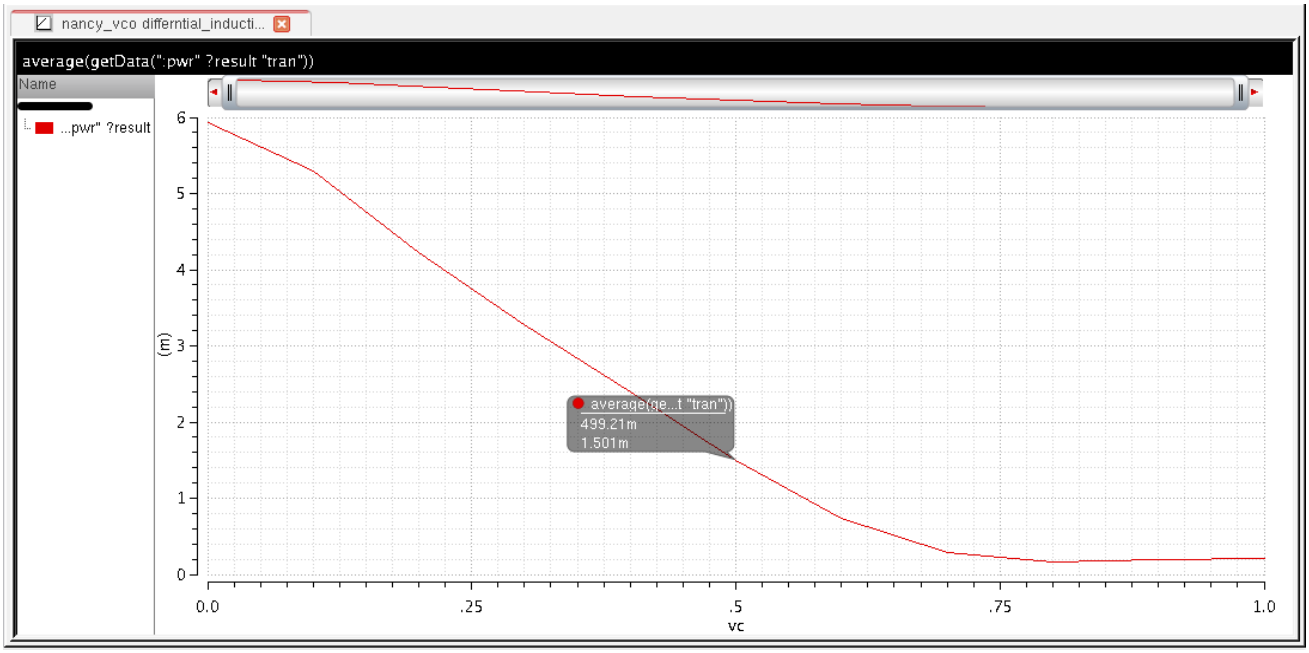


Fig. 6.4 (b): Power response.

The periodic steady state response is shown in Fig. 6.4(c):

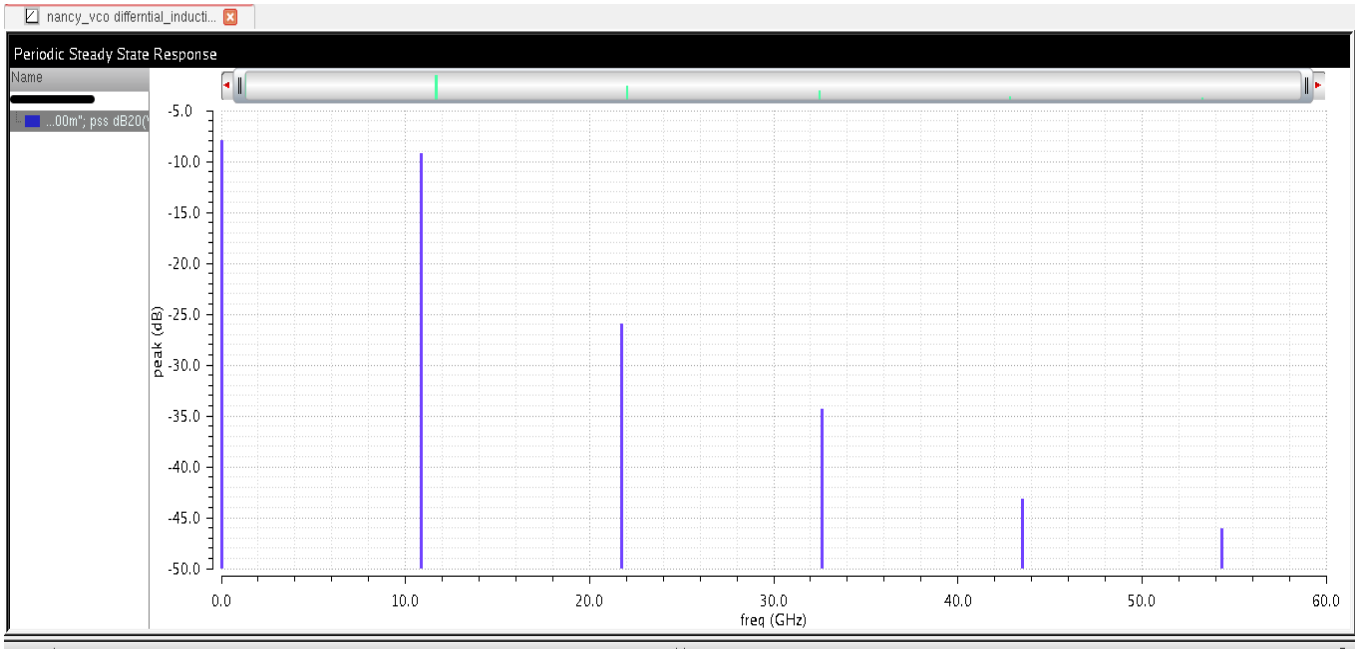


Fig. 6.4 (c): Periodic steady state response.

The phase noise is -119.02dBc/Hz at 100MHz offset is shown in Fig. 6.4(d).

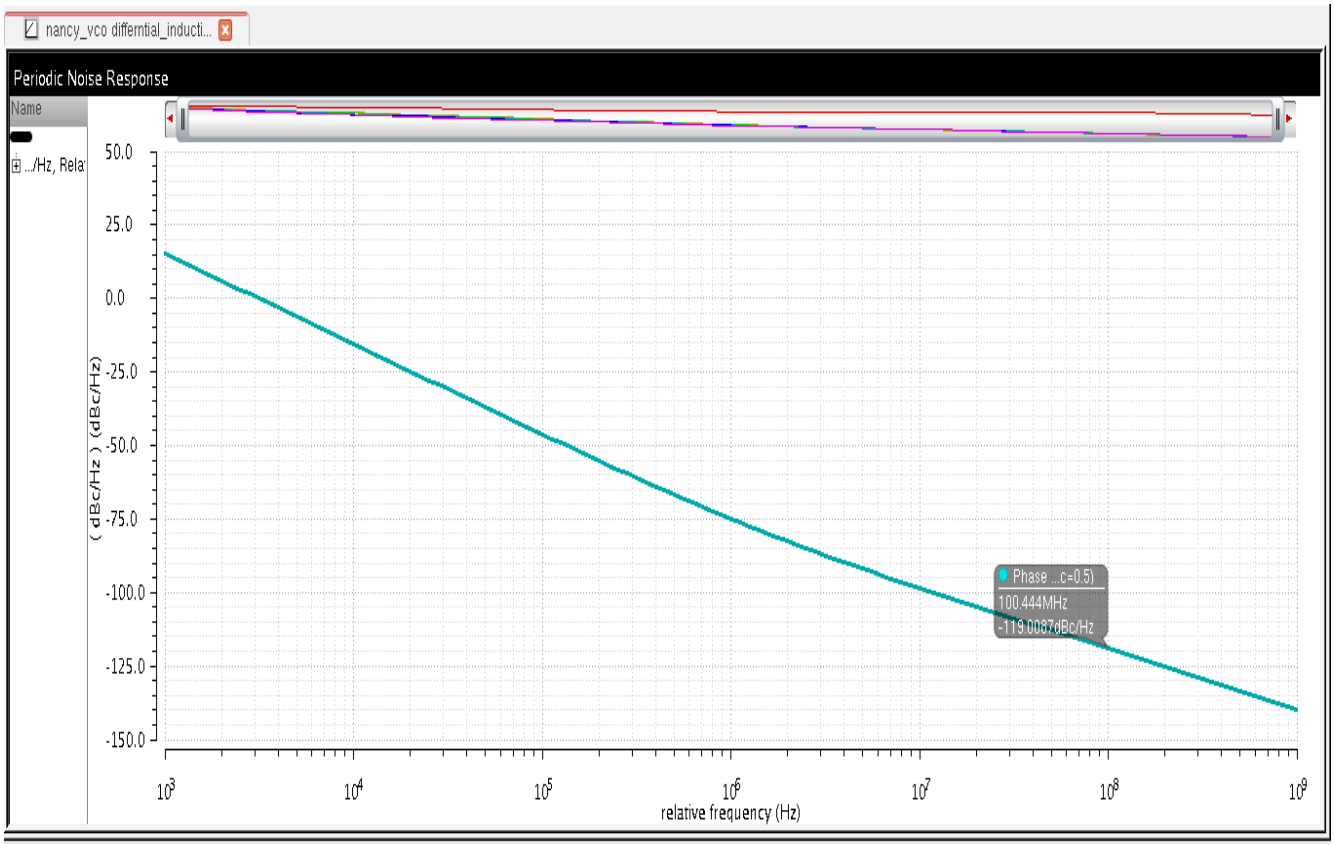


Fig. 6.4 (d): Phase noise response.

The phase noise response with respect to each control voltage is shown in Fig. 6.4(e).

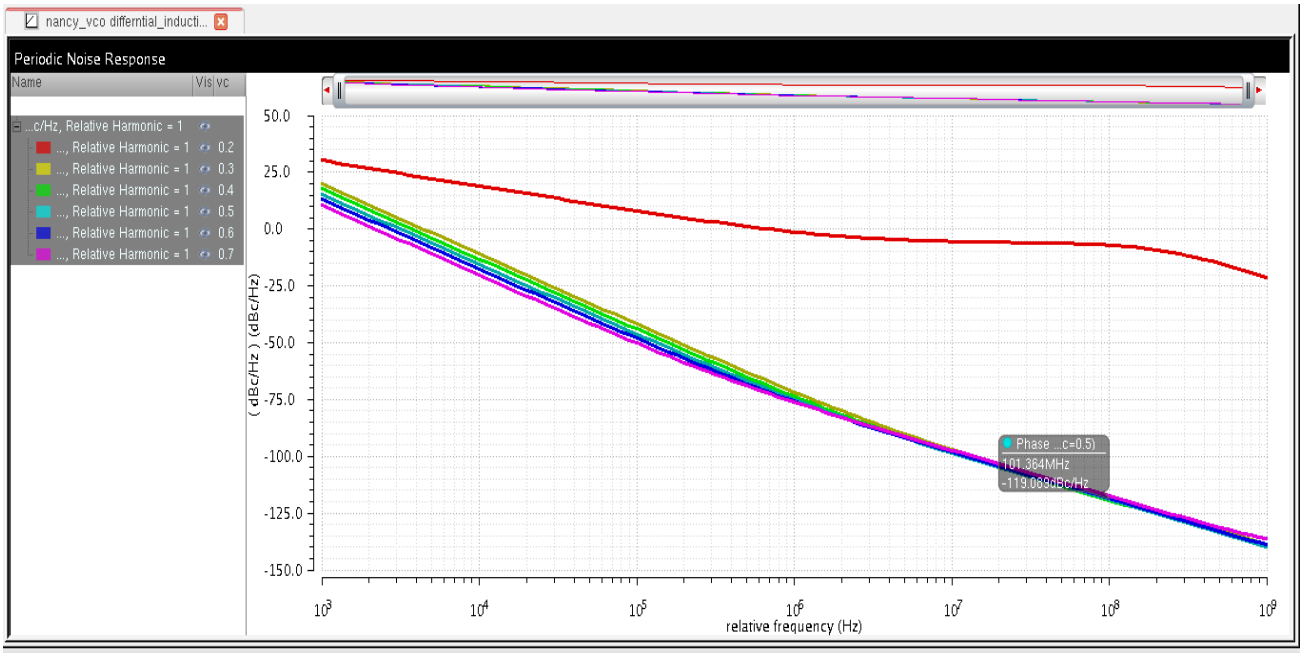


Fig. 6.4(e): Phase noise response corresponds to each control voltage.

The performance table of 3-stage differential multi-loop ring VCO with inductive load is tabulated in Table 1.6.

Table 1.6: Performance of 3-stage differential multi-loop ring VCO with inductive load.

Control Voltage (V)	Frequency (GHz)	Power (mW)	Phase Noise (dBc/Hz) @ 10MHz offset
0.2	23.42		
0.3	19.22		
0.4	14.76		
0.5	10.40	1.5	-98.43
0.6	5.96		
0.7	2.19		

6.1.5 Proposed 3-stage multi-loop CMOS ring VCO additional PMOS load

The schematic of proposed ring VCO is shown in Fig. 6.5(a).

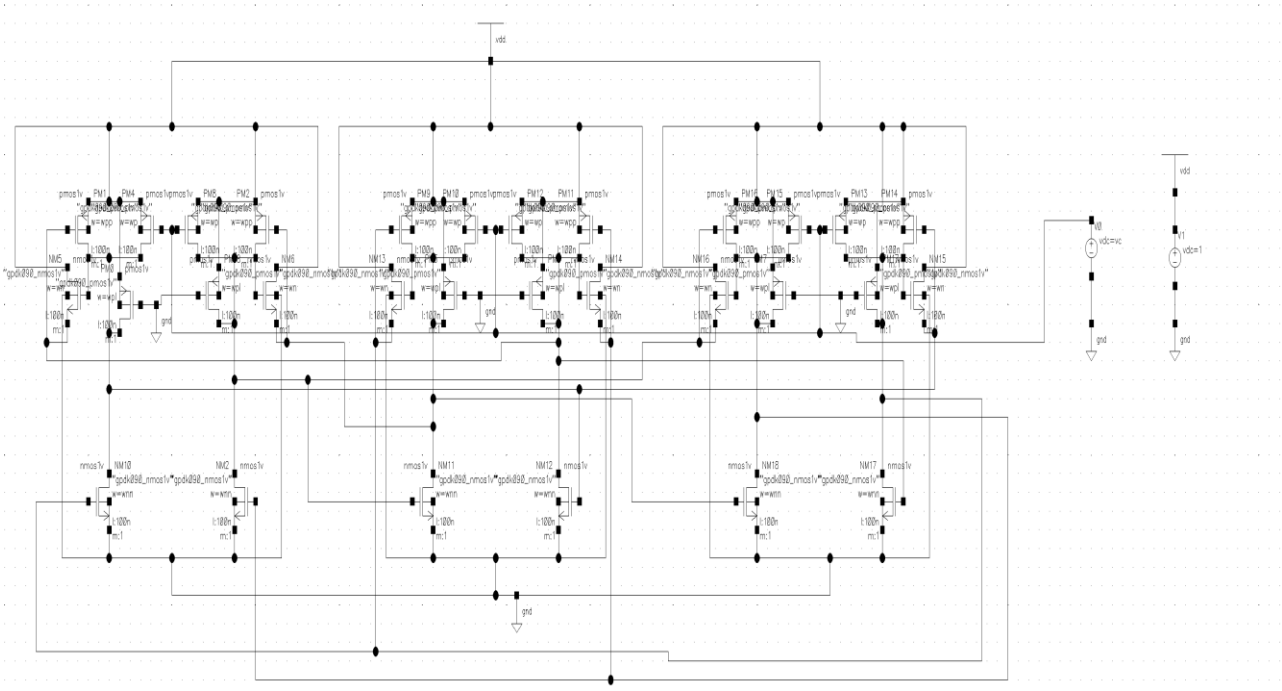


Fig. 6.5(a): Schematic of proposed ring VCO

The transient response is shown in Fig.6.5 (b).

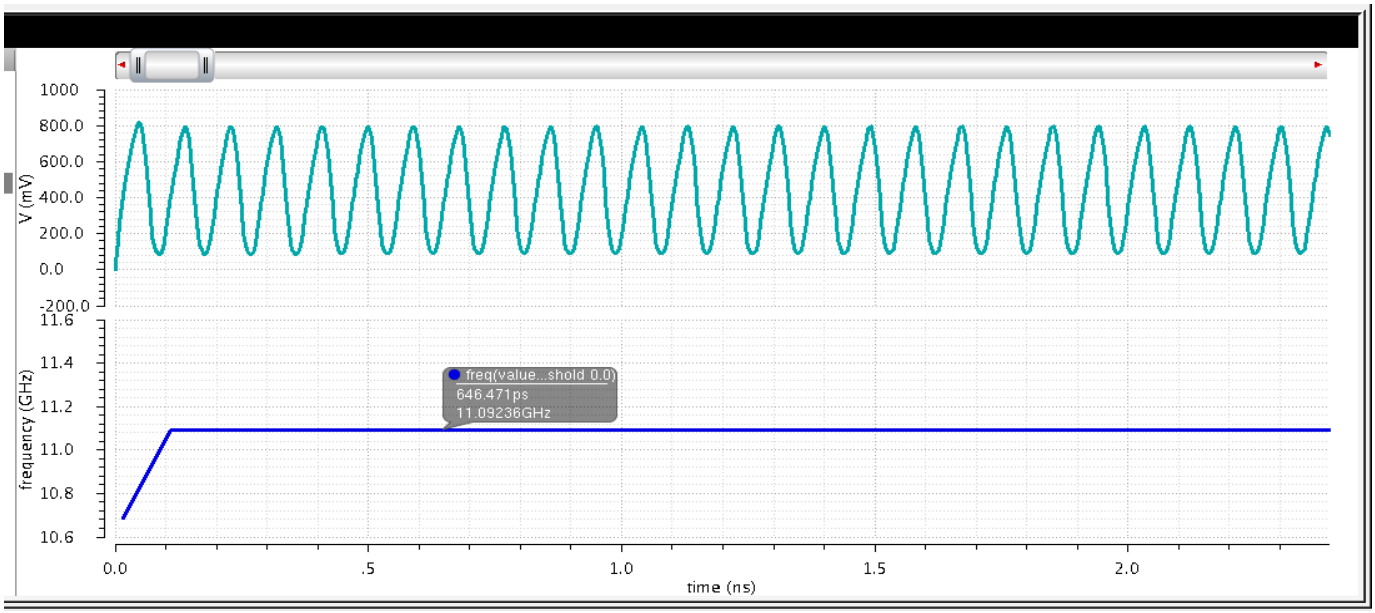


Fig.6.5 (b): Transient response.

The periodic steady state response is shown in Fig. 6.5 (c).

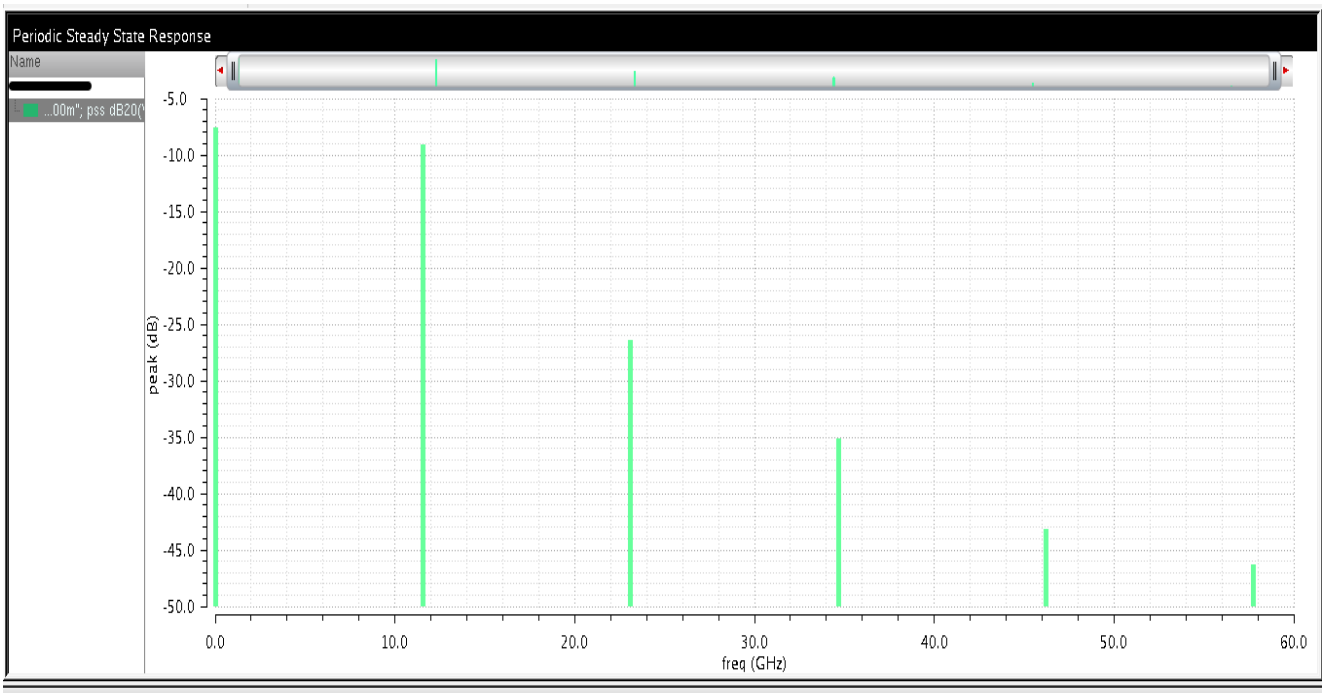


Fig.6.5(c): Periodic steady state response

The power response is 1.64mW shown in Fig. 6.5 (d).

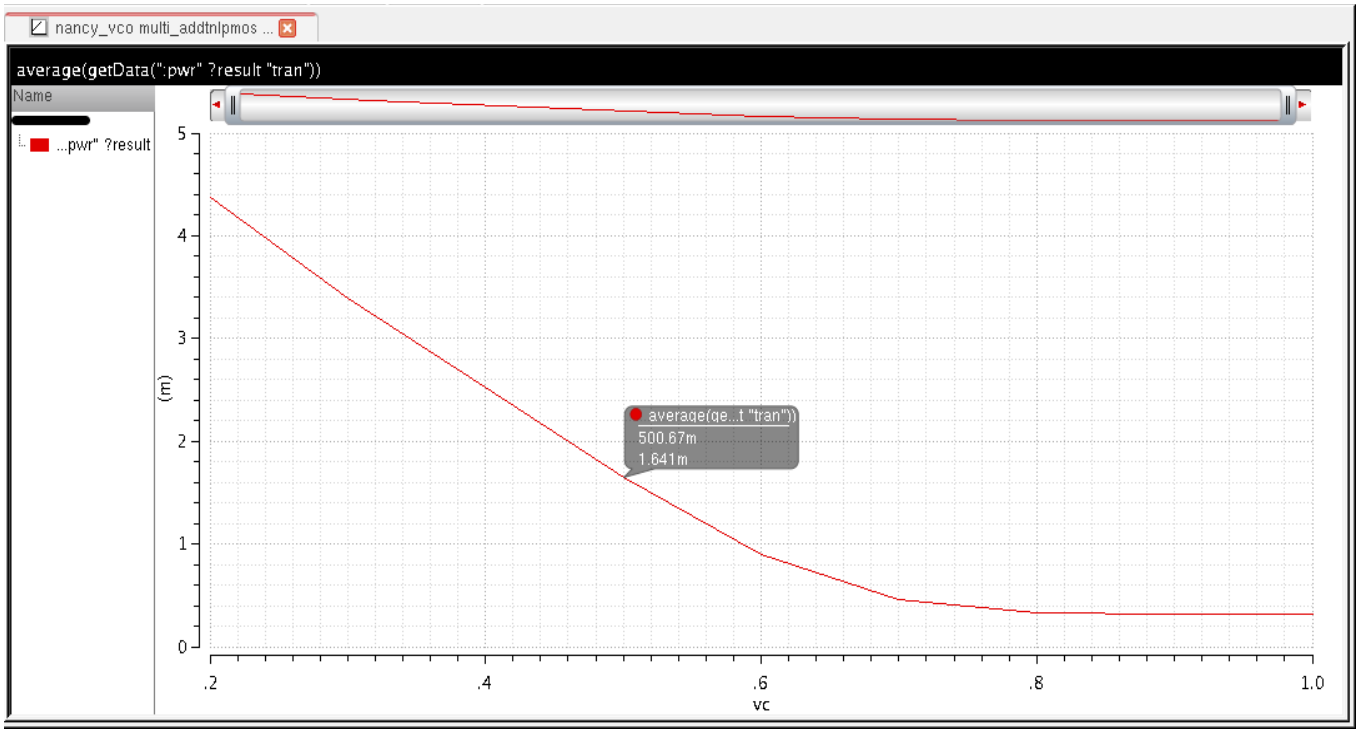


Fig. 6.5 (d): Power response.

The phase noise response is -95.84dBc/Hz is shown in Fig. 6.5 (e).

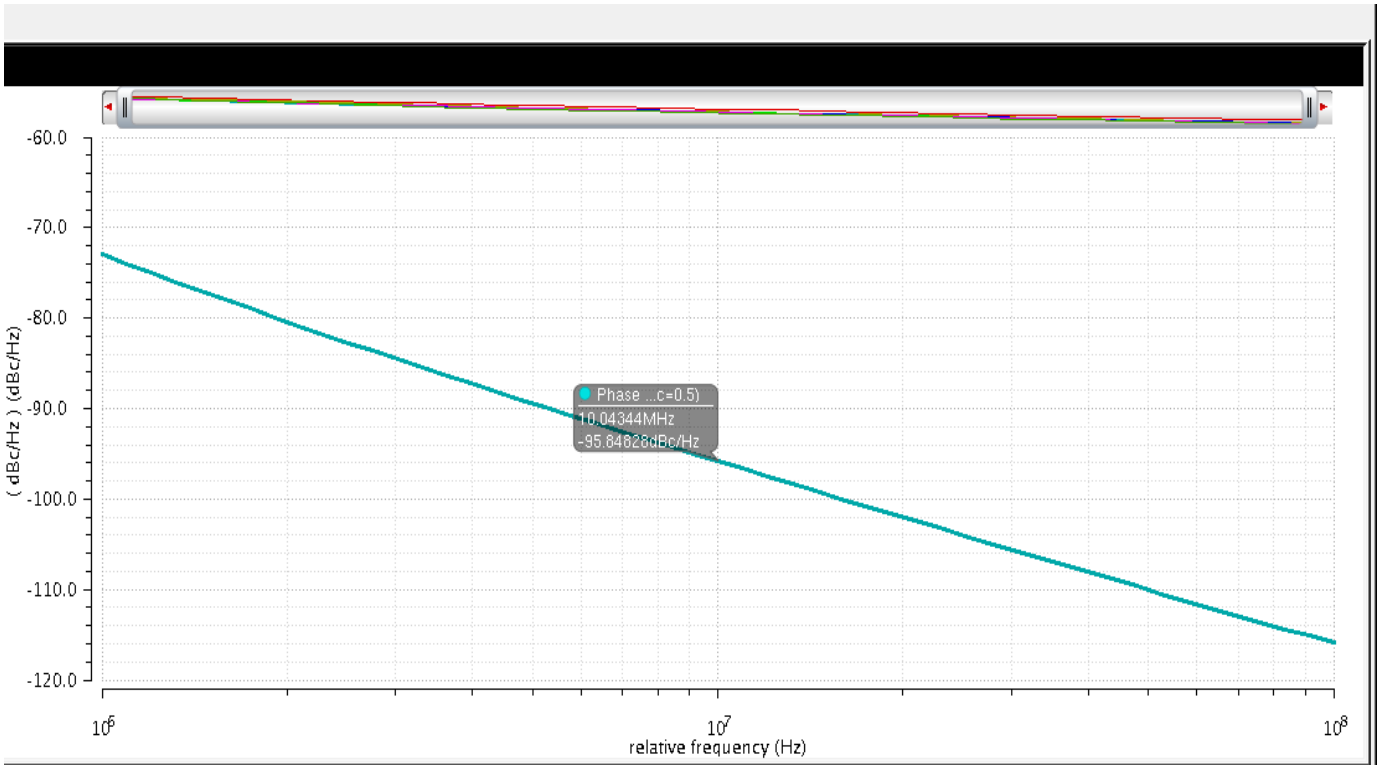


Fig. 6.5 (e): Phase noise response.

The performance table of proposed 3-stage multi-loop CMOS ring VCO additional PMOS load is tabulated in Table 1.7.

Table 1.7: Performance of proposed 3-stage multi-loop CMOS ring VCO additional PMOS load.

Control Voltage (V)	Frequency (GHz)	Power (mW)	Phase Noise (dBc/Hz) @ 10MHz offset
0.2	23.63	4.378	-90.55
0.3	19.62	3.397	-94.48
0.4	15.29	2.522	-95.87
0.5	11.09	1.646	-95.81
0.6	6.95	0.898	-95.71
0.7	3.601	0.457	-95.94
0.8	2.37	0.332	-97.34
0.9	2.27	0.318	
1	2.23	0.317	

Adjusting the PMOS load transistor sizes to achieve X-band tuning range. When width of both PMOS load is set to 500nm, the frequency is 9.49GHz.

The transient response is shown in Fig. 6.6(a).

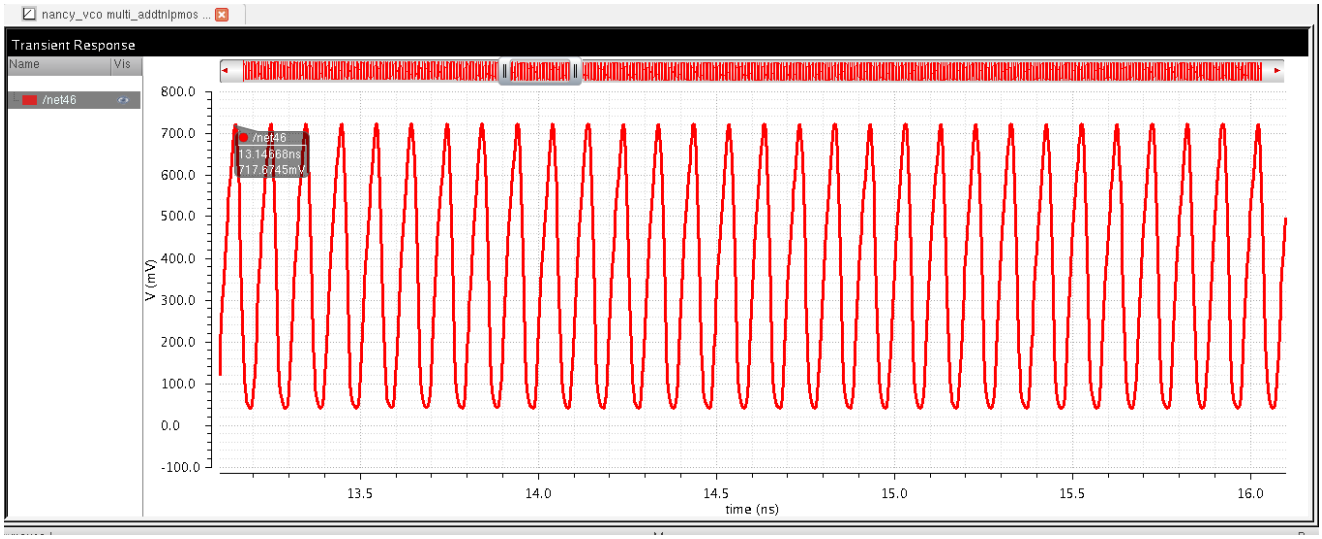


Fig. 6.6(a): Transient response.

The power response is shown in Fig. 6.6(b).

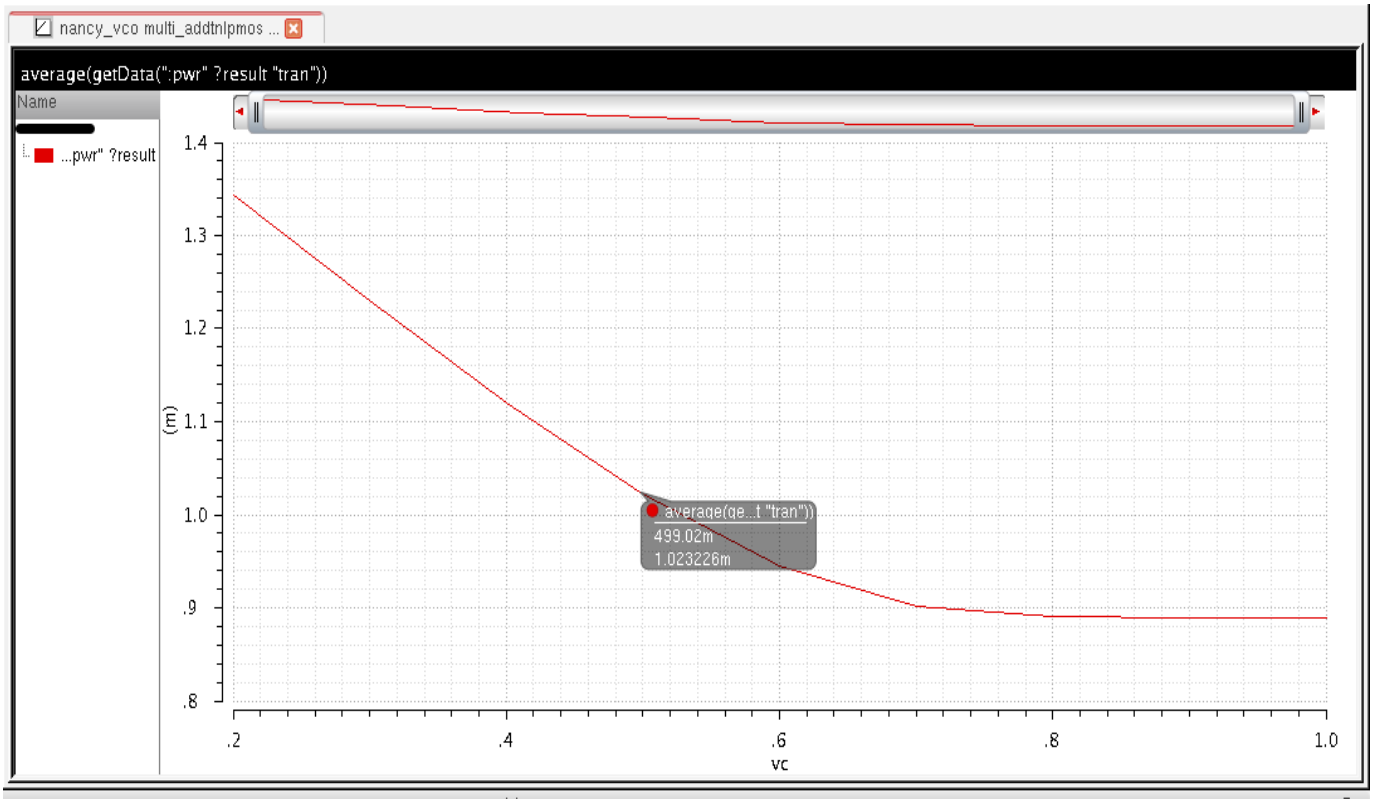


Fig. 6.6(b): Power response.

The periodic steady state response is shown in Fig. 6.6(c).

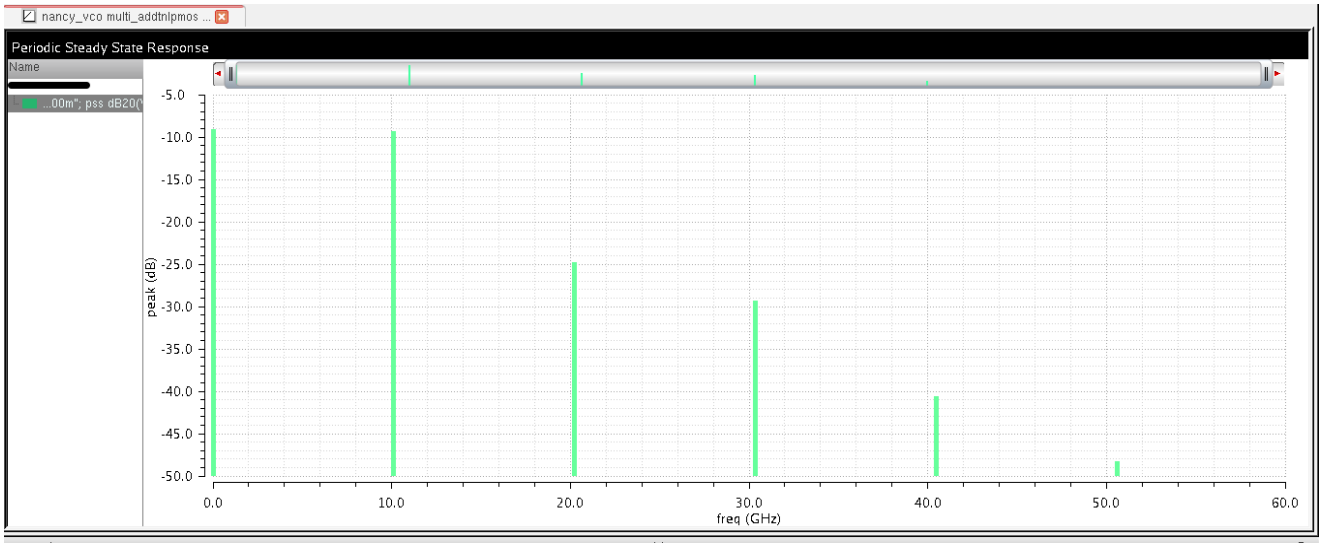


Fig. 6.6(c): Periodic steady state response.

The phase noise response is shown in Fig. 6.6(d).

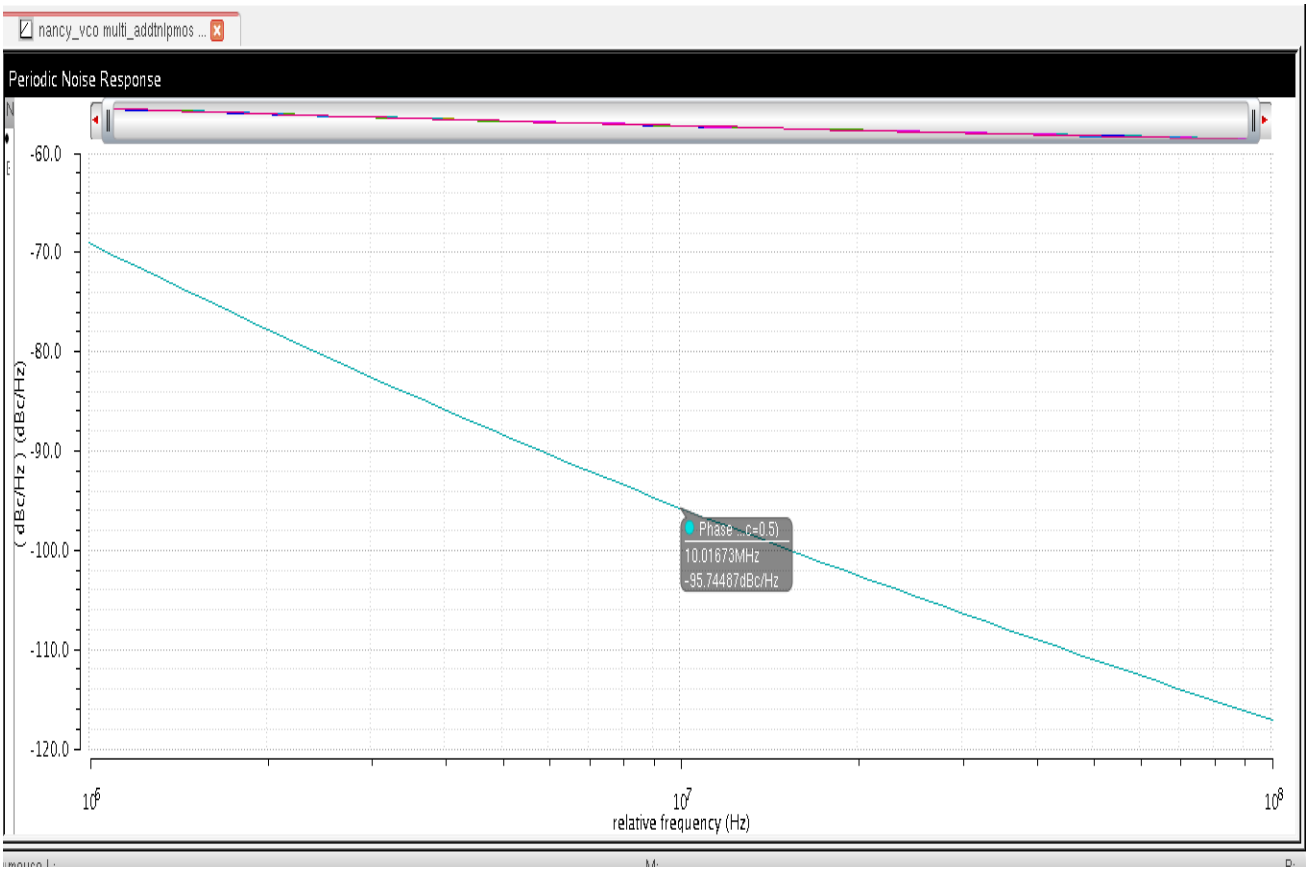


Fig. 6.6(d): Phase noise response.

The performance table of proposed 3-stage multi-loop CMOS ring VCO is tabulated in Table 1.8.

Table 1.8: Performance of proposed 3-stage multi-loop CMOS ring VCO.

Control Voltage (V)	Frequency (GHz)	Power (mW)	Phase Noise (dBc/Hz) @ 10MHz offset
0.2	11.91	1.343	-95.56
0.3	11.05	1.230	-95.71
0.4	10.24	1.120	
0.5	9.49	1.023	-95.79
0.6	8.85	0.945	-95.85
0.7	8.47	0.901	-96
0.8	8.36	0.890	-96.15
0.9	8.34	0.888	-96.25
1	8.34	0.888	-96.26

6.1.6 Modified 3-stage proposed multi-loop CMOS ring VCO

The schematic of modified proposed ring VCO is shown in Fig. 6.7(a).

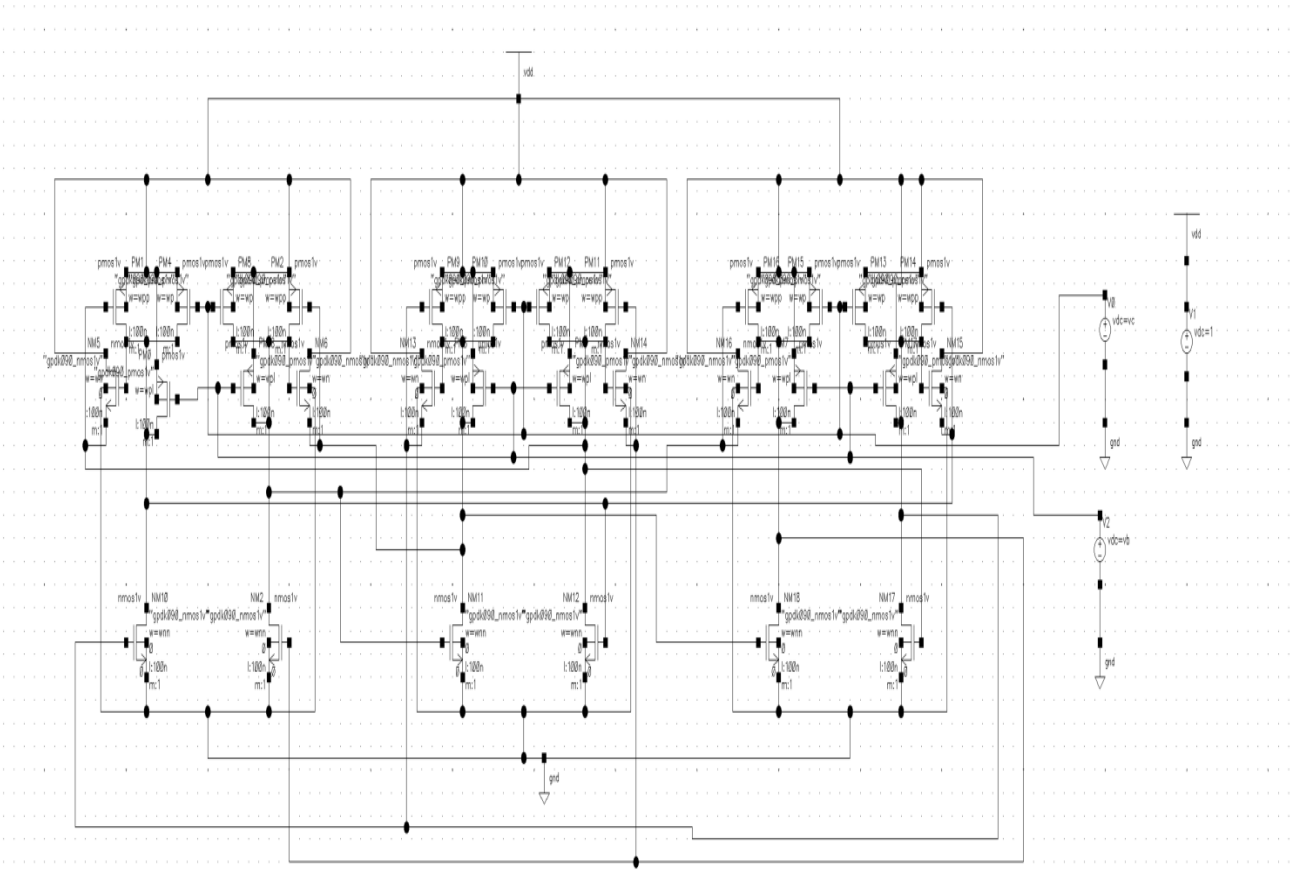


Fig. 6.7(a): Schematic of modified proposed ring VCO.

The transient response is shown in Fig. 6.7(b).

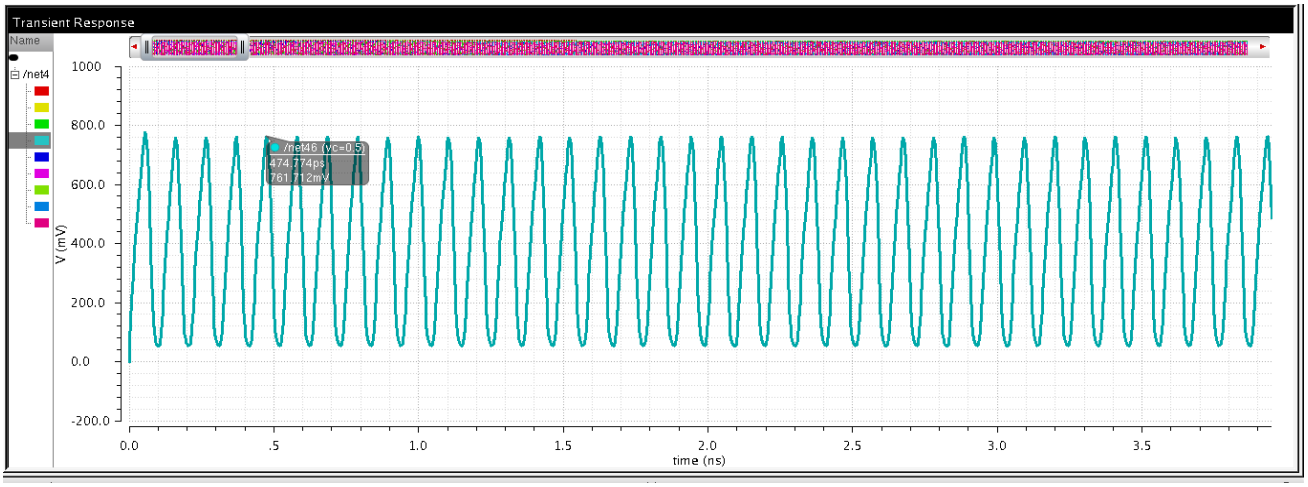


Fig. 6.7(b): Transient response.

The power response is shown in Fig. 6.7(c).

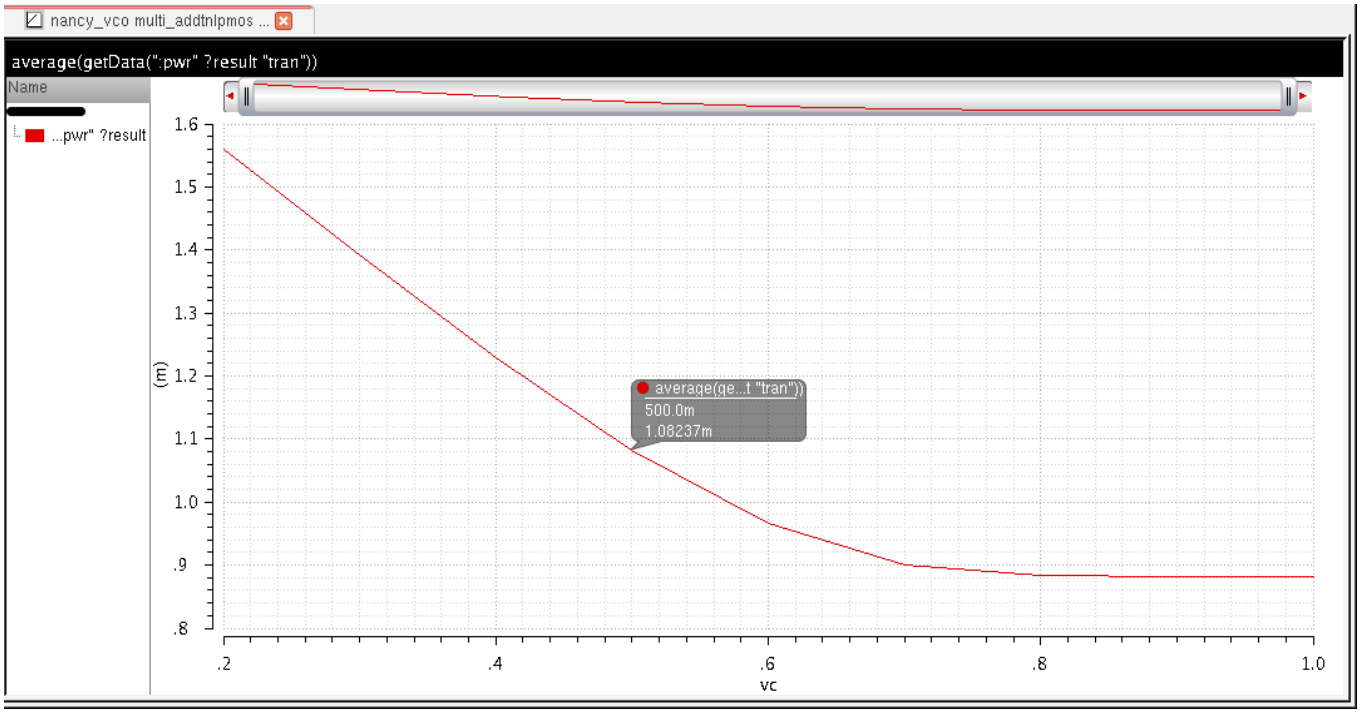


Fig. 6.7(c): Power response.

The periodic steady state response is shown in Fig. 6.7(d).

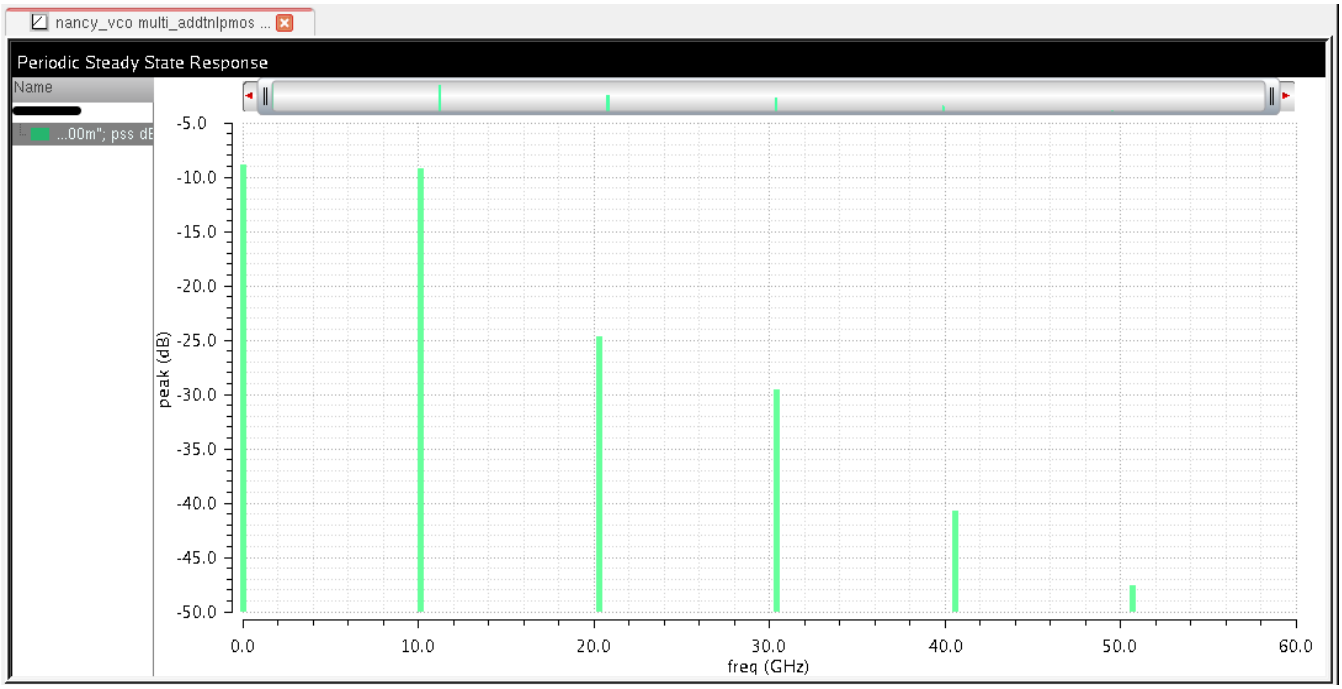


Fig. 6.7(d): Periodic steady state response.

The phase noise response is shown in Fig. 6.7(e).

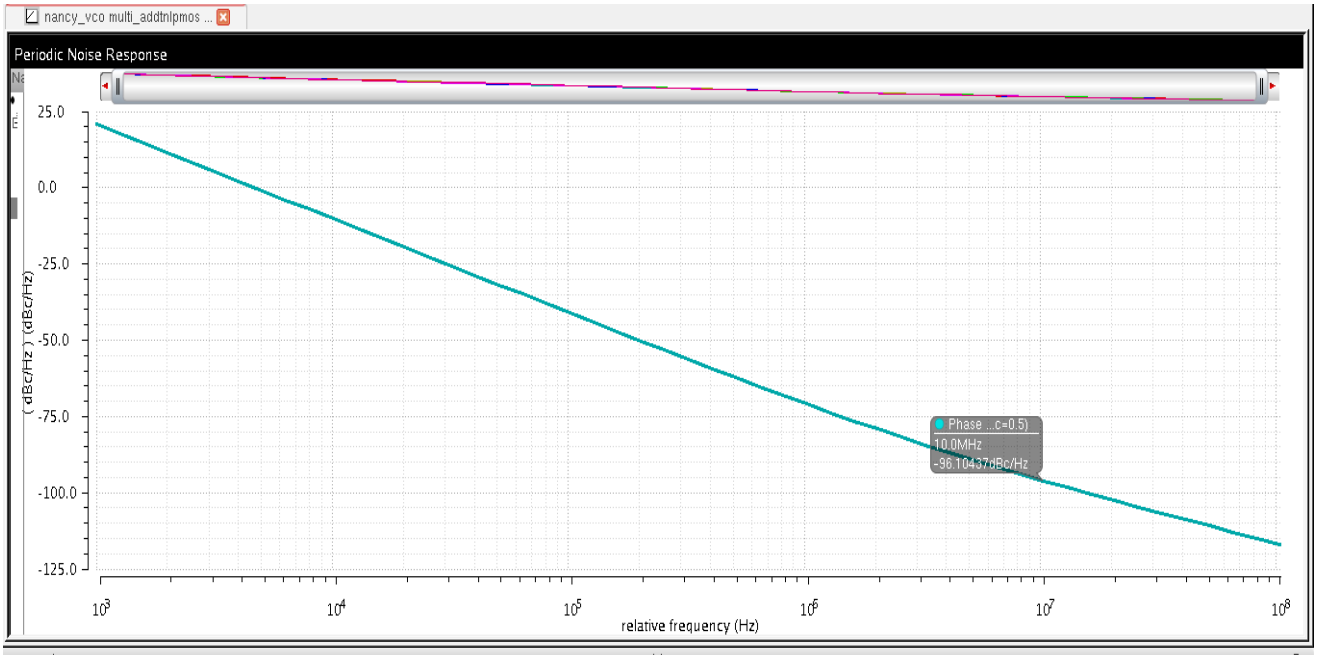


Fig. 6.7(e): Phase noise response.

The performance table of modified proposed 3-stage multi-loop CMOS ring VCO when bias voltage is 0.2V is tabulated in Table 1.9.

Table 1.9: Performance of modified proposed 3-stage multi-loop CMOS ring VCO (Vbias =0.2).

Control Voltage (V)	Frequency (GHz)	Power (mW)	Phase Noise (dBc/Hz) @ 10MHz offset
0.2	12.889	1.56	
0.3	11.70	1.39	
0.4	10.58	1.22	
0.5	9.546	1.082	-96.18
0.6	8.67	0.966	
0.7	8.102	0.900	
0.8	7.925	0.884	
0.9	7.91	0.882	
1	7.906	0.882	

When Vbias is increases from 0.2 to 0.5V, the phase noise improves but the power consumption also increases as shown in Fig. 6.7 (f).

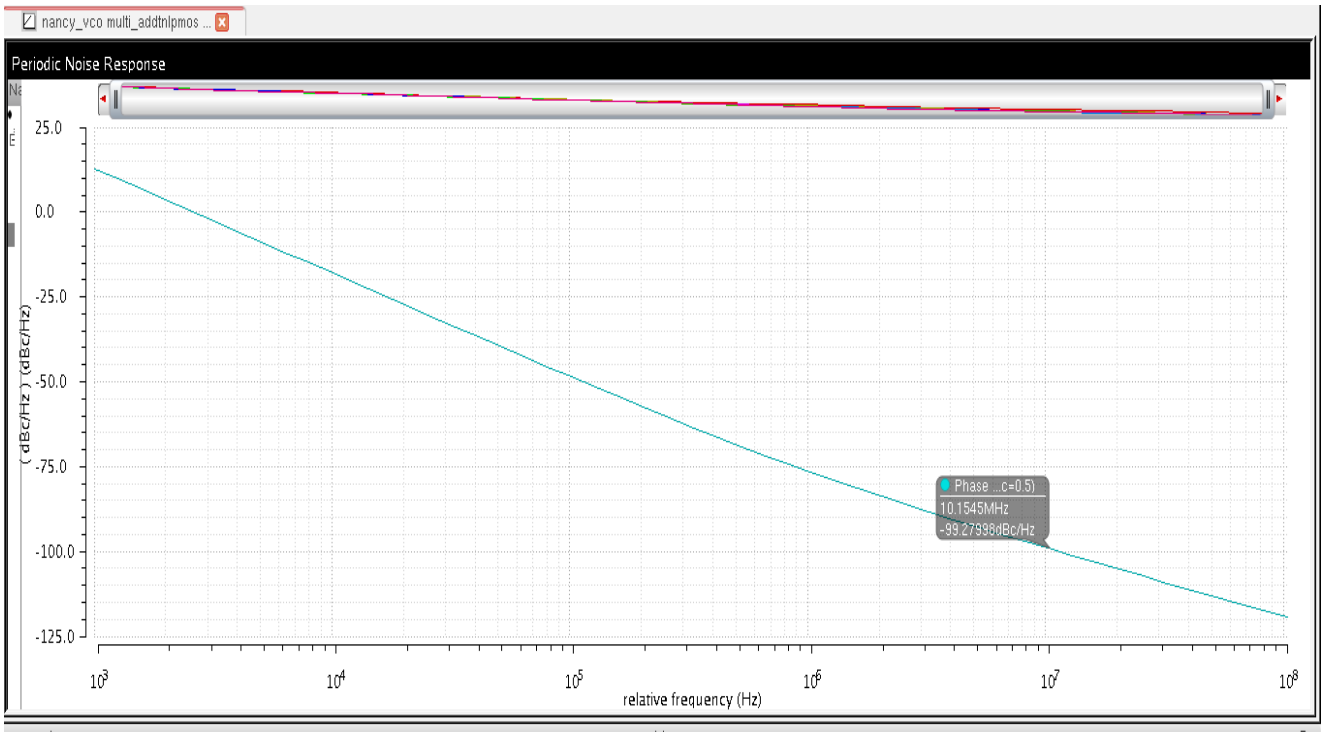


Fig. 6.7(f): Phase noise response at Vbias=0.5V.

The power response is shown in Fig. 6.7(g).

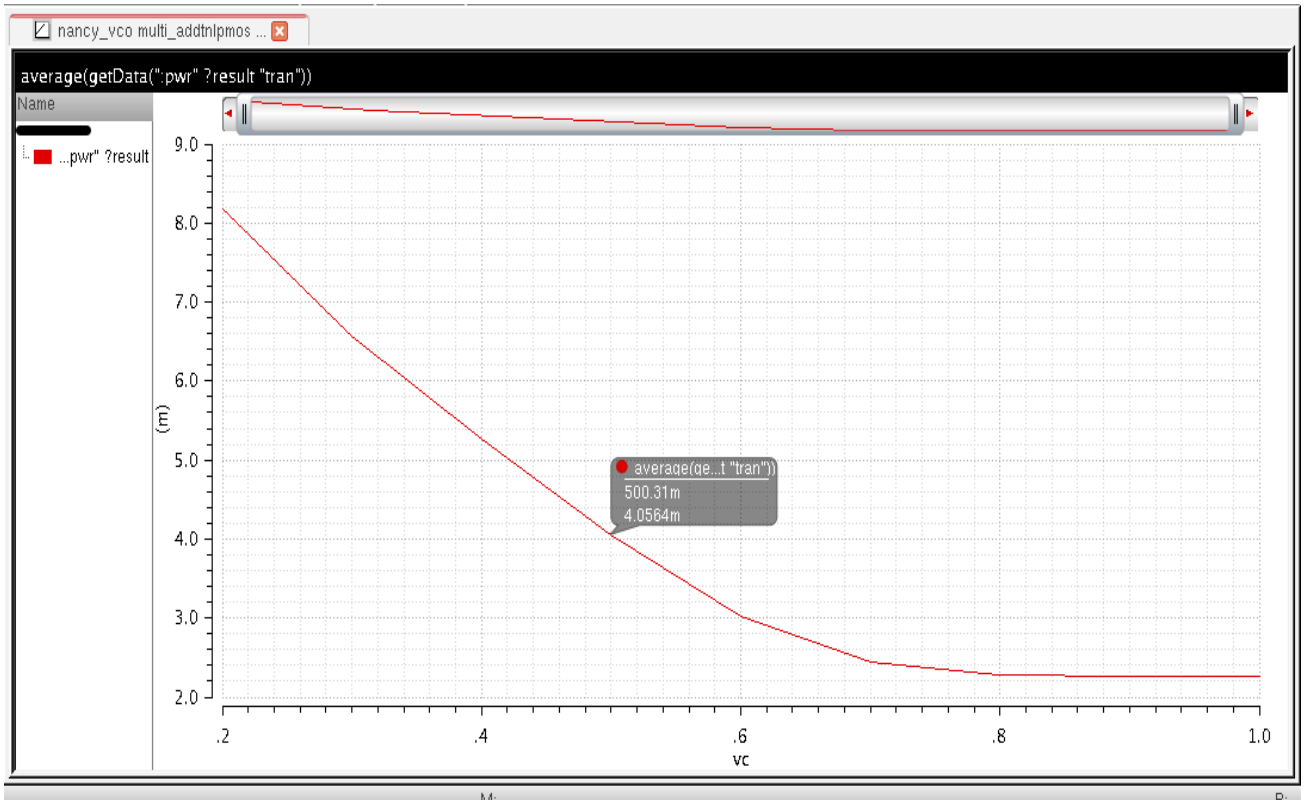


Fig. 6.7(g): Power response.

The performance table of modified proposed 3-stage multi-loop CMOS ring VCO when Vbias is 0.5V is tabulated in Table 1.10.

Table 1.10: Performance of modified proposed 3-stage multi-loop CMOS ring VCO (Vbias=0.5V).

Control Voltage (V)	Frequency (GHz)	Power (mW)	Phase Noise (dBc/Hz) @ 10MHz offset
0.2	19.20		
0.3	16.59		
0.4	13.59		
0.5	10.67	4.05	-99.21
0.6	9.59		
0.7	7.8		
0.8	5.87		
0.9	5.82		
1	5.82		

6.2 Summary of Ring VCO

A. 3-stage CMOS inverter ring oscillator

The frequency ,power and phase noise graph of ring oscillator with respect to varying Vdd is shown in Fig. 6.8.

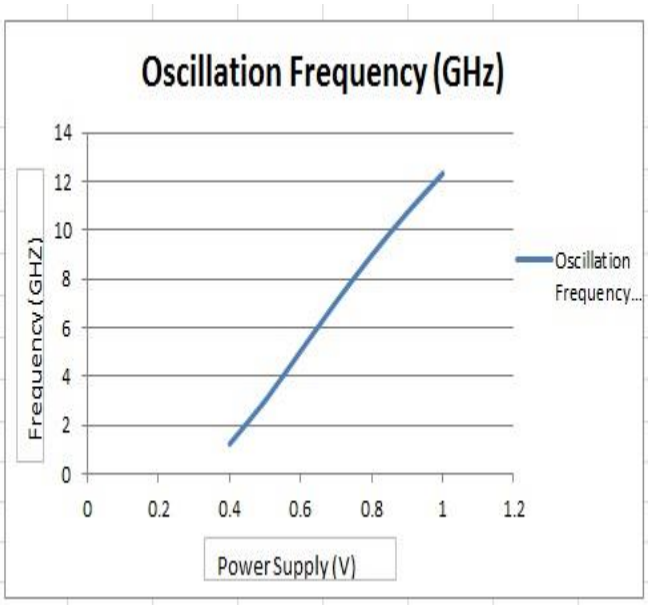


Fig. 6.8 (a) Frequency vs Supply

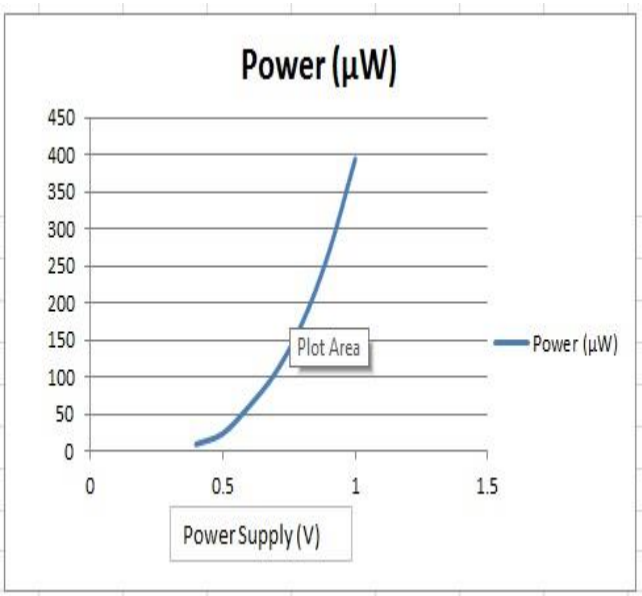


Fig. 6.8 (b) Power vs Supply

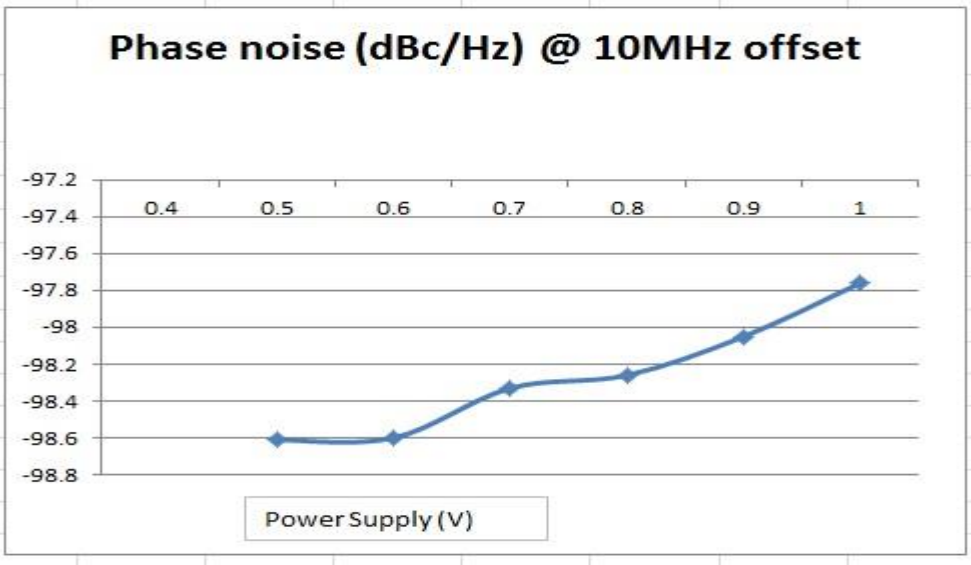


Fig. 6.8 (c) Phase noise vs Supply.

As it can be seen from graph that as the power supply increases, the frequency and power increaeses but the phase noise decreaeses.

B. 3-stage CMOS VCO with varying PMOS load

The frequency graph of ring oscillator with respect to varying control volatge is shown in Fig. 6.9.

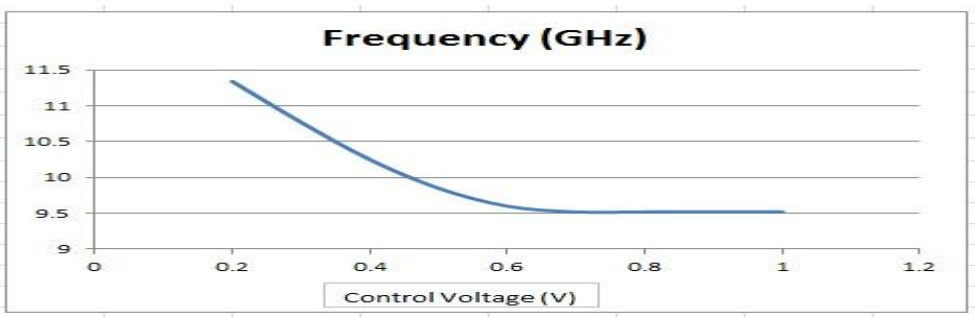


Fig. 6.9: Frequency vs Control voltage.

As the control voltage increases, the operating frequency decreases.

C. 3-stage CMOS VCO with inductive load

The frequency graph of ring oscillator with respect to varying control voltage is shown in Fig. 6.10.

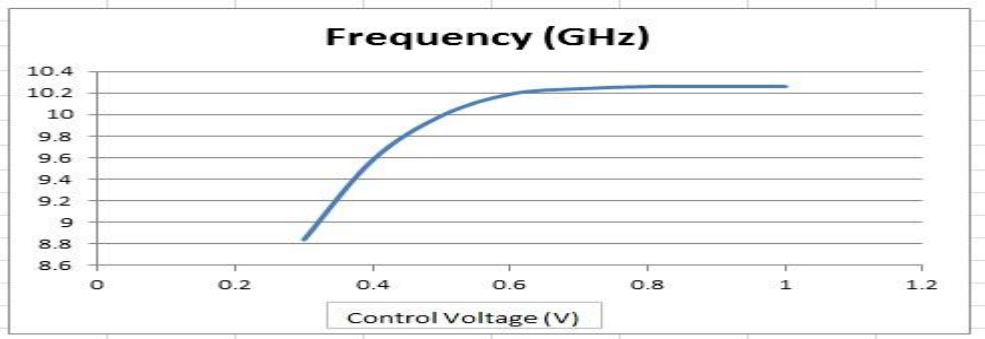


Fig. 6.10: Frequency vs Control voltage.

D. 3-stage Differential multi-loop VCO with inductive load

The frequency graph of ring oscillator with respect to varying control voltage is shown in Fig. 6.11.

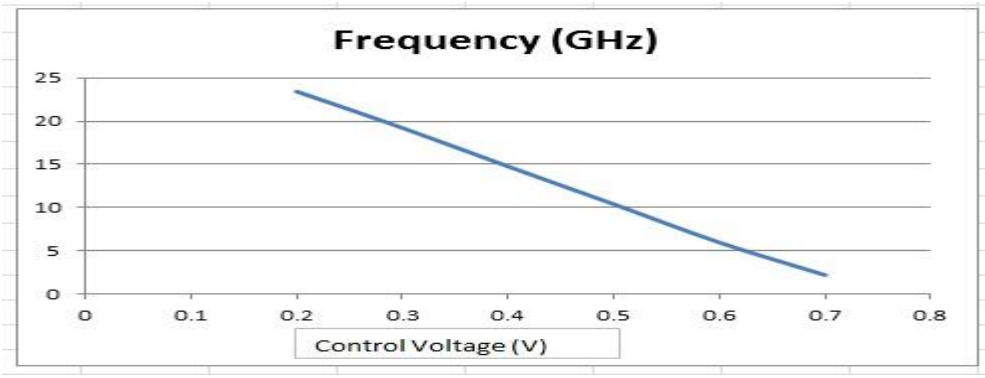


Fig. 6.11: Frequency vs Control voltage.

E. 3-stage Proposed Differential multi-loop VCO with inductive load with additional PMOS load

The frequency ,power and phase noise graph of ring oscillator with respect to varying control voltage is shown in Fig. 6.12.

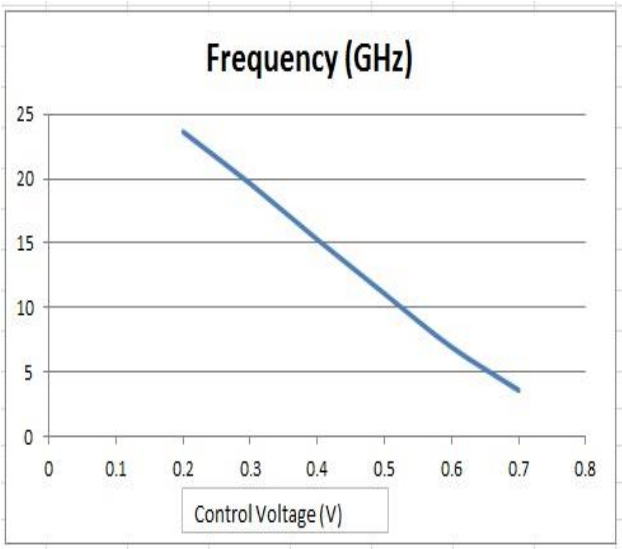


Fig. 6.12 (a): Frequency vs Control volatge

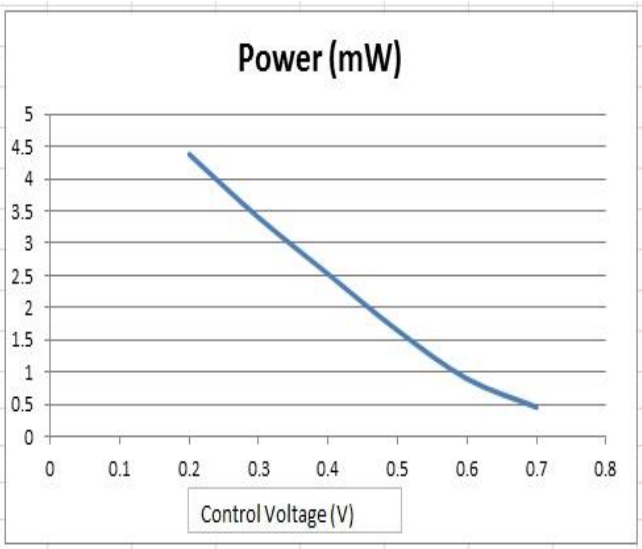


Fig. 6.12 (b): Power vs Control voltage.

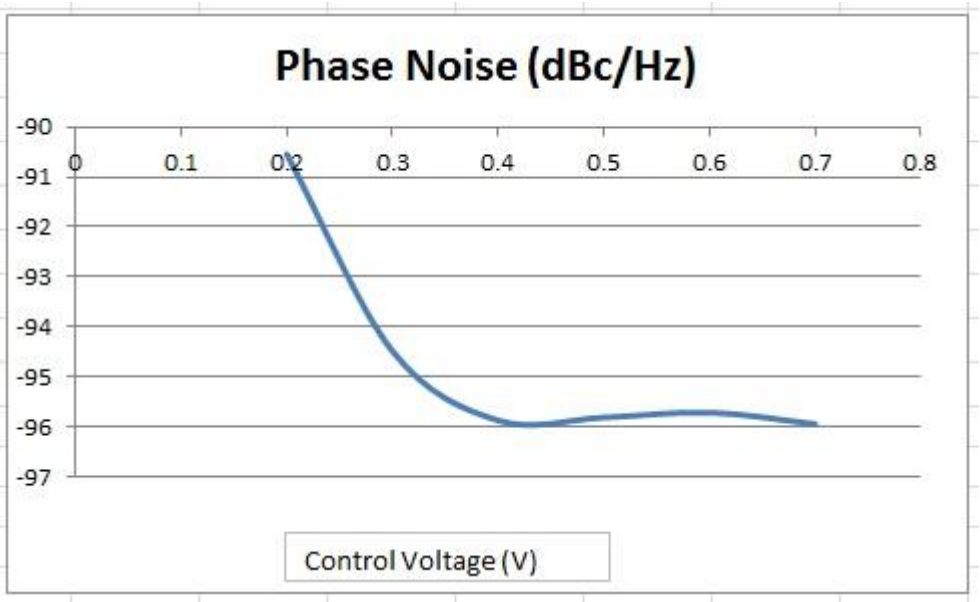


Fig. 6.12 (c): Phase noise vs control voltage.

As it can be seen from graph that as the control volatge increases, the frequency and power decreases but the phase noise increases.

F. **3-stage Proposed Differential multi-loop VCO with inductive load with additional PMOS load(Wp=500n)**

The frequency ,power and phase noise graph of ring oscillator with respect to varying control voltage is shown in Fig. 6.13.

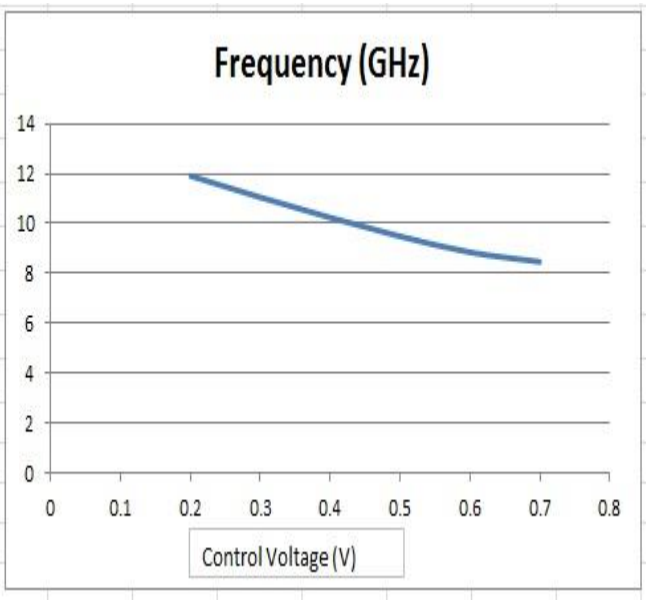


Fig. 6.13 (a): Frequency vs Control volatge

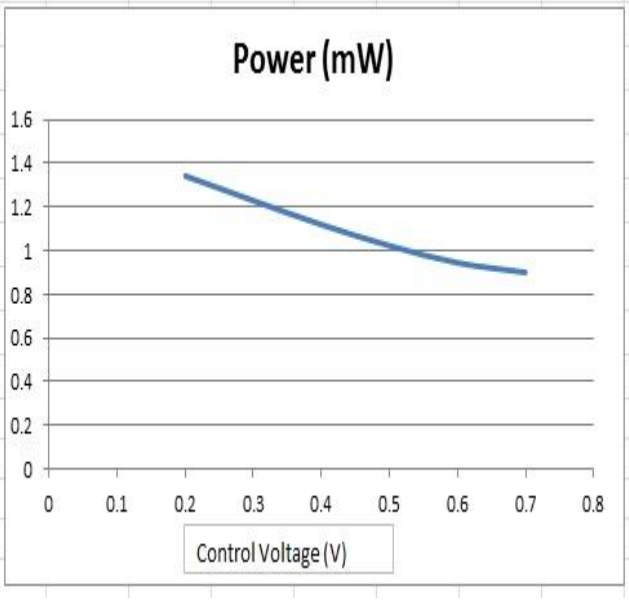


Fig. 6.13 (b): Power vs Control voltage.

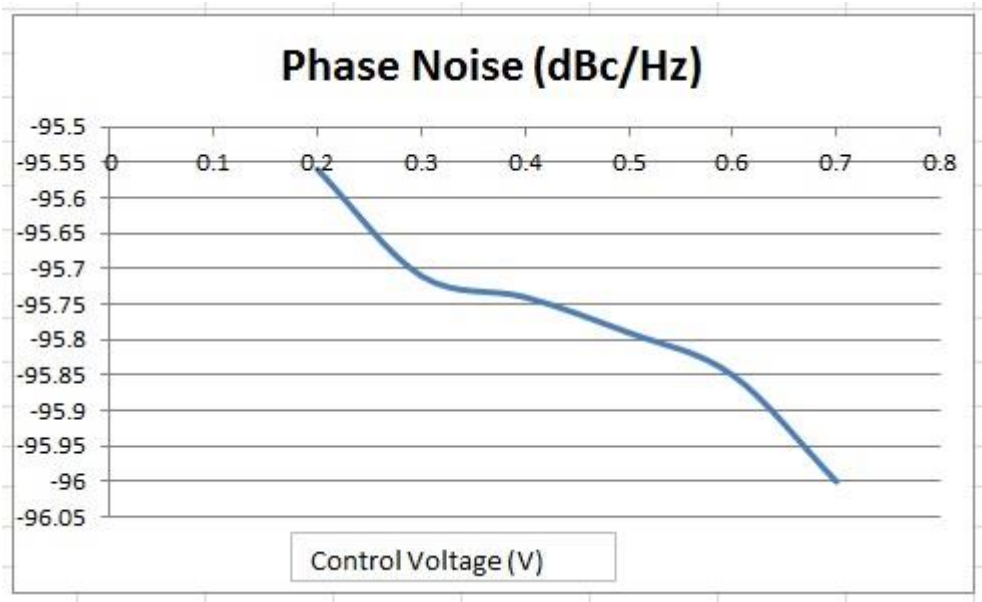


Fig. 6.13 (c): Phase noise vs control voltage.

As it can be seen from graph that as the control volatge increases, the frequency and power decreases but the phase noise increases. The X-band frequency range is achieved.

G. 3-stage Modified-Proposed Differential multi-loop VCO with inductive load with additional varying PMOS load (Vbias=0.2)

The frequency and power graph of ring oscillator with respect to varyingcontrol voltage is shown in Fig. 6.14.

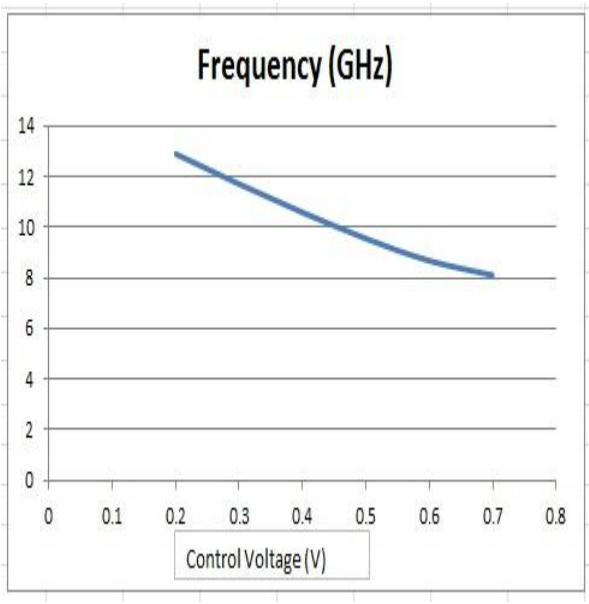


Fig. 6.14 (a): Frequency vs Control volatge

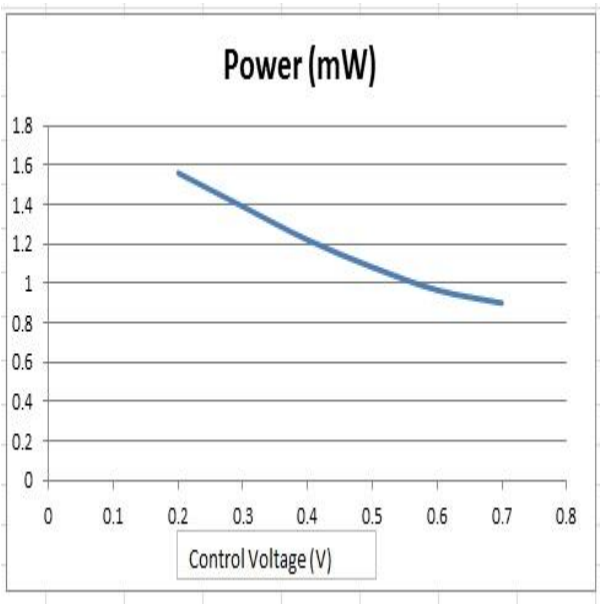


Fig. 6.14 (b): Power vs Control voltage.

As it can be seen from graph that as the control volatge increases, the frequency and power decreases but the phase noise improves with respect to previous ones.

H. 3-stage Modified-Proposed Differential multi-loop VCO with inductive load with additional varying PMOS load (Vbias=0.5)

The frequency graph of ring VCOr with respect to varying control voltage is shown in Fig. 6.15.

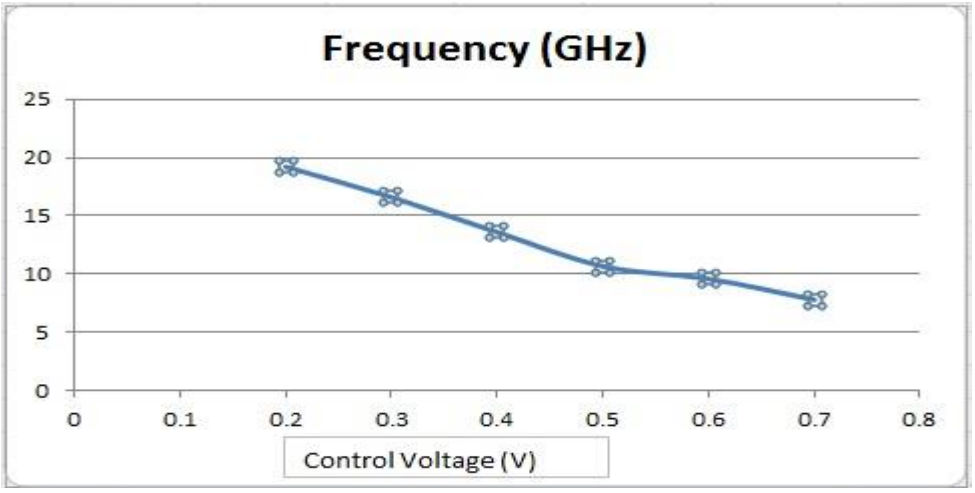


Fig. 6.15: Frequency vs Control volatge

The tuning range performance comparison of multi-lopp VCO with inductive load, proposed VCO and modified-proposed VCO is shown in Fig. 6.16.

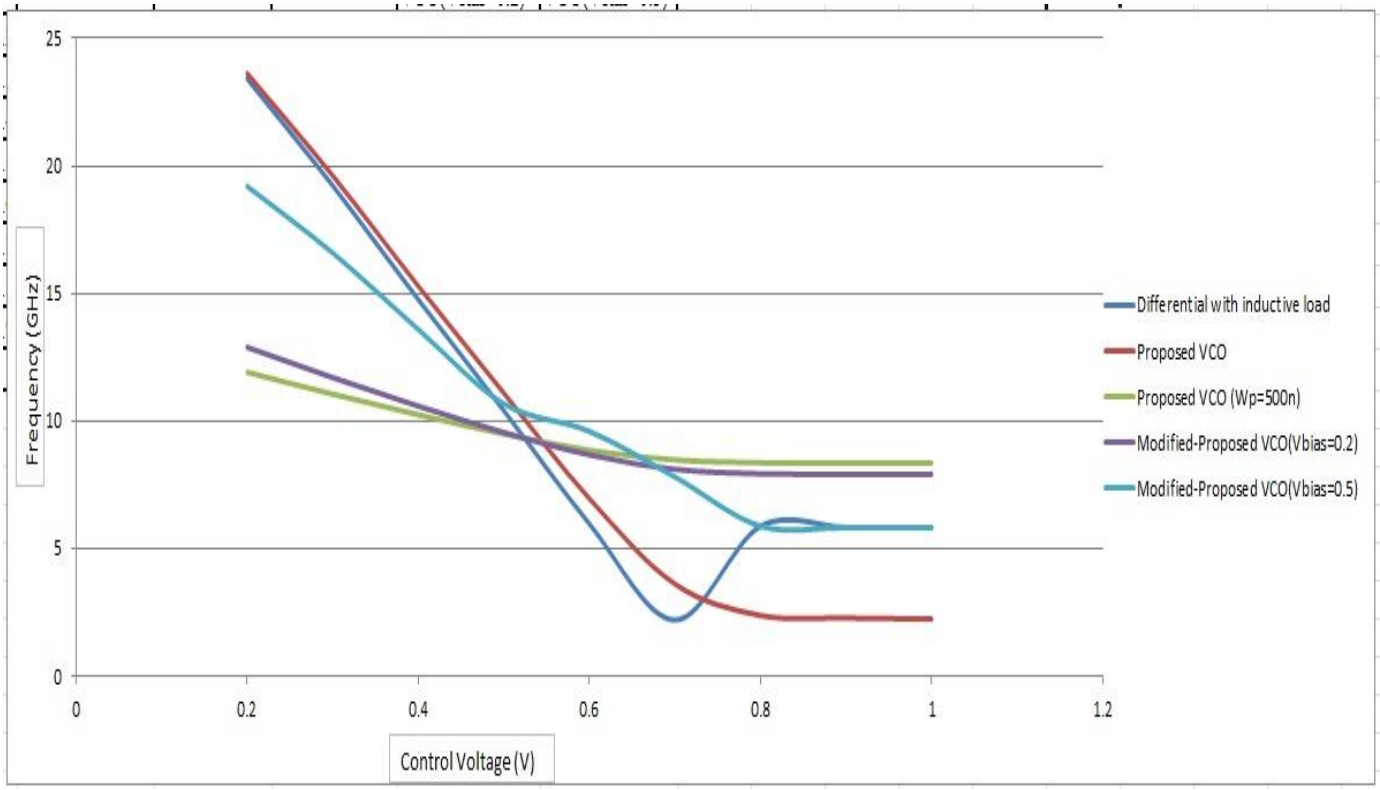


Fig. 6.16: Frequency range performance comparison of CMOS VCOs.

The power dissipation performance comparison of multi-lopp VCO with inductive load, proposed VCO and modified-proposed VCO is shown in Fig. 6.16.

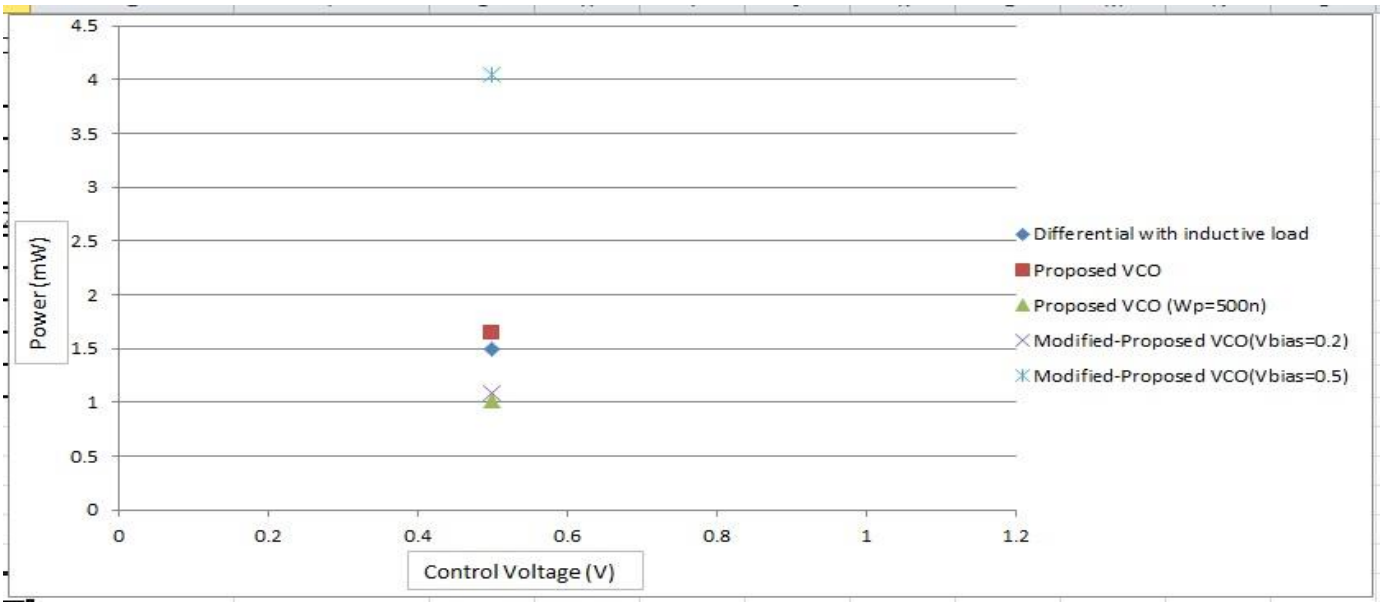


Fig. 6.17: Power dissipation performance comparison of CMOS VCOs.

The phase noise performance comparison of multi-lopp VCO with inductive load, proposed VCO and modified-proposed VCO is shown in Fig. 6.18.

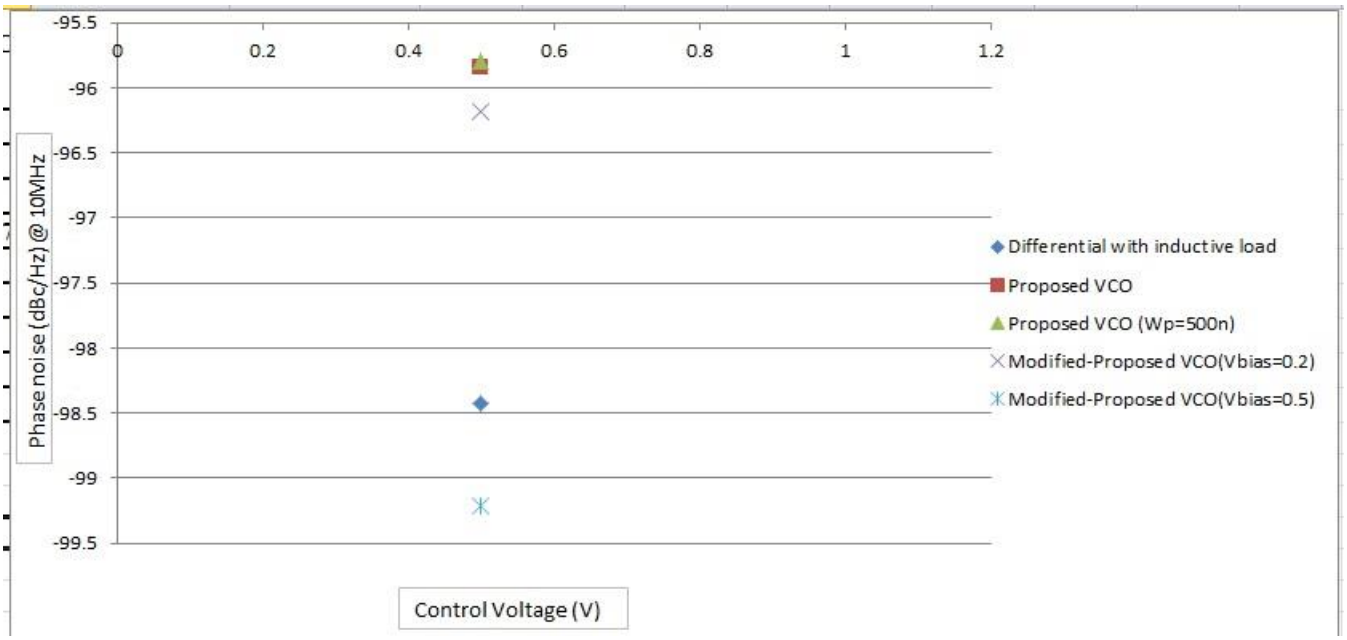


Fig. 6.18: Power dissipation performance comparison of CMOS VCOs.

The performance comparison of CMOS VCO with inductive load, proposed VCO and modified-proposed VCO is tabulated in Table 1.11.

Table 1.11: Performance comparison of CMOS VCOs

Specifications	Single-ended VCO with varying PMOS load	Single-ended VCO with inductive load	Differential-ended multi-loop VCO with inductive load	Proposed Differential-ended multi-loop VCO with aditional PMOS load (Wp_{load}=5µ,Wp_{add}=120n)	Proposed Differential-ended multi-loop VCO with aditional PMOS load (Wp_{load}=Wp_{add}=500n)	Modified-proposed VCO with additional varying PMOS load (Vbias-0.2)	Modified-proposed VCO with additional varying PMOS load (Vbias-0.2)
Frequency of Oscillation (GHz)	9.85	9.989	10.4	11.09	9.49	9.54	10.67
Power(mW)	0.04	0.677	1.5	1.64	1.022	1.082	4.05
Phase noise (dBc/Hz) @ 10MHz offset	-87.68	-97.43	-98.43	-95.81	-95.79	-96.18	-99.21

The center frequency performance of CMOS VCOs is shown in Fig. 6.19.

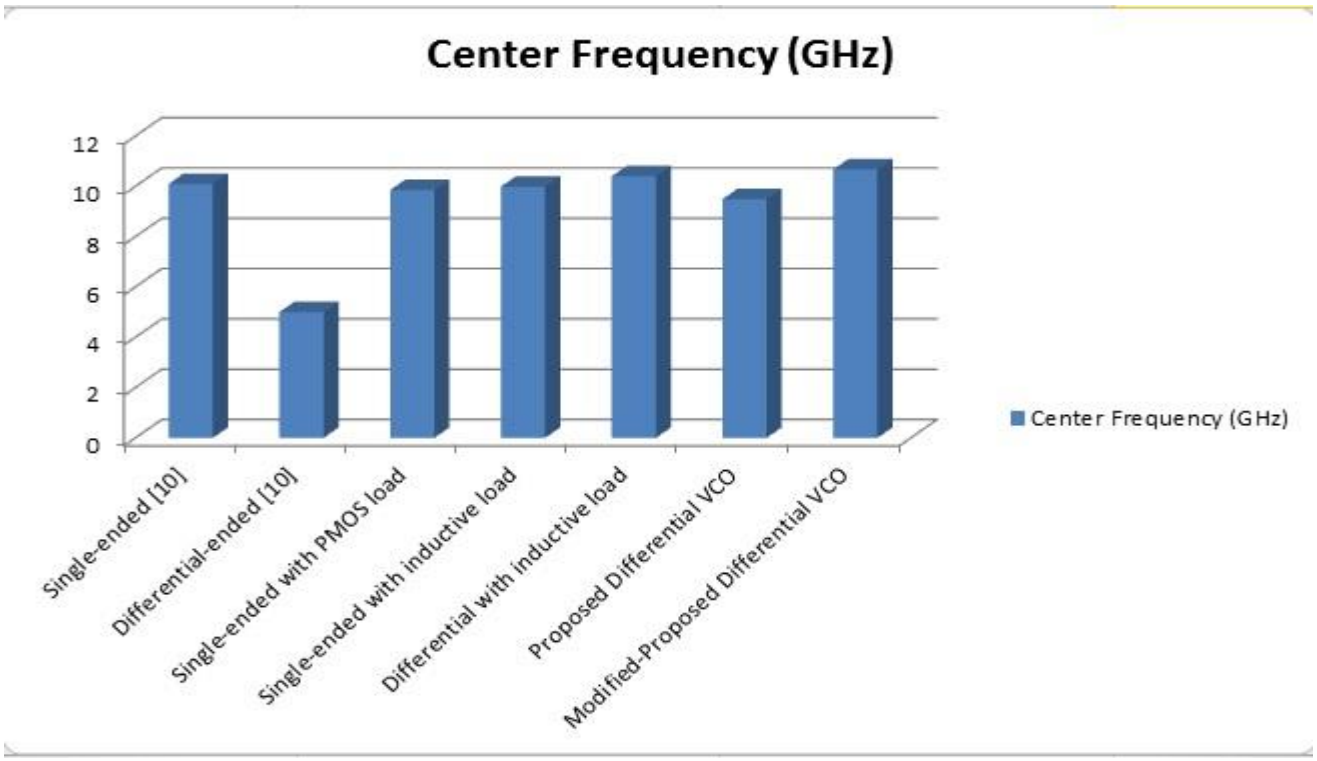


Fig. 6.19: Oscillation Frequency Performance.

The power consumption performance of CMOS VCOs is shown in Fig. 6.20.

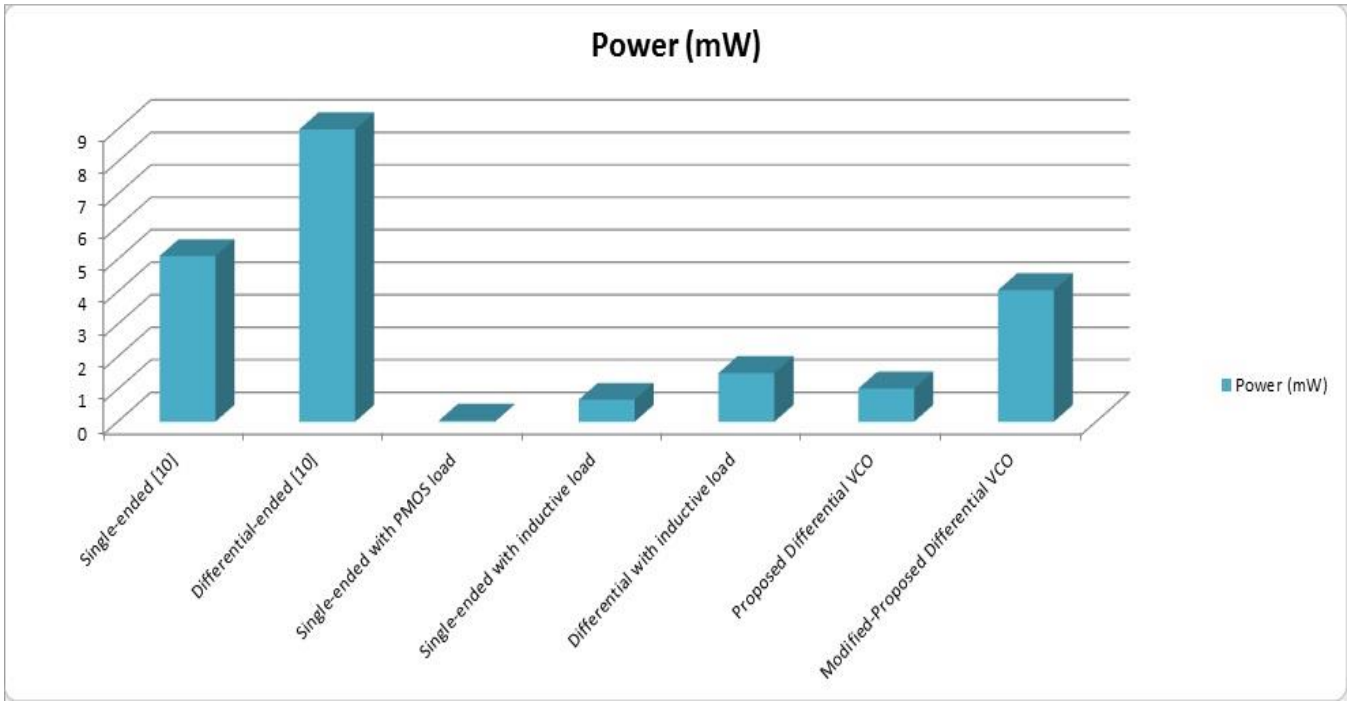


Fig. 6.20: Power consumption Performance.

The phase noise performance of CMOS VCOs is shown in Fig. 6.21.

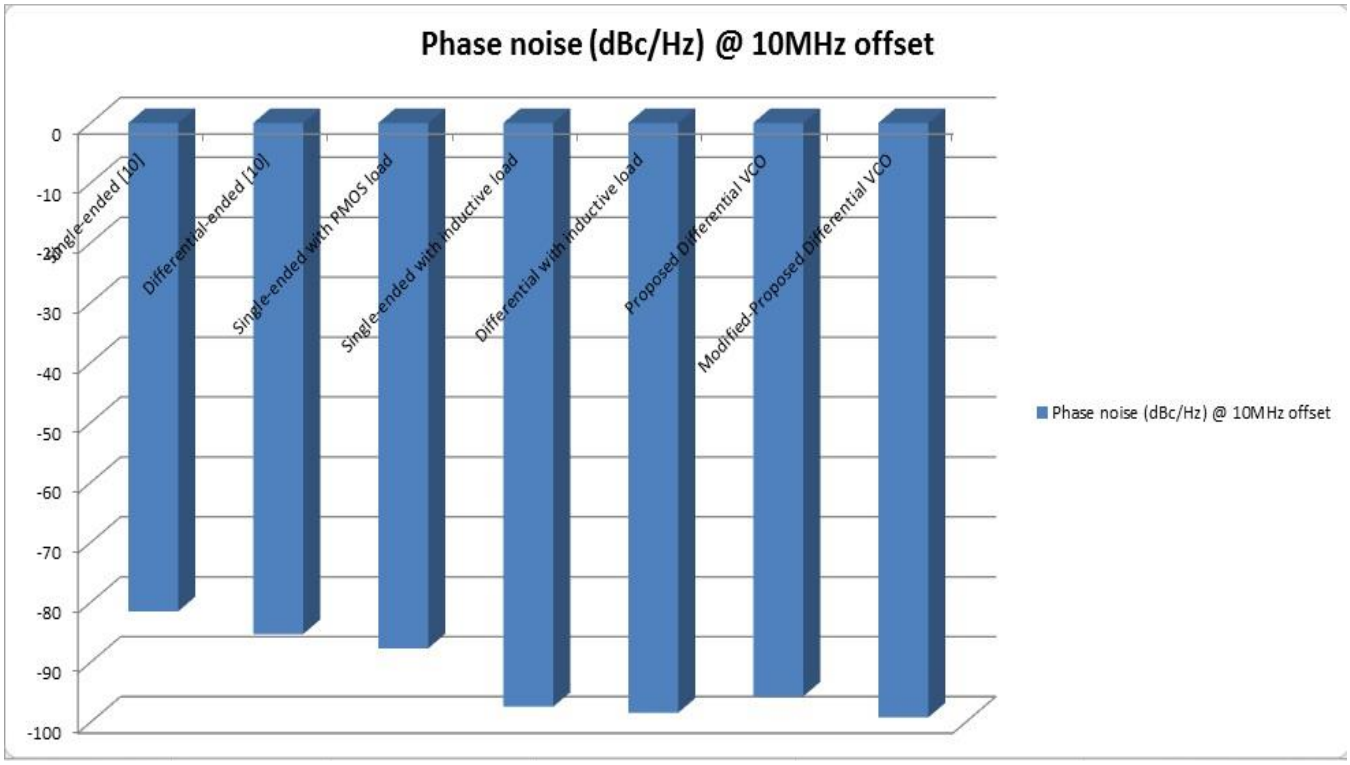


Fig. 6.21: Phase noise Performance.

The performance comparison of single-ended CMOS VCOs is shown in Fig. 6.22.

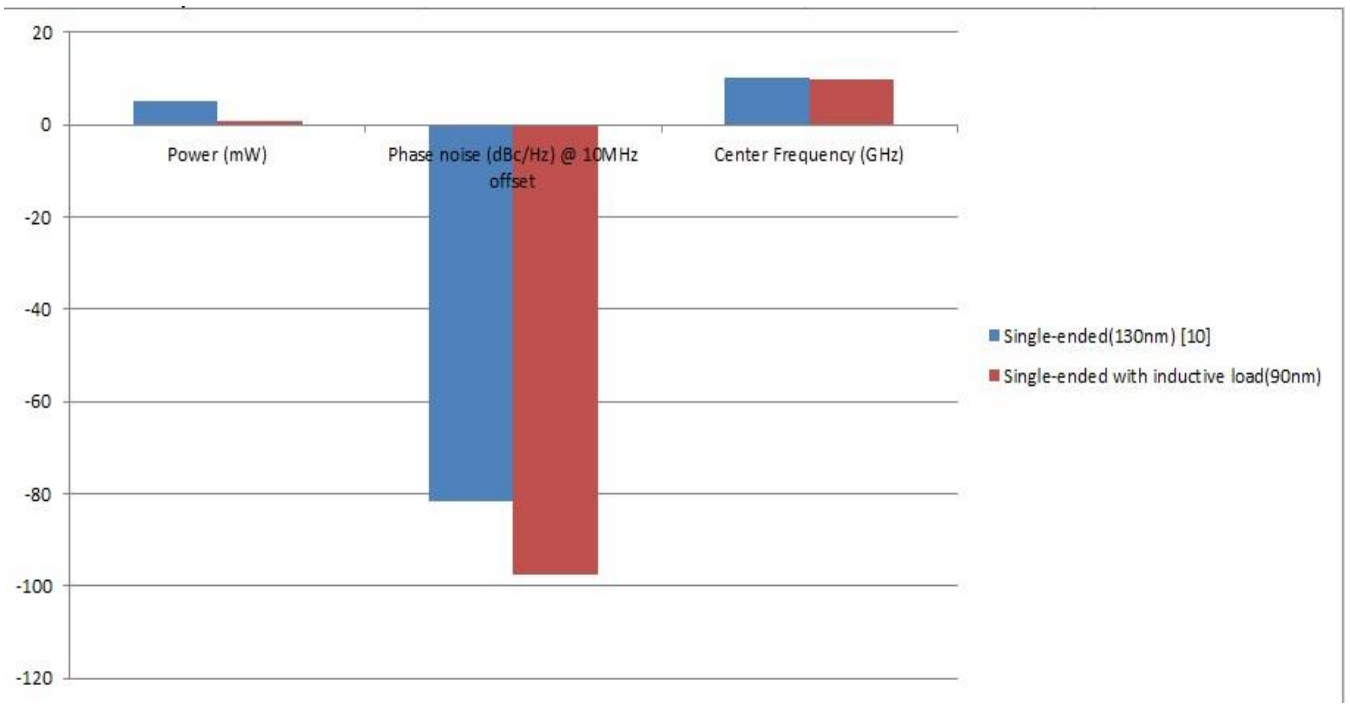


Fig. 6.22: Performance Comparison of Single-ended CMOS VCOs

The performance comparison of differential base CMOS VCO in 130nm and 90nm is shown in Fig. 6.23.

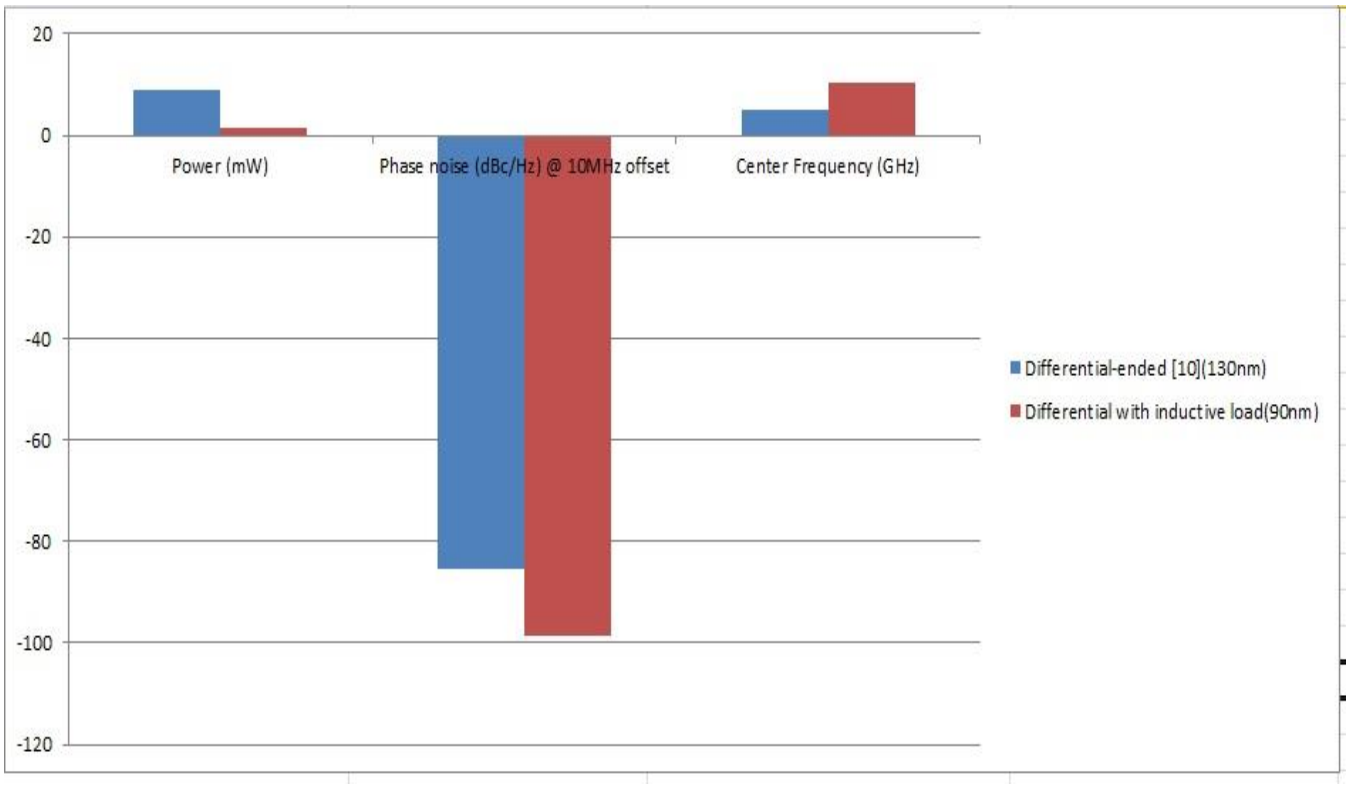


Fig. 6.23: Performance comparison of differential base CMOS VCO in 130nm and 90nm.

The performance comparison of differential CMOS VCOs is shown in Fig. 6.24.

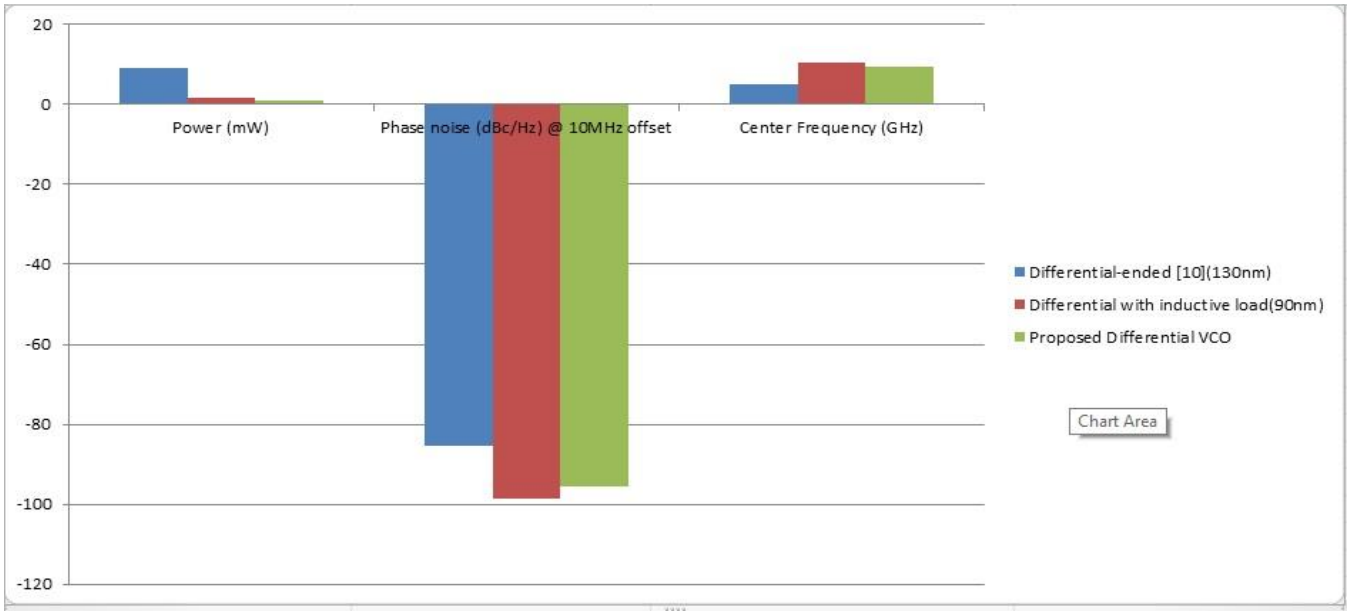


Fig. 6.24: Performance comparison of differential base CMOS VCO in 130nm and 90nm and proposed VCO in 90nm.

The performance comparison of differential proposed and modified CMOS VCOs is shown in Fig. 6.25.

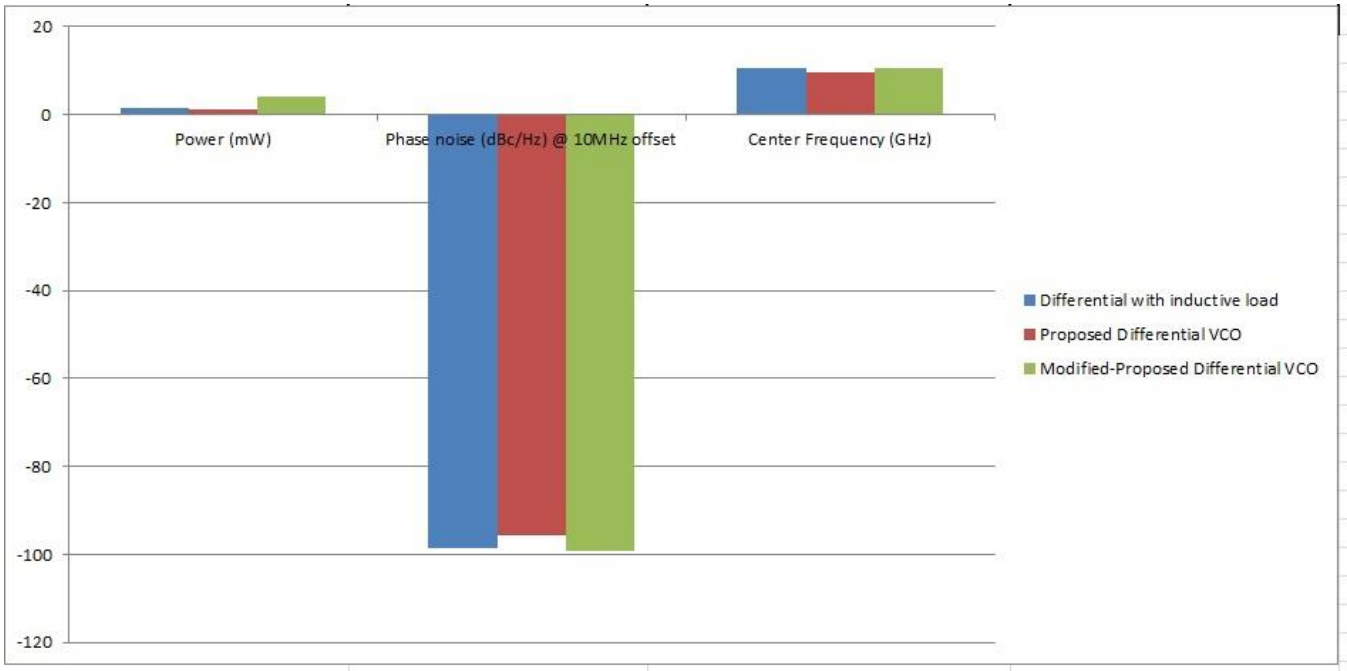


Fig. 6.25: Performance comparison of differential proposed and modified CMOS VCO in 90nm.

The performance comparison of differential CMOS VCOs is shown in Fig. 6.26.

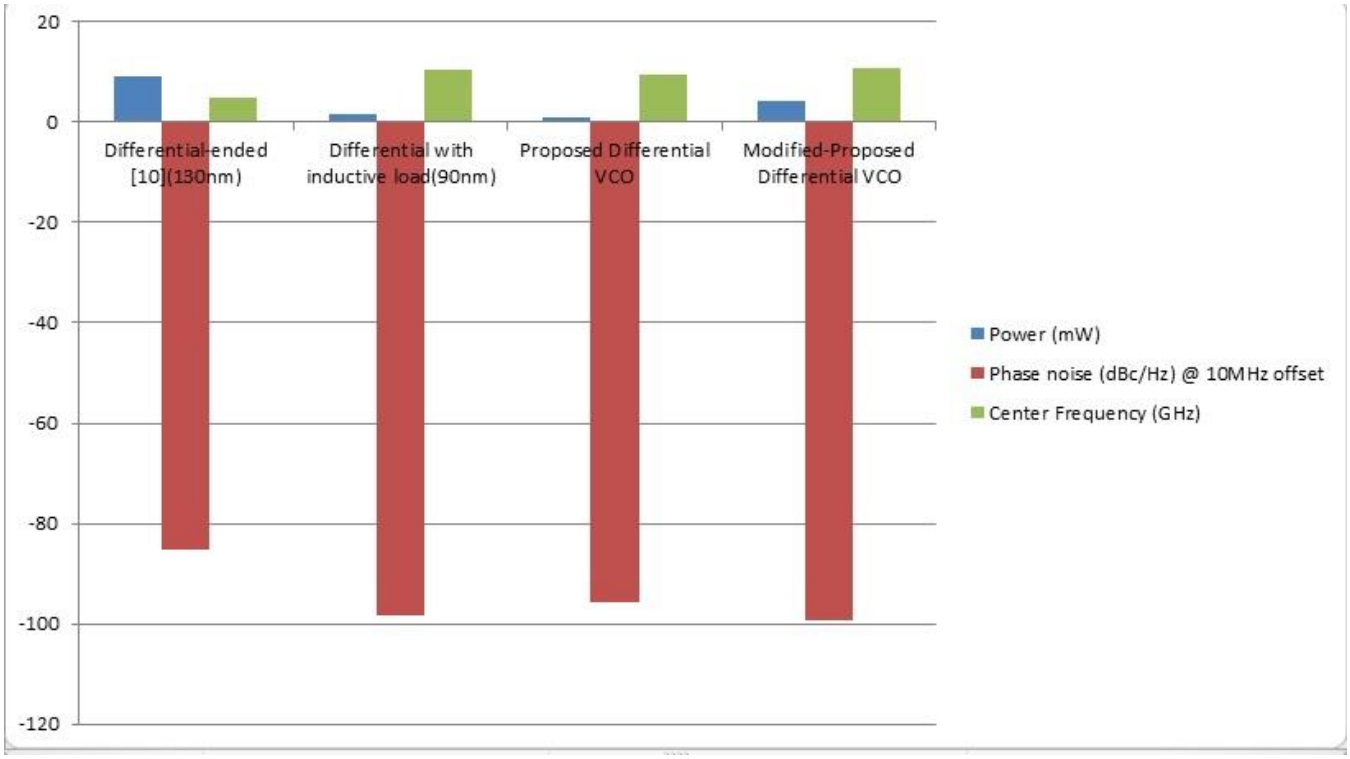


Fig. 6.26: Performance comparison of differential CMOS VCO in 90nm.

The performance comparison of CMOS VCOs is shown in Fig. 6.27.

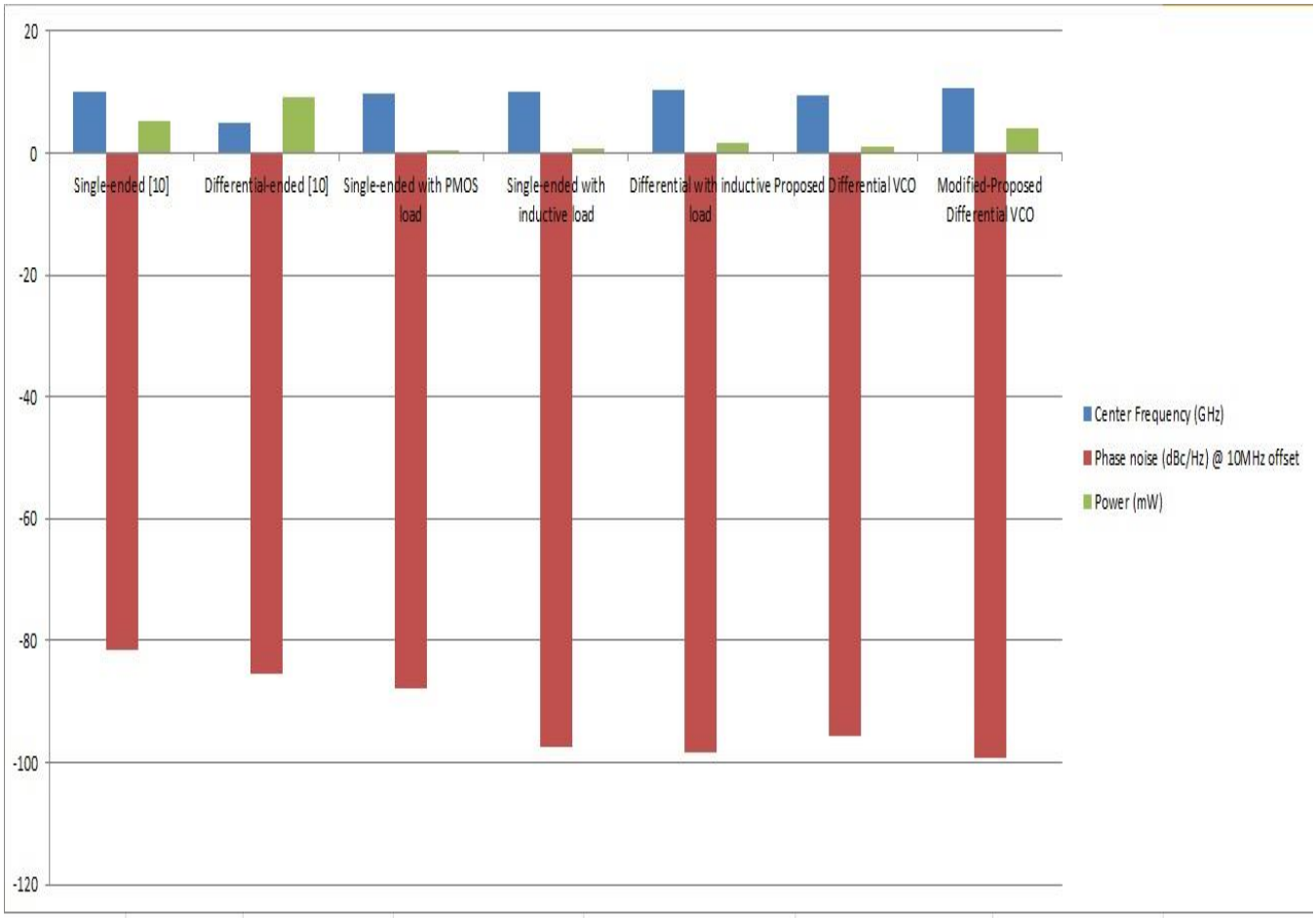


Fig. 6.27: Performance comparison of CMOS VCO in 90nm.

CHAPTER 7
CONCLUSIONS

This report presented a study of high-frequency low-noise CMOS voltage controlled oscillators. A feed-forward type differential architecture: multiple pass loop architecture along with inductive load delay stage has been found with promising characteristics to increase the maximum frequency and to reduce the output phase noise of ring oscillator. The presented results, in conclusion, suggest that it may become possible to extend the applications of cost effective ring VCOs into some areas that previously required the performance of LC oscillators. The attractive features of this approach are the simplicity of the design and the facts that the ring oscillators can be implemented in any CMOS process. This VCO can be used in military application for ATC, vehicle speed detection for target identification. It can also be used in motion detectors (10.5GHz) for traffic light crossing detectors and also in deep space telecommunications. Further, it can also be designed in 65nm and 45nm CMOS technology.

Some practical applications of the ring design are listed below:

- Phase-locked loops
    - Clock generation for CPUs, DSP chips and DRAM.
    - Frequency Synthesizers.
    - Clock/Data recovery network.
- Stand-alone applications
    - Direct frequency synthesizers
    - Clock generation
    - System synchronization applications such as zero-delay-clock buffers.
    - Oversampling A/D converters.

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