DESIGN AND STUDY OF GRAPHENE FIELD EFFECT TRANSISTORS

A Dissertation submitted

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to

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ABSTRACT

Silicon is the most widely used semiconductor material that meets the current needs of the electronic industry. To go in coordination with Moore's law, devices are miniaturized and are expected to give better performance. But silicon devices has its own limitations when they are scaled down in terms of dimensions that leads to degradation of device performance. Due to this industry has reached closed to the point of end of silicon era. Researchers in the field of academics and industry are indulged in finding the alternatives of silicon based field effect transistors.

Graphene, a 2D nanomaterial is being studied widely to be employed as channel material. Its potentials are proved with its extraordinary physical, dimensional, thermal and optical properties. In recent times, many studies have been done on the graphene field effect transistror and much advancement have been achieved in this field. This research work is based on the study of graphene field effect transistors (GFET). As optimization is the need of every new research, this work is an effort to achieve graphene field effect transistor optimization. Changing the dimensional and other material properties of the device the variations in the I-V characteristics are observed. Finally, a device with optimized parameters are suggested that gives better performance characteristics. These parameters can be help for the graphene FET designers while fabrication.

CERTIFICATE

This is to certify that Jasleen Kaur bearing registration number 1100095 has completed the thesis titled "Design and Study of Graphene Field Effect Transistor" under my guidance and supervision. To the best of my knowledge, the present work is the result of her original investigation and study. No part of the thesis has ever been submitted for any other degree at any other university. this thesis is fit for submission and the partial fulfillment of the conditions for the award of Masters of Technology in Electronics and Communications.

Dr. Anita Kumari

ACKNOWLEDGEMENT

Every Day I remind myself that my inner and outer life depends on the labor of other men"- Albert Einstein

Acknowledgement is not a mere obligation but an epitome of humility and indebtness to all those who have helped in the compilation of this pre dissertation work and without whom my work would have been nothing.

First of all, I am thankful TO GOD "THE ALMIGHTY" for helping me succeed in the venture.

I specially want to thank to my guide, mrs Anita kumari, Associate Professor, Department of Electronics and Communication, Lovely Professional University, Jalandhar who took personal interest in my research work and also lend me a very helping hand in understanding the very basics of nanoelectronics field. I also wish to express my sincere thanks to all the colleagues at Lovely Professional University Jalandhar, who were of great help during the course of my research period.

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DECLARATION

I, Jasleen Kaur Student of M.Tech, Department of electronics and communications of lovely professional university, Punjab, Hereby declare that all the information furnished in this report is based on my own intensive research and is genuine. This thesis does not, to the best of my knowledge, contain any part od work which has been submitted for the award of any other degree either of this university or any other university without proper citation.

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PUBLICATIONS

Jasleen Kaur And Anita Kumari, “Exigency for fusion of graphene and carbon nanotube with biomaterials” , Toxicology and Environmental Chemistry, Vol 96 issue 4, 2014.

Jasleen Kaur and Anita Kumari “ Impact of source/Drain concentration on Nanoribbon field effect transistor performance” , International Journal of Numerical Modelling: Electronic Networks, Devices and Fields. (under review)

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Chapter 1

INTRODUCTION

1.1 Background and Research Motivation

Since the creation of the first transistor in 1947 at Bell labs, the electronic industry progressed tremendously that have great impact on human life today. It has sincerely obeyed the technology scaling trend predicted by one, Gordon Moore, in his famous paper [1] in 1965. Today, the best microprocessor from very known group, Intel has about 2.5 billion transistors with a technology of just 32nm. Moore's law could not be continued forever in the electronics industry. Gordon Moore, the co founder of the Intel, predicted that the number of transistors that could be placed on a chip would double every two years [2]. Since the publication of this paper various manufactures are following this law efficiently but unfortunately (as shown in figure 1.1) this law cannot sustain forever [5]. The main obstacles are in the way: the limits of the lithography techniques, the rising cost of fabrication and the size of the transistor [5].

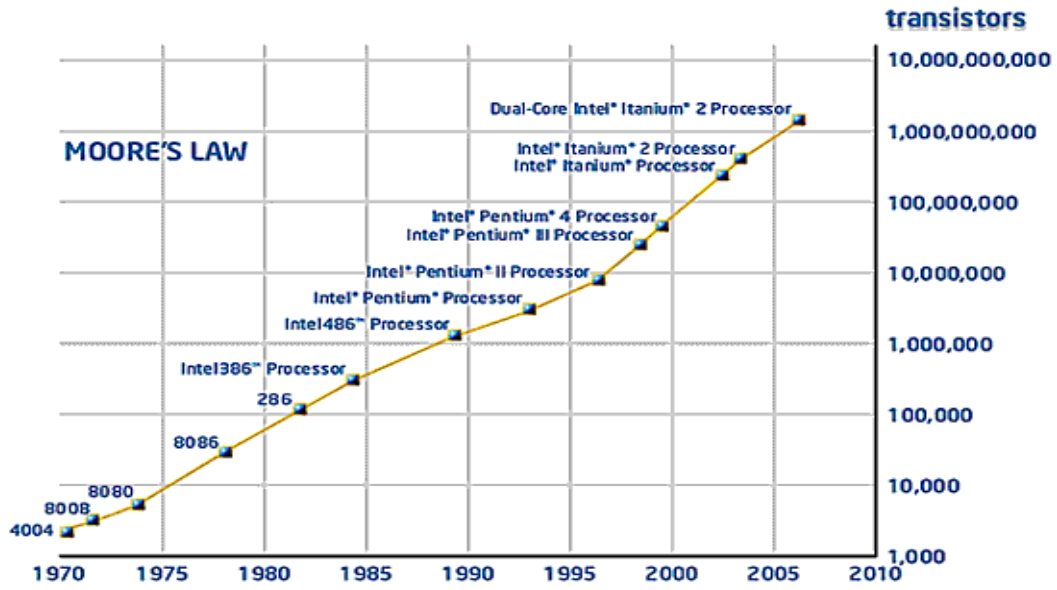

Figure 1.1: Chip manufactures following Moore law

The use of the silicon in chip manufacturing is going through the fundamental limitations including the tunneling current and the sub threshold current which lead to the high power consumption and circuit failure [4].And the cost of fabrication Si devises with increase in number of transistors is also increasing that cannot be avoided [3].So by this time there is a need of a technology that overcome these disadvantages and can sustain moores law efficiently with less power consumption, faster speed ,cheaper manufacturing and readily available this technology is none other than nanoelectronics [3].

1.2 Nanoelectronics

Nanoelectronics is basically the application of the nanotechnology on an electronic device having size less than 100 nm, so it can be said that it is the science which deals with the electronic components manufactured and engineered at a molecular scale [12]. Almost everything made using silicon in microelectronics can be made using nano technologies including wires , integrated circuits, FETs (field effect transistors),sensors devices ,amplifiers , oscillators [6,9,10,17]. Nanotechnology is emerging in every field whether its biomedical, biotechnology, industry and Agriculture with its incredible applications [11]. Nanostructures have a unique electronic transport such that it can have negligible resistivity due negligible scattering leads to large conductivity hence can be used in many applications [13]. Nanoelectronics is believed to overcome all those limitations faces while scaling silicon based devices or chips [14]. For the study of nanotechnology quantum mechanical effects as well as tunneling effects are significant[15]. Nanoelectronics technologies are carbon nanotubes (CNT), semiconductor nano wires, quantum automata and graphene nanoribbons[7].

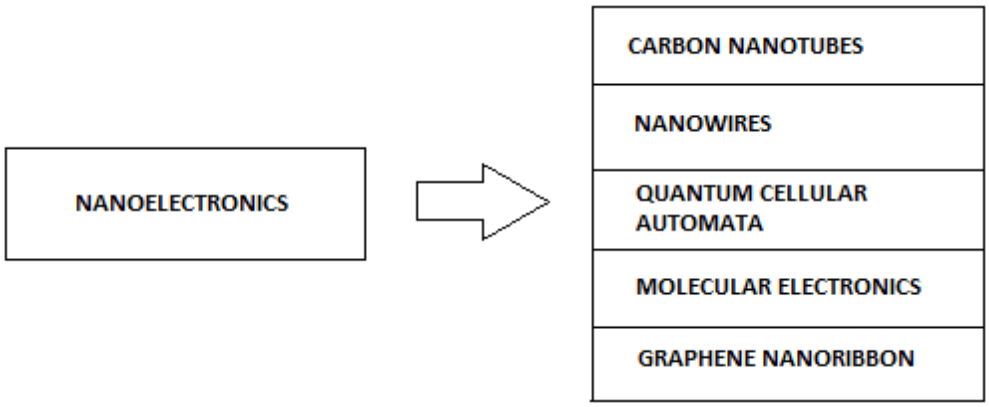

Figure 1.2: Nanoelectronic technologies

Carbon nanotubes are cylindrically rolled carbon sheets, as that has significant electronic transport properties, making them a good candidate in the nanoelectronics. Implementing carbon nanotubes in different structures can be used in many applications [16]. Since its discovery tremendous research is going on for the future replacement of silicon devices with carbon nanotubes and the researchers are somehow successful in finding out large number of applications that uses carbon nanotubes. During fabrication the dimensional parameters for CNTs are not under control so manufacturers limits their implementation in present day devices [7].Semiconducting nano wires that seems to be similar to CNTs but actually not is a good candidate for interconnects ,pn junction devices as well as transistor devices[7]. Quantum cellular automata (QCA) is a computational model made up of quantum dots.[19].Position of electrons helps quantum dot in deciding the logic either 1 or 0.When low voltage area is surrounded by a higher voltage area QCA traps the electrons [18]. Lithography techniques are used along with aluminum to create quantum dot. Quantum cellular automata are used in logical devices [7]. Molecular devices are the naturally made nano structures that can be made in large with same structural dimensions and properties [19]. Molecular devices are used to work as switches, wire and quantum effect based electronic devices [20]. Graphene is a wonder material that can have fascinating applications that is because of it exhibits unusual properties [22]. Initially it was believed that graphene will not be stable in its free form but in 2004 it was isolated by researchers at university of Manchester.Graphene is a 2 dimensional material made up of carbon atoms that form a honeycomb lattice structure [23] . Graphene is the thinnest

material and the strongest of all [23]. It can conduct electricity more efficiently than copper and is also known as the best conductor of heat [24]. Graphene is transparent and still strongly impermeable[8]. 2004 heralded a new dawn of study of 2dimensional material and of graphene in particular.[7]. The intermolecular, weak π-π interactions are of utmost importance for understanding the various properties of graphene sheets [27]. The single-layered honeycomb structure of graphene makes it the "mother" of all carbon-based systems the graphite we find in our pencils is simply a stack of graphene layers [20]. Carbon nano tubes are made of rolled-up sheets of graphene; and buckminsterfullerene molecules, or "buckyballs", are nanometer size spheres of wrapped-up graphene. Decreasing the width of graphene layers form graphene nano ribbon (GNR) that can be used in vast number of applications [21].

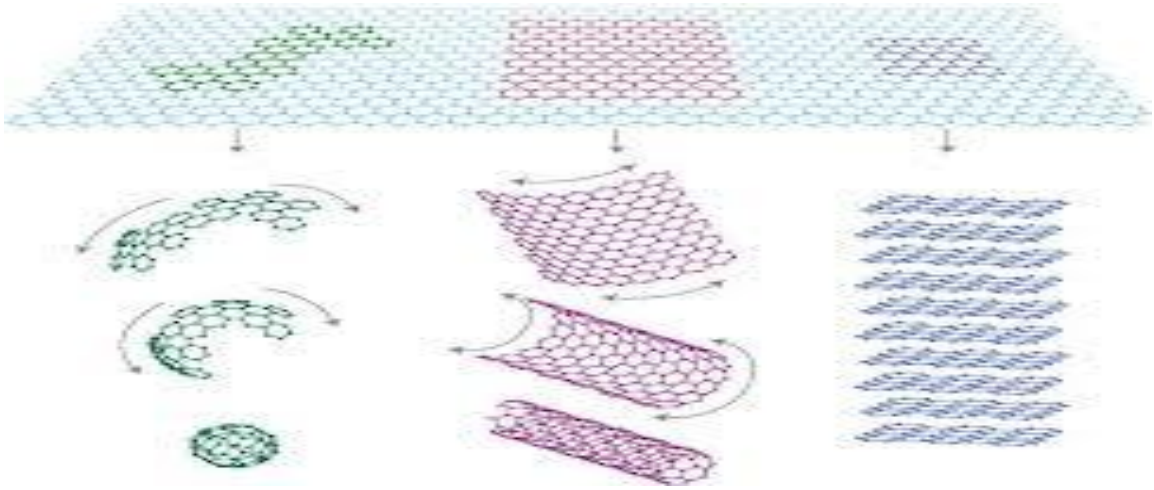

Figure 1.3 carbon nanostructures fullerenes, carbon nanotubes, graphene nano ribbon

1.3 Graphene Nanoribbon

A. Introduction

Basically graphene is a material made up of carbon atoms arranged in 2d honeycomb lattice as shown in figure 1.4 and can be utilized to make the various other carbon based materials, namely carbon Bucky-ball structure, carbon nanotubes, graphene nano-ribbons and the graphite [30]. The honeycomb structure can be thought of as a triangular lattice with a basis of two atoms per unit cell. These Dirac points are of great importance in the electronic transport of graphene.

Theoretically the graphene has been studied for the sixty years and widely used for describing the properties of various carbon based materials [30]. Forty years later it was found that graphene can be used to produce excellent 2d nanostructures. In graphene the carrier mobility from 3000-15000 cm2/Vs can be achieved even under ambient conditions, which makes it an important material for use in nanoelectronics [33]. It clearly reveals the ambipolar electric field effect such that the carriers can be continuously tuned between the electrons and the holes in a very high concentration [30]. Also it was further known that the carrier transport in graphene takes place in π-orbitals perpendicular to the surface [34]. So in the structure this translates into a mean free path for carriers of L = 400 nm at the room temperature [33]. Hence it makes the ballistic transport possible even at the scaled down device compared to the CMOS technology at present. An added advantage in graphene is that the electronic transport follows the Dirac equation and the charge carriers are relativistic in nature [37]. Also the carriers have shown to be having zero effective mass and travel at the speed of light which makes the use of graphene into the devices more favorable as they will work at higher speed [37]. In order to increase the carrier velocity and maximum drain current in MOSFETs while minimizing leakage currents and power dissipation for technology scaled to 16 nm and beyond GNR is used. [37]

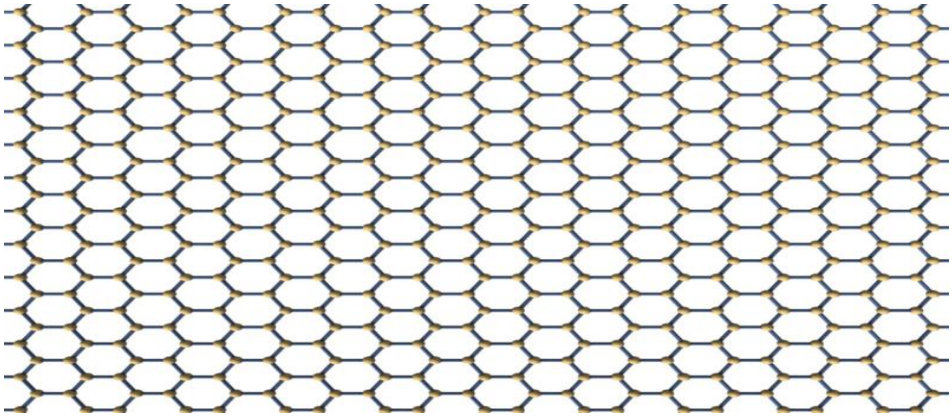

Figure 1.4: Graphene sheet

The most important aspect of graphene energy dispersion is its linear energy-momentum relationship with the conduction and valence bands intersecting at q = 0, with no energy gap [33].Graphene is a zero band-gap semiconductor with linear rather than quadratic long wavelength energy dispersion for both electrons (holes) in the conduction (valence) bands. Thus, in spite of having high carrier mobility and significant current characteristics the graphene could not be used in digital applications because the conduction in graphene could not be switched off

due to the absence of band gap. In the mean time some research workers were able to propose a bilayer graphene complementary field effect transistor [51]. This showed high on/off ratio making an important step towards graphene based logic devices [51]. One of the ways to open the band gap is patterning the graphene sheets into narrow ribbon [52]. Band gap is inversely dependent on the width of the graphene nanoribbon [52]. So by tuning the width of the graphene nanoribbon we can get the desired energy band gap. Other way of creating band gap is using a multilayered graphene.

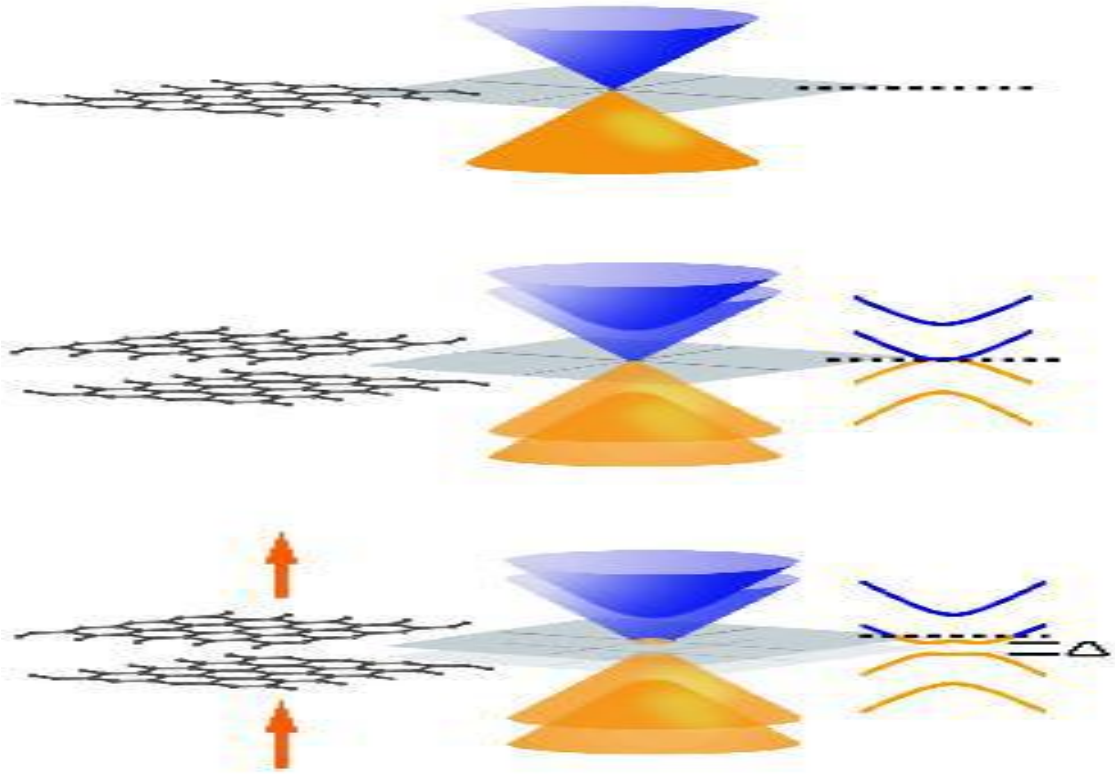

Figure 1.5 shows the variation of the energy band gap in the graphene in which the Top most figure shows the single layered graphene sheet and the lower figures showing addition of the layer and the orientation factor.

B. Types of Graphene Nanoribbon

Depending on the termination style, normally, non chiral GNR can be divided into two types: Armchair and Zigzag graphene nanoribbon. For armchair GNRs when N=3M-1 where M is an integer the GNRs will be metallic, otherwise they are semiconducting, and the energy band gap decreases as N increases. Unlike armchair GNRs, zigzag GNRs are all metallic; this is mainly because additional energy states appear on their edges [33]. Figure 1.6 shows the different types of the graphene nanoribbons, from the left armchair shaped graphene nanoribbon has been shown, further zigzag nanoribbon is shown and the last figure shows the various orientation graphene nanoribbons or chiral graphene nanoribbons having properties based on the chirality of the graphene.

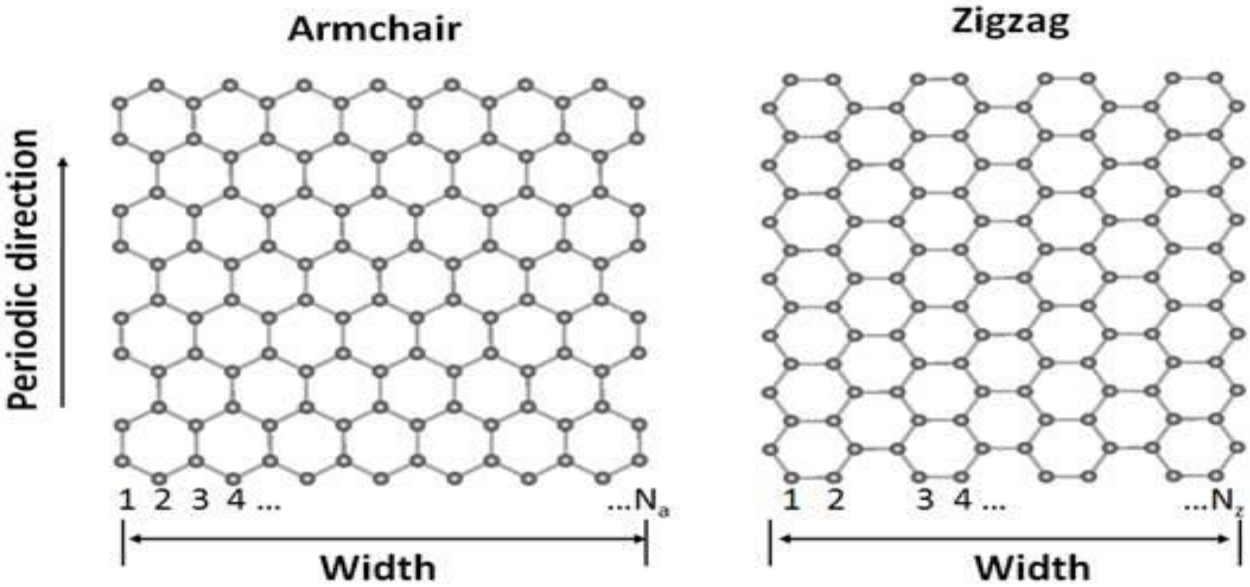

Figure 1.6 armchair and zigzag graphene

C. Various Properties of Graphene Nanoribbon

There are various properties of GNR that may be discussed, like magnetic properties, optical properties, strain properties, electronic properties, conductivity properties, thermal properties and many more physical and chemical properties which are the basic fundamentals for any material. But here in our dissertation we will keep ourselves restricted to the utilization of electronic-

transport properties under different thermal conditions which are vital for the thesis work being done

Electronic Properties of Arm Chair GNR

The electronic structures of arm chair GNR have been carefully investigated by DFT calculations [53]. Their results show that all armchair GNRs are semiconductors with energy gaps, which decrease as a function of increasing ribbon widths. No magnetism has been found in armchair GNRs. As seen from Figure 1.7 the energy gaps as a function of ribbon width are well separated into three different kinds: Na = 3p, 3p+1, 3p+2 (p is integer). Moreover, the gap size hierarchy is well separated. Na = 3p+1 categories has the largest energy gap, while the Na = 3p+2 series is the smallest one.

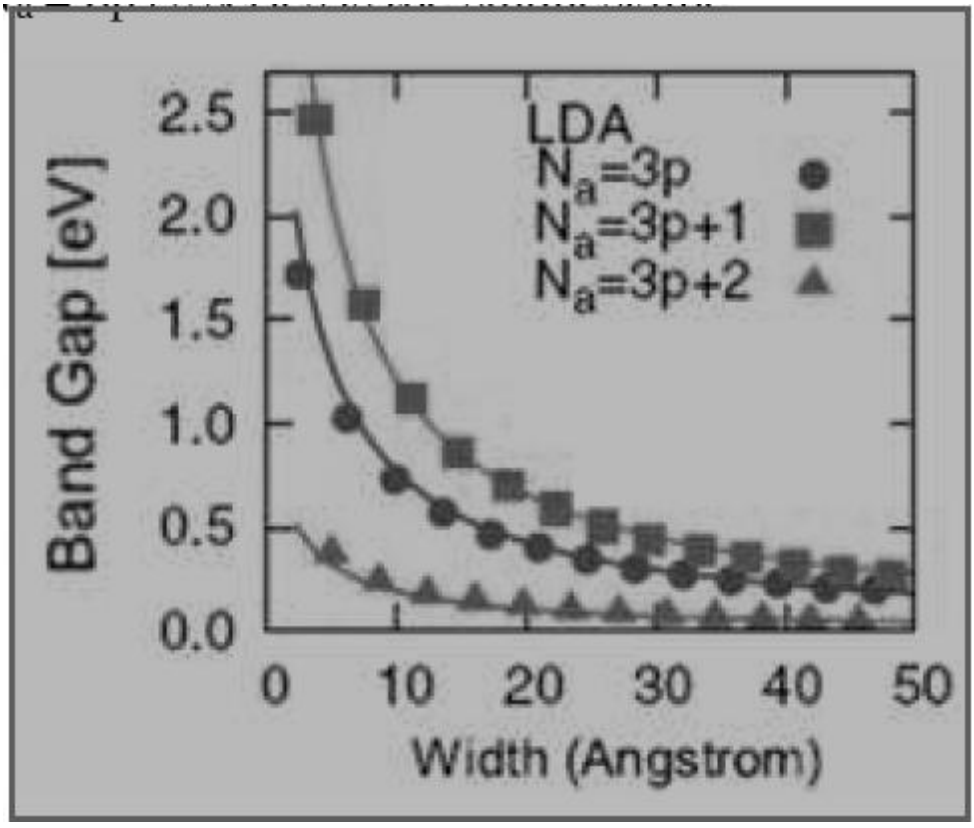

Figure 1.7 Band gap versus ribbon width for arm chair GNR

Electronic properties of zigzag GNR

For nanoribbon with zigzag shaped edges, without taking into account spin states, DFT Calculations have shown that a set of doubly degenerate flat edge-state bands at Fermi level (Ef

) give rise to a very large density of states (DOS) at Ef [54]. If compared to armchair GNRs, the zig zag GNRs have the same hierarchy of band gap-width relationship.

Thermal Conductivity of Graphene Nanoribbon

The unusual thermal properties of graphene include very high in-plane thermal conductivity (strongly affected by interfacial interactions, atomic defects, and edges) and relatively low out-of-plane thermal conductance. The specific heat of graphene is dominated by phonons and is slightly higher that of graphite and diamond below room temperature [55]. The in-plane thermal conductance G of graphene can reach a significant fraction of the theoretical ballistic limit in submicrometer samples, owing to the large phonon mean free path ($\lambda \approx 100$ to 600 nm in supported and suspended samples, respectively) [55]. Nevertheless, this behavior leads to an apparent dependence of thermal conductivity κ on sample length, similar to the behavior of mobility in quasiballistic electronic devices. In the context of integrated electronics, heat dissipation from graphene devices and interconnects is primarily limited by their environment and the relatively weak Vander Waals interfaces of graphene [55]. In the context of graphene composites and 3D architectures, simulation results have suggested that the thermal properties could be highly tunable. Such tunability raises the interesting prospects of both ultrahigh thermal conductivity for heat-sinking applications and ultralow thermal conductivity for thermoelectric applications.

D. Graphene field effect transistors

Graphene, a sheet of carbon one atom thick, has been studied for its capable use in electronics, and was initially recoganized as a material that would take place of silicon and make devices faster and less tedious to manufacture. Not like all other known materials, graphene remains highly stable and conductive even when it is moulded into devices one nanometer wide. The main problem in this material is that when we see its band structure , graphene has no “band gap”. In semiconductors, electrons can be at two different energy levels known as conduction and valance bands. The energy space that exists between the regions is named the band gap. The energy gap between the two permits transistors to switch on and off which allows the storage of information in the ones and zeroes of binary code. This problem can be solved by making

graphene inverters, which is a necessary component of a digital transistor. Graphene devices have grown by leaps and bounds over the past few years, and they are probably the best bet to eventually replace Silicon. Demonstrations like this are important because they show that wafer-scale production is possible, and the properties, while not ideal, are truly impressive, in that they're already beginning to push the limits of Si technology.

Recently Graphene which is sp2 hybridized single layer of graphite forming honey comb lattice of carbon atoms has attracted researchers for its extraordinary properties that includes high mobility ,high strength ,optical properties etc[21,24]. Few years later after the discovery of this wonder material it was predicted that graphene will soon take electronic industry at a higher level [24] and It did what it promised . Graphene due to its ballistic transport properties have worked wonders in CMOS technology and is still progressing at a faster pace. In the last few years the progress in graphene business was very rapid and the graphene's prospects proceeded to improve with every new research. This super material proved to be a potential substitute for silicon in transistors with much better electronic properties [21]. Graphene based devices shows high mobilities as the electrons in graphene act as dirac fermions. Graphene based transistors have reached maximum cut-off frequency of 1THz at the channel length of about 100nm[26] and now the researchers are working towards bendanble electronic devices based on graphene owing to is properties of conductivity, transparency and elasticity[10]. It is declared that graphene technology might supersede Silicon technology by 2020 [26]. what more can be expected?

With the development in nano-device technologies it is necessary to find techniques to reduce the leakage current caused due to band to band tunneling, particularly significant in small scale devices. Leakage is currently the biggest limitation of latest computer processors. Along with taking care of the leakage current this growing industry needs better performance in terms of gain and frequency. Moore's law [1] will cease because of significant passive power consumption due to off-current/leakage current. Power consumption has become the limiting factor for device design. Researchers working in academic and industrial fields are focusing on the ways to reduce this power dissipation [25].

Graphene based devices shows high mobilities as the electrons in graphene act as dirac fermions. But because of the zero bandgap of graphene it was considered unsuitable to be used in

electronic devices because of its low Ion/Ioff ratio. One of the ways to induce a band gap in graphene is to convert Graphene into Graphene Nanoribbon(GNR) which is nothing but a narrowed strip of graphene. The energy gap is inversely proportional to the width of the graphene nanoribbon as shown in Figure 1.7 and this nanoribbon is proved to be a potential candidate for transistor technology.

Chapter 2

LITERATURE REVIEW

Paper on the scaling down process of the components

G.E. Moore (1998) [1], the above cited paper talks about the factors involving the scaling down process of the conventional integrated circuits. It takes into account the rising cost to put more components in a circuit thus reducing the size of the chip and making the chip more denser. The author also talks about the problem of increasing the yield and the production of the integrated chips. It also takes into account the heat problems associated with it. He also said that the density would not increase linear in nature but still a considerable number of the integration would be achieved in the linear circuits in the coming future.

Paper on the limitation of silicon devices while scaling to sustain moores law

Michael Haselman and Scott Hauck [4] in this paper state the problem in silicon mosfets of short length channel which include current leakage, process variation and cost. As the channel length decreases due to which the threshold voltage is lowered and with this the leakage current increases terribly causing the device to consume more power. It tells us about the various factors involved that is, primarily the tunneling currents , which leak through the various barriers in a MOSFET when the dimensions are scaled down and the other being thermally generated currents which are also called as sub-threshold currents. Dynamic power per transistor is decreased when the channel length is decreased, as this decreases the minimum current required in switching the transistor. but, due to increase leakage current discussed above the static current as well as power dissipation is increased. so the Overall, power usage increases due to integration of more transistors on a particular chip area. Fabrication processes also change as the devices ans wire size decreases and with to sustain the change fabrication cost also increases.

Lloyd R.Harriott [5] .in this paper the lithography fabrication process limits are stated which includes resolution, accuracy and throughput are discussed. Researcher also states that the advancement in technology can overcome resolution problem but other ones actually impose limits on lithography scaling. Lithography scaling, the key enabler for Moore's Law, will proceed efficiently for next advanced technology beyond the 100nm and but likely to end at 30nm. There is no shortage of solutions for high-resolution printing methods that can go well beyond 30 nm, but the ultimate limit to lithography scaling will more likely be set by overlay accuracy requirements and economics rather than purely resolution performance.

Papers on High carrier mobility of Graphene

A K. Geim *et al.* (2007) [30], this particular paper gives us a precise and brief idea of the potentials of the Graphene and the future prospects related to it. It starts with the basic structure of graphene and explores the hidden potentials of the graphene. It tells us about the various electronic and conductivity properties of the graphene which makes it a material of the choice for the nanoelectronics. Also the different properties of the graphene have been discussed like thermal properties, the Hall Effect in the graphene, the mass less carriers of the graphene. It gives us an insight of how we can use these remarkable properties of the graphene in our electronic applications and develop a product which is far ahead of the times. So this paper provides us about the very wide perspective of how the graphene out performs the silicon and could be used for the various applications in which silicon is being used.

M.C. Lemme *et al.* (2008) [31], carrier mobility in single and double-gated graphene field effect transistors are compared in this paper. This research shows an astonishing result that reveals that even in double-gated graphene FETs; the carrier mobility exceeds the universal mobility of silicon. In addition to that, reported mobility's for ultra thin body silicon-on-insulator MOSFETs cannot compete with the graphene FET values which can give way to graphene-based nanoelectronics in near future.

Kristen N.Parrish et al (2012) [32] states that Graphene field-effect transistors (GFETs) are the future candidates for due to its high carrier mobility. In this work researcher synthesized graphene monolayer films on cu substrate Using chemical vapor deposition technique. The obtained carrier mobility was greater than 2000 cm2/V-s was obtained on a flexible GFET. And On quartz substrates, even higher mobility ~5000cm2/V-s was obtained for a graphene transistor. An experimental graphene frequency doublers circuit was subsequently realized affording -23dBm of output power at the doubled frequency, with a bandwidth of 3GHz, 2x higher than prior achievement. Finally the novel switching mechanisms have been introduced in the graphene transistors which could be used in the future memory devices.

Paper on ballistic transport of graphene

K. S. Novoselov *et al.* (2004) [33], in this paper a monocrystalline graphite film has been described which is just a few atoms thick and highly stable under ambient conditions. It is metallic in nature and is of high quality. The films demonstrated were found to be two dimensional semi metallic in nature with the valence and the conductance band overlapping slightly. These exhibit a strong ambipolar electric field effect with very high electron and hole density and a high carrier mobility of about 10000 cm^2/ Vs which can be induced by applying the gate voltage.

S. Banerjee *et al.* (2006) [34], in this paper it has been observed that the conductivity of graphene sheets is higher whenever they are loosely bound to the underlying bulk graphite. Also it has been seen that certain edges of the graphene layers show sharp rise in current when biased, indicating enhanced electronic density of states spatially localized near those edges. In certain edges this phenomenon is not observed. The two observations, i.e., enhancement of conductivity of loosely bound layers and sharp rise in current at the edges are discussed with possible reasons and keeping into account the recent theoretical predictions.

Paper on the relativistic nature of carriers in graphene

K. S. Novoselov *et al.* (2005) [37], the above cited paper tells us about the condensed matter system in which the electron transport is carried and is governed by the Dirac equation. Usually what it has been observed is that electronic properties of the most of materials is governed by quasiparticles that behave as non relativistic particles with a finite mass and obey the Schrodinger equation whereas here a condensed system has been reported which tells us about the electron transport which is different and follows the Dirac equation. Their study has revealed a lot about the unusual phenomena characteristic of the two dimensional (2D) Dirac fermions. It is also observed that the conductivity of the graphene never falls below the quantum conductance even if the carrier concentration falls to zero. Also it tells about the charge carriers which mimic the relativistic particles having zero effective mass and travelling at the speed of light. Hence making the ballistic transport possible in the graphene based devices.

Papers on applications of graphene

Viacheslav Sorkin et al (2011) [47] in this work graphene based pressure sensors is made in which the sensing material is graphene nano flakes in a suspended form on SiC substrate ans the edges of graphene have bonding with silicon carbide. Simulation are performed on this device to analyze the pressure change. This research work is a quantative analysis design of pressure sensing device this device is single use so it is cost efficient and easy to operate.

A. Sakhaee-Pour et al (2007)[48] Molecular dynamics is implemented to model the behavior of defect free graphene layer. Behavior of single layer graphene sheets in mass and dust detectors is examined. on the principal of frequencies different mass distribution effects are analysed,it was stated that single layer graphene can detect the particles of order 10^{-6} .this sensitivity is higher than conventional detectors .it increases tha aspect ratio of graphene

Chuan Xu et al (2009) [50] this paper states that GNRs are very efficient candidates of interconnects. A comprehensive conductance and delay analysis of GNR interconnects is presented in this paper. Many graphene nano ribbon models are analyzed for conduction and compared with carbon nano tubes copper tungsten that are being used in traditional interconnect applications. Band gap, mean free path and Fermi level are explored to verify the applicability of

GNR as a interconnect .considering all the parameters graphene proved to better candidate of all the conventionally used interconnect materials.

Papers on Graphene Field Effect Transistors

Liang et al (2007) [35] this paper give a explanation of limits on performance of ballistic graphene nanoribbon field effect transistors. Bandstructure of graphene semiconductor is calculated and I-V characteristics are obtained. It is declared that although narrow channels have leakage current due band to band tuneeling but its ON state current would still be the attractive feature .and this is the motivation behind their employed in high speed devices with a potential to outperform silicon MOSFETs.

Jacub et al (2008) [36] this paper gives the demonstration of how graphene technology can be implemented on SiC substrate,this group for the very first time fabricated hundreds of graphene transistors that gives Ion/Ioff ratio of five which was a very big achievement for electronic industry. The electrical conduction in graphene transistors can be of holes or electrons. At negative gate voltages due to accumulation of holes the current flows and at positive voltages electron current flows due accumulation of electrons. At a point known as dirac point the conduction is minimum and that is contributed by holes and electrons equally.

Joerg et al (2009)[38] gave evidences of for extraordinary properties of graphene. One of the adavantage of graphene is quantum capacitance and it gives a report on width scaling of graphene FETs that improves the Ion /Ioff ratio of the device. Tunneling current that limits the scaling can be scaled according to the width of the graphene channel.

Stephen Thornhill et al (2008) [49] in this paper graphene nanoribbon fielt effect transistor is made and better features are obtained. The results when compared with carbon nanotubes, are found to be similar. There is no effect of defects on the performance characteristics. Bi layer graphene gives higher throughput in comparison to single layer graphene.arm chair and zigzag type GNRs produced similar I-V curves.

Frank Schwierz (2011)[39] demonstrated how graphene is a material very appropriate for its employment in field effect devices with cutoff frequency of 300GHz. This paper also shed some light on the limitation of graphene field effect transistors that it has a gapless band gap. Zero bad gap restrict its application in logic transistor or for switching applications. Narrow graphene field effect transistors are suggested that induces a bandgap and then can be used as channel material for logic FETs.

Michael et al (2012) [40] reported a 500nm graphene field effect transistor giving frequency of 3GHz which is double than the frequency of conventiaonal transistors.this means the device will be two times faster. A high quality graphene was patterened with carrier mobilities of 5000cm^2/V-s. the GFET devices provide double frequency because of its ambipolar characteristics.

Chung-yung Sung (2011) [41] this paper gives a report of implementation of graphene field effect transistors that yielded a cut off frequency greater than 200GHz. The graphene P-N junction can be used for witching applications which is 86% faster than Si CMOS. This report also suggest that much research needs to be done on channel scaling , reducing contact resistance and take care of other extraordinary properties of graphene.

Youngki et al (2013) [42] compared the graphene nanoribbon mosfets with doped contacts and graphene MOSFETs (GNRFET) with metallic contacts (SBFET). It was reported that GNRFETs have 50% better ON state current than SBFETs and GNRFETs gives significantly larger Ion/Ioff ratio. GNRFETs gave 30% better performance in terms of frequency and are 20% better performance in terms of speed than SBFETs. if the impurities are introduced in the channel MOSFETs show more robustness than SBFETs.

Summary of Current Technology

Due to the leakage currents in scaled down silicon devices, Moore's law seem to cease in the coming years. The new technology that can replace todays technology is nanoelecronics. And have already proved that it has potentials to work in electronic industry and compete with the conventionally used material, silicon. After having gathered the information on the current technology, we had a better understanding of the graphene and the devices that can be implemented. The first basic thing that has been concluded from this information is that it is possible to characterize a Graphene Nanoribbon Field based devices in the same way as silicon based devices. Graphene FETs have seen many ups and downs in its advancement and finally have reached the level where it can be now commercialized as field effect transistors. Its high mobility, high strength, nano scale size, ballistic transport are the factor that provides the motivation for its implementation as field effect transistors. Graphene FETs have shown some of the problems during its initial development like zero band gap the solution of which is now available. Renowned company like IBM have developed a graphene field effect transistor in 2011 and gave a start to its commertialization. Finally, there is a need for more research and advancement in this field.

Chapter 3
SCOPE AND OBJECTIVE OF STUDY

In this work the graphene based field effect transistor will be focused. As the electronic device industry is growing faster there is need of better and efficient technology. In many systems, speed is fundamental. There are a number of passive and active devices that can be used to as sensors, switches and amplifiers etc. A transistor with high frequency, low power dissipation, high gain and high area efficiency is the exigency of todays industry. Many research scholars in academic and industrial field are working to satisfy the above mentioned requirements. In this study will be working on following things:

- Design graphene based MOSFET structure .
- Stimulate that device structure to get the transfer and output characteristics.
- Compare the obtained results with the already published results.
- Change different parameters of device and obtain the I-V curves to compare the results with previous results.
- To give optimum values of device characteristics that shows optimum performance characteristics.

The scope of this work is limited to the design of a field effect transistor and and analyse its behavior.

OBJECTIVES

With the development in nano-device technologies it is necessary to find techniques to reduce the leakage current, which is particularly significant in small scale devices. Leakage is currently the biggest limitation of latest computer processors. Moore's law [1] will cease because of significant passive power consumption due to leakage current. Along with taking care of the leakage current this growing industry needs better performance in terms of gain and frequency. Power consumption has become the limiting factor for device design. Researchers working in academic and industrial fields are focusing on the ways to reduce this power dissipation[25].

Various engineered devices have been proposed concerning the need for low power consuming devices. Reasearchers are looking for a different technology that can give good results even at extensively small channel lengths.

1: To prove that graphene has potential to be used in graphene field effect transistor

2: To prove that the graphene nanoribbon based devices would be better in terms of different performance characteristics as when compared to the present day silicon based devices.

3: optimization of graphene field effect transitor in terms of channel length, gate oxide thickness, source drain material etc

4: Finally develop a graphene nanoribbon field effect transistor, which would be better in terms of leakage current, power dissipation, switching delay, frequency and gain.

Chapter 4
MATERIAL AND RESEARCH METHODOLOGY

Dual gated geometry of GNRFET is assembled as shown in Figure 5.1 with 1nm SiO_2 gate insulator (κ=3.9), 20nm channel length, 10nm source and drain terminals. The double gate MOSFET is used because it enhances the gate control capabilities of the device [42]. The gate dielectric used is well known for its high thermal and chemical stability and therefore perfect for the use in graphene based MOSFETs. The channel material is a perfectly patterned armchair edge type Graphene Nanoribbon (12-AGNR) as shown in Figure 2(b) with a band gap of ~ 0.6eV, width of the ribbon is ~1.37nm (6 atoms along the width of nanoribbon). SiO_2 is used as a dielectric owing to its best dielectric properties and lesser leakage current inducing properties than other insulating materials [12]. Step doping is used in the patterned GNR with the channel area of 20nm as intrinsic and the source and drain of 10nm each are doped with fully ionized dopants.

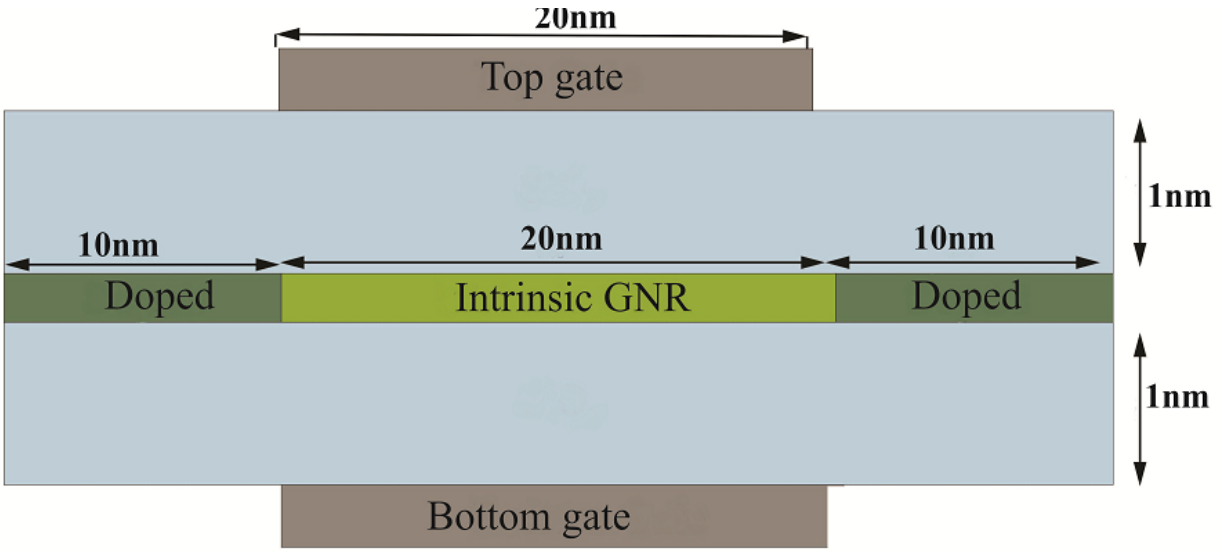

Figure 4.1 crossectional geometry of graphene field effect transistor

Three dimensional poisson solver is used which solves the poisson equation given by

$$\nabla(\in(\vec{r})\nabla\emptyset(\vec{r})] = -q[p(\vec{r}) - n(\vec{r}) + N_D(\vec{r}) - N_A(\vec{r}) + \rho_{fix}]$$

where $\in(\vec{r})$ is dielectric constant, $\emptyset(\vec{r})$ - electrostatic potential, N_A and N_D are donor and acceptor concentration respectively and ρ_{fix} is the fixed charge. The self consistently solved possion's equation gives the potential ∅ that represents the electron-electron interactions.

To stimulate the device characteristics Non equilibrium green function formalism is used is considered self consistently coupled with 3D solution poisson-schrodinger equation. where green's function is represented as:

$$G(E)=[EI - H - \sum_S - \sum_D]^{-1}$$

Where E represent energy ,I is the identity matrix ,H is the Hamiltonian of graphene naoribbon used ,$\sum_S$ represents self energy of source terminal and $\sum_D$ represents the self energy of drain terminal. H gives the description of the isolated device. The Hamiltonian (H) of the device is determined from π orbital tight binding nearest neighbor model. These self energy matrices ($\sum$) are added to the H in order to account for device coupling to the reservoirs. All These matrices stores all the physics of the device that is to be simulated. Assuming the ballistic transport in graphene channel real approach is followed with dirac Hamiltonian constructed with atomistic (p_z orbital) bases and tight binding model with tight binding parameter t=2.7eV which is suitable parameter for arm chair graphene obtained from Extended Huckel's theory in order to describe the characteristics of GNRFET.

After this electron and hole concentration is represented as $n(\vec{r})$ and $p(\vec{r})$ respectively.

Where

$$n(\vec{r}) = 2\int_{Ei}^{+\infty}.dE[|\Psi_s(E,\vec{r})|^2 f(E - E_{FS}) + |\Psi_D(E,\vec{r})|^2 f(E - E_{FD})]$$

$$p(\vec{r}) = 2\int_{Ei}^{+\infty}.dE[|\Psi_s(E,\vec{r})|^2 (1- f(E - E_{FS})) + |\Psi_D(E,\vec{r})|^2 (1- f(E - E_{FD}))]$$

where $\vec{r}$ is the coordinate of the carbon site, f is the Fermi dirac occupation factor ,fermi level of source and drain is represented as E_{FS} and E_{FD} respectively and $|\Psi_s|^2$ and $|\Psi_D|^2$ is the probability of reaching of states the point i.e $\vec{r}$ injected by source and drain respectively.

Current is calculated using a well known landauer's formula for current calculation in nanoscale devices given by:

$$I = \frac{2q}{h}\int_{-\infty}^{+\infty} dE\, T(E)[f(E - E_{FS}) - f(E - E_{FD})]$$

Where q is the electron charge, h is the Planck's constant and T(E) is the transmission coefficient

$$T = -T_r \left[(\sum_S - \sum_S^{\dagger}) G (\sum_D - \sum_D^{\dagger}) G^{\dagger}\right]$$

As already stated the schrodinger equation was solved by Green's function, the technique used to compute green's function is Recursive Green's Function (RGF) technique. Results are obtained by a code based on Newton-Raphson method in which one starts with a value reasonably closer to the root and then the iterations are performed to satisfy a condition and the true root is obtained.

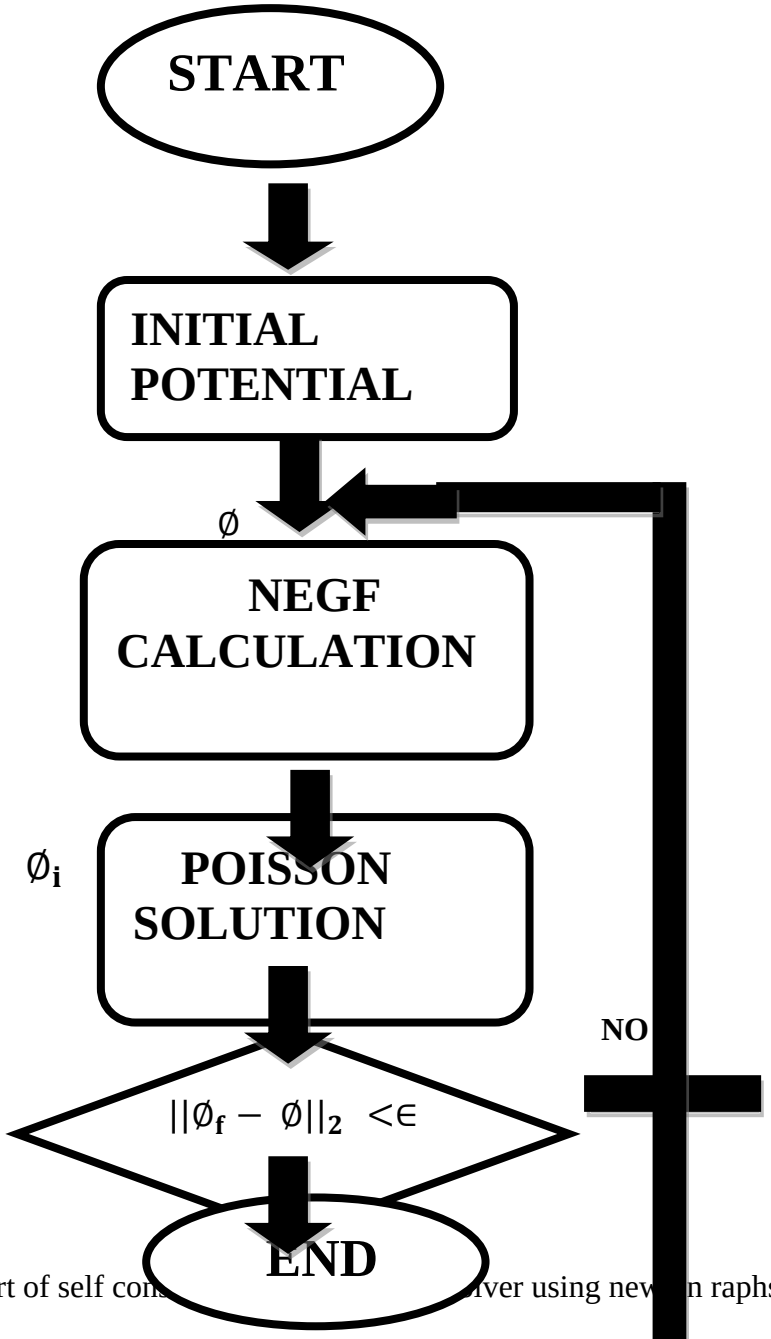

Figure:4.2 Flowchart of self con iver using new n raphson algorithm.

All these simulations are performed on open source software Nano Tcad Vides.[45]

Input Parameters	Default Values
Gate Insulator Thickness, t (nm)	Boltzmann's Constant, k= 1.8 *10^{-23} J/K
	Planck's constant,h= 6.63* 10^{-23}
Relative dielectric constant, ε_r	Reduced Planck's constant, ħ= 1.05*10^{-34}
Temperature, T (K)	
Gate Voltage, V_G(V)	Mass of electron, m_0= 9.11 10^{-31} kg
Drain Voltage, V_D(V)	Source Fermi level, E_f= 0.32eV
	Overlap integral of tight bonding C-C model, ς= 2.7 eV
Channel Length, Lch(nm)	Charge of an electron, q=1.6 10-19 C
	Permittivity of free space, ε0= 8.854 10-12 C-C bond length, ac-c= 1.42 10-10 m

Table 4.1 Parameters and Constants used in simulations.

The basic steps involved to proceed with this work are:

1: To study more on Field effect behavior of graphene nano ribbon some articles regarding performance of graphene FETs are read some more information can be gathered by looking into some more literature .By going for more in depth studies deciding the model for Graphene based device that used graphene nano ribbon will be easier.

2. Learn using the software : As nano electronics is a newer field than conventional microelectronics the software developed for the simulation of the models made with nano structure are different and the basis behind the result involves quantum theories that the much

complex than the microelectronic theories. The software we will be using is the non equilibrium green's function. Different commands used are studied extensively

3. Learning pyrhon script : As the input files that are provided to this software are the python scripts. It was necessary to learn python language basic commands.

4. Starting with the simulations : This research involves the study of behavior variation in the I-V characteristics on changing the parameters. The python scripts are simulated and outputs are plotted in the Microsoft excel.

Chapter 5

RESULT AND DISCUSSION

Simulation the device with variations in the parameter affected the I-V characteristics. These variations in I-V characteristics gave a insight into the scope of reducing off currents and power dissipation hence, increasing the performance of the graphene transistor. The simulation started with changing the width and length of the channel to the source and drain terminal material. Finally all the I-V plots together suggest a way of designing a graphene field effect transistors with superior performance in terms of speed and power dissipation. For the simulations device with default values as described in previous chapter is used at default temperature of 300 K.

5.1 Changing the channel length

The simulation task started with changing the channel length because channel length is the most vital parameter of electronic industry. Channel length which is more formally called as the technology is so much significant that the manufacturer rate the device on basis of its channel length. Lesser is the channel length better is the technology.

In this section the effect of channel length variation is discussed. As shownFigure 7.1 As we increase the channel length the channel current start decreasing. As the channel length is decreased to 100 nm the channel current is the maximum. These results are obtained by simulating verilogA model of graphene field effect transistor developed by a certain research group. These plots are verified with the results of expericental data obtained by IBM.

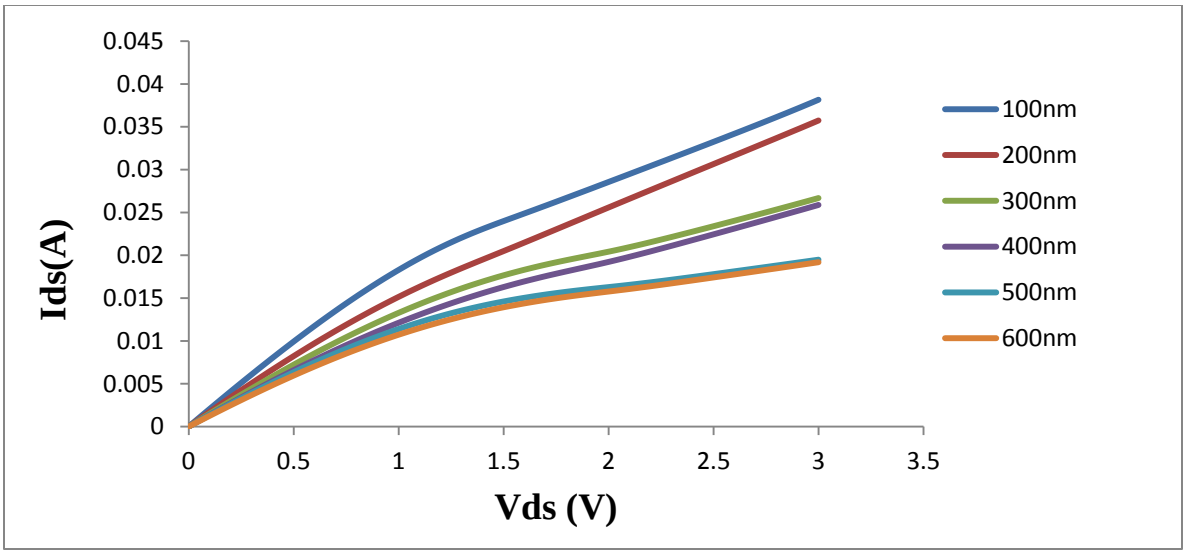

Figure 5.1: Output characteristics of graphene field effect transistor at different channel length.

Figure 5.2 shows the input characteristics of the device at different channel lengths. These plots gives the idea the as the channel length reduces more charge density is there and more is the current so at minimum channel length of 100nm we have the maximum current value. But as we decrease the channel length the Ion- Ioff ratio is increased as shown in figure 5.3.

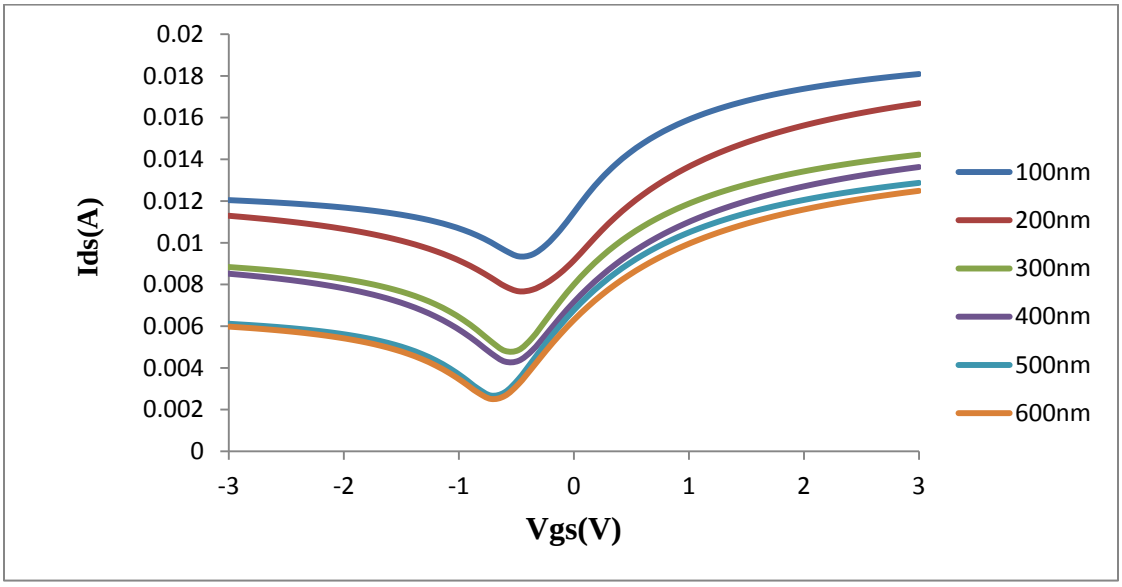

Figure 5.2 : Input characteristics of graphene field effect transistor at the drain voltage of 0.3V at different channel lengths.

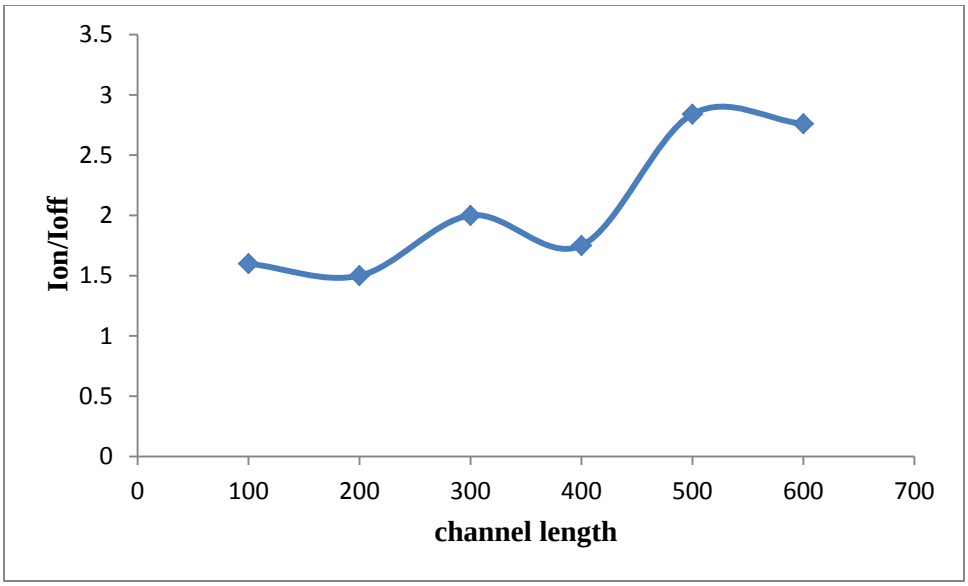

Figure 5.3 Ratio of on state current to off state current with respect to channel length at drain voltage of 0.3 V.

This plot says that we cannot decrease the channel length as the Ion/Ioff ratio gradually decreases from 3 to 1.5 as the channel length changes from 600nm to 100nm. Even at maximum channel length Ion-Ioff ratio is still less to be used in digital applications.

5.2 From Graphene to Graphene nanoribbon.

Graphene based devices shows high mobilities as the electrons in graphene act as dirac fermions. But because of the zero bandgap of graphene it was considered unsuitable to be used in electronic devices because of its low Ion/Ioff ratio. One of the ways to induce a band gap in graphene is to convert Graphene into Graphene Nanoribbon(GNR) which is nothing but a narrowed strip of graphene. The energy gap is inversely proportional to the width of the graphene nanoribbon as shown in Figure 5.4. and this nanoribbon is proved to be a potential candidate for transistor technology [7].

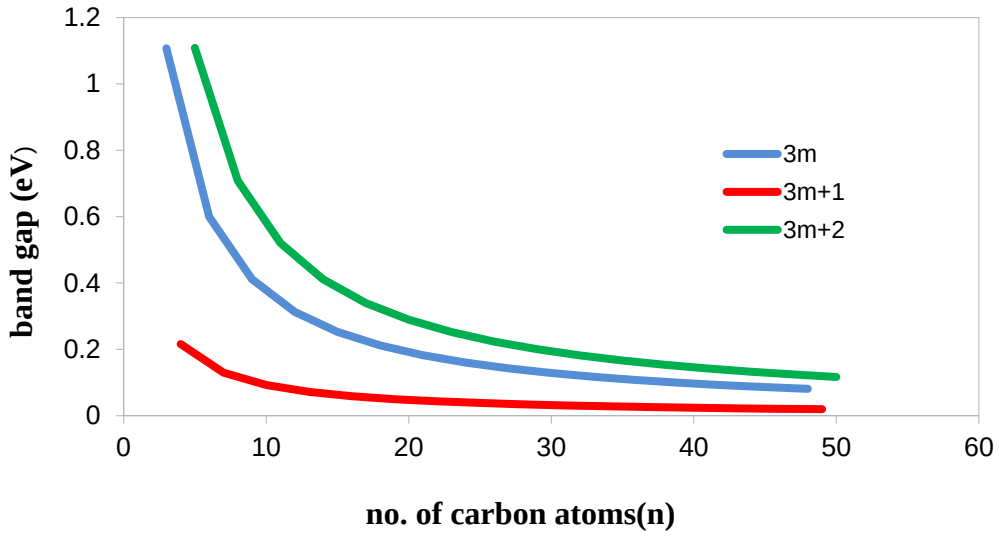

Figure 5.4 Band gap versus number of carbon atoms in the width of graphene channel where m is any integer.

With the induction of the band gap there is decrease in the off current hence the Ion-Ioff ratio increases. Figure 5.5 clearly shows that even at 20nm channel length graphene nanoribbon shows high Ion-Ioff ratio approximately 100 where as the input characteristics clearly depicts that this ratio is not more than 4 even at 600nm of channel length. So to save power with less off state current and better digital characteristics graphene nanoribbon field effect transistor came into action.

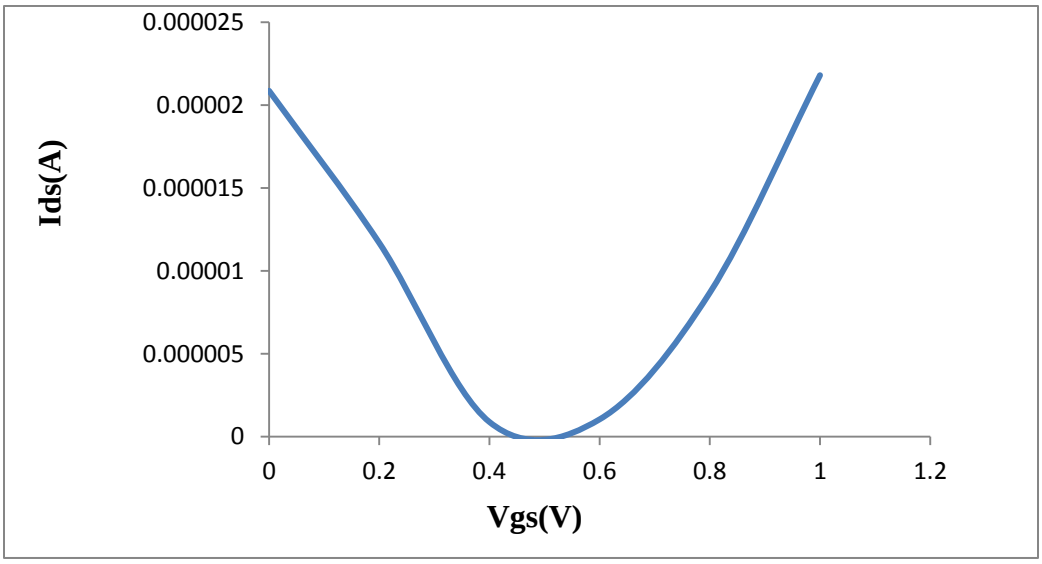

Figure5.5 : input characteristics of graphene nanoribbon transistor with channel length of 20nm and supplied drain voltage of 0.3V.

5.3 Change in the Temperature

changing the temperature of graphene field effect transistor the changes the On current of the device as shown in figure 7.5. As the temperature is increased the on sate channel current increases. This increase in current with the temperature is due the linear decrease in channel resistance of the graphene nanoribbon with the increase in temperature[162]. The current changing effect in a simple graphene nanoribbon sheet with the change in temperature can be seen fron the figure 5.6.

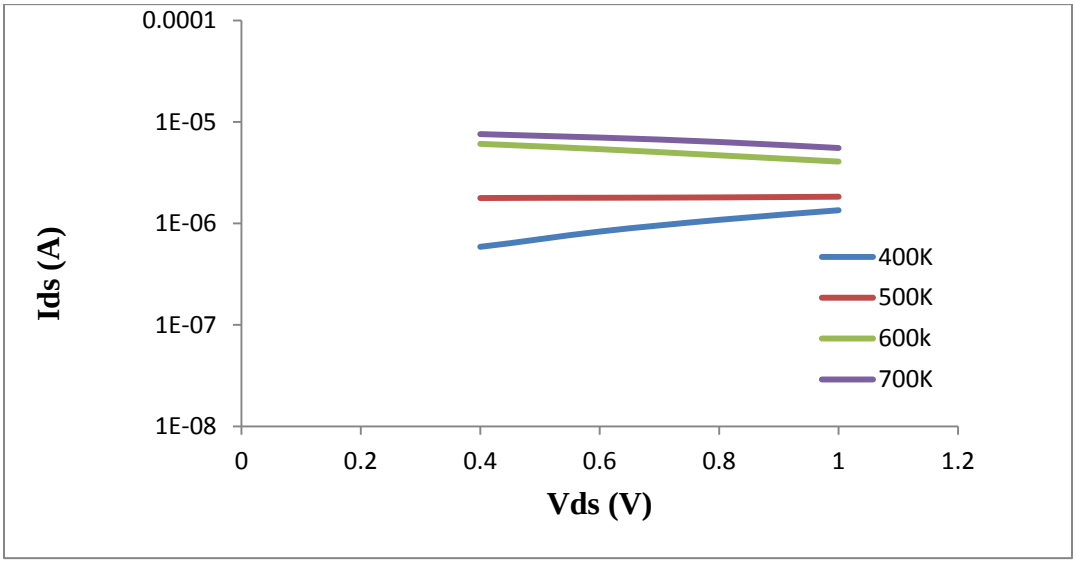

Figure 5.5 Output Characteristics of graphene nanoribbon field effect transistor at Vgs of 0.5V at different temperatures.

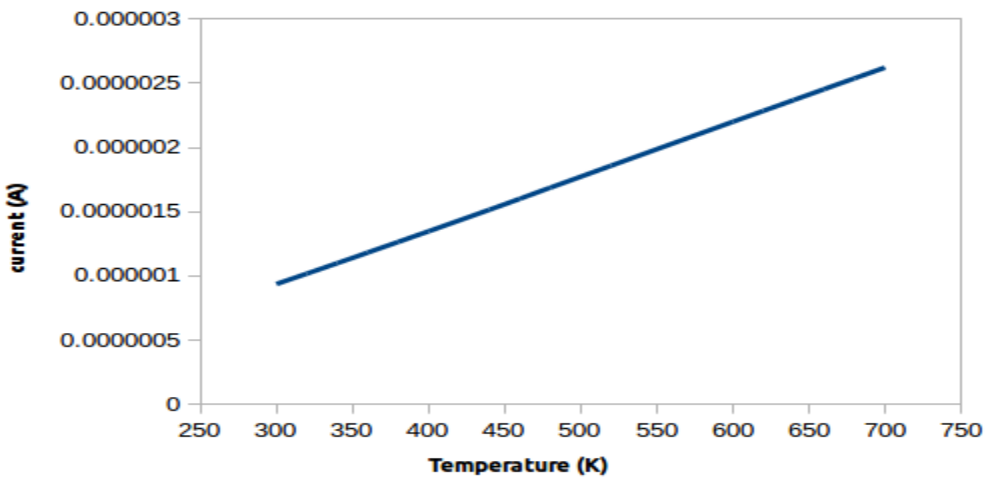

Figure 5.6 current variation in graphene nonnoribbon sheet at constant terminal voltage of 0.3V.

This results tells that the working temperature of the graphene nanoribbon devices should not increase much otherwise it can change the current values and deviate from the expected outcomes. Small temperture variations may not harm the device characteritics but large temperature changes may cause the results to deviate.

5.4 Change in Gate Oxide Thickness

over the past decades the the researchers in academia and industry are working on miniaturization of devices not only in terms of length and width but also the gate dielectric material. As the gate dielectric thickness reduces to 1.3 nm the electrons tunneling is dominated and large leakage curent due to tunneling of electrons leads to device failure. Figure 5.7 shows the variations in input characteristics with the change in gate oxide thickness from 1nm to 2nm.

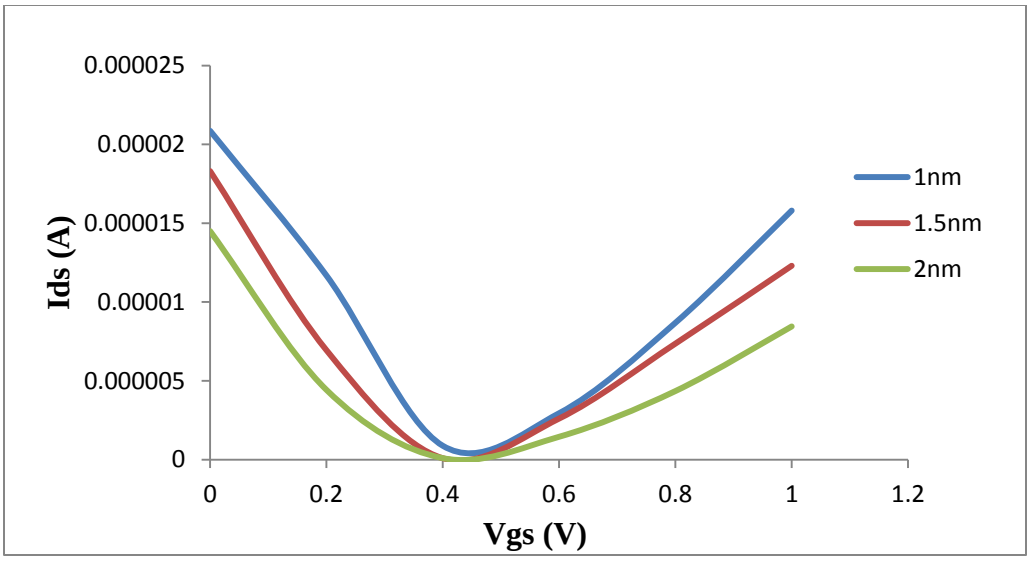

Figure 5.7 Ids-Vgs at different oxide thickness and constant drain voltage of 0.3V.

Gate insulator should be thin to have superior control over the channel current but thinner gate oxide induces leakage current as can be clearly depicted by figure 5.7. but the leakage current increase is lower than on current increase so we can afford to have minimum thickness of gate oxide for graphene nano ribbon field effect transistor. The increase in on current grain current with decrease in thickness is beneficial and can be seen in output characteristics in figure 5.8.

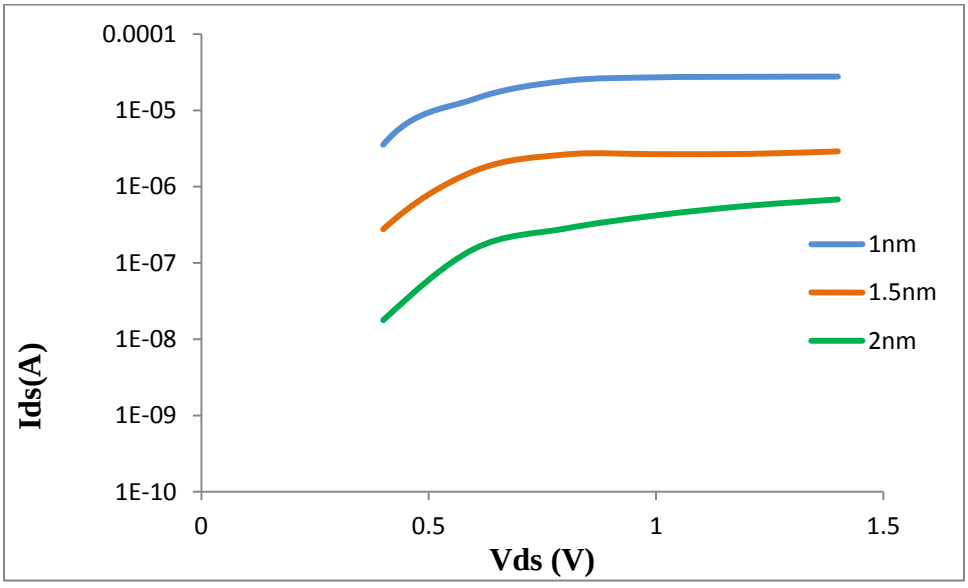

Figure 5.8 Ids-Vds at different gate oxide thickness and contant drain voltage of 0.3V.

5.5 Change in the Dielectric Material

with thinner oxides transistors face tunneling and hence the unwanted leakage current flows to overcome this we can use high dielectric constant material. Changing the dielectric material can also improve the performance of the device,. The most commonly used material is SiO_2 because of its good thermal and electrical insulation properties. however if we use high dielectric constant material we can increase the channel current.

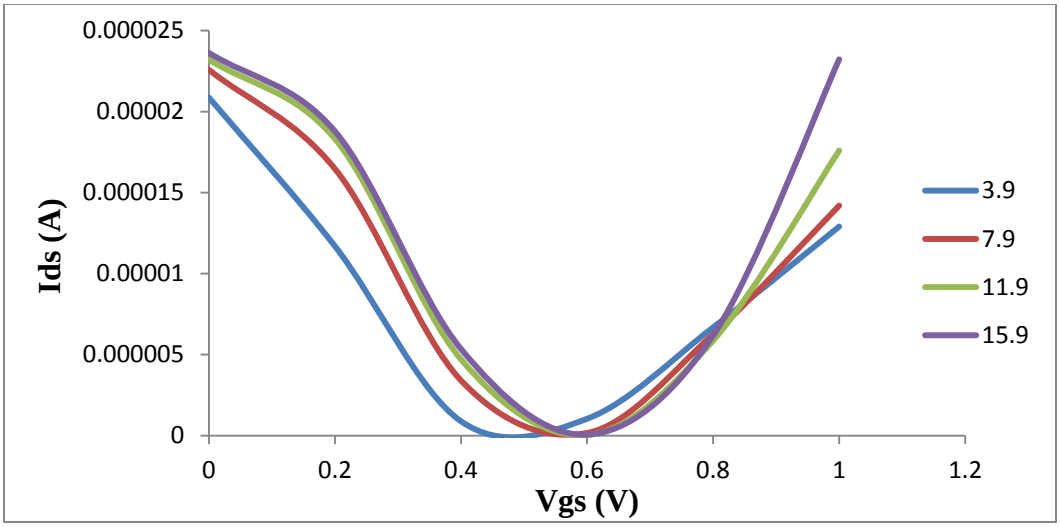

Figure 5.9 Input Characteristics of Graphene Nanoribbon field effect transistor at different dielectric constants.

Figure 5.9 shows that with the increase the dielctric contant the off currents do not rise much but the on current increases significantly leading to better Ion-Ioff ratio. Figure 5.10 shows the output characteristics at different dielectric constants. On current with dielectric constant of 3.9 is $1.1905*10^{-4}$ and with dielectric constant of 15.9, it is $9.77*10^{-4}$.

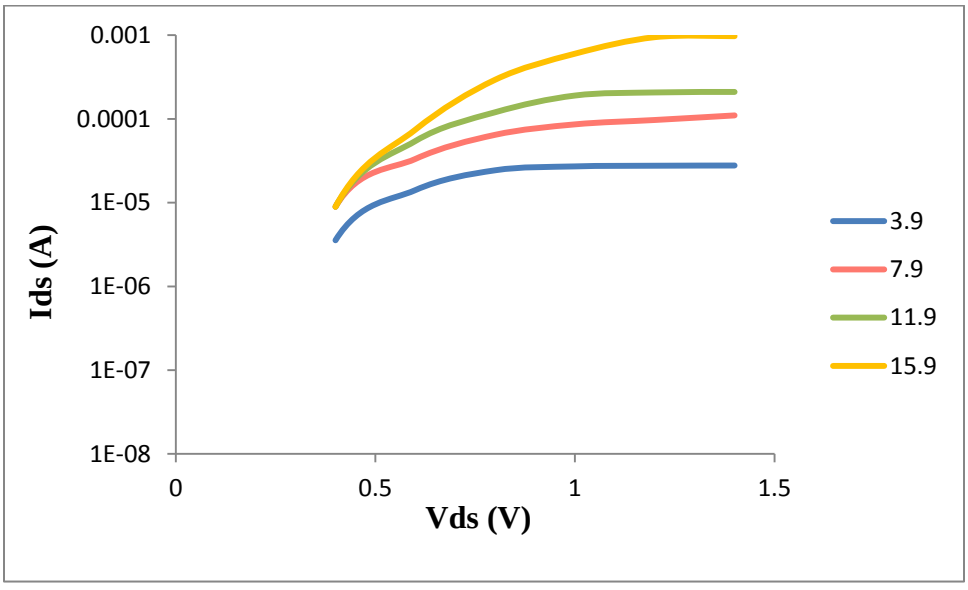

Figure 5.10 output characteristics of Graphene Nanoribbon field effect transistor at different dielectric constants.

Some of the dielectrics that match the simulated values are SiO_2 with dielctric constant of 3.9, silicon nitride Si_3N_4 with dielctric constant of 7.9, yttrium oxide Y_2O_3 with dielectric constant of 15 and other material that are suitable are hafnium oxide hfO_2 , alluminium oxide Al_2O_3 etc [12].

5.6 Changing the source/drain material.

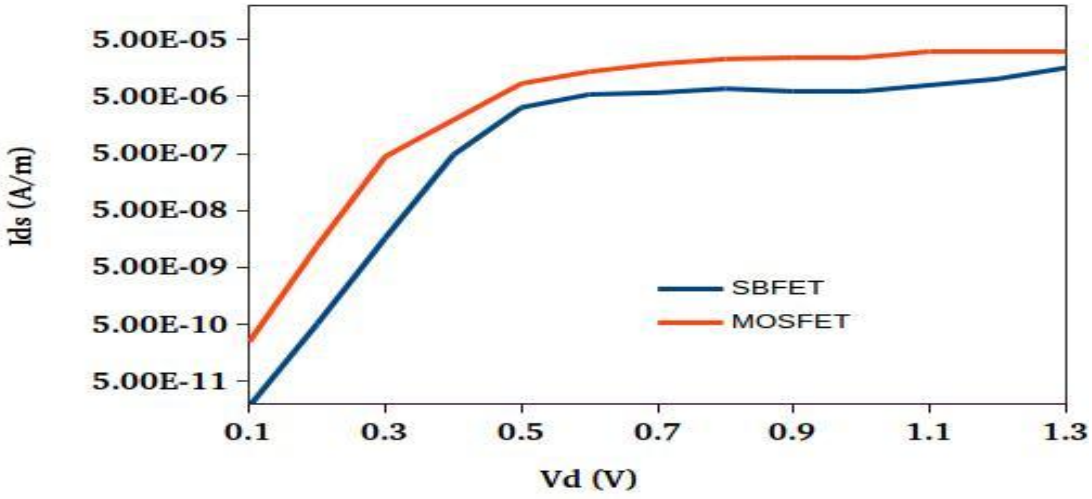

Figure 5.11 output characteristics of graphene nanoribbon field effect transistor with ohmic contacts(MOSFET) and metallic contacts (SBFET).

GNR field-effect transistors (GNRFETs) have been fabricated very recently [58]. Most of the GNRFETs are demonstrated experimentally , by connecting the channel to source and drain terminals through metals forming with Schottky contacts [59], therefore such kind of FET is called Schottky barrier FET (SBFET). Another type of source drain contacts are ohmic contacts that can in principle be obtained by heavily doping the GNR source and drain , making the device operation MOSFET-like and hence called MOSFET in the following text. Since fabrication techniques are at the very first steps, simulations can represent an important tool to evaluate device performance. However, due to the embryonic stage of this new field of research, many issues still remain unsolved. It is, for example, not clear how much performance improvement can be obtained by using a MOSFET device structure, as compared to the Schottky contacts counterpart, as well as the extent to which non-idealities can affect device characteristics.

In this work, GNR SBFET and MOSFET are numerically studied in order to establish their potential and the performance that can be expected if technological challenges are met. As can be seen from the figure 5.11 the MOSFET shows better on current than SBFET the saturation current for MOSFETs is $5.26*10^{-6}$ and SBFET is $5.67*10^{-7}$. From the graph we can see that MOSFET has better saturation behavior than SBFET. The better saturation characteristic can be confirmed by taking the slope of the plots in the saturation region , this slope is technologicaly called as output transconductance denoted by $G_{d.}$ This G_d is (1.1-4.5/0.4) $8.5*10^{-5}$ for MOSFETs and G_d for SBFET is (7.12-.55/0.4) $16.425*10^{-5}$.

5.7 Changing the source/drain doping concentration

In this section Graphene Nanoribbon Field Effect Transistor is numerically studied at different percentage of doping concentration of source-drain (S/D) terminals of the devices. To exploit full capabilities of a nano scaled field effect transistor S/D engineering is also a significant study. Step doping profile for S/D doping is used as shown in Figure 5.12. Other device parameters are kept same while input/output characteristics, frequency, transconductance and switching time at different doping concentrations are obtained. Effect of dopant quantity in the terminals is analysed and an optimum doping value is suggested accounting power dissipation, frequency, Ion-Ioff ratio and gain. It is found that on increasing the doping concentration lateral leakage current increases and other performance parameters also degrade. This work suggests an approximate value of optimum doping concentration that shows better characteristics than at other doping concentrations.

This curve shown in Figure 5.13(a) indicates that at 0.5%(aproximately 3 doping atoms in total of 540 carbon atoms) ,1%(aprroximately 5 atom in total of 540 carbon atom) and 2% (approximately 11 atoms in 540 atoms) (S/D) doping concentratin ,the off current is very high. At 0.5% the off current is higher than the OFF current (Ioff) at any other doping concentration which is equal to 2.08e-5 A/m and can cause a high power dissipation which is not acceptable so doping of source and drain is neccesary to minimize the power loss. Ioff is the minimum drain current. At 3% doping the off current is minimum leading to minimum power loss at this concentration. When we increase the doping concentration to 4%(aprroximately 22 doping atoms in total 540 carbon atoms) and so upto 10% the off current again increases gradually.

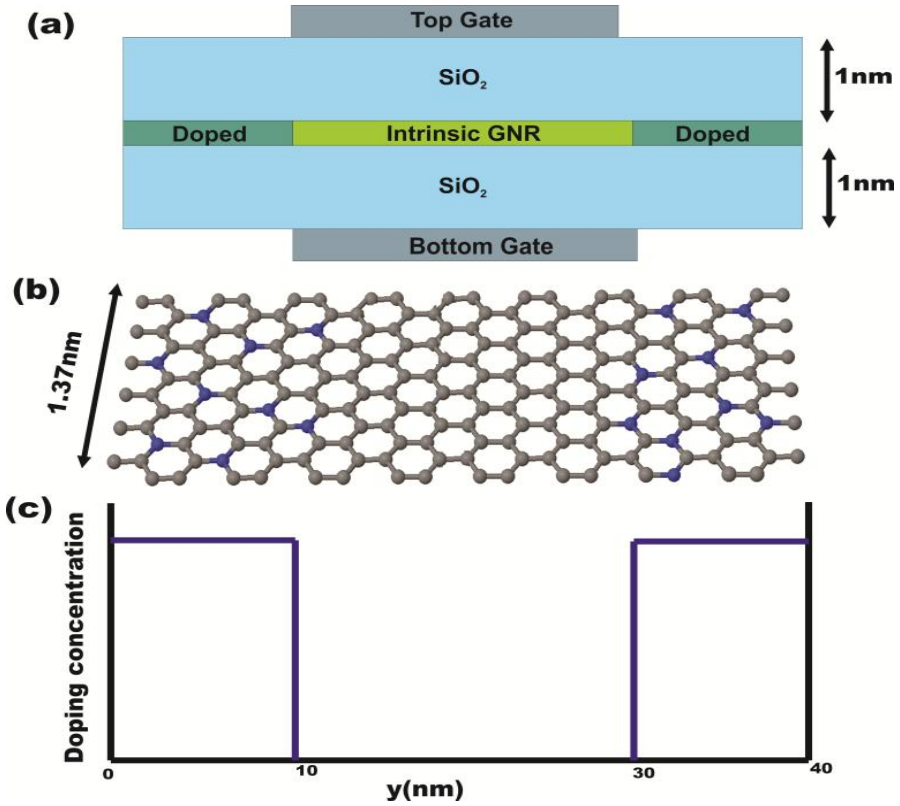

Figure 5.12 (a) cross sectional view of simulated device 1nm wide silicon dioxide insulator for both back gate and top gate, both top gate and back gates of 20nm, intrinsic graphene material for channel is 20nm and source and drain contacts of 10nm each (b) perfectly patterned graphene nanoribbon of width 1.37nm and length of 40 nm in which 20 nm is used as intrinsic channel and 10nm is the doped source and drain terminals(ohmic contacts) (c) represents the step doping profile in which doping is done in the 10nm part from both the sides.

The cause of increase in the leakage current with the increase in doping concentration is the band to band tunneling. Quantum NEGF simulation provides the models for Klein Band to Band tunneling in devices with channel legnth below 100nm. With the increase in dopants in the source the barrier hieght between source and the channel goes higher and thus increases the tunneling probability that induces a leakage current that keeps on increasing with the doping concentration as shown in Figure 5.13(b). As the doping concentration increases till 3% the path for band to band tunneling narrows but after 3% as the doping concentration increases the band structure for the device provides broader paths for the tunning current.

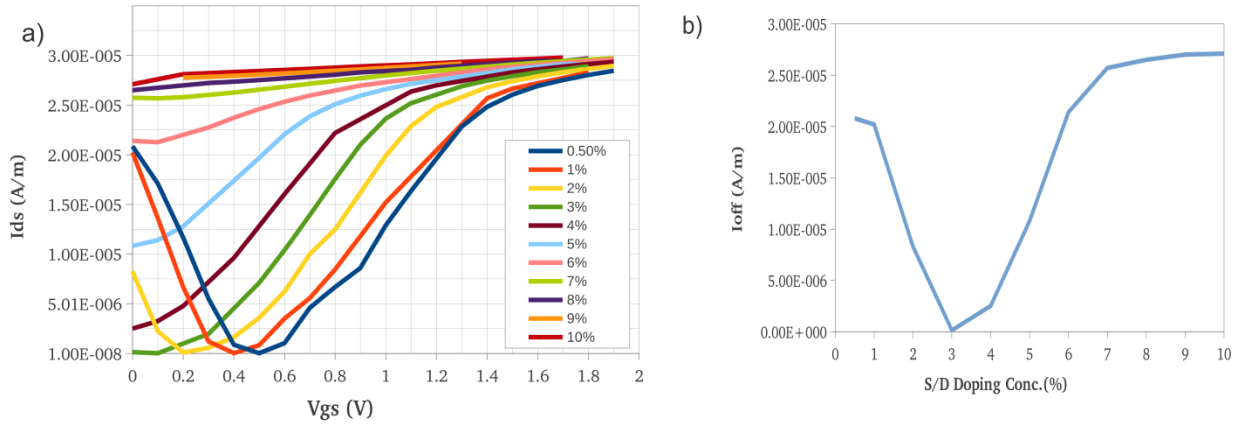

Figure 5.13(a) Ids-Vgs curve is shown at different percentage of (S/D) doping concentration with vds=0.3V .(step size is 0.1V) .(b) Ioff versus S/D doping concentration

More the ON state current more favourable is the device performance. So accordingly we need a high ON state current and low OFF state current as discussed in the former text. The ratio of Ion to Ioff should be high for device with good operating potentials. As shown in Figure 5.14(a) when the S/D doping concentration increases upto 3% the ion/ioff increases and after 3% as we move towards 10% of dopants in total carbon atoms the Ion/Ioff value decreases showing maximum at 3%. So to maintain good Ion/Ioff value the S/D doping concentration should be around 3%.

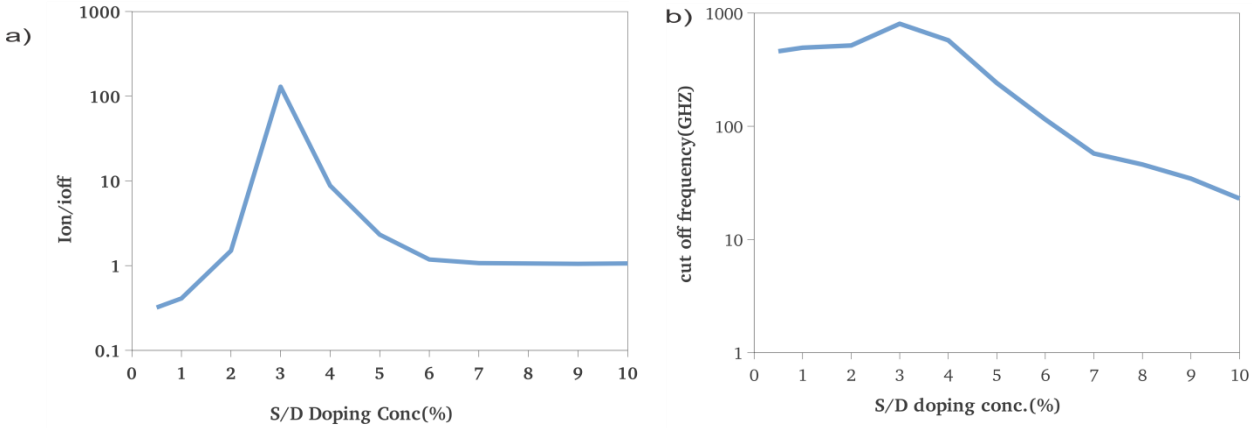

Figure 5.14 (a) Ion/Ioff versus S/D doping concentration(b) cut off frequency versus S/D doping concentration

For a MOSFET to be used as amplifier we must limit doping concentration of S/D regions as with the increase in number of dopants in S/D transconductance decreases and hence the

amplifying potential decreses. The significant reduction in the gain is not accetable. Transconductance is directly proportion to the cut off frequency of the device which is given by:

$$f_T = \frac{gm}{2\pi C_G}$$

Where gm is the transconductance and C_G is the gate capacitance[60]. Recent research works have proved the intrinsic cutt off frequency of graphene MOSFETs at sub 100nm channel length is in the range of few hundreds of giga hertz which significantly outperform the conventional silicon channel MOS devices[56-57]. From Figure 5.14(b) It can be inferred that as we increase the number of dopants in source and drain terminals of the device the cut off frequency decrease and the device performance degrades. In addition, parasitic capacitances are not accounted for the cut-off frequency of the devices and can effect the frequency values.

Chapter 8

CONCLUSION AND FUTURE SCOPE

Today one of the most extensively studied nanomaterial is graphene and is being focused by scholars in the field of electronics for its superior performance as field effect transistors. However the device fabrication at nanoscale face number of problems like defect and material variations. Graphene is known for its high mobility so with this kind of material, devices with high performance are expected to be designed. In this work comparative evaluation is performed with graphene field effect transistor with different parameter and their variations.

In the first section we simulated device that uses graphene channel and found that as we reduce the channel length , the current increases accordingly. So for a device with better performance the user is expected to take small channel length. It was also noticed that the Ion/Ioff ratio is very low that means there will be large power dissipation.

In the second section the study proceeded with changing the channel material from graphene to graphene nanoribbon. Using graphene nanoribbon significantly increased the Ion to Ioff ratio hence leads to lesser power dissipation.

In the third section the effect of changing external temperature was diccussed . it was observed that increasing the temperature leads to variations in the nanoribbon channel resistance and hence the drain current. So for proper working of the device the constant room temperature of 300K should be maintained.

In the fourth section effect of changing the dielectric constant of gate oxide is observed and it say that choosing a high dielectric constant material will lead to large drain current and high Ion-Ioff ratio.

In the fifth section gate oxide width was varied and the I-V characteristics were analysed. It was seen that unlike conventional Si transistors , graphene nanoribbon field effect transistor

generates small increase in leakage current on reducing the gate oxide thickness along with significant increase in on current. This promises its better performance than Si transistors at csaled dimensions.

In sixth section we compared the schottky contact transistor with the ohmic contact transistor. The ohmic contact FET prove to be better in term of On current and output conductance than schottky FET.

In the last section we optimized the doping concentration of ohmic contact with respect to power dissipation and speed of the device. It was found that with 12 AGNR the optimum doping concentration is aroung 3%.

DEVICE PARAMETER	OPTIMUMIZED VALUE
Channel Material	Graphene Nanoribbon
Length	20nm(can be any minimum length)
Temperature	300K
Oxide thickness	1nm
Oxide value	15.9 (can be higher) or 3.9
contacts	Ohmic contacts
No of atoms in Channel width	6 (12 AGNR)
Doping concentration	3%

Table 6.1 Proposed optimized values.

Future scope

- In future this study can be extended to working with another substitutes for channel material like Carbon nanotube and other organic material. Finally the best channel material will be determined.
- Further optimization can be done with respect to particular application for example Amplifier and device can be optimized to have maximum gain.
- There is much research going on for developing different models for graphene field effect transistor . A comparative study can be done with respect to differet physics models.
- After all this a physics model can be developed in one of the languages like verilog A or Hspice keeping all the optimized parameter in mind.

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