Designing of Power Amplifier in 180, 90 and 45nm CMOS Process

DISSERTATION-II REPORT

Submitted in the partial fulfillment of the requirement for the award of degree

Masters of Technology

In

ECE

Submitted by

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Under the guidance of

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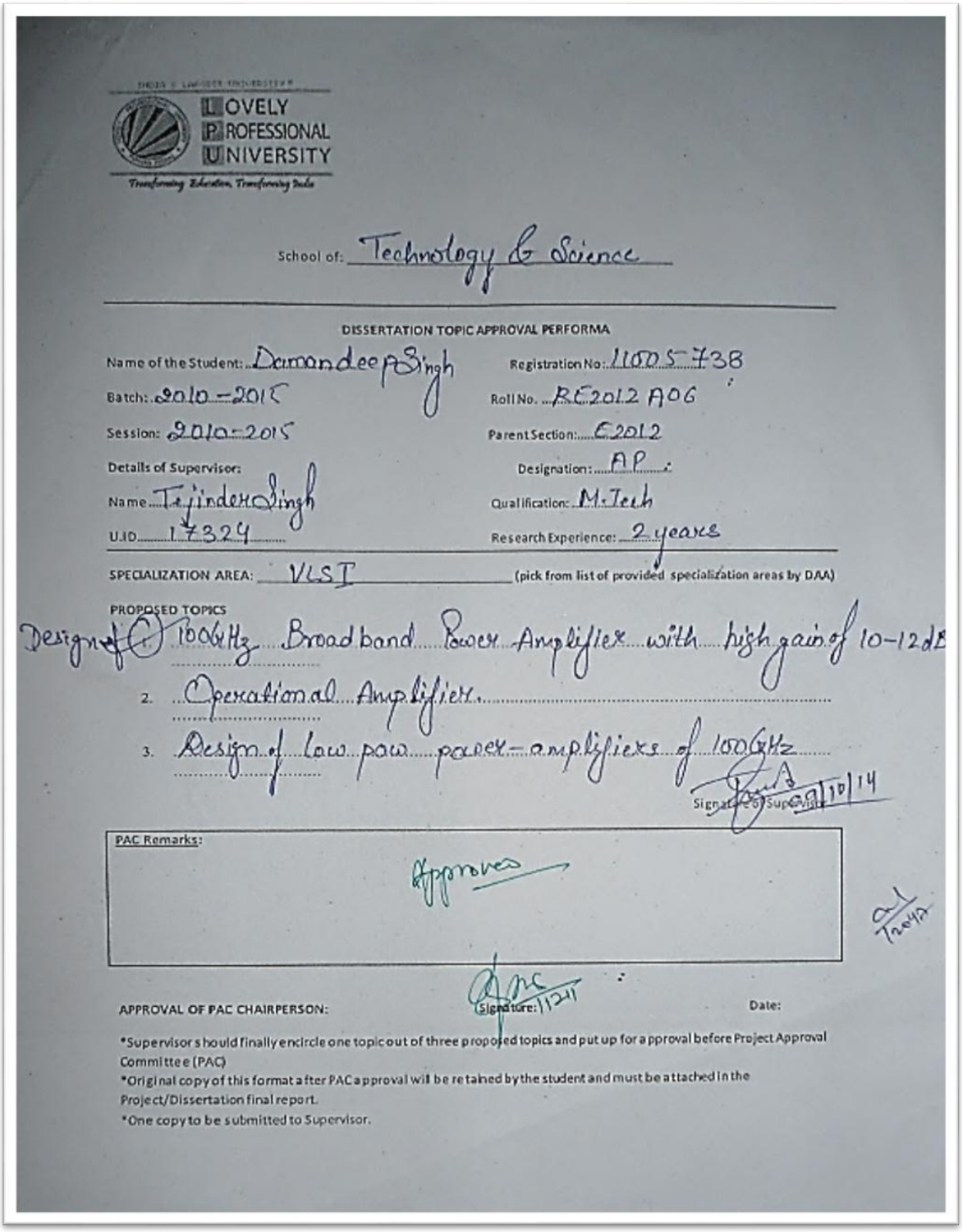
"*I would like to provide gratitude to the **God** and my **Parents** for providing me the opportunity to be work on my thesis and also to our university faculty for helping me to achieve my goal*."

Damandeep Singh
Lovely Professional University

APPROVAL



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DISSERTATION TOPIC APPROVAL PERFORMA

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PROPOSED TOPICS

1. Design of 100GHz Broad band Power Amplifier with high gain of 10-12dB
2. Operational Amplifier.
3. Design of low pass power-amplifiers of 100GHz

Signature of Supervisor: 9/10/14

PAC Remarks: Approved

APPROVAL OF PAC CHAIRPERSON: Signature: 1241 Date:

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ABSTRACT

This study investigate around the study for the implementing of the amplifier, for the award of Master degree in Technology(M.tech) and the literature survey done for the dissertation and knowledge acquired in the time of literature survey and the problem that's found in the papers and technology and deciding the complete narrow topic for the same. This report present the Designing of Power Amplifier in 180, 90 &45nm CMOS Process,

In 180nm: The design reported in this paper is the broadband power amplifier which is designed in 180nm CMOS process technology very efficient to amplify the small signal input sinusoidal resulting gain of 21.3dB. The design proposed consists of three stages having two Cascode stage amplifiers coupled with the single Wilkinson power divider and combiner stage. The noise figure is 3.57dB centered at 30GHz with input and output matching of 50ohms. The reported design has average power dissipation observed to be 163.28mW at 1.8V Vdd and unconditionally stable throughout the broadband frequency band of 100GHz.

In 90nm: Demonstrated a multi-stage power amplifier design in 90nm CMOS technology for the wideband of 13GHz including the WiMAX (802.16e).It proves to be very efficient with maximum gain of 54.38dB at 1V and power dissipation is observed to be 92.14uW at 1V. The minimum noise figure achieved is 5.62dB centered at 4.32GHz. The design is matched at 50ohms with the average S12 value of -51.43dB.The design is unconditionally stable through-out the bandwidth of 13GHz and consume power which is relatively less from other similar designs.

In 45nm: It demonstrate the design of Power Amplifier designed in 45nm CMOS process. The design of PA having the gain of

ACKNOWLEDGEMENT

First of all, I would like to express my gratitude to Mr. **Tejinder Singh** Assistant Professor, Electronics and Communication Engineering Department, Lovely Professional University, Jalandhar for his gracious flawless efforts and forth right suggestions blended with an innate intelligent application have crowned my task with success. I am truly very fortunate to have the opportunity to work with him. I found this guidance to be extremely valuable.

I am also thankful to entire faculty and staff of Electronics and Communication Engineering Department and then friends who contributed directly or indirectly through there constructive criticism in evolution and preparation of this report work.

It is a pleasure to be associated with CADENCE Laboratory of Lovely Professional University (LPU), Phagwara and I would like to thanks the entire lab members.

I am thankful to **Sanjeev Kumar**, Research Scholar (LPU, Phagwara) who is always there at the need of hour and give me suggestion and inspiration in my tough time.

Last but not least I would like to thanks my all friends for their smile and friendship making the life at LPU University, Phagwara enjoyable and memorable. They rendered me enormous support during the whole tenure of my thesis work.

I extend my deepest gratitude to my parents and brother for their love, affection, encouragement and support

CERTIFICATE

This is to certify that **Damandeep Singh** bearing registration number **11005738** respectively has completed Dissertation titled as "**Designing of Power Amplifier in 180, 90 and 45nm CMOS process**" under the guidance and supervision of **Tejinder Singh** with **UID:- 17342**. To the best of my knowledge, the present work is the result of his original investigation and study. No part of the dissertation has ever been submitted for any other degree at any University.

The dissertation is fit for submission and the partial fulfillment of the conditions for the award of degree.

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DECLARATION

I hereby certify that the work, which is being presented in the report, entitled "Designing of Power Amplifier in 180,90 and 45nm CMOS process**"**, in partial fulfilment of the requirement for the award of the Degree of **Master of Technology(VLSI Design)** and submitted to the Department of Electronics and communication Engineering of Lovely Professional University, Punjab, institution is an authentic record of my own work carried out during the period *August-2014* to *May- 2015* under the supervision of **Mr. Tejinder Singh** . I also cited the reference about the text(s)/figure(s)/table(s) from where they have been taken.

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Date: Signature of the Candidate

This is to certify that the above statement made by the candidate is correct to the best of my knowledge.

Date: Signature of the Research Supervisor

ABBREVIATIONS

PA	Power Amplifier
G	Gain
G_P	Power Gain
G_V	Voltage Gain
MOS	Metal Oxide Semiconductor
PAE	Power Added Efficiency
S-Param	Scattering Parameters
P-noise	Phase Noise
THD	Thermal Harmonic Distortion
GD Load	Gate Drain Load
CS Amp	Common Source Amplifier
CD Amp	Common Drain Amplifier
$G_{m\ (n/p)}$	Trans-conductance of NMOS and PMOS
K_f	Stability Factor
NF	Noise Figure / Noise Factor
S11	Scattering parameter from In 1 to Out 1
S12	Scattering Parameter from In 1 to Out 2
S21	Scattering Parameter from In 2 to Out 1

S22	Scattering Parameter from In2 to Out 2
EER	Envelope Elimination and Restoration
WCDMA	Wideband Code Division Multiple Access
WiMAX	Worldwide Interoperability µWave Access
Freq	Frequency
CS	Common Source

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μ	Charge carrier mobility
C_{gs}	Gate Source capacitance
C_{gd}	Gate Drain capacitance
G_m	Trans-conductance
I_d	Drain current
K_p	PMOS trans-conductance parameter
K_n	NMOS trans-conductance parameter
V_{dd}	Positive supply
V_{ss}	Ground supply
V_{sat}	Saturation voltage
V_{th}	Threshold voltage
V_{out}	Output voltage
V_{tho}	Threshold voltage at $V_{sub} = 0$
L	Channel length
W	Channel width
C_{ox}	Oxide Capacitance
F	Frequency
dB	Decibel
dBm	Decibel milliWatt

V_{IN}	Input Voltage
p	Pico(10^{-12})
f	Femto(10^{-15})
η	Efficiency
ohm	Unit of Resistance

Chapter 1 INTRODUCTION

1 INTRODUCTION

An electronic amplifier (amp) is an electrical device that increases the power of a signal. It do it by the help of energy from a Biasing supply voltage and control the o/p to match the applied signal shape but with benefit of larger heft. In this sense, an amp modulates or amplify i/p and provide the high output.

1.1. About the Amplifiers

There are at least four basic types of electric amplifiers namely: The voltage amplifier (for voltage amplification), the current amplifier (for current amplifications), the Trans conductance amplifier, and the Trans resistive amplifier. A further disunion in category is reliant on whether the o/p is a rectilinear or not. Amplifiers can also be divided by their physical placement in the signal blocks.

1.2. Types

There are four types of Amplifier design available and generally used according to the design and requirement of the device. They can also be classified according to the application of the Amplifier:

On the basis of characteristics:

- Power amplifier
- Voltage amplifier
- Current amplifier

On the basis of stages:

- Single stage amplifier
- Dual stage amplifier
- Multi stage amplifier

On the basis of topology:

- Cascade amplifier
- Cascode amplifier
- Folded cascade amplifier
- Common Source amplifier

So, from the above classification it can be seen that there are large variety of amplifier and they can be used according to the need and requirement of the individual.

1.3. Requirement:

While working in the analog (and many digital) circuits there is a need of amplification because the input signal might be very small to drive load of the device, overcome the noise for the subsequently following stages, or to provide high logical levels to digital circuit.

Depending on the type and number of stages, the amplifiers can be analyzed and evaluated for their respective gain.

1.4. Amplifier:

While talking to the Amplifiers, its good explain their usual types and the load which can be implanted on it. Single stage amplifiers are used in virtually every operational amplifiers design. By replacing a passive resistive load with MOS transistor (as Active Load), it also saves the chip area and the power consumption.

A MOS load can produce higher load resistance than the passive device. And result in the higher gain. There are several types of load that can be used namely:

- Gate Drain load
- Gate Source load

1.4.1. Gate Drain Load (GD load):

A GD load is the configuration of MOSFET as the gate and drain of MOS are shorted together by the means of Path. As shown below:

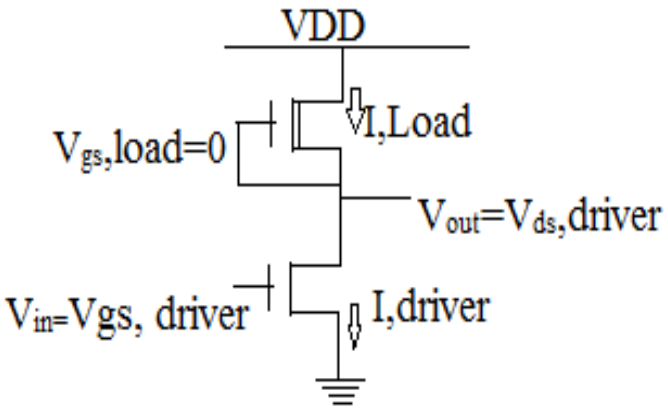


Figure 1.1 Gate Drain Load amplifier

A GD connected MOS can be thought as the resistance of value $1/g_m$. There are four possible configuration of designed that can be generated as amplifier using GD load. As shown in Figure1.1.

1.4.2. Cascade Amplifier:

For increasing the voltage gain (A_V) of the amplifier, an N no of amplifiers are connected in series. The output of first amplifier acts as the input of following stage. This topology represent the overall voltage gain is increased rapidly, when large number of amplifiers steps are used. It can also be referred as the multistage amplifier. The load of the first amplifier is acting as input resistance of the following stage and so on**.** In such a manner each amplifier gain is multiplied by the previous stage amplifier and it is best method to increase the gain of any design but with a drawback of reduction in the stability of design and overall power consumption of the circuit also get increased and more the number of MOS's more will be the parasitic capacitance and more will be load consumption. The example of basic design of such an amplifier is shown in figure 1.2

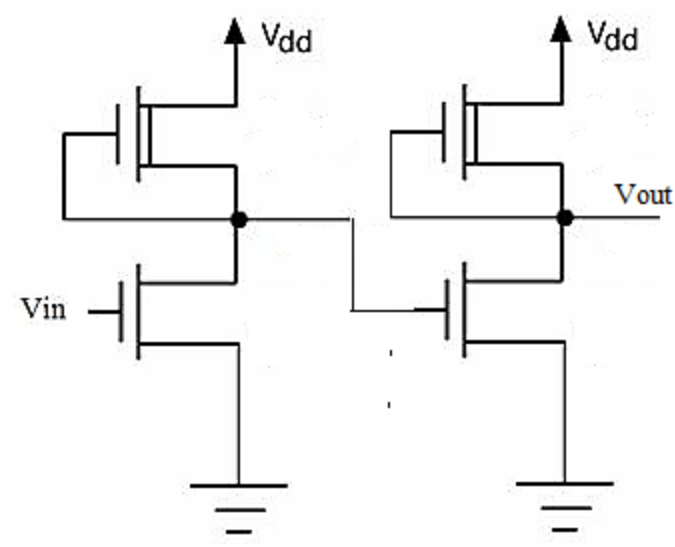


Figure 1.2 Cascade amplifier design

1.4.3. Cascode Amplifier:

The CS amplifier with current source load but implemented using the short channel CMOS process. The Gain of topology is around 16.7. To optimize the gain for the single stage amplifier and to eliminate the noise from design and also to reduce the Miller effect its better to use the Cascode topology of connecting Amplifiers. As Shown in Figure 1.3, resistance into the drain of load MOS is Gmp.r2op with a value up to 16.6MΩ. The gain can be written as the following:

$$V_{out}/V_{in} = (G_{mp}.r^2_{on} \| G_{mp}.r^2_{op})/ G_{mn} = - G_{mn}.R_{oca} \quad (1.1)$$

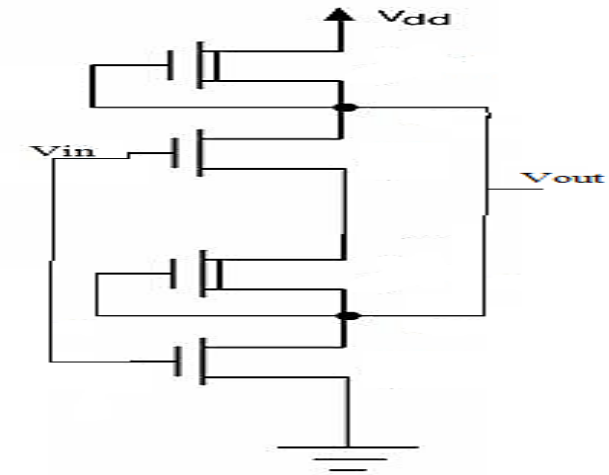


Figure 1.3 Cascode Amplifier Basic Design

1.5. Efficient Power Amplifiers:

The methodology of tailing the designing purpose of RF PA with higher efficiency, is associated with the reason that which type of the modulation schemes of communication systems is employed in application for generating the specification list including bandwidth, frequency of response, and type of input signal and so on. Primarily there are two prevailing sorts of cadence outlines for atypical wireless applications are as follows:

- Constant-envelope modulation and
- Non-constant envelope modulation.

The constant-envelope tone up schemes narrowly accepted by structures such as Globe System for Mobile Communications (GSM) and RF-ID. Linearity necessities of a PA are less stringent with the usage of constant-envelope signals, e.g. GMSK (in GSM). In such circumstances, a non-linear amp with high efficiency can be considered: it sustains the modified information while skillfully exploiting the narrow battery resource. In contrast to a linear PA where output signal amplitude ostensibly to be linearly controlled by the input signal amplitude, a non-linear PA's output signal is well-ordered by the phase and frequency information of its modulated input signal. Having transistors works as on-off switch in switching, class E type Power amplifier is a nonlinear PA capable of achieving high efficiency at RF frequency.

In a class E PA, the current (I_D) and output voltage (Vo_{ut}) waveforms are molded by the parallel plate capacitance or with load network to minimize the overlapping of Noisy signal over information signal, with less power dissipation by transistor and improving the efficiency of an amplifier. For optimal operation the drain voltage decreases to zero and turns to zero slope just as the value of transistor turns on. And thus losses from drain capacitance discharge is avoided as will leads to the theoretical drain efficiency to be exactly to 100%.

Class F PA is added variety of capable non-linear PA for grasping high efficiency. It wants that harmonics in the transistor load circuit to contour the device's drain voltage and current waveforms to be terminated, assuring the situation in which the transistor's current and voltage doesn't become high instantaneously. Academically, the ultimate waveforms of drain

(I_D and V_D) are always considered to be non-parallel Square wave and semi- sinusoid waves individually, achieving 100% efficiency. It is essential to note that extremely non-linear class E or class F power amplifiers are realistic for linear amplification of non-constant envelope modulated signals, with the relief of special modus operandi such as envelope elimination and restoration (EER).

On the other hand, the non-constant envelope modulation smears to rising wireless systems such as wideband CDMA (WCDMA) and WiMAX. The used shaped-pulse modulations (e.g. QAM, QPSK) or multiple carriers (OFDM) allow high data rate but lodge broader range of bandwidth and requires highly linear components, specifically PA to transfer RF signals with time-varying envelope and phase. In such case a linear PA (typically controlled current sources) is required to inferior the inter-modulation and adjacent channel interference of the amplified signals. Regularly it works at back-off for passable linearity. Staying away from its peak I/O power in most of the time. However, litters the supplied DC preference power designed for the maximum output proficiency and roots low PA efficiency.

Table 1.1 Efficiency of Amplifiers

Serial Number	Class	Efficiency (%)
1	A	20-27
2	B	30-38
3	C	29-45
4	D	32-52
5	E	40-63
6	F	72

Chapter 2 SCOPE AND LIMITATION OF STUDY

This study is conducted as we all know that with era of up gradation is in progress everything which is available is redesigned and optimized up to the level of beneficial. This study is based on the advancement of the generation of wireless communication. As it open to all that there is always a limited frequency band available for the communication and the signal transmitted go degraded by the environment or by the obstacles and at the receiver there is a need of amplifier such that it could just not amplifies the Message signal but also remove the Noise from it.

The receiver antenna having the amplifier is specific with the type of signal and operates on or up to the specific frequency. And as per condition the amplifiers always have the limitation of the low frequency range to operate (say about MHz to up to 10/20 GHz). But our studies objective is to increase its range up to the 100GHz.

2.1. Applications:

- With the need of wideband and faster access of data in cellular communication requires the need for the development of power amplifier that amplifier the Base Band signal at Receiver BTS and provide more clear voice call and approximately zero Jitter and other noise also.

- With the advancement in the technology and the Wireless network which have reached to 4.5G communication operate on higher frequency and wider bandwidth in the IEEE 802.X series of wireless network. This can be achieved only we have proper micro scaled designed amplifier in the devices itself.

- As we continue to work on the Power Amplifier in increasing the Bandwidth and Higher frequency signal. That will leads to the no need of using the Carrier Signal for transmission.

- As the Carrier Signal is removed from the transmission of signal for larger distance it also remove the need of high frequency of oscillator to generate the high frequency signal.

As the number of customer are increasing in Telecom industries there is always a need of an amplifier that can prevent the frequency mixing of two signals and provide user the best service.

2.2. Limitations:

- The very first limitation of this design is that of its application is limited for the band width range of 16GHz to 25GHz, for the higher range frequency band its needed to re-designed by using the certain set of topologies.
- The other very first limitation of the design is its power consumption, the design proposed by Jing-Ning Chang consume the power upto the 163.8mW which is much higher and that needed to be reduce to have the better performance and the other parameters to be optimized.
- The PAE of proposed by the design of Jing-Ning Chang is around 14.6% and it can be optimized. By improving the circuit without using the Inductors or with low value inductors or by designing the active inductors and keeping the other parameters to be same.

Chapter 3 Terminology

3.1. Trans-conductance:

The Trans-Conductance is made up of two words called as Transfer and Conductance. Its unit was *mho* and sooner got replaced by the *Siemens* which is its SI unit.

The Trans-Conductance is generally a ratio of the amount of change in Drain current (I_D) to the amount of change in Gate voltage (V_G). Mathematically it can be written as follow:

$$G_M = \Delta I_D / \Delta V_G$$

For the input of Small Signal with an Alternating Current the value of G_m is changed as follows:

$$G_M = I_{OUT} / V_{IN}$$

3.2. Linearity:

It refers to the mathematical relation which can be plotted in X-Y axis coordinate as a straight line. In electronics i/p signal is sinusoid with F freq, the steady formal output of the circuit. Such that the current through a should also be the sinusoid with the F freq.

$$F(ax`+bx``) = aF(x`) + bF(x``)$$

In simple words it can be said that Linearity is a parameter which defines output, gain, phase etc of design doesn't change due to any other parameters like temperature or so on.

3.3. Gain:

Gain is parameter which defines the transfer function of design or circuit which says that the amount of improvement of voltage from input while moving to output. In general, the ratio of output response to the input stimulus applied.

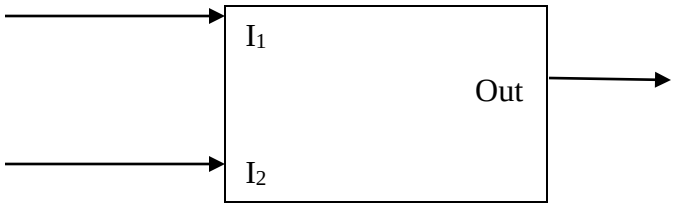
$$G = V_{OUT} / V_{IN}$$

In dB

$$G = 20Log_e(V_{OUT} / V_{IN})$$

3.4. S-Parameters:

The S-Parameters are the values which represent the amount of scattering from the input and out ports of the design. For finding these the design is considered as the black box with gain such that it just pass input to the output terminal.



These are of four types for two port network and increase accordingly.

For two port network:

- S11 Scattering from port 1 to 1
- S12 Scattering from port 1 to 2
- S21 Scattering from port 2 to 1
- S22 Scattering from port 2 to 2

3.5. Stability:

Stability is parameter which defines that amount for which the design doesn't deviates from its properties and acts as ideal design. It's a unit less measurement.

Chapter 4 Background of Amplifiers

4.1. Power Amplifier Operation

A power amplifier's competence is swayed by its group in which it operates, which include class A, B, AB, C, D, E and F. The conventional class A, B, C and AB belongs to the plain category while the other classes like D, E and F occupy with much complicated concepts. The basic PA configuration consists of power transistor, RF choke inductor (L1), and DC blocking interconnect capacitor (C1), output filter network and the load inductance. DC power supply, gate (or base) bias and the input drive are employed to the PA for biasing.

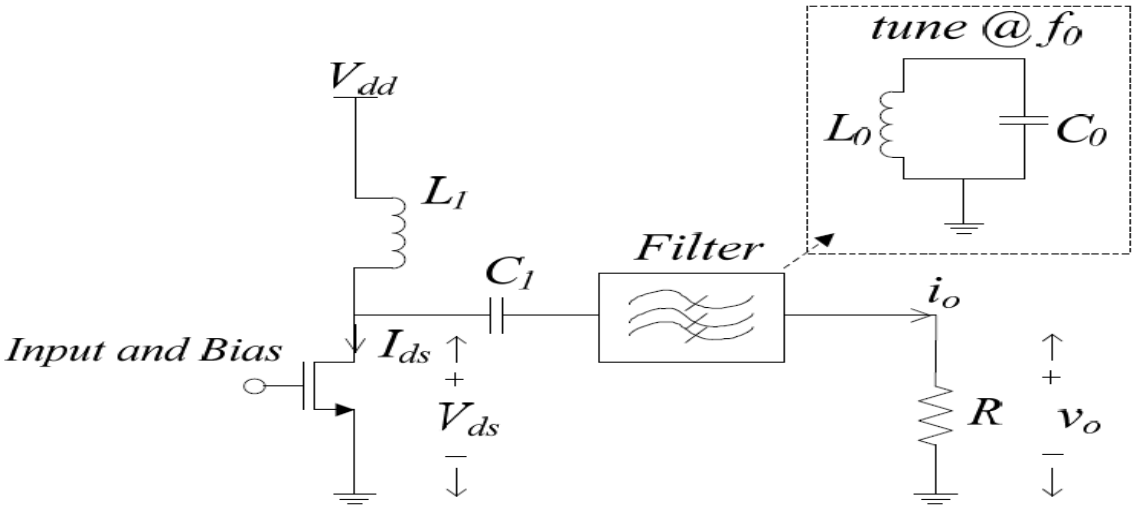


Figure 4.1 Concept of Power Amplifier

The major issue to distinguish class A, B, AB and C is the angle (θ) of transmission of a RF transistor's drain current or collector current in case of BJTs. For class A, the quiescent gate bias is set large enough above threshold voltage, so that the drain current remains greater than zero during any signal period at the PA's working frequency. As can be seen in Fig. 5(a), conduction angle of a class A is 2π. The PA transistor completely operates in the active region and acts as a current source controlled by the input signal drive. The resulting ideal drain voltage and drain current are both sinusoidal, intrinsically with absence of harmonics and considered as "pure linear". Is the major factor to differentiate class A, B, AB and C is the conduction angle (θ) of a RF transistor's drain (or collector) current. For class A, the quiescent gate bias is set large enough above threshold voltage, so that the drain current

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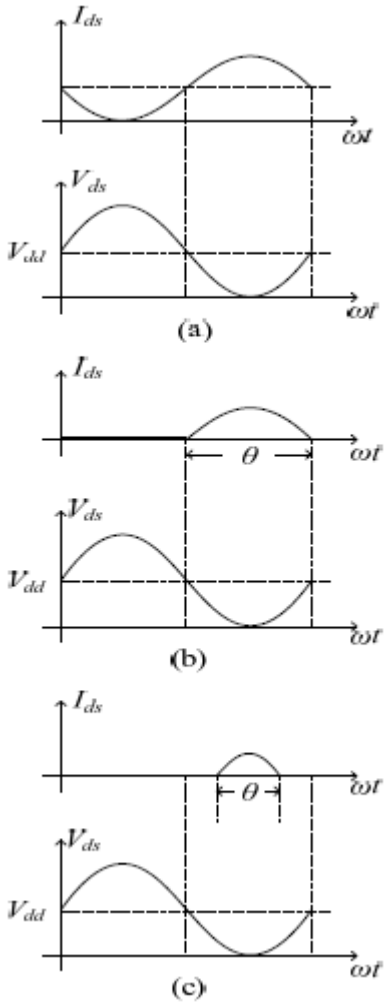


Figure 4.2 Ideal voltage and current waveforms for

(a) Class A (θ= 2π) (b) Class B (θ= π) (c) Class C (0<θ< π)

In general the RF output power is defined by:

$$P_{out} = (V_{om}^2 \ / 2) / R$$

Where $R = V_{om}^2 / 2R$

Where, V_{om} represents the amplitude of drain voltage waveform at fundamental frequency (f_0) and R for load resistance. With full voltage swing, V_{om} is permitted to reach the supply voltage V_{dd} as maximum (knee voltage neglected), which corresponds to the highest output power ($P_{out,max} = 0.5V^2_{dd}/ R$) for class A PA.

The two common DC-to-RF efficiency metrics for class A (and other classes) PA_s are drain efficiency (η) and power added efficiency (PAE):

$$\eta = P_{out} / P_{DC}$$

$$PAE = (P_{out} - P_{in}) / P_{DC}$$

Where P_{in} represent the RF input drive power and P_{DC} for consumed DC supply power. The maximum drain efficiency of an ideal class A PA turns out to be 50%.

Chapter 5 Literature Review

Debasis Dwan et. al [1] designed and fabricated 60 GHz power amplifier with a 20dB small signal gain using 1P7M 90nm CMOS technology. The bandwidth exceeding 57 to 65 GHz is achieved and delivers +8.2dBm output with a linear gain of 20dB with PAE of 90% when operated with 1.5V achieved 22dB small signal gain. A temperature dependent scalable CMOS design is made and made it stable in operation upto the temperature range between -10^{o}C and 80^{o}C. but having the limitation of very high PAE and low output power.

Bevin Perumana et. al [2] 60GHz power amplifier is designed and implemented using the design of 90nm CMOS technology and obtained the Gain of 14.3dB and the saturation power PSAT of +12dBm with the PAE of 8.2% with the power dissipation of 150mW. But having the limitation of high power saturation and relatively lower Gain of the design due to the use of large number of inductors

Jae Jin lee et. al [3] designed a low power single chip CMOS receiver and SOP in the low temperature cofired ceramic (LTCC) is proposed for 60GHz frequency band. It consist of 4stages current re-use LNA, compensating resistive mixer, Ka-band low phase noise,VCO, frequency doubler. Used the 130nm CMOS technology, chip size is (2.67*0.75)mm^2. Power consumption of 210.9mW. But while controlling the operation on the LTCC it resulted with the power dissipation of the design and also the large area of chip.

Sofiane Aoui et. al [4] designed power amplifier from STMicroelectronics for Low cost wireless personal Area network (WPAN). Optimized for delivering the maximum linear output power without using parallel amplification topology. Using 65nm techniques having the chip size (0.48*0.6)mm2. Gain of 8dB, PAE 11% and power consumption 72 at 0.9(mW at V). but have the limitation of low gain of 8dB.

Dajee Zeng et. al [5] designed the power amplifier in 90nm CMOS technology for 60GHz wireless point to point communication using IBM 90nm CMOS. Used the 4stages of design in cascade and got a PAE of 24.3%. at 60GHz in simulation with the gain of 16dB and power consumption of 217mW. But having the limitation of the high PAE and relatively low Gain of amplifier and results in more power consumption as used 4cascade stages of design.

A Siligaris et. al [6] designed the LNA for WPAN application upto the 60GHz frequency in the 65nm CMOS technology. Using two cascaded stages of LNA design and got the Noise figure of 8dB at 60GHz.with a gain of 11dB. But results in the low gain of the amplifier which is the need of amplifier.

Eric Kerherve et. al [7] designed the RF pad transmission lines and balun optimization for 60GHz CMOS power amplifier in 65nm STM CMOS technology and used two stages in cascade with a combined gain of 8.5dB and PAE of 2.3% and power consumption of 9.6 at 1.6(mA at V). but resulted in the low gain of the design upto 8.5dB only and with the limitation of higher power consumption of 183mW.

Jing-Ning Chang et. al [8] designed a 24 GHz PA for direct-conversion transceiver using standard 0.18nm CMOS process. The cascaded three-stage power amplifier comprises two Cascode stages for high gain, followed by a CS stage for high power linearity. To increase the saturated output power (Psat) and PAE, the output stage adopts a Wilkinson-power divider-and combiner-based two-way power dividing and combining architecture. The power amplifier consumes 163.8mW and achieves power gain (S21) of 22.8 dB at 24GHz. The corresponding 3-dB bandwidth of S21 is 4.2GHz, from 22.7 to 26.9 GHz. At 24GHz, the power amplifier achieves Psat of 15.9dBm and maximum PAE of 14.6%, an excellent result for a 24 GHz CMOS power amplifier. In addition, the measured 1-dB compression point is -7dBm at 24 GHz fundamental.

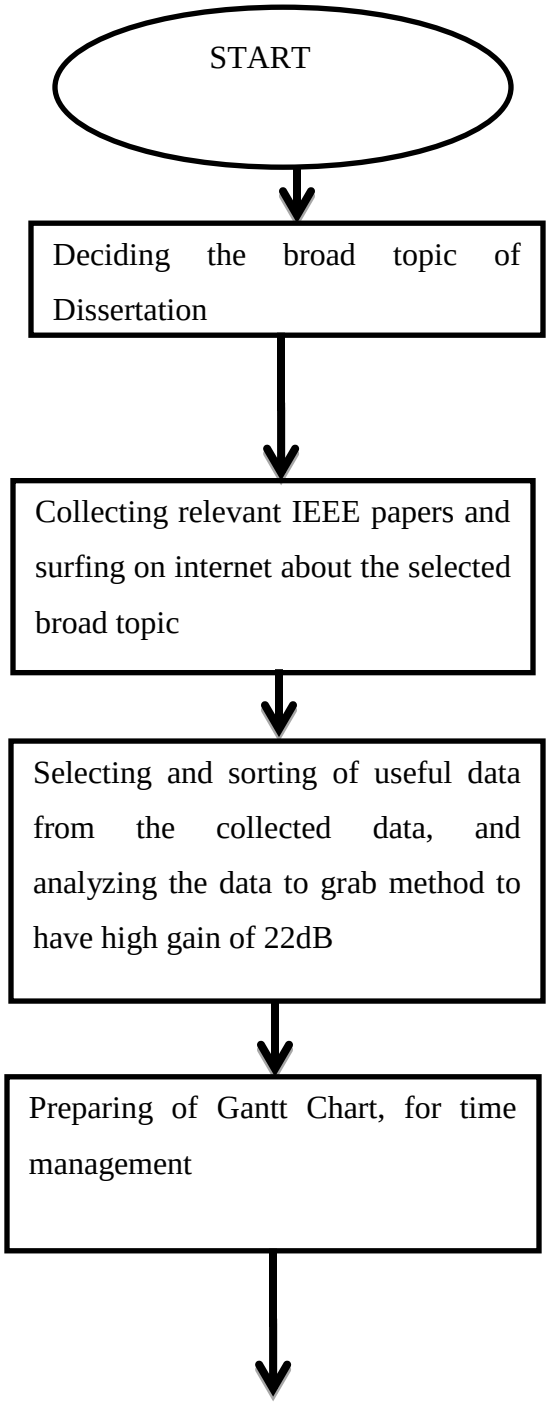
Meng-Ping Chen et .al [9] demonstrated the design of a radio frequency (RF) power amplifier for WiMAX IEEE 802.16e application in 180 nm CMOS technology. A novel two-stage Cascode CS amp and a load-pull output matched power amplifier are designed for the WiMAX application of 2.5GHz transmitting frequency. Proposed power amplifier exhibits 19.8dBm of I-dB compression point, 24.1dBm of output power, 35% power-added-efficiency (PAE), and 23.3dB of G_P at V_{DD} 3.3V and 1.8V supply voltages. The power consumption is about 827.34mW.

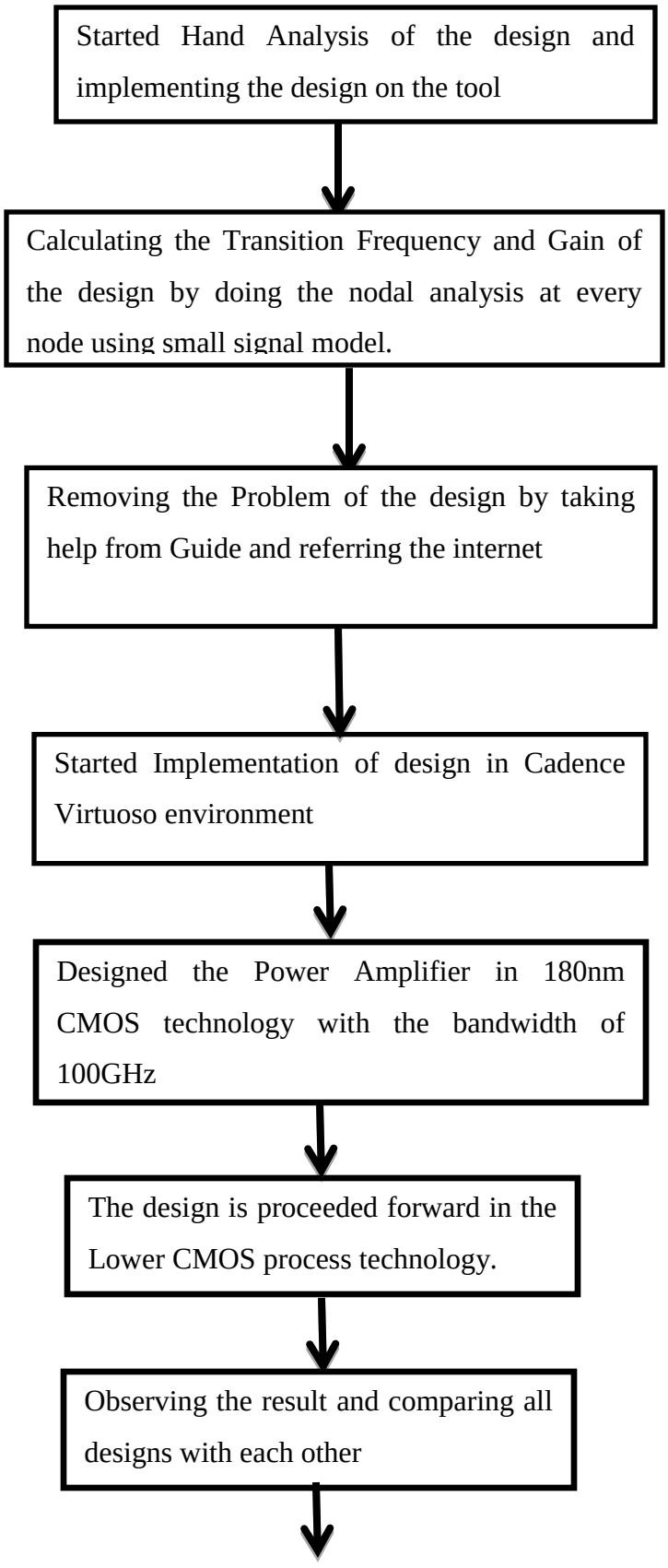
Ofir Degani et .al [10] paper represent a single stage 90nm CMOS PA WiMAX (802.16e) band applications. The design is added with BALUN for matching 50ohm load. The PA gain and saturated power are +18dB and +32dBm, respectively, working from a 3.3V supply, with

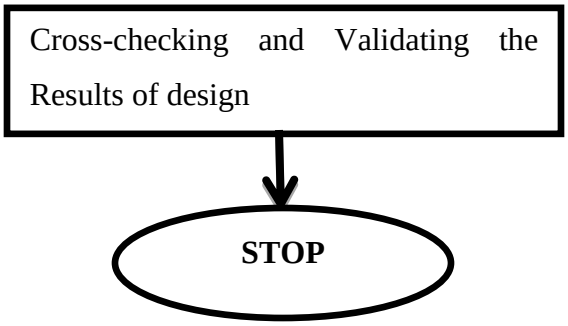
a peak power added efficiency (PAE) of 48%. Digital pre distortion (DPD) technique is used to enhance the PA linearity. The measured EVM for a 64-QAM OFDM signal is improved from -24dB to -30dB at +25dBm output power. Compliance with the FCC 10MHz WiMAX mask is demonstrated at +25dBm of output power with power efficiency of ~25%. Under these conditions, the measured second harmonic level at the PA output is -31[dBm/MHz].

Chapter 6 Research Methodology

6.1. Flow Chart




Started Hand Analysis of the design and implementing the design on the tool
Calculating the Transition Frequency and Gain of the design by doing the nodal analysis at every node using small signal model.
Removing the Problem of the design by taking help from Guide and referring the internet
Started Implementation of design in Cadence Virtuoso environment
Designed the Power Amplifier in 180nm CMOS technology with the bandwidth of 100GHz
The design is proceeded forward in the Lower CMOS process technology.
Observing the result and comparing all designs with each other



6.2. Analysis Equations:

While making Analysis i have used the following equation for the mentioned task, as using 180nm technology they might not work for above or lower technology series.

6.2.1. Square Law Equation:

The drain current passing through MOS is correlated by the Gate-Source Voltage (VGS) in the form of equation:

$$I_D = (K_{Pn} / 2).(W \setminus L)(V_{GS} - V_{TH})^2 (1 + \lambda(V_{DS} - V_{DS_{SAt}})$$

6.2.2. Threshold and Body effect:

For an NMOS devices the threshold of it increases with a increase in the potential at the source with lower body potential. This change of threshold is called as the Body Effect of NMOS: [10]

$$V_{THN}(V_{SB}) = V_{THN0} + \xi_n(2|V_{FP}| + V_{SB})1 \setminus 2 - (2|V_{FP}|)1 \setminus 2)$$

6.2.3. Parasitic Capacitances and Resistances:

The source to drain parasitic resistance can be expressed as the following relation as:[11]

$$\frac{N_{RS}}{N_{RD}} = l/w$$

6.2.4. Saturation area:

For the MOS to work in saturation region there are some conditions need to be followed and given as below: [12]

$$V_{GS} > V_{DS},$$
$$V_{DS} > V_{GS} - V_{TH}$$

6.2.5. Speed:

For higher the its necessary to increase the Overdrive Voltage (VOV). But it reduce the swing of the device. The transition frequency (ft) can be written as follow: [11]

$$F_r = \frac{g_m}{2\pi C_{gs}}$$

Chapter 7 Our Expected Product

While implementing the design proposed by Jing-Ning Chang it's been observed that this design lacks in the same qualities which can be achieved with the help of some techniques in the same design. The parameters are listed as below:

1: The frequency band of the design is low and our expectations is to achieve the frequency band up to 100GHz.

2: The PAE of a design is 14.6% and our expectation is to reduce it and limit it up to 10%.

3: The Gain of the design can be improved with higher frequency band.

4: The power consumption is the most important factor and proposed design consumes the power of 163.8mW and it can be reduced up to 100mW.

Table 7.1 Target to obtain

Design	Frequency band (GHz)	P_{SAT} (dBm)	Gain (dB)	Max PAE (%)	DC power (mW)	CMOS technology (nm)
This design	22-29	15.9	23	14.6	163.8	180
Achieved Results	18-25	16.9	22.13	---	67.4	180
Desired Result	Up to 100	--------	20	<14	<100	180

7.1. Observed Output

Our Objective was to design the Power Amplifier which would be capable for amplification of the input sinusoidal signal of the order of values of mVolts. And applicable for the large bandwidth.

7.1.1. In 180nm:

The aspect ratio is being modified and the additional circuitry is added as shown in next chapter. The aspect ratio values are:

Table 7.2: Aspect Ratio for 180nm

MOS	Value
M1	8.8
M2	7.9
M3	10.8
M4	9.4
M5, M6	8.6

7.1.2. In 90nm:

The aspect ratio is being modified and the additional circuitry is added as shown in next chapter. The aspect ratio values are:

Table 7.3: Aspect Value of 90nm

MOS	Value
M1	29.38
M2	29.38
M3	37.76
M4	29.8
M5	14.92
M6	19.8

7.1.3. In 45nm:

While pursuing with in 45nm technology there are number of parameters like first deciding the what kind a topology is to be employed and pursued with the same method but changing

the aspect value of the each MOS separately using finger method. The net value of W/L is shown in the following table.

Table 7.4: Aspect Value for 45nm CMOS

MOS	Value(W/L)
M1	39u/45n
M2	51u/45n
M3	51u/45n
M4	51u/45n

Chapter 8 Results & discussions

8.1. Base Design in180nm:

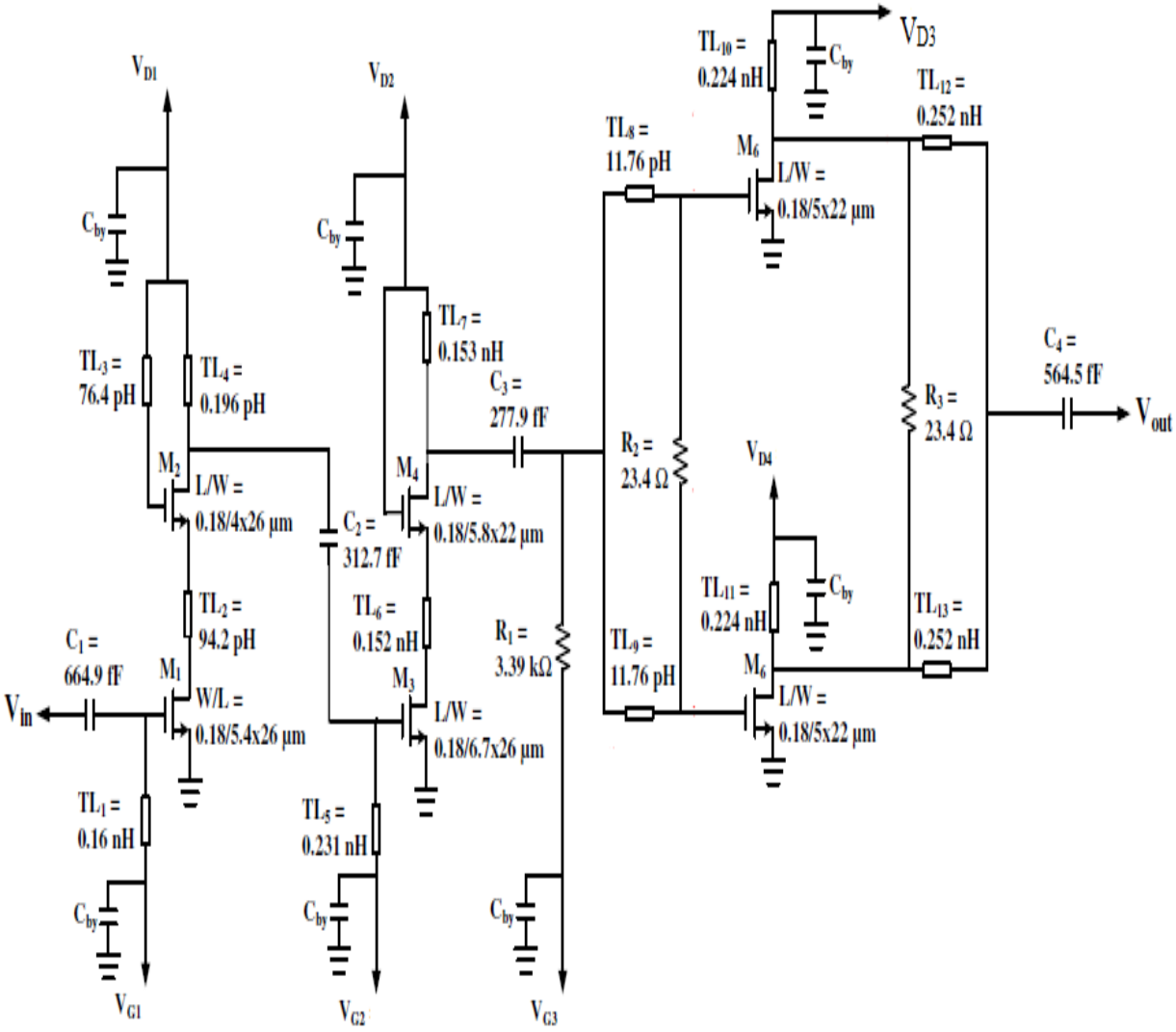


Figure 8.1 Schematic of design

8.2. New Designs:

8.2.1. Modified Design:

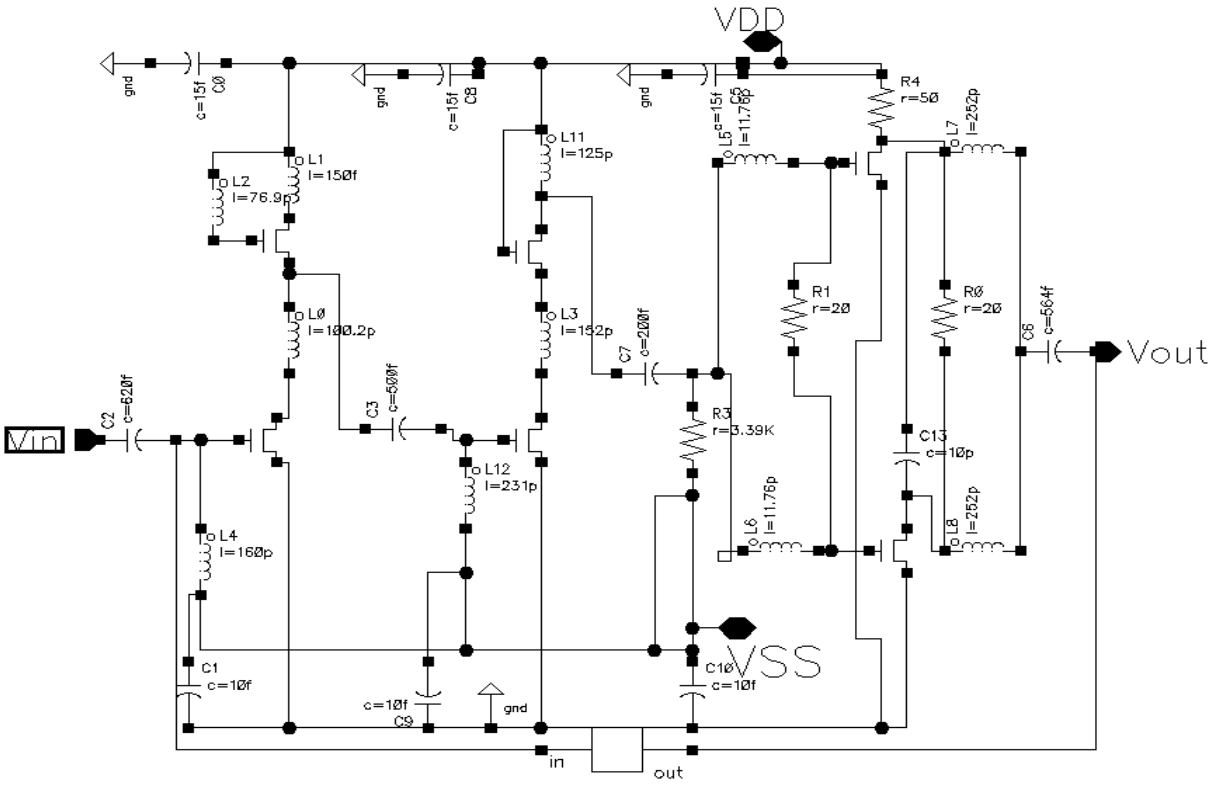


Figure 8.2 Modifier Design of Power Amplifier in 180nm

8.3. Hand Calculations:

First of all to proceed with the calculation. It's better to find the value of by-pass Capacitance (C_{by}) , as it acts as a tuned circuit to pass only the desired signal and block all the feedback capacitances.

F= 25GHz

L= 0.196pH

From the relation

$$F = 1/2\pi\sqrt{(LC)}$$

We get the,

C= 1pf

The total current (ID1) is equal to the 9.21mA.and the VD1 = 3V

Similarly the (ID2) is equal to 18.9mA and VD2=3V

The first Cascode structure of the Amplifier will transform as shown below in figure 6.3.

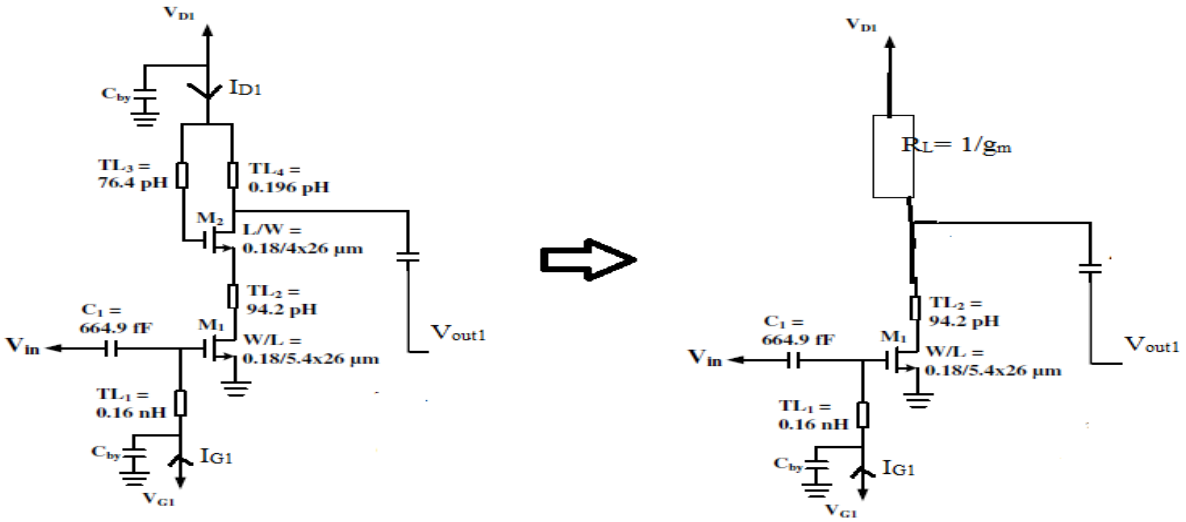


Figure 8.3 Node 1 of amplifier

Now, creating the small signal model of the transformed structure and calculated the Gain for the same. The small signal model of the design

Using the unity gain frequency relation [11]

$$ft = gm/(2\pi Cgd)$$

The value of the Cgd= 0.3 * 10-9 F/m and the FT=25GHz

So, value of gm = 157 F.

And the input is kept at 0.1V the Vout1 is observed to be amplifier by the gain value of 18 and the Vout1= 1.521V which is amplified using the VG1=0.7V and the IG1= 1.76mA.

Vth= 0.695

$$ft = gm/(2\pi Cgd)$$

Proceeding with the node 2, it is reduced to the following structure as shown in figure 6.4:

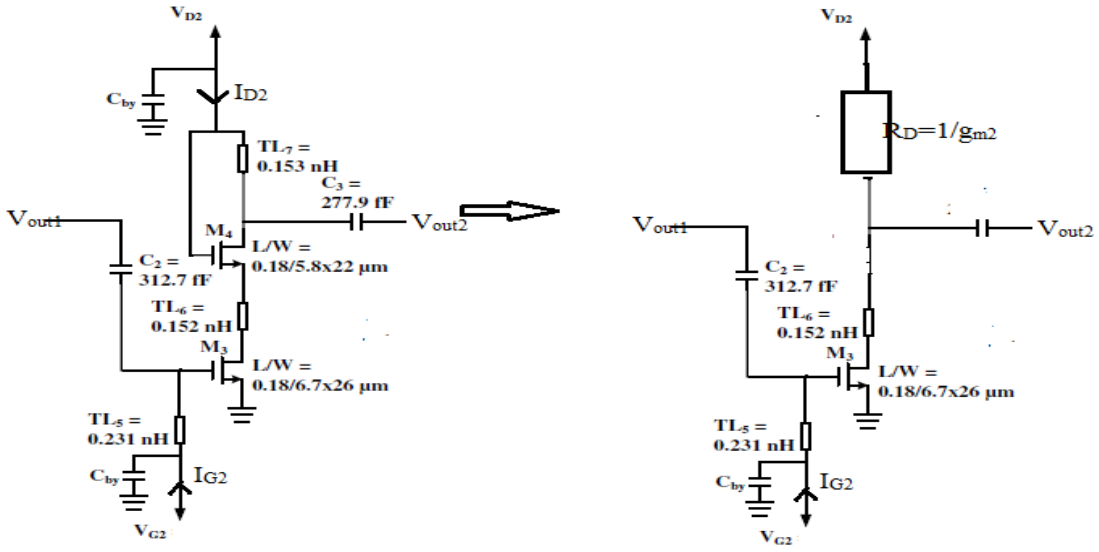


Figure 8.4 Node 2 transformed design

Output Vout1 of first design will act as the input to the design and the value of gm can be calculated by the following relation:

$$ft = gm/(2\pi Cgd)$$

And Cgd=0.4 * 10-9 and

gm= 157 F and the load resistance (RD) is found to be as the following

$$Rd = 1/gm$$

And the VG2= 0.8V and IG1= 1.82mA across the inductor TL5.

The effect of the base of the transistors is assumed to be grounded.

And the Vout2= 10.76V

VTH= 0.654V.

Proceeding circuit is the Wilkinson Power Divider and Combiner circuit made to reduce the effect of thermal noise and it also provide the Amplification of small amount and the final output is found to be equal to the [12]

Vout= 12.89V

The need for the Wilkinson design is to provide security from the feedback current of the device. As the amplifier is connected between the two high voltage operation device, there is always an effect of reverse current and in that case the Wilkinson provide security to not only the device but also to the Antenna from getting damage and further secure the Information data from getting loss.

8.4. Software Design:

8.4.1. Schematic for 180nm:

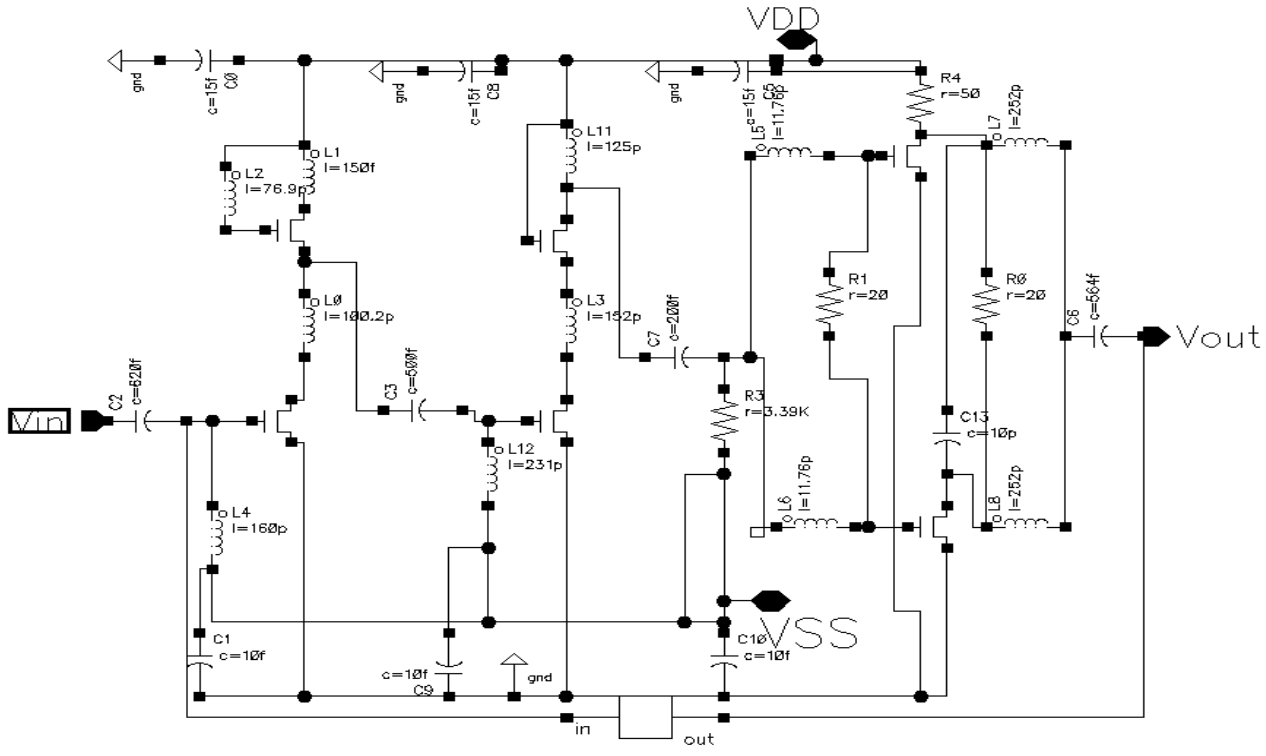


Figure 8.5 Implemented Design for 180nm

8.4.2. Output result:

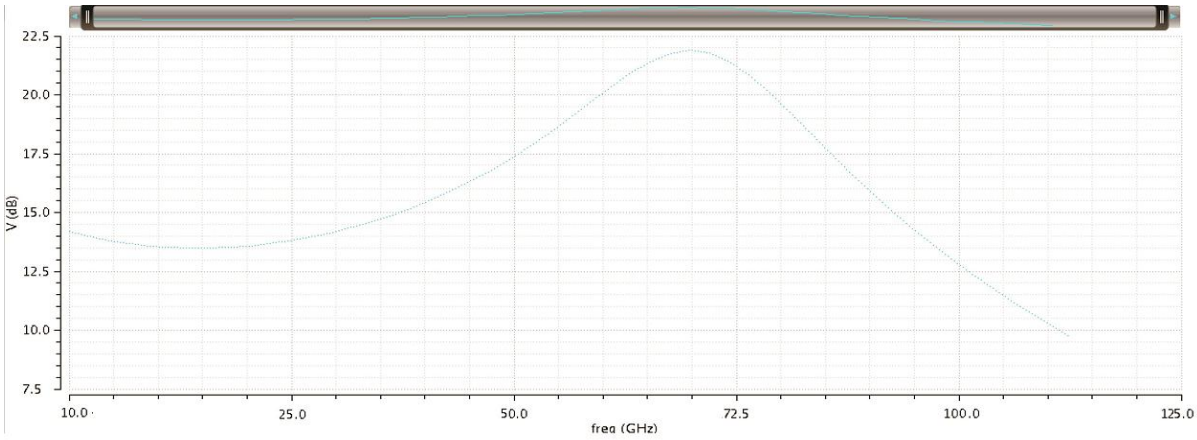


Figure 8.6 Gain for Power Amplifier in 180nm

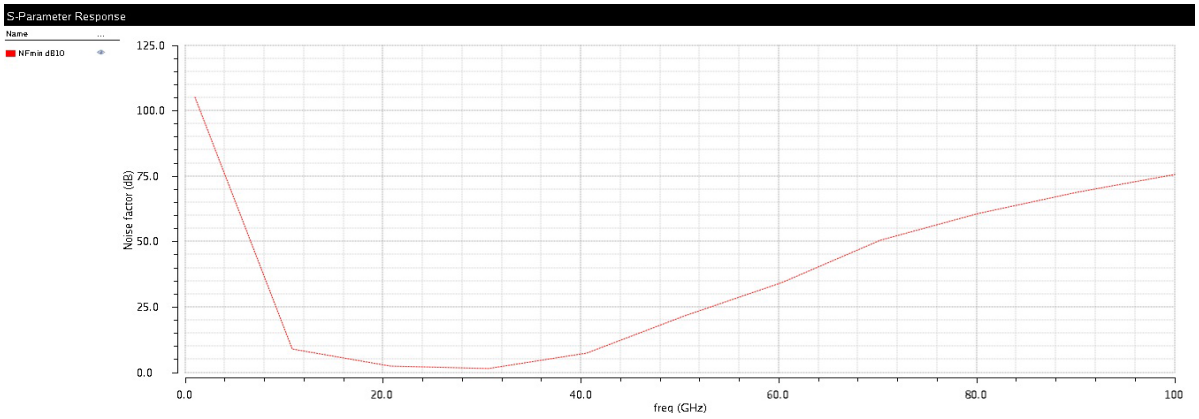


Figure 8.7 Noise Figure of PA in 180nm

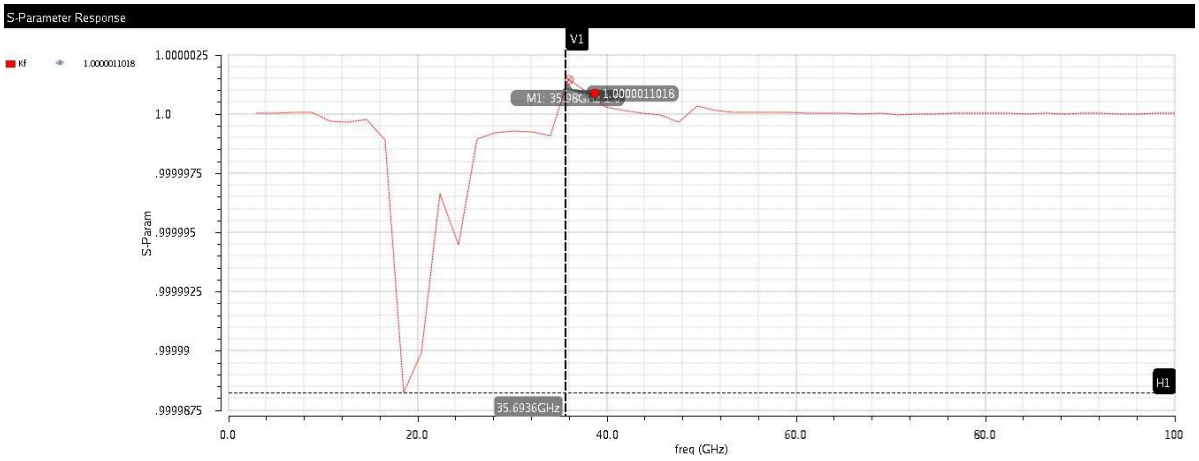


Figure 8.8 Stability Plot for 180nm PA

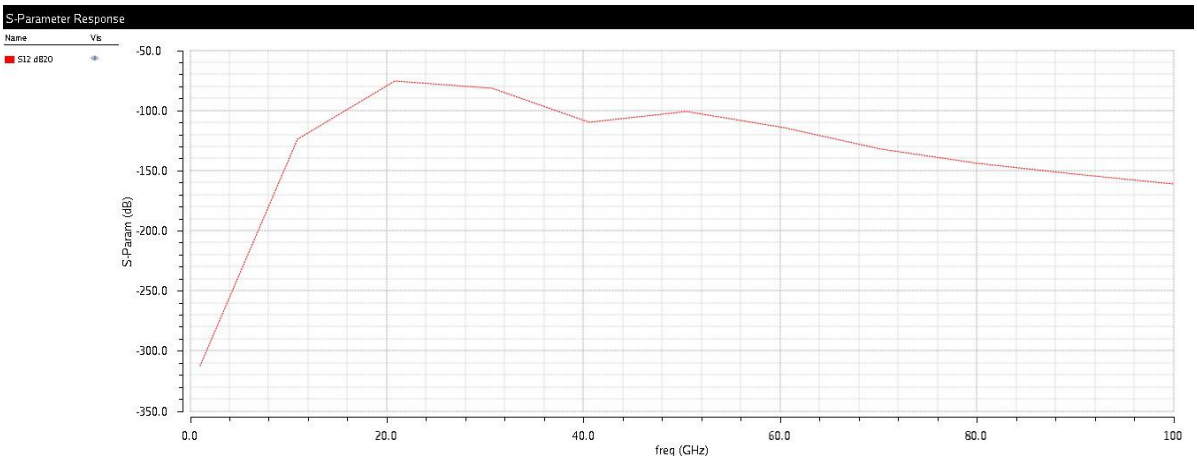


Figure 8.9 S12 Plot in 180nm PA

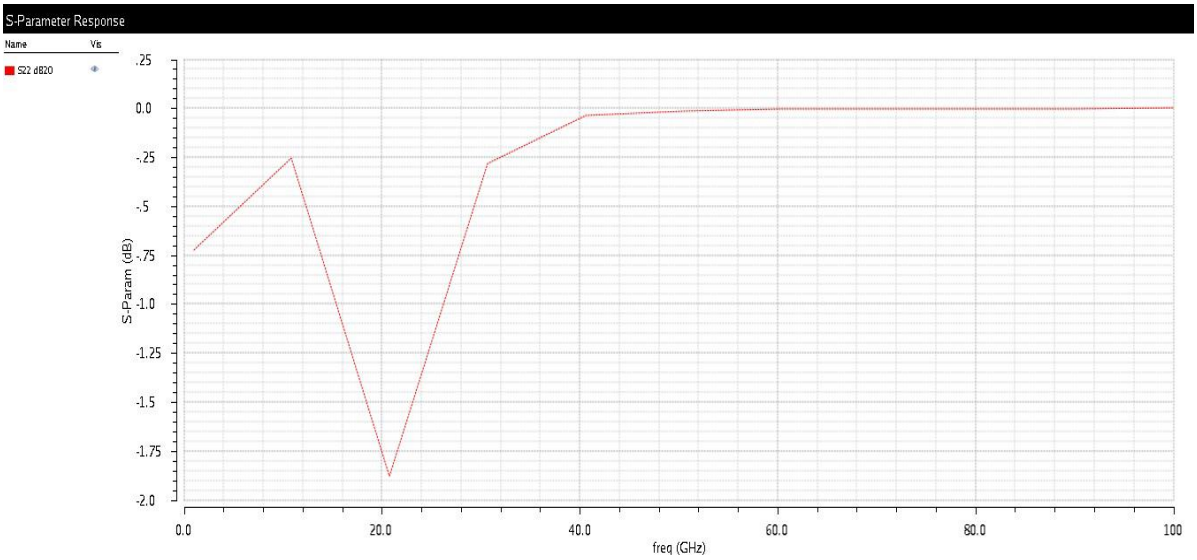


Figure 8.10 S22 Plot for 180nm PA

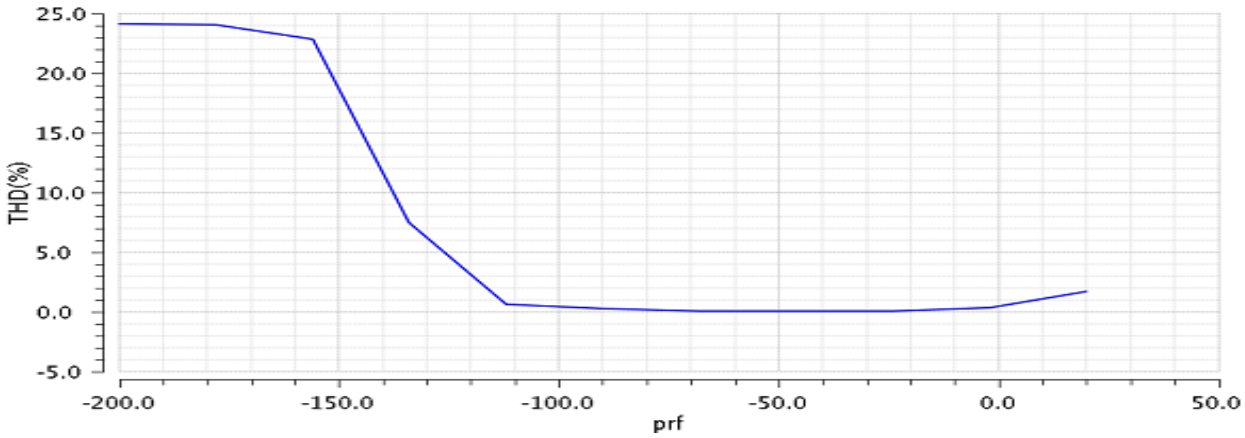


Figure 8.11 THD of PA for 180nm CMOS

8.4.3. Schematic for 90nm CMOS process:

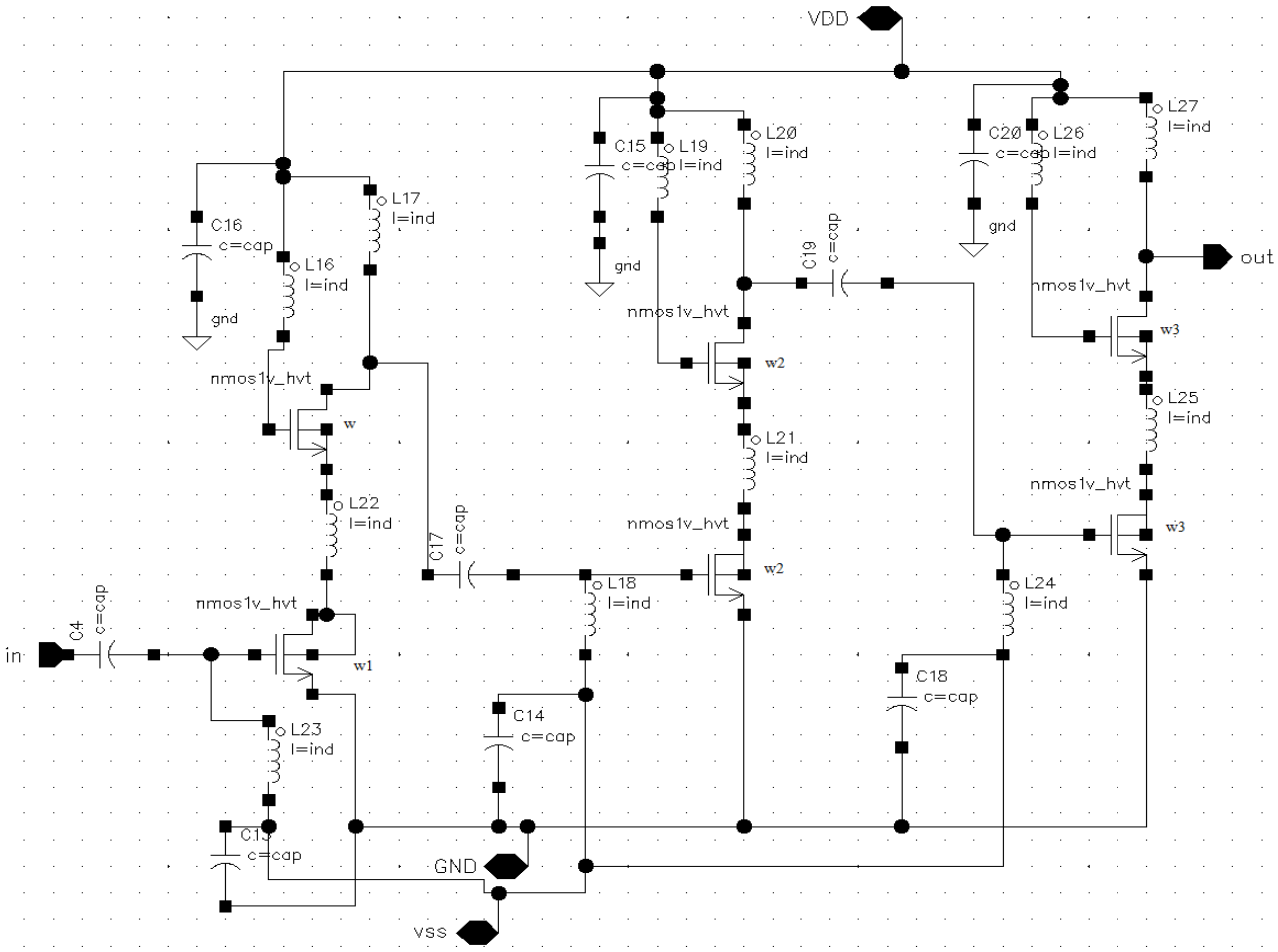


Figure 8.12 Design of Power Amplifier In 90nm CMOS

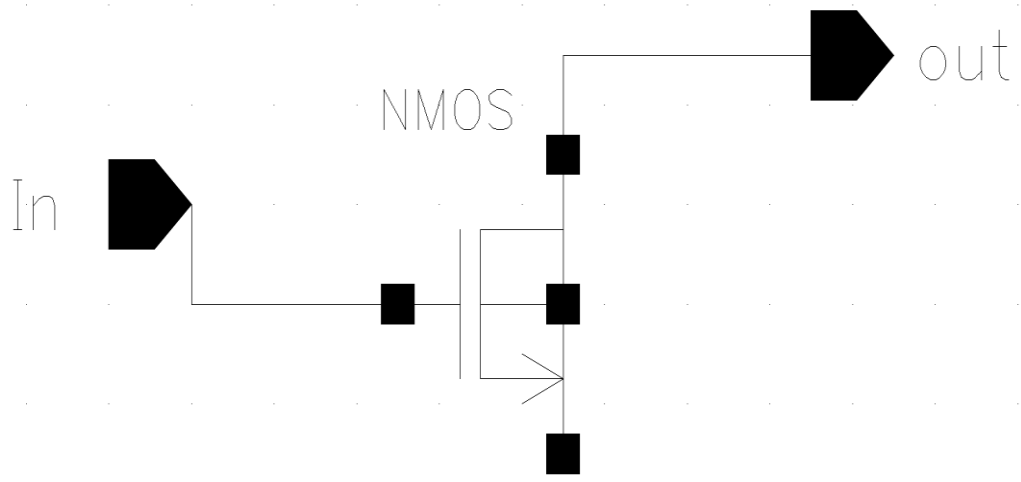


Figure 8.13 VSS for Power Amplifier in 90nm CMOS

8.4.4. Result and Analysis for 90nm CMOS Power Amplifier

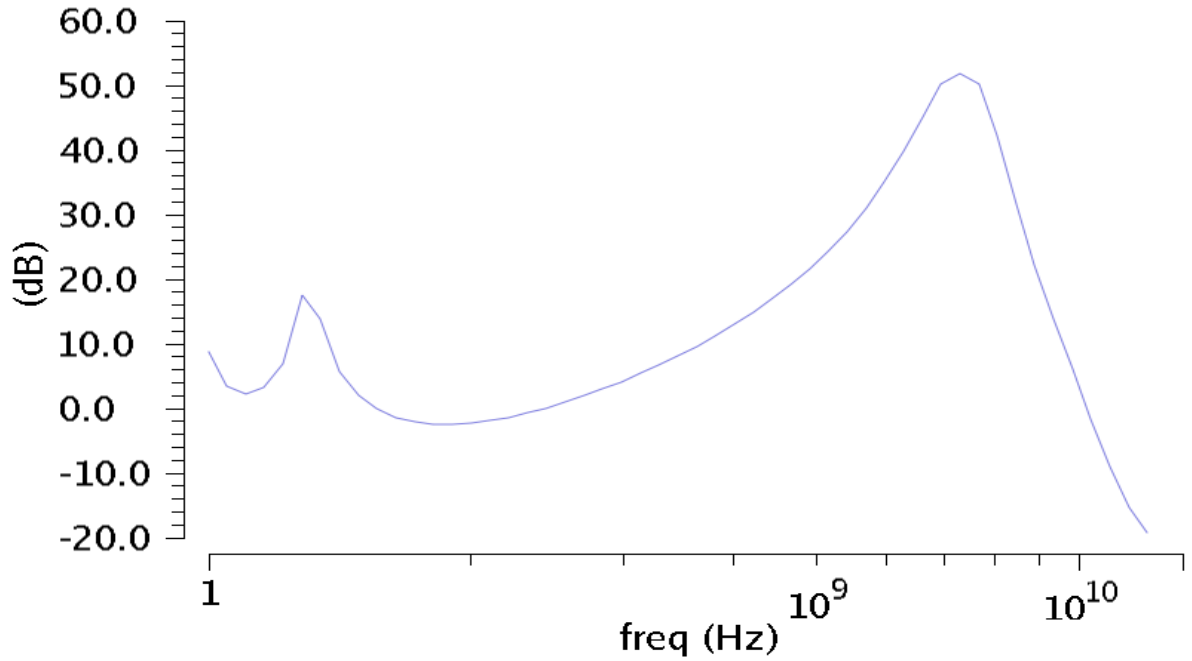


Figure 8.14 Gain of PA in 90nm CMOS

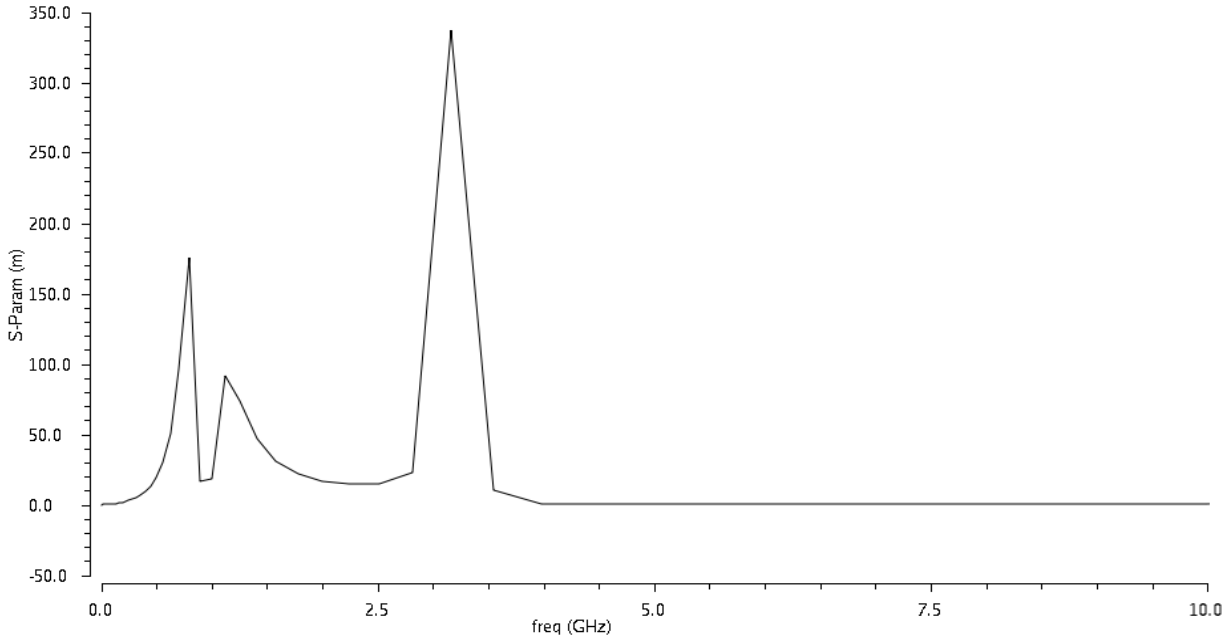


Figure 8.15 Power Gain of PA for 90nm CMOS

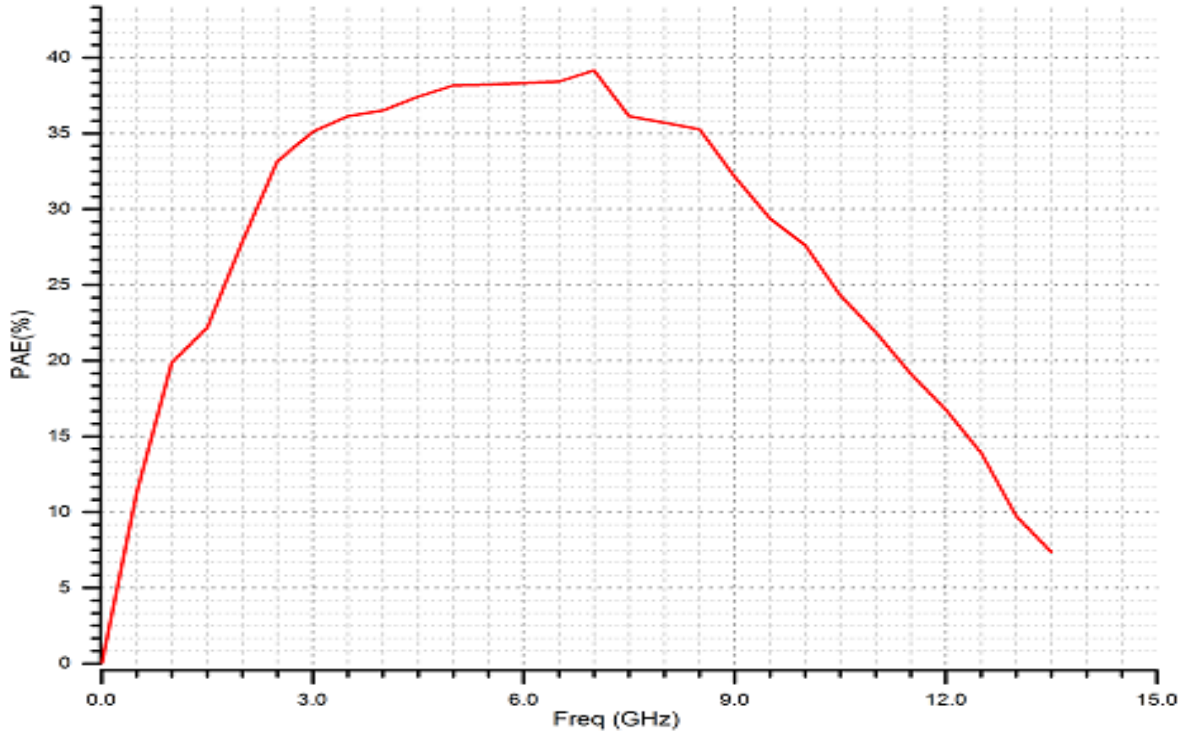


Figure 8.16 PAE plot of PA in 90nm CMOS

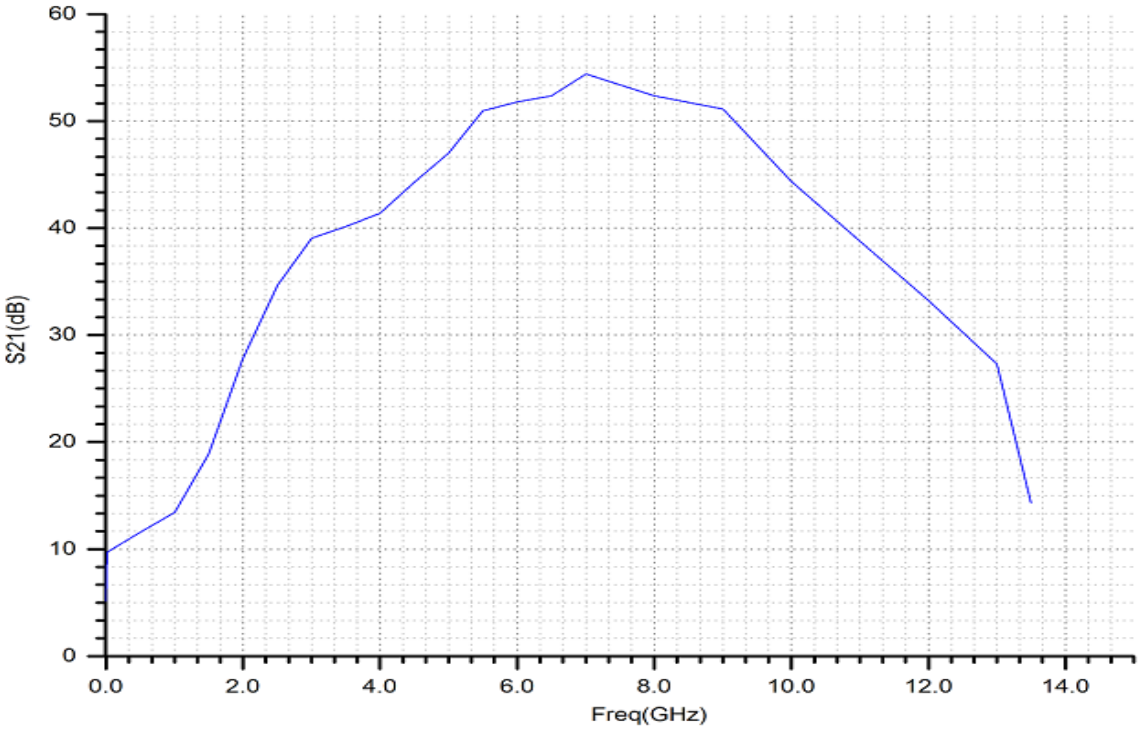


Figure 8.17 S21 plot of PA in 90nm CMOS

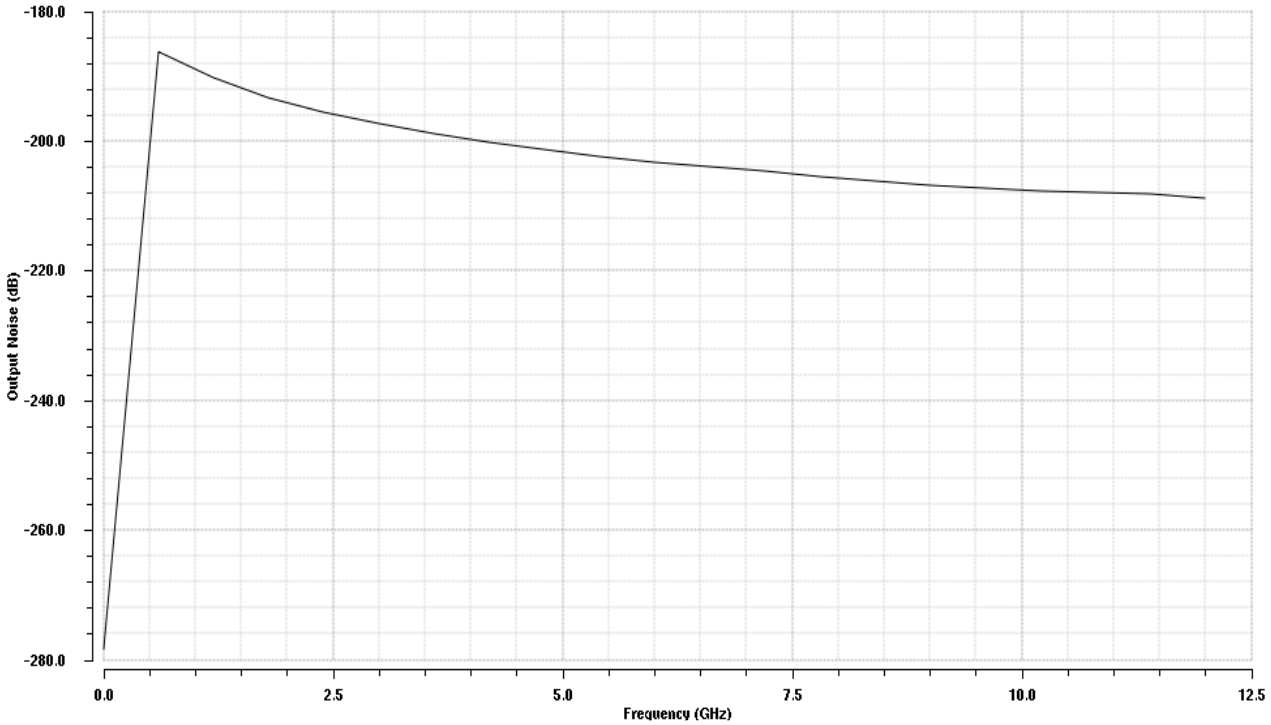


Figure 8.18 Output Noise plot for PA 90nm

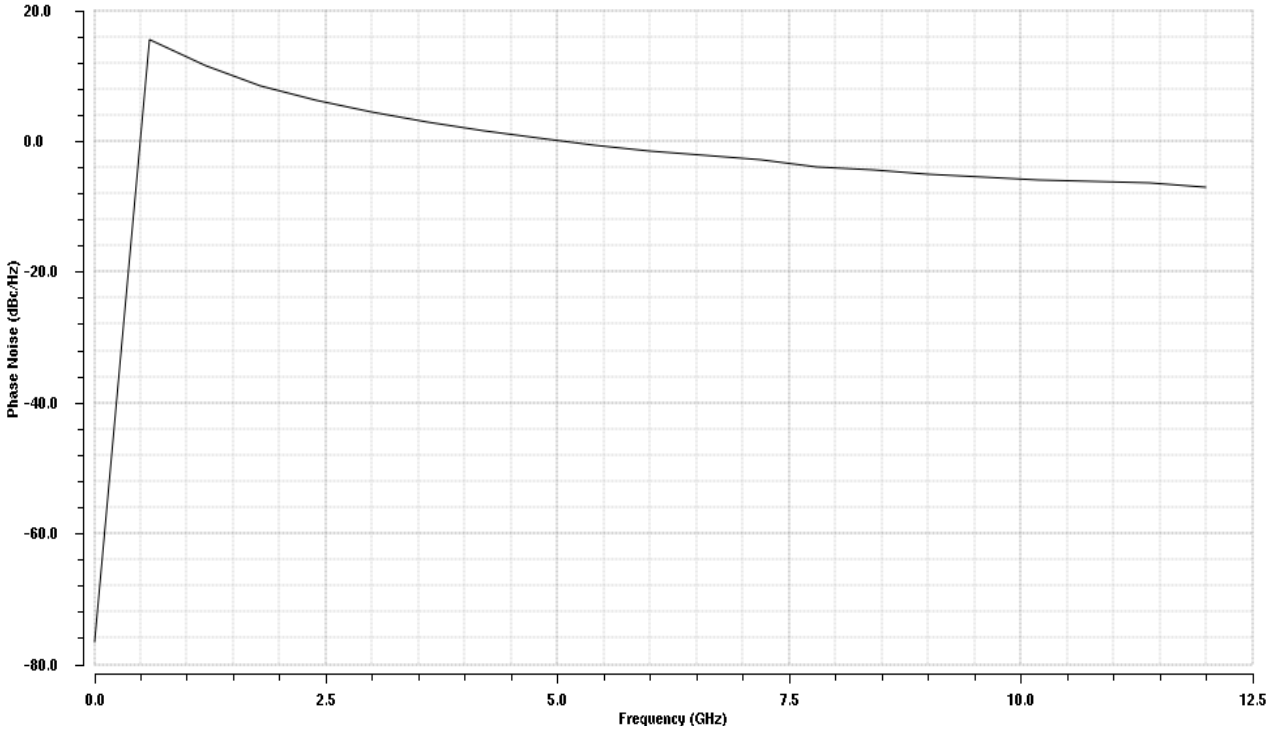


Figure 8.19 Phase Noise in 90nm CMOS process

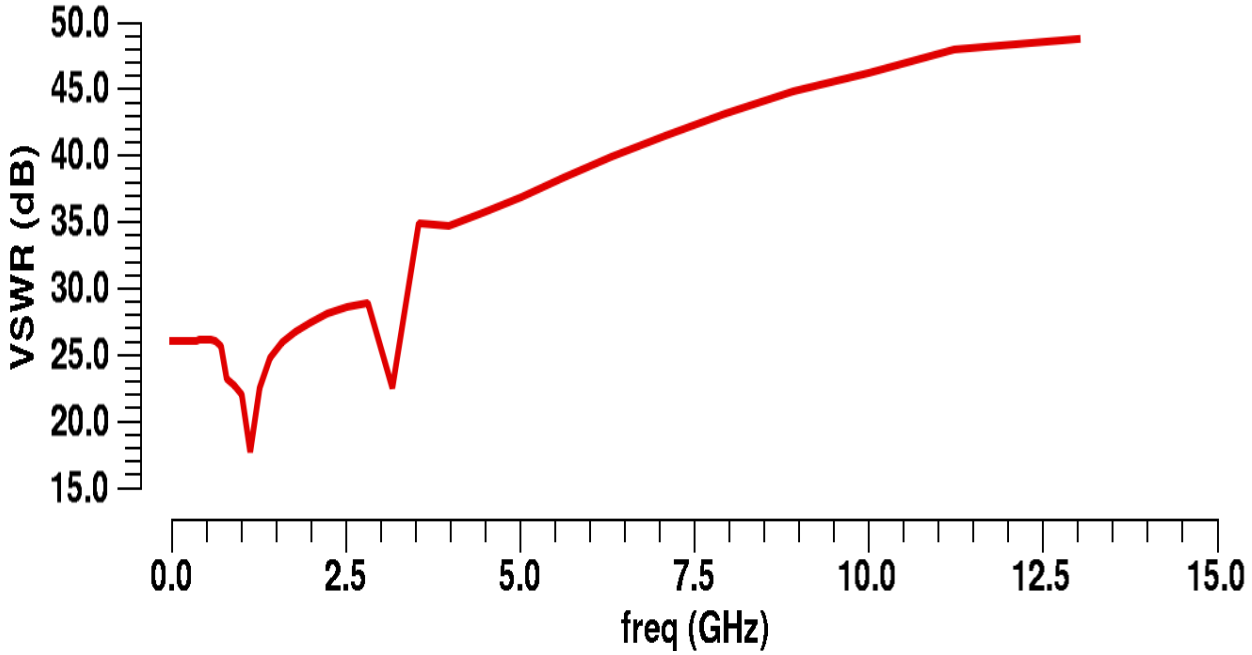


Figure 8.20 VSWR for PA in 90nm CMOS

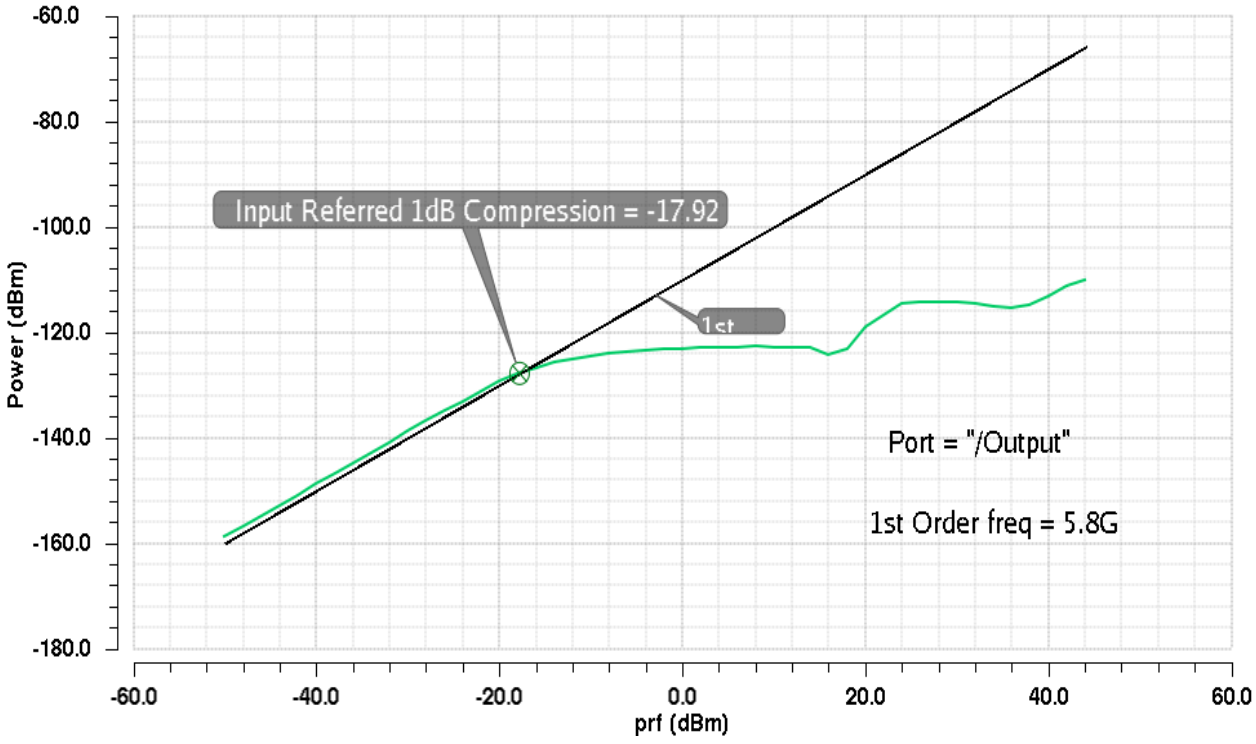


Figure 8.21 1dB compression Point in 90nm CMOS

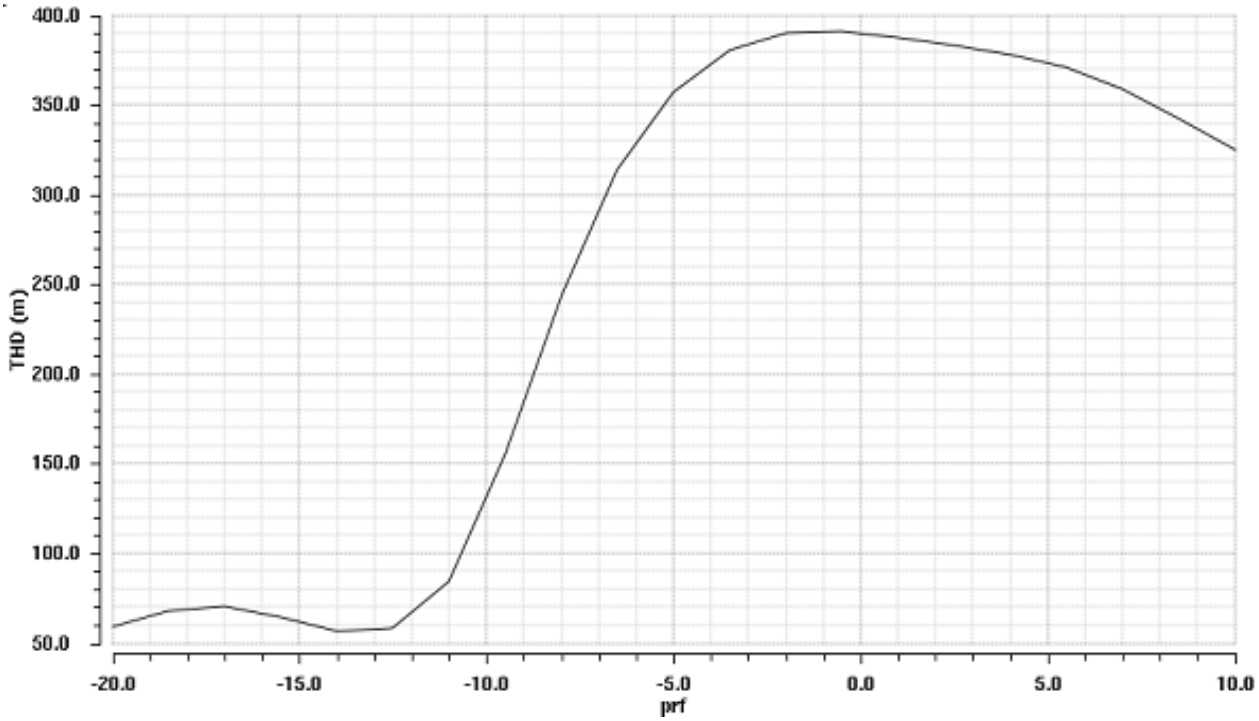


Figure 8.22 THD plot for PA 90nm CMOS

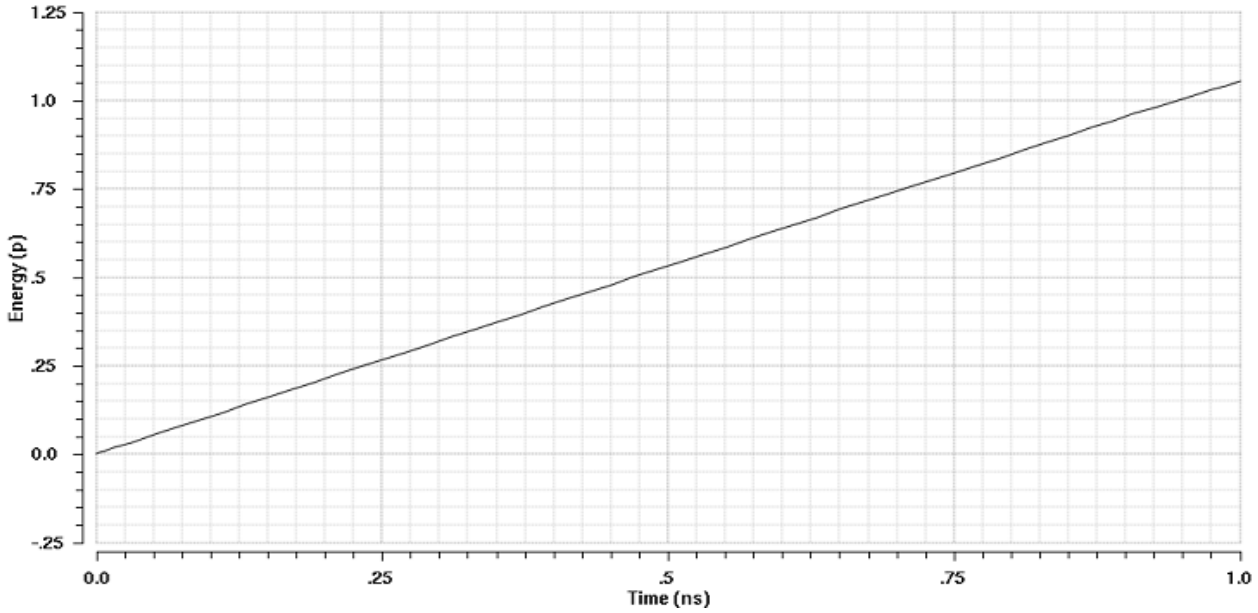


Figure 8.23 Energy Consumed by PA in 90nm

8.4.5. Schematic for 45nm CMOS process:

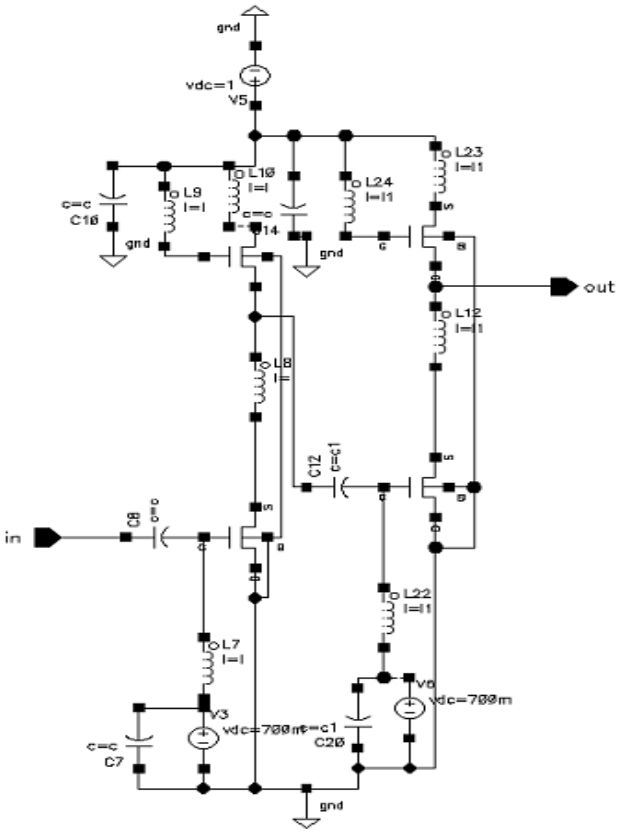


Figure 8.24 Design of Power Amplifier in 45nm

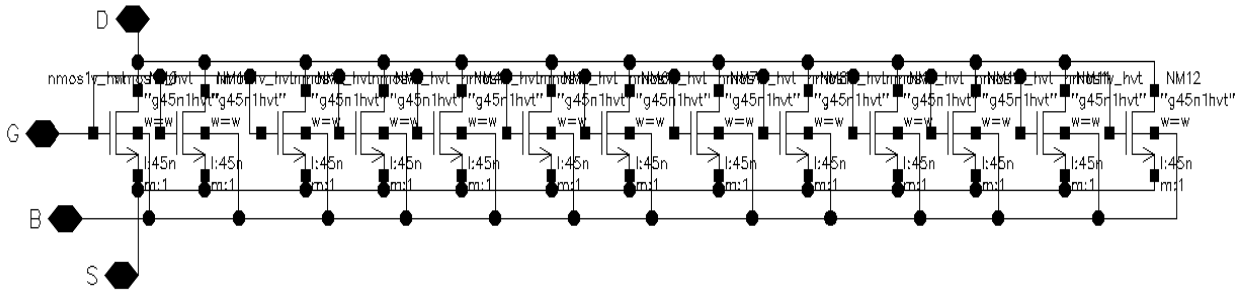


Figure 8.25 NMOS1

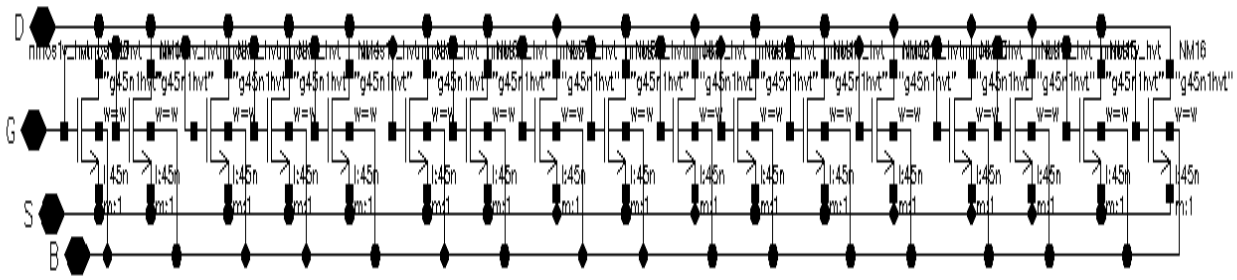


Figure 8.26 NMOS2

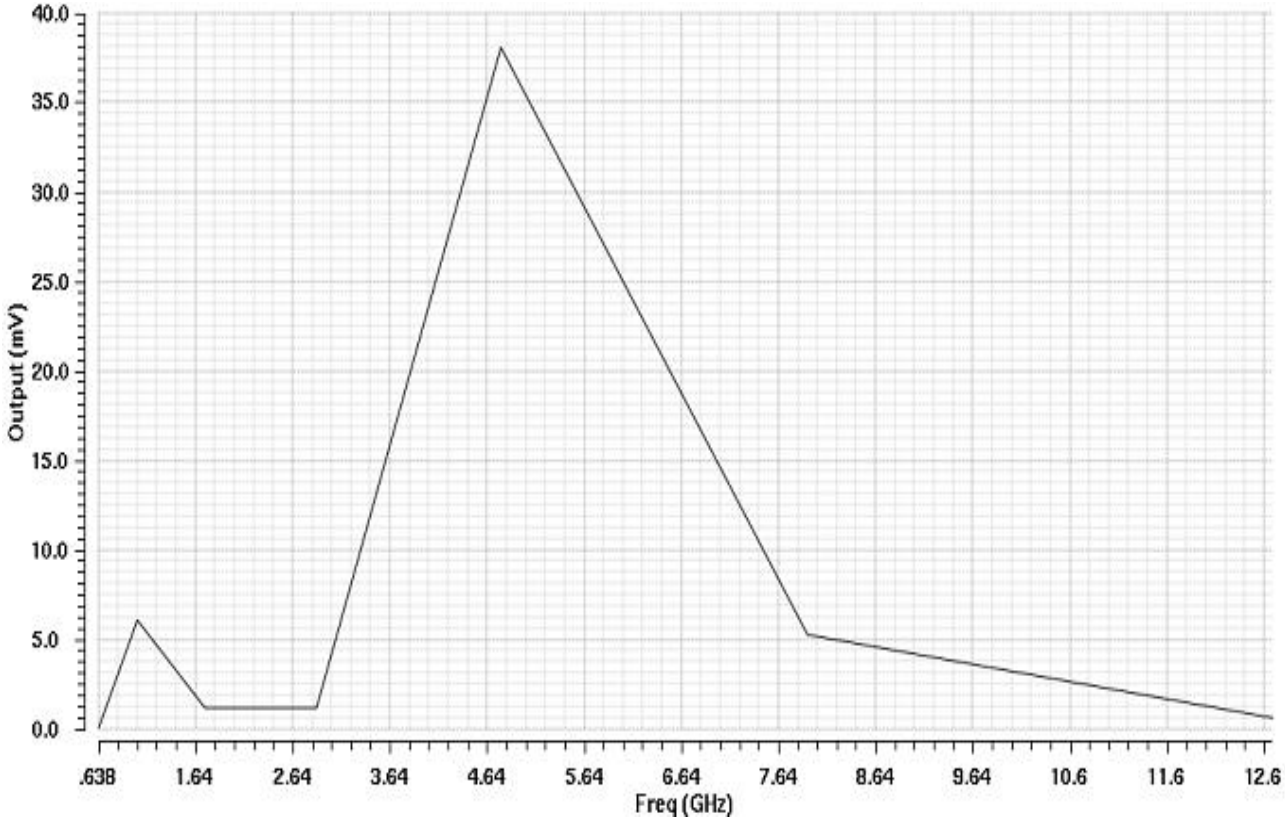


Figure 8.27 Gain Plot of PA in 45nm

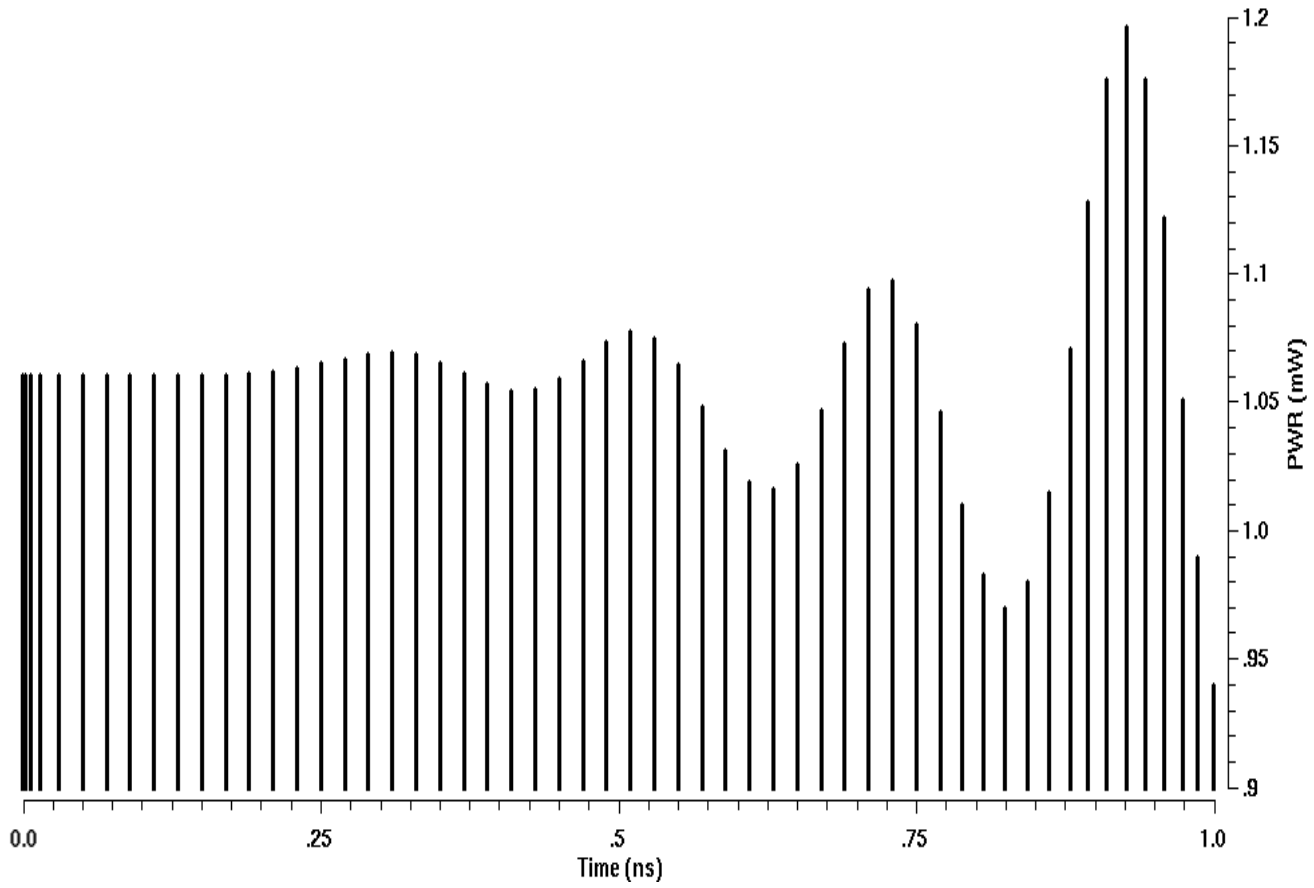


Figure 8.28 Power Dissipation by PA in 45nm

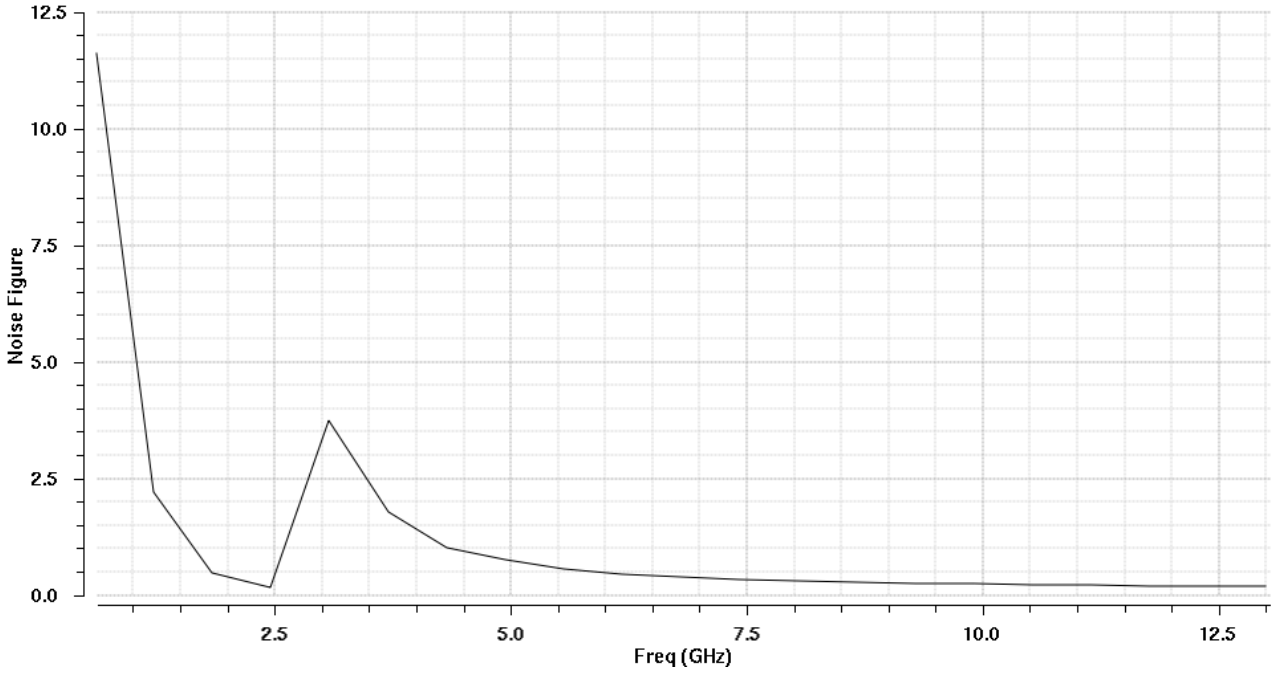


Figure 8.29 Noise Figure of PA 45nm

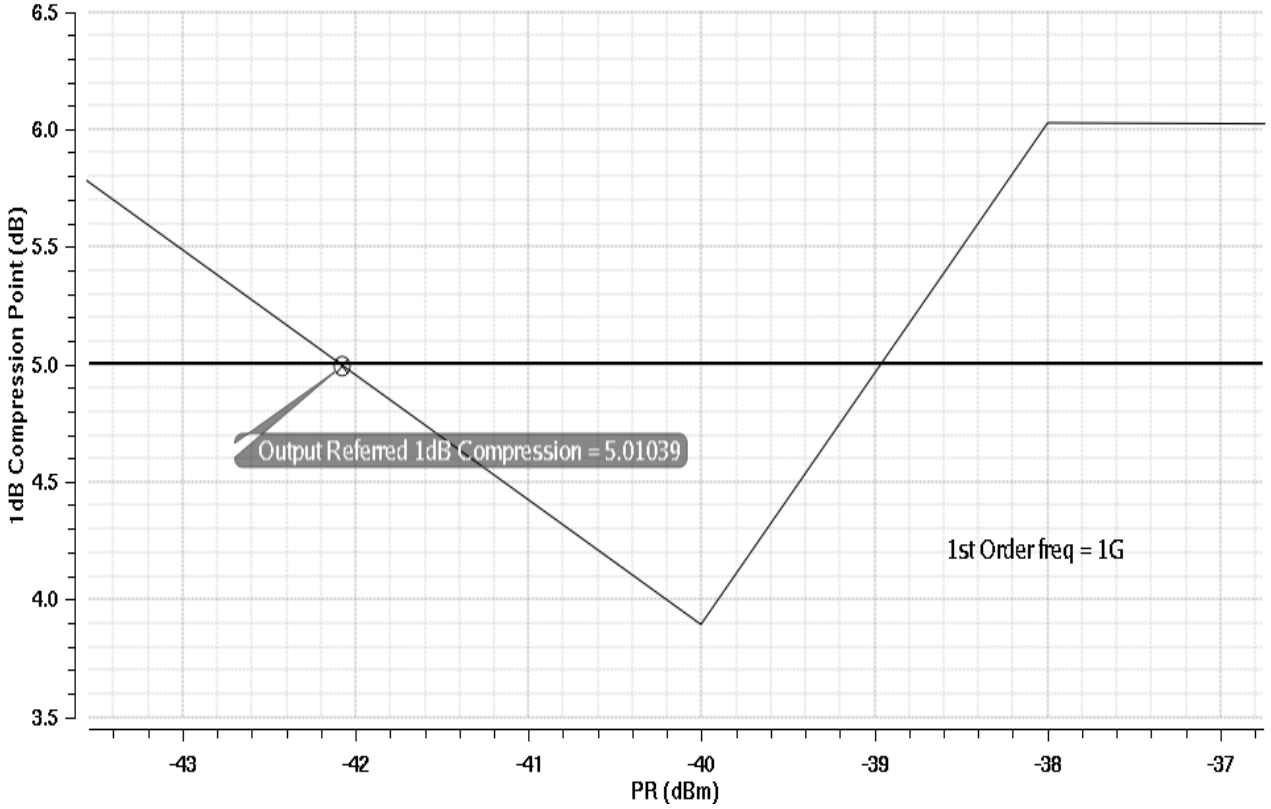


Figure 8.30 1dB Compression Point for PA in 45nm

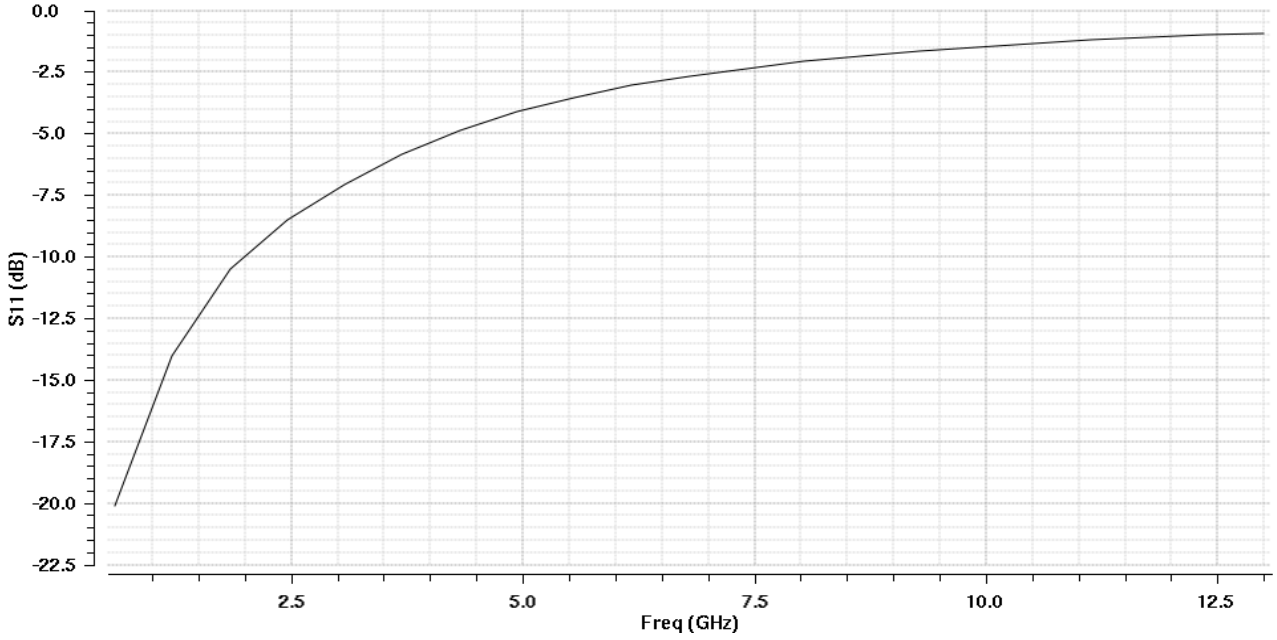


Figure 8.31 S11 of PA in 45nm

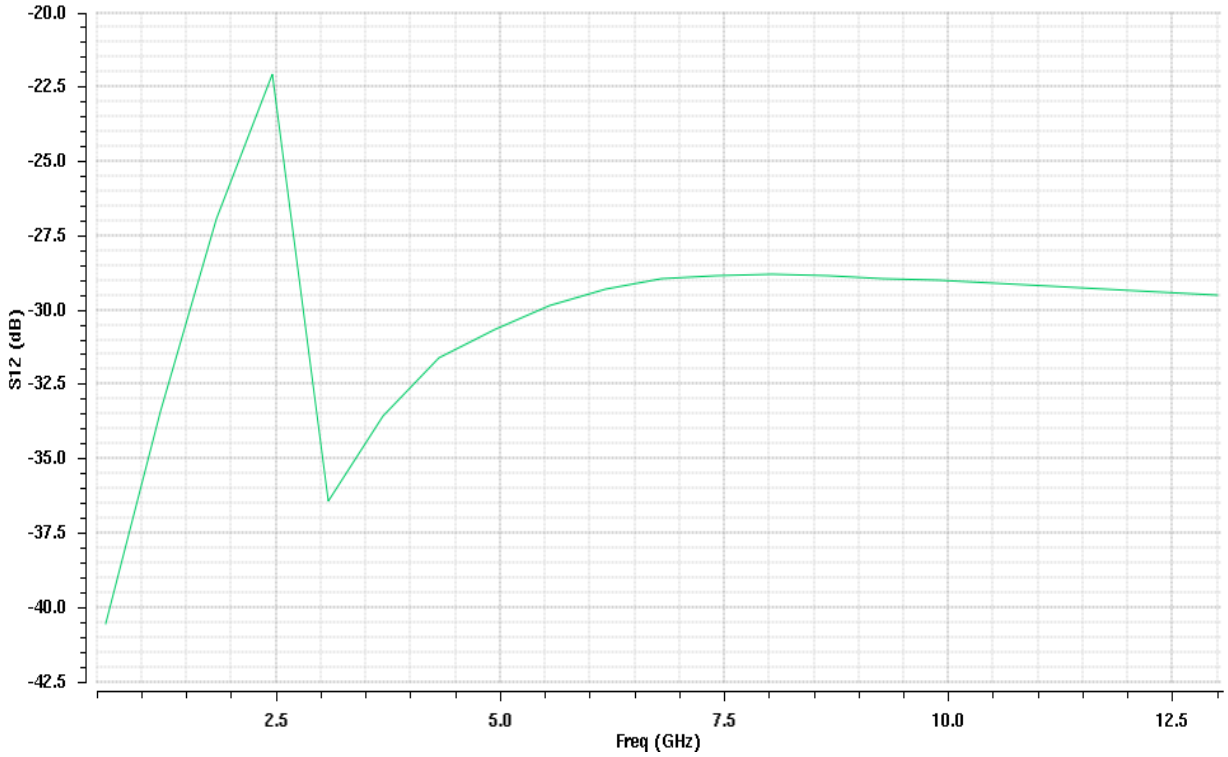


Figure 8.32 S12 of PA in 45nm

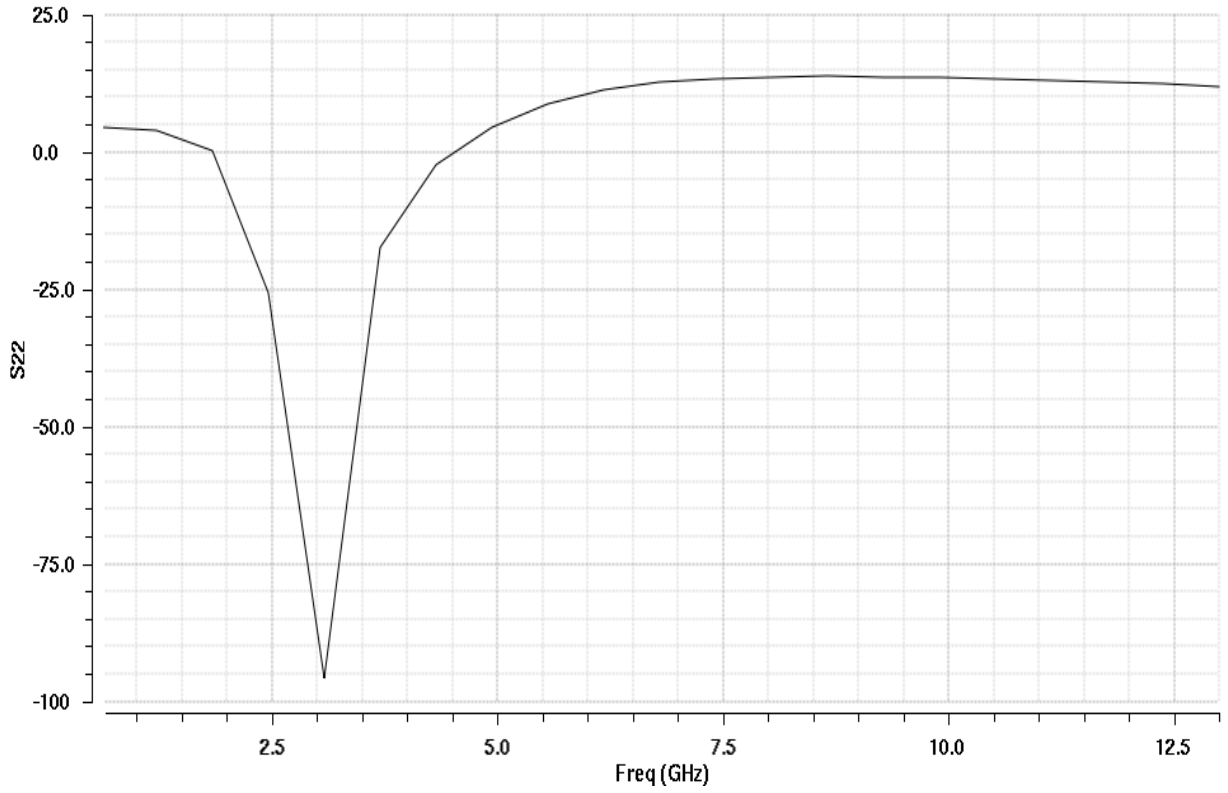


Figure 8.33 S22 of PA in 45nm

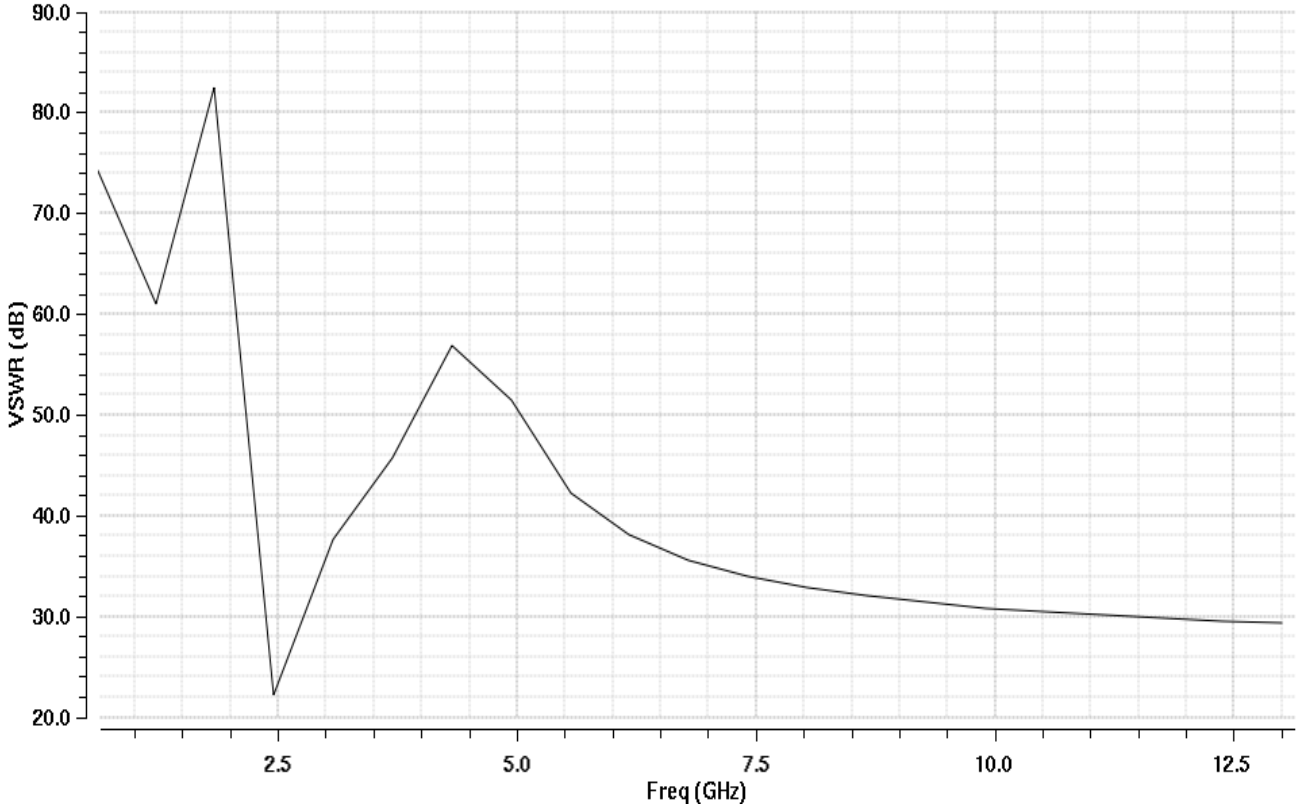


Figure 8.34 VSWR of PA in 45nm

Chapter 9 FINAL RESULT TABLE

9.1. 180nm PA:

Table 9.1 Result of PA in 180nm CMOS process

Serial Number	Parameter	Value
1	Bandwidth(GHz)	100
2	Average Noise Figure(dB)	5.21
3	Minimum Noise Figure(dB at GHz)	2.76 at 31.2
4	Power Dissipation(mW)	163.28
5	Average Stability(dB10)	1.01
6	Average S12 (dB)	-76.32
7	Gain(dB)	21.32
8	Power Gain(dBm)	103.21
9	VSWR(dB)	121.36
10	Group Delay(psec)	1.131

9.2. 90nm PA:

Table 9.2 Result of PA in 90nm CMOS process

Serial Number	Parameter	Value
1	Bandwidth(GHz)	13
2	Noise Figure(dB)	5.62
3	Power Dissipation(mW at Vdd)	92.14 at 1 V
4	Average Stability(dB10)	1.71
5	Average S12(dB)	-51.43
6	Average S21(dB)	34.95496
7	Power Gain(dBm)	338
8	Gain(dB at GHz)	54.38 at 7.019
9	1dB compression point(input referred)	-17.92
10	Noise Figure(dB at GHz)	3.71 at 4.27
11	VSWR(dB at GHz)	48.61 at 12.5
12	Group Delay(psec)	0.972

9.3. 45nm PA:

Table 9.3 Result of PA in 45nm CMOS process

Serial Number	Parameter	Value
1	Output Voltage(at 1mV input)	38.125
2	Gain(dB at GHz)	31.624 at 4.7
3	Bandwidth(GHz)	11.962
4	Power Dissipation(mW at Vdd)	1.075 at 1
5	Average Noise Figure(dB)	3.26
6	S12 (dB at GHz)	-36.491 at 3.61
7	VSWR(dB at GHz)	83 at 2.12
8	Output Referred 1dB compression Point(dB)	5.01039
9	Group Delay(fsec)	97.13

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