Lovely Professional University

"DESIGN OF 40 GHz INDUCTORLESS VCO FOR ULTRA WIDEBAND APPLICATIONS IN 90 nm CMOS TECHNOLOGY"

Dissertation-II

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By

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Under the guidance of

Mr. Tejinder Singh

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ABSTRACT

In modern communication system, VCOs act as basic building block for transmitting the frequency. Due to high phase noise performance, VCO with LC tank are highly utilized with passive inductors and varactors in radio frequency. Practically the tuning range of VCO is low and this makes it unsuitable for wide band applications. By using switched capacitors and switched inductors, tuning range of wide frequencies can be obtained. The limitations are enlargement of chip area and making the control mechanism complex. For overcoming these restrictions, the concept of frequency tuning is introduced by removing practical inductor from the circuit which increases the stated problems. So we will try to remove the L i.e. inductor from the VCO by replacing it by an equivalent circuit.

For ultra wide band RF systems, a wide frequency tuning range of an LC VCO is required. By using switched capacitors and switched inductors, tuning range of wide frequency can be obtained. The disadvantages are enlarging the chip area and complexity of control mechanism. By using an inductor-less circuit which tends to reduce the chip area, we wish to fabricate the circuit with no physical inductor present on the chip or in a way, using simulated inductor.

The LC Voltage Controlled Oscillator has been designed with the centre frequency of 40 GHz and frequency tuning range varying from 37.7GHz to 41.9 GHz. The conventional passive has been replaced by a simulated active inductor with the value of 401.75pH. The IMOS varactors have been used in the resonant tank circuit. The proposed VCO is designed in 90 nm CMOS technology.

CERTIFICATE

Certified that this Dissertation-2 Report entitled "**Design of an Inductor-less Voltage Controlled Oscillator for Ultra Wideband Applications in 90 nm CMOS technology"** submitted by **Inderjeet Kaur Saini** having registration number **11004846,** student of Electronics and Communication Engineering Department, Lovely Professional University, Phagwara, Punjab in the partial fulfillment of the requirement for the award of Masters of Technology (Electronics and Communication Engineering) Degree of LPU, is a record of student's own study carried under my supervision and guidance.

This report has not been submitted to any other university or institution for the award of any degree.

Name of Supervisor

ACKNOWLEDGEMENT

"Though revenge is profitable, gratitude is a great virtue."

It would not be possible to complete this Dissertation-II without the help and valuable support of certain people. Let this paragraph be my own way to thank those who contributed or supported me along the way. So there it is.

All you can see here would not be possible without Mr. Tejinder Singh, the project supervisor. He gave me a chance to work on this topic and was both supportive and motivating. I do not recall exactly how many times he convinced me and motivated to work harder. Numerous times he provided me with constructive criticism and acted as the as a real guide for me.

I present a deep sense of gratitude to all those who have been detrimental in the Dissertation-II work. Special acknowledgement to the Lovely Professional University for providing with all the required stuffs in the library, all the good books which were readily available and an easy access to the IEEE terminal and Springer for downloading quality papers.

Finally, I would like to express thanks to my Family. Without their support all of this could not be even started. Thanks to them I was always able to focus on my education, never worrying about the financial side of it. They always supported me mentally too.

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Inderjeet Kaur Saini

11004846

DECLARATION

I hereby certify that the work, which is being presented in the report entitled "DESIGN OF AN INDUCTROLESS VOLTAGE CONTROLLED OSCILLATOR FOR ULTRA WIDEBAND APPLICATIONS IN 90 nm TECHNOLOGY" in partial fulfillment of the requirement for the award of the Degree of Masters of Technology submitted to the institution is an authentic record of my own work carried out during the period August 2014 to April 2015 under the supervision of Mr. Tejinder Singh.

Inderjeet Kaur Saini
Date: April 2015
11004846 Signature of student

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CHAPTER 1
INTRODUCTION

Communication between people led to the beginning of civilizations. For communicating, the message signal is modulated at the transmitter end at a very high carrier frequency so as to travel long distances. This process requires the use of local oscillators. At the receiver side, the message signal needs to be extracted from the modulated signal. For the withdrawal of the baseband signal from the up converted signal, a local oscillator producing the same carrier frequency must be present. Therefore, local oscillators are a crucial component for frequency synthesizers in wireless communication. Also, Voltage Controlled Oscillator forms the basic block of PLL (Phased locked loops). The frequency phase detector's input (PFD) is the reference frequency from crystal oscillator which needs to be very accurate. The output of the PFD goes to the charge pump and that of charge pump serves as an input to the loop filter. The loop filter generates voltage which serves as an input to the VCO. There is a negative feedback loop and divide by N circuitry to the PFD. We can only generate an accurate clock which is an output when the input is accurate. Here the whole PLL is not discussed. Just a single block is taken and worked upon.

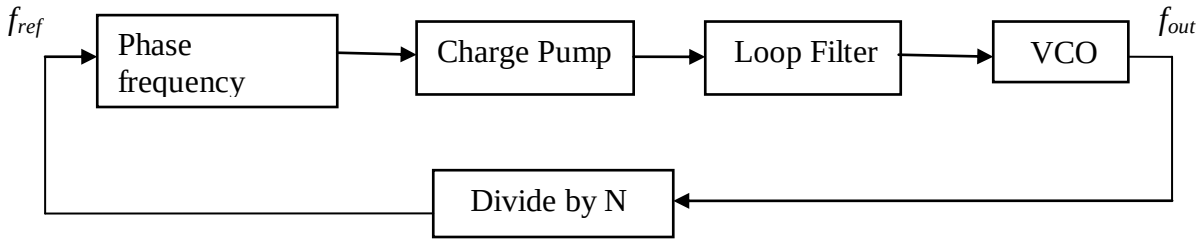


Fig. 1.1 Basic PLL Circuit

1.1 Basics of VCO

1.1.1 Definition

Oscillator is a type of amplifier that imparts itself with an input signal via feedback. The chief rationale of using an oscillator is to spawn a waveform or an oscillation of amplitude which possesses constant peak and a definite lock frequency and the waveform must have sustained amplitude and oscillation which is the basic requirement of an oscillator. The figure shows the block diagram of basic oscillator circuit.

Oscillators can be defined as electronic circuits that yield the output without the call of any input. The dc supply voltage is the only input and the output is achieved in the form of a periodic wave. Waveforms like sine wave, triangular wave, square wave etc. can be obtained from the oscillator.

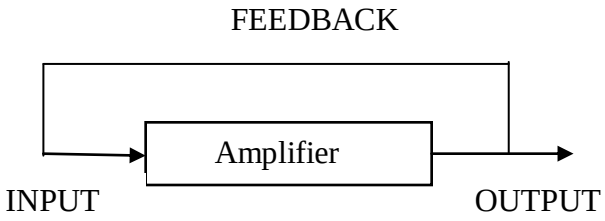


Figure 1.2 Basic Oscillator Block Diagram

1.1.2 Classification of VCOs

There are two different types of oscillators- LC tank oscillators and Ring Oscillators. If the noise is less and there is a stringent requirement of clean oscillations, we use LC oscillators. An LC VCO comprises of amplifier and resonator. The resonator consists of varactors, capacitors and inductors. Collpits oscillator and cross coupled LC VCO are the examples. LC VCOs are extensively used in RF circuits because of good noise performance and a wide tuning range. The harmonic distortion is also low for the ring oscillators. If the phase noise is relaxed, a chain of cascaded inverters can be used and if the output of the last stage is fed back to the first stage, oscillations can be produced. This topology is called ring oscillator.

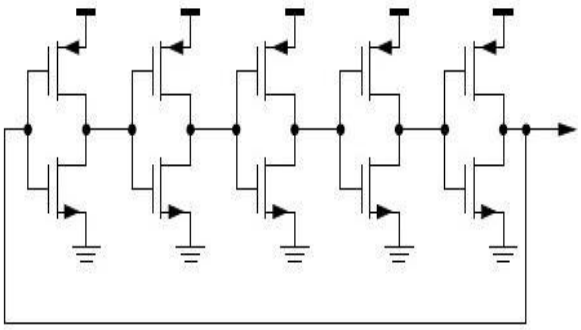
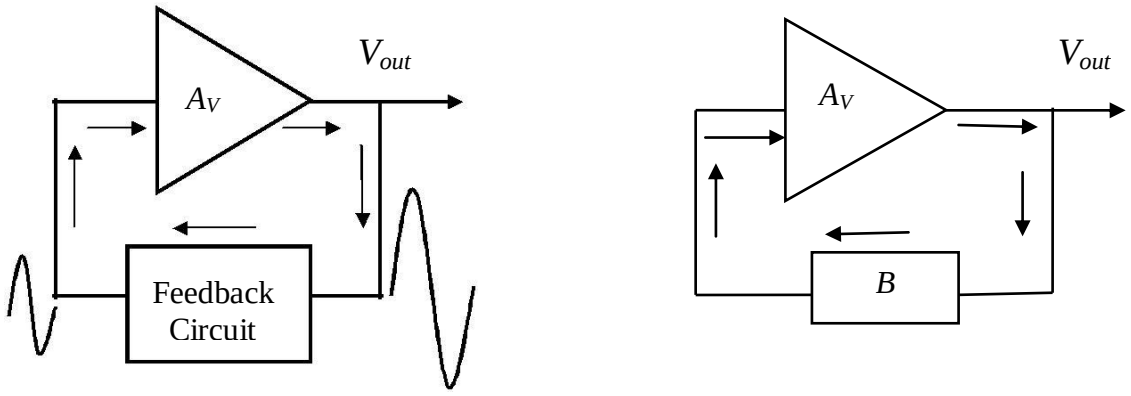


Figure 1.3: 5 stages Ring Oscillator [8]

It does not require any resonator. They operate in switching mode and produce a square wave as an output signal. The ring oscillators have the advantages of ease of integration, small chip area and high oscillation frequency due to which it is employed in high speed applications.

1.1.3 Conditions for oscillations

1. The phase shift around the feedback loop must be 0 degrees. 2. The voltage gain Acl around the closed feedback loop (loop gain) must equal 1 (unity) [8].



(a) The phase shift around the loop is $0^{0.}$ (b) The closed loop gain is unity.

Figure 1.4 General conditions to sustain oscillation

The output of an oscillator is in form of voltage that repeats itself periodically. No input is imparted to the circuit while the output should be sustained. Consider the unity gain negative feedback system where β is constant .The closed loop transfer function can be jotted down as:

$$\frac{Y(s)}{X} = \frac{H(s)}{1+\beta H(s)}$$

If βH(s) = -1 at s= jω1, gain=∞. The circuit amplifies its own noise and eventually begins to oscillate. If βH(jω1) = -1, then the circuit begins to oscillate. The condition may be expressed as | βH(jω1)|= 1 and LβH(jω1)= -180 which is called Barkhausen's criteria [8].

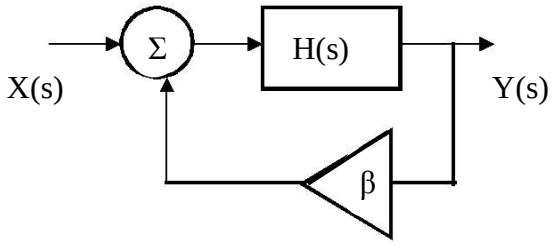


Figure 1.5 Basic negative feedback systems

The negative feedback itself introduces 180 degrees phase shift. Therefore, the net phase shift is 360 degrees. The 360 degrees phase shift is mandatory to build up oscillations since the feedback signal must be in-phase to the noise. The loop gain must be unity for the growth of oscillations.

1.2 Design Methodology

For the VCO to be known as an ideal VCO, the output frequency must be a linear function of its control voltage [12].

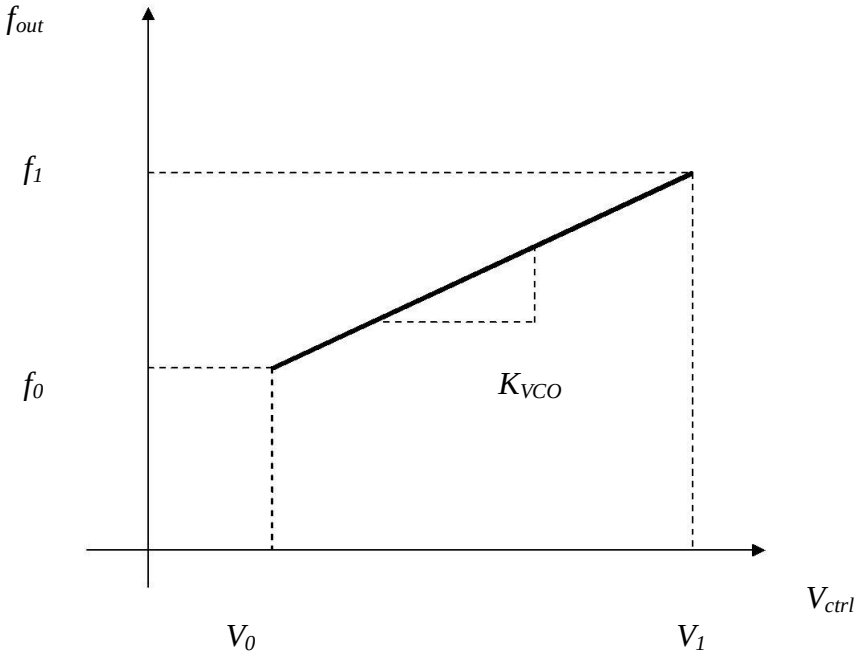


Figure 1.6 Frequency versus control voltage plot

$$f_{out} = f_0 + K_{VCO}.V_{ctrl}$$

Where f_0 is the frequency of oscillation at V_{ctrl} =0 and K_{VCO} presents the gain of the circuit. The frequency tuning range is f_2-f_1.

Frequency tuning is obligatory not only to swathe the complete application bandwidth but also to reimburse for variations of the centre frequency of the voltage controlled oscillator

that are rooted by the process and temperature. The oscillation frequency of the LC VCO is equal to:

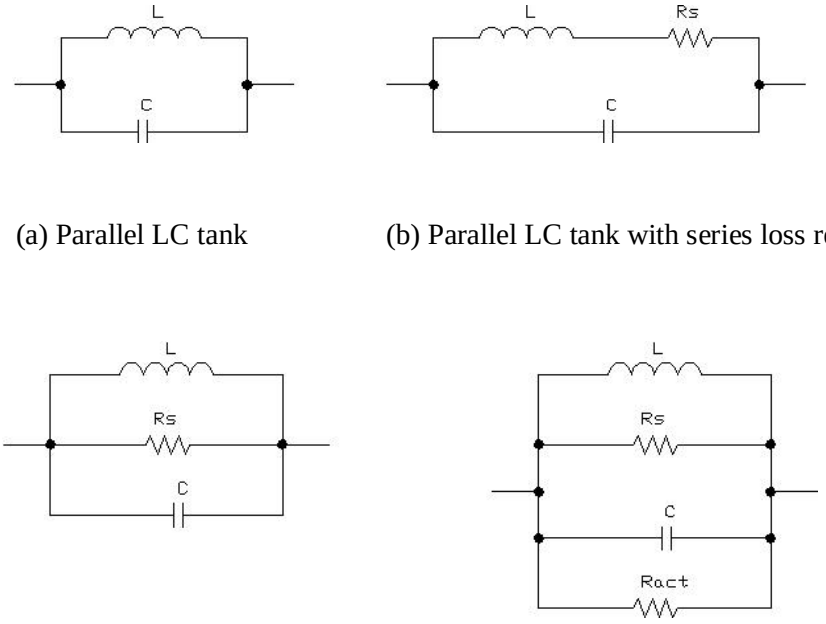
$$f_{osc} = \frac{1}{2\pi\sqrt{LC}}$$

The basic LC VCO consists of an LC tank with an inductor and capacitor in parallel. On chip inductors have finite losses with them. The quality factor Q can be 10, 12 or 15 or may draw near to 20-25 if good thick metal is used. If the Q is shrill, losses are less and superior are the oscillations. If energy is instilled into the tank, oscillations will be produced that will damp down gradually.

1.2.1 Negative resistance oscillator

One way of taking the series loss is to convert it into an equivalent parallel resistor. The same LC tank has been converted to one with series R to parallel R. The parallel resistance can be roughly given as: $R_p = Q(L\omega)$

This relation is not valid for all the ranges of ω but only when Q is high i.e. only for a narrow band of frequencies.



(a) Parallel LC tank (b) Parallel LC tank with series loss resistance

(c) LC resonator with parallel loss resistance (d) Negative resistance parallel resonator

Figure 1.7 LC tank Circuit

Some component is required in parallel with R_p which posses some negative resistance to cancel it. Therefore, resonators possessing losses are connected to an additional component which has negative resistance R_{act} which is equal to:

$$R_{totS} = R_s - R_{act} = 0 (R_s = R_{act})$$

$$R_{totP} = \frac{-R_P . R_{act}}{(R_P - R_{act})} = \infty$$

But in CMOS, no passive negative resistance components are available. So nmos cross coupled pair can be used for producing negative resistance.

1.2.2 Cross coupled Pair

Let Vx be the superficial voltage source and Ix be the current flowing out of V_x. Due to positive gate voltage at nmos-2, it will be on and the current will be pulled down through it as shown in the figure. The resistance is given by:

$$\frac{V_x}{I_x} = \frac{-2}{g_m}$$

Various cores are used now-a-days. One of them is CMOS core. The reason it is called CMOS core is because it has two cross coupled pmos s well as two cross coupled nmos pair. Here we will get gm from p side and gm from n side for single bias. Therefore it is 2 times gm obtained from the nmos core. Having more gm, we can have less bias current and keep power lower and can still generate negative resistance and can make the LC tank to oscillate. The nmos core will bear more power and less voltage swing. The benefit of the nmos core is in the case of lesser voltage supply. If the voltage supply is much dwindled, scaling vdd down and down, voltage drop across pmos as well as the voltage drop across nmos is needed so we might rum into headroom issues where the oscillator might not oscillate. The following figure shows the 2 nmos cross coupled devices.

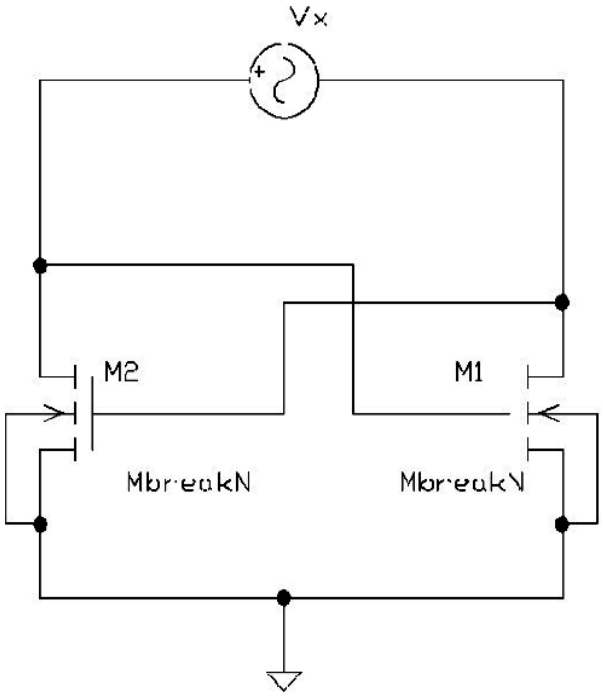
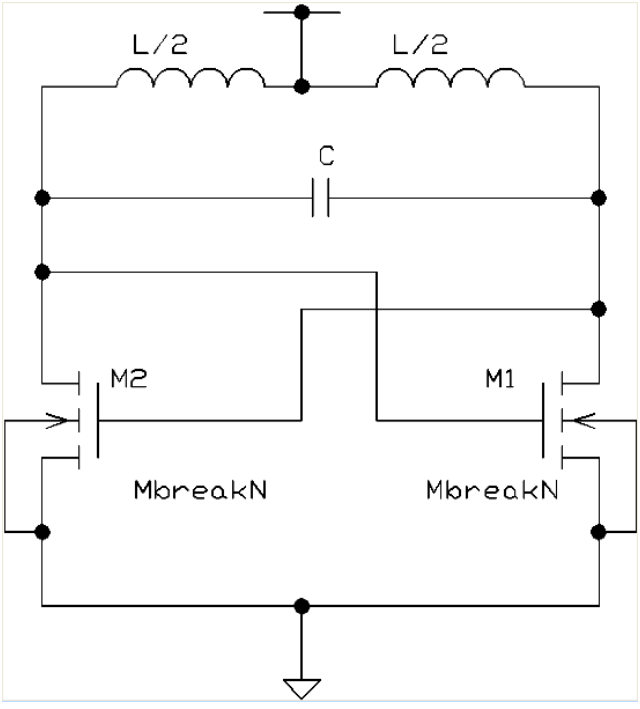
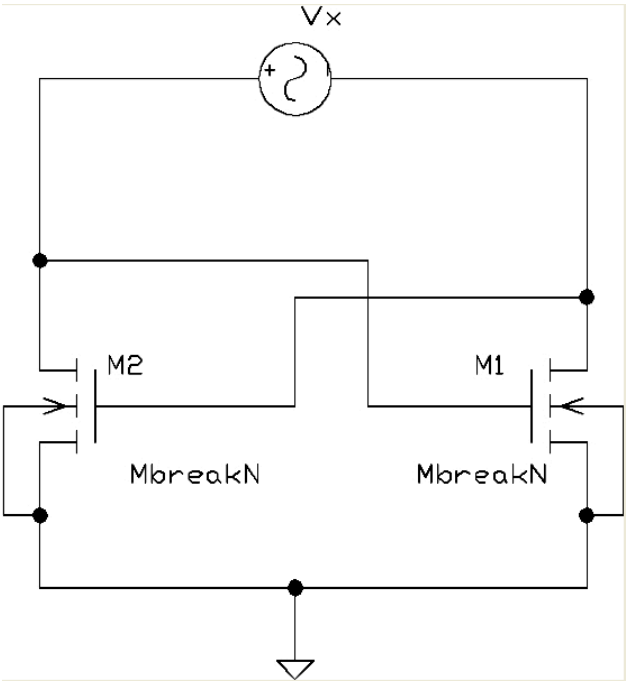


Figure 1.8 NMOS Cross coupled Core



(a)



(b)

Figure 1.9 (a) pmos core (b) nmos core with splitted inductor

Moreover, employing more than two active devices except the NMOS or PMOS pairs augments the number of noise sources and parasitic, thereby resulting in negative impact on the phase noise performance and frequency tuning characteristics. If we compare the pmos and nmos only circuits, pmos only circuits also have pros and cons. Pmos cross coupled pair is employed in voltage controlled oscillators for low noise characteristics [10].

Flicker noise in pmos is about 10 times lesser than that of the nmos counterpart with same dimensions. The size of pmos devices is double the size of nmos devices. Moreover, the mobility of holes is lesser than that of the electrons. As the transconductance is solely controlled by the size of the device so nmos only pair can be used to reduce the chip size.

1.2.3 Key specifications

- Oscillation frequency (ω_{osc}) and tuning range($\omega_{oscmin} - \omega_{oscmax}$)

Usually we can't tune the inductor because the inductor always employed is on chip inductor but we can tune the capacitor. And the desirable thing is to have wide tuning range.

- Phase noise, spurs etc.

Different types of components employed in the resonators:

- Spiral on chip inductors:

These are the most widely used inductors due to their advantages of being robust to the changes, cost effective, reliable and can be employed in KHz to MHz range. A lot of attention has been paid to the modeling of these inductors [11]. But they suffer from a very high loss due to low quality factor Q.

- Wirebond inductors:

Bond wires can be employed as inductors. Also they eradicate the problem of high loss as they hold a high quality factor. But they are susceptible to mechanical vibrations. At higher frequencies short length wirebond is brought into play which further corrodes the tolerance of the inductor. Due to this, wire bond inductors have not found significant use in the practical applications.

- Switched inductors and switched capacitors:

They consist of an active switch to switch between the inductors and capacitors. During the on state of the switch, the charging of the inductors in the inductor switching block occurs in series and the capacitors are discharged in parallel in the capacitor switching block. During the off state of the switch, the inductors are discharged in parallel in the inductor switching block while charging the capacitors occurs in series in the capacitor switching block. Using this method, wide tuning range can be obtained but the size of chip increases drastically making the design procedures complex.

1.2.4 Components required for tuning the frequency range

- PN Junction varactor:

Other names for p-n junction varactor are varicap or capacitor diode. It has the advantage of small size and being inexpensive. But lower quality factor Q, non-linearity in the characteristics, lower voltage and limited range of voltage are the drawbacks of p-n junction varactors. The p-n junction varactors are shown in the figure. The connection of p-substrate is with the ground. The p+/n-well are single ended while the n+/p-well are floating varactors. The voltage swing at the varactors must make certain that the varactors are reverse-biased incessantly to produce the capacitance. The junction capacitance is given by:

$$C_J = \frac{C_{J0}}{\sqrt{1+\frac{v_R}{\phi_o}}}$$

Where the junction capacitance at zero-biasing voltage is denoted by C_{jo}, is the reverse bias voltage of the junction and o is built-in potential of the junction. The graph of C_j versus V_R is a non linear graph. The large parasitic series resistance, large resistance between n-well and p-substrate, smaller capacitance tuning range determine the performance of the p-n junction varactors.

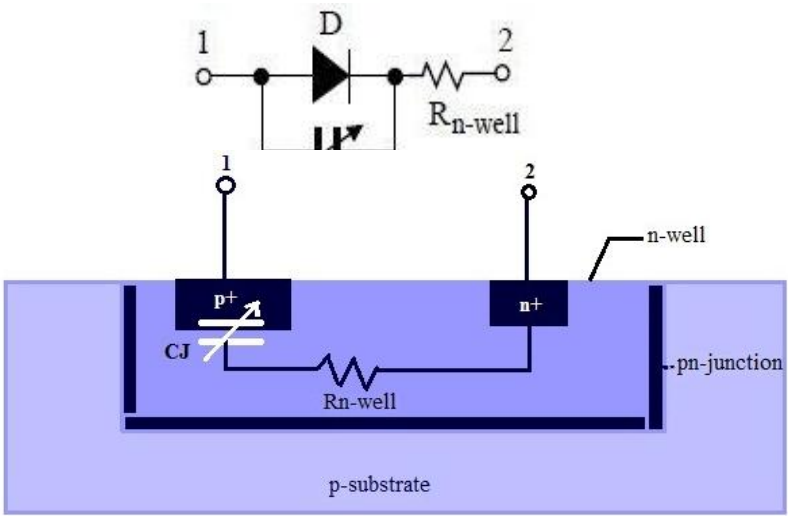


Figure 1.10 Side-view of p+/n-well varactor [12]

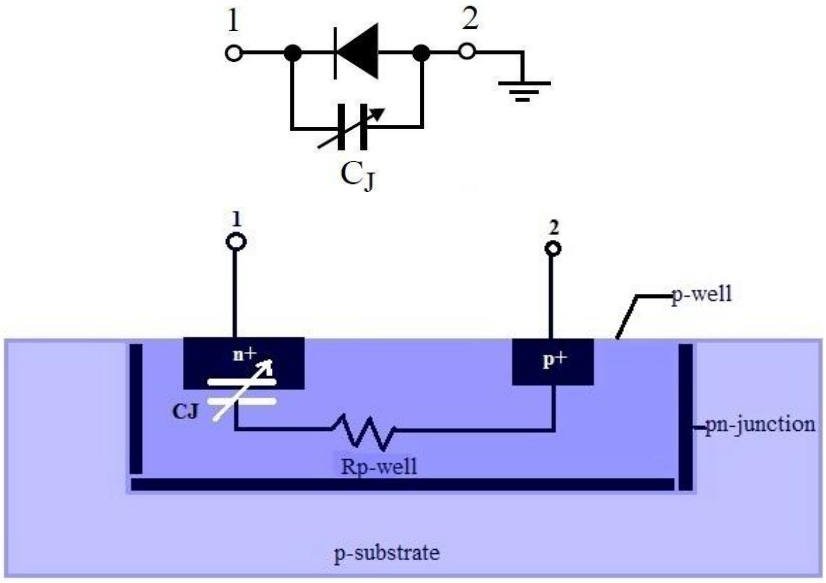


Figure 1.11 Side-view of n+/p-well varactor [12]

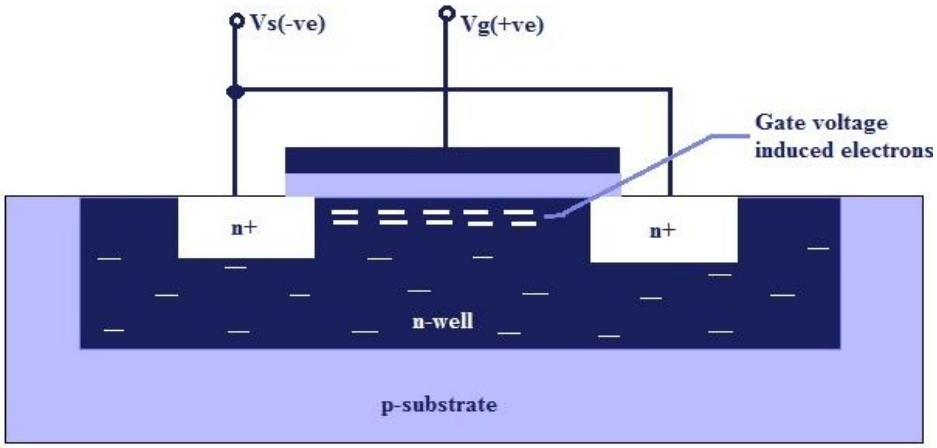


Figure 1.12 Side view of accumulation mode MOS varactor when Vg>Vs [12]

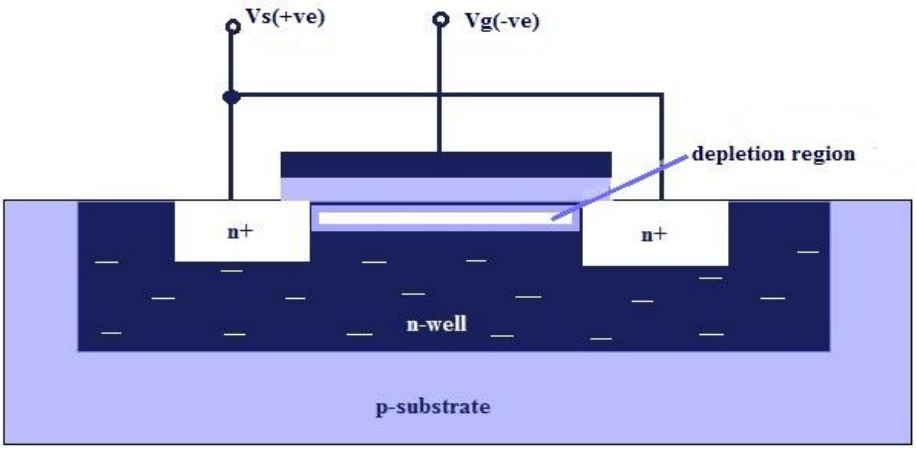


Figure 1.13 Side view of accumulation mode MOS varactor when Vg<Vs [12]

Case 1: Vg < Vs: n-well region electrons beneath the gate will face repulsion and depletion region is crafted.

Case 2: Vg > Vs: n+ diffusion regions electrons will be drawn to the area beneath the gate, leading to the formation of an accumulation layer and C_{gs} rises to the C_{ox}. The capacitance of the accumulation mode varactor is determined by the dc operating voltage. The accumulation mode varactors have large voltage swing across their terminals which serve as the biggest advantage.

- MOS Varactor:

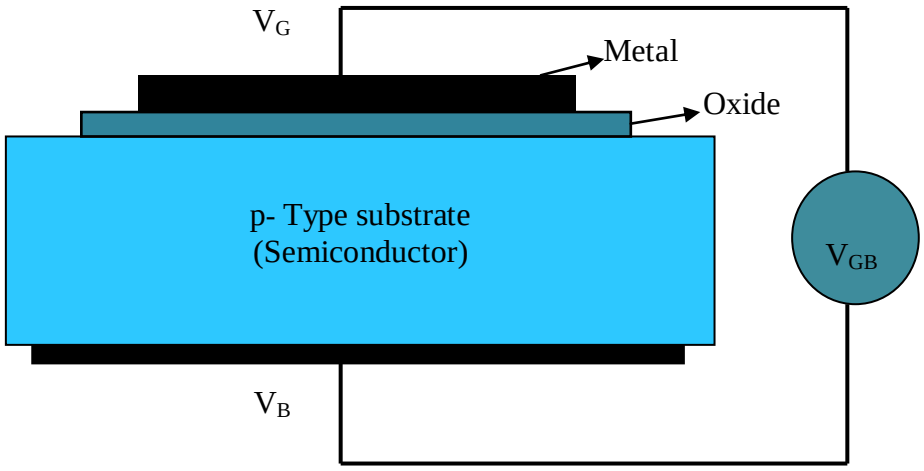


Fig. 1.14 n-type MOS varactor Structure

Although the reverse –biased p-n junction varactors could be used to supply the capacitance for the LC- VCO but these were not able to scale down with the technology node and endured low C_{max} / C_{min} ratio imposing limitation to the tuning frequency range. There persisted one more limitation when the p-n junction might become forward biased with the increase in the voltage swing aggravating the losses in the circuit. So another medium for tuning the VCO is MOS varactor. The figure shows the basic structure of nmos varactor with top metal contact, thin oxide layer and p-type substrate. The MOS varactor holds high Capacitance/Area ratio when a comparison is drawn between a MOS varactor and a p-n junction varactor.

CHAPTER 2
LITERATURE REVIEW

Robert M. O Leary et al. [1] presented three different integrated differential designs with different resonator circuits. These topologies can be used for high data rate achievement in UWB communication. The first topology involving the use of a spiral inductor and a pair of MIS varactors produced potentially large frequency range but the VCO gain becomes extremely large in the middle of the range grounding instability in the loop. The second one known as dual capacitor resonator involving the use of one varactor diode pair for coarse tuning and the other one for fine tuning possesses the advantage of having the requirement of only one resonator. In the third topology, so as to increase the frequency range, a switched inductor is used. The dual capacitor and switched inductor LC VCO produced the highest tuning frequency range i.e. 20.2% and 26% respectively presented three different integrated differential designs with different resonator circuits. These topologies can be used for high data rate achievement in UWB communication. The first topology involving the use of a spiral inductor and a pair of MIS varactors produced potentially large frequency range but the VCO gain becomes extremely large in the middle of the range grounding instability in the loop. The second one known as dual capacitor resonator involving the use of one varactor diode pair for coarse tuning and the other one for fine tuning possesses the advantage of having the requirement of only one resonator. In the third topology, so as to increase the frequency range, a switched inductor is used. The dual capacitor and switched inductor LC VCO turned out to produce the highest tuning frequency ranges i.e. 20.2% and 26% respectively.

	Tuning range (MHz)	BW (MHz)	tuning range (%)	Core current(mA)	PN 1MHz (dBc/Hz)	PN 10MHz (dBc/Hz)	Core area (mm^2)
Basic	5.87-6.18	310	5.12	3.25	-97	-111	0.117
Dual cap.	3.56-4.16	800	20.2	3.25	-93	-113	0.157
Inductor	2.52-3.27	750	25.9	4	-117	-125	0.136

The limitation of this paper is that despite of good phase noise, the frequency range of the LC oscillators cited here (all the 3 configurations) is very less (in MHz only). Due to large size of the inductor, the core area increases.

Chien-Hsuan Liu et al. [2] reported a low power current reused VCO with source damping resistors for low power consumption in 0.18um technology. The voltage swings in each output terminal are asymmetric. Here, the phase difference of two voltage swings procured by pmos and nmos are simulated with varied source damping resistors. Phase noise is reduced.

The proposed oscillator has a center frequency of 2.26 GHz only which is very less. This parameter can be worked upon i.e. the narrow tuning frequency can be broadened.

	Tuning range (GHz)	Centre frequency (GHz)	Power dissipated (mW)	PN 100KHz (dBc/Hz)	PN 1MHz (dBc/Hz)
[2]	2.25-2.45	2.26	1.62	-101.87	-121.66

S. Zafar et al. [3] portrayed a 4.224 GHz complementary cross coupled LC –VCO along with tail resistor instead of current source for UWB applications in 0.18um. Phase noise can be reduced by:-

- The utilization of pmos exhibiting low phase noise as compared to nmos.
- Use of capacitive cross coupling to suppress noise up conversion in differential LC-VCO.
- Use of LC tank to remove noise from tail resistor Symmetric VCO design to achieve low noise.

An increment in the bias current in the mA range can lead to the improvement in the phase noise. Trade off exists between power consumption and phase noise. Fine tuning is the role performed by the varactors while the coarse tuning role is done by the inductor. A tail resistor and source damping resistors in series with the nmos and pmos are employed for avoiding noise contribution from the active current source. By-pass capacitors in parallel

with the damping resistors make up for the parasitic and thermal noise of the resistor. Hence, an improvement in the symmetry and the reduction in the noise are obtained.

	Tuning range (GHz)	Centre frequency (GHz)	Power dissipated (mW)	PN 100KHz (dBc/Hz)	PN 1MHz (dBc/Hz)
[3]	3.77-4.27	4.224	3.42	-94.7	-120.1

The parameters that need to be worked on in this paper are narrow tuning range and large power dissipated.

N.C Shirazi et al. [4] have drawn a comparison the differential tunable active and passive inductor for LC tank in 0.18 um technology. The design based on active inductor produces unacceptable phase noise in comparison to passive inductor. nmos cross-coupled transistors are employed for providing negative transconductance (which is further used to compensate the losses from the LC tank) and for compensating the losses. For obtaining least inductance at maximum frequency, the control voltage Vctrl should be adjusted at the lowest frequency. The nmos cross-coupled transistors and active inductor are for circuit bias and to minimize power consumption.

Technique	Centre frequency (GHz)	DC power (mW)	Output power (dBm)	PN @1MHz (dBc/Hz)
Active inductor	5.5	29.38	0.211	-80.214
Passive inductor	5.5	7.592	-0.454	-106.4

The active inductor configuration consumes high DC power plus the phase noise needs to be worked upon which is not optimum.

L. Aspemyr et al. [5] designed a 0.6 V VCO based on the cross-coupled differential NMOS configuration in a 90 nm RF-CMOS GPS L1 band. The motive of the design is to reveal the relevance of low voltage and low power in deep submicron CMOS transistors. The operating frequency of the VCO is 6.3 GHz and a divide-by-four circuit buffer offers the wanted

1575.42 MHz signal. The supply voltage is 0.6 V and 1.58 GHz carrier is used when the bias current of 2.6 nA is attained with -122 dBc/Hz at 1 MHz offset.

Technology	Power(mW)	Vdd(V)	PN (dBc/Hz)	Offset (MHz)	Current(mA)
90 nm	1.56	0.6	-103	0.1	2.6

Although this work has upgraded the technology but continues to use the same conventional inductor for L which occupies a large core area. Also the narrow frequency range is a main problem.

Liang-Hung Lu et al. [7] presented a design for LC – voltage controlled oscillator by employing a differential tunable active inductor for wide frequency tuning range. The coarse tuning is achieved by the tunable active inductor while the fine tuning is controlled by the varactors.

Tuning range (GHz)	Tuning range (%)	PN 1MHz (dBc/Hz)	Core area (mm^2)	DC power (mW)
0.5 - 3	143	-101 to -118	0.15 x 0.3	6-28

The tuning range of the circuit is narrow plus the circuit is implemented in 0.18 um technology.

J. Lu, N.Y Wang et al. [8] presented is an LC-VCO operating at 20 GHz centre frequency in 65 nm Technology with differentially tuned MOS varactors. A simple voltage converter is used to generate differential tuning voltages without compromising the VCO gain or phase noise. Differential cross-coupled nmos with negative transconductance is used. Tail resistor is used to reduce flicker noise.

Tuning range (GHz)	Center frequency (GHz)	PN @1MHz (dBc/Hz)	Core current (mA)	Core Area ($mm^{2)}$
14.6-22.2	20	-96	4	0.06

The phase noise can be further optimized as well as core area can be reduced further. The core current is also more in this case.

J.J Kim et al. [9] presented an ultra wide band VCO in 65 nm technology. The proposed VCO adopts series/parallel reconfigurable structure of inductor arrays to attain the twice of the tuning range of their equivalent inductance. The frequency range obtained is 4.2 to 18.7 GHz.

Both series as well as parallel structure of tunable inductors can be implemented by adding switches. With same number of inductors, the reconfigurable structure can formulate the tuning range of equivalent inductance two times wider. The circuits use switches for gaining a large tuning range but it is very difficult to design such ideal switches. So, designing such switches can be the drawback.

M. Mehrabian et al. [10] implemented an UWB VCO in 0.18um CMOS technology with the tuning range of 308 to 7.4 GHz employing a tunable active inductor (TAI) which can be tuned from 0.34 to 0.61nH with the help of tunable resistor. The active inductor topology exploits the gyrator-c configuration which comprises of transistors engendering inductive impedance. The conventional gyrator-C topology has been improved by making its cascade structure and providing the feedback. The power dissipation is approximately 29.1mW and phase noise of -92.05dBc/Hz is obtained.

M. Filanovsky et al. [11] utilized the active inductor approach for realization of CMOS voltage controlled oscillator with wide tuning range. The passive inductor is replaced with the active tunable inductor in the LC VCO configuration. The operation is carried out and the output frequency ranging from 500 MH to 10.3 GHz is obtained.

Dominic DiClemente et al. [12] presented an active inductor based LC voltage controlled oscillator topology for ultra wide band applications. The oscillator is designed in 0.18 um CMOs technology. Two methods for tuning the inductance are used. Using the wide band tuning mechanism(coarse tuning), a frequency range from 0.2 GH to 6.5 GHz is obtained while from the second method i.e. the primary tuning method (fine tuning) grants the

frequency range from 1.4 GHz to 1.7 GHz. The phase noise performance is optimum with -118.5dBc/ Hz at 1MHz offset frequency. A wide tuning range is obtained by the liability of the tuning of the active inductor.

Markus Tormanen et al. [13] presented a 25 GHz CMOS differential Voltage Controlled Oscillator in 90 nm CMOS technology. The technique of filtering is employed at the common source terminal to slash the phase noise. The VCO uses incessantly tuned Accumulation mode MOS varactor for frequency tuning due to low losses. The VCO consumes 6.6 mW of power with the tuning range of 8.7% and the phase noise of -106 dBc/Hz is achieved at 1 MHz offset. FET is used as the current source because it provides the best phase noise performance.

Li Xian et al. [14] proposed a low noise LC VCO using the technique of switched capacitor array design. The 2.4 GHz LC VCO uses three bit binary weighted switched capacitor array dictated by digital control word. The three bit binary weighted switched capacitor array technique switches the frequency to eight distinct levels and IMOS varactor is used to tune the frequency. Less voltage headroom is provided because of the presence of top and bottom current sources which leads to decrease in the output swing and hence deterioration of the phase noise. Further removal of the current sources leads to the increase in the output swing and decrease in the flicker noise thereby sinking the phase noise.

CHAPTER 3
RESEARCH METHODOLOGY

The CMOS integrated circuits are extensively used now-a-days for RF circuits. It has become the technology of choice. Due to very large scale integration of circuits, the construction of high frequency circuits using amalgamated components instead of the distributed ones has become realistic. Due to the recognition of the CMOS technology, miniaturization along with cost effectiveness is being demanded. The cost of the integrated circuits decreases if more circuits can be fabricated on the same chip i.e. the same silicon area. Nevertheless the minimum size of the analog circuits is larger than that of the digital circuits. The analog circuits employ the use of passive components like inductor (the largest analog circuit component) and capacitor which lead to the enlargement of the chip area.

The concern for the silicon area for the LC oscillator can be put to an end by the use of such circuits which can possess the inductive characteristics and still occupy the smaller chip area. These circuits are known as active inductors or simulated active inductors. They consist of only active components and capacitors and can simulate the inductive impedance.

3.1 Problem Formulation

Voltage controlled Oscillators serve as a vital component in the RF transmitters and receivers and are commonly used in the frequency modulation and demodulation for the better transmission of the message signal at long distances in the communication purposes as local oscillator, in frequency selection and signal generation. Many signal processing systems require the reference signals. Therefore these oscillators are very important in the wired and wireless communication.

If we use the crystal oscillators, then we have to deal with various problems. At low frequency, the quartz crystal resonators have fixed frequency which can’t be tuned. At high frequency there is degradation in the performance of the quartz crystal due to the shortcomings of the material properties.

Now-a-days Radio frequency receivers employ Phase Locked Loops (PLLs) where the frequency can be controlled with the help of a control voltage signal. Then the PLL is locked to a certain desirable frequency. Different VCOs with different centre frequencies involving various techniques have evolved from the last few years and every time either they try to reduce the noise performance or increase the frequency tuning range etc. to make robust systems. But the demand for miniaturization of the circuits continues. The shrinking size of the active components has made it possible to continuously decrease the chip size.

Various VCOs have been implemented in 180nm, 130 nm, 90 nm and 65 nm technologies and have achieved the desired centre frequencies. Some of them tried to replace the lossy inductor component with an active inductor. Therefore, some active inductors have been designed in the CMOS technology. Therefore this study has tried to collaborate with both the requirements of miniaturization as well as lossless technology. The study has implemented an LC VCO in 90nm technology using active inductor using 40 GHz frequency range with less noise power and lesser area.

The problem is to design and simulate an inductor-less voltage controlled oscillator with a center frequency of 40 GHz. The conventional LC VCO has various passive components like capacitor and inductor but the proposed VCO has replaced these passive components with PMOS based varactor serving the purpose of capacitance and a 4-transistor based active inductor instead of passive inductance.

3.2 Basics of Gyrator

The resulting voltage is shifted by 90^0 when the passive inductor is biased with the sinusoidal current. This action is carried out by impedance and admittance functions that typify the electronic circuits in the frequency domain. If an assembly of non inductive components is able to result into impedance with a phase shift of 90^0, the circuit simulates the characteristic behavior of the inductor.

3.2.1 Active Inductor Fundamentals

There is an inverse phase relationship between the V-I characteristics of the capacitor and the inductor. Due to this reason, the capacitive impedance has to be inverted in order to simulate inductance by the deployment of capacitors in a circuit to get the desired phase relationship. This is done by the use gyrator circuit which is a two port network. The active inductors are a special case of gyrator circuit. The simple gyrator- C circuit consists of two back to back connected inverters as shown in the figure 3.1. Active inductors have emerged as an alternative to the passive inductors due to their compact size and the ability to control over the simulated inductance.

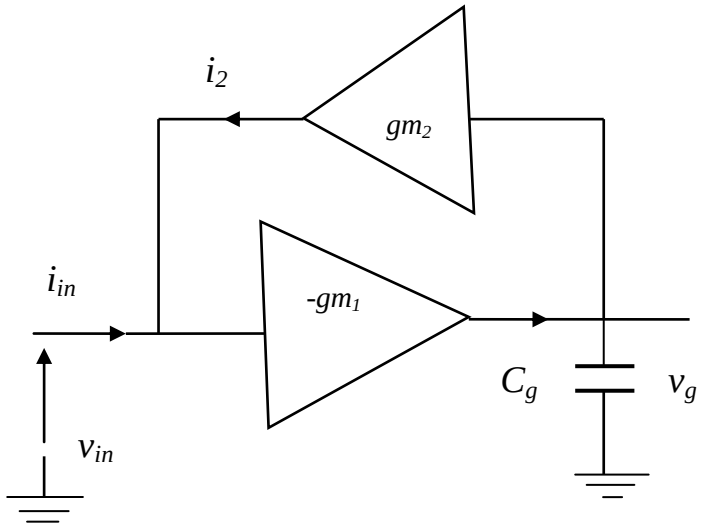


Figure 3.1 An ideal Active Inductor [12]

3.2.2 Types of active inductor

- Single ended or differential active inductors:

Single ended circuits have simple designs and experience inductive impedance at only one port while differential tunable inductors have differential transconductors to improve CMRR but require double the number of components employed in single ended active inductors. The one node of the single ended active inductor is connected either to ground or the supply voltage while the input voltage is fed to the other node. The both nodes are connected to different inputs in the case of differential active inductor.

- Grounded or floating:

Grounded inductors have one lead connected either to ground or VDD i.e. simulate parallel inductance. Floating active inductors have two ports with inductive impedance in series between them and are suitable for applications requiring series inductance.

- Single or multistage transconductance amplifiers:

Single stage amplifiers use one transistor to provide gyration conductance. Multistage amplifiers provide larger gains and can minimize some of parasitic effects. The cost is larger power consumption and required number of components is also large.

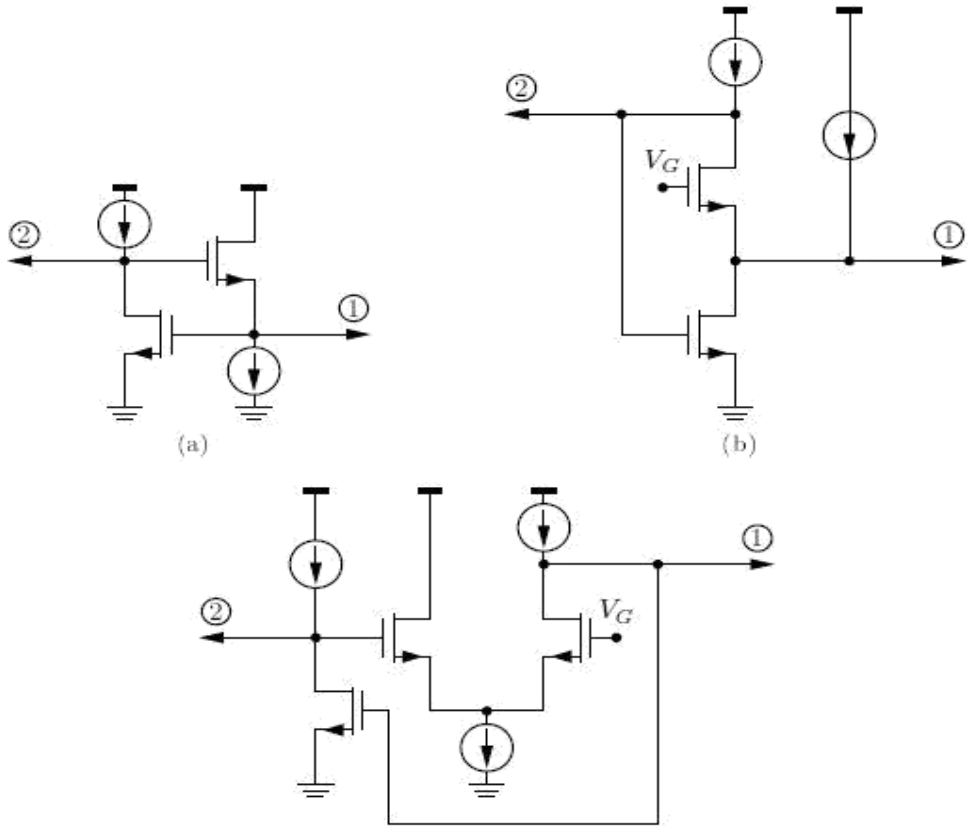


Figure 3.2 Commonly used CMOS grounded gyrator circuits (a) Common source-common drain (b) Common source-common gate (c) Common source- 2 stage amplifier [12]

In practice, the hybrid structures are used. The single ended architecture directs to a grounded inductor circuit, while the differential architecture is more appropriate for a floating gyrator. The multistage amplifiers can be deployed if necessary in every case. Figure 3.2 shows some grounded active inductors that over the years served as a base for further improvements reported in numerous papers. The load at one node is capacitance, whereas the opposite port

generates inductive impedance. It is mandatory to indicate that practical circuits are seldom symmetrical and for this reason one of the ports is usually preferred as an input. The grounded gyrators from Figure 3.2(a) and 3.2(b) represent the simplest architectures (single ended using single stage transconductor). The advantages are simple design and small number of components used. The large circuit loss due to the parasitic is the drawback. The third gyrator from Figure 3.2(c) uses a two stage amplifier to increase input impedance of the active inductor. In comparison with the former architectures, an extra transistor introduces additional noise and non-linearity to the circuit.

3.3 Design Specifications of Active Inductor

The spiral inductor using lossy silicon could not easily attain high quality operation in CMOS technology. Moreover, it amplifies the area factor of the chip leading to intricate mechanism. The substitute method is to exploit an active inductor using active devices [15]. The conventional active inductor is grounded active inductor which consists of two back to back connected trans-conductors generating inductive impedance and if one of the terminals is connected to the capacitor, it is called gyrator-C network. The basic gyrator-C topology has stumpy inductance value and constricted tuning range. Hence the structure can be improved with the cascade transistor topology and active resistor in the feedback line [16]. The pmos based active inductor circuit is exploited in this design asshown in figure 3.3.

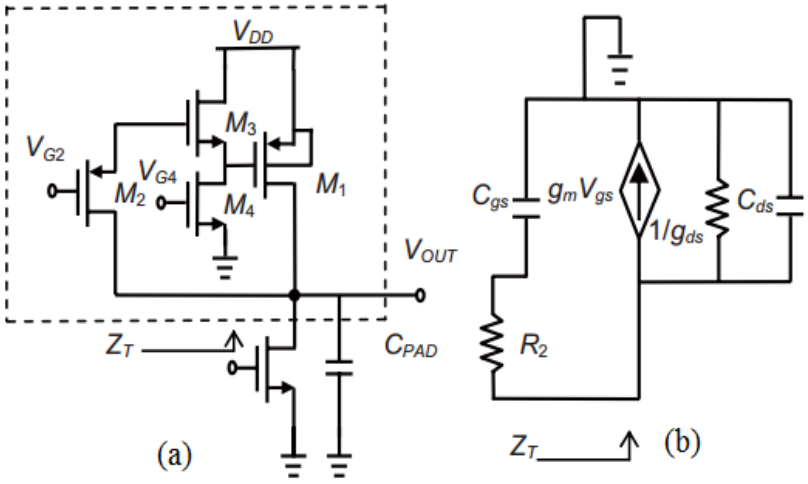


Fig.3.3 (a) Active inductor Schematic (b) Small signal Model

The M2 transistor working in deep triode region performs the role of a MOS resistor in addition to combining the output node to the transistor M1. To grant a vast bias current to M1, the circuit is appended by an additional circuitry in between M1 and M2. The supplementary circuitry is the level shifter which consists of the source follower transistor M3 and M4 as a current source. This configuration can work with even dwindling voltage supply without the want for any extra supply source other than VDD for greater voltage as in the case of NMOS based active inductor. The PMOS based configuration of active inductor offers the advantage of less power consumption in contrast to the NMOS based design while demonstrating low resistance of 50Ω at the termination. The M1 transistor doesn't endure body effect and has comparatively persistent V_{th} which further gives it consent to function with minimal voltage headroom. Because of the body effect, g_{m3}, g_{ds3} and g_{mb3} of M3 may fluctuate but the alterations will have insignificant effect on the gain of the level shifter which is given by [17]:

$$gain_{levelshifter} = \frac{1}{(1+(gds_4 + g_{\partial ds3} + g_{mb3})/g_{m3})}$$

The gain of the level shifter is here taken as unity. g_m, C_{gs}, C_{ds} and g_{ds} are the parameters of M1, R_2 is the on-resistance of M2 . The small signal model is depicted for the PMOS based active inductor in the figure and the termination impedance can be given by [17]:

$$Z_T = \frac{1 + j\omega C_{gs} R_2}{(g_{ds} + g_m) - \omega^2 R_2 C_{ds} C_{gs} + j\omega(C_{gs} + C_{ds} + R_2 C_{gs} g_{ds})}$$

$$L = \frac{R_2 C_{gs}}{g_{ds} + g_m}$$

$$R_S = \frac{1}{g_{ds} + g_m}$$

$$C_p = C_{ds}$$

$$\omega_o = \sqrt{\frac{g_{ds} + g_m}{R_2 C_{gs} C_{ds}}}$$

The inductive impedance of the active inductor is not conditional to R_s and can be amended by modifying V_{G2} which further alters the value of R_2. The value of R_s is 50Ω. The resonant frequency depends on the process technology. The active inductors overcome the

disadvantage of the magnetic coupling of the passive inductors. Moreover the area factor is reduced in the active inductors in contrast to the passive ones. For impedance matching, R_s should be minimum.

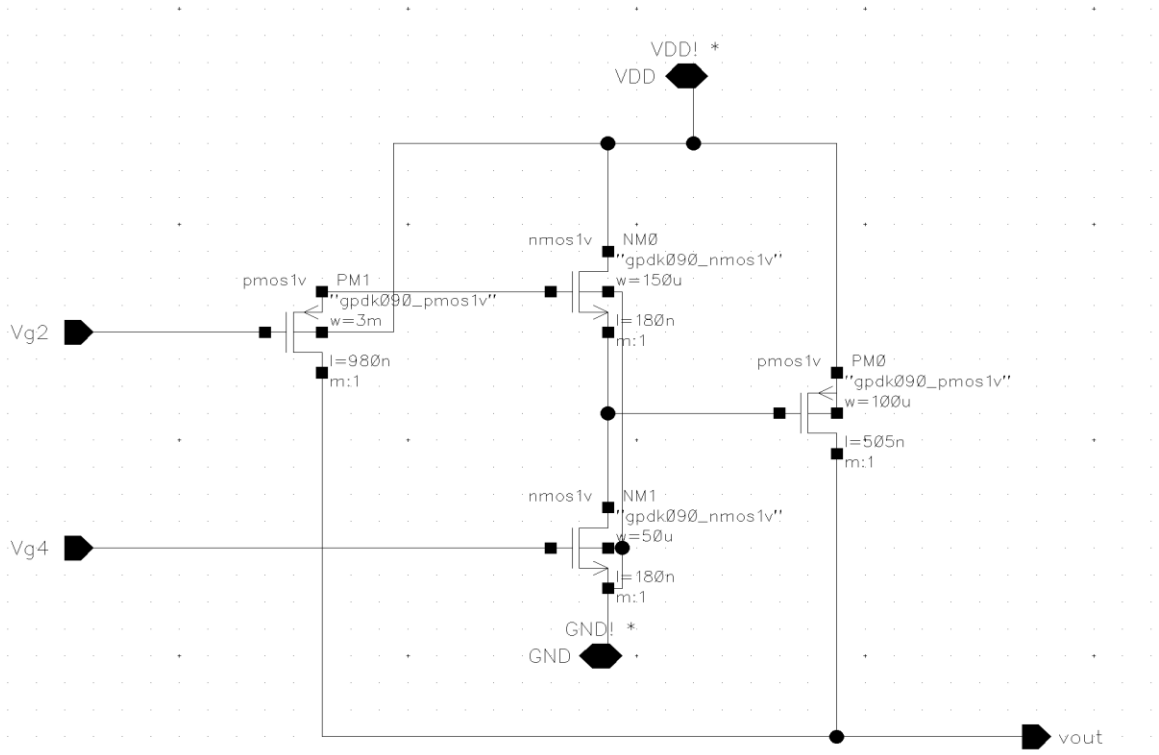


Fig. 3.4 Schematic for the Active Inductor

3.4 Design Specifications of Switched Capacitor Bank

Varactor is a source of variable capacitance which acts as the basic component for tuning the LC VCO. The gate oxide capacitance in the accumulation and inversion regions is given by [18]:

$$C_{in,acc} = C_{ox} = \frac{\varepsilon WL}{t_{ox}} = C_{\max}$$

Where WL comprises of the area of the varactor, $\mathcal{E}$ is the permittivity of the silicon dioxide, t_{ox} is the thickness of the oxide layer. The total depletion capacitance is series combination of depletion capacitance and C_{ox} given by [18]:

$$C_{dep,tot} = \frac{C_{ox}C_{dep}}{C_{ox} + C_{dep}} = C_{\min}$$

There are different varactors in which can be utilized to tune the circuit .One is the reverse biased p-n junction varactor but it has low C_{max}/C_{min}. The other one is forward p-n junction but it has large amplitude swings leading to losses in the circuit. Another commonly used varactor is the MOS transistor itself. The ratio of capacitance to area is higher for MOS varactor in comparison to the p-n junction varactor resulting in higher capacitance tuning range. They also show strong capacitance variations if the input voltage varies even in hundreds of milli volts making the circuit to operate at low voltages. MOS varactors can work in different regions: depletion region, accumulation region and inversion mode. In inversion mode of operation, when the substrate of the varactor is separated and connected to the voltage supply, the varactor does not work in the accumulation region but is said to be in inversion mode of operation.

For the present design, PMOS based varactors are used. In this, the source and drain of the PMOS transistor are shorted and the substrate is connected to VDD. Two identical PMOS transistors with shorted source and drain are connected in such a way that they form a mirror image at the junction and the tuning voltage is applied at the junction. It displays invariable capacitance characteristics and displays a wide tuning range. The invariability of the dc/small signal plot inhibits the tuning range deprivation by the amplitude swing. Further, IMOS varactor is less susceptible to latch-up as its n-well is connected to VDD instead of tuning voltage.

Another MOS varactor that can be used is accumulation mode varactor which witnesses abrupt, non-linear and invariable characteristics. It is made with n^+ source/ drain regions. The injected holes are restraint in the MOS channel ceasing the creation of strong, moderate and weak inversion region. The AMOS varactor exhibits good phase noise performance and lesser parasitic resistance as compared to the IMOS varactors. However, C_{max}/C_{min} ratio for AMOS and IMOS varactors is almost same. Regrettably, the n+ source/drain varactor was not accessible for this thesis.

3.5 Proposed VCO Circuit Design

The LC VCO is an oscillator with feedback arrangement which can be represented as shown in the figure 3.5. The active transistor provides the necessary negative transconductance - $1/G_m$ to reimburse the tank losses. R_p is the resistance of the tank circuit. The stable oscillations occur when the Barkhausen criterion is fulfilled i.e. the loop transfer function is exactly equal to 1[19].

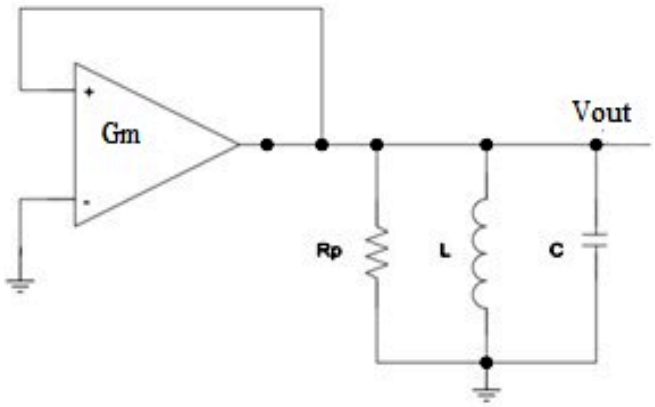


Fig. 3.5. Model of LC VCO [19]

The loop transfer function is given by [19]:

$$T_{loop}(s) = G_M \frac{sL}{1 + s\frac{L}{R} + s^2 LC}$$

Two elementary parameters of VCO design act as a constriction in resonator design - tuning range and oscillation frequency. Further in both the cases, the selection of the materials depends on their contribution to noise performance. For a wider tuning range, it is necessary for the inductor to have lager inductor to resistance ratio *(L/R)* and for the varactor to have large intrinsic maximum capacitance to minimum capacitance (C_{max}/C_{min}) because [20]:

$$Tuning = \frac{C_{v,\max} + C_{fix}}{C_{v,\min} + C_{fix}}$$

The fundamental oscillation frequency of a basic LC VCO is given by [20]:

$$f_{osc} = \frac{1}{2\pi\sqrt{L_{\tan k}(C_V + C_B)}}$$

Where C_V is the varactor capacitance and C_B is the capacitance given by switched capacitor bank. C_B is further given by [20]:

$$C_B = C_p + \sum_{n=0}^{N} n.C_{unit}$$

Here, C_p is the parasitic capacitance when all the capacitors in the bank are disconnected. C_{unit} is the unit capacitance of C_{bank}. N is the maximum value of code n. The figure 3.6 shows the basic LC VCO with NMOS core and the inductor and the capacitor forms the tank circuit which is responsible for generating the oscillations. The circuit is symmetrical on both ends and the output can be obtained in such a way that *Vout+* and *Vout-* are 180 degrees out of phase. Different VCO cores like CMOS core or PMOS only core can also be used. Every core has its own advantages and disadvantages. Therefore, PMOS core has its own benefit of good noise performance. It has been evident that flicker noise in case of PMOS is ten times smaller than that of the NMOS core of identical dimensions. On the other hand, PMOS core also possess a drawback that the mobility of the holes is lower than that of the electrons. Since the current in the PMOS flows because of the holes, the width of the PMOS must be kept twice the width of the NMOS to attain similar transconductance which in turn increases the area of the circuit.

The CMOS core provides twice g_m as in case of PMOS only or NMOS only core and can less bias current can be obtained keeping power lower and obtaining the negative transconductance. The NMOS core bears more power and less voltage swing. The benefit of using NMOS core is in the case when power supply is low. If the voltage supply is much dwindled, scaling VDD down and down, voltage drop across PMOS and voltage drop across NMOS is needed, so there might be headroom issues where the oscillator may not oscillate. The PMOS only core topology is not used here because of their contribution to parasitic capacitance that results from its reduced transconductance. Also more voltage from the supply voltage will be consumed in case of PMOS only core providing less voltage for generating oscillations.

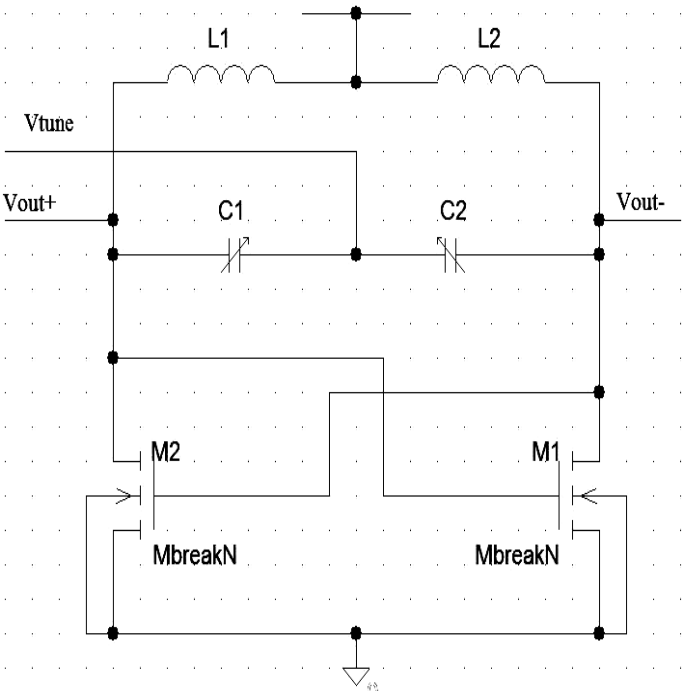


Fig. 3.6. The simple LC VCO schematic with NMOS only core

The major performance parameters of concern are operation at low voltage, low power consumption and high frequency tuning range. The proposed LC VCO consists of two cross-coupled NMOS transistors which provide negative transconductance as shown in figure 3.7. The proposed active inductor simulating the inductance of 401.75pH is used in place of conventional inductor which occupies a lot of area. The PMOS varactors provide the necessary capacitance value. The PMOS varactors used here are IMOS varactors. The bias current source is looked upon as the major contributor of flicker noise. So the pmos transistor can be used to combat with this problem. The w/l of the pmos must be kept high in order to keep it working in saturation region to keep voltage drop across it lesser. The differential mode of operation is practiced in the proposed circuit by using two PMOS varactors by shorting their source and drain terminals and providing Vtune to the shorted junction and the body is connected to VDD. The gate terminals of the varactors are connected to the active inductor's terminal to form the tank circuit. The *C1* and *C2* capacitors are employed so that the active components do not add to noise. In the proposed circuit, seven pairs of IMOS varactors are used to form the capacitor bank with digitally controlled inputs. The capacitor bank with N=7 is used to provide wide tuning range to the LC VCO which sets seven

discrete bank values. The active inductor's value is fixed and the capacitance is made variable to obtain the tuning range.

The schematic for the inductor-less voltage controlled oscillator is shown in the figure 3.7 in 90 nm CMOS technology process nodes and a power supply of 0.9 V. This topology can be efficiently used for operations at high frequencies and low voltage supply. The PMOS core has not being used here due to its participation in the parasitic capacitance resulting into downfall in the transconductance.

Also, PMOS cross-coupled pair devours supplementary voltage headroom providing lesser voltage for oscillations. $-GM$ from the NMOS cross-coupled pair is sufficient to compensate for the losses in the resonator circuit. The length and width of the NMOS transistors in the core are taken to be 0.2 μm and 2.5 μm respectively keeping in view the trade-off between tuning range and phase noise. The capacitor *C4* employed in parallel with the bias current imparts certain attenuation in terms of high frequency noise from the bias current source.

The bias current source provides considerable amount of flicker noise to the VCO. To combat with this problem, one PMOS transistor is used as a bias current source due to its characteristic of worse flicker noise up conversion compared to the NMOS of identical dimensions. The PMOS is operating in saturation region. If the dimensions of PMOS i.e. w/l are kept high, there will be lesser voltage drop and hence improved symmetry between the two outputs of the LC-VCO thereby reducing the flicker noise up conversion.

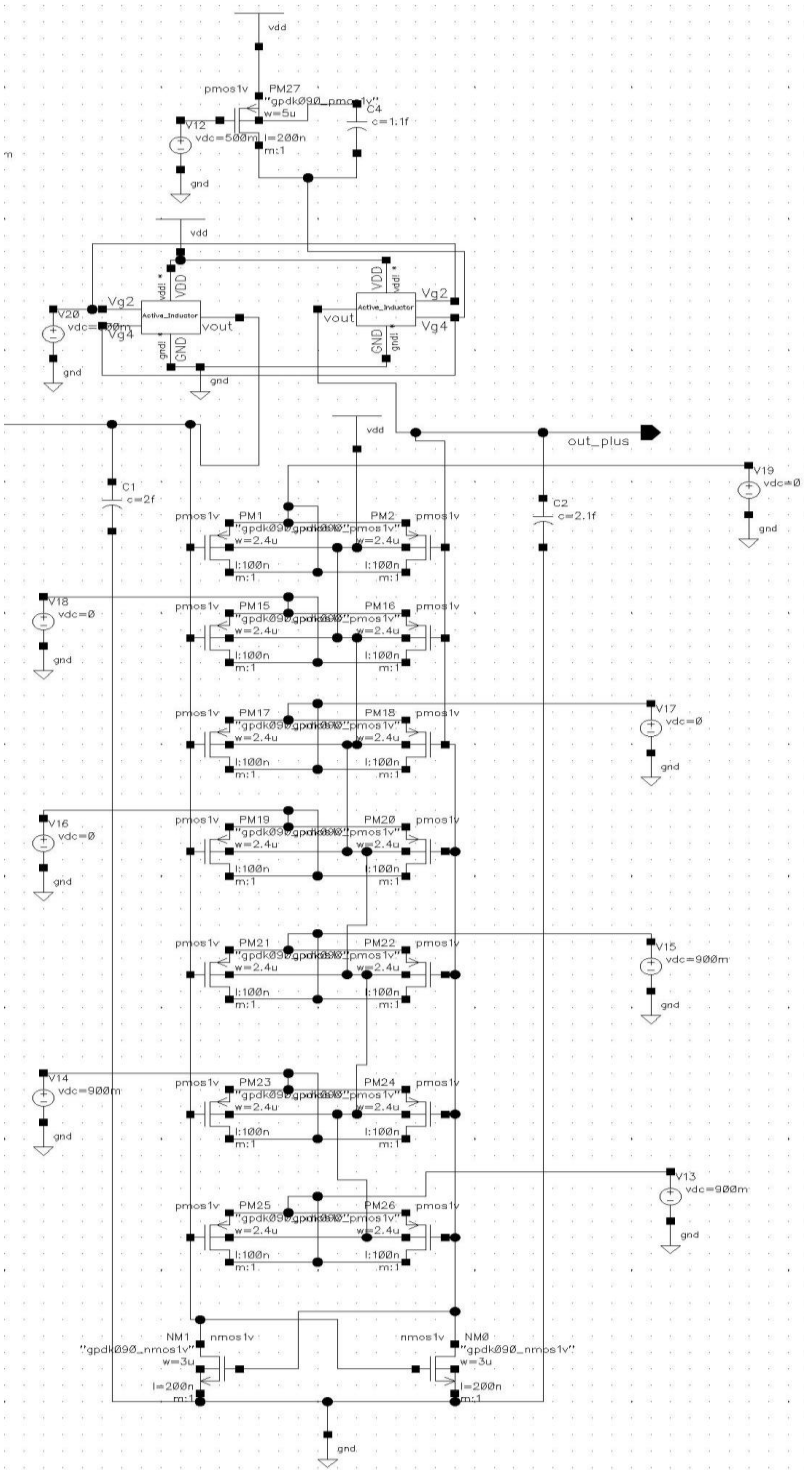


Fig. 3.7 The proposed inductor-less VCO topology

IMOS varactor has been realized using two PMOS transistors (M6,M7) with equal dimensions with their source and drain connected and tuning voltage is applied to the

interconnect of the source and source and VDD is provided to their substrates. The overall resonator circuit is formed by connecting gate nodes of seven different pairs of PMOS varactors in parallel to provide wide tuning range. Additional capacitances are used with the transistors in the NMOS core to eliminate high frequency noise components while not contributing to the thermal noise. MOS varactor uses multiple fingers and the length is positioned at the minimum to get good quality factor. Highest FOM can be obtained if the varactors have length < 0.5 μm and width of 1-5 μm.

CHAPTER 4
RESULTS AND DISCUSSION

The curve for MOS varactor in inversion mode is obtained by small signal test circuit. For making IMOS varactor, a PMOS is taken with its bulk connected to VDD. The source and drain terminals are connected together and a tuning voltage is applied to their junction. A sinusoidal wave of 0.5V and frequency 10GHz is applied as the gate voltage.

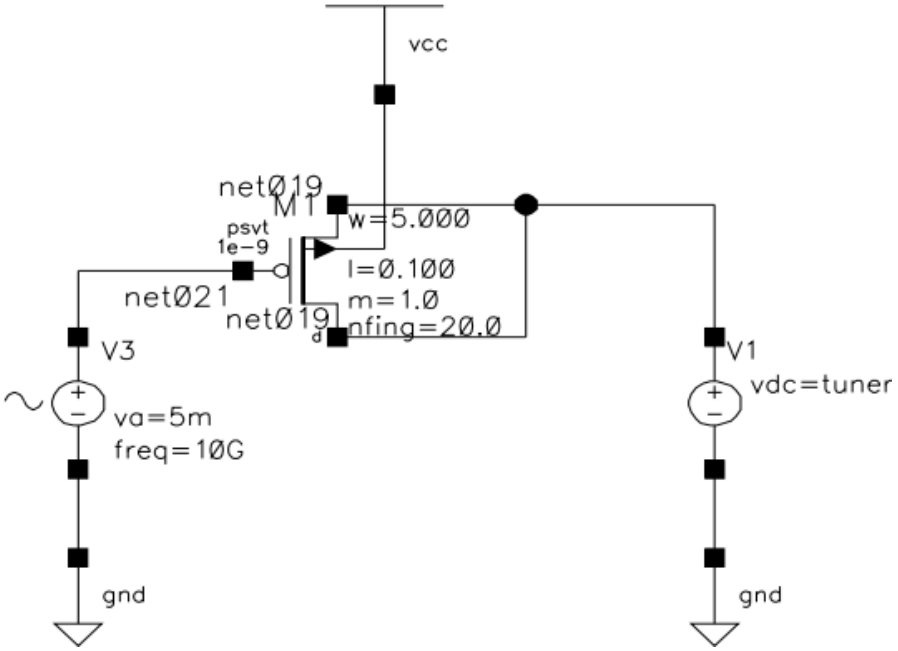


Fig. 4.1 IMOS varactor small signal test circuit

The procedure to plot the capacitance plot for the varactor in the Cadence Virtuoso involves the following steps:

- While performing DC analysis, operating point was saved.
- Then, parametric analysis was done stepping up the tuning voltage for the analysis.
- Operating point (op) was selected in the calculator window presenting a list of different parameters in which say *cgg* (gate-oxide capacitance) is selected.
- The plot for capacitance is then simulated using plot button in the calculator window.

For low power operation, the tuning voltage must not exceed VDD. However, to exhibit the capacitance characteristics, the tuning voltage is taken from -1 V to 1 V for wider area.

The IMOS varactor implemented here used PMOS transistor with length of 100 *nm*, finger width of 120 *nm* and employed 20 fingers.

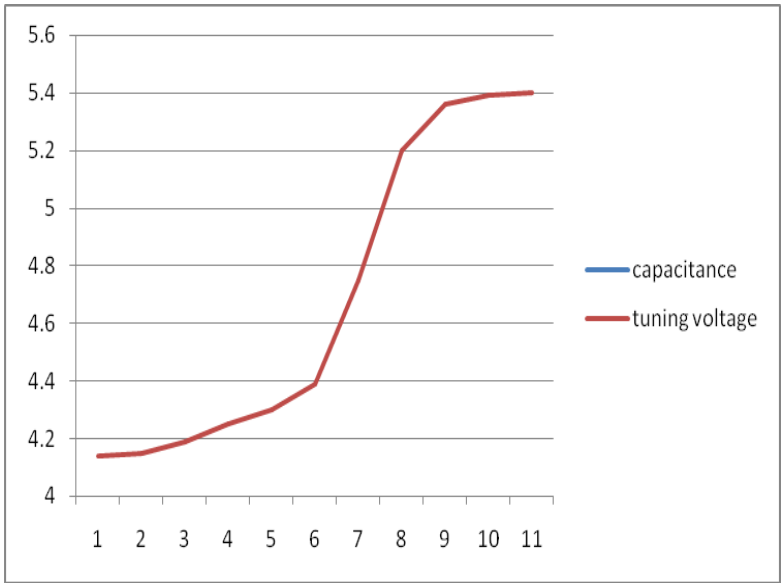


Fig. 4.2 IMOS varactor small signal characteristics

It has been observed that the maximum limit for length and width in 90nm technology is limited to 30 *µm.* Therefore, it imposes a constraint on the value of capacitance also. Two PMOS varactors are connected in series through their source/drain terminal. Then, seven pairs of PMOS varactors are connected in parallel to form the digitally switchable capacitor bank.

The biasing circuit consists of a PMOS transistor with 1 finger, length 200 *nm* and width of 5 *µm.* The capacitance value is taken as 1.1 fF. The gate voltage to the PMOS transistor is taken as 0.5 V. The VCO core consists of two cross coupled NMOS transistors each having length of 200 *nm*, 20 fingers, finger width of 150 *nm* and total width of 3 *µm.*

The transient analysis was made of the proposed VCO from the analysis window. Time for analysis was selected to be 50 *ns* and moderate was enabled. First, digital input '0' is given to all the varactors leading the voltage transient response to be as shown in the figure. The VCO takes around 0.33 *ns* to lock the frequency of 38.15 GHz and for the frequency to settle.

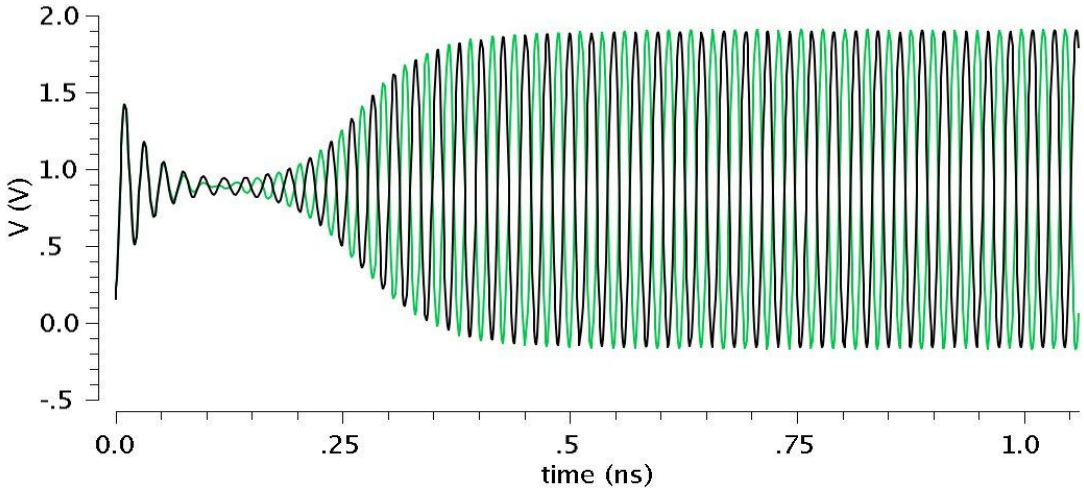


Fig. 4.3 Transient response when all vtunes have digital input '0' showing the settling time

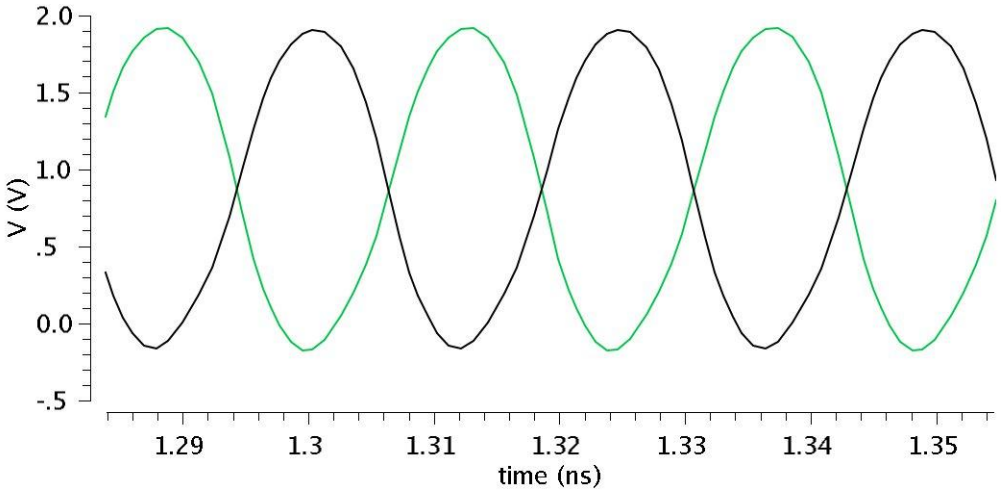


Fig. 4.4 Transient response with complementary out_plus and out_minus and all vtune= '0'

The figure 4.4 shows the two complementary outputs of the proposed VCO named as out_plus and out_minus. The output waveform of the VCO is the periodic sinusoidal signal. The lock frequency for the VCO with capacitor bank select having value 0000000 is obtained to be 38.15 GHz.

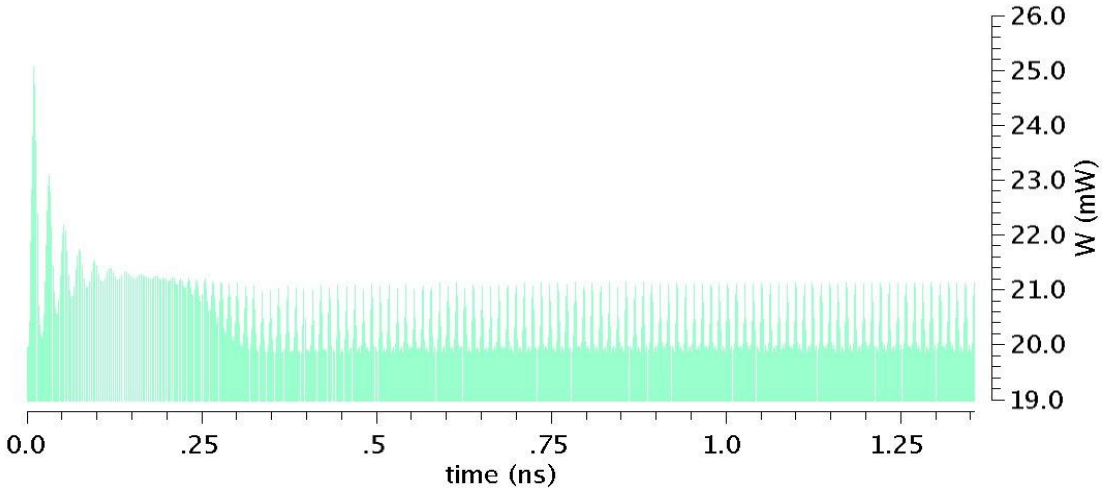


Fig. 4.5 Power response of the VCO when digital input to the Cbank=0000000

The average power consumed by the proposed VCO when the capacitor bank has digital input '0' for all varactors is 20.06 mW.

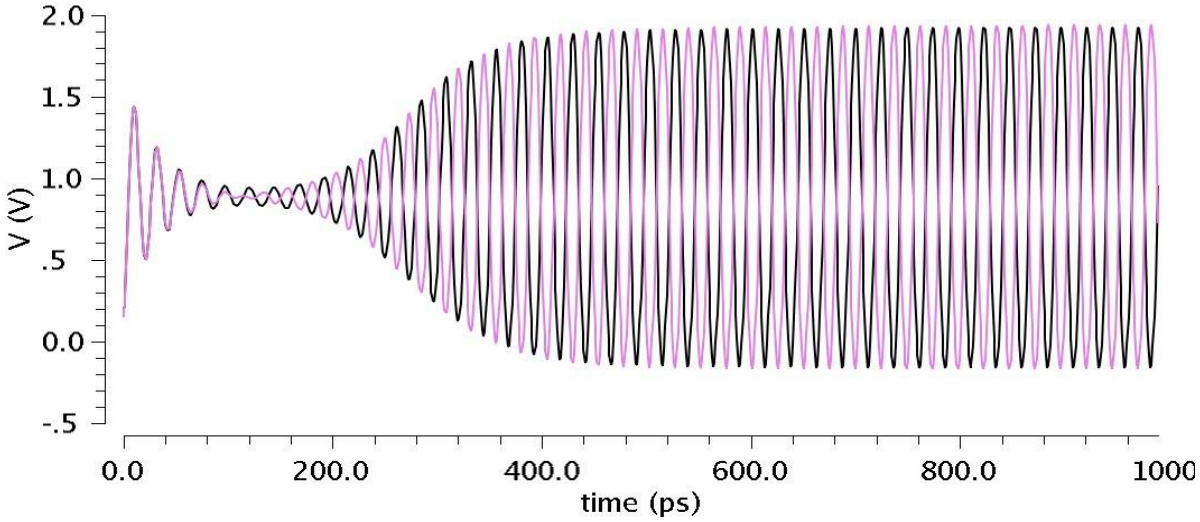


Fig. 4.6 Transient response with capacitor bank having digital input '0000001' showing the settling time

When one of the varactor pair is provided with the digital input '1' or voltage of 0.9 V, the frequency of oscillation of the VCO increases and the lock frequency achieved is 38.53 GHz with the settling time of less than 300 ps.

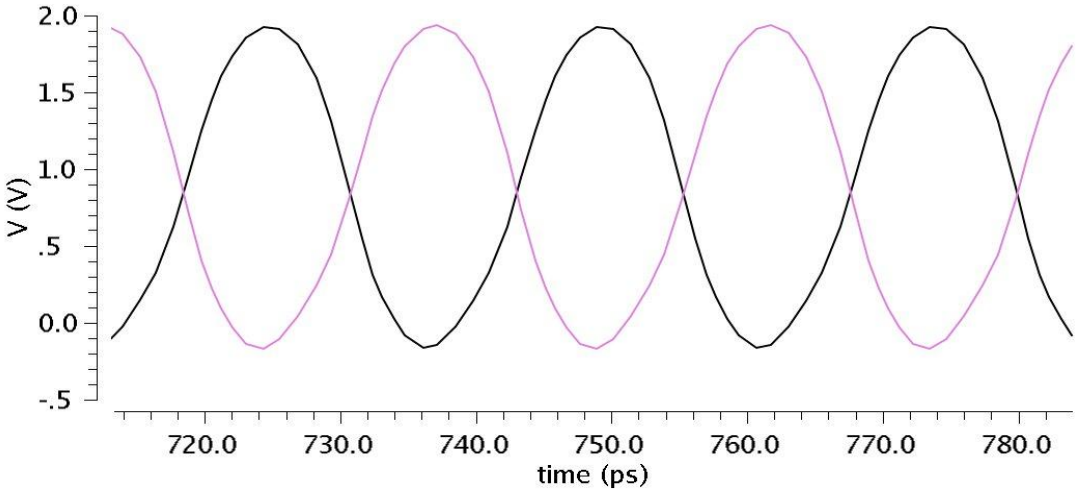


Fig. 4.7 Transient response with complementary out_plus and out_minus and capacitor bank input= '0000001'

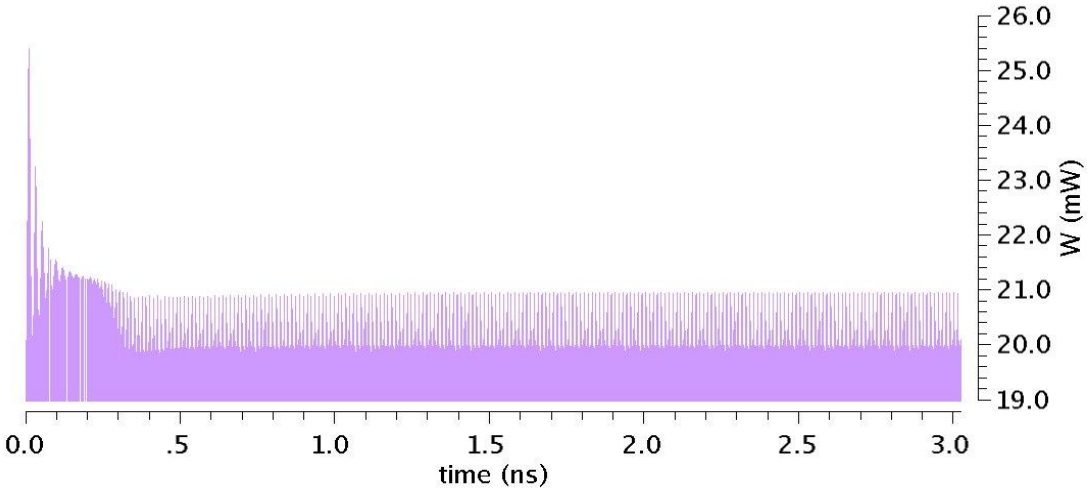


Fig. 4.8 Power response of the VCO when digital input to the Cbank= '0000001'

The power consumption by the VCO when one of the varactor pair has digital input '1' or the Cbank has the input '0000001' is 20.07 mW.

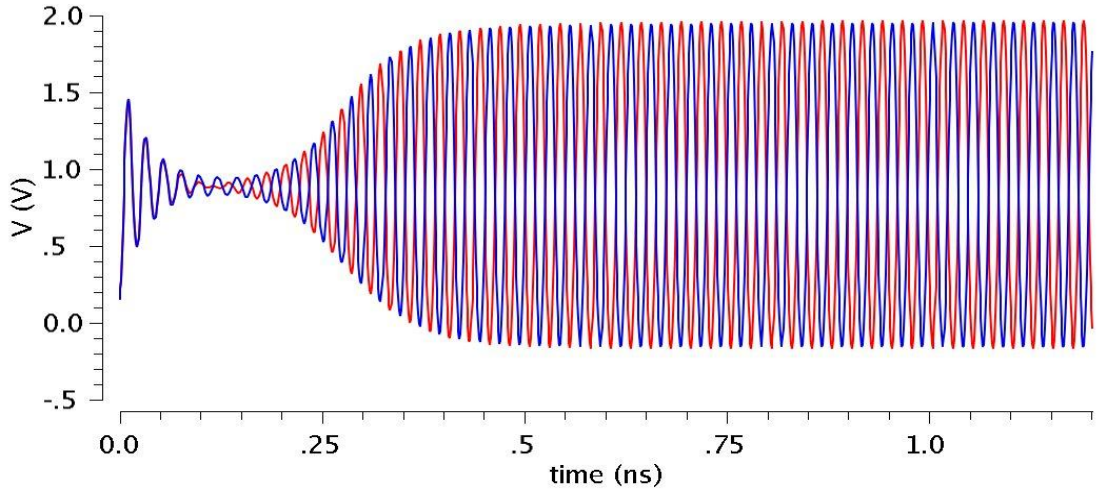


Fig. 4.9 Transient response with capacitor bank having digital input '0000011' showing the settling time

When two of the varactor pairs are provided with the digital input '1' or voltage of 0.9 V, the frequency of oscillation of the VCO increases and the lock frequency achieved is 38.86 GHz with the settling time of less than 0.33 ns.

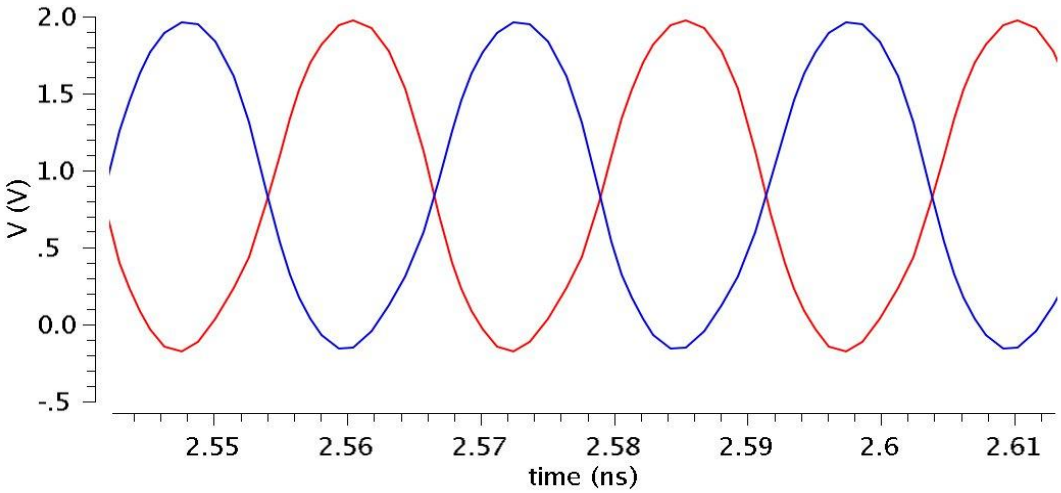


Fig. 4.10 Transient response with complementary out_plus and out_minus and capacitor bank input= '0000011'

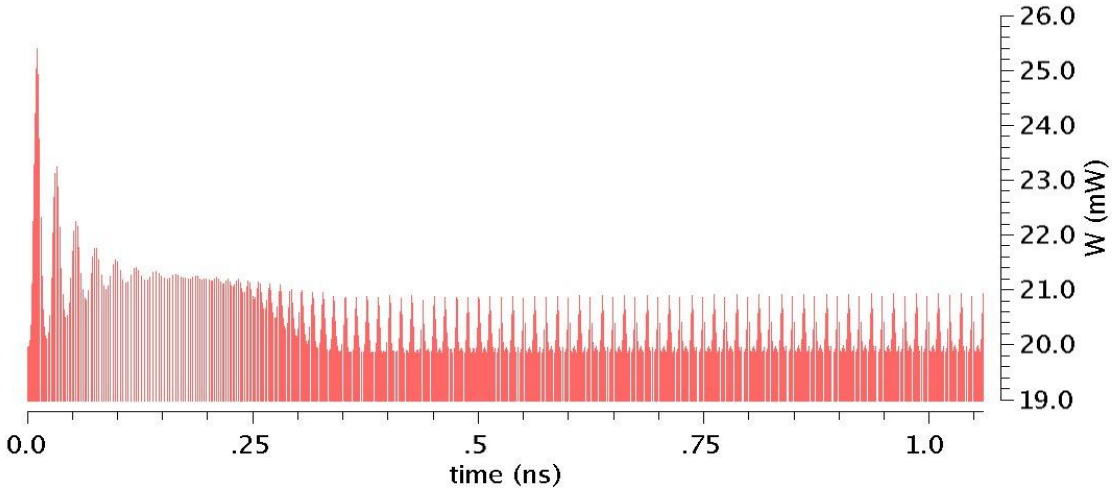


Fig. 4.11 Power response of the VCO when digital input to the Cbank= '0000011'

The average power consumption by the VCO when two of the varactor pairs having digital input '1' or the Cbank has the input '0000011' is 20.08 mW.

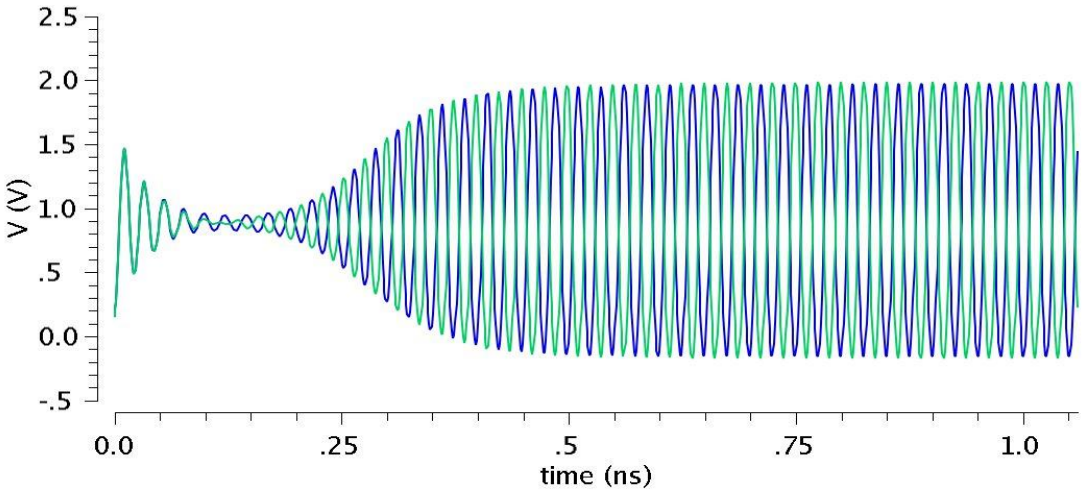


Fig. 4.12 Transient response with capacitor bank having digital input '0000111' showing the settling time

When three of the varactor pairs are provided with the digital input '1' or voltage of 0.9 V, the frequency of oscillation of the VCO increases and the lock frequency achieved is 39.27 GHz with the settling time of less than 0.33 ns.

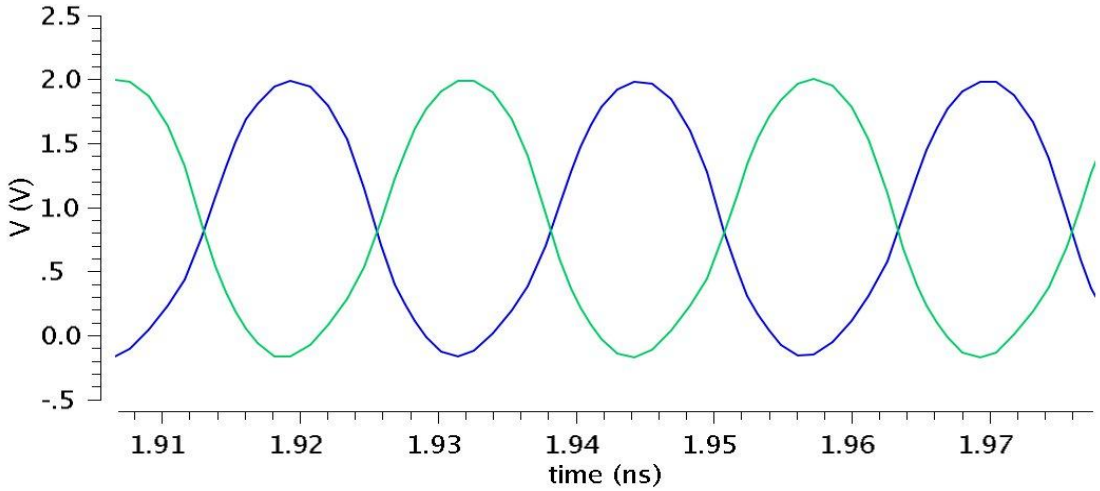


Fig. 4.13 Transient response with complementary out_plus and out_minus and capacitor bank input= '0000111'

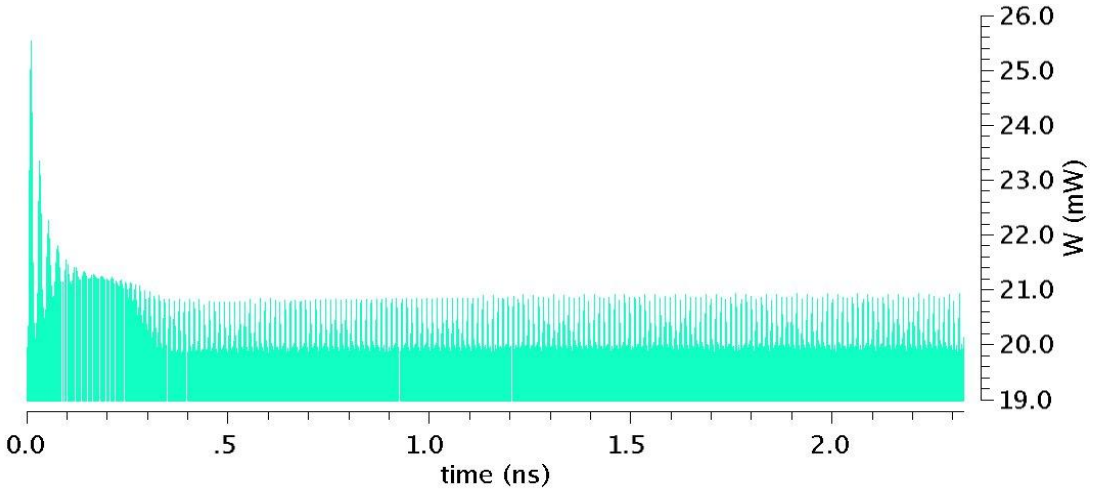


Fig. 4.14 Power response of the VCO when digital input to the Cbank= '0000111'

The power consumption by the VCO when one of the varactor pair has digital input '1' or the Cbank has the input '0000001' is 20.10 mW.

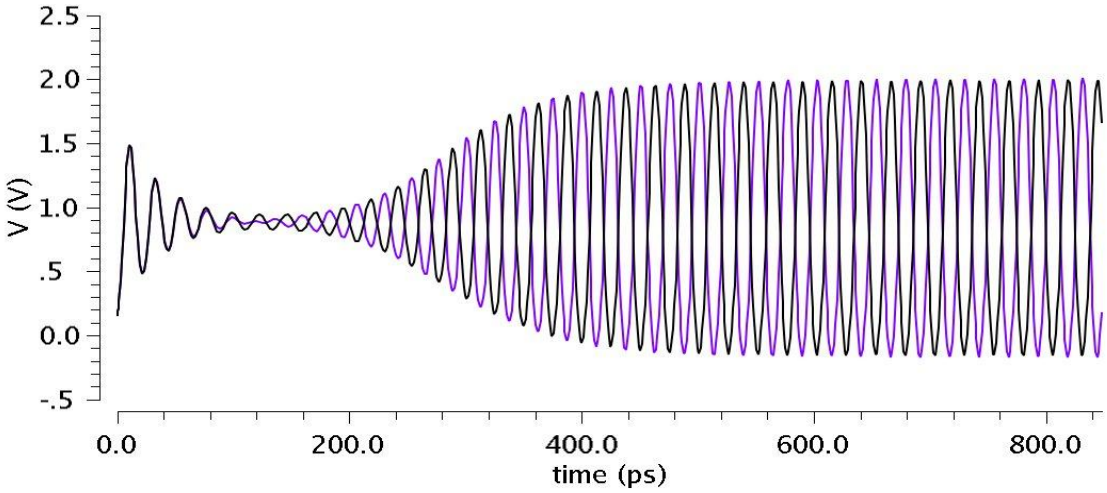


Fig. 4.15 Transient response with capacitor bank having digital input '0001111' showing the settling time

When four of the varactor pairs are provided with the digital input '1' or voltage of 0.9 V, the frequency of oscillation of the VCO increases and the lock frequency achieved is 39.70 GHz with the settling time of less than 0.33 ns.

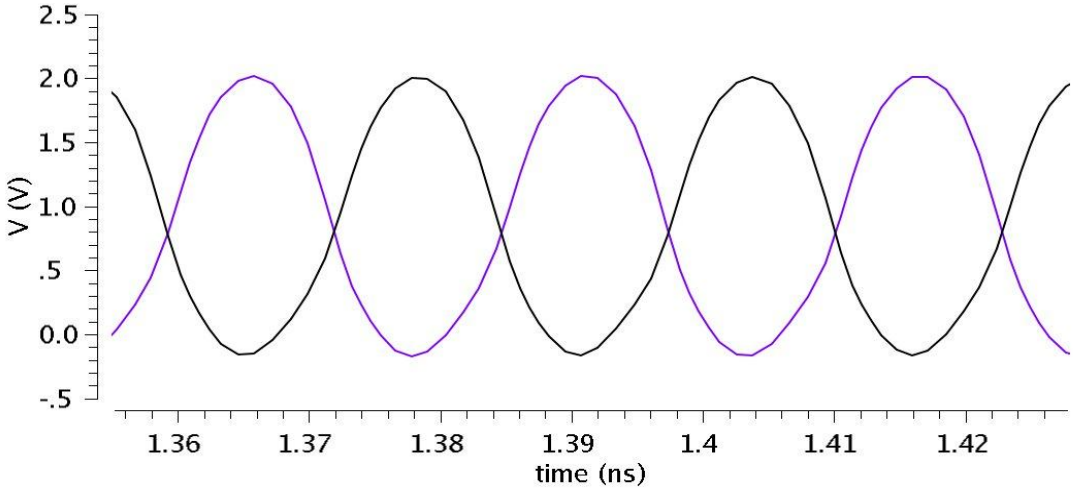


Fig. 4.16 Transient response with complementary out_plus and out_minus and capacitor bank input= '0001111'

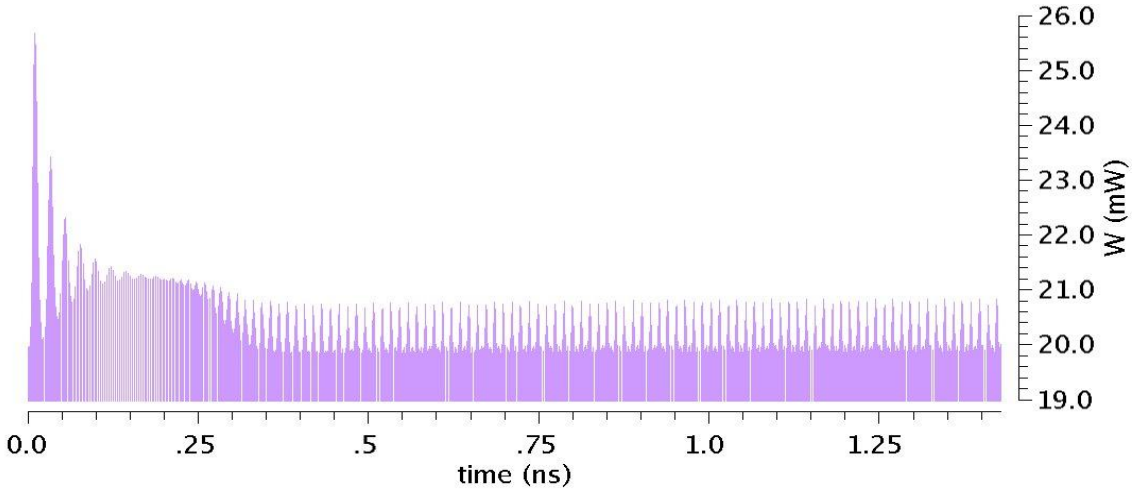


Fig. 4.17 Power response of the VCO when digital input to the Cbank = '0001111'

The power consumption by the VCO when one of the varactor pair has digital input '1' or the Cbank has the input '0000001' is 20.11 mW.

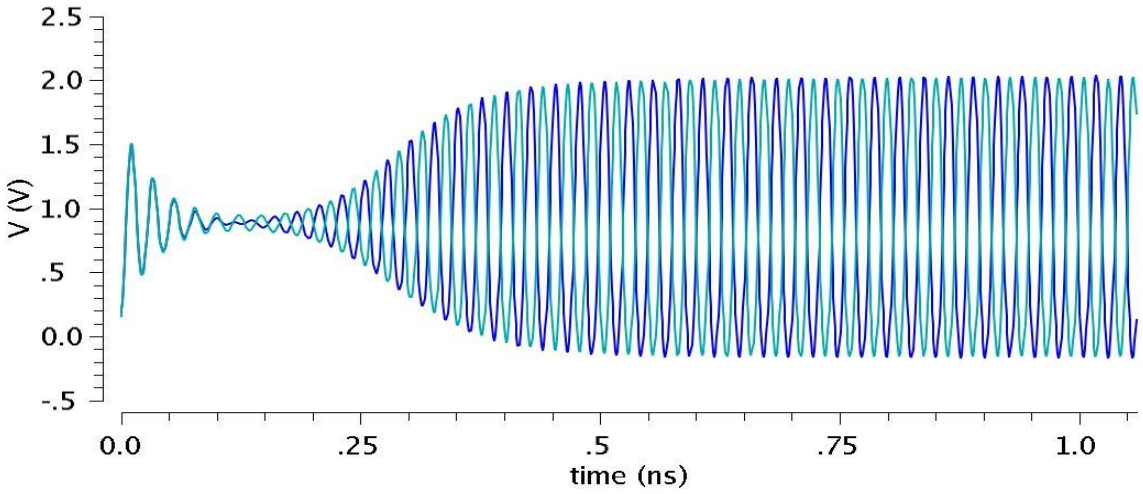


Fig. 4.18 Transient response with capacitor bank having digital input '0011111' showing the settling time

When five of the varactor pairs are provided with the digital input '1' or voltage of 0.9 V, the frequency of oscillation of the VCO increases and the lock frequency achieved is 40.14 GHz with the settling time of less than 0.33 ns.

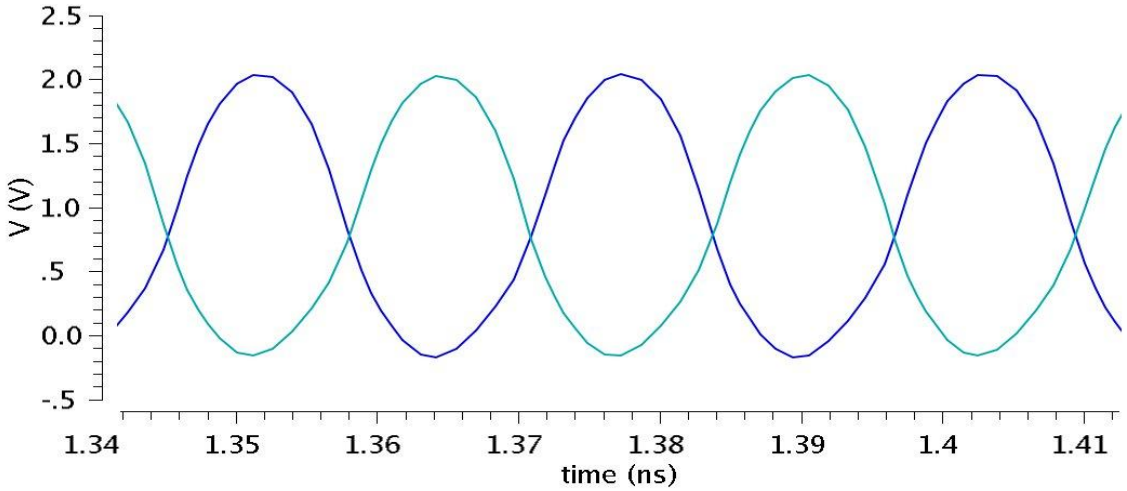


Fig. 4.19 Transient response with complementary out_plus and out_minus and capacitor bank input= '0011111'

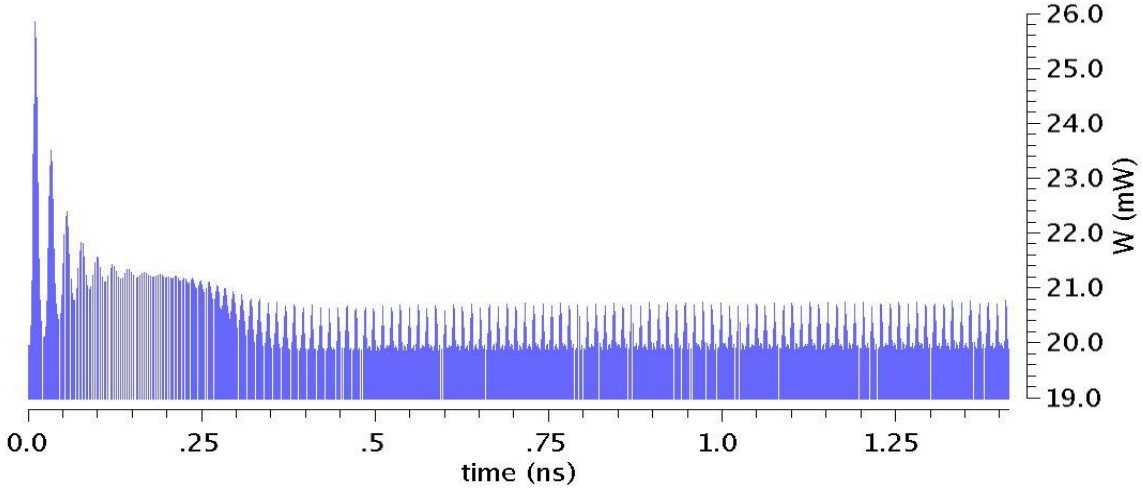


Fig. 4.20 Power response of the VCO when digital input to the Cbank= '0011111'

The power consumption by the VCO when one of the varactor pair has digital input '1' or the Cbank has the input '0000001' is 20.13 mW.

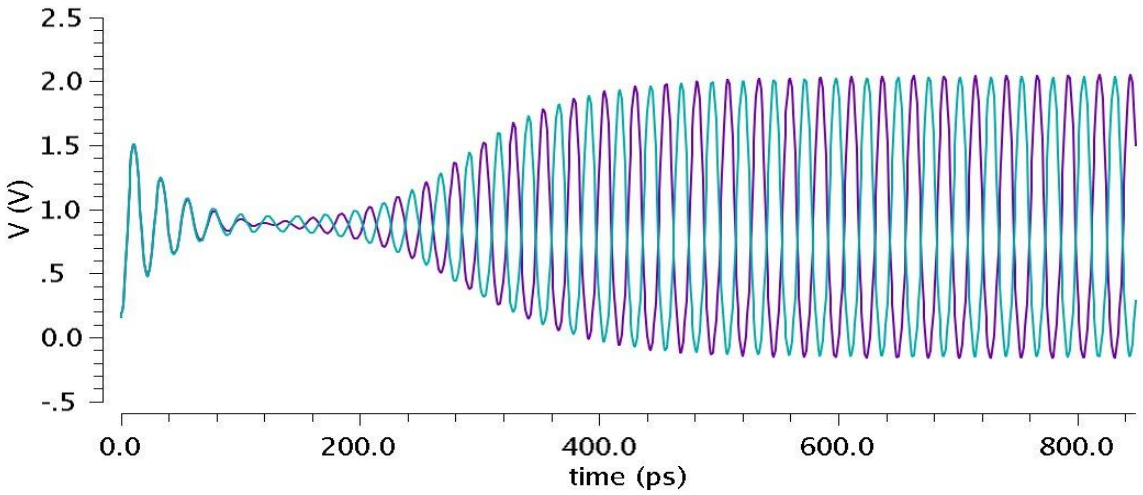


Fig. 4.21 Transient response with capacitor bank having digital input '0111111' showing the settling time

When six of the varactor pairs are provided with the digital input '1' or voltage of 0.9 V, the frequency of oscillation of the VCO increases and the lock frequency achieved is 40.63 GHz with the settling time of less than 0.33 ns.

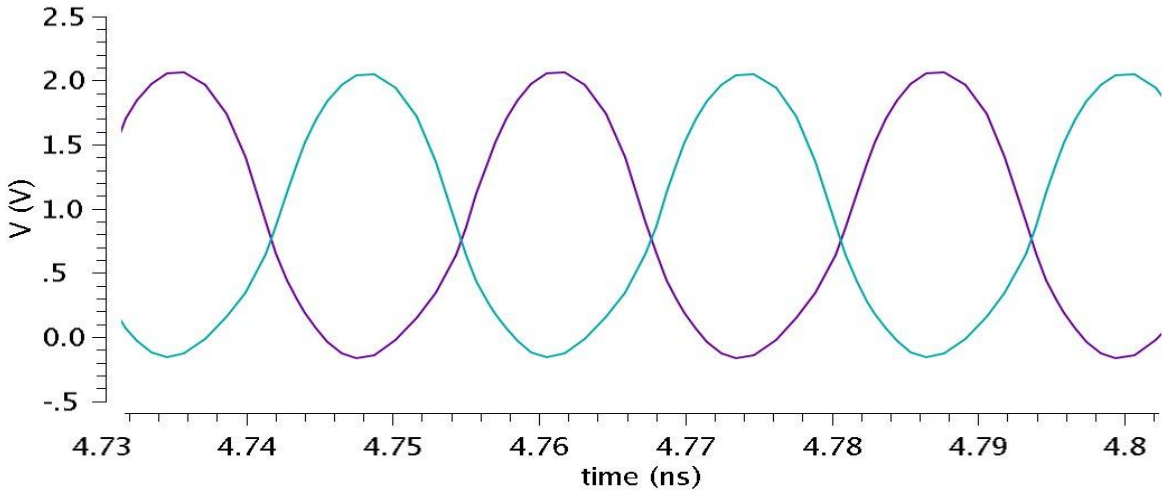


Fig. 4.22 Transient response with complementary out_plus and out_minus and capacitor bank input= '0111111'

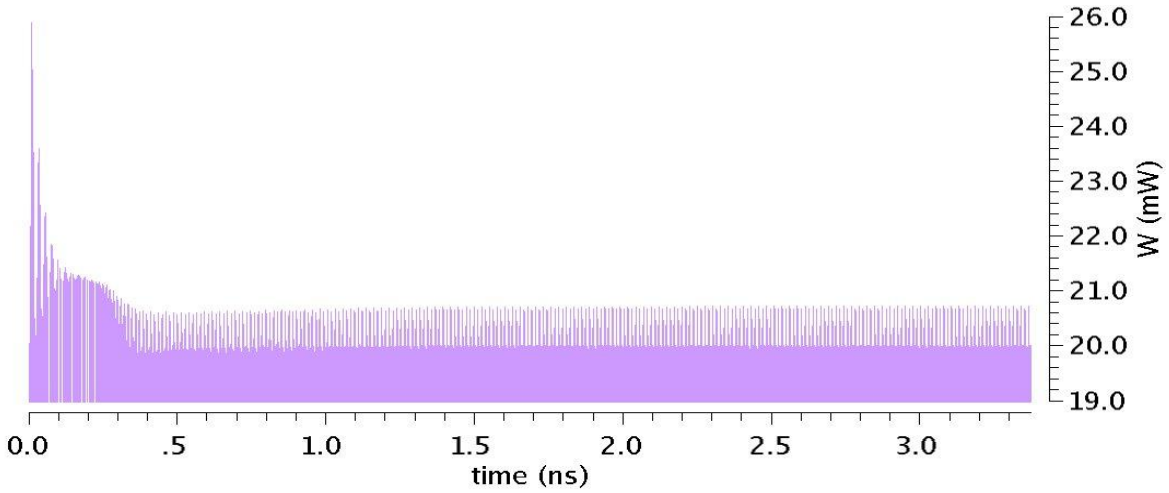


Fig. 4.23 Power response of the VCO when digital input to the Cbank= '0111111'

The power consumption by the VCO when one of the varactor pair has digital input '1' or the Cbank has the input '0000001' is 20.14 mW.

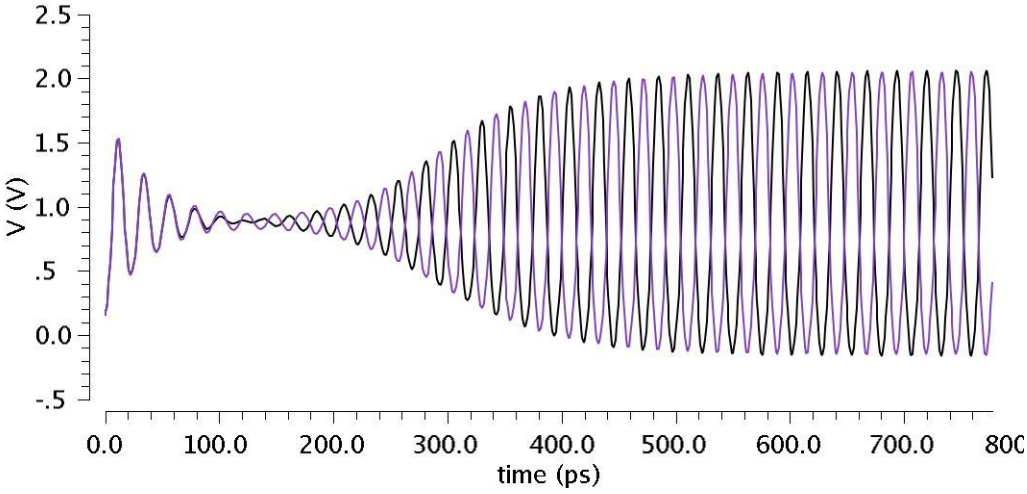


Fig. 4.24 Transient response with capacitor bank having digital input '1111111' showing the settling time

When all seven of the varactor pairs are provided with the digital input '1' or voltage of 0.9 V, the frequency of oscillation of the VCO increases and the lock frequency achieved is 40.91 GHz with the settling time of less than 300 ps.

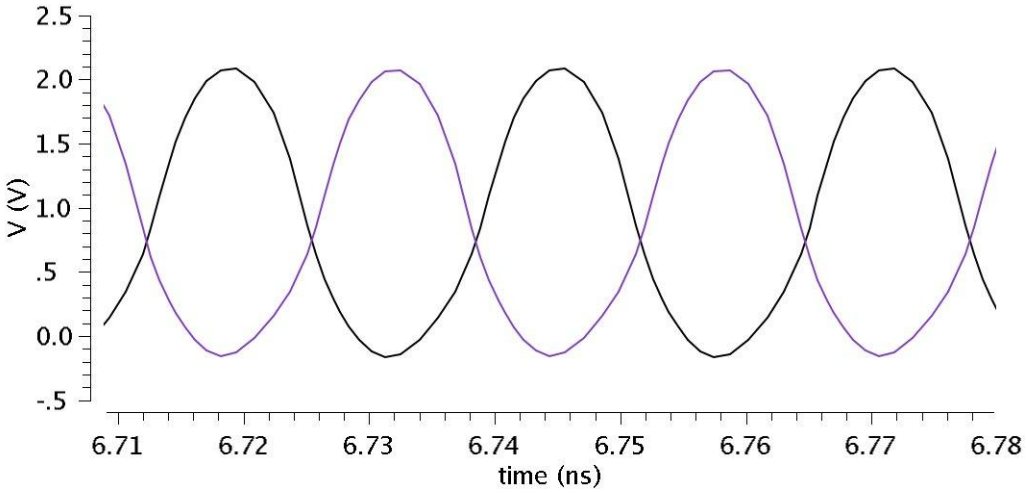


Fig. 4.25 Transient response with complementary out_plus and out_minus and capacitor bank input= '1111111'

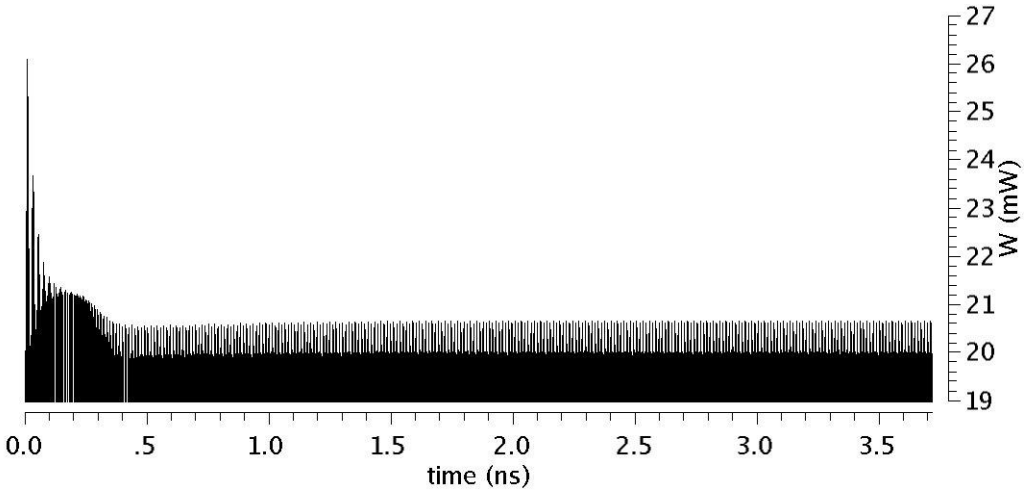


Fig. 4.26 Power response of the VCO when digital input to the Cbank= '1111111'

The power consumption by the VCO when one of the varactor pair has digital input '1' or the Cbank has the input '0000001' is 20.16 mW.

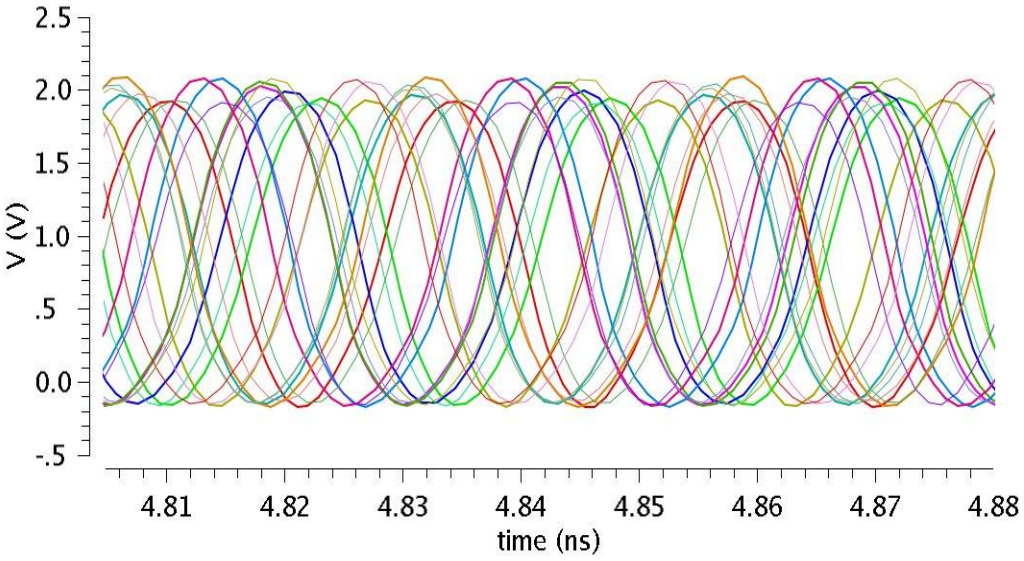


Fig. 4.27 Parametric analysis plot showing different frequency plots

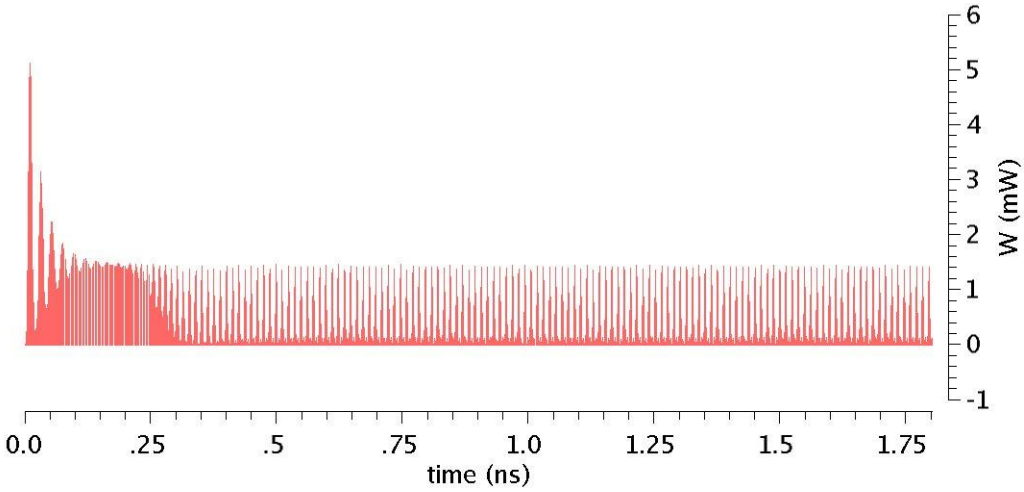


Fig. 4.28 Power response of the VCO with passive inductor

In the proposed VCO, the active inductor was replaced with the conventional inductor and the transient response was seen. It is observed that with the same value of inductor i.e. 401.75 pH, the VCO circuit was able to produce and lock all the frequencies that were obtained in the proposed circuit but the power factor for the one with passive one consumed lesser power. The power consumed by the LC voltage controlled oscillator with the passive conventional inductor came out to be 0.45 mW.

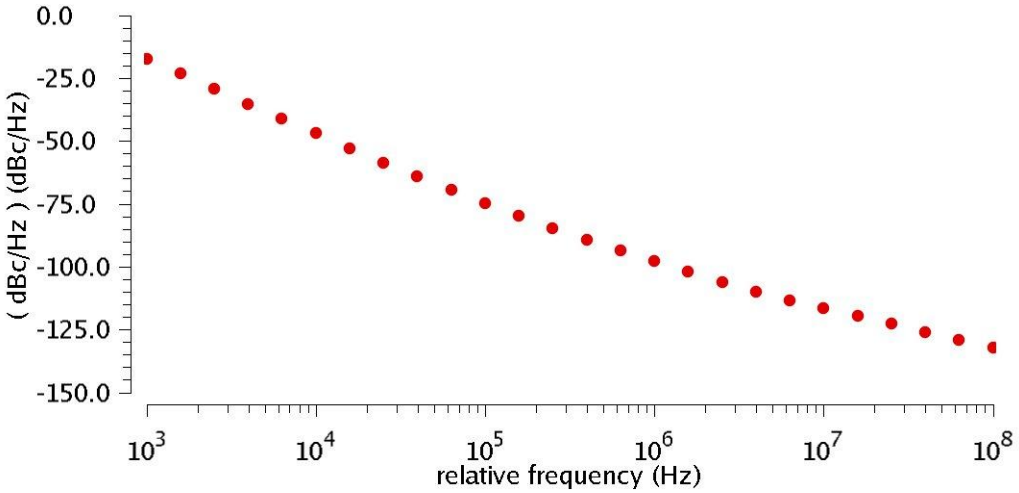


Fig. 4.29 Phase noise performance plot for the LC VCO with passive inductor

The LC- voltage controlled oscillator with the passive inductor has the phase noise plot as shown in the figure. The phase noise performance comes out to be -97.5 dBc/Hz at 1 MHz offset which is much better than the VCO with active inductor. The proposed VCO with active inductor has the phase noise performance of -78.8 dBc/Hz at 1 MHz offset.

Table 4.1: Comparison table of the specifications obtained for present work and ref[11]

	Reference [11]	This work (active inductor)	This work (passive inductor)
Technology	180 nm CMOS	90 nm CMOS	90 nm CMOS
Power Supply	1.8 V	0.9 V	0.9 V
Power Dissipation	29.1 mW	20 mW	0.45 mW
Frequency Range	3.8 GHz ~ 7.4 GHz	38.15 GHz ~ 41.9 GHz	38.15 GHz ~ 41.9 GHz
Phase Noise	-75.42 ~ -92.05 dBc/Hz at 1 MHz offset	-78.8 dBc/Hz at 1 MHz offset	-97.8 dBc/Hz at 1 MHz offset

The tuning voltage for the IMOS varactors was made to vary from 0 to 0.9 V with the help of parametric analysis and following results were obtained.

Table 4.2: Tuning voltage and the corresponding frequency obtained for the proposed VCO

Voltage (volts)	Frequency (GHz)
0	38.15
0.1	38.50
0.2	38.87
0.3	39.30
0.4	39.72
0.5	40.11
0.6	40.52
0.7	40.81
0.8	41.52
0.9	41.91

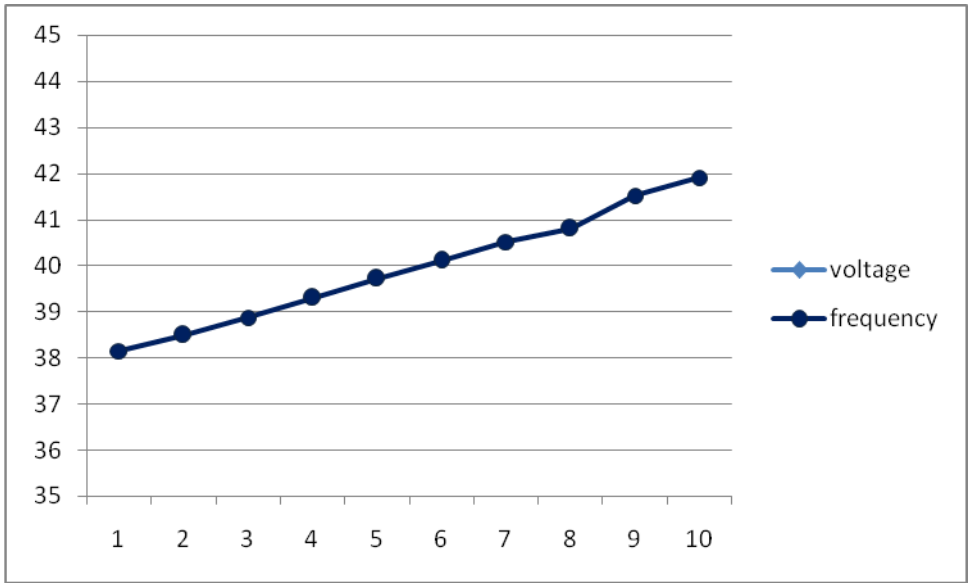


Fig. 4.30 Tuning voltage Versus frequency plot for the proposed VCO

CHAPTER 5
CONCLUSION AND FUTURE WORK

Due to the rapid developments of various systems that have different operating frequencies, it becomes the need of the hour that a single oscillator is capable of tuning at wide range of carrier frequencies. At the same time the oscillator must fulfill the requirements of having low phase noise, lesser power consumption and it must permit full on-chip integration within the least possible area. Some of these requirements exhibit trade-offs. S due to this reason, it is mandatory to study various solutions that can contribute to the robust and versatile design of voltage controlled oscillators.

One such technique involves the use of active inductors that although have limited performance in comparison to passive LC based VCOs, allow for a high degree of circuit integration.

For ultra wide band RF systems, a wide frequency tuning range of an LC VCO is required. By using switched capacitors and switched inductors, tuning range of wide frequency can be obtained. The disadvantages are enlarging the chip area and complexity of control mechanism. By using inductorless circuit which tend to chip area, we wish to fabricate the circuit with no physical inductor present on the chip or in a way, using simulated inductor.

The proposed design of Voltage Controlled Oscillator achieves the centre frequency of 40 GHz with a range varying from 38.15 GHz to 41.9 GHz frequency. Both the design with and without passive inductor have been simulated. The frequency is obtained in 90 nm CMOS technology for ultra wideband applications especially for Ka band without using any practical inductor thus reducing the chip area.

The proposed VCO with active simulated inductor and IMOS varactors achieves the phase noise performance of -78.8 dBc/Hz at 1 MHz offset while the design with passive inductor is capable of achieving -98.5 dBc/Hz at the same offset. Although the power consumed by the

inductor-less VCO is 20 mW and by the one with passive inductor is 0.45mW, however the chip area of the former is drastically reduced in comparison to the latter.

Hence, the present design can be still improved by further decreasing the power dissipated by the circuit. Since the need of the hour is to minimize the power consumption as well as the chip area. There exists a trade-off between them. Further techniques can be used to minimize the power consumed keeping the area of the chip lesser.

REFERENCES

[1] Robert M. O Leary, Kevin G. McCarthy, "IC design of area efficient Voltage Controlled Oscillators for UWB wireless systems in 0.18 um CMOS*", ISSC, Maynooth*, June 2012

[2] Chien-Hsuan Liu, Chia-Yo Chan, Ruey-Lue Wang, and Yun-Kuin Su, "Low Power Current-reused Voltage-Controlled Oscillator with Optimum Source Damping Resistors". *IEEE Radio frequency Integrated circuits Symposium,* pp. 399-402, Sept. 2007

[3] S.Zafar, T.Z.A Zulkifli and M.Awan, "Design of Voltage Controlled Oscillator (VCO) for ultra wide band (UWB) CMOS frequency synthesizer", *IEEE International Conference on Intelligent and Advanced systems*, 2007.

[4] N.C Shirazi, Ebrahim Abiri and R. Hemzehyan, "A 5.5 GHz Voltage Controlled Oscillator (VCO) with differential tunable active and passive inductor", *International Joural of Information and Electronics Engineering,* Vol. 3,No. 5,Sept. 2013.

[5] Jongsik Kim, Jaewook Shin,Seungsoo Kin, Hyunchol Shin," A wideband CMOS LC VCO with linearised coarse tuning characteristics", 2008

[6] D.S Jayalalitha and D. Susan," Grounded simulated inductor – A Review", Middle East Journal of Scientific Research", 278-286, *ISSN*, 2013

[7.] Liang-Hung Lu, Hsieh-Hung Hsieh and Yu-Te Liao,"A Wide Tuning-Range CMOS VCO With a Differential Tunable Active Inductor", *IEEE Transactions on Microwave Theory and Techniques,* VOL. 54, NO. 9, SEPTEMBER 2006

[8] Behzad Razavi, "Design of Analog CMOS integrated Circuits", McGraw Hill Education (India) Edition 2002.

[9] Yoon, Sangwoong,*"* LC-tank CMOS voltage-controlled oscillators using high quality inductors embedded in advanced packaging technologies", PhD Thesis, GEORGIA INSTITUTE OF TECHNOLOGY, 2004.

[10] C.-C. Ho, C.-W. Kuo, C.-C. Hsiao, Y.-J. Chan, "A 2.4 GHz low phase noise VCO fabricated by 0.18um pMOS technologies". *Proc. of IEEE Int. Symp. VLSI Tech*., pp 144-146, 2003.

[11] C. P. Yue and S. S. Wong, "On-chip spiral inductors with patterned ground shields for Si-based RF ICs," *IEEE J. Solid-State Circuits*, vol. 33, pp. 743-52, May 1998.

[12] Fei Yuan, CMOS Active Inductors and Transformers-Principle, Implementation, and Applications, Springer *(2008)*

[13] J. Lu, N.-Y. Wang and M.-C.F. Chang, "14.6–22.2 GHz LC-VCO in 65 nm CMOS technology for wideband applications", Vol. 47 No. 6 , *Electronics Letters* 17th March 2011

[14] J.J. Kim et al. "Ultra-wideband CMOS voltage-controlled oscillator with reconfigurable tunable inductors". *Electronics Letters*, Vol. 47, No. 4, 2011

[15] Chein – Cheng Wei et al., "An Ultra-Wideband CMOS VCO with 3-5GHz Tuning Range". *IEEE International Workshop on Radio frequency Integration Technology*, 2005

[16] M. Mehrabian et al., "A 4~7GHz Ultra Wideband VCO with Tunable Active Inductor". *Proceedings of the 2008 IEEE International Conference on Ultra- Wideband*, Vol. 2, pp. 21-24, 2008

[17] Yen Sung Michael et al., "A 10Gb/s Active-Inductor Structure with Peaking control in 90nm CMOS".*IEEE Asian Solid State Circuit Conference*, November 2008

[18] R. L. Bunch and S. Raman, "Large-signal analysis of mos varactors in mos− g_m LC VCOs". *IEEE Solide-State Circuit*, August 2003.

[19] LI Xian et al., “A Wide Tuning Range LC-VCO Using Switched Capacitor Array Technique”. Proceedings of International Symposium on Signals, Systems and Electronics, Vol. 1, pp. 1-4, 2010

[20] Jongsik Kim et al., “A Wide-Band CMOS *LC* VCO with Linearized Coarse Tuning Characteristics”. *IEEE Transactions on Circuits and Systems*, Vol. 55, No. 5, pp. 399-403, May 2008