Implementation of Voltage Controlled Ring Oscillator with improvement in Delay reduction

THESIS REPORT

(Dissertation-II, Month: January-May)

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To

Department of ECE

Lovely School of Technologies and Science

Lovely Professional University, Phagwara

In partial fulfilment of the Requirement for the

Award of the Degree of

Master of Technology in Electronics and Communication Engineering

Under the Guidance of

Advisor

Dr Ravi Shankar Mishra

(May, 2015)

CERTIFICATE

This is to certify that Rishu Bhabra has completed dissertation in Master of Technology, titled "*Implementation of Voltage Controlled Ring Oscillator with improvement in Delay reduction*" under my guidance and supervision. To the best of my knowledge, the present work is the result of her original investigation and study. No part of the dissertation has ever been submitted for any other degree or diploma. The dissertation is fit for the submission and the partial fulfilment of the conditions for the award of Master of Technology in Electronics and Communication Engineering.

Date: 2nd May, 2015 Signature of Advisor

(Dr Ravi Shankar Mishra)

DECLARATION

I, Rishu Bhabra, student of B.tech-M.tech (Dual degree) under ECE Discipline at Lovely Professional University, Punjab, hereby declare that all the information mentioned in this Dissertation-II report is based on my own intensive work and is genuine. This report is not copied and also not taken from anywhere.

Date: 2nd May, 2015 Signature:

Rishu (11001692)

ACKNOWLEDGMENT

Gratitude cannot be expressed with just words. It can only be felt in heart. Often words are inadequate to serve as a model of expression of one's feeling, specially the sense of indebtedness and gratitude to all those who help us in our duty.

It is of immense pleasure and profound privilege to express our gratitude and indebtedness along with sincere thanks to my mentor Dr Ravi Shankar Mishra for providing me the guidance to work for a dissertation report on "*Implementation of Voltage Controlled Ring Oscillator with improvement in Delay reduction*"..

I also want to thanks Lovely Professional University for providing the Laboratories to work and granted the permission to work day and night which helps me in completing my work.

I formally acknowledge my sincerest gratitude to all those who assisted and guided me in completing this thesis report

Rishu

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ABSTRACT

In communication system, phase-locked loops (PLL) are widely used. It helps in keeping everything in order and synchronised. PLLs are extensively used in frequency synthesizer and clock recovery circuits. The most crucial component of PLL is Voltage Controlled Oscillator (VCO) as it provides the output of a PLL. In the present work, different ring VCO topologies and architectures are designed for improving the performance from the conventional VCO structure. A single-ended ring VCO is designed and implemented at different control voltages. The output frequency range observed is 3.27-12.57GHz with control voltage ranges 1V to 0.5V. The minimum delay measured is 17.8picosecond. The other architecture involves Reverse Substrate-Bias (SB) technique for the improvement in performance of the VCO. The third topology considered is differential structure for further improvement in the performance parameters of the VCO. All the topologies are designed in Cadence Virtuoso with gpdk90nm technology so a comparison is made on the same ground. The characterisation is done on the parameters including delay, power consumption and frequency. The Differential structure and reverse SB structure results in the frequency range of 17.405GHz-10.982GHz and 11.87GHz-13.77GHz, respectively. The simulation show minimum delay of 8.1picosecond for differential configuration and 8.27picosecond for reverse-substrate bias technique. The measured power consumption for differential configuration 62.42 μW whereas, for substrate-bias structure the value is measured to be 32.96 μW.

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CHAPTER 1

INTRODUCTION

In many electronic devices and systems, oscillators act as an integral part. From clock generation to carrier synthesis, we require vast different topologies for different applications and also different performance parameters. The applications of oscillators' ranges from microprocessors in embedded to cellular telephones in communications. Therefore, oscillator found its uses in almost every field of technology. For such different applications we need robust and high-performance oscillators. To achieve these requirements many interesting challenges are need to be overcome. Since the topologies for different applications are different therefore challenges faced are also varied [1].

We have various topologies to implement the VCO. The two popular topologies are: LC-tank oscillator and Ring Oscillator. Both of the topologies have their own advantages and disadvantages over each other. The LC oscillator shows minimum phase noise because of the resonating structure, whereas, ring oscillators are more prone to phase noise. The advantage of ring oscillator over LC is that the integration of ring oscillator using CMOS technology is much easier than that of LC-oscillator. In this thesis work we are using mainly ring VCO because of its easy implementation using CMOS technology and of their minimum area requirement. The ring VCO can be further improved by adding various circuits and applying various techniques to the topology. Number of research has been done and is still going on to improve the frequency response, lower the power consumption, phase noise and jitter in the VCO. Therefore, the scope in this area for research work is wide enough.

1.1 Basic Voltage Controlled Oscillator:

There are many integrated circuits we can use to generate a periodic output signal, but oscillators design is one area in which discrete transistors has a marked advantage. Oscillator provides high-frequency, low-noise oscillations which are required in communication circuits. Various oscillators are available. The circuit with a periodic output but no periodic input are electronic oscillators. If the output signal is sinusoidal then the oscillator is harmonic oscillator. There are oscillators in which crystal resonator is used to control the oscillation frequency, known as crystal controlled oscillators. The oscillators in which voltage is used to control the oscillation frequency are known as Voltage Controlled Oscillators.

Figure 1.1 shows the basic VCO system. The block diagram contains the necessary components of an oscillator [2]:

1. Amplifier with frequency-dependent forward loop gain G($j\omega$)
2. Frequency dependent feedback network h($j\omega$).
3. The output voltage is given as

$$V_0 = \frac{V_i G(j\omega)}{1+G(j\omega)H(j\omega)} \tag{1.1}$$

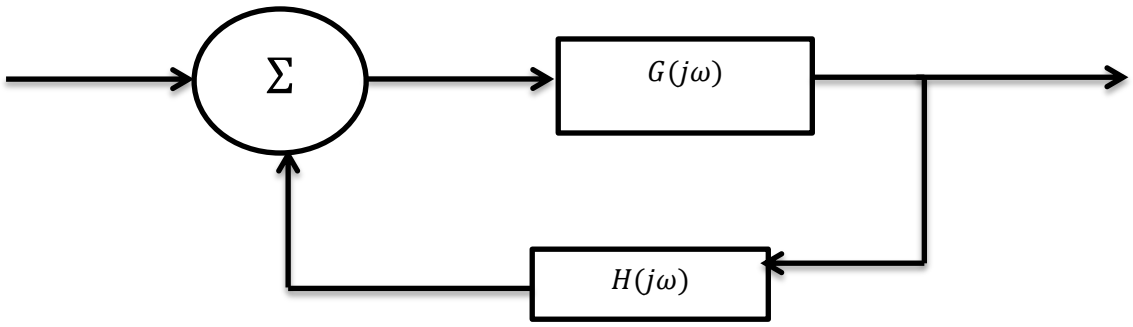


Fig 1.1: Basic structure of Oscillator

Now, for an oscillator, output voltage is non-zero even if the input signal is zero. Therefore, the denominator is

$$1 + G(j\omega)H(j\omega) = 0 \tag{1.2}$$

Therefore, the magnitude of the open-loop transfer function is

$$G(j\omega_0)H(j\omega_0) = -1 \tag{1.3}$$

$$|G(j\omega_0)H(j\omega_0)| = 1 \tag{1.4}$$

And the phase shift

$$\arg G(j\omega_0)H(j\omega_0) = 180^0 \tag{1.5}$$

The conditions for stability are also known as "Barkhausan criteria".

Barkhausan criteria: It states that, if

$$\frac{V_0}{V_i} = \frac{\mu}{1-\mu B} \tag{1.6}$$

Then system will oscillate if, μβ=1.

1.2 Different Architectures:

Single-loop architecture: It comprises of the odd number of inverter chains, in which output of one inverter stage is given as the input to the preceding inverter stage. The output of the final inverter is again feedback to the first inverter stage. This type of inverter is used in the study in [10], where 9-stages are designed of such inverters and also used in [13]. A single ended ring VCO is shown in Figure 1.2.

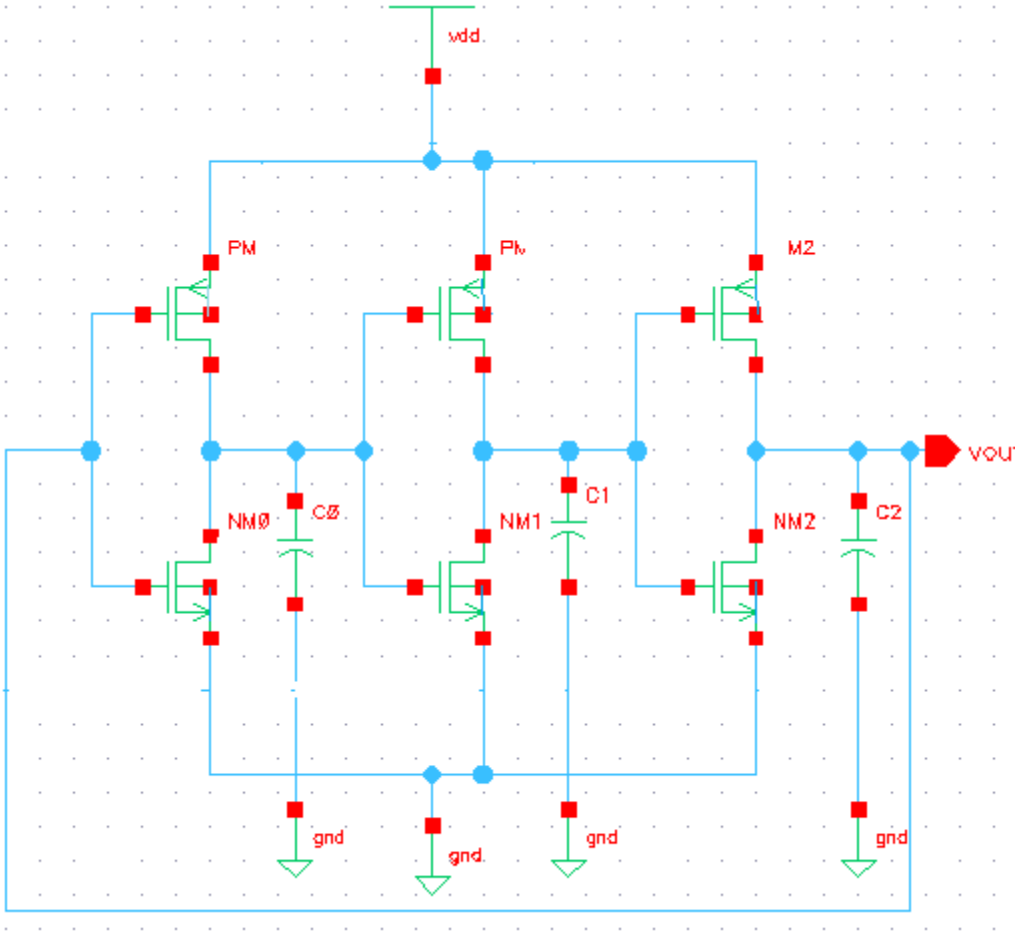


Fig 1.2: single-ended ring VCO

This architecture is more beneficial and is commonly used as compared to LC-tank oscillator because of its various advantages over LC oscillators such as, wide tuning range, low power consumption and low area required.

Multiple-pass loop architecture: It comprises multiple inputs which utilizes the skewed delay scheme [13]. This architecture is more beneficial than the single loop as multiple-pass VCO as noise performance is improved and power consumption also reduced to very low level.

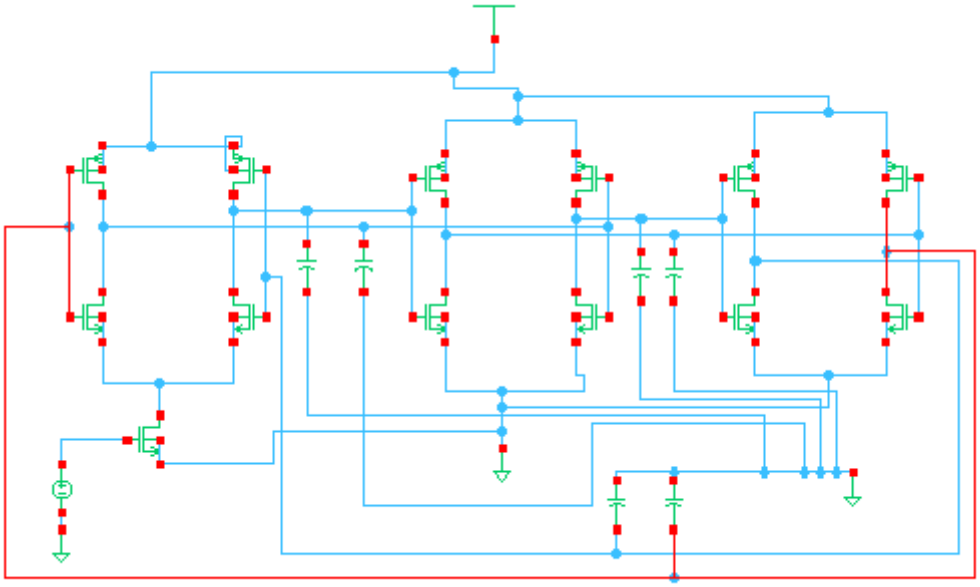


Fig 1.3: basic differential VCO

Various configurations of differential pair is used to design a single delay stage. We have different types of delay stages:

- Differential pair with diode connected loads paralleled with adjustable current sources[14]
- Differential pair with Source-coupled delay cell[3]
- Differential pair with Cross-coupled delay cell[3], [12]
- Dual-inverter delay cell.[3]
- Basic differential delay cell[9]

1.3 VCO Parameters:

A good VCO is one which has low power consumption, low phase noise, delay of each stage is less, low jitter and a wide range of frequencies. These parameters decides whether a VCO can be acceptable for any application or not. The basic idea about the parameters of the VCO is given below:

Phase Noise: Phase noise is the random fluctuation caused by jitter in the frequency domain and is represented as :

$$L\{\Delta f\} = \frac{8KTV_{DD}f_{osc}^2}{3\eta P_{avg}V_{char}\Delta f^2} \quad (1.7)$$

The above equation represents the phase noise as mentioned in [10].

Delay: delay basically refers to as the time taken for the signal to propagate from input to output. Delay is inversely proportional to the centre frequency, therefore, for high frequency range the delay should be as minimum as possible.

$$f_{osc} = \frac{1}{N(\tau_{rise}+\tau_{fall})} \quad (1.8)$$

The above equation describes the relation between delay and oscillation frequency as given in [7].

Power: power consumption depends on the control voltage given to the circuit. More the voltage is supplied, more power will be consumed. Ring VCO generally consumes less power as it consumes power during switching events only.

$$P_{avg} = C_{load}.V_{DD}^2.f_{osc} \quad [7] \quad (1.9)$$

Jitter: jitters are the undesired factors caused by electromagnetic interferences. Other reason includes the crosstalk with other signals[10]. There are two types of jitter:

- Period jitter
- Cycle-to-cycle jitter

Tuning range: The tuning range gives the approximate bandwidth in which the frequency of the oscillator oscillates. The ring VCOs generally have wide frequency ranges starting from several MHz to GHz. Hence they are used in many applications in communication systems.

1.4 Applications in different fields:

1) The oscillators are mainly used as one of the module in Phase Locked-Loops. The PLLs helps in keeping everything in order and synchronised. The task of phase-locked loop is to regenerate the data with low noise information from an NRZ data signal. The basic building block in PLL performing this function of keeping everything synchronised is Voltage Control Oscillator. VCO is also known as the core of the PLL device. Whenever we need to improve the power consumption or phase noise or any other parameter, we simply do some modifications in VCO block [2].

2) In wireless communication, due to rapid growth high performance of the radio frequency components is required; therefore, highly efficient VCOs are used to achieve the desired goal.

3) In designing of X-band frequency synthesizer for Radar applications [16].

4) Voltage-Controlled Ring Oscillators are used in implantable electronics operating in the Medical Implant Communication Service (MICS) [13].

5) For clock control, synchronisation and data recovery in high speed systems, VCO acts as the crucial element [15].

6) Frequency synthesizer is one of the key block in communication system, which is implemented using PLL [4].

1.5 Comparison of Ring VCO and LC-Tank VCO:

RING VCO	LC-TANK VCO
1. The phase-noise for ring oscillator is much larger than that of LC design.	1. LC design has better phase-noise and frequency performance.
2. Ring Oscillators do not have high quality factor (Q-factor).	2. A large quality factor (Q-factor) is achievable with resonant networks.
3. A wide tuning range can be achieved using Ring topology.	3. LC-tank has Narrow tuning range.
4. The ring oscillator comprises only of NMOS and PMOS transistors therefore it can be fabricated in a single chip. Hence, less die area is needed for its fabrication.	4. More area is to be required to design the LC oscillator for fabricating the inductors and capacitors outside the chip area.
5. Easily integrated using CMOS technology.	5. Integration is tough as it does not scale well with technology.

Table 1.1: Comparison of Ring VCO and LC-Tank VCO

As seen from the table, the ring oscillator is mostly more advantageous as compared to LC-oscillators. Therefore, the main work in this report is based on the ring topology. The conventional ring VCO structure is implemented and a technique is implemented on it for improving the performance parameters. The tool used for this work is Cadence Virtuoso and technology used is gpdk90nm.

1.6 Thesis Outline:

The second chapter covers the literature review in which the study on voltage controlled oscillator is discussed. In chapter third, the scope and objective of the thesis work is mentioned. It describes the aim of the work and research to be done on the VCO. In the fourth chapter, design methodology is defined for the problem. Fifth chapter carries the implementation part. In this chapter, the implementation of the proposed design is carried out and the responses are noted for the same. Sixth chapter comprises the results and discussion. Comparison is carried out in this chapter showing the validation of the results obtained. Finally, the seventh chapter concludes the overall conclusion of the work done.

CHAPTER 2

LITERATURE REVIEW

In this chapter various topologies and techniques are described and the work done on them is reviewed. For different applications we need robust and high-performance oscillators. For an ideal voltage controlled oscillator, we require low power consumption, low power supply, high speed and minimum area. To achieve these requirements many interesting challenges are need to be overcome. Since the topologies for different applications are different therefore challenges to be faced are also varied [1]. VCO's structure can enhance its performance by increasing its frequency from few GHz to greater than 10 GHz, improving its tuning range, reduction in delay and low power consumption**.**

Hai Qi Liu, L et al. (2008) A three-stage multi-loop architecture is utilised to achieve high operational frequency [16]. Different types of delay cells had been reviewed and analysed in this study. The main objective is to reduce the delay of each stage so as to get higher frequency range. In this design a push-pull inverter is adopted and used as secondary input to reduce the high to low and low to high propagation delays. The supply voltage given in this circuit is 1.8 V and control voltage value is changed from 1.3 V to 0.3 V. the operational frequency achieved in this study is 7GHz. the speed and phase noise is improved by this architecture.

Yalchin Alper Eken, J. et al. (2004) This paper describes two types of ring VCO, three-stage and nine-stage [15]. Technology used for fabrication process is TSMC 0.18 µm. The architecture used for the analysis purpose is multiple-pass loop architecture in which delay stages have cross-coupled FETs. It provides the switching speed and also improves the noise parameter. Multiple-pass loop is used over single-loop to remove the frequency limitations imposed on the circuit as it adds auxiliary feed-forward loops which works in conjunction with the main loop. Basically we need to reduce the delay to have maximum frequency level. With increase in frequency the phase noise and jitter also get increased hence we need to switch the gain transistor periodically. The analysis shows that the centre frequency achieved by using multiple-pass loop wit latched saturated gain stages can reach up to 5.9 GHz. For three stage, the frequency range 5.16-5.93 GHz is obtained whereas for nine-stage range is 1.1-1.86 GHz. The phase noise for three and nine-stage are-105.5dBc/Hz at a 1-MHz offset from 1.8 GHz operation frequency and -99.5 dBc/Hz at 1-MHz offset from 5.79 GHz operation frequency, respectively.

Huiting Chen, Rendall Geiger (2001) This paper mentions the transfer characteristics of the ring oscillator which is one of the most important properties of VCO of any type [14]. Other important property which is mentioned is the relationship between operation frequency of the ring VCO and the control voltage. It is already told that according to many designers, the relationship between control voltage and operation frequency is monotonic, i.e., they are directly proportional to each other or inversely proportional to each other. So, this thinking is proved wrong in this paper. The beginning is done with the transfer characterization of the Ring VCO and it is found at the end of the analysis that the operational frequency is given by the number of delay cells, total capacitance and resistance at the output node of the delay cell. The three modes in which our transistor's work is analysed as the total capacitance and resistance depend upon it. With the analysis of the modes of the transistor's it is proved that in saturation region operating frequency is directly proportional to the control voltage, in triode the relationship is undetermined and in cut-off the operation frequency is independent of the control voltage. The delay cell structure used for determining these factors is differential input structure having current source in parallel with diode-connected loads. Tuning range obtained is 1.1GHz to 2.5 GHz.

B.Gaphari, L. et al. (2013) A small size ring VCO with low power consumption and noise voltage is implemented in this study to be used in Medical Implant Communication Service [13]. This five-stage ring VCO requires very small area for fabrication. The power consumption achieved is as low as 158 µW and tuning range is 352-454 MHz which is acceptable for medical applications. A multiple pass loop ring VCO is used and the delay cell topology is the differential one. The design is simulated in Monte Carlo simulations and different parameters are found. The results of the simulation show that the phase noise is -111 dBc/Hz at 1 MHz offset. This design requires less area compared to the LC oscillators' designs.

Xuemei Lei, Z. et al. (2013) A wide tuning range VCO is implemented in 180 nm CMOS process [12]. The topology defined in this paper is differential pair with cross coupled load transistors. The maximum operational frequency of the VCO is 6.9 GHz. And the tuning range is 75MHz-6.9GHz. The control voltage alters the output load; therefore, the frequency is controlled. The total area consumed by this ring VCO is 70 µm× 105 µm. The phase noise is improved if the control voltage is high.

Akansha Shrivastava, S. et al. (2013) An improved design for VCO is mentioned having five-stages with reverse body bias and SAL techniques [11]. These techniques are used to improve the parameters of performance in VCO. The design is implemented in 45 nm cadence virtuoso environment. The topology used in this study provides less delay, low phase noise and low leakage power with substrate bias technique. The frequency range achieved is 3-6.62 GHz and delay as minimum as 0.21 psec.

Vandana Sikarwar, N. et al. (2012) The design and analysis of CMOS ring VCO is described in this paper [10]. In ring VCO, The output of each stage depends upon the previous stage. A capacitor at the output of each stage is used and the design is simulated for various parameters like noise, power consumption, jitter and delay. The implementation is done on cadence virtuoso tool in 45 nm technology. Nine-stages of the oscillator are designed and simulated for various parameters and improve those parameters.

Ashish Raman, J. et al. (2012) A low power differential ring oscillator is designed in 1P6M 0.18 µm CMOS process provided by TSMC [9]. The output frequency lies in the range of 3.125-5.26 GHz. The power supply varies from1V to 1.8V. The power consumption is low for 1.8 V. the simulations show that the frequency range obtained is wide enough (3.125GHz to 5.26 GHz) and power consumption comes out to be 0.621 mW. Therefore, this design is used for radio frequency applications.

Ghenggang Zhang, J. et al. In this paper two differential delay stages constitute our VCO. The transmission gates controls are added to this architecture [8]. The VCO designed has low power low phase noise. To further improve the performance of the VCO, cross-coupled PMOS pair is used and resistors for compensation are used in every delay cell. Since two stages are used in this VCO therefore, we need an extra pole to provide 90 degree phase shift. Additional resistors were added to the design to equalize the rising and falling time and speed up the transition. Hence, the oscillation frequency is increased. The technology used for implementing this architecture is 90 nm CMOS technology. The power supply given is 1.2V and frequency ranges from 1.1GHz to 3.2GHz. The phase noise that is calculated for this architecture is -94 dBc/Hz and power dissipated is calculated to be 0.9 mW. The total area in which the VCI is designed is found to be approximately 12 µm by 13 µm.

Ashish Raman, R. et al. (2011) Implementation of low power VCO is described using technology 1P6M 0.18 µm provided by TSMC [7]. The power supply taken for this circuit is 1.8V. The conventional ring oscillator circuit is used with some modification in it. The tail current improvement is used to improve the delay by reducing the charging and discharging time. The phase noise of the ring VCO is more as compared to LC VCO. But the power consumption is negligible. In this work, the power and phase noise analysis is done. The average power consumption comes out to be 0.226 mW and the phase noise is -94.51 dBc/Hz at the offset of 1MHz. The frequency range achieved by this particular architecture is 0.958 to 4.43 GHz.

J.K.Panigrahi, D.P. Acharya (2010) A fully differential delay cell is proposed and analysed. Two stages are implemented of such delay cell [6]. The technology used is GPDK 90 nm CMOS technology. The VCO designed in this study has many features including wide frequency range, low power consumption and low phase noise. The phase noise can be improved by increasing number of stages. The frequency range obtained ranges from 1.22-3.22 GHz. Power dissipation is 9.61mW only and phase noise achieved is -90.01 dBc/Hz.

Xiaoyan Guiu, M. et al. (2012) In this study, a topology is defined which reduces the supply sensitivity. The topology used for this purpose is CMOS CML ring oscillator [5]. it mostly effects the jitter caused by supply variations. The technology used is 0.18um CMOS process to show the effectiveness of this technique. There are various techniques described in [5] to improve the power supply rejection ratio(PSRR). But many designs results in increasing power consumption and coupling effect. Therefore, this technique is finally implemented to reduce such unwanted effects. CML latches are connected to each buffer which exerts an opposite effect on the delay. The bandwidth obtained is 2.3-2.8 GHz and reduction in jitter can be achieved is up to 80%.

Luciano Severino de Paula, S. et al (2007) Two stage differential CMOS ring VCO is designed to be used as one of the module in the frequency synthesizer [4]. The local oscillator is generated to produce a quadrature output in multi-band acquisition system. The objective is to obtain the wide frequency range with low consumption of power and linearity between the operational frequency and control voltage. 0.18um IBM CMOS technology is used in this paper. Positive partial feedback is used in this paper with proper biasing. The centre frequency is determined by number of delay cells. Also the capacitances and resistances at the output node depend on the operating regions of transistors. The behaviour of the frequency has inverse relationship with the delay. In this work, wide frequency range, low power consumption and good linearity is obtained.

Motorola, S et al. (2004) The comparing of three ring VCO is been discussed in this paper [3]. Four-stage ring oscillator is fabricated in different topologies. The operating voltage for all the oscillator is kept constant only which is 1.8V. The technology used is 0.18 μm CMOS process. The comparison is done for phase noise, tuning range and power consumption. The topologies being compared in here are source-coupled, cross-coupled and dual inverter delay cell. The output buffer topology is single capacitive coupled. The data shows that among the three architectures described, the dual inverter is much better than the source-coupled and little better than cross-coupled when compared in power consumption and phase noise.

CHAPTER 3

SCOPE AND OBJECTIVE OF THE STUDY

3.1 Scope of the study:

With growth in the electronic industry, it is required to have the oscillator whose performance parameters, are not only acceptable but also better than the previously used technology. Hence, we need to improve the voltage controlled oscillator, so that its delay get reduced and phase noise and power consumption also get low. Earlier we used single-loop structures mostly but now multiple-loop architecture is preferred more. The delay cell comprises of the differential pair.

Modifications are done every time during implementing of delay cell for different applications. We have different improved structures for getting high tuning range, low power consumption, better phase noise and reduction in delay. Various configurations have its own advantages and disadvantages over other. It is not possible to have all positive aspects in one topology only. But several trade-offs are there. Like the frequency has monotonous relation with control voltage[1] but increasing of voltage may deviate the frequency from its behaviour.

The advancement in the technology opens the window for new research in the designing of the VCO based system. So we can say that the research will continue on the improvement in the performance parameters of the VCO in different fields.

3.2 Objective of the study:

While designing a voltage controlled ring oscillator following characteristics are mostly required:

- Reduction in delay when input is propagating from input to output.
- Minimum power consumption.
- Maximum frequency range.
- Minimum phase noise and jitter

It is not possible to achieve all the features in one system. There are several trade-offs present. If we increase the W/L ration of the transistor, it will improve its phase noise but surely decrease the frequency range and increases the delay of the VCO. Hence, it is necessary to look at each aspect while designing the VCO system according to our need.

Our main objective is to design a VCO with minimum delay, i.e. speed is to be increased. A conventional single-ended VCO structure is designed to achieve the minimum achievable

delay. The reverse substrate-bias (RSB) technique is implemented to improve the results obtained in the conventional structure..

Another topology discussed in this report is differential topology. The advantage of differential over single-ended topology is that the noise has lesser effect and power consumption is also reduced.

The technology in which VCO is to be designed affects a lot on the parameters. The implementation of the three architectures are done in tool Cadence Virtuoso with gpdk 90 nm CMOS technology in the same environment.

CHAPTER 4

DESIGN METHODOLOGY

The work of designing is done step by step. For designing a VCO, firstly a design flow should be followed to proceed with the implementation. We need to define the problem, in this case which is to reduce the delay of the ring VCO. Single ended VCOs are most common topology with various design issues and differentia architectural designs also have different pros and cons of their own. Like the design which may contribute in tuning range can also increase the delay of the circuit. So choosing the proper design is important according to the defined problem. The desired output should be first calculated before implementing it in some tool. Proper analysis steps should be followed for this purpose. As we need these results later on for comparison. The parameters which we need to modify or reduce should be studied carefully. Once the design problem is defined and architecture is been selected and analysed carefully in theory, next step comes is implementing it on some efficient tool. The tool used for designing the VCO is Cadence Virtuoso. Different techniques are available for designing the VCO as discussed in chapter 2. The structures which are considered to be implemented and analysed in this work are mentioned in this chapter step wise.

4.1 Conventional ring VCO Structure:

The conventional ring VCO structure comprises of an odd chain of inverters, in which output of one stage is input of next state. The output of last stage is feedback to the first stage. The main feature of this structure includes easy implementation with present CMOS technology; oscillations are achieved at low voltage level and wide frequency range. A single stage of the ring VCO comprises of an NMOS and a PMOS. When the input voltage level is low, NMOS turns off and PMOS turns on. Hence the current will flow through PMOS from Vdd to output voltage node. Similarly when the input voltage is high, PMOS turns off and NMOS turns on. Hence the current will flow through NMOS from output node to ground. Therefore, we get the inverted version of the input.

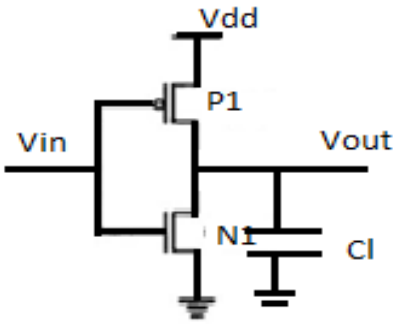


Fig. 4.1: Simple inverter

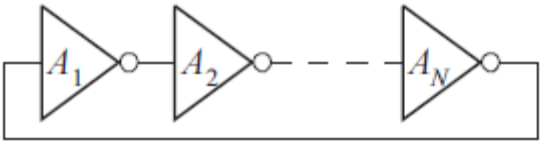


Fig. 4.2: Inverter chain ring VCO

Both N1 and P1 in figure 5.1 need to work in saturation region. The necessary conditions for turning on the transistors in saturation mode are:

$$V_{GS} > V_{TH} \tag{4.1}$$

$$V_{DS} > V_{TH} - V_{GS} \tag{4.2}$$

Now, each stage has its propagation delay, which can be written as the sum of rise time and fall time of single inverter. The delay is written for N stages as:

$$f_{osc} = \frac{1}{N(\tau_{rise}+\tau_{fall})} \tag{4.3}$$

Or we can write it as,

$$f_{osc} = \frac{1}{2Nt_d} \tag{4.4}$$

3-stage conventional ring VCO is designed in Cadence Virtuoso. The voltage supply is varied from 1V to 0.5V to determine how the frequency and other parameters changes. Other important parameters which play a considerable role in the VCO designing are delay, power consumption and phase noise.

The (W/L) ratio of the PMOS and NMOS is characterised according to the voltages as:

$$\left(\frac{W}{L}\right) = \frac{C_l}{\tau\mu_n C_{ox}(V_{DD}-V_{th})}\left[\frac{2V_{TH}}{V_{DD}-V_{TH}} + \ln\left(\frac{4(V_{DD}-V_{TH})}{V_{DD}} - 1\right)\right] \tag{4.5}$$

4.2 Reverse Substrate-Bias VCO structure:

In general, we connect the bulk of the transistor to the ground. For this structure, we are using the bulk voltage to be the controlling voltage for Change in frequency and power consumption.

By biasing the bulk of the transistor, the threshold voltage is increased. This increase in threshold voltage decreases the sub-threshold leakage currents. The threshold voltage is increased as given:

$$V_{TH} = V_{TH0} + \gamma(\sqrt{|2\emptyset_f + V_{Sb}|} - \sqrt{2\emptyset_f}) \quad (4.6)$$

Where,$\emptyset_f$, is the Fermi potential

γ is the SB coefficient.

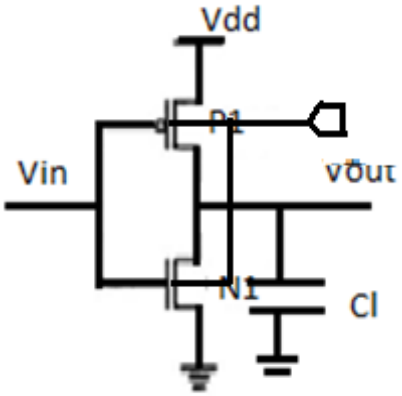


Fig. 4.3: Reverse SB inverter

The NMOS and PMOS bulk voltages are varied from 0.5V to 1V for controlling the frequency. The supply voltage is fixed to 1V. The delay is reduced in this configuration with respect to the conventional structure.

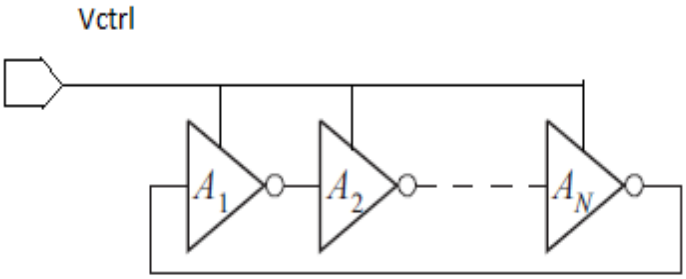


Fig. 4.4: Ring VCO using RSB technique

The analysis for power consumption, delay and phase noise is to be done for this structure. The results obtained are compared to the conventional structure previously implemented. The comparison must be done on the same ground for both the structures. The comparison will show how much the parameters are improved from the initial values.

4.3 Differential VCO structure:

The main advantage of using differential delay cell is that it reduces the common mode voltages and power supply variations. Therefore, it is used for noise performance and reduces the power consumption.

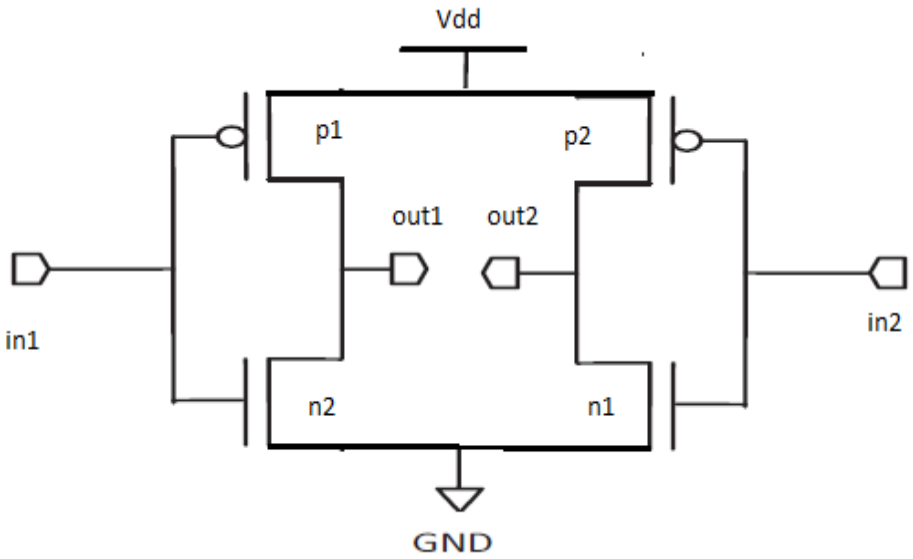


Fig. 4.5: Differential delay cell

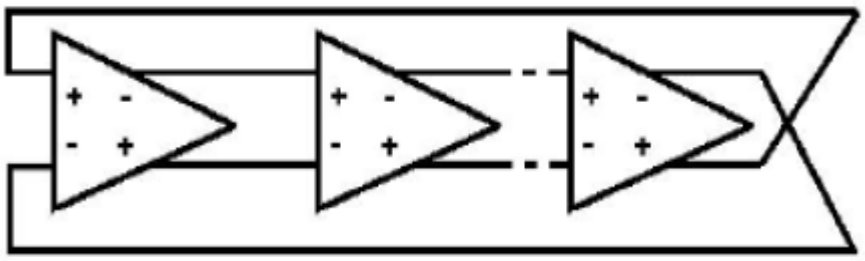


Fig. 4.6: Differential ring VCO

Differential VCO has two inputs and two outputs. An additional differential stage can also be added if the output is not coming out stable, making even number of stages in VCO. The delay stage is the differential inverter stage. The VCO is implemented in Cadence Virtuoso and supply voltage is varied from 0.9V to 1.4V and the variations in frequency and delay is noted. The main purpose of this structure is to reduce the power consumption obtained in the SB VCO.

4.4 Summary

The conventional structure, reverse SB structure and differential structure were implemented in gpdk90nm technology. The input voltages and control voltages are adjusted for obtaining the frequency range in which the VCO will work. The results are improved as compared to the conventional structure. The frequency range is enhanced and delay is minimised in both the architectures. Power consumption is also reduced to the acceptable level.

CHAPTER 5

IMPLEMENTATION

5.1: Conventional structure outputs:

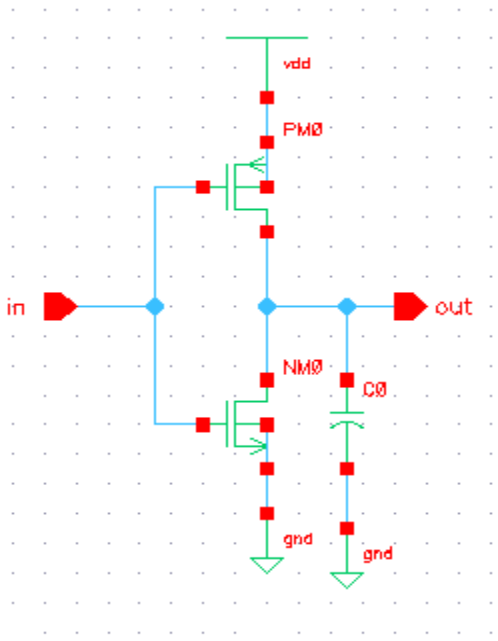


Fig. 5.1: Basic inverter delay cell.

Fig. 5.1 shows the basic delay cell architecture of the conventional ring VCO. The three stage VCO is implemented in cadence virtuoso for voltage supply ranging from 0.5 V to 1 V. The frequency and delay obtained at different Voltage supply is shown in table 5.1. The minimum power consumption of this inverter based VCO comes out to be 0.032mW.

Power Supply	Frequency	Power consumption	Delay
1V	12.57 GHz	31.2µW	17.8ps
0.9V	10.98 GHz	21.85 µW	23ps
0.8V	9.22 GHz	14.37 µW	31ps
0.7V	7.324 GHz	8.68 µW	46ps
0.6V	5.30 GHz	4.60 µW	79ps
0.5V	3.274 GHz	1.96 µW	85ps

Table 5.1: Implementation results of conventional structure

The three stage conventional VCO architecture to be implemented on Cadence Virtuoso is shown in:

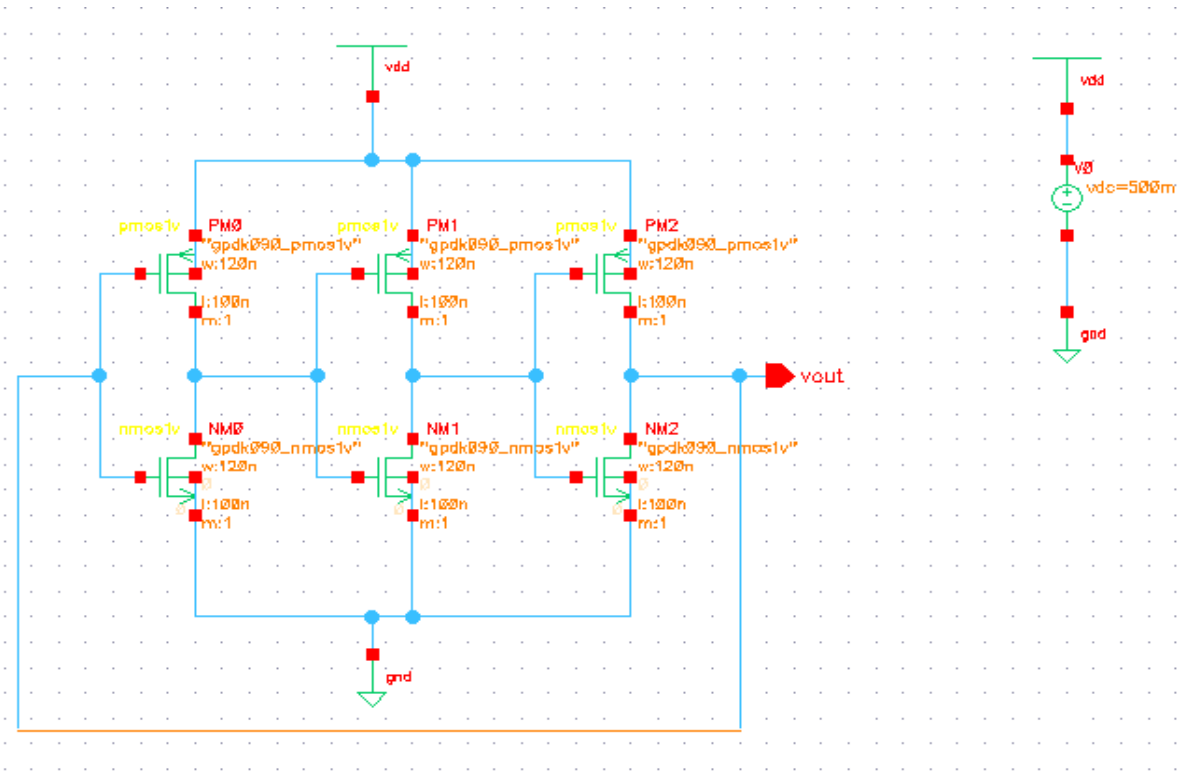


Fig. 5.2: the three stage conventional VCO architecture:

The transient responses of the conventional VCO structure shown in figure 5.2, for different power supply are shown in the figures below:

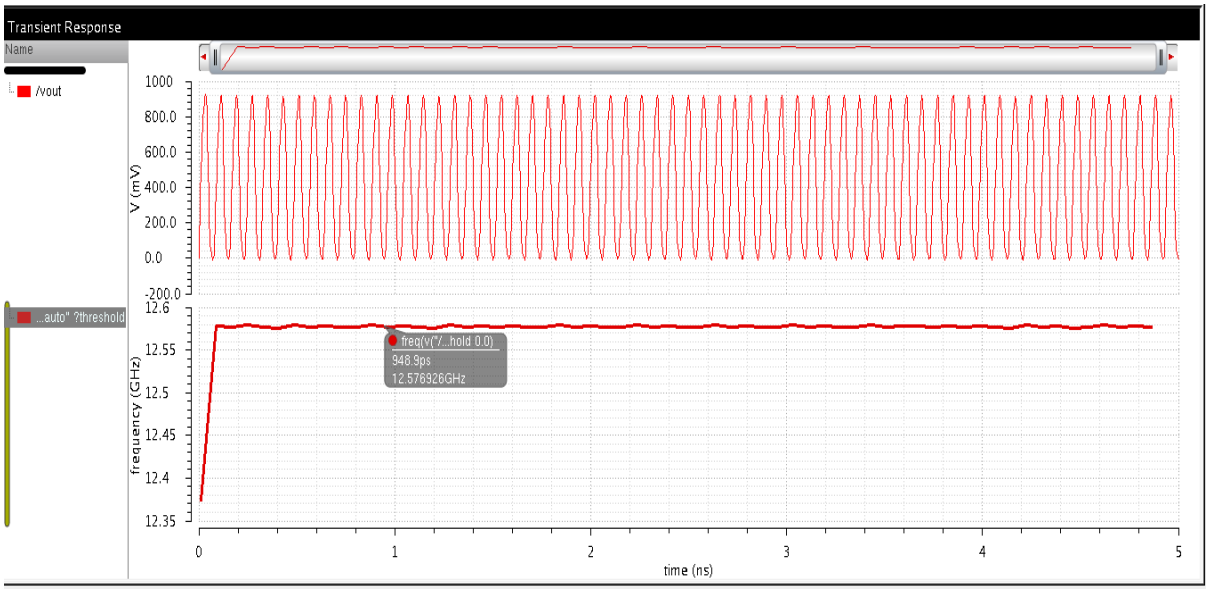


Fig. 5.3: Transient response and maximum frequency at power supply of 1 V

The maximum frequency achieved for 3 stage single-ended ring VCO is 12.57GHz at 1V

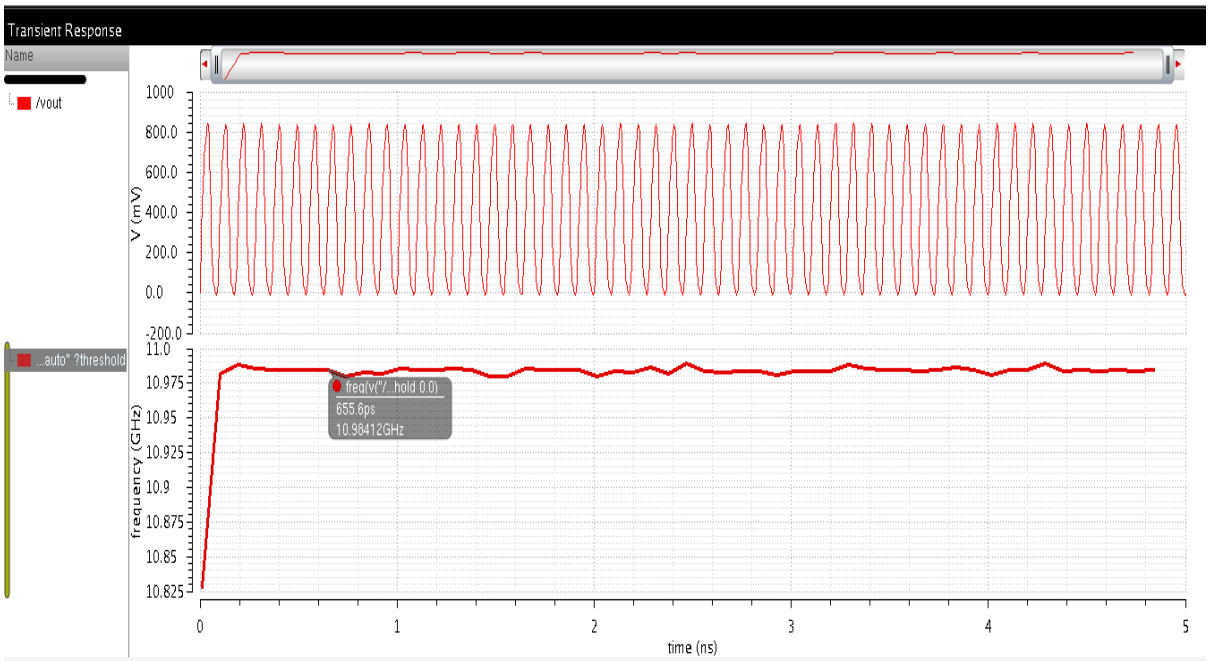


Fig. 5.4: Achievable frequency at input voltage of 0.9 V

. The frequency achieved at 0.9 V is 10.98GHz which validates the statement that the frequency decreases with decrease in input voltage.

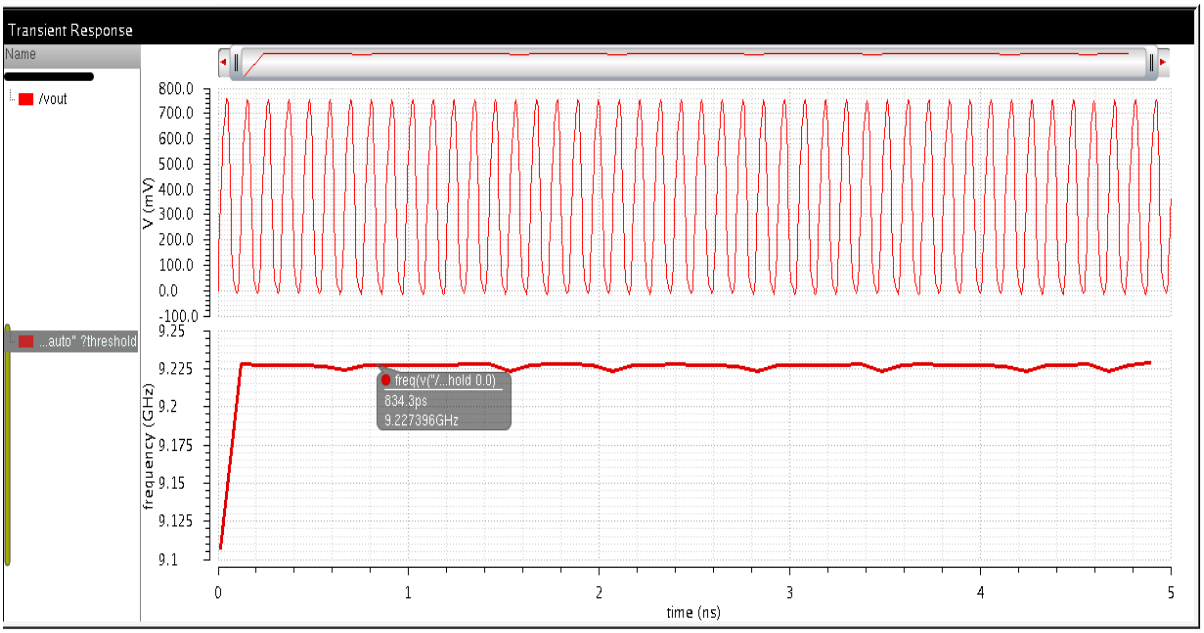


Fig. 5.5: Achievable frequency at input voltage of 0.8 V

Further decrease in input voltage decreases the frequency and also decreases the power consumption.

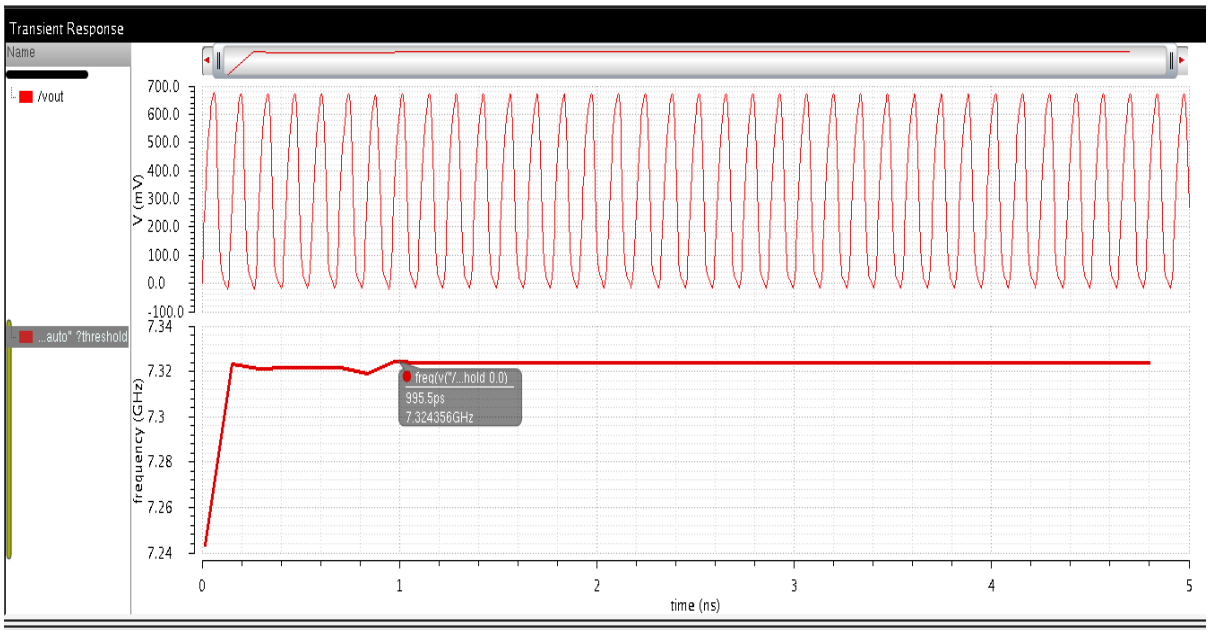


Fig. 5.6: Achievable frequency at input voltage of 0.7 V

Frequency shows the linear decrease from 12.57GHz in fig.5.3 to 7.724GHz in fig.5.6 when input voltage changes from 1V to 0.7V.

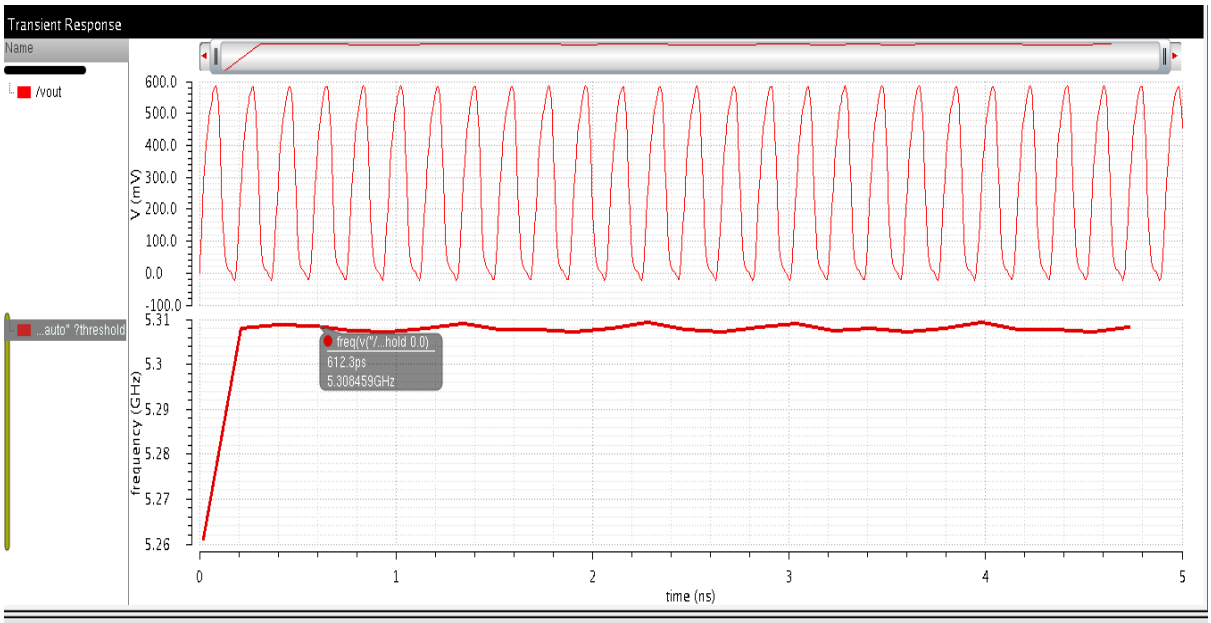


Fig. 5.7: Achievable frequency at input voltage of 0.6 V

The frequency achieved at 0.6V input voltage is 5.30GHz as shown in fig. 5.7.

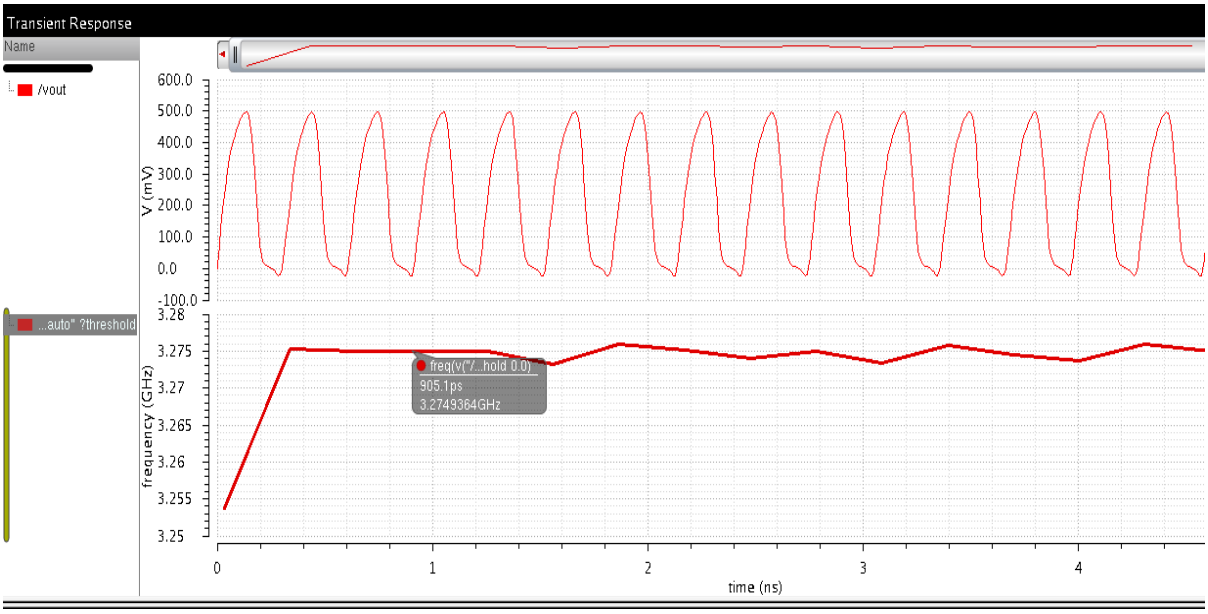


Fig. 5.8: Achievable frequency at input voltage of 0.5 V

5.2 Ring VCO with Reverse substrate-bias technique:

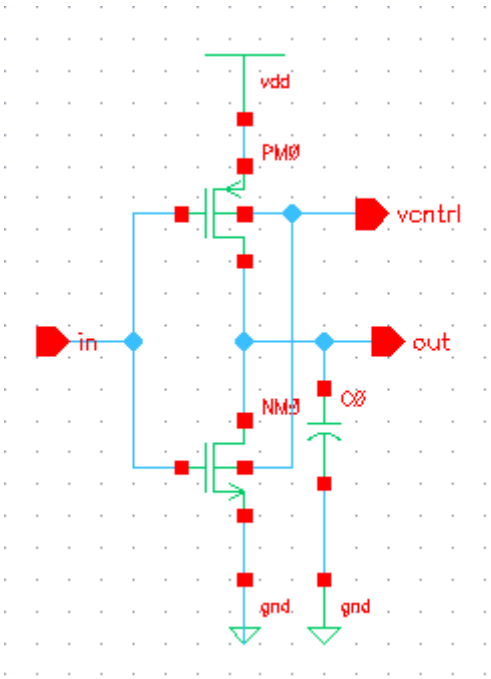


Fig. 5.9: Inverter delay cell with reverse substrate bias technique

The delay cell shown in figure 5.9 forms the one stage of the VCO. Three such stages are used for the implementation.

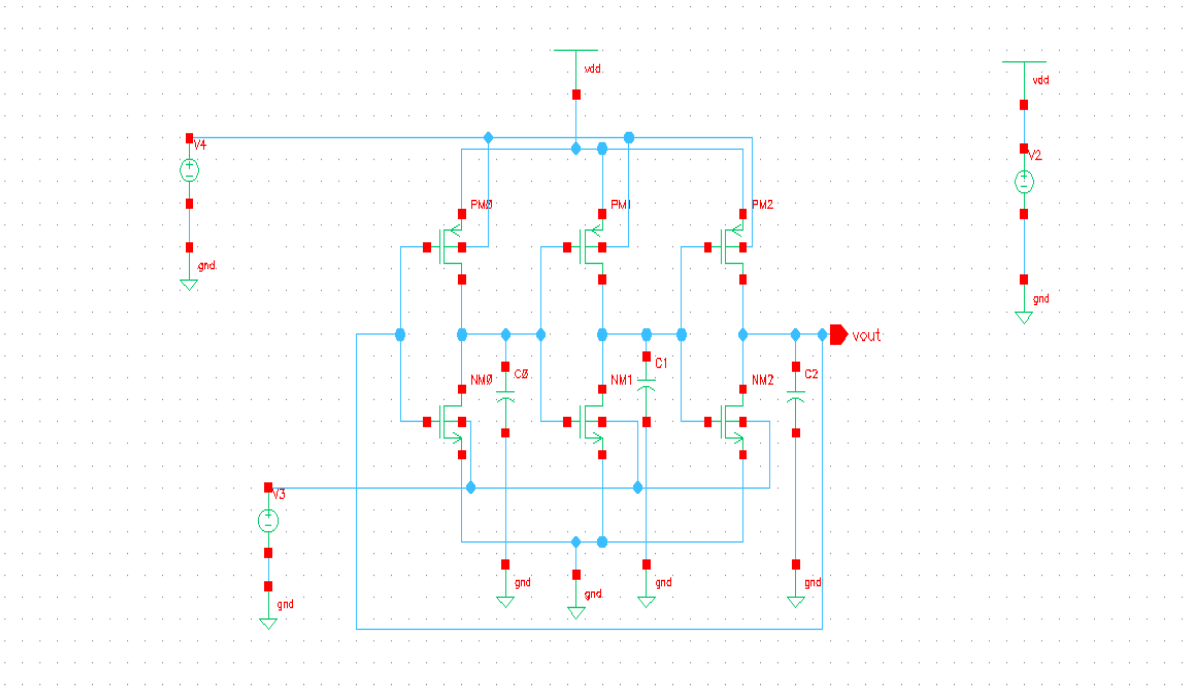


Fig. 5.10: 3-stage ring VCO with substrate-bias

The architecture is designed in Cadence Virtuoso at voltage supply of 1V. The control voltage is varied from 1V to 0.5V. The simulation results obtained for this architecture is tabulated in table 5.2.

Control Voltages	Frequency	Power consumption	Delay
1V	11.87 GHz	50.11 mW	8.27ps
0.9V	13.03 GHz	25.76 mW	12.5ps
0.8V	13.77 GHz	7.96 mW	14.4ps
0.7V	13.54 GHz	607.4 µW	15.75ps
0.6V	12.75 GHz	44.8 µW	17.15ps
0.5V	12.51 GHz	32.96 µW	17.68ps

Table 5.2: Change in parameters with change in control voltage

The frequency of the VCO at input voltage 1V will increase first and then decrease with the decrease in the control voltage from 1V to 0.5V.

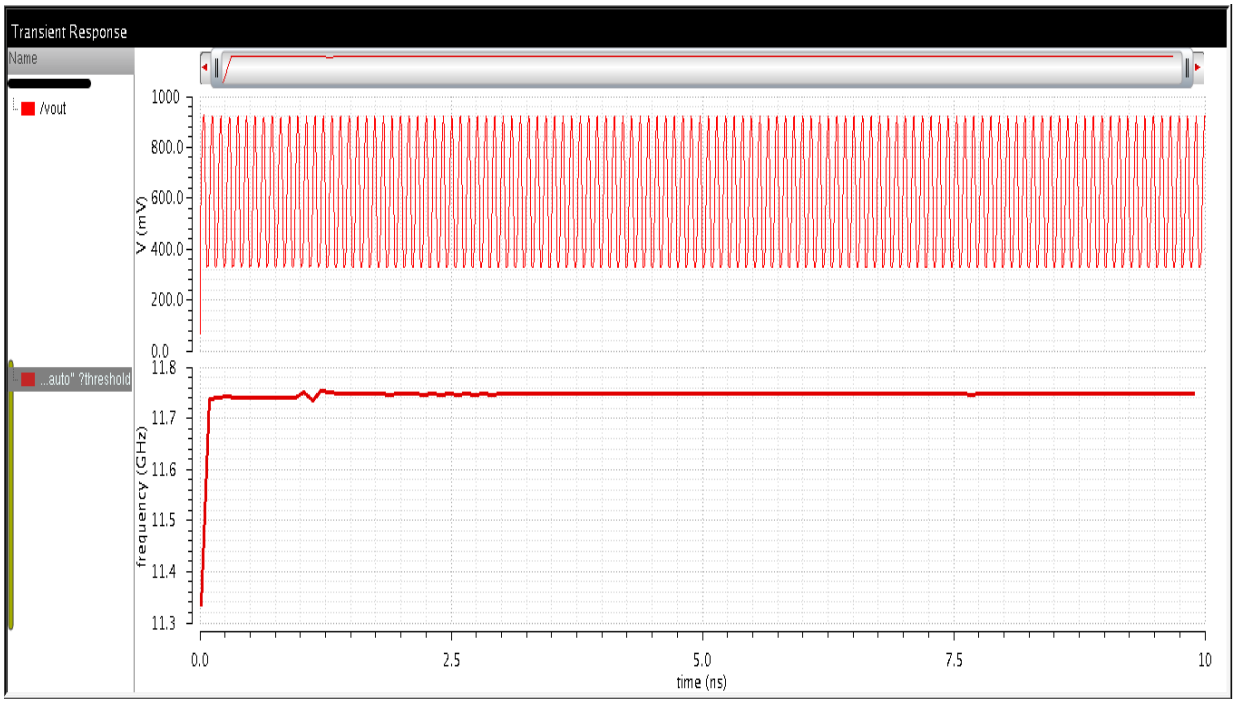


Fig. 5.11: Frequency at control voltage of 1 V

The frequency achieved at input voltage 1V and control voltage of 1V is 11.87GHz.

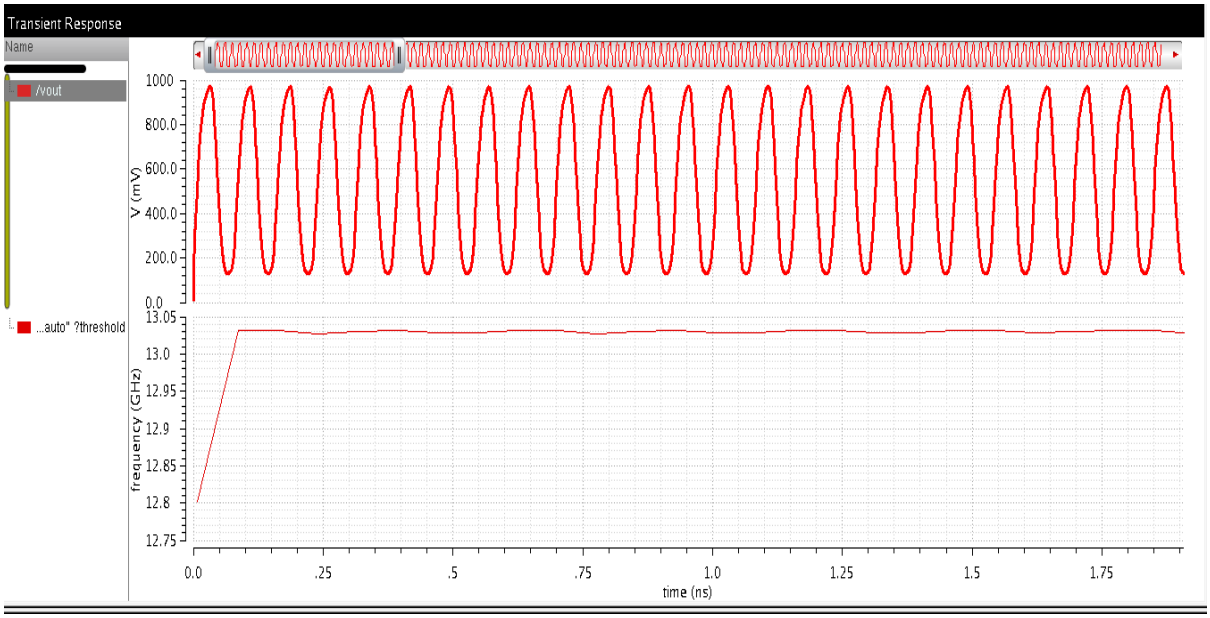


Fig. 5.12: Frequency at control voltage of 0.9 V

The frequency increases as we decrease the control voltage from 1V to 0.9V. the achieved frequency at this voltage is 13.03 GHz.

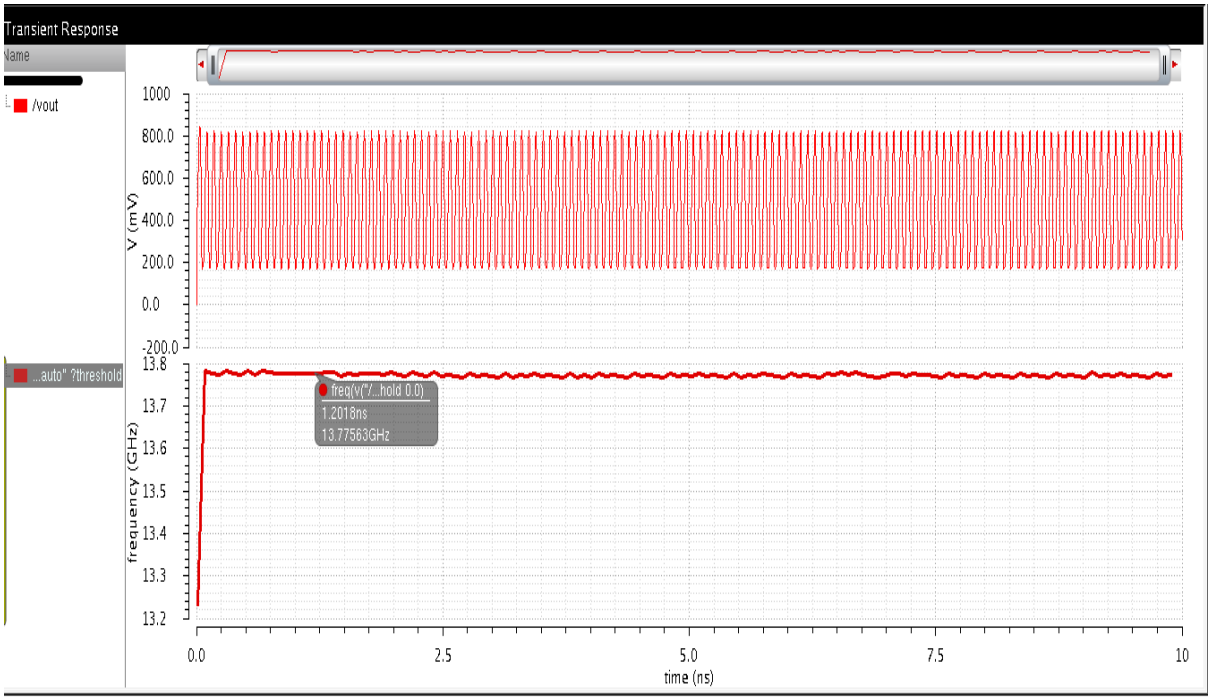


Fig. 5.13: Maximum frequency at 0.8 V

The 0.8V control voltage shows the maximum frequency achieved with this configuration which is 13.57GHz.

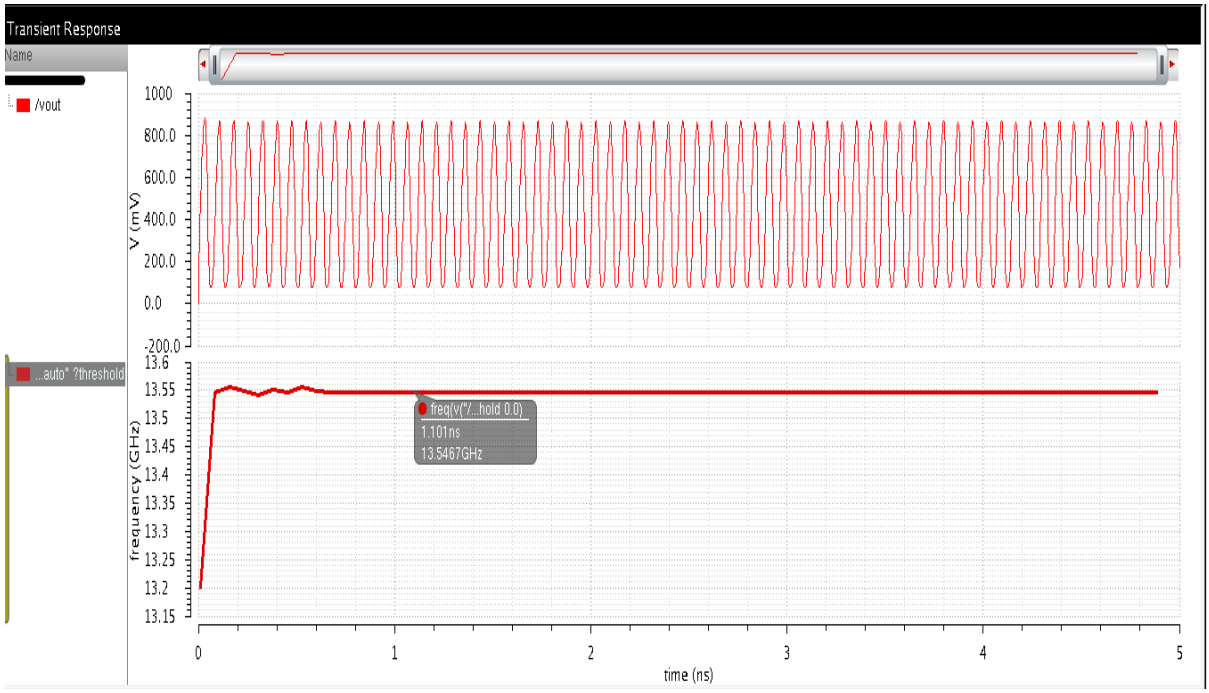


Fig. 5.14: decrease in frequency at control voltage of 0.7 V

Once the maximum frequency is achieved, further decrease in the control voltage will decrease the frequency as shown in fig.5.14, when control voltage is decreased to 0.7V, the frequency reduced to 13.54GHz.

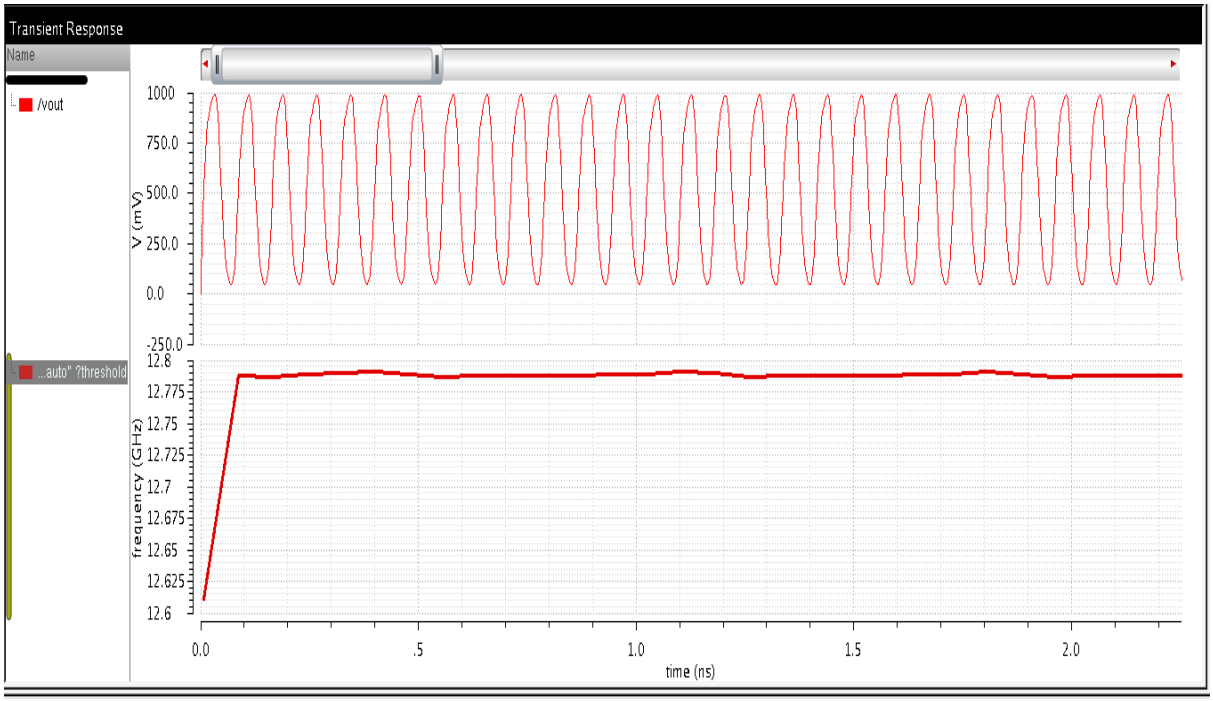


Fig. 5.15: frequency at control voltage of 0.6 V

Fig.5.15 also shows the decrease in frequency with decrease in control voltage.

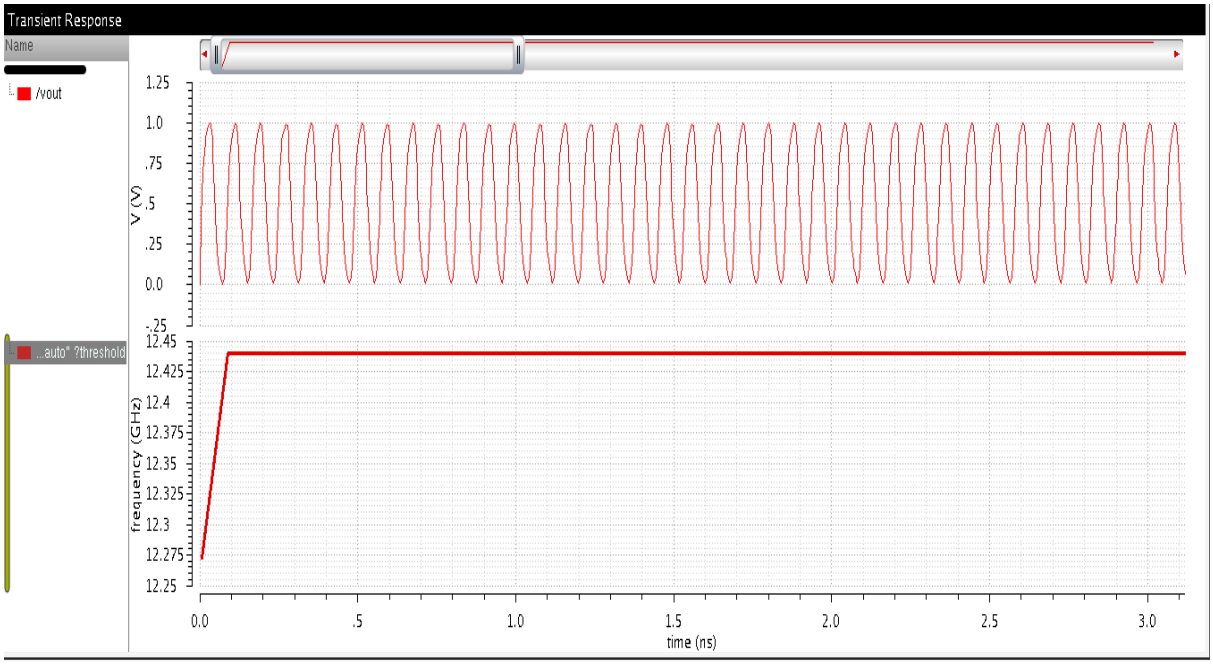


Fig. 5.16: minimum frequency at control voltage of 0.5 V

Observing these outputs we can say that with decrease in control voltage, the frequency first increases to a certain level and then start decreasing.

5.3 Differential Structure:

The differential architecture is also designed for the comparison of the performance parameters of a VCO. The differential structure is implemented in Cadence Virtuoso in the same environment so that comparison can be done on the same ground.

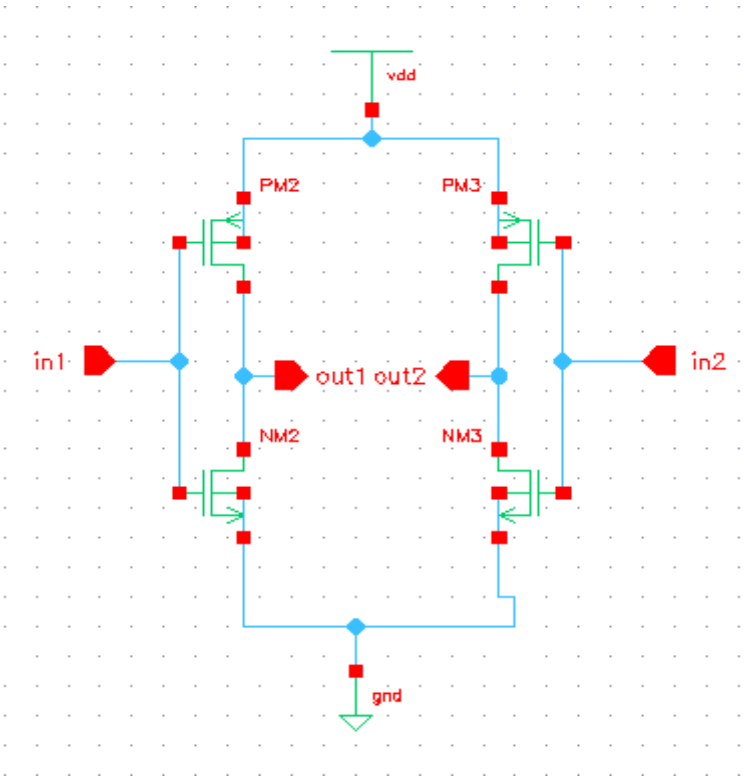


Fig. 5.17: Differential delay cell

The table5.3 shows the variation in the parameters with the change in voltage supply.

Input voltage	Frequency	Power consumption	Delay
1.4V	17.405 GHz	178.1 µW	8.1ps
1.3V	16.405 GHz	142 µW	9.6ps
1.2V	15.273 GHz	111.91 µW	11ps
1.1V	14.002 GHz	85.14 µW	14.17ps
1V	12.577 GHz	62.42 µW	17.8ps
0.9V	10.982 GHz	43.7 µW	20ps

Table 5.3: change in parameters with change in control voltage

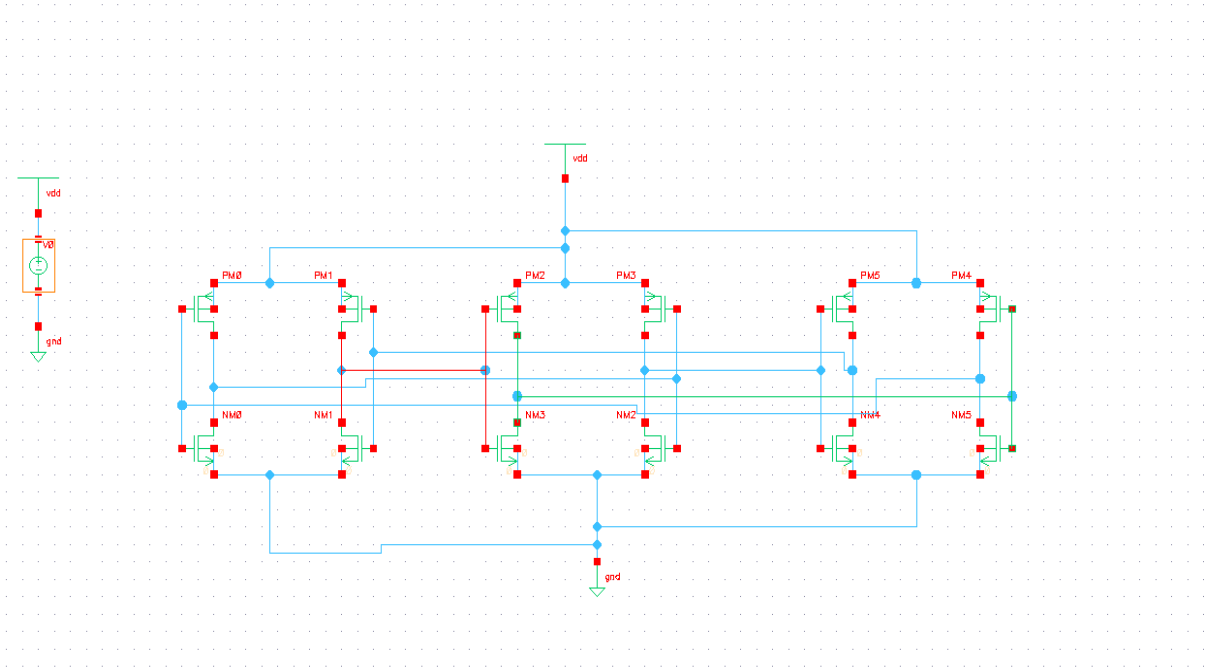


Fig. 5.18: Differential VCO structure

The transient response of the differential VCO with change in input voltage and output frequency is shown in the following simulations.

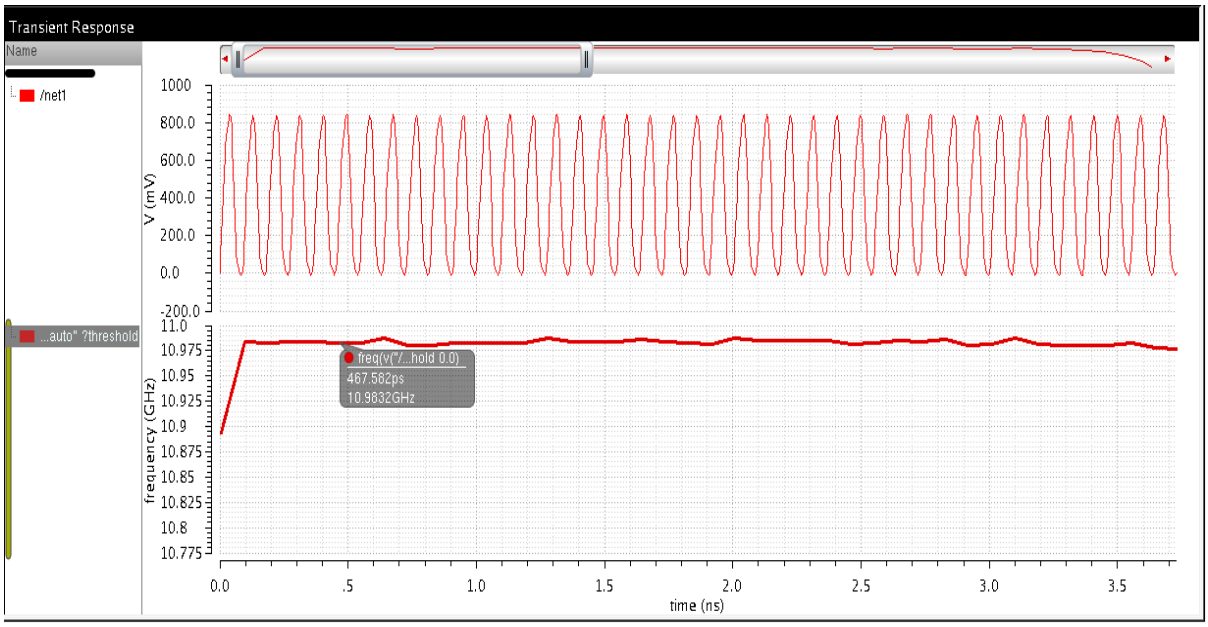


Fig. 5.19: Frequency at input voltage of 0.9 V

Minimum frequency of 10.98GHz is achieved at the input voltage of 0.9V. as we increase the input voltage frequency will also increase linearly.

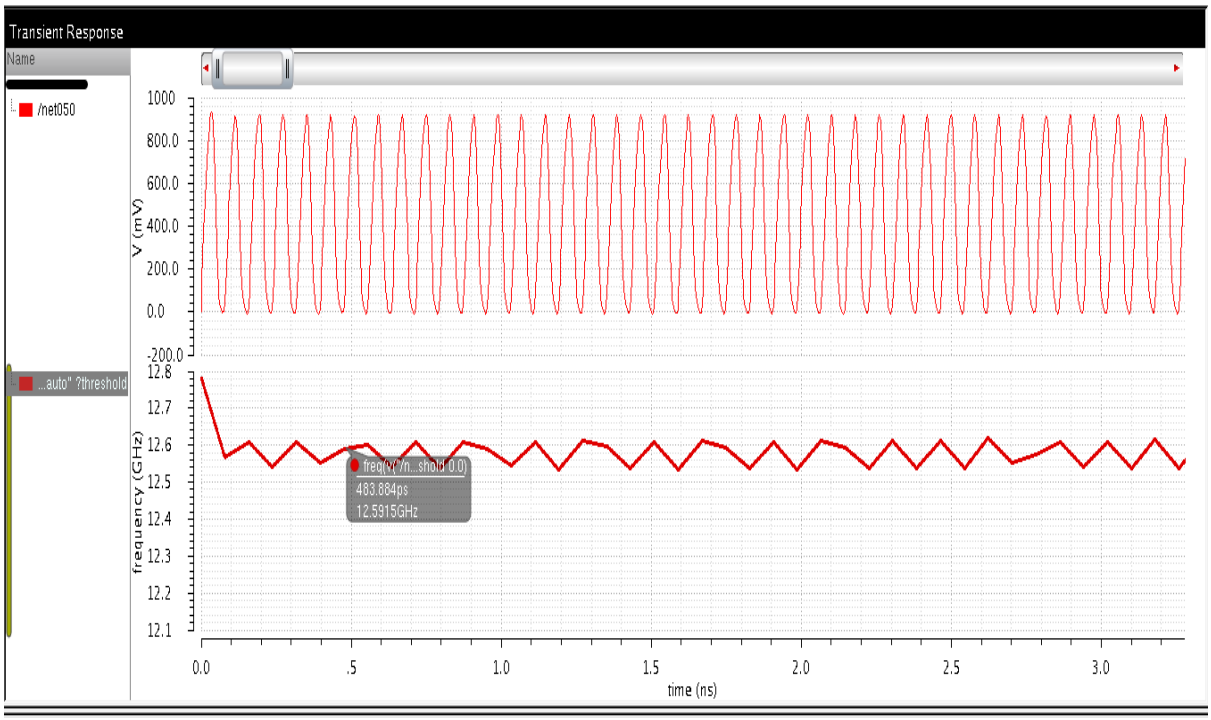


Fig. 5.20: Frequency at input voltage of 1 V

Output frequency increases to 12.57GHz with increment in the voltage from 0.9V to 1V as shown in the simulation results in fig.5.20.

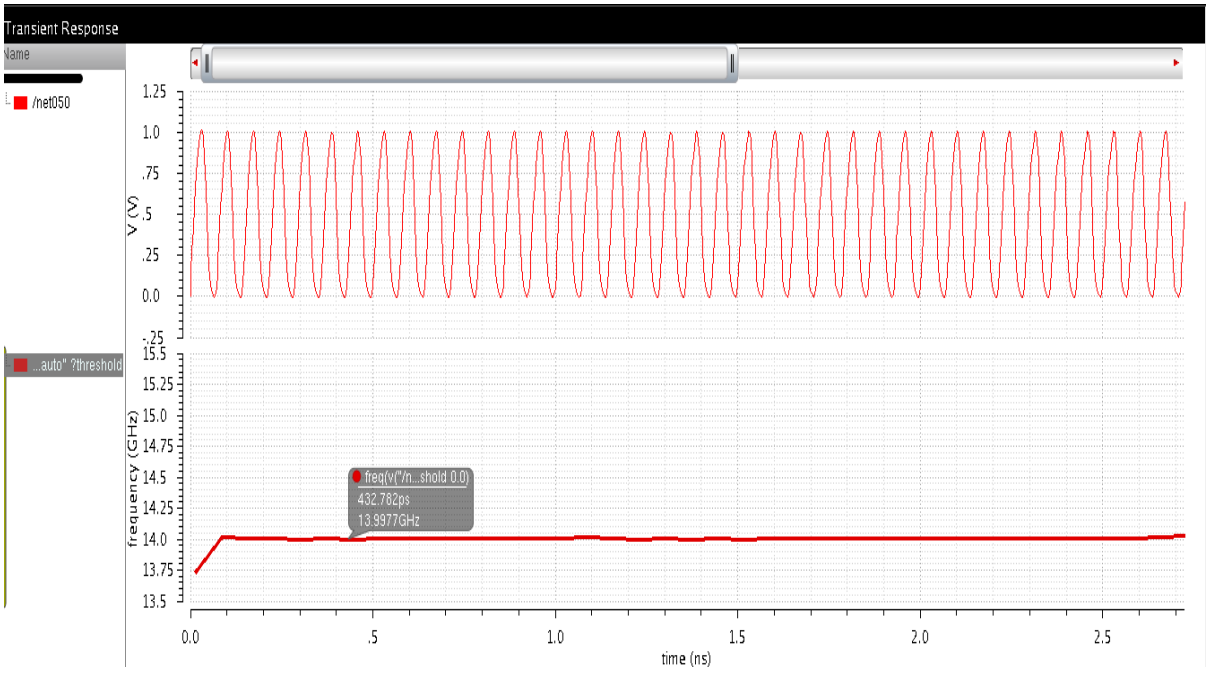


Fig 5.21: Frequency at control voltage of 1.1 V

Output frequency increased to 14.002GHz when the input voltage is 1.1V in fig. 5.21.

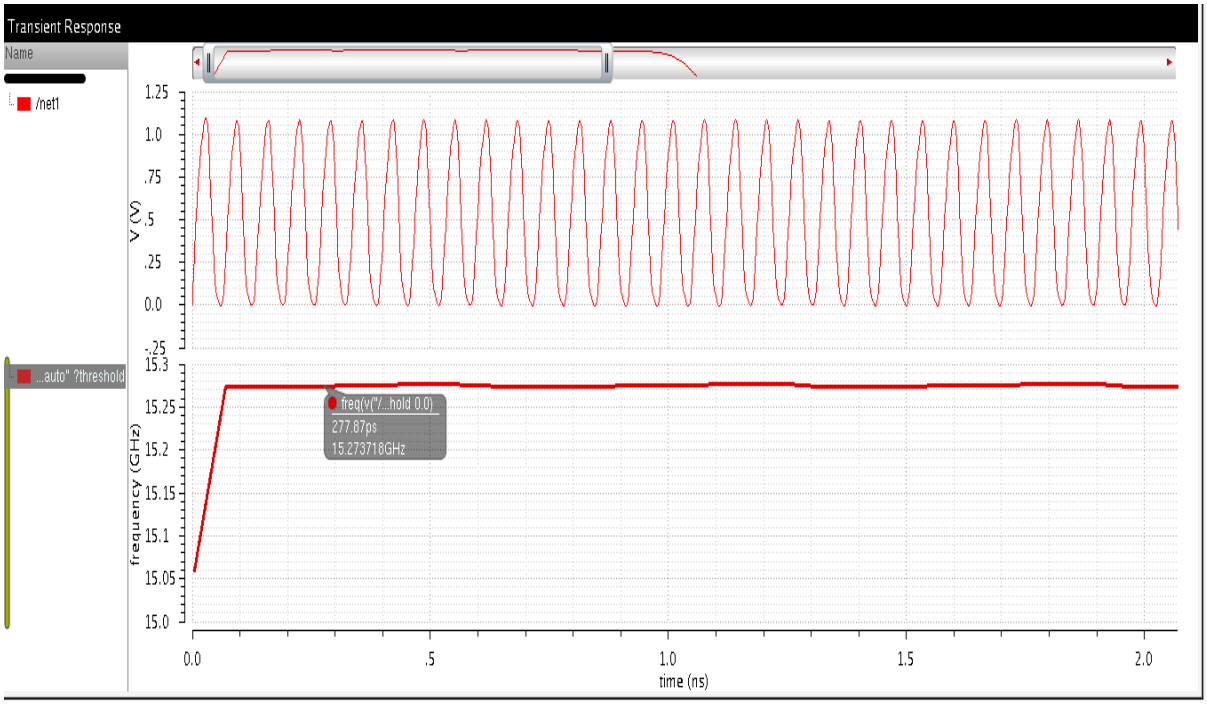


Fig. 5.22: Frequency at control voltage of 1.2 V

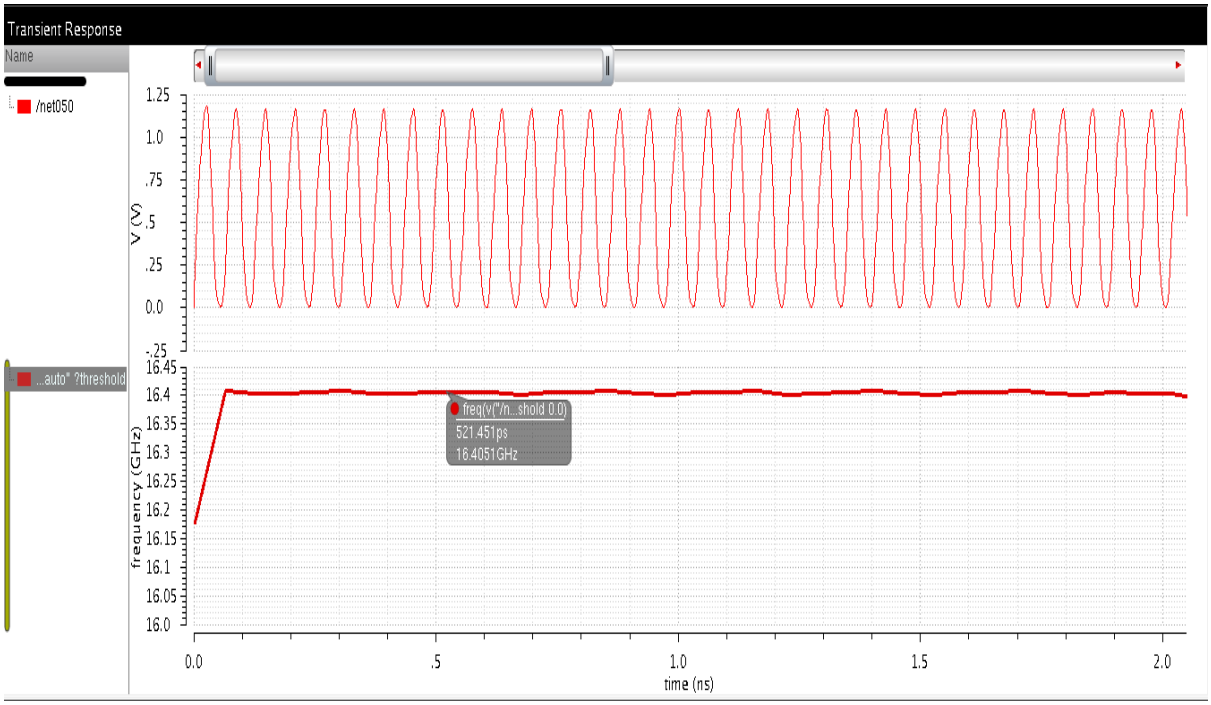


Fig. 5.23: Frequency at control voltage of 1.3 V

Output frequency increases linearly with increase in the input voltage. In fig. 5.22, the output frequency was 15.27GHz when voltage given is 1.2V and the frequency increases to 16.40GHz when 1.3V is given.

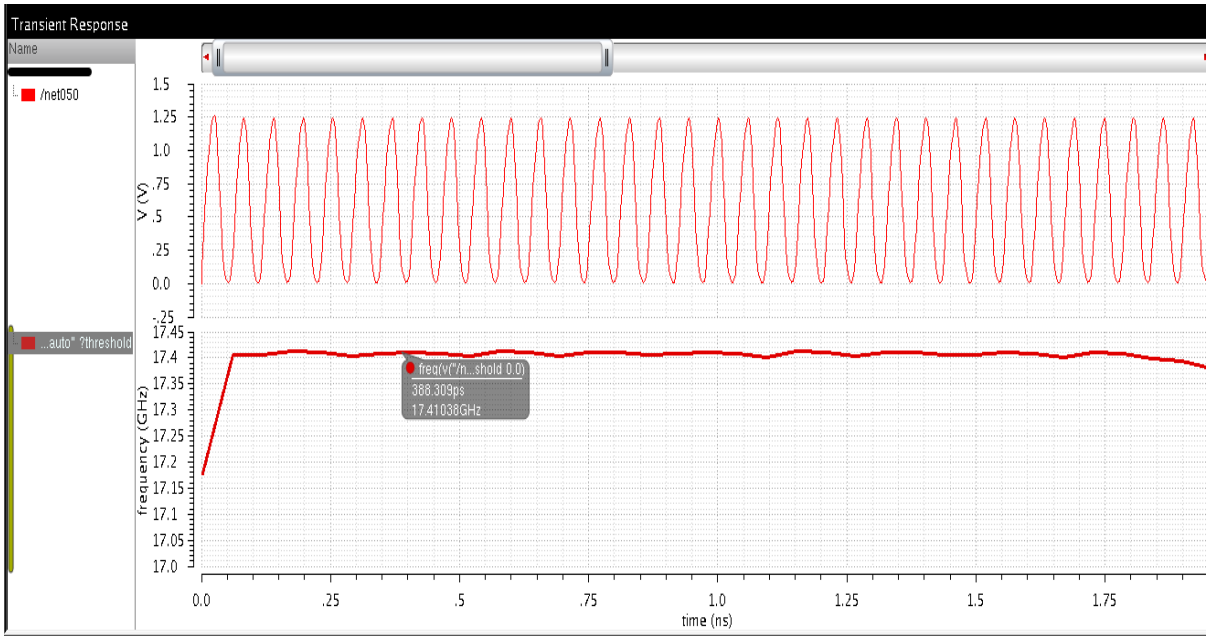


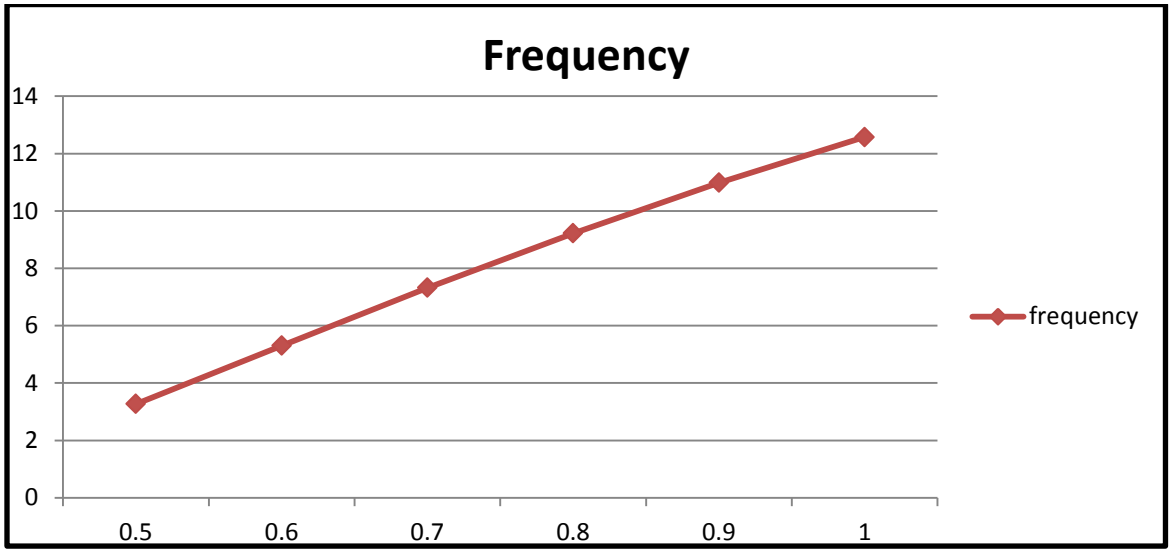
Fig 5.24: Maximum frequency at control voltage of 1.4 V

The increase in the frequency of the ring Voltage Controlled Oscillator with increase in the input voltage shows that frequency and input voltage are directly proportional. The simulation results also show the validation of the statement. The power consumption measured for the above configurations shows the decrease with decrease in the input voltage. On the other side, the delay decreases with increase in the input voltage.

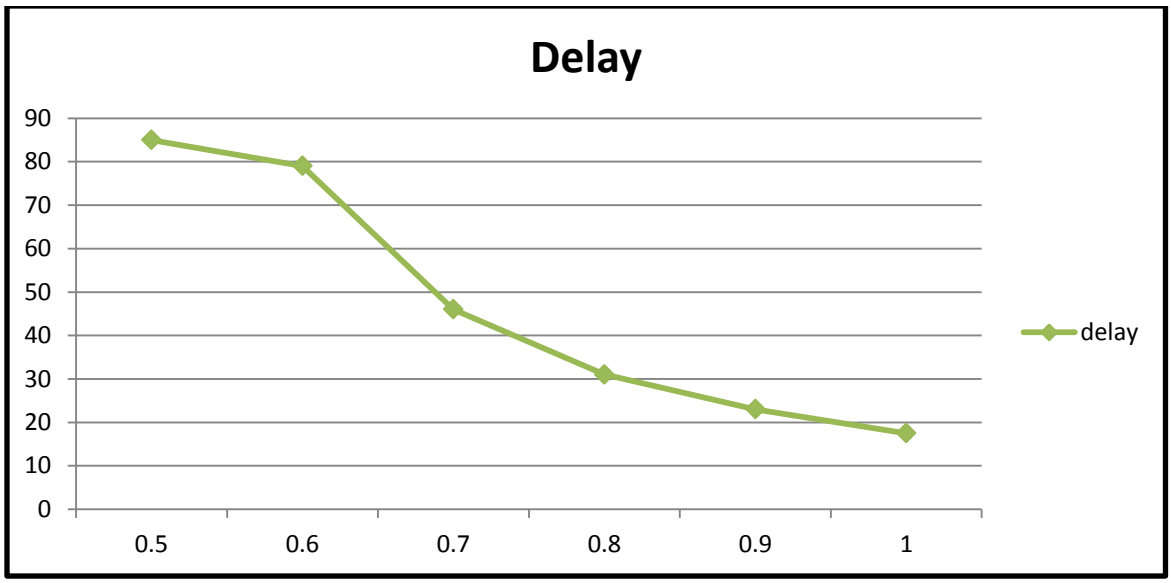
Chapter 6

Results and Discussions

.6.1 conventional VCO structure:



(a)

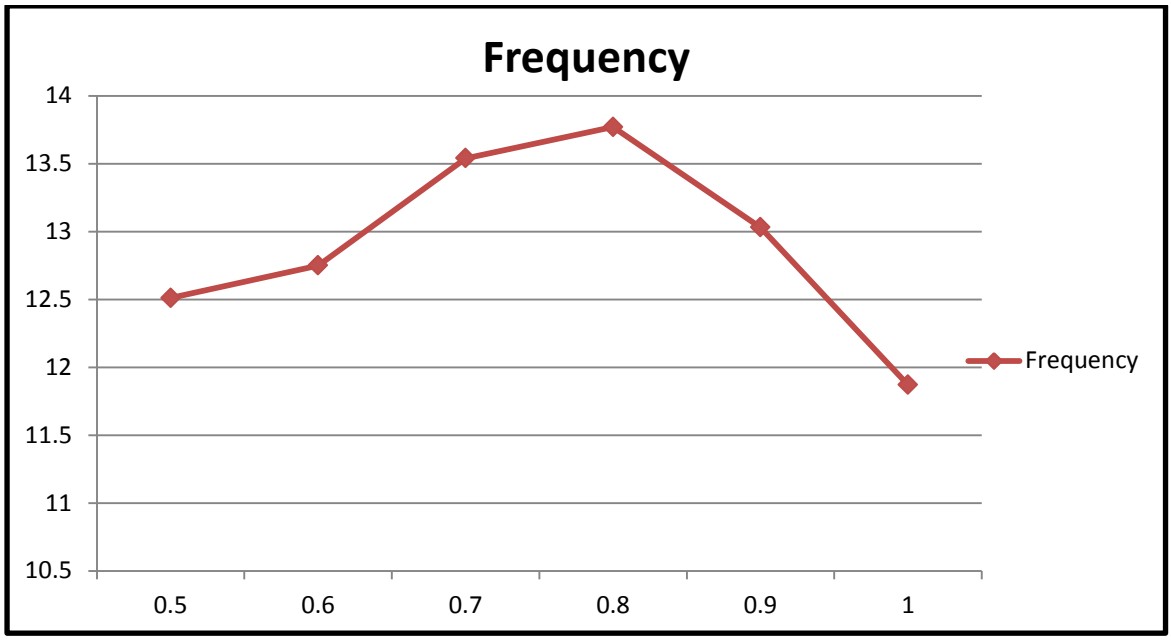


(b)

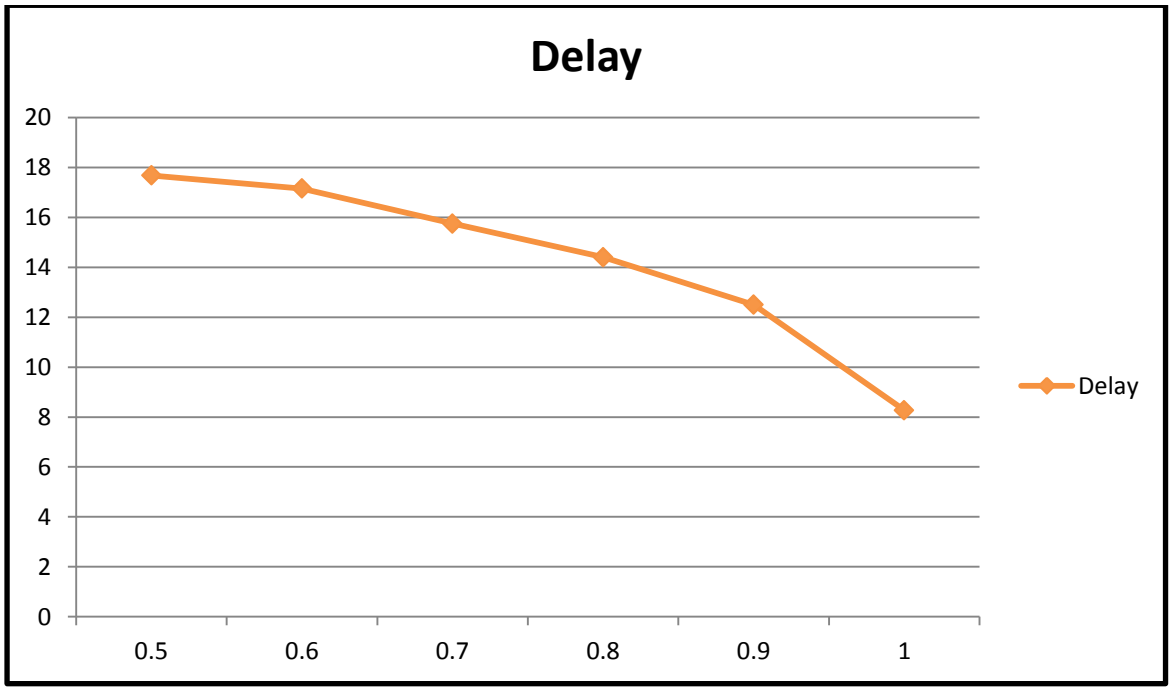
Fig. 6.1: (a) Variations in frequency and (b) Delay at different voltage supply for conventional structure

The maximum frequency for conventional single-ended VCO achieved is 12.57GHz at 1V. The corresponding minimum delay achieved is 17.8picosecond. The power consumed at 1V is measured to be 31.2 µW.

6.2 RSB VCO structure:



(a)

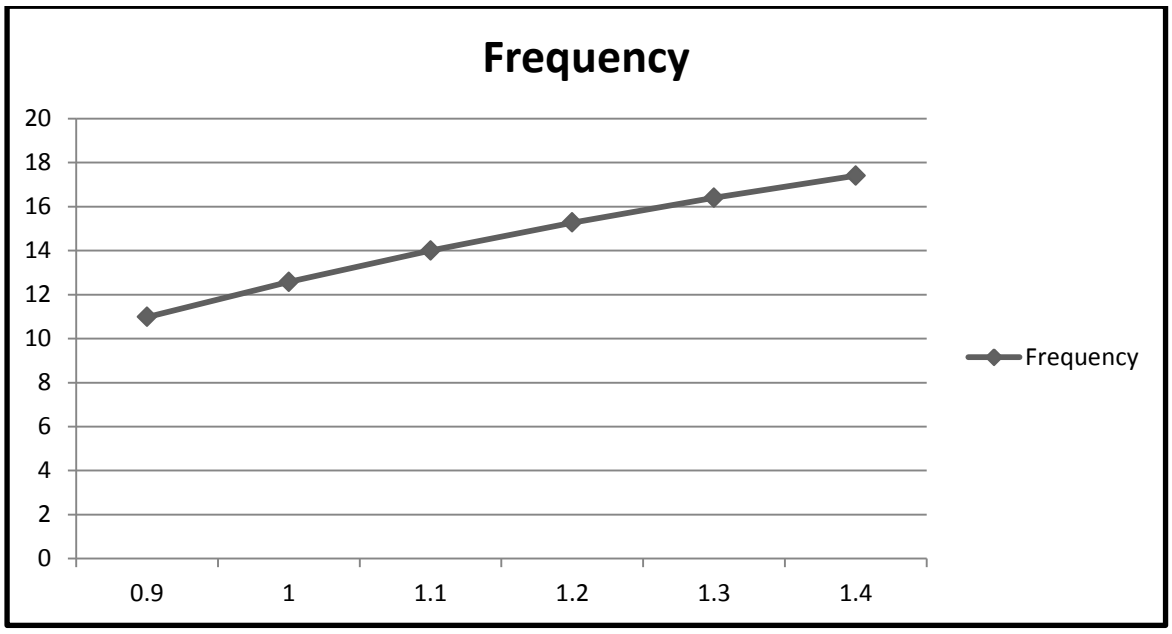


(b)

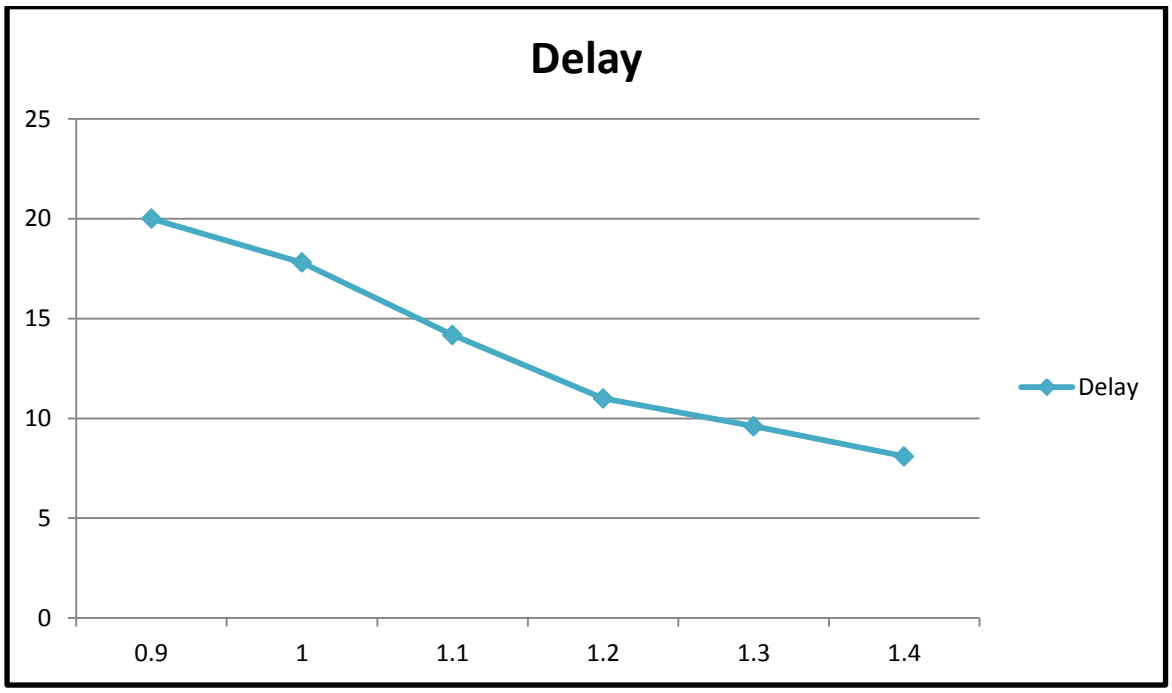
Fig. 6.2 (a) Variations in frequency and (b) Delay at different voltage supply for reverse SB Technique

The maximum output frequency achieved at 1V input voltage and 0.8V control voltage is13.77GHz. The minimum delay is achieved is 8.27picosecond at 1V control voltage.

6.3 Differential structure:



(a)



(b)

Fig. 6.3(a) Variations in frequency and (b) Delay at different voltage supply for differential structure

The output frequency increases linearly from 10.98GHz to 17.40GHz as the input voltage changes from 0.9V to 1.4V.

6.4 Comparison of Data:

The three configurations whose outputs are to be compared:
1) Conventional structure

2) Reverse SB structure

3) Differential structure

The comparison is to be done for maximum frequency, minimum delay and minimum power consumption. Fig. 6.4 and fig. 6.5 shows the comparison results for frequency and delay between conventional ring VCO structure and VCO using reverse SB technique. The comparison graphs clearly show that frequency range is improved and delay is also reduced in the modified structure.

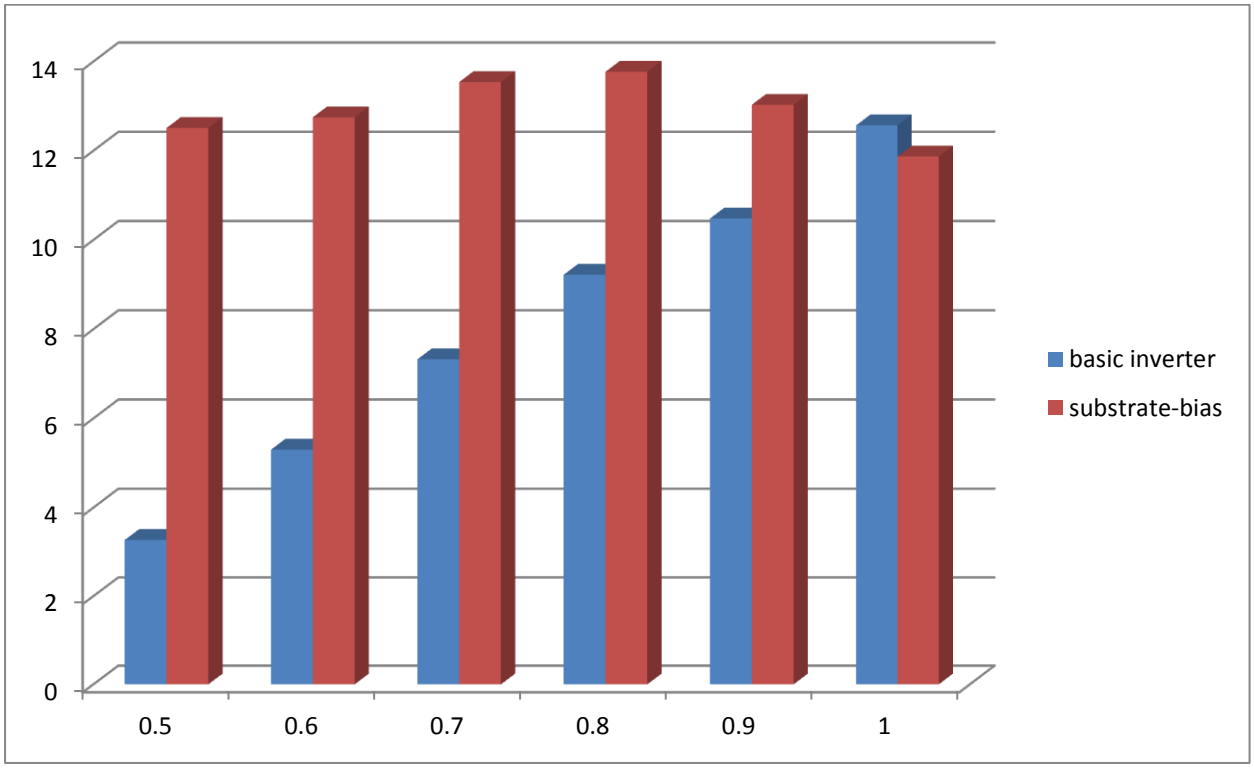


Fig. 6.4: Frequency comparison between Basic inverter and SB technique

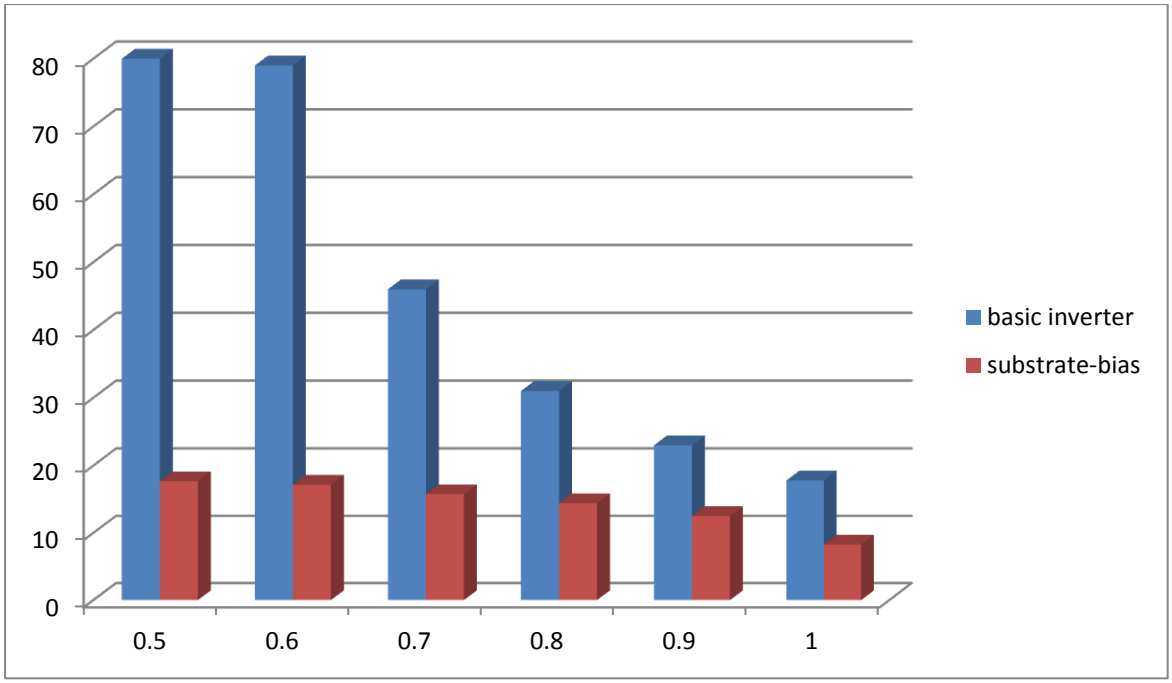


Fig. 6.5: Delay comparison between basic inverter and SB technique

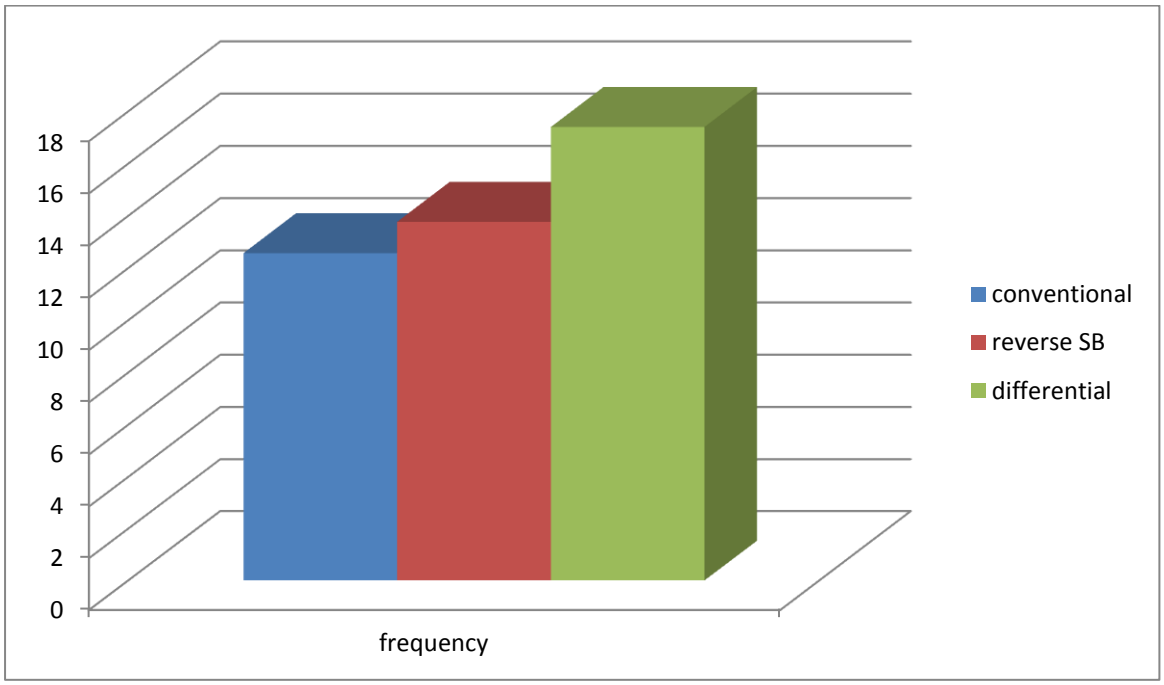


Fig. 6.6: Maximum frequency achievable by the three structures

The comparison shows that the maximum frequency is achieved by differential configuration which is 17.40GHz. The reverse SB structure also shows the maximum frequency of 13.77GHz which is more than the conventional VCO.

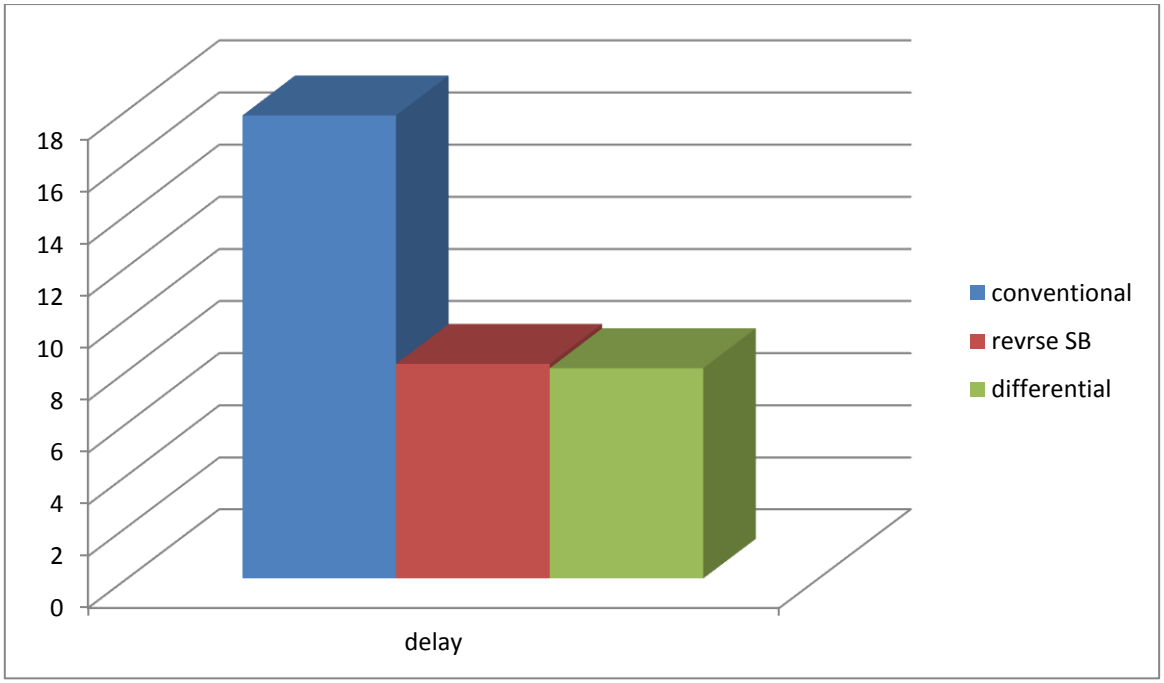


Fig. 6.7: Minimum delay observed in differential at supply voltage 1.4V

The minimum delay is also shown in differential structure which is equals to 8.1picosecond. A comparable amount of delay is observed in SB structure which is 8.27picosecond. The conventional structure shows the minimum delay of 17.8picosecond.

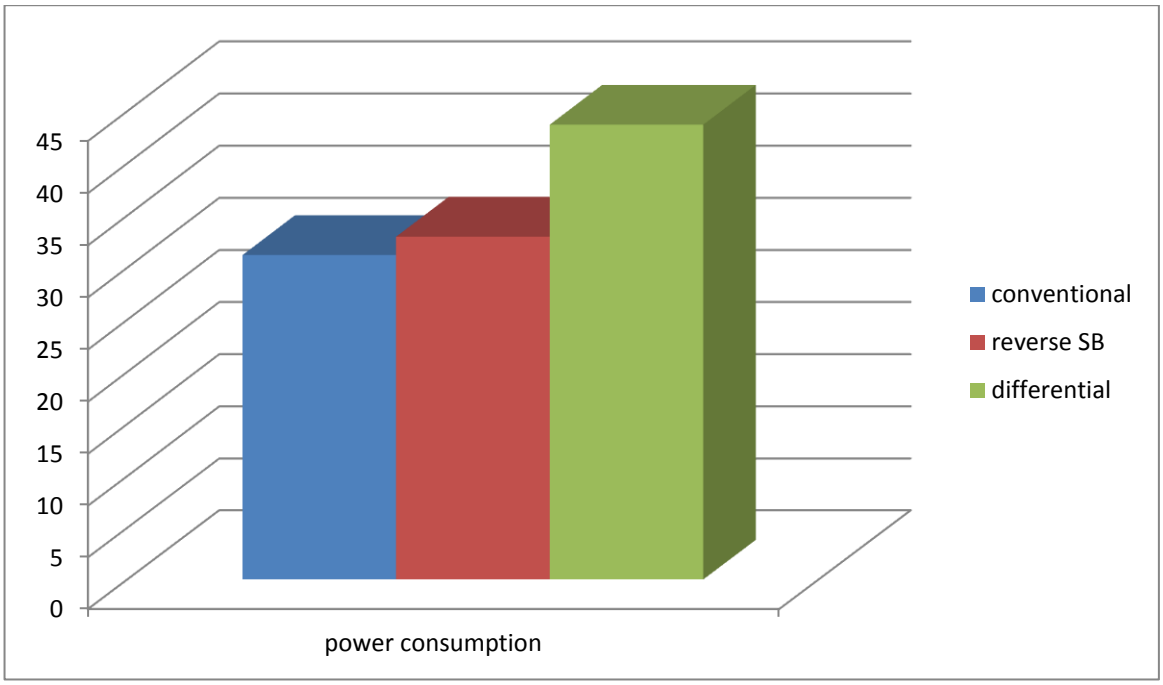


Fig. 6.8: Power consumption at 1 V

The minimum power consumption in differential structure is measured to be 43.7µW and in SB structure it measured to be 32.96 µW which is comparable with 31.2 µW power of conventional structure.

6.5 Validation of Results:

The frequency range observed in this work is improved for reverse SB structure as well as for differential structure.

6.5.1: Reverse SB technique:

The comparison of the performance for reverse SB technique in this work and in previous work [11] is show in table6.1.

Voltage	[11]	This work
0.6V	6.62GHz	12.75GHz
0.9V	4.92GHz	13.03GHz
1V	4.73GHz	11.28GHz

Table 6.1: Performance comparison table for reverse Substrate-Bias Technique

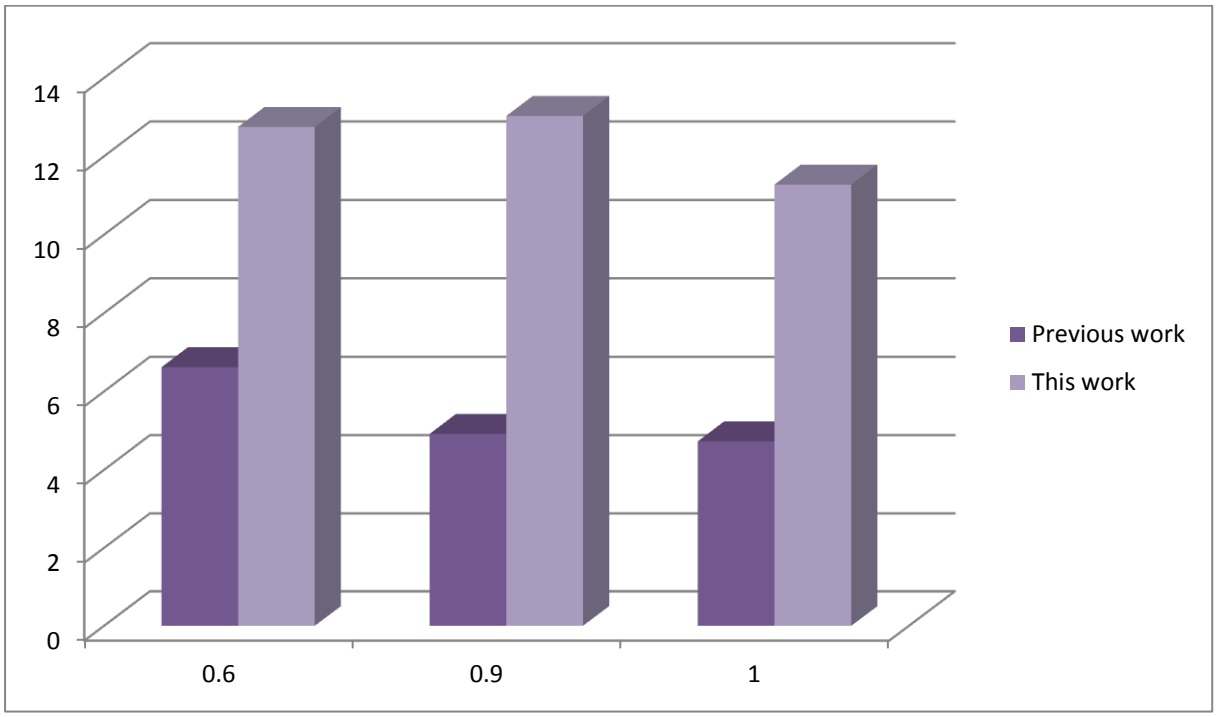


Fig. 6.9: Comparison between the frequencies achieved in this work and the previous work done.

6.5.2: Differential structure:

The differential architecture in [9] is implemented in 180nm CMOS technology. The frequency range observed in previous work [9] and this work is shown in table 6.2.

Voltage	[9]	This Work
1	3.126GHz	12.57GHz

Table 6.2: Performance comparison for differential architecture

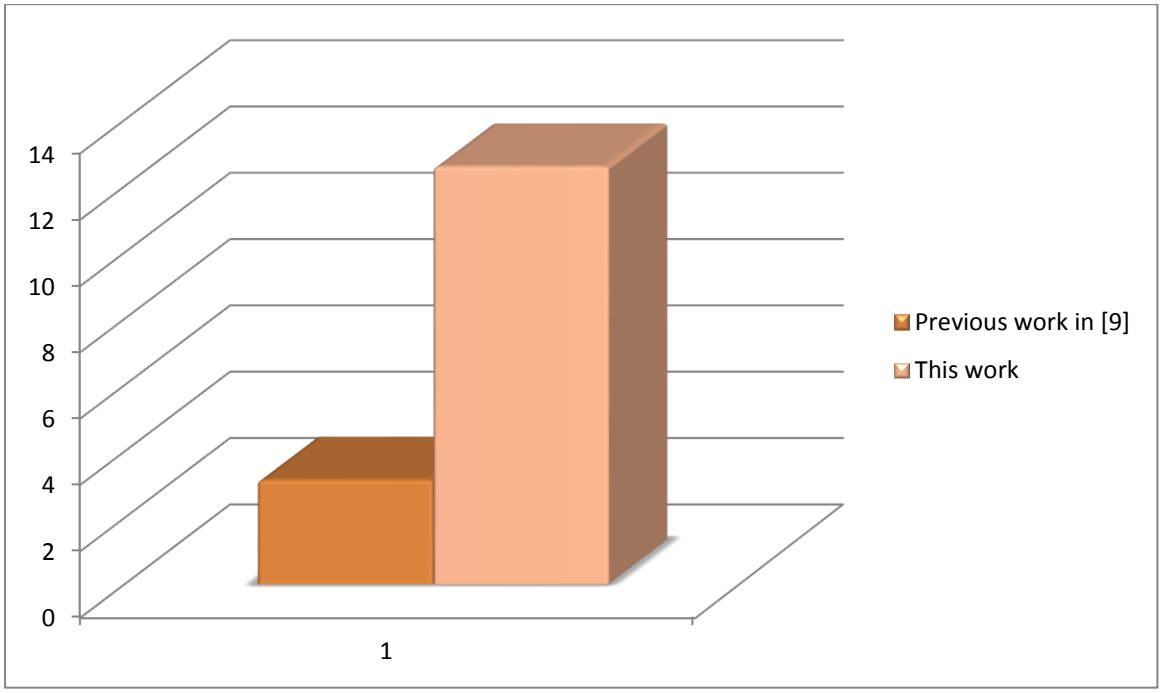


Fig. 6.10: Frequency achieved at 1V supply voltage.

The comparison of data observed in this work and previous work [9] clearly shows that the frequency range is improved in this work. In the previous work, the resulted frequency range was 3.126GHz-5.26GHz for voltage range of 1V-1.8V whereas, in this work it is 12.577GHz-17.405GHz for voltage range of 1V-1.4V.

Chapter 7

CONCLUSION

A Comparative study of various structures for voltage controlled oscillator has been done in Cadence Virtuoso in gpdk90nm technology. The different configurations implemented for comparison are Conventional VCO structure, VCO with Reverse SB technique and Differential structure. The simulation results obtained clearly shows that the reverse SB technique used is very helpful in improving the delay of the VCO. The minimum delay observed in reverse SB technique is 8.27picosecond which is comparable to the minimum delay observed in differential architecture.

A comparative study is also made for the frequency range observed in this work for both differential structure as well as reverse SB technique with the frequency range observed in the previous work done. The comparison with the previous data shows that in this work the frequency range is improved as much as twice the value observed in the previous work done.

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