DESIGN OF LOW POWER SRAM ARCHITECTURE USING 18 nm FinFET TECHNOLOGY

A

Thesis

Submitted in partial fulfillment of the requirements for the

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DOCTOR OF PHILOSOPHY

In

Electronics and Communication Engineering

By

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LOVELY PROFESSIONAL UNIVERSITY

PUNJAB

2021

DECLARATION

I hereby declare that the thesis entitled "DESIGN OF LOW POWER SRAM ARCHITECTURE USING 18 nm FinFET TECHNOLOGY" is submitted by me for the Degree of Doctor of Philosophy in Electronics and Communication Engineering is the result of my original and independent research work carried out under the guidance of **Dr.Suman Lata Tripathi**, Professor, Lovely Professional University, Punjab. It has not been submitted for the award of any degree, diploma, and associateship, fellowship of any University or Institution.

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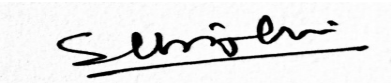

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Abstract

The scaling of transistors in to nanometre for better speeds and power consumption which is done according to the International Technology Roadmap for Semiconductor (ITRS)-2013 report, has a positive drive in the industry and also the usage of silicon based devices increased. , scaling trend of advanced commercial chips from 1950 to 2020 is identified. We have clearly observed the evolution of the microprocessor from 4004 to Core i7 with the increment in number of transistors per Integrated Circuit. To achieve this, the size of the transistor is reduced which further acts as a challenge for Nanoscale MOSFETS. These challenges influence the performance of the MOSFET based SRAM cells particularly below 65nm technologies. To overcome these challenges, various advanced MOSFETs were introduced such as DG-MOSFETs, TGFETs, SOI MOSFETS, FinFETs, etc. FinFET has been chosen as a transistor of choice because it is not affected by Short Channel Effects. The problems with FinFET have been observed and accordingly objectives have been decided. The present day semiconductor devices most part of the device is utilized by SRAMs so it is necessary to have these devices consuming less power and also dissipating less power.

In this thesis, an extensive literature survey has been conducted to select a best procedure for proposing a SRAM which has better performance, stability and low power consumption. In this regard a detailed evaluation of CMOS based SRAM cells is done in terms of static noise margin, Leakage current, power consumption and power dissipation, Subthreshold leakage currents for 6T, 7T, 8T, 9T, 10T, 12T at 45nm CMOS technology and comparison of the above parameters is done where the leakage currents are 61nA,59.7nA,62.9nA,64.9nA,65.4nA,67.6nA respectively and power dissipation is found to be 15.4μW,12.8 μW ,22.3 μW ,34.6 μW ,42.7 μW ,51.3 μW respectively and found that 7T SRAM has better performance among all the transistor topologies.

Further SRAM is designed by using 18nm FinFET technology ,where the designed 6T , 7T , 8T , 9T ,10T ,12T topologies have leakage current of 51.31nA , 50.26nA , 52.63nA , 52.87nA , 53.32nA , 54.12nA respectively and the power dissipation of 35.91nW, 35.22nW, 36.84nW, 37.1nW, 37.32nW, 37.88nW respectively. Its performance is compared with that of the same topologies designed in 45nm CMOS technology. The leakage currents and power consumption and dissipation of these SRAM cells are compared. It is found that the 7T SRAM has better performance than other SRAM because of the proposed design in which the power consumption is reduced by 40% because of the reduced switching activity employed in the design

And to reduce the leakage currents the leakage reduction techniques are applied to the proposed 7T SRAM cell and by applying the SVL technique the leakage current is reduced by 84.9% and the leakage power is reduced by 87.3% in comparison to the 7T SRAM without applying the technique .whereas by applying MTCMOS method the leakage current is reduced by 75.9% and power by 70.1% and by AVL technique the leakage power has come down to 72.8% and current by 77.5% and another technique drowsy cache has brought down the leakage current by 82.6% and leakage power by 81.3% in comparison to 7T SRAM based on FinFET. It is evident that of all the techniques the SVL is better.

And the Proposed SVL method is applied to the circuits of other transistor topologies and it is found that the leakage current of 6T SRAM has reduced by 80.9% and power by 78.2%.and the 8T SRAM has a reduction of 81.5% of leakage current and 80.2% of leakage power. The 9T has 81.3% and 82.1% of reduction in leakage current and leakage power.10T and 12T SRAMs have 82.75%,80.72% and 83.3%,84.1% of the leakage current and leakage power respectively when compared to the 6T , 8T,9T,10T,12T FinFET based SRAMs respectively.

The process variation analysis is done for 6T, 7T and 8T SRAM cells related to the data retention voltage of SRAM cell to hold a Zero value.as the input is Zero to retain that value the voltage at the output should be less than 100mv as we are checking the device in OFF state .It is observed that in all the process corners at low temperatures the data retention voltage is minimum and as the temperature increases the data retention voltage also is increasing and at certain temperature it is constant for certain region and further increased to the maximum value at high temperatures. As observed the FS mode has least voltage for all three configurations, whatever voltage shown here is the leakage voltage and also it is found that whenever the device is operated in TT corner it has least leakage power compared to all other corners as both the transistors in this configuration operate evenly. Among all SRAM topologies 7T SRAM cell based on 18nm FinFET technology, have shown minimum power consumptions at all TT, SF, FS and FF corners. The layout of 6T, 7T, 8T are drawn and found the area to be 1.07, 1.2533, 1.286μM^2 respectively.

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LIST OF ABBREVIATIONS

Abbreviation	Abbreviation Meaning
VLSI	Very Large Scale Integration
CMOS	Complementary Metal Oxide Semiconductor
MOS	Metal Oxide Semiconductor
FET	Field Effect Transistor
DG FET	Double Gate Field Effect Transistor
TG FET	Triple Gate Field Effect Transistor
FinFET	Fin type Field Effect Transistor
SOI	Silicon on Insulator
nMOS	n – Channel MOSFET
pMOS	p – Channel MOSFET
SCE	Short Channel Effect
DIBL	Drain Induced Barrier Lowering
GIDL	Gate Induced Drain Lowering
SRAM	Static Random Access Memory
SNM	Static Noise Margin
RNM	Read Noise Margin
WNM	Write Noise Margin
nW	Nano Watt
μW	Micro Watt
pA	Pico Ampere
nA	Nano Ampere

WL	Word Line
BL	Bit Line
BLB	Bit Line Bar
VDD	Power Supply
GND	Ground

CHAPTER 1
INTRODUCTION

In the present day electronics a device named Metal-Oxide-Semiconductor Field Effect Transistor i.e. (MOSFET) which has 3 terminals is used for numerous applications based on the requirement. The electronic signals are amplified or switched on. In the year 1925, Julius Edgar Lilienfeld first proposed the fundamental functioning of the device. In this device, the voltage that appears on an oxide insulated gate electrode may perhaps be a cause of conducting channel among the source terminal and a drain terminal. The transistor can be a P-type or an N-type or it can be a mixture of both P-type and N-type called Complimentary Metal-Oxide-Semiconductor (CMOS).

Over the past decades, the most used device is CMOS based transistor. Due to constant scaling of a CMOS technology, there has been an incessant and steady growth in a silicon-dependent semiconductor industry [1]. Though, CMOS devices face many serious issues when scaling of a technology enters a nanometer design a reduction in gate electrode is observed where it loses its control over a channel. The issues include increase of on-current, increased leakage currents, lower reliability and yield problem, huge parameter variations, huge manufacturing cost, etc. To survive the developments made historically, varied inventions in CMOS device materials and its structures are proposed as well as explained in the literature.

To overcome the problems evolved due to scaling the CMOS devices beyond 65nm a new device i.e. FinFET structure is introduced in order to overcome the issues that are discussed above and been faced by CMOS technology designers during the design of a device beyond 65nm. FinFET based devices have been designed for solving the limitation of performance through enveloping the gate electron around the channel in place of keeping the gate electron on top of the channel.

1.1 History Of CMOS Device

In 1930, the fundamental term Field Effect Transistor (FET) was been patented in the name of Lilienfeld [2]. He suggested a structure having three-electrode making use of copper-sulfide (Cu2S) semiconductor material. Nowadays, it is called FET. It was finally used with Si-SiO_2 by Kahng and Atalla after thirty years, [3].

At Bell Labs, M. M. Atala and D. Kahng achieved the first successful insulated-gate field effect Transistor (FET) in 1960. This had been extended predictable by prevailing over the surface states which obstructed electric fields from entering into the semiconductor material by Heil, Lilienfeld and Shockley. After examining the thermally developed silicon-dioxide layers, they discovered that these states could be clearly curtailed at the boundary stuck between the silicon and its oxide containing layers of metal, oxide and silicon. This is how it got its name MOSFET, commonly known as MOS. The MOSFET has been integrated into IC‘s after that and has become the most vital device in the field of microelectronics.

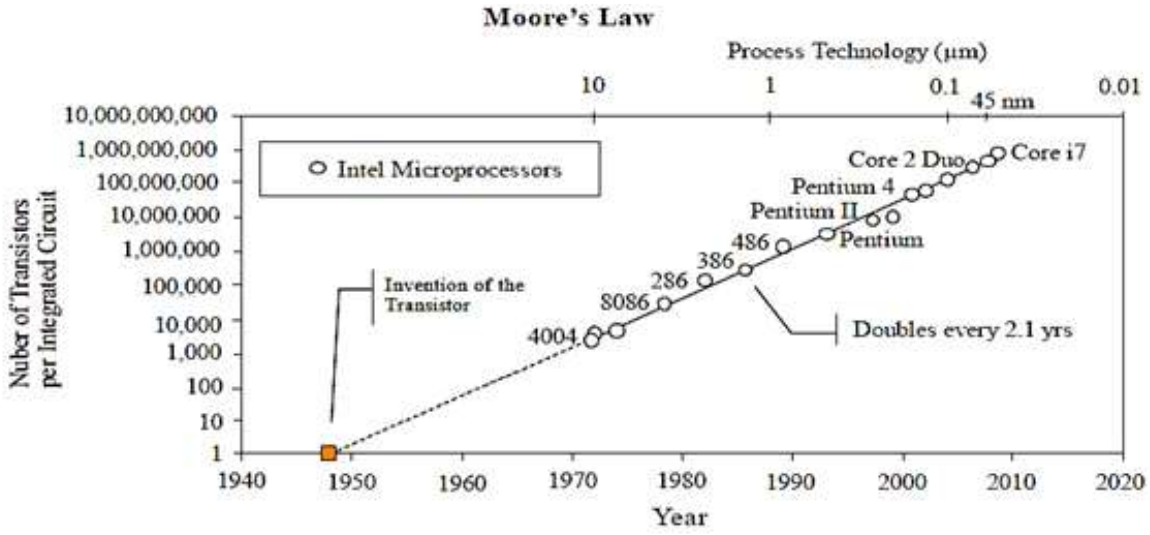

Figure 1.1: Moore’s Law

As displayed in Figure 1.1, the count of transistors on a chip doubled every eighteen months in the last few decades. This rapid rate of changed behavior of CMOS advancement, widely termed as Moore‘s Law, primarily motivated by the scaling of extended MOSFET [4]. This pattern has continued for more than 50 years and will continue till 2020 as per the literature report in 2005 [5]. However, according to the latest update in 2010 to the ITRS, the growth will slow down by the end of 2013. After this the density and count and of transistors will double after every three years [6].

1.2 Complications In Scaling MOSFET

The procedures beginning from a brief review of scaling pattern of bulk MOSFETs based on scaling and throwing light on the challenges to be resolved. Recent advancements to overcome these minute geometry impacts like threshold voltage variations, short channel impacts and increased leakage currents will also be discussed.

1.2.1 Scaling Of MOSFET

The notion of scaling is schematically illustrated in Figure 1.2 showing the doping concentration is scaling up and the device voltages and device measurements are scaled down using the similar feature. As per the electrostatics, the configurations of the electric field will be similar to that of unique device [7].

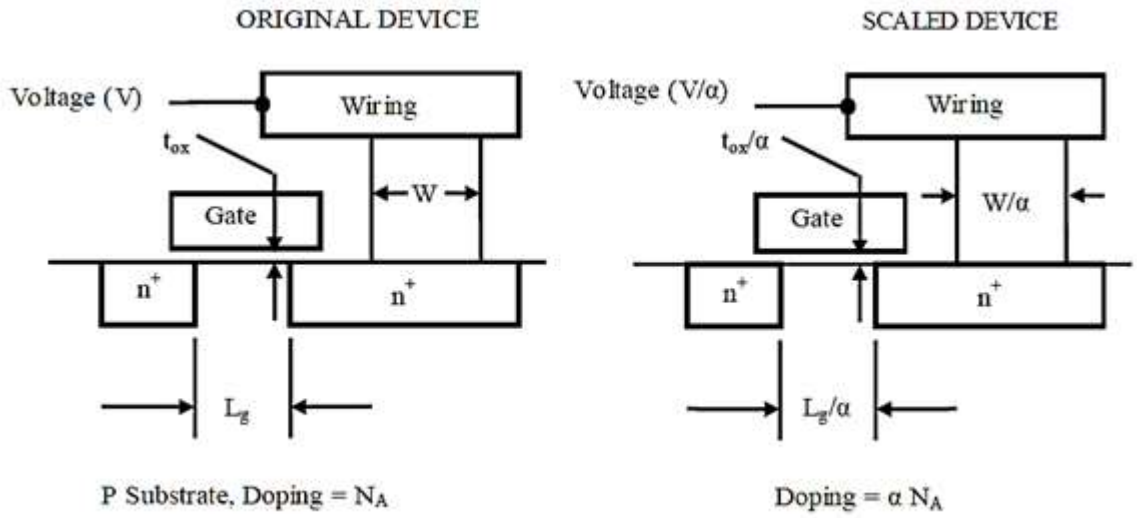

Figure 1.2: Principle of Scaling

Using the same behavior, we can scale down a large FET to a small FET very easily. There are set of rules which only provide us a directive that is used to compress a device [8]. However, they will not inform us how small the devices can be made. As the length of a channel get diminishes, a MOSFET current augments while an inherent capacitance gets decreased for a given layer thickness and given supply voltage. Consequently, the switching speed of MOSFET is enhanced. Nonetheless, the device channel length cannot be randomly reduced owing to Short Channel Effects (SCEs) namely punch through, threshold voltage roll-offs, Induced Drain Leakage (GIDL), Drain Induced Barrier Lowering (DIBL), Hot Electron Effect gate etc.

We have some other scaling limits enforced by a non-scalability of a silicon energy band gap and a thermal voltage, in addition to a scaling edge of channel length forced by SCEs. Non-scaling of silicon band gap energy results in non-scaling of build- in potential, short channel effect and width depletion. Furthermore, the non-scaling of thermal voltage results in subthreshold non-scaling. The physical aspects which are passed through the different barriers in a MOSFET device are controlled by a quantum mechanical tunneling currents. With the oxide thickness including 2 to 3 layers of SiO_2 atoms is being scaled towards 1.5nm, the oxide tunneling current leads to gate leakage, thus growing the standby power dissipation. Elements of these limitations have been concluded by D. J. Frank et.al [9]. There are different approaches to avoid these scaling limitations, carry on scaling down of MOSFEET without altering the thickness of an oxide; modify the structure of a device to be further scaled down while the effect of short channel is still under control for a physical insulator to have an effective thickness we need to change the material that is used at gate terminal.

As VLSI technology is reaching its edge there are some devices that need to be scaled down further. The three key devices are silicon on insulator, conventional bulk MOSFET and DG MOSFET. Most of the MOSFET's are affected by SCE when they are further scaled down [10]. In SOI MOSFET if it is fully depleted, then in channel region a drain electric field gets penetrated through an oxide layer. For DG MOSFET and bulk MOSFET the conducting layer present at the bottom of a channel can move the electric field away from it. Such that they achieve a better SCE than SOI MOSFET which is fully depleted. Whereas for a bulk MOSFET, the minimum length of the channel can be estimated roughly as [11].

$$L_{min} = 2\left(W_d + \frac{\varepsilon_{si}}{\varepsilon_{ox}}\, t_{ox}\right) \qquad \text{----------1.1}$$

Here W_d is the width of a depletion layer in bulk MOSFET from equation (1.1), during the scaling down of bulk MOSFET it is observed that t_{ox} and W_d both need to be reduced consequently. In bulk MOSFET for reducing the depletion width it requires an advanced doping in the substrate region. A junction capacitance is increased by the elevated doping that is done at substrate there by increasing the band to band tunneling current from a body to drain and declines the sub threshold slope by reducing the carrier mobility. In bulk MOSFET, Gauss law defines the surface electric field by the below equation.

$$\psi_S = \frac{Q_i + Q_d}{\epsilon_{si}} \quad \text{----------1.2}$$

Here Q_d is the depletion charge concentration and Q_i is the reversal charge sheet density. Due to the more amount of charge depletion, MOSFET devices are operated at a higher surface field for same Q_i that rise the mobility degradation.

Another area of growing concern in Nano scale MOSFETs device for ON-chip caches is the enhanced leakage consumption, Due to leakage current, consumption of energy for active mode devices is more than 40% [12]. As more number of MOSFETs transistors are packed onto ICs with every passing novel technology era, energy consumption of an active mode will be surpassed by leakage energy. Besides, in an idle circuit, the only source available for energy consumption is leakage. For instance, SRAM cells are principal basis of leakage as most of the transistors in present time‘s high performance ICs are used for on-chip memory caches [13]. The expansion of innovative robust memory circuit and a low leakage technique is thus, essentially required.

1.2.2 Effects of Scaling

The Short Channel Effects and threshold voltage variation are also important issues for nanoscale MOSFETs and affect directly the device speed, degrades the performance etc. These variations and its effects on MOSFETs are explained below in detail.

a.Sub-threshold leakage current-weak inversion conduction current

It is defined as the current that flows among the drain terminal and a source terminal that is controlled by diffusion current. When $|V_{gs}| < |V_{th}|$. This situation is believed to be a unique feature of a non- ideal MOSFET that acts as switching device, it adds to the leading areas of the stand-by leakage power dissipation. This can be showed through Equation (1.3) [14],

$$I_{subthreshol} = \mu C_{dep} \left(\frac{W}{L}\right) V_T^2 \left(exp\left(\frac{V_{gs}-V_{th}}{\eta V_T}\right)\right)\left(1 - exp\left(-\frac{V_{ds}}{V_T}\right)\right) \text{----------1.3}$$

Where

$$C_{dep} = \sqrt{\frac{\varepsilon_{si} q N_{sub}}{4\varphi_B}}, \quad V_T = \frac{KT}{q}$$

Here, μ is the charge-carrier effective mobility, C_{dep} depletion region capacitance in the gate area, thermal voltage is denoted by V_T,Boltzmann Constant is represented by K, Absolute temperature is given by T, Electron charge is denoted by q and its value is (1.6×10^{-19} C), η is the sub-threshold parameter, V_{gs} signifies the gate to source voltage, V_{ds} signifies the drain to source voltage, V_{th} depicts the threshold voltage, W denotes a channel width of MOSFET and L displays the channel length of MOSFET [15].

b. Threshold voltage variation

The variants of a threshold voltage (Vt) is correlated clearly with a sub-threshold leakage current and the device speed, which should be decreased and is normally explained in expressions of Vt falloff (or roll-off). A transistors residing in a wafer with same die have a different length of a channel and threshold voltage. Here reduction in a threshold voltage denotes Vt roll-off, which is result of the reduced channel length. Furthermore, reduction in V_t increases the drain voltage and it explains DIBL that is shown below in the Figure 1.3. Both the physical processes erupt from lower potential barrier amid the source and a drain because of comparatively increase of charge-sharing impact among the source to drain depletion regions and channel depletion region that is compared with a device having a long-channel [16-17]. A transistor is been created by an effect of charge sharing that needs low voltage at gate terminal for reducing the substrate below the gate dielectric by decreasing the Vt that was generated.

In any given technology node like the 90nm CMOS process, V_t i.e. threshold voltage relies on preference of an oxide and depth of oxide. If the thickness of the oxide is thin the threshold voltage will be low. However, it may perhaps be an enhancement in the performance; it does not come without a price. As the thickness of oxide is thinner for a given device its sub threshold leakage current will also be higher. As a consequence, for 90nm design specification the thickness of a gate-oxide was set at 1nm for controlling the leakage current [18].

This method of tunneling is termed as “Fowler-Nordheim Tunneling” [19]. Basically tunneling effect is the interpretation of a single object moving beyond an occluding object and then reappearing after a certain amount of time on the other side of it where as In Fowler- Nordheim tunneling, during high electric field presence, electrons tunnel through a barrier. Sub-threshold leakage current is the current that drifts from source terminal to drain terminal in an idle condition

of the device. When we reduce the thickness of the oxide, threshold voltage also decreases. This reduction in threshold voltage allows the devices to turn on even in small value of current which normally flows in the device at ideal mode.

$$If_n = C_1 W_L (E_{ox2})\, e{-}E_o E_{ox} \text{ ----------1.4}$$

Here, Electric field is denoted by Eox which lies across the gate oxide and C_1 and Eo are constants. Before scaling down the features of the design to 90nm, the solution to this problem was to create an oxide thickness by an approach of dual-oxide. In some cases an approach of triple oxide thickness was adopted [20]. For most transistors a single standard thin oxide was used, one more thin oxide is for an input/output driver cells while the third one is for pass transistor and memory cells. These differentiations are based purely on some features of a threshold voltage and oxide thickness of a CMOS based technologies.

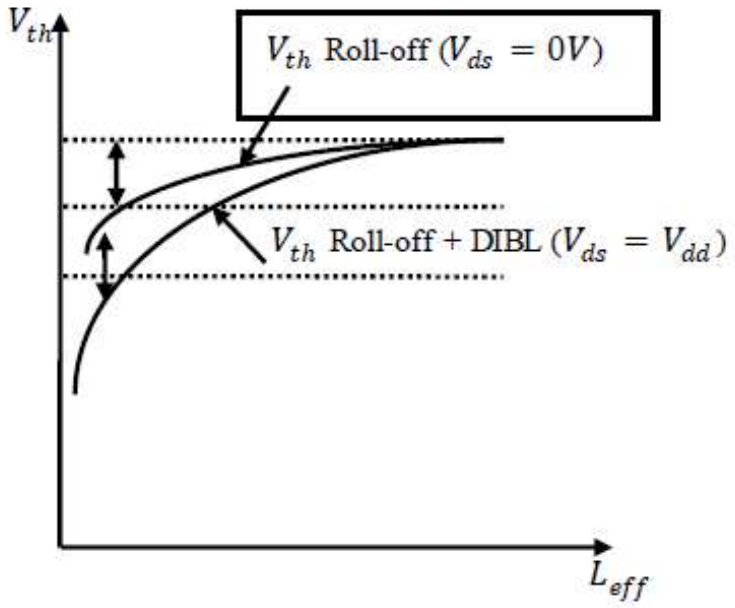

Figure 1.3: Voltage VS Channel length

C. Short-Channel Effect

A MOSFET device is termed as short if a channel distance has same magnitude as that of a width of depletion- layer of a source terminal (x_{dS}) and drain junction (x_{dD}). It is called as a short channel effects crop up as length of a channel length L and it is reduced to amplify the swiftness of process and the sum of modules present on a chip. [21-22].

Particularly, three different short-channel effects can be distinctly seen:

i. Drain-Induced Barrier Lowering (DIBL) and punch-through

ii. Impact Ionization

iii. Hot Electrons

i. Drain-Induced Barrier Lowering and Punch-Through

Punch-through takes place when a depletion regions that surrounds a drain extend to a source for merging its layers (i.e., when $x_{dS} + x_{dD} = L$). Punch-through can be reduced by having a larger substrate doping, shallower intersections, thinner oxides and a clearly longer channel [23]. The equations for a width of drain junction and source junction are given below [23]:

$$X_{dD} = \sqrt{\left(\frac{2\varepsilon_{si}}{qN_A}\right)(V_{ds} + \phi_{si} + V_{SB})} \text{----------1.5}$$

$$X_{dS} = \sqrt{\left(\frac{2\varepsilon_{si}}{qN_A}\right)(\phi_{si} + V_{DB})} \text{----------1.6}$$

Here V_{DB} is a voltage at drain-to-body, V_{SB} is a voltage at source-to-body, ε_{si} is permittivity of silicon material = 11.7 ε_o. ε_o is the absolute permittivity which is 8.854 × 10-12 F/m, N_A is the concentration of the accepter ion and ϕ_{si} is the built- in voltage of silicon material.

The channel‘s current flow is dependent on producing as well as holding an inverted layer on its surface. In a channel electrons will face a potential barrier which stops the flow of electrons, if the voltage at gate bias is not that sufficient enough for reversing a surface ($V_{gs} < V_{th}$). By cumulative a gate voltage, the barrier is reduced, finally allowing the carrier flow in the channel in the control of an electric field. A potential barrier is operated by V_{gs} and V_{ds} voltages in the small geometry MOSFETs [24]. In the channel the potential barrier decreases if there is an increase drain voltage, proceeding to lower the drain- induced barrier (DIBL).Finally the electrons flow in among the source to drain terminals due to the potential barrier reduction, even if the threshold voltage (V_{th}) is better than the gate-to-source voltage (V_{gs}). Under these circumstances the flow of a channel current is identified as the sub-threshold current [25].

ii. Impact Ionization

In NMOS, one more short-channel effect takes place in the electrons due to its high velocity in the existence of high longitudinal fields that generates an electron-hole pairs through impact ionization by having an impact on silicon atoms and ionizes them.

This is how it happens. Here drain attracts much of the electrons, whereas the holes move into a substrate region to be a portion of the substrate current. Furthermore, the region amid the drain and a source will work as base of a NPN transistor with a drain acting as a collector and a source as an emitter. Here the holes mentioned above are composed by a source terminal, and the current corresponding to holes generates a drop in the voltage of 0.6 V in a substrate material, a PN junction diode which is reversed-biased will efficiently conduct itself. From source terminal to substrate the electrons can then be inserted, as the electrons get inserted from an emitter terminal to a base terminal. Enough energy is attained as they move towards the drain terminal to create a pair of electron and hole. But the condition can deteriorate if few electrons escape the drain fields that were generated because of the high fields and move into a substrate, due to which other devices on chip gets affected. **[26]**.

iii. Hot Electrons

One more term called hot electrons is caused due to high electric fields. Generally, in a PN junction diode flow of electrons will be only in one direction. Normally flow of electrons cannot be either way, since there are junctions both ways between a drain terminal and a source terminal. When voltage is supplied to gate terminal, it produces an electric field below the gate pulling the electrons in and effectively changing the P-type silicon to N-type silicon. In addition, it also allows the current to flow. In the nanometer domain, fields and speeds have gone up, dimensions have shrunk so the electrons in the channels move very swiftly. The field in the gate draws the electrons, so they are pulled towards the gate rather than moving horizontally as depicted in Figure 1.4 [27].

On certain occasions, an electron will strike the oxide barriers quickly enough to partly break through and will ultimately wedge itself in the oxide. When this situation arises, the gate develops a permanent static charge. Depending on the type of device, this can result in the required gate voltage for electrons to either flow up or flow down. If it decreases, leakage currents shoot up and the power usage increases. In such a case, the previous device must supply a larger gate-source

voltage difference whereas the chip will require a higher power rail. This is one of the most ordinary failure modes for devices and only one who faces consistent problems knows. Many of such problems have arisen in the nanoscale MOSFETs like scaling, threshold voltage variation, sub-threshold leakage current and short channel effects. For overcoming these problems, advance MOSFETs like Double Gate, Triple Gate MOSFETs and FinFET devices are used. [28]

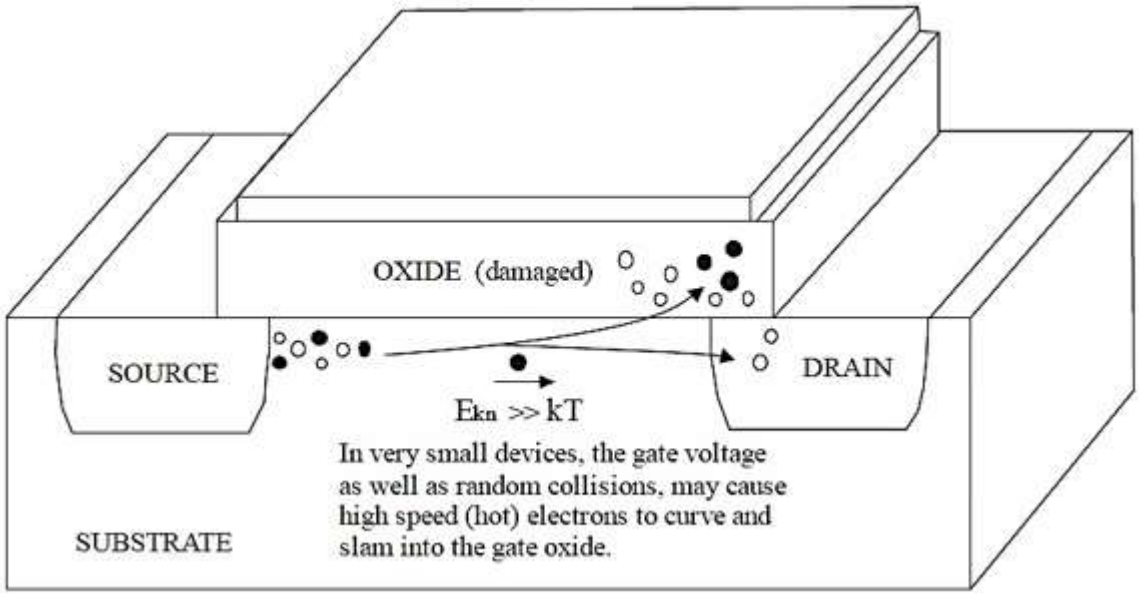

Figure 1.4: Hot Electron Effect

1.3Types Of MOSFETS

Novel technologies have been presented for continuous scaling of planar MOSFET device past the 60 nm. These comprise gate stacks of HK/MG and a technology based on channel stress (e.g. strained-silicon substrate [29], engravved-Si1-xGex (Si1-xCx) for a p and n-channels MOSFETs and raised source/drain [30-31]).

Meanwhile a channel region which is heavily doped or a halo doping is required by a planar bulk MOSFET in order to subdue the DIBL and a short channel effect it will suffer with a RDF effect. In order to avoid the usage of a heavy channel doping in recent years a new technique is been introduced called as Multi-gate transistor structures. [32].

1.3.1 Double-Gate MOSFET (DG MOSFET)

A generic N-channel DG MOSFET schematic exhibited in Figure 1.5. Arrow in figure denotes the gate dielectric layer (and spacer), $t_{ox,f}$ is thickness of a front gate dielectric layer and $t_{ox,b}$ is the thicknesses of a back gate dielectrics layers and t_{si} is the silicon body thickness. In a DG MOSFET, the channel is controlled by two gates such as; a front gate ($V_{g,f}$) and a back gate ($V_{g,b}$). This reduces the drain field impact on the source, thus resulting in a reduced Short Channel Effect (SCE). Owing to the increase in share charge from source terminal to drain terminal there will be a shrink in length of the channel and there is a decrease in threshold voltage due to the gate voltage control. Hence, a reduction in threshold voltage occurs with a decrease in a channel length and Drain Induced Barrier Lowering (DIBL). These factors are noteworthy concerns and need to be taken care to provide the protection against a Short-Channel Effects (SCEs) [33-34]. A novel technique called Dual Material Gate (DMG) MOSFET was designed and suggested for improving the immunity in contrast to short channel effects. [35-38].

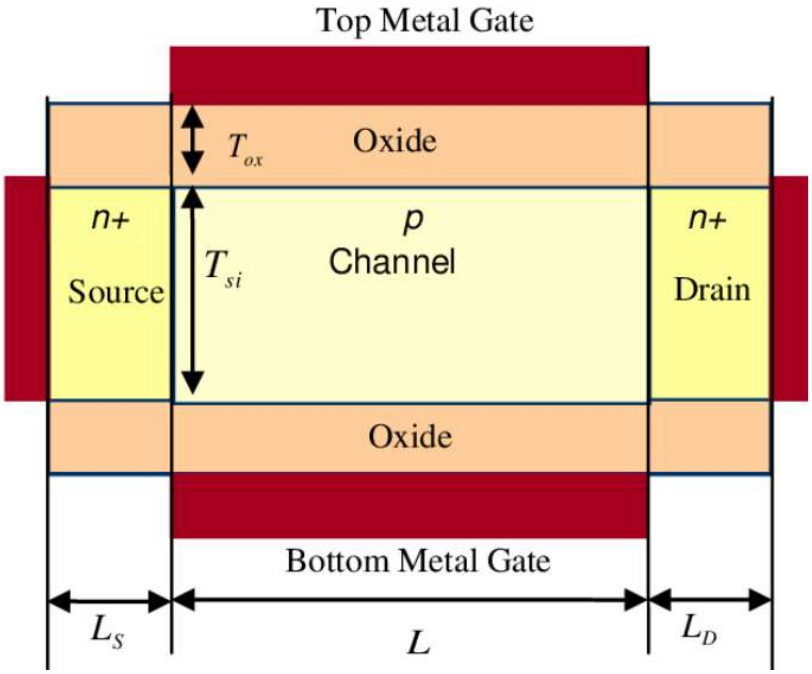

Figure 1.5: Double Gate MOSFET

A Double Gate MOSFET having same thickness and material for a front gate electrodes, back gate electrodes and a dielectric material is named as symmetrical DG MOSFET . Conversely, a DG MOSFET that is not a symmetrical DG MOSFET is called an asymmetrical DG MOSFET [39].

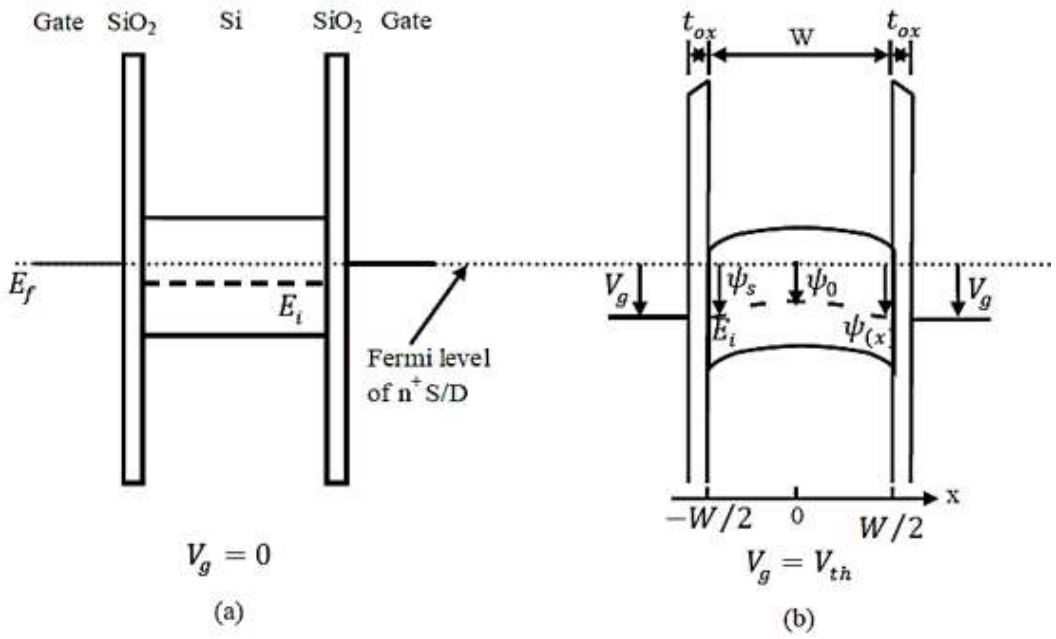

Figure 1.6: Energy Band of DGMOSFET

The two gate biases at a channel with their energy band illustrations for both symmetrical, asymmetrical DG MOSFETs are exhibited in below figure 1.6 and Figure 1.7. In a symmetrical DG MOSFET having a gate electrode at mid-gap, in a sub threshold region there exist flat bands in silicon, with a constant carrier concentration throughout the channel. When the gate bias is high the bands turn downwards in silicon region near to the sidewalls. When the bands are turned near or over the quasi Fermi level sufficiently, the density of the carrier near the sidewalls increases greatly. Thus, the transistor is powerfully inverted. Several definitions describe a precise inception of a robust reversal. The threshold voltage (V_{th}) is the gate bias that corresponds to an onset of a strong inversion **[40]**.

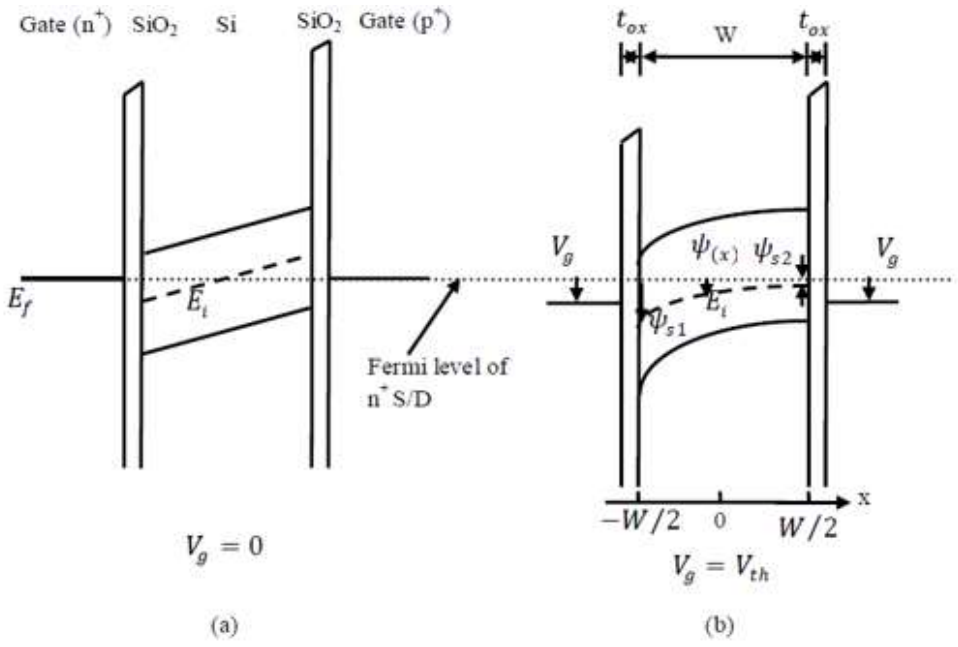

Figure 1.7: Energy Band of Asymmetrical DGMOSFET

1.3.2 Triple-Gate MOSFETs (TG MOSFETs)

A silicon body which is wrapped by gates and it is a non-planar narrow transistor is known as Triple-Gate MOSFET [41]. In this the gates control the two channels i.e. a top horizontal channel and a lateral channels. This MOSFET is made up of a thin film comprises of thin silicon base having a gate terminal on three edges.TG-MOSFET transistor find it's applications in a fully depleted transistors ideally. A TG MOSFET substrate has a thin body of semiconductor on it, with a gate dielectric on the top of surface and on the side walls of it. On a semiconductor body source region and drain regions are created at an opposite side of a gate electrode. A transistor has three distinct channels and gates because three sides of a semiconductor body is enclosed by a gate dielectric and gate electrode [42]. Here width of the transistors gate corresponds to the sum of three individual sides of a semiconductor body. A TG MOSFET 3D structure has been depicted below in Figure 1.8 that explains the dimension of a basic transistor.

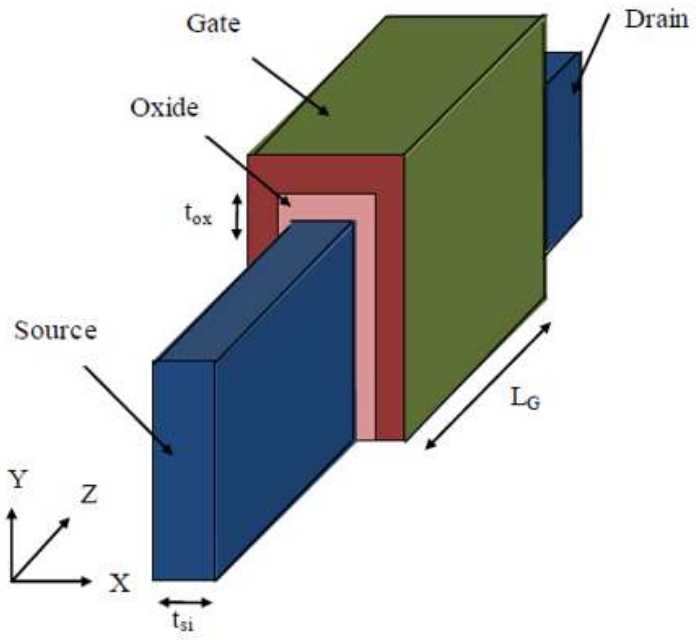

Figure 1. 8: Triple Gate MOSFET

1.3.3 SOI MOSFET

Silicon on Insulator (SOI) technology includes a usage of layered silicon-insulator i.e. instead of using conventional silicon substrate it make use of silicon substrate during the semiconductor manufacturing, specifically in microelectronics in order to progress the performance by reducing the parasitic capacitance of a device.[43]. SOI-MOSFET devices are different from conventional based silicon devices. This is for a reason that the electrical insulator is just below the silicon junction i.e. either a sapphire or a silicon dioxide. The selection of an insulator purely based on a proposed design application, like for short channel effects we can use silicon dioxide in microelectronics devices and for a high performance based radiation-sensitive applications and Radio Frequency we can use sapphire [44]. The top most silicon layer and the insulating layer also vary widely due to application [45]. Benefits of SOI MOSFETs over conventional MOSFETs are: due to isolation of bulk silicon a lower parasitic capacitance will enhances the consumption of power at matched performance; Due to complete isolation of both p-well and n-well there is a resistance to latch up; working on lower VDD and higher performance at equivalent VDD; Because of non-doping present there is a reduction in temperature; better wafer utilization, decreased antenna concerns; better yield due to high density; no need of well taps or body taps; due to isolation the leakage currents are lower with a high power efficiency; inherent hardened radiation (it is resistant for soft errors), need of a redundancy is reduced.

SOI MOSFETs manufacturing is well-suited with a most conventional fabrication process [46]. Generally, an SOI-based process can be applied without a help of any specific device. The main obstacle in the implementation of a SOI is the substrate cost which is increasing drastically, that leads an estimated increase in the value 10–15% of an overall manufacturing costs [47].SOI based MOSFET devices are used by the computer industry. SOI devices are basically of two types: PDSOI (Partially Depleted SOI) and FDSOI (fully depleted SOI) MOSFETs [48]. For an n-type based PDSOI MOSFET, a p-type film which is inserted in between a buried oxide (B_{ox}) material and gate oxide (t_{ox}) material is large; therefore whole p region cannot be covered by the depletion region. PDSOI up to some extent acts similar to a bulk MOSFET. FDSOI is more advantageous compared to bulk MOSFET. In FDSOI devices, as it contains a thin film so it covers a whole depletion region. A front gate ($t_{ox,f}$) supports a less depletion charges compared to the bulk MOSFET in FDSOI so inversion charge get increases which helps to achieve a switching speed at higher rates. Other disadvantages in a bulk MOSFETs are high sub-threshold slop, threshold voltage roll off, body effect, etc. and are decreased in Fully Depleted SOI because the source electric field and drain electric fields may not be able to interfere with each other due to B_{ox}. In PDSOI the main fault is a "Floating Body Effect" (FBE) as the film in it is not associated to any of the given supplies. The 3D-structure of a SOI MOSFET is shown in Figure 1.9.

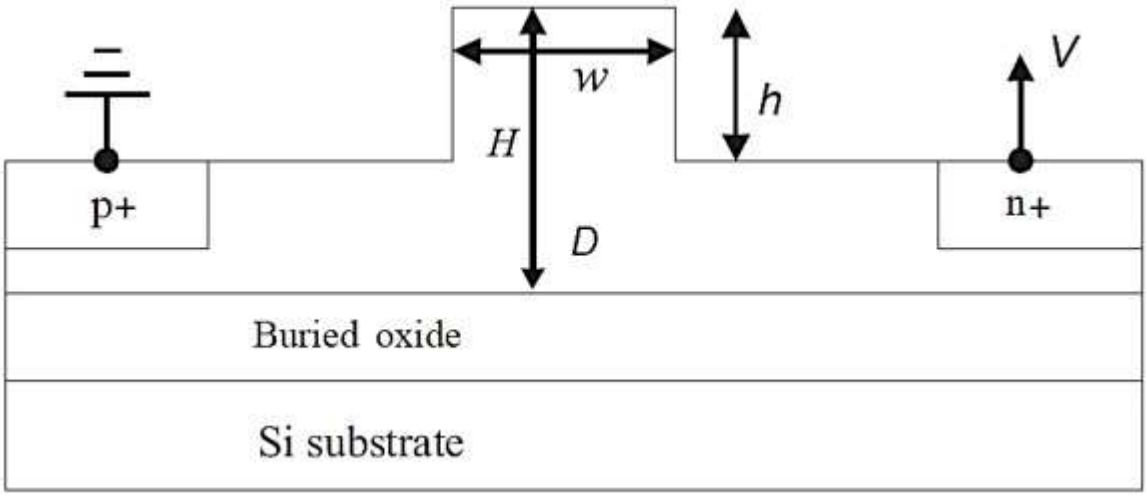

Figure 1. 9: SOI MOSFET

In Bulk silicon MOSFET, parasitic capacitances between drain / source junction and interconnects are formed which degrade the performance of the circuit. Latch up was also a serious issue for bulk CMOS circuit [49]. In Figure 1.9, a buried oxide layer has been introduced between the substrate and p^+ n^+. With this implementation, junction capacitance is found to be smaller than the bulk silicon MOSFET. Other than this advantage, SOI MOSFETs provide latch-up free CMOS

technology, and has an ability to get operated in harsh environments having a higher radiation rate and high temperature, operated at a low voltage, etc. [50].

1.3.4 FinFET Devices

It is difficult to fabricate planar DG MOSFETs [51-52]. The difficulties faced are alignment of a gate at top region and bottom region and to make a low resistance contact with a gate at bottom region. Another variation of a DG MOSFET is fabricating it easily as FinFET [53-54]. Figure 1.10 depicts a FinFET structure. In order to construct a DG FinFET the oxide present on top is abundant denser than the side walls to disable the top gate effectively.

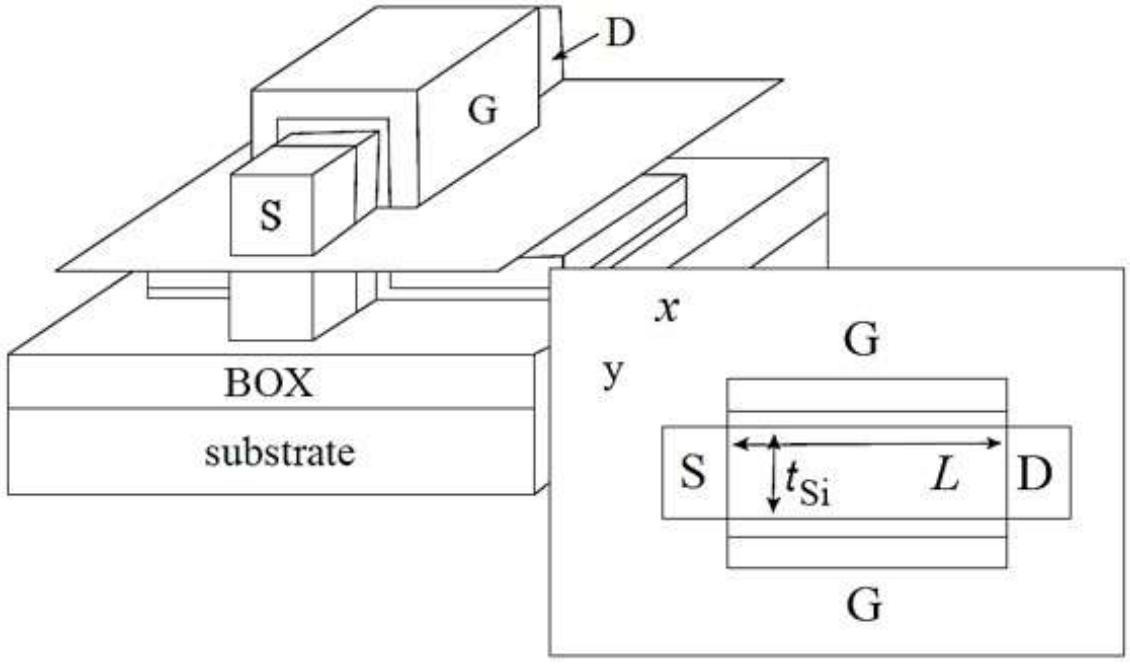

Figure 1.10: FinFET 3D View

Evidently, a double-gate FinFET width is defined by an equation as W = 2Hfin + Wfin. In most of the cases, to have a short channel effect sufficiently smaller, Wfin is of a small order. Moreover, a top gate in DG FinFET is ineffective so, W is nearly 2Hfin. Accordingly, the behavior of FinFET device turns out to be large, same like a DG MOSFET. Thus, the literature that been studied gives the compact idea of designing a DG MOSFET's model and it can be easily implemented with a small adjustment of parameter i.e. (Hfin) to FinFETs, as it is done in [55].

An extension region in fin is a long narrow portion that is not in the gate. This region is technologically unavoidable because there is no probability of having a doping gradient of steep

lateral, which starts from a highly doped region and ends at lightly doped region. Basically a body that is blithely doped is chosen as it will decreases the corner effects [56- 58], effect of a mobility degradation and a random dopant fluctuations. Therefore, FinFET devices typically will have large parasitic series resistance.

1.4 Memory Organization

Memory organization mainly consists of three basic parts as shown in Figure 1.11

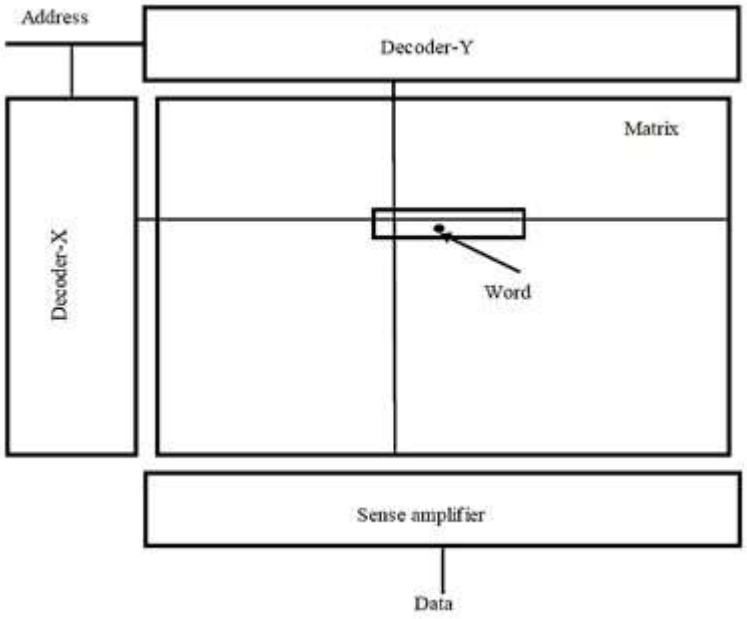

Figure 1.11: Memory Organization

At first the actual data is stored in cell matrix in word format whose length is predefined. Based on the two inverters and there positive feedback loop the data is stored in cell. The positive loop here provides the static retention of data without refreshing it. In order to access the cell we do it through bit lines to a sense amplifier. Here sense amplifier is the secondary part of a cell matrix used for translating a signal with low swing i.e. generated on a bit lines by a cell to a digital signals having full levels. Decoder is a third main part used for decoding the given address into a physical position. Some other peripheral circuits like timing and control unit, write system and pre-charge system are needed. One of the critical situations is to activate all the subcomponents at a particular time in the given memory. As it play a dynamic role in the functionality of device, consumption of power, delay in memory. A word line that is turned ON will cause an access of wrong address. If it is turned ON late it will have a delay of overall memory. The timing of activating a sense

amplifier is critical, as if the activation is done too soon, will prompt a bit-line pair to generate the differential voltage i.e. needed. Throughout a write process all the bit lines will be fetched to correct levels before the pass transistors are enabled. For a conventional cell, one of the bit line is discharged fully whereas the complementary vit line is kept high. [59].

1.5 Conventional SRAM Cell

The SRAM cell includes a latch consisting of 2 inverters which are connected cross coupled, such that it need not be refreshed periodically to retain the data that is stored. Based on the condition that for a given SRAM cell an ample of power supply voltage is present. [60-61].

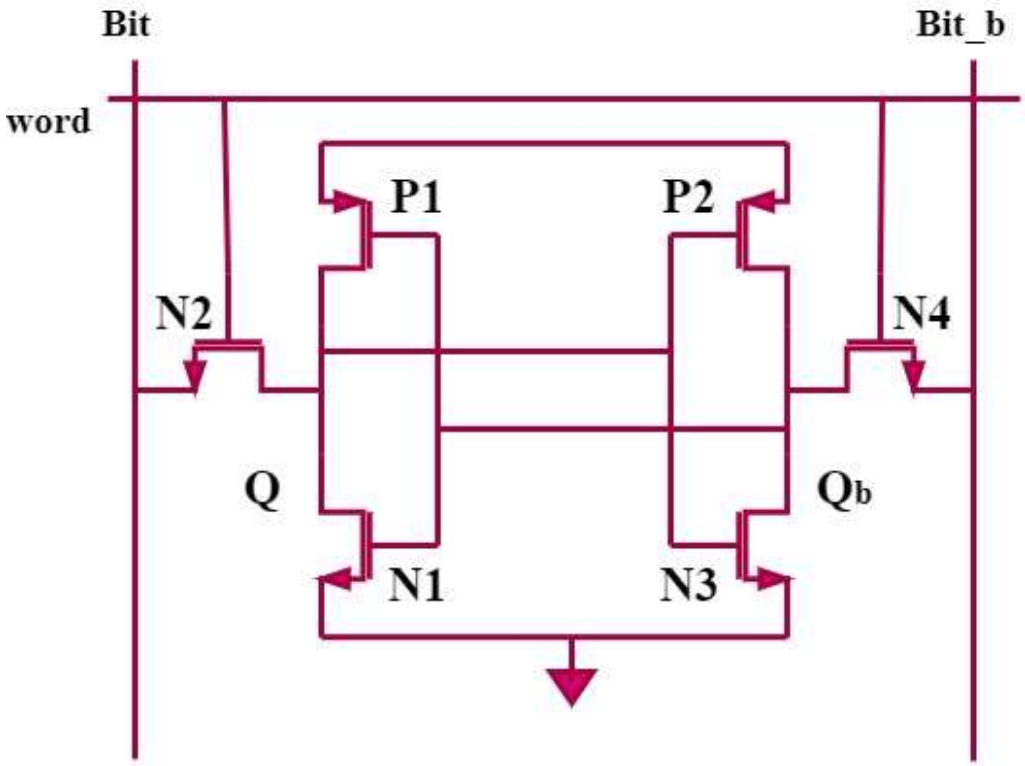

Figure 1.12: 6T SRAM

A 6T SRAM is shown in Figure 1.12 which has 2 inverters connected to each other and 2 more transistors which decide the functionality of these two inverters. The two transistors N2 and N4 are connected to a bit and bit_b line and both together are connected to word line. [62-65]
Here a read, write and hold operations are performed depending on the modes of selection of the bit and bit_b lines. And data input to the device depends on the bit given through word line.

1.6 Research Gap

The prediction of device performance of FinFET structure for SRAM cell design, simulation of 2D/3D device is inevitable. In some research papers, FinFET 2D/3D model has been proposed, and a detailed study of output characteristics variation with process parameters variation, device structure, temperature effect, etc have been not carried out.

To the best of our knowledge, very few research papers have actually dealt with the leakage aspect of FinFET. The study is critical in order to analytically estimate simulation otherwise the power dissipation of Fin FET is under bias. Band to Band Tunneling (BTBT) and Evaluation of Edge Direct Tunneling (EDT) have not been reported extensively for the FinFET device.

It is felt that the conventional bulk CMOS SRAM should be preceded by Nano scale semiconductor novel devices in order to appreciate the qualitative behavior of FinFET under various bias/process condition. There are few reported research papers in the area of process variation which are aware of the SRAM cell based on FinFET. No advanced SRAM cell has been proposed for FinFET based structure.

The study of advanced SRAM cells i.e. 7T, 8T, 9T, 10T and 12T SRAM under all conditions of temperature/process parameters variation would be required for determining the driving capability of FinFET structure for low power applications. At subsystem level, very small number of work has been reported on FinFET based SRAM design with process variation and temperature effects. Most of the papers in this area are based on fabrication/process technology for generation of SRAM cell by bulk MOSFET or DG MOSFET. The Static Noise Margin (SNM) has been reported in number of papers but its variation with process parameters and device structure is not elaborated. The evaluation of RNM and WNM is highly appreciable from stability point of view.

There are possibilities to extend research work in all area of work, as no work is complete as knowledge is infinite. To go further, we briefly point out some directions in which further research may be carried on.

i. The analysis of FinFET device structure with single Fin is available. Multi-Fin FinFET device can be used to enhance the driving capability of the device. However the fabrication techniques required to meet such stringent guidelines would be an issue which can be looked into in future.

ii. The available design of FinFET based SRAM cells, gave reasonably good results. However, if even better results are required then technology must be scaled down.

iii. A substantial decrease in leakage current and power dissipation has been witnessed in available SRAM cells. As the leakage will be more significant in scaled down technology like 18nm, so this work further may be extended to scaled technologies such as 7nm or beyond.

iv. There can be several other leakage reduction techniques apart from those which are proposed. So in order to further improve the performance, new leakage reduction techniques may be proposed and implemented for future work.

v. The different spacer materials can change the potential modeling and hence various leakage components estimation is expected to change in FinFET device. This might be a good area of further research.

1.7 Research Objectives

The objectives of the proposed research work are as follows:

1. Analysis and design of advanced SRAM cell (i.e. 7T, 8T, 9T, 10T, and 12T) based on CMOS and FinFET device in Nano scale domain.
2. Performance evaluation of FinFET based SRAM cells at 18nm technology node for low power applications.
3. Modelling and estimation of total leakage current in Nano scale FinFET based SRAM cell considering the effect of parameter variation using different leakage reduction techniques.

1.8 Thesis Organization

A Continuous literature survey was done for identifying the problems associated in convention SRAM cell and also the problems associated with scaling of MOSFET. And the alternate devices for MOSFET that can replace the devices and with great stability, speed and low power consumption. The existing gaps were identified related to the existing architectures through the literature survey and are presented in Chapter 2.In Chapter 3 the design of 45nm CMOS based 6T, 7T, 8T, 9T, 10T, 12T SRAM is done and analysis of these SRAMs in terms of SNM,Power consumption is done . In Chapter 4, the study of 18nm FinFET based 6T, 7T, 8T, 9T, 10T, 12T SRAM is illustrated. Various leakage reduction techniques are proposed in Chapter 5 to reduce sub-threshold and total leakage current on different FinFET based SRAM cell. In Chapter 6, effects of process variation on SRAM and layouts of 6T, 7T and 8T have been explained and the outcome

of temperature on power consumption is also presented. Finally, conclusion and future scope are presented in Chapter 7.

Figure 1.13: Thesis Organization

1.9 Chapter Summary

In this Chapter, scaling trend of advanced commercial chips from 1950 to 2020 is identified. We have clearly observed the evolution of the microprocessor from 4004 to Core i7 with the increment in number of transistors per Integrated Circuit. To achieve this, the size of the transistor is reduced which further acts as a challenge for Nanoscale MOSFETS. These challenges influence the performance of the MOSFET based SRAM cells particularly below 65nm technologies. To overcome these challenges, various advanced MOSFETs were introduced such as DG-MOSFETs, TGFETs, SOI MOSFETS, FinFETs, etc. FinFET has been chosen as a transistor of choice because it is not affected by Short Channel Effects. The problems with FinFET have been observed and accordingly objectives have been decided.

CHAPTER 2
LITERATURE SURVEY

Over a year there is an increase in the cache memories that are designed based on SRAM used for different applications that requires high speed such as multimedia devices, mobile phones and few portable devices. As we know that in an integrated circuit the major concern is speed and low power performance at a Nano scale technologies as demand of VLSI chips is increasing in computing devices mobile communications. As there is an increase in battery powered smart devices and its usage is wide spread similarly a Nano medical devices, where a low power is turned to be a big problem for system on chip design (SOC). For analyzing a SOC, a low power based SRAM is considered as it occupies a large portion in SOC chip and increases the overall power of the device. If a SRAM cell is used at higher frequencies it will consume more power and if we use SRAM cell for less speed applications then it will consume a negligible power. There are various techniques in SRAM based cells for managing the power.

2.1 FinFET Device

Kumar Gupta et al. has discussed a problem based on conventional planar MOSFET that are shrinking more when compared to CMOS devices in a nanoscale regime. In transistor one of the limit that effects the scaling is short channel effect (SCEs). Some effects like Gate Induced Drain Leakage (GIDL), hot carrier effects, Vth roll off, sub-threshold leakage, gate direct tunneling leakage, Drain Induced Barrier Lowering (DIBL) will result in degrading the performance of a BULK CMOS device. Different methods like a shallow source/drain junctions, having a high channel doping with a thin di-electric gate electrics that are deployed for improving the control on gate and thereby enhancing a performance by scaling down the gate length. With a reduction in power supply, hot carrier and power effects are downgraded but it will degrade the performance, and it can be improved by decreasing the threshold voltage $V_{th,}$ but it will affect the leakage obtained at Source/Drain terminals. [66].

The thickness of oxide can be reduced by decreasing a DIBL and will increase the adequate channel control with a change in gate terminal but it also increase the leakage current produce at gate terminal. [67]. Hence solving one issue will create another issue. Hence efforts are made to for finding a high K gate dielectric by a thick oxide which will reduce a gate leakage, and will

have a sufficient control on channel. A problem based on band alignment and instability problem of band is studied by various researchers for replacing a metal gate electrode by a polysilicon [68-69] and here insufficient activation will rise the poly depletion effects.

Here based on various work functions a metal gate has not been founded. In its absence a poly silicon gate can be used wherever the threshold voltage is established to high by doping the channel. It leads to a Random Dopant Fluctuations (RDF) (where length of the gate is small) it will reduce the mobility with an increase in impurity scattering. So , it is strongly recommended that in place of planar MOSFET a Field Effect Transistor (FET), Fin Field Effect Transistor (FinFET), Ultra-thin body (UTB) and Double- Gate Metal Oxide Semiconductor Field Effect Transistor (DG MOSFET) may be used for continuous scaling down of gate length to 32 nm technology [70]. FinFETs devices are utmost promising devices instead of other bulk CMOS devices at nanoscale regime as they have double gates in it. These two gates can be independently organized to decrease the leakage or to enhance the performance or to decrease the count of transistor used for a design. [71].

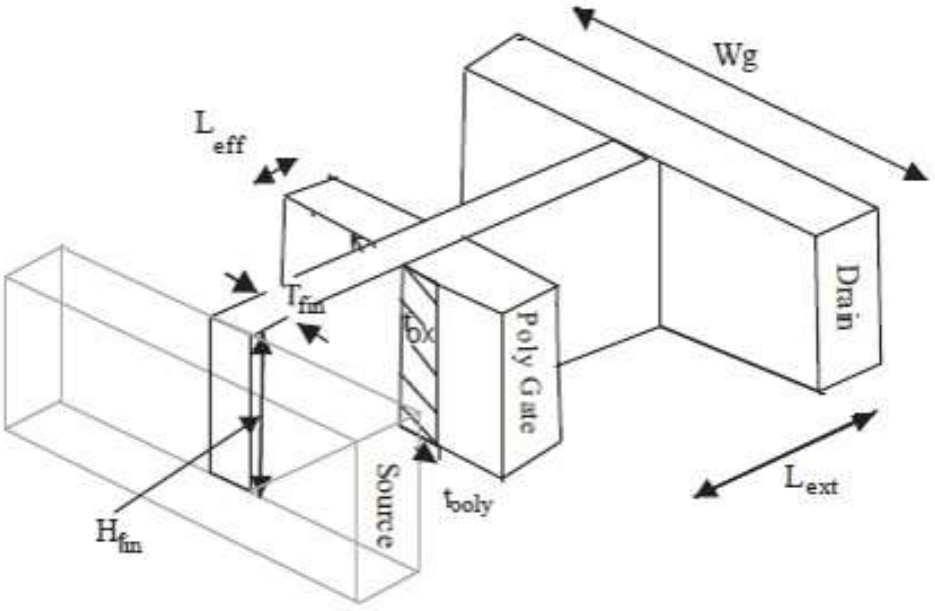

Figure 2.1: FinFET Device

Here author has proposed a novel model of schottky MOSFET i.e. double gate metal source/drain (MSD) and simulated it. The designed structure novelty is it realizes a CMOS inverter completely,

that is generally realized by grouping MOS transistors a P-type transistor and N-type transistor in conventional CMOS technology. By using the designed structure we can reduce the number of transistors used for an implementation of sequential and combinational circuits and also regions and junctions required are reduced when compared to CMOS technology. Hence a designed device is termed as Sajad-Sunil-Schottky device (SSS) and its design is compact and also consumes very low power. For proposed design a mixed mode circuit analysis has shown that a conventional CMOS inverter with logic level high i.e. (V_{OH}) as V_{DD} and low logic level i.e. (VOL) as GND. [72]

In paper [73], for improving the Figure of merit an exploration of a (Dual-KS) Trigate FinFET structure was used by considering only source for operating low power devices at gate length of 20nm, it is observed that the design rises the combination of gate and underlap region to source side and also improves an output conductance (g_{ds}) and trans conductance (g_m). During the observation it is found that at drain it increases the coupling of gate field to an underlap region to drain side and that makes the drain field to move away from a gate by improving the output conductance (gds) only when there is an increase in miller capacitance. [73]
Fin type FET's are most favorable alternate for a bulk CMOS devices at nanoscale operation. In general FinFET's are termed as double gate devices. Here the FinFET dual gates are shortened for achieving a high performance and the gates are controlled independently to achieve low leakage current or to decrease the number of transistor. This parameter will also give a compact design. This particular paper gives an overview on different set of design styles of FinFET logic, novel design and its layout's. [74]

In this paper a FinFET architecture that has been designed at 22nm has provided an improvement of MOSFET electrostatics and also enable L gate i.e. length of gate and it is scaled down at 48-nm technology, contacted gate pitch (CGP) scaled down at 7 nm technology by "Fin Effect" an enhanced performance gain has been achieved that has improved a drive current for the applied load capacitance. An approach on limiting the thickness of Fin is on study that will limit the scaling of L gate further and results in the size reduction of source and drain with CPP. An increase in the combination of L gate plateau and Fin effect place an extreme force on the conduction of vertical path from contacts towards source/drain. Based on contact resistivity values for a metal layer to dope the silicon degenerately of -2×10^{-9}. The performance of FinFET will drastically decreases

below -40nm that of CPP, while an ohmic floor of ~$1\times10^{-10}\Omega$-cm^2 can push the CPP under 30nm. Therefore from this a conclusion is made that electronic industry will have high pressure for adopting a novel architecture for designing a circuit or for scaling it in CPP region of 30-40nm, for carrying the benefits of power and performance of CMOS device scaling. [75]

In FinFET a scalable model and analytical model for a threshold voltage is developed by a 3-D Poisson equation and solving it by various techniques, as the model is based on an investigation of transmission path and a movable charge need be solved that was considered in Poisson 3D equation. Whereas the threshold voltage is termed as a voltage charge density. As the FinFET has a 3-D basis and a design model has an influence of short channel and roll off the threshold voltage and DIBL effect. A 3-D simulation of FinFET is observed. [76]
As CMOS basic IC technology scales down to a 14nm technology and sub 14nm technology based on Moore's law, one of the most favorable architecture selected is Si-Bulk FinFET as it has quiet few advantages as high transmitter performance, low leakage and high density. Thought the length of gate continuously scales down, a short channel effect and rolling of Vth is a serious issue that needs to take care off. This paper demonstrates two different mechanism, where a n-type FinFET are induced by a fluorine diffusion from a tungsten to a gate layer which is of metal and in situ a high phosphorous is deposited that will give a meaningful development of FinFET beyond 14nm technology.[77]

As planar MOSFET faces an issue of getting scaled at nanometer regime, FinFET devices and Trigate FET's have emerged as there successor that owns two or three gates in it and are capable to handle the short channel effect better than a general MOSFET structure at deep scaled down technology and enable for continuous scaling of transistor. Here a review is done on FinFET from device level to architecture level based on the various types of FinFET and it is possible asymmetric, their impact, novelty and trade-offs. [78]

When compared with conventional MOSFET, a FinFET based device is more suitable for decreasing the leakage current and power dissipation by improving the performance. While to move forward with parameters such as performance, integration, low-power and stability. A perfect FinFET is the solution for designing a SRAM cell. A proposed nanoscale based FinFET at

low-power 6T SRAM is been designed at 32nm and 45nm technology in Cadence Virtuoso Simulator.

2.2 Conventional 6T SRAM Cell

A conventional 6T based SRAM represented in Fig 2.2, consist of dual transistors that remain cross coupled and two excess transistors; here an inverter is crossly coupled and it is called as latch. Here two inverters that are cross coupled consist of four transistors (M3, M4, M5 and M6), where an each bit is stowed on all four transistors. M1 and M2 an excess transistor has its source terminals connected to input latch whereas drain terminals of transistor is connected to the Write Bit Line (wbl) and Write Bit Line Bar (wblb), and when Word Line is made low (wl = 0), the bit lines will be detached from a latch by turning OFF the excess transistor. During this state a latch will able to hold a bit as long as voltage is V_{DD} and GND. When a Word Line is made high (wl = 1), the bit lines (wbl and wblb) both are attached to latch and excess transistor will turn ON. At this point the bit lines will transfer the data for both the operations read and write.

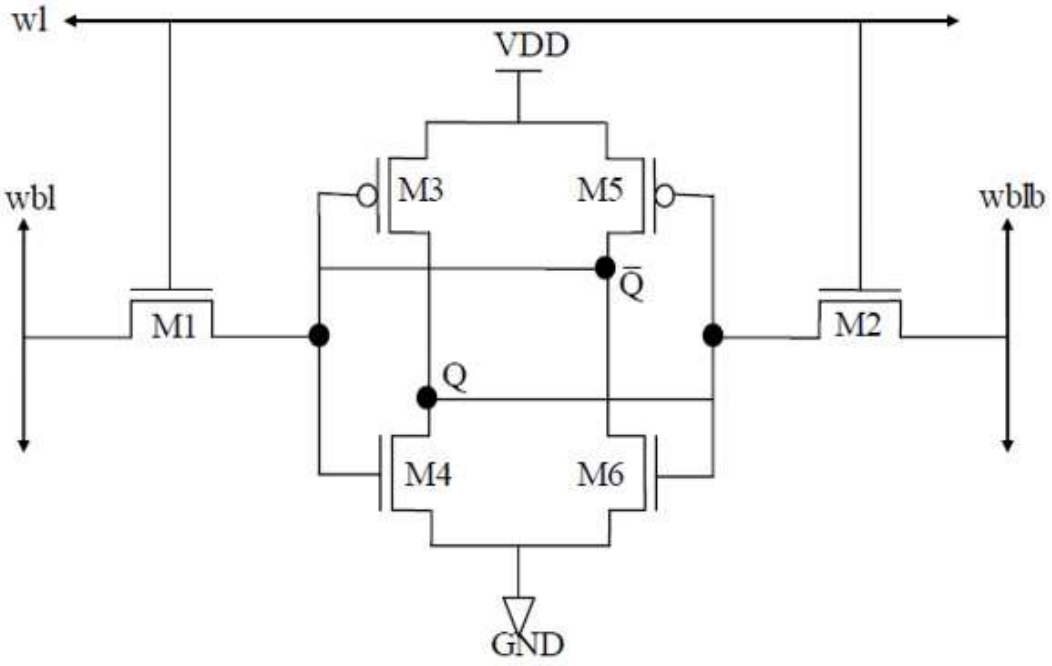

Figure 2.2: 6T SRAM

2.3 Design of 6T SRAM Cell using FinFET Device

Here a FinFET is proposed for low power based robust SRAM's that has an unequal drain doping and source concentrations i.e. asymmetrically doped FinFETs. Where an effect of its doping on characteristics of device is examined and the elementary changes among conservative FinFETs and AD FinFETs are shown. In device an asymmetry leads to an unequal current for both drain biases i.e. positive and negative and it exploits for achieving easing of read-write conflict in 6T SRAMs. A proposed design exhibits a higher short channel features related to a conventional FinFET because of reduction in electric fields from a terminal which has low doping and will result in a low leakage current. [79]

In conventional 6T SRAM few of the major challenges are reducing the leakage current, power dissipation by enhancing the performance of design. Figure 2.3 shows the displays the advised structure of 6T SRAM cell by using a Double Gate FinFET device. A proposed design of SRAM having 6T will reduce power dissipation, leakage current and has improved the performance too. Hence it is clear that optimizing a FinFET device properly is essential for leakage reduction and to provide stability. Therefore a supply voltage (V_{DD}), threshold voltage (V_{th}) optimization and Fin height H_{fin} is applied FinFET based SRAMs for leakage reduction thereby increasing the Fin height that reduces a supply voltage (V_{DD}) [80].

As V_{DD} gets reduced there will be a negative effect on stability of cell with various parametric variations. Thus an optimization technique is required by a FinFET for reducing a standby leakage current and for improving a stability in design of SRAM cell.[81].

SRAM contains a significant proportion of area and power that is used as cache memory in all VLSI chips and in SOC. It is considered as more intense handy devices and the processors that are high end. SRAM plays a vital role in world of microprocessors as there is scale down in technology in nanometer mode. The problems that affects the SRAM are leakage power, leakage current and delay present for low power based applications. Hence with a use of low-power FinFET SRAM based cell for handy operated devices a faster speed, improved battery life is accomplished. A key objective of present paper is to reduce the delay, power consumption in a desired nanoscale 6T FinFET SRAM cell structure [82]

SRAM cells based FinFET are used in memories that need a shorter access time having a low tolerance to the atmospheric conditions with less power dissipation. Such SRAM cell are most popular because of its lower dissipation among various circuits and there configurations based on logic processes. Moreover it offers a high noise margin with high switching speed.[83].

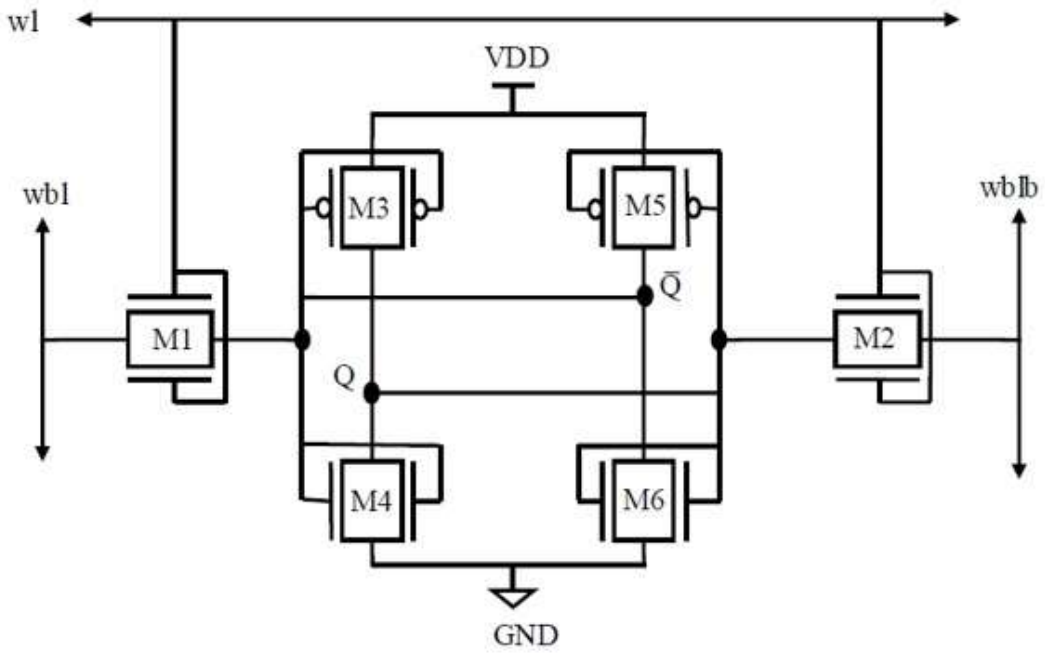

Figure 2.3: FinFET based 6T SRAM

2.4 Design Problems in Conventional SRAM

One of the key obstacles in 6T based SRAM is both a read operation and writes operation doesn't go hand in hand. Here cell that has read of lower Static Noise Margin (SNM) will leave an improved write ability and vice-versa. Hence if a decoupling is provided between a read and write operation then a designer will have flexibility for optimizing the operations read and write independently.

In previous SRAM proposed on average-8T is having a modest area such that it doesn't require a scheme of write-back. Its architecture has bit line (BL) and it is directly attached to gate terminal of read buffer and is succeeded by a boosted voltage of word line (WL). Though, in an average 8T based SRAM of 22nm based FinFET there is a large threshold voltage variation and voltage appeared at WL is not used as it will degrade the read stability. Hence, we cannot achieve the full-swing output, gate terminal of a read buffer will not able to drive Vdd which causes an increased read delay.[84]

Here in the present paper a 7T based SRAM is proposed and then designed as shown in Figure 2.3 with a single ended read and differential write operations that work near to threshold region. The proposed structure is a modification of 5T cell that uses low and high threshold voltage transistors for improving the stability to read and write. For enhancing a RSNM by maintaining a low write time and high write time, n additional transistor used known as access transistor by setting the threshold voltages of it, and for maintaining cell's low leakage power we need to increase a ratio *Ion*/*Ioff* of an access transistors and a high *VTH* will be used for pulling down a cell path. For evaluating the efficiency of proposed design, the features of a proposed design are matched with 5T, 6T, 8T, and 9T based SRAM. [85]

A SRAM cell design based on nanoscale regime is becoming challengeable increasing day by day due to its more leakage power, weak write ability and a degradation of data stability and intensified process variation parameter in every generation of a CMOS technology. A new technique termed as asymmetrically ground-gated seven-transistor (7T) based SRAM cell was planned that provides high data stability and a low leakage current and also has a sleep mode. A proposed method has an enhanced data stability of 7.03x for reading operations and 2.32x for idle status and it is compared with a 6T based SRAM designed at 65 nm based CMOS technology. Here in 7T SRAM cell for transferring data a specialized circuit for write assist is designed. [86]

Here In the paper, a new design of SRAM cell having 8T based on a Si technology that provides a low leakage power when compared to conventional design. Its design consists of fully functional design that has small supply voltages when compared with 6T based SRAM. In order to verify a design of a proposed system a 32 kb of SRAM cell is considered and simulated in 90nm based CMOS technology. During the operation of circuit at V_{dd} minimum simulation results show an improvement of 58% during write operation, 67% during read power per operation. During a write operation a half selection challenge is overcome by a low power internal write back scheme.[87]

For most of the performance oriented applications a near threshold voltage (Vth) based operation will be an effective method. For SRAM cells its get affected due to circuit stability. Hence a near threshold voltage based 9T SRAM is implemented at 22nm based FinFET technology. In this cell read stability is ensured by a read buffer by decoupling a stored node from a read bit line and thus improves the read performance by using a single transistor path of read. In read buffer with the elimination of sub threshold leakage will reduce the standby power and energy a new method of

yield estimation is proposed used for providing an accurate sensing yield estimation that also considers the dynamic trip voltage. It achieves a minimum operating voltage of 0.3V.[88]

In today's SOC the memories in it occupies larger than 70 percent of total area and it is trending to increase continuously in upcoming years. As there is a scaling in technology a bulk MOSFET faces numerous issues that lead to an increase in leakage power. FinFET is one of the most selected techniques below 32nm technology as it will have reduced short channel effect. A proposed method of 10T based SRAM cell that is designed by 16nm based technology and its performance metrics are compared with a conventional 6T based SRAM. [89]

A traditional planar metal oxide semiconductors FET's are replaced by Fin field-effect transistors (FinFETs) because of having an extreme capability to control the effect due to short channel, power dissipation, propagation delay and leakage current. Here planar based MOSFETs will have an issue of process variability whereas FinFETs will lessen the variability of device performance that is due to number of doping ions[90].It includes SRAM design by using FinFETs. While an analysis of performance of ST11T, and proposed ST13T based SRAM cell, having a power gating sleep transistor is studied by a Cadence Virtuoso Tool (V.6.1). Based on results an improved gate stability and controllability is achieved that makes an FinFET transistor structure better compared with other planar structures. Hence a proposed will reduce the power thus improves the speed of SRAM. From result it can be observed that FinFET-based ST13T based SRAM cell is 92% is having more power by using a power gating technique, i.e. with a use of an approach of sleep transistors and have 12.84% less delay because of transmission gates in given path.[91]

Here a structure configuration is not changed and it is similar as 8T SRAM cell proposed by L. Tony Tae et.al. [92] The proposed system desires to separate a read line from write line to achieve a better stability by enabling a low voltage to operate. For a 6T SRAM cell by adding two FETs will provide read to a 6T SRAM cell that provides a read and will not interfere with internal nodes, and read line and word line are separated and accommodated by separate bit lines. Whereas 7T cell consist of an extra MOSFET when compared with 6T SRAM cell thereby decreasing the leakage current even if the cell switches to standby mode. [93].

An extra MOSFET is sized identical to that of the inverter for matching their current carrying capacity. Here the design of 9T SRAM cell is introduced in [94-95]. Write access transistor will

give the access of writing the data to cell that is controlled by write bit line (wbl), Write Bit Line Bar (wblb). Whereas read access transistor will allow a read access to an SRAM cell and is controlled by a Read Word Line (rwl). A Read Bit Line (rbl) is therefore charged before a read access. Here as we can see word lines for both read and write are different. A write access unit is holded and maintained by reading SNM margin. In 8T cell a leakage issue is observed on read bit line and causes the input data to change at read operation. And a bit line here should be kept high, but because of a leakage it will drop to low level. This effect limits 8T cell for low density based applications. Whereas in 9T cell leakage at bit line is reduced by stack effect where a NMOS transistor is added in between M7 transistor and M8 transistor. In 10T based SRAMs [96] a SNM is increased and operations at subthreshold are also enabled. Under particular schemes the available data nodes are decoupled from a read access. It will ensure that read SNM is similar to hold SNM and thus improves the read stability. For write ability improvement a supply power gating and transistor accessing for long channels is used. 10T cell will reduce the leakage power wherever it is present. 11T cell that is proposed by A. Islam et. al. will achieve a low power dissipation as it is connected in series and it is drive with bit lines and the read buffers that provides a stack effect. After simulating the 11 T cell it has shown a huge improvement in leakage and power dissipation at 84% of total area.

A novel structure of 12T SRAM bit-cell having a differential cross-point Data-Aware Power-Cut off (DAPC) is studied for operating a low-voltage and having a write assist. Based on input data and a bit cell it internal reduces the supply voltage. At present a write operation is used at left cell or right cell for weakening a pull-up network of SRAM network and provides a discharging node. It employs the additional peripheral devices and improves a write-ability for assisting write circuits that boosts the timing and control circuits [97].

Moreover, a bit cell that cross point a write structure based on the data is a column based on write word line (wl) to revoke an write Half-Select (WHS) an disturbs it. Thus for enhancing a soft error immunity an architecture of bit interleaving is used which supports a bit cell. [98].

2.5 Power Reduction in SRAM Cell

In modern CMOS devices based on nanoscale should be operated on low power supply and have a reduced leakage power. In current scenario the architectures having a memory with low leakage is more challenging that is almost a 30 percent of power consumption of a total chip. Since, in SRAM during the operation data holding much of the memory processing data remains stable as density of a cell is low, and then data stored in the memory is affected by a leakage problem as the parameters are scaled down. In this study, we have discussed about an origin of a leakage current that is present in a short-channel device and different techniques of leakage reduction for an ultra-low power based SRAM design. Based on their functions and design structures a classification is made like a multi threshold, power gating and biasing technique. Based on data collected a summarization of merits and demerits and various challenges of different techniques is been given. [99]

Most of the area on IC chip is occupied by a memory block and improving the performance of a memory cell enhances the performance of an overall system. SRAM on-chip integration will increase the levels of it by degrading the stability of a cell. Here author has used a low-power multimodal switch (LPMS) with a power gate structure and designed for minimizing the leakage power thereby improving the stability of data. It provides a maximum leakage power reduction of 91% and a dynamic power reduction of 23.5% when compared with conventional CMOS methods. Whereas a read margin is 4.7 and a write margin is 7.5%. This method provides a better stability and leakage reduction under operation of various parameter variations. [100]

A 7T SRAM is described in this paper that has a large impact of gate on it and in order to reduce a leakage produced by sub threshold and gate leakage currents three different methods are used. In first method we will decrease the supply voltage. Whereas in second method ground node voltage is increased. When moving to third method an effective voltage Vd = 0.348V, Vs = 0.234V is observed for an SRAM cell. In all the three methods of SRAM cell its effective voltage is decreased when it is in standby mode by using a dynamic self-controllable voltage level (SVL) switch. The circuit simulation is carried out at 45 nm technology by sing cadence tool and it is detected that the source voltage is reduced by reducing the gate leakage and a ground node voltage is increased. Based on the obtained result the leakage current reductions of 437 FA is achieved in 7T SRAM cell. [101]

A bulk CMOS based technology during the scaling will lead to an increase in leakage current and will also have a short channel effect. SRAM cell occupies a 90% of SoC area. In SRAM the major concerned factor is a leakage current and thus it is implemented by a FinFET. Additionally, a DG-FinFET device is a better choice of design for deep submicron based technology. By considering it a 6T based SRAM implemented by independent gate DG-FinFET having both gate sides to be independently controlled and provides scalability to a designed cell. Hence an implementation of design is done by various leakage reduction methods like multi threshold, gated-Vdd. Therefore in SRAM power consumption is thus reduced by providing a better performance. IG- FinFET based SRAM cell designed using different leakage reduction methods is simulated at 45nm CMOS technology by cadence virtuoso tool. [102]

A 9T based SRAM that is based on sub threshold is designed at 14 nm based FinFET technology and simulated by cadence tool. Based on the observations it is concluded that it offers an improvement in access time while compared with an 8T SRAM based cell. Additionally, for reducing a leakage current of the design an extra circuit called assist is used which decreases it to 20% while '0' is hold, and equal leakage current while '1' is hold when compared with SRAM 8 T cell. The proposed design has improved the access time with 40 percent compared to 8T SRAM cell by not having any degradation in noise margins of both read and write. [103]

2.6 Process Variation

In VLSI chips its reliability is greatly affected by an electro migration (EM). By this effect it will not only affect the power line and ground line but also SRAM bit lines are damaged. Here in this paper we describe the reliability of an EM for a SRAM array that is affected dramatically by a process variation due to an increase of subthreshold leakage current on bit lines. Hence the process variation affects are modeled statistically and various methods are used for the EM failure prevention and we modify the width of bit lines and P/G lines. While considering an effect of modification of a bit line on stability of a cell and its performance. A tradeoff is been given among the functionality of circuit and EM failures that maximize an yield of SRAM and also indicates an bit line on array.[104]

In today's world a SRAM that is having a low power and have a noise tolerant is in much demand. It presents a method that uses a differential circuit and consumes a less power. The design is similar to a 6T based SRAM cell having dual buffer transistors in addition having one tail transistor and other is complementary of word line. Due to effect of stacking, a proposed SRAM will achieve low dissipation of power. Here process variations based on different design parameter metrics are represented and

compared by a conventional differential 6T (D6T), transmission gate-based 8T (TG8T), and single ended 8T (SE8T) SRAM cells. Process variation effect based on threshold voltage and channel length for various SRAM design is shown with different metrics of a cell like write access time (T_{WA}), read access time (T_{RA}), and read static noise margin (RSNM) is presented below. [105]

Here author has proposed an assist circuits for variation tolerant against different process and used temperature. Here author has introduced a passive resistance to read assist circuit by a memory that is exact replica to a voltage of lower word line.in order not to enlarge the write margin and for reduction in speed overhead and power consumption a scheme based on divided dynamic power-line is adopted on charge sharing. Whereas 512-Kb SRAM test chips having macros with a memory cell that is isolated is fabricated on 45nm bulk CMOS based technology [106]. Two types of 6-T based SRAM cells, having the size of a 0.245 mum ^{2} and 0.327 mum ^{2} is designed and then evaluated. Based on results obtained a static noise margin was improved with a factor of 100-mV and white margin of 35 mV for both SRAM cells at supply voltage of 1.0-V i.e. a worst condition with assist circuitry. Moreover the circuit enables a level of word line for keeping the voltage high at slow condition of typical process. It results in improvement of 83% of a cell current when compared with a conventional assist circuit. [107]

Since past decades CMOS technology is scaling severe based on the challenges of variability and reliability. Whereas bias temperature instability (BTI) is one of the key challenge in reliability. Here it analyzes an impact of BTI on delay sensing for a standard latch type base sense amplifier (SA), that is one of the serious component to provide a high performance in memories; hence the analysis here is done process incorporation, voltage, and temperature variations (for investigating the impact of severity) by considering the four nodes of technology (i.e., 45, 32, 22, and 16 nm) at various workloads. At last results shows an importance of considering the SA degradation for memory design i.e. robust, and it depend on the technology node that is been used and the application, here SA delay will increase with 184.58% at worst case at 16 nm. [108]

A major source of variation is observed due to various parameters in considered. Here each parameter affects the other parameters of transistor in different ways. In lithography an etching, polishing steps impact physical dimensions of transistors with an effective lengths and widths. Similarly variations observed in an oxidation process will affect the thickness of a gate oxide of transistor. In ion implantation process it has a random dopant fluctuation and will affect the

threshold voltage of a transistor. Some other process that causes the variation in metallization, polysilicon and deposition of nitride will cause the variation of a film thickness by differing in degrees during the transistor fabrication. [109].

In earlier technologies the process variation effect was small having the feature sizes (> 90nm). For allowing the safety margin and a critical path delay at worst condition the designers has set a clock frequency that is set to a microprocessor. This process is termed as guard band [110]. By using such guard band techniques with some margins at feature size we can overcome the process variation affects. Moreover these approaches will not take care of various approaches that are used for process variations for scaling don of device size. Thus, designers need to face lot of complexities and should meet all targets to achieve the performance. A sub-90nm technology is a sudden upsurge for addressing and modeling the various impacts. Bowman et al. [111] has conducted few analyses in process variation field and has a substantial performance that is lost due to variation of process. Thus a statistical model was developed in order to overcome the problem been faced by process variation and there correlation with parameters based on micro architecture such as logic depth and total number of critical paths that are independent. Later models were been verified against microprocessor chip and were fabricated on 0.25µm process and 0.13µm process technology and an error of 3 % was achieved. Later to quantify an impact at low power circuits a variation of intra die local parameters was done. Later investigations were carried out on various supply voltages, path delays and size of transistor and path lengths and based on the data the conclusion was made to reduce the logic depth that will in turn increase the relative path delay.
S. Borkar et al. has a long debate on process variation and its influence on various micro architecture based circuits. Based on the debate they pointed that temperature, voltage and process variation will cause the chip frequency to vary. As a result there is a low performing circuits and has not fulfill the basic requirements and that to be eliminated based on the result of few IC's. Osman S. Unsal et al. has represented an influence of various micro-architecture and circuits. Based on some sources process variations a circuit level technique can be mitigate to various process variations. According to authors, a gate delay variations is due to variability of parameter and on account having a large percentage delay margins that are minimum (hold time) and maximum delay margins is termed as (setup time). In CMOS circuits a die-to-die fluctuations are considered to be the key source of concern. Hence it classify a process variations based on several characteristics like a source of variations, manifestation, design parameter granularity and device

aging. Sherief Reda and Sani R.Nassif [112] proposed a statistical structure for modelling an effect of process variations on semiconductor circuits with the use of test structures that are process sensitive. Based on this an algorithm is suggested that produces an accurate or precise statistical parameters that is based on multivariate statistical methods. Authors have also proposed a method for analyzing the sources randomly and systematically for various process variations. [113]

CHAPTER 3
DESIGN AND ANALYSIS OF CMOS SRAM CELL

Usage of SRAM based cache memories has increased over years for portable devices, mobile phones and all kinds of multimedia devices to attain higher speeds. Lower power and higher speed performance is the major puzzling task for Integrated circuit design in Nano scale technologies as VLSI chips are in demand in mobile communications and computing devices. Since there is a wide spread use of battery powered smart devices, Nano medical devices, low power process has turned out to be a serious problem with system on chip design (SOC).In order to examine a SOC, low power based SRAM is considered because a large area on SOC is occupied by it, it really disturbs an over-all power of SOC.

Depending on how frequently we access the SRAM cell, the power consumption varies largely. If we use a SRAM cell at high frequencies it consumes much power but at the same time if we use at low speed applications that use microprocessors having a clock in it consumes almost negligible power. There are many techniques for managing power in SRAM based memory structures. The adverse consequence of threshold voltage (Vth) variations becomes substantial at lower operating voltages as SRAM cell remains vastly susceptible to the differences in Vth. In 6T based SRAM operated at different procedures of low power requires lot of adjustment between READ and WRITE operations to obtain required stability.

3.1 Conventional 6T SRAM cell

A SRAM based cell includes latch consisting dual inverters that are joined cross coupled, such that for retaining the stored data we need not refresh it periodically. Based on the condition that for a given SRAM cell an ample of power supply voltage is present. [114].

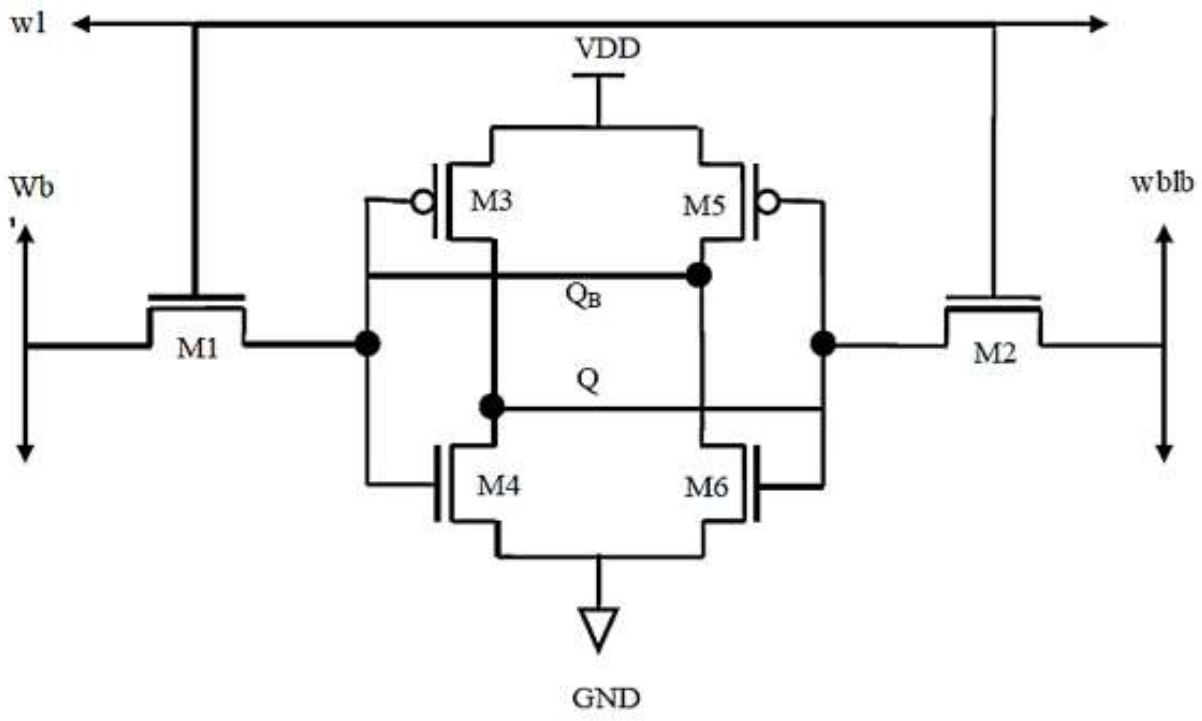

Figure 3.1: CMOS based 6T SRAM

A conventional 6T based SRAM contains 2 inverters that are cross coupled and has dual access transistors as demonstrated in Figure 3.1. Here inverters connected in cross-coupled fashion are called as latch. There are four transistors present in 2 inverters that are cross-coupled namely (M3, M4, M5, and M6). These four transistors store each bit in an SRAM. Here M1 and M2 access transistor's to latch input, whereas bit line (wbl) is connected to M1 and bit line bar (wblb) is connected to M2 at source terminals[115]. When (wl = 1) i.e. word line is high, the access transistor will turn ON, where bit lines is used for data transferring for read, write operations that is attached to a latch .When (wl = 0) i.e. word line is low, the access transistor will move into OFF state, and disconnects the bit line from latch. During the particular state a bit is hold by latch until the voltage remains at V_{dd} and GND.

3.2 SRAM Operations

a. Write Operation

To perform both operations, activation of M1 and M2 access transistor is must. In order to activate both the access transistor word line must be pulled high i.e. (w1=1) and then a write operation can be performed. A data that is to be written is applied to (wbl) bit line, whereas its complemented

version of it is given to (wblb) bit line bar. So for writing '1' a value '1' is set to bit line and value '0' is set to bit line bar. Hence it will automatically change a cell accordingly. If we change state of latch then it will deactivate the word line and data is written on cell [116].

b. Read Operation

Similarly in SRAM for reading the data a higher value is applied on word line that activates an access transistors i.e. M1, M2 for accessing the latch. For read process both the bit lines should be pre-charged to value '1'. Based on latch state one bit line will be pre-charged and another will be discharged to GND i.e. if a bit line is pre-charged then bit line bar must be cleared through ground and vice-versa. [117].

c. Hold Operation

The M1 and M2 access transistors bit lines will get disconnect from a SRAM cell, if a word line is not asserted to low (wl = 0). As long as inverters i.e. cross coupled is attached to Vdd supply voltage the dual latch transistors M3 and M4 can reinforce each other. A current which drifts from Vdd during this state is known as leakage current. [117].

3.3 Performance Parameters

3.3.1 Static Noise Margin

Static noise margin (SNM) in SRAM is Figure of Merit (FOM). Here SNM of CMOS inverter is extracted by nesting a possible square in two voltage curves observed. Whereas SNM is length of a side in square and represented in volts.

In order to measure SNM a method called butterfly curve is used, SNM of SRAM depends on supply voltage, pull-up ratio and the ratio of cell. A good SNM value is required for SRAM stability and it usually depends on supply voltage used, pull up ratio and cell ratio value. During the operation read the ratio among the transistor sizes of driver and load is calculated and it is known as cell ratio. Whereas a pull-up ratio is ratio among the size of load and access transistor for write operation [118].

$$CR = \frac{W/L\ MN3}{W/L\ MN2} \qquad \text{During Read Operation----------3.1}$$

$$CR = \frac{W/LMN4}{W/LMN1}$$ During Write Operation----------3.2

In SRAM we can achieve various speeds by changing a cell ratio. If there is an increase in cell ratio then driver transistor size will increase and it increases the current and in turn it will increase the SRAM speed. By changing a cell ratio we can achieve its corresponding SNM. Hence for different CR values we will have different SNM values in various SRAM technologies. Figure3.2 shows the VTC of an inverter with one cell versus the inverse of another cell. In the figure the resultant graph is termed as "butterfly" curve it is two lobed used for determining a SNM, and its value is length of side of largest square that fits inside the two lobes of curve [118].

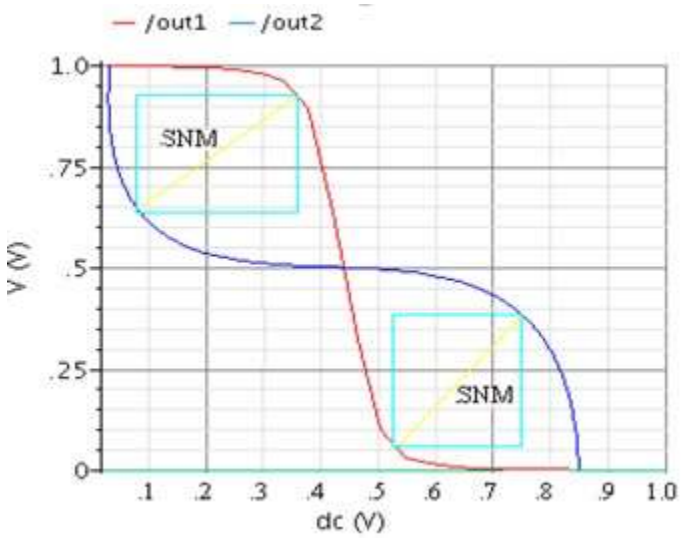

Figure 3.2: Butterfly Curve

3.3.2 Power Consumption

Larger embedded based SRAM arrays occupy the major segment of application processor and its power. In SRAM array the power consumption contains small active periods and elongated idle periods. In large SRAM arrays major concern is power consumption in standby mode. Thus, in large SRAM memory arrays leakage reduction is a big task for low power circuits. We will represent the cell leakage by longer length of channel or by using a high threshold voltage. When we use long length for a channel it will negatively impact the area of cell and it also amplify the capacitance of wl and wbl and increases the power and access time. Hence long length channels are rarely used [119]. During write process to estimate the power consumption we will estimate the voltage and current across the ON transistor [120]. Because of high threshold voltage of

transistor it will affect the access time and also lowers the read current. However, this increases the write and read margins. In pull down device i.e. a NMOS will have a high threshold and will tend to surge the trip point of inverter and in pull up transistor i.e. PMOS the loads get decreased. As we know that pull-down device's current driving capability is greater than PMOS load and grows the NMOS transistor threshold voltage for having a stronger impact and ensures of having a large read margin and write margin. [121]

3.3.3 Cell Area

The two most significant properties of memory array is its functionality and a density. Memory in memory arrays that are large will have functionality that will provide a design margins that are large, and it is decided by supply voltage, sizing of device (channel widths & lengths) and slightly, by threshold voltages selection. Even though upsizing a transistors increases a noise margin, by increasing a cell area thus lowering the density [122].

3.3.4 SRAM Delay

In SRAM, the transmission delay is reliant on column height and the delay in wires. Thus, for reducing a delay segmentation is used. As for device we have a constant power-delay product, which increase or decrease the other device and vice-versa. In SRAM an upsizing of CMOS device will lower the delay and increases the dissipation of power. For decreasing the leakage current and power dissipation we have to minimize the current that intends increases the length of channel and provides a high delay such that there is trade-off among them [123].

3.4 Different Types of Leakage Currents in SRAM

In CMOS technology having a deep submicron will have leakage current which is a serious problem. In semiconductors the quantum occurrence will cause a leakage due to the charge carrier's mobility through a tunnel in insulating region. As insulating region thickness decreases it cause to increase the leakage exponentially. When a semiconductor is heavily doped between P-type and N-type regions it will cause a leakage at junction tunneling. Here in MOS transistor there will be leak of carriers in between source and drain terminals, irrespective of tunneling it happens via gate junction or insulator. A leakage occurs in transistor but leak of electrons can be in interconnects thereby increase the consumption of power and if leakage is large then it will damage the whole circuit.

Three main components that give rise to leakage current are junction tunneling gate leakage and sub-threshold leakage and it is discussed below.

i. Sub-Threshold Leakage Current

In CMOS transistors, a key component of the static leakage is a current produced at sub-threshold. A front-gate leakage is almost self-regulating of the back-gate in DG-MOSFET transistors. With a large leakage at sub-threshold is the transistor current observed at drain to source terminal and here the voltage at gate source terminal is less than threshold voltage i.e. $V_{gs} < V_{th.}$

ii. **Gate Leakage**

In oxide layer its field is increased by oxide scaling. A lower oxide thickness with a higher electric field will cause a leakage current at gate tunneling i.e. from gate terminal to channel and from source/drain overlap region to gate terminal. Thus a gate leakage current will always be at three components of a cell like gate to channel current, Gate to source/drain overlap current and from gate to substrate current. While transistor remains in OFF state it causes gate to source/drain overlap current and when transistor remains in ON state it causes a gate to channel leakage current. Leakage at Vgs < Vg and current at gate to source/drain is leakage current at gate and it will be in OFF state and it is small compared to leakage current at gate in ON state [124].

iii. Junction Tunnelling Leakage

Normally, during PN junction reverse biased condition a leakage at junction tunneling occurs that has two constituents. First is to generate an electron hole pair at depletion region. Another is minority charge carriers diffusion at an edge of depletion region. At reverse bias and doping at junction we have an exponential function [125]. There will not be any extra leakage by junction leakage.

3.5 Performance Analysis of 45nm CMOS Based SRAM cell

The design is simulated for performance assessment of designed 6T based SRAM, using the Cadence Virtuoso tool at 45nm technology to compute and observe the results of diverse parameters such as total leakage current, power dissipation, SNM, sub-threshold leakage current, etc. The total leakage current is observed to be having a high value under normal operating condition and needs to be minimized.

3.5.1 Power Dissipation and Leakage Current

In SRAM cell leakage current is defined as current that is flowing in a circuit in the idle mode [126]. Ignorance of the leakage current leads to flipping of the data stored in it [127]. Hence, in order to observe the dissipation of power and leakage current of SRAM cell, word line is asserted with zero signal (wl=0). This disconnects the bit line (wbl) at M1 transistor and bit line bar (wblb) at M2 transistor from an inverter that is cross coupled to form a latch (M3 – M6). A latch carries on strengthen as long as it is associated to the supply voltage (VDD). The current flowing at VDD is termed as Leakage Current. Total power dissipation and leakage current in 6T CMOS based SRAM comes out to be 15.4µW and Leakage Current is 61nA respectively as shown in Figure 3.3 and 3.4.

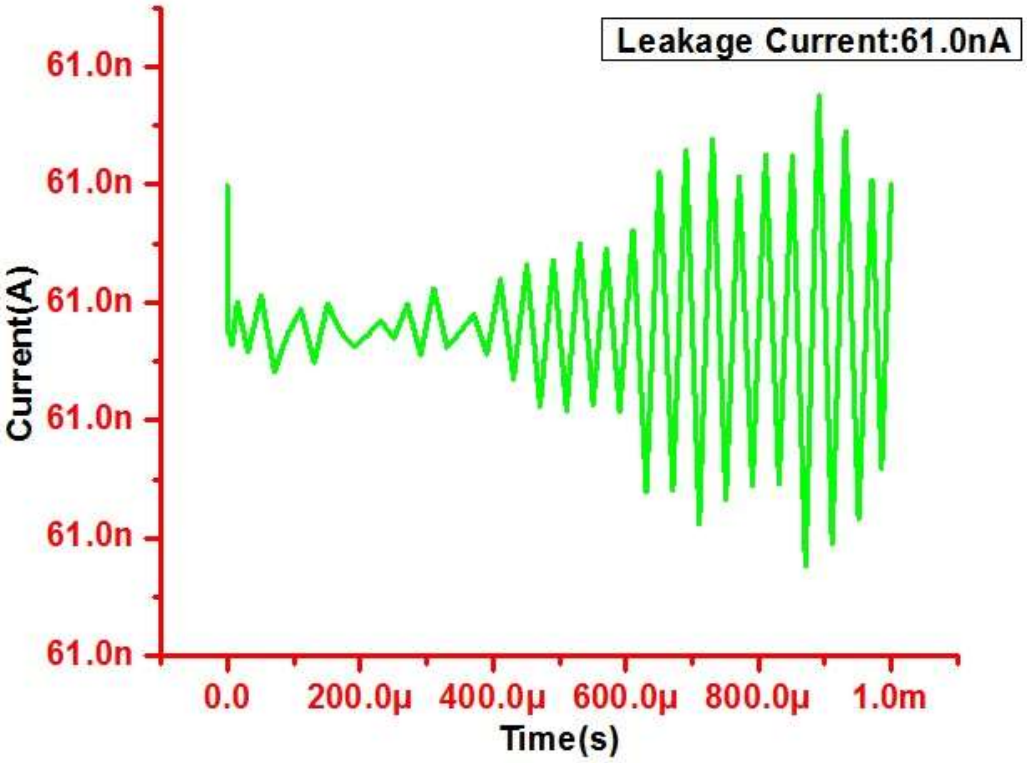

Figure 3.3: Leakage Current in CMOS based 6T SRAM

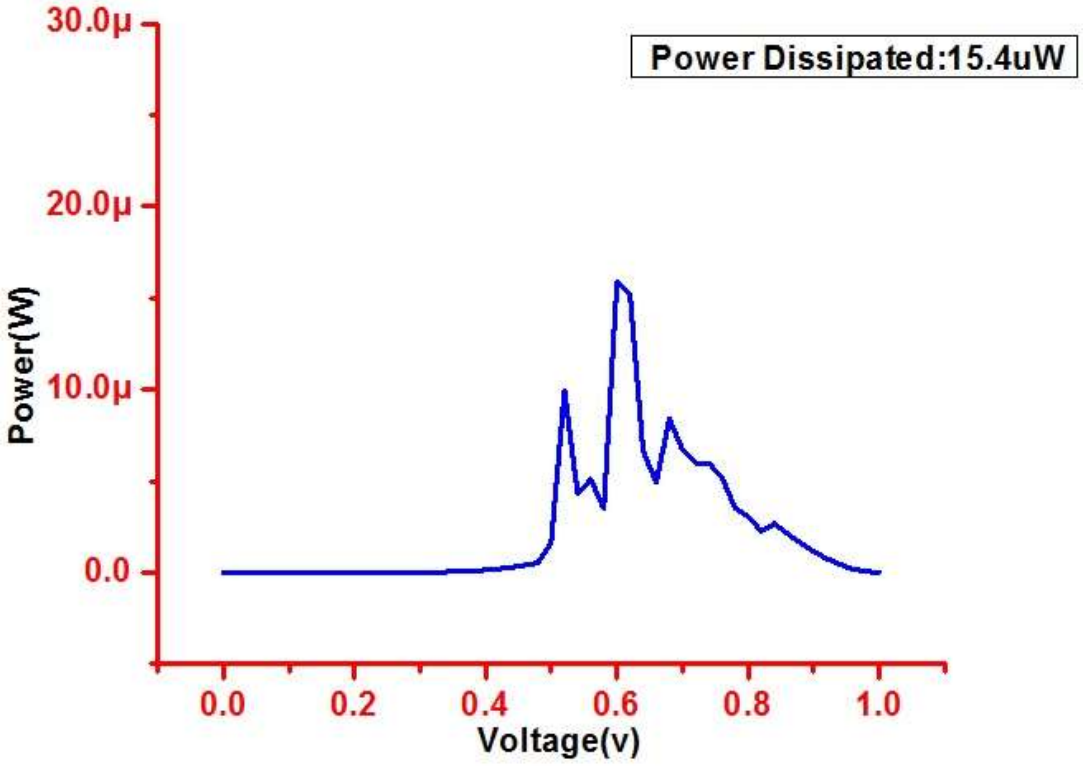

Figure 3.4: Power Dissipated in CMOS based 6T SRAM

3.5.2 Calculation of Static Noise Margin

In SRAM a Static Noise Margin (SNM) is minimum DC voltage noise used for varying the state of cell and also calculates the SRAM cell stability [128].Fig 3.2 explains test setup for SNM measuring. Fig 3.5 shows ―butterfly curve of FinFET based on SRAM having 6 transistors. This curve is attained using test circuit as given below:

1) Word- line (wl) is attached to the ground and bit lines (wbl and wblb) are attached to the VDD.
2) V1 voltage is removed from 0V to VDD during the measurement of Q voltage.
3) V2 voltage is removed from 0V to VDD during the measurement of $\overline{Q}$ voltage.
4) In order to achieve a butterfly curve we have plotted a measuring voltage. Length of sides will give the maximum square and it is enclosed in smaller loops of butterfly curve and it is cell SNM [129].

SNM of CMOS based SRAM 6T cell is 271 mV at 45nm technology as seen in Figure 3.5.
The Static Noise Margin is calculated by using this formula

$$\left.\begin{aligned} NM_H &= V_{OH} - V_{IH} \\ NM_L &= V_{IL} - V_{OL} \\ SNM &= \sqrt{(NM_H)^2 + (NM_L)^2} \end{aligned}\right\} \quad \text{----------3.3}$$

Where NM_L= Low Noise Margin and NM_H = High Noise Margin. The SNM expression for a 6T based SRAM is given below:

$$SNM_{6T} = V_{th} - \left(\frac{1}{K+1}\right) \times \left(\frac{VDD - \frac{2r+1}{r+1}V_{th}}{1+\left(\frac{r}{K(r+1)}\right)} - \frac{VDD - 2V_{th}}{1+K\frac{r}{q}+\sqrt{\frac{r}{q}\left(1+2K+\frac{r}{q}K^2\right)}} \right) \quad \text{----------3.4}$$

A voltage gain at each inverter is given as r, where $r = \beta_{driver}\,\beta_{access}$ = loop gain, V_{th}=threshold voltage, $q = \beta_p\,\beta_a$ = charge of electron (1.6×10^{-19}) and VDD=supply voltage, K is the Boltzmann constant.

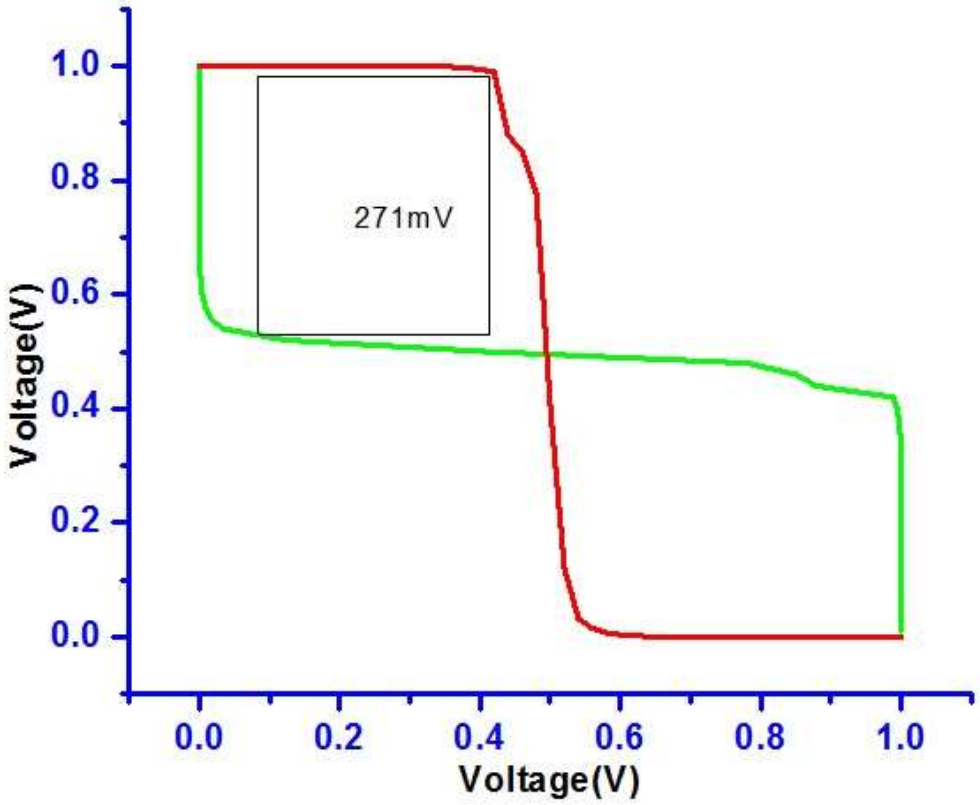

Figure 3.5: CMOS 6T SRAM SNM

3.5.3 Sub-Threshold Leakage Current

A sub-threshold leakage current is observed at drain to source terminal while the transistor is in OFF mode. It occurs when threshold voltage is greater than the voltage that is applied at gate to source terminal at weak-inversion mode. This is because of the minority carriers that cause diffusion current of a MOS device operated in sub threshold [130]. This current can be calculated using the given equation.

$$I_{ds} = K\left[1 - e^{\frac{-V_{ds}}{V_{th}}}\right] e^{\frac{V_{gs}-V_{th}+\eta V_{ds}}{\eta V_{th}}} \qquad \text{----------3.5}$$

Here ŋ denotes the DIBL coefficient and equation clearly shows that when threshold voltage is decreased it exponentially increases the leakage current. Similarly, leakage current also increases on reducing the size of the transistor. Leakage current produced due to sub-threshold in CMOS 6T based SRAM is 2.63pA for PMOS transistor and 10.57 pA for NMOS transistor as shown in Figure 3.6 and Figure 3.7.

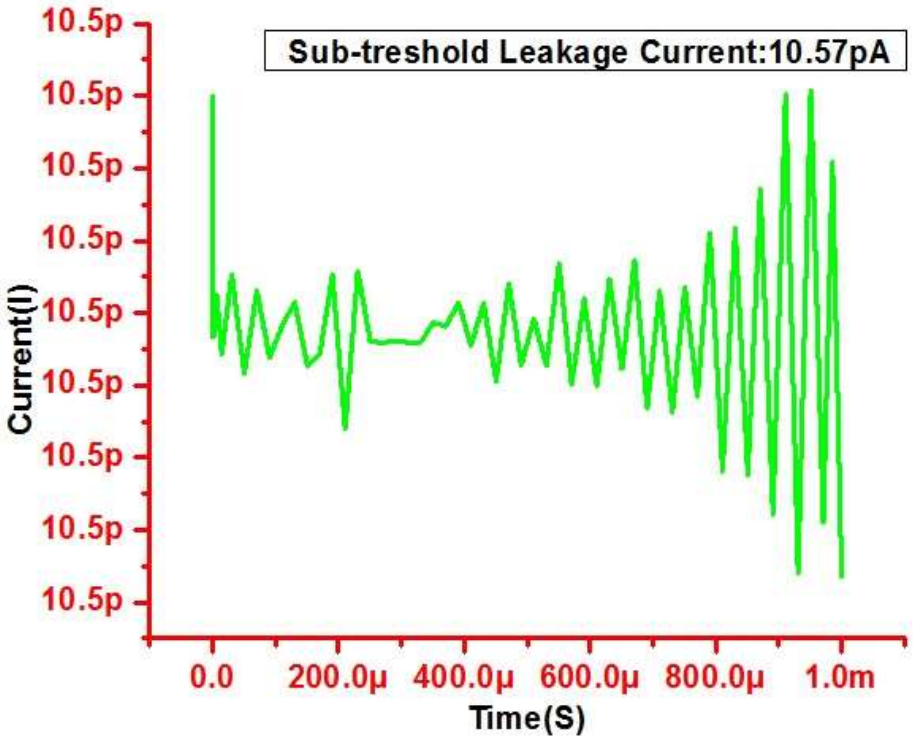

Figure 3.6: Subthreshold Leakage in NMOS

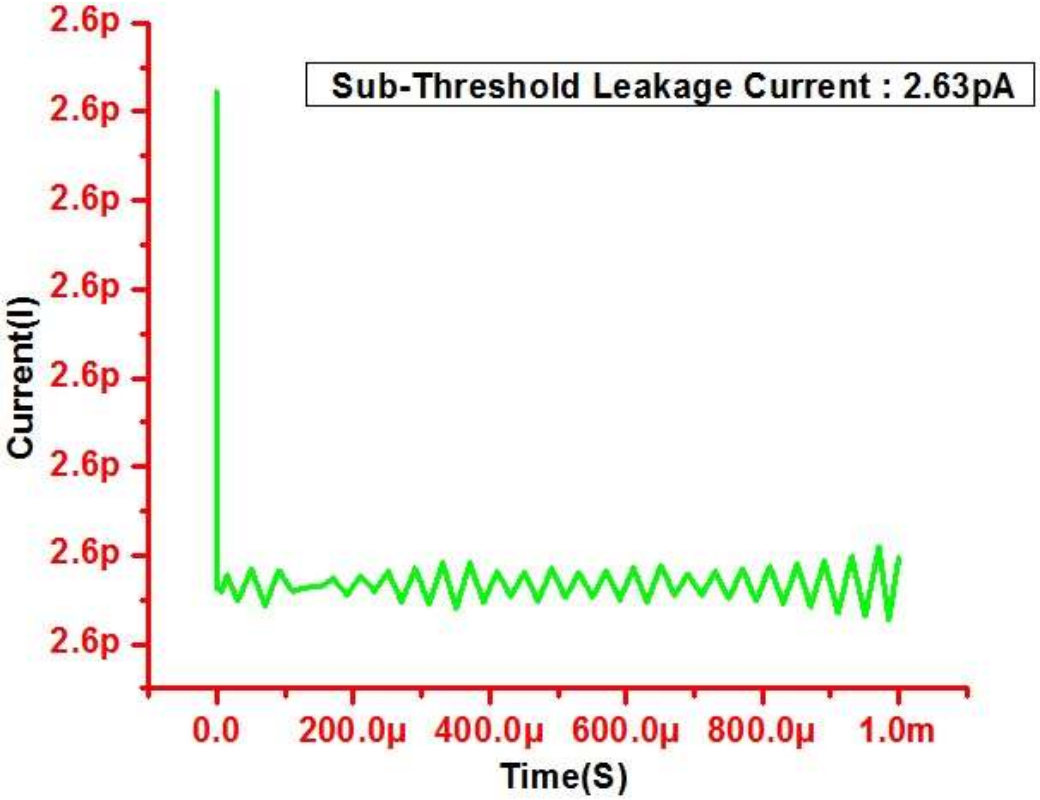

Figure 3.7: Subthreshold Leakage in PMOS

3.6 SRAM Cell with Different Transistor Topologies

As conventional 6T SRAM has certain limitations in terms of power consumption and stability it is required consider other topologies for better performed SRAM cells.

3.6.1 7T SRAM Cell

A 7T SRAM cell has read signal and write signal lines and has one additional NMOS transistor for achieving read operation without any disturbance. Here a cell area is increased by 13%. In NMOS a WL signal will control the gate and it is present in between the voltage node V2 and transistor NMOS to 7T SRAM design as shown in Figure3.8. Here a cell is accessed by turning OFF the transistor by setting WL to '0'. And when '0' is read the voltage at node 2 will not be able to pull-down to GND by preserving the data to store. While data retention a value '1' is set by WL and SRAM cell operated same as 6T SRAM cell [131]

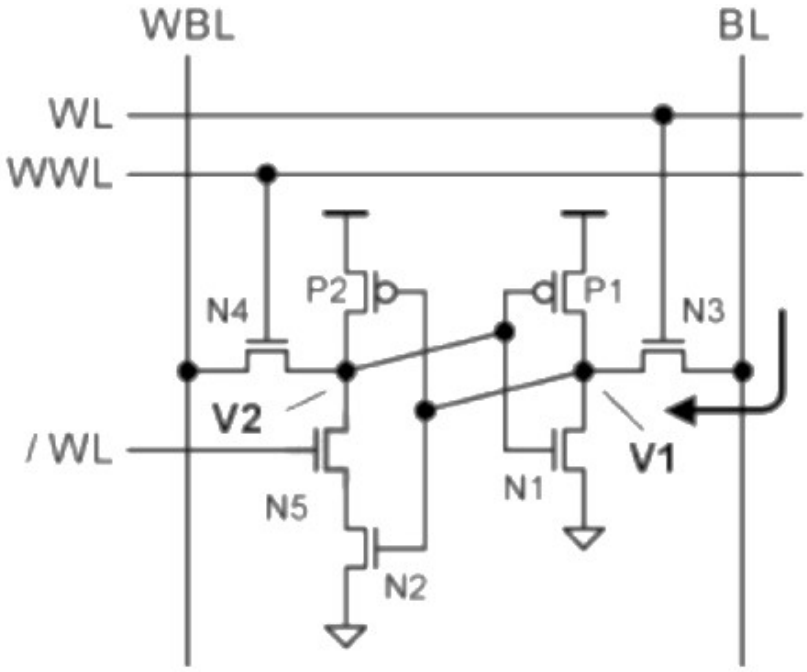

Figure 3.8: CMOS based 7T SRAM

Total power that dissipated, leakage current in CMOS based 7T SRAM cell comes out to be 12.8µW and 59.7nA respectively.

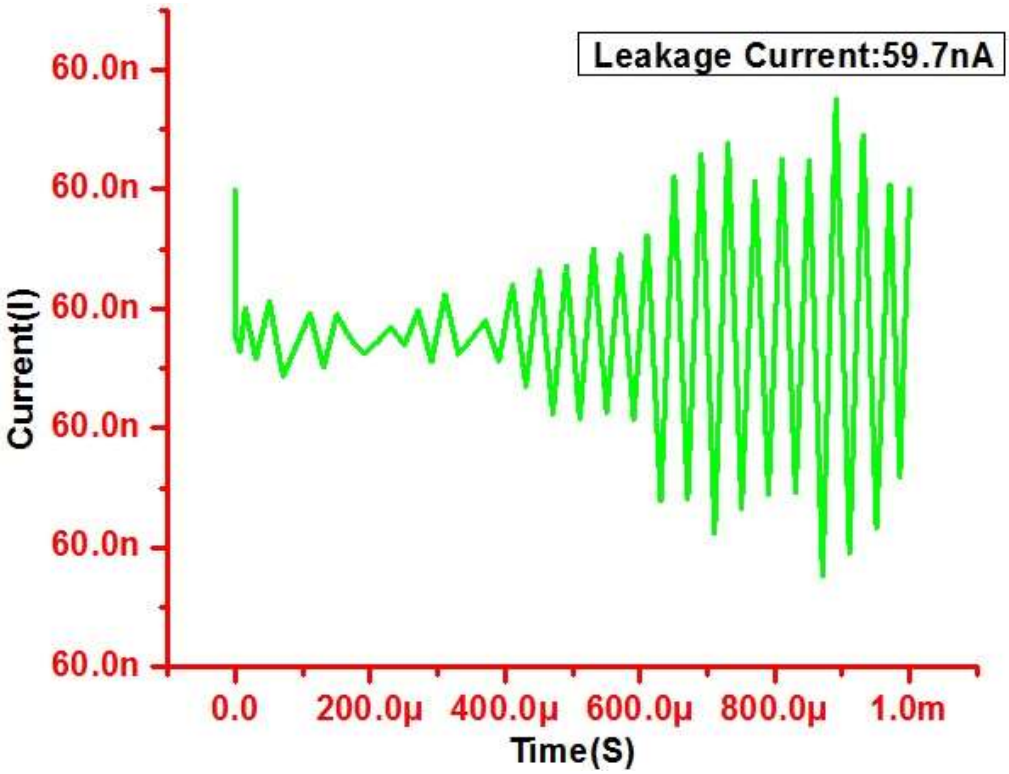

Figure 3.9: Leakage Current of CMOS 7TSRAM

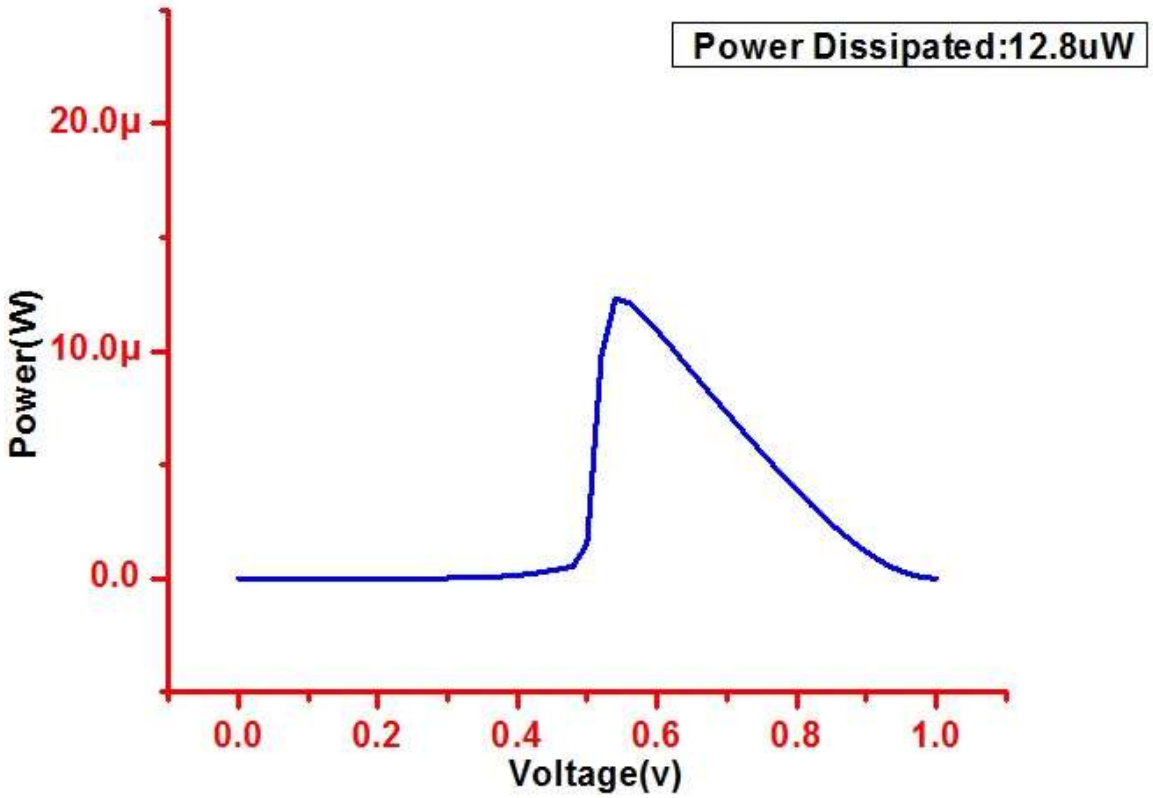

Figure 3.10: Power Dissipated of CMOS 7TSRAM

SNM of CMOS based 7T SRAM cell is 290mV at 45nm technology as seen in Figure 3.11.

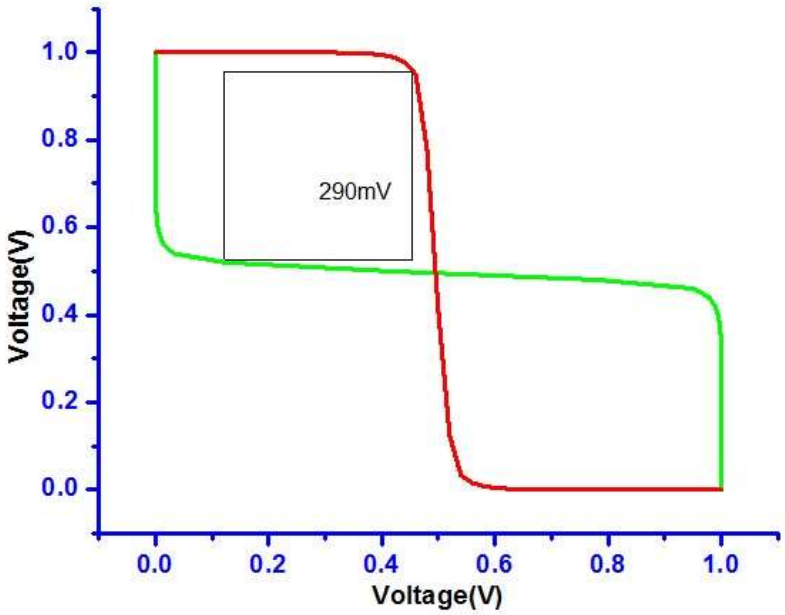

Figure 3.11: SNM of CMOS 7T SRAM

3.6.2 8T SRAM cell

To achieve better stability, 8T SRAM cell is proposed for isolating read operation from write operation at low power. Figure 3 exhibits an 8T SRAM where two extra FET are added to 6T SRAM for providing reading of data that will not disturb the internal cell nodes. It requires two lines separately read word i.e. RWL and write word i.e. WWL lines and it will accommodate two way operation with separate lines for both the operation's as shown in Figure 3.12. A read operation is activated by RWL and by pre-charging. At Q node if '1' value is stored it turns transistor M6 to become ON and creates a path of low resistance towards the GND through which current flows by RBL and it is sensed by sense amplifier. [132].

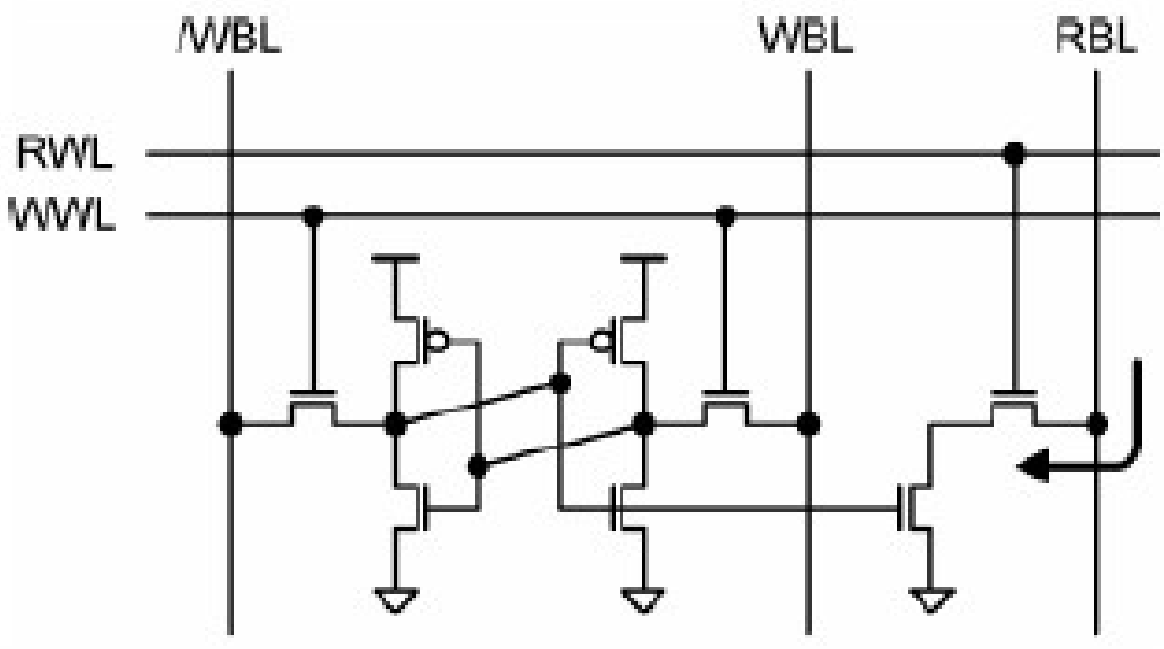

Figure 3.12: CMOS based 8T SRAM cell

Total power that got dissipated, leakage current of 8T based SRAM cell comes out to be 22.3 µW and 62.9nA respectively as shown in Figure 3.13, 3.14

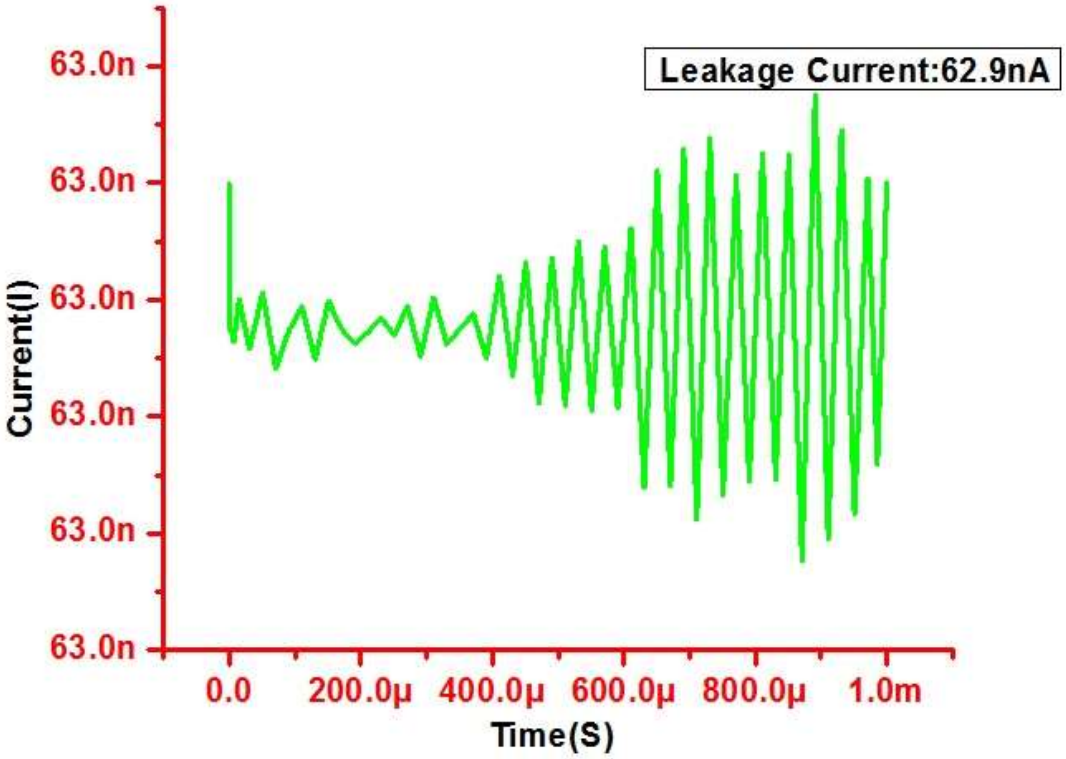

Figure 3.13:Leakage current of CMOS 8T SRAM

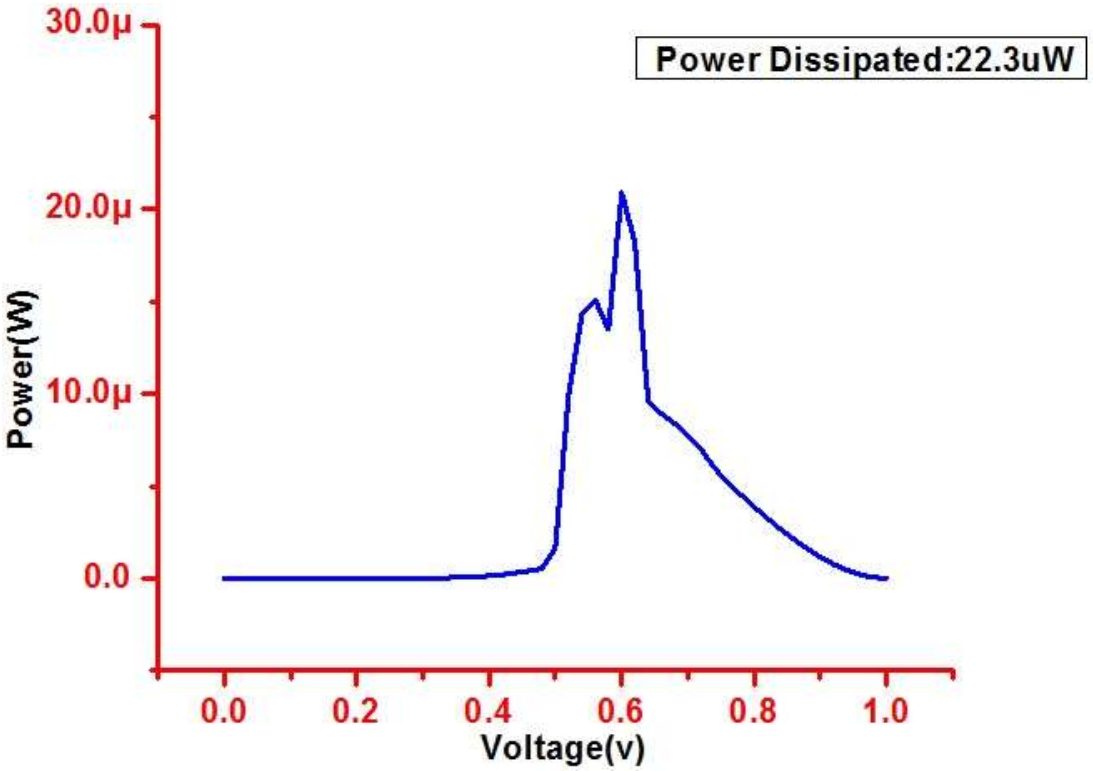

Figure 3.14:Power Dissipated of CMOS 8T SRAM

SNM of CMOS based 8T SRAM is 310 mV at 45nm technology as seen in Figure 3.15.

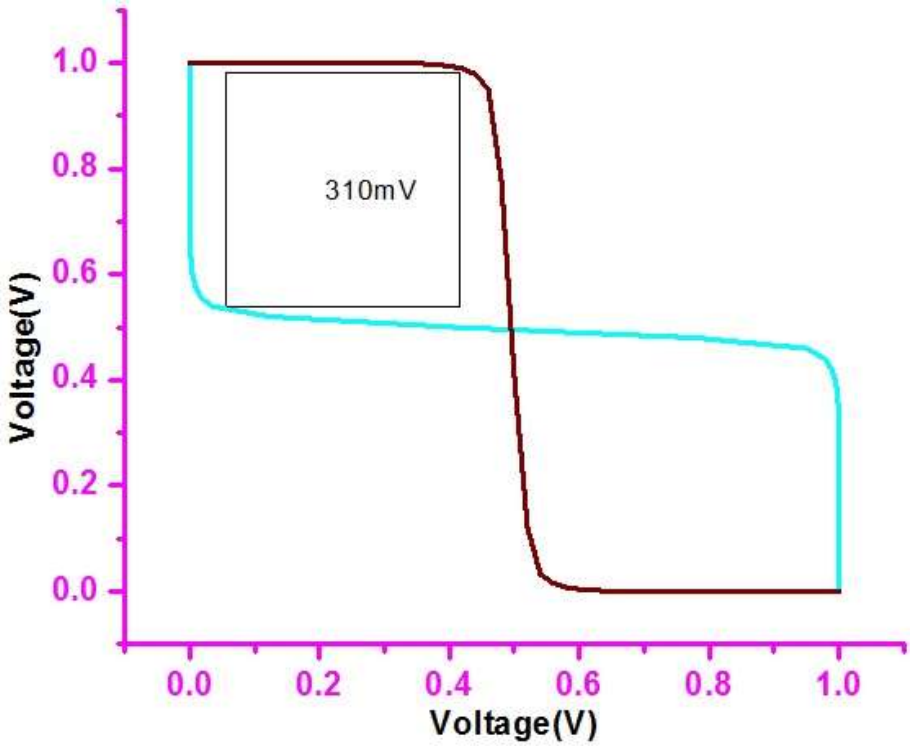

Figure 3.15: SNM of CMOS 8T SRAM

3.6.3 9T SRAM Cell

A SRAM cell having 9 Transistors is used for reducing the consumption of power of SRAM cell and has leakage in bit line. A design of 9T based SRAM is shown below in Figure3.16. Its structure is similar to 8T based SRAM and has transistor from M1 to transistor M6. Here SNM margin of read is retained by access circuit that involves write operation by adding a M9 transistor i.e. NMOS present in between of M7, M8 transistor. As we can see in the below figure the transistors M7, M8 and M9 having a leakage current is reduced by method stack effect, while M7 and M9 remains in OFF state.[133]

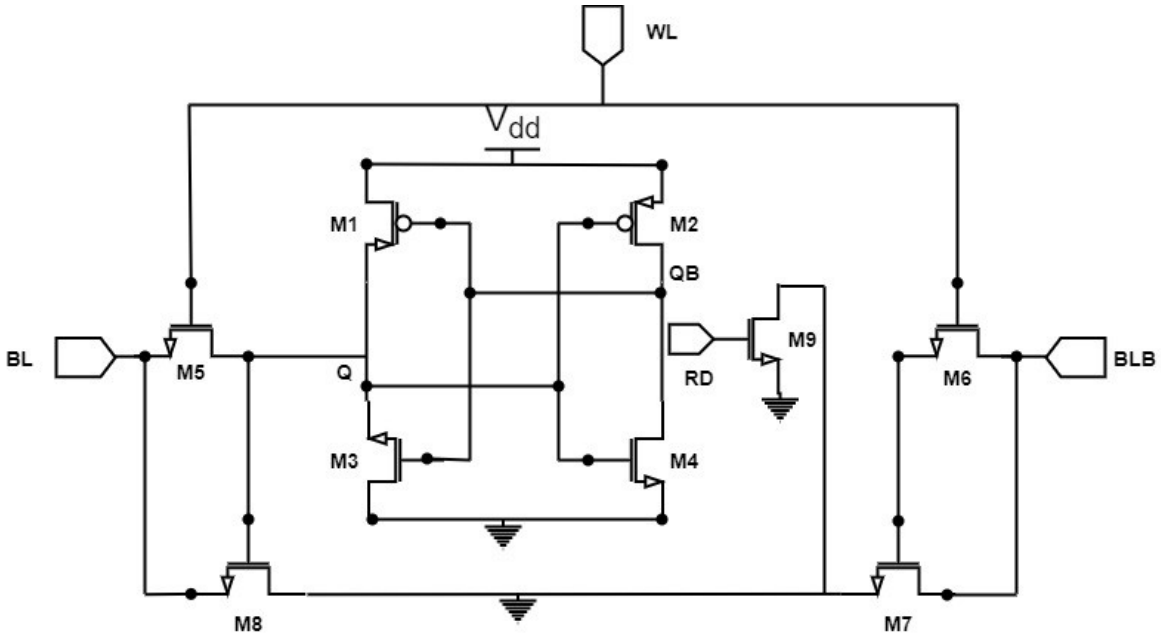

Figure 3.16: CMOS based 9T SRAM

Total power that got dissipated, leakage current in CMOS based SRAM 9T cell comes out to be 34.6µW and 64.9nA as shown in Figure 3.17 and 3.18 respectively.

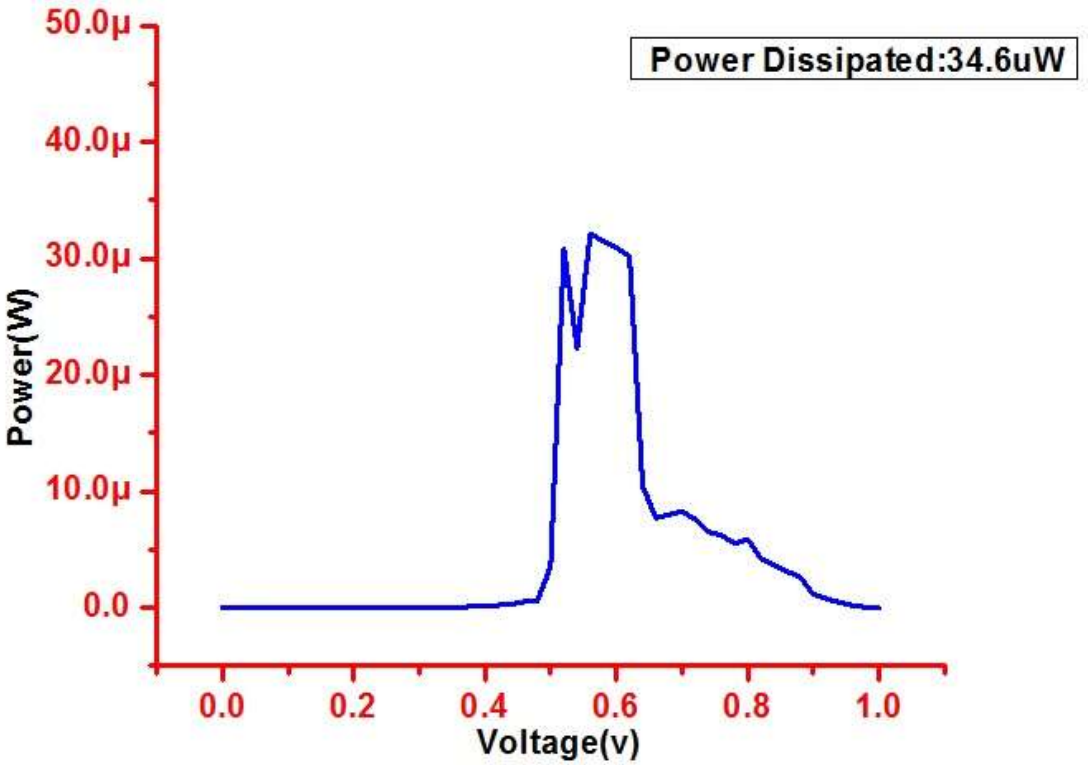

Figure 3.17: Power Dissipated in 9T SRAM

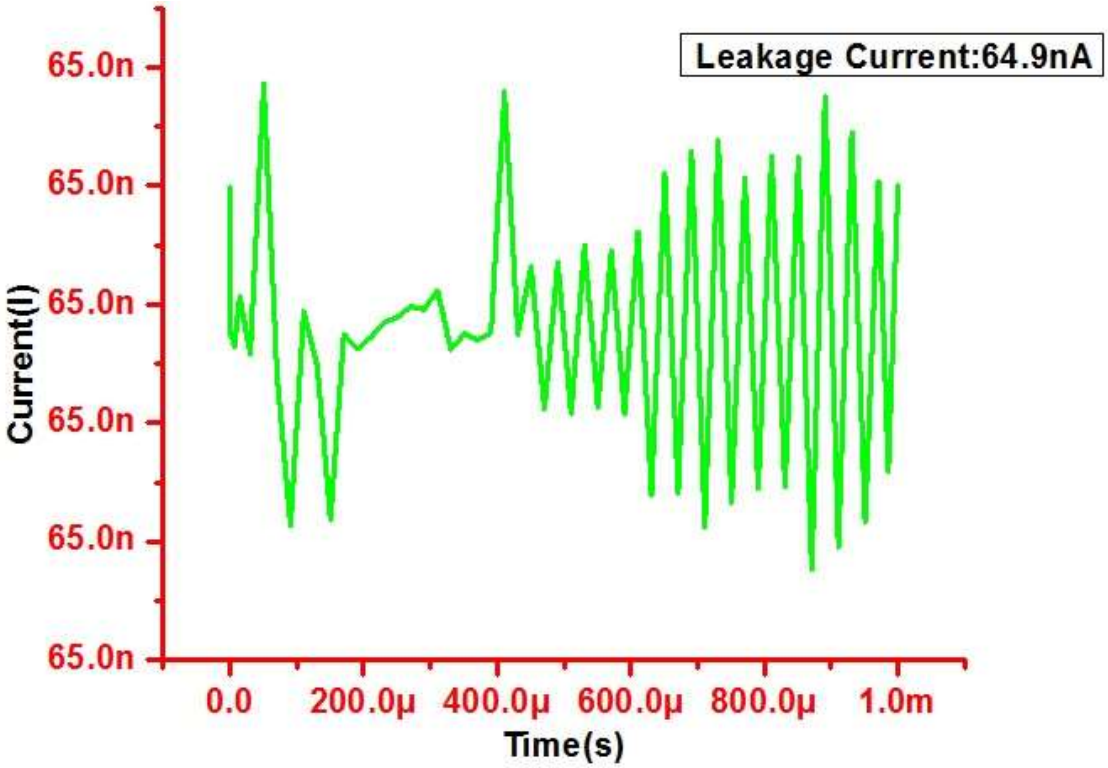

Figure 3.18: Leakage Current in CMOS based 9T SRAM

SNM of MOSFET based SRAM 9 T cell is 327 mV at 45nm technology as seen in Figure 3.19.

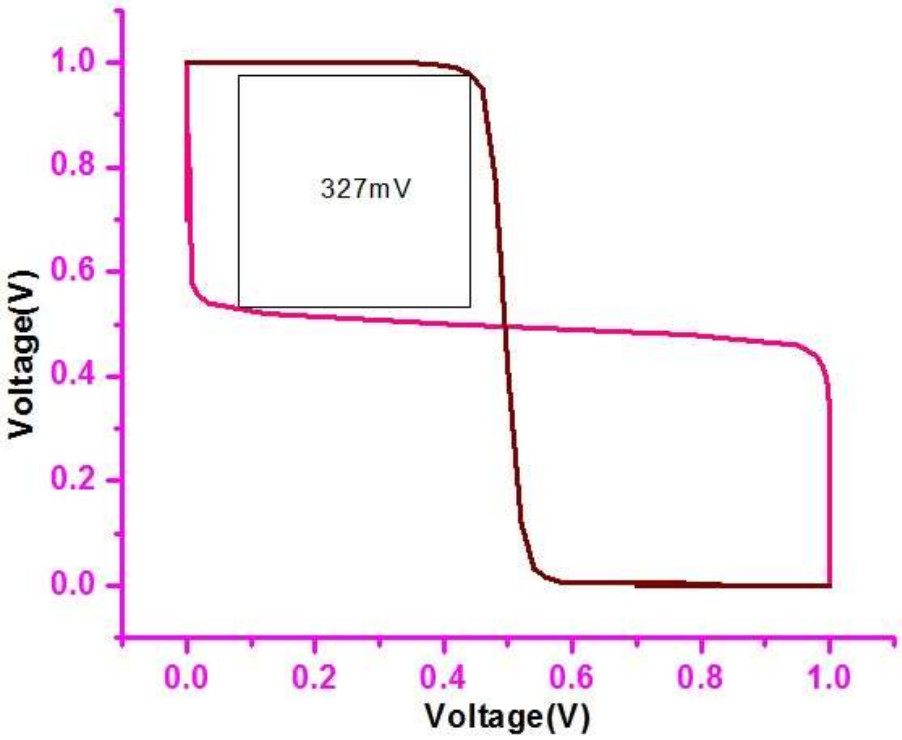

Figure 3.19: SNM of 9T SRAM

3.6.4 10T SRAM Cell

A 10T based SRAM in Figure3.20 has extra two transistors on either side to improve read performance and also write buffer on each side to progress the write performance apart from that it has six main body transistors which make its functionality same as a 6T based SRAM cell.[134]

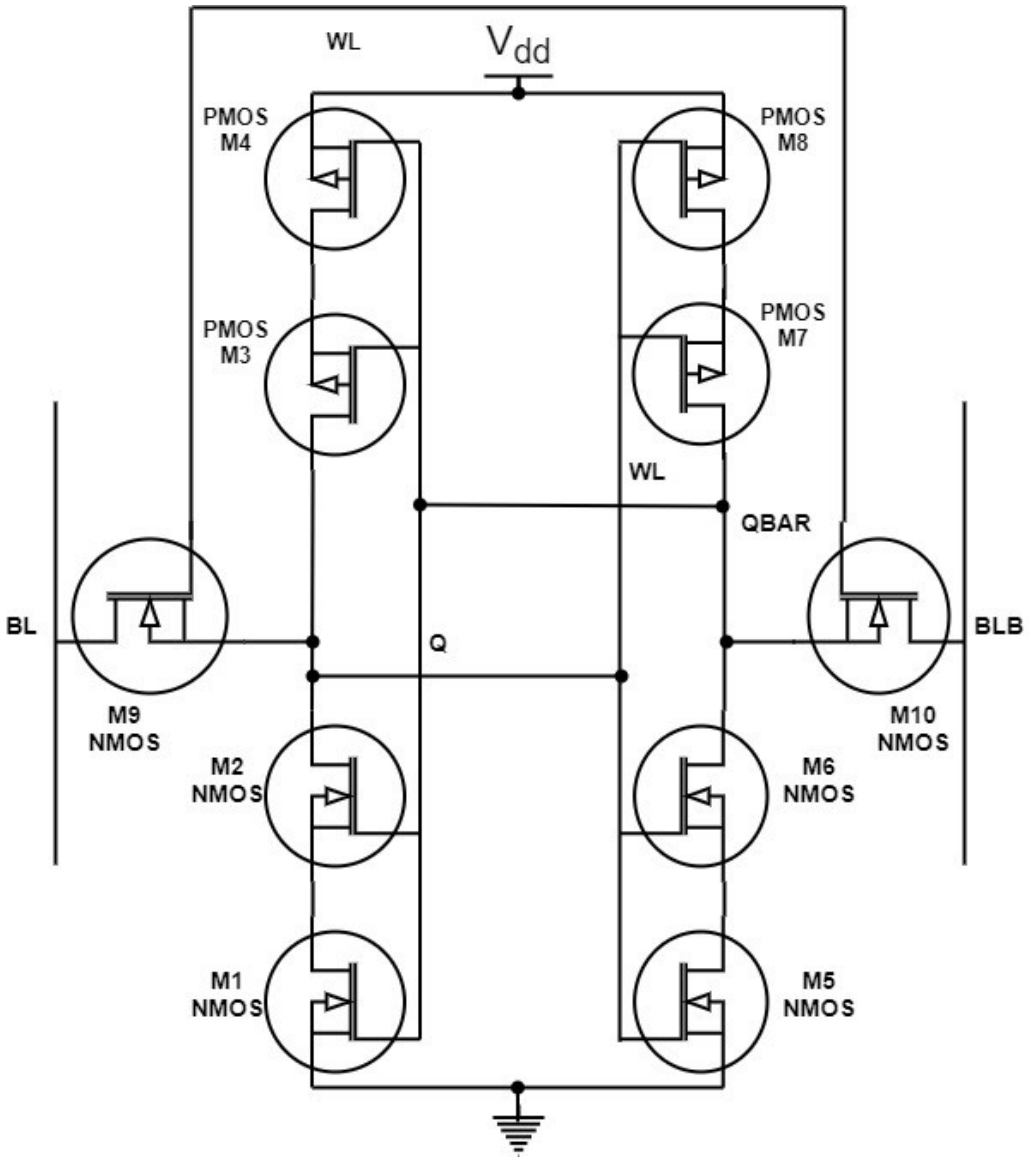

Figure 3.20: CMOS based 10T SRAM

Total dissipated power, leakage current produced in CMOS of 10T based SRAM comes out to be 42.7µW, 65.4nA as shown in figures 3.21 and 3.22 respectively

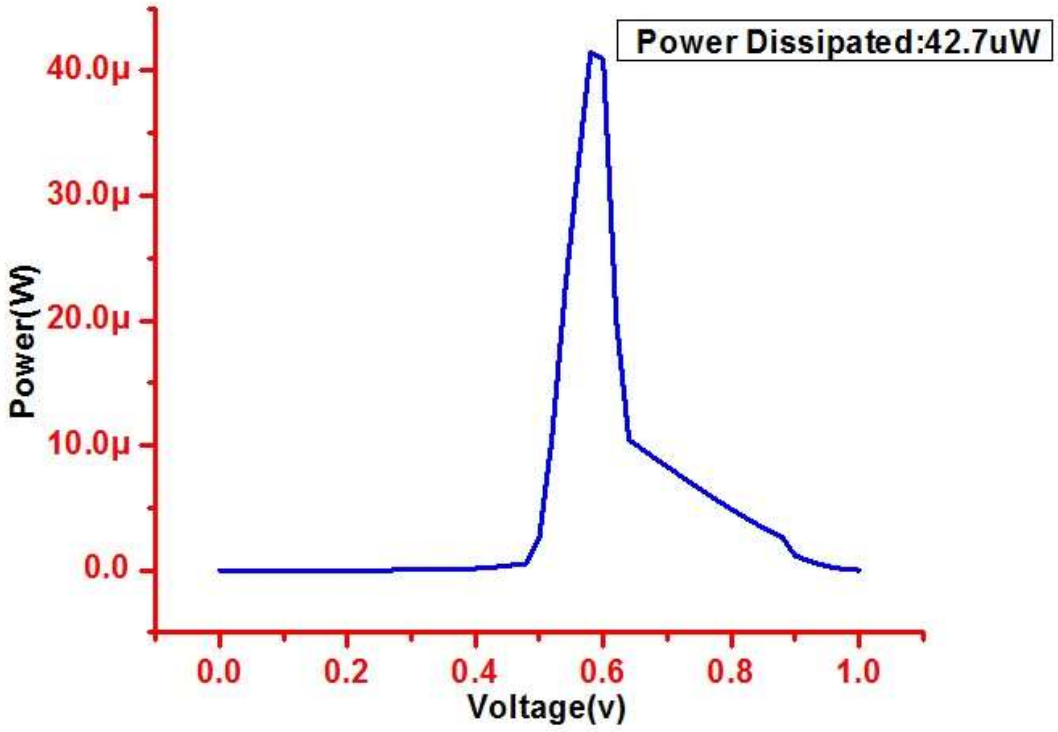

Figure 3.21: Power dissipated in 10T SRAM

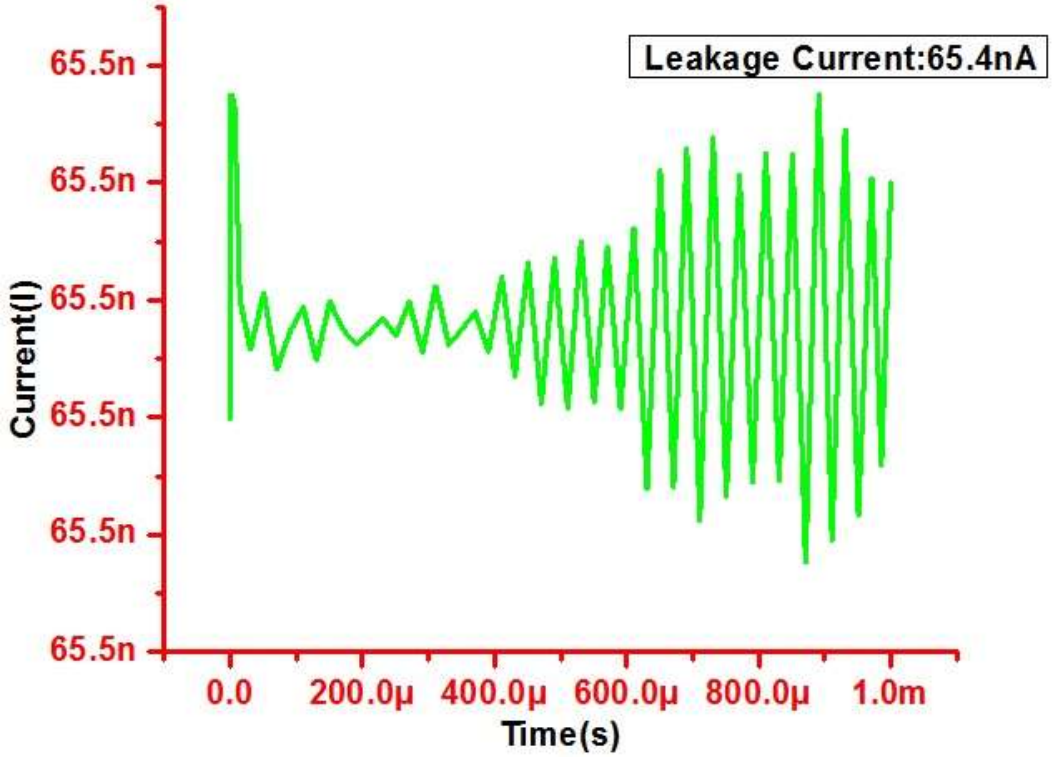

Figure 3.22: Leakage Current in 10T SRAM

SNM of CMOS based 10T SRAM cell is 330 mV at 45nm technology as seen in Figure 3.23.

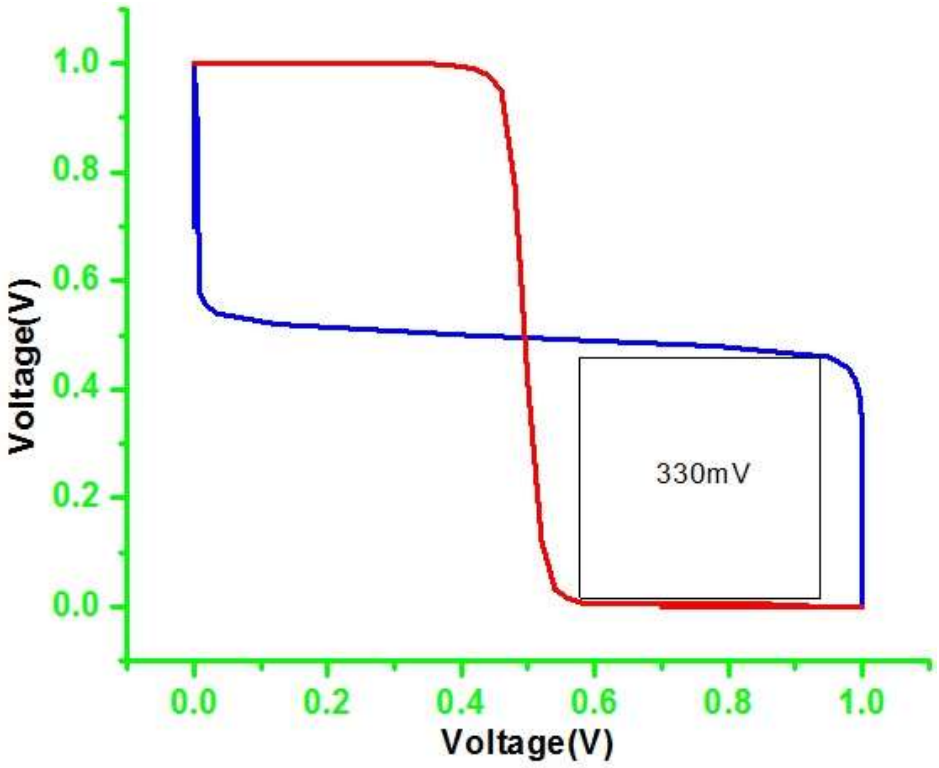

Figure 3.23: SNM of 10T SRAM

3.6.5 12T SRAM Cell

A 12T transistor SRAM is designed for improving a steadiness of SRAM based cell as shown in Figure 3.24 with one transistor on the top and the other in the bottom connected to Vdd and Gnd respectively. [135]

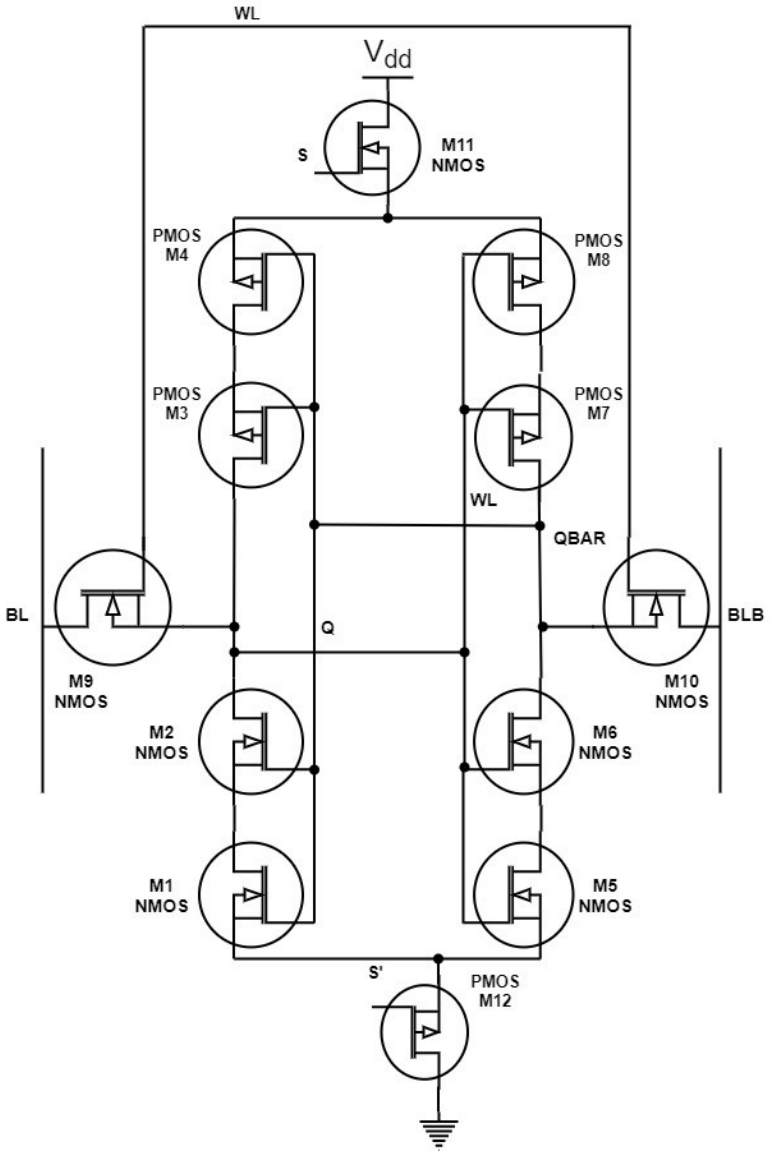

Figure 3.24: CMOS based 12T SRAM

Total power dissipated, leakage current of CMOS based SRAM on 12T cell is 51.3µW and 67.6nA which can be seen in figures 3.25 and 3.26 respectively.

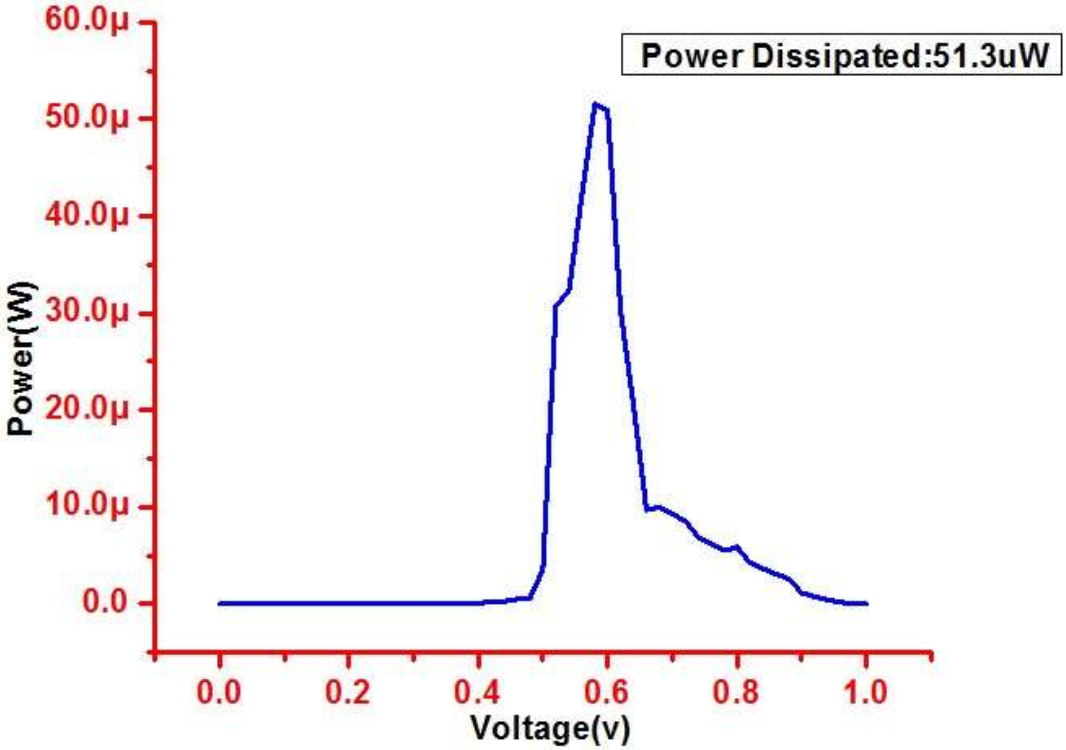

Figure 3.25: Power Dissipated in 12T SRAM

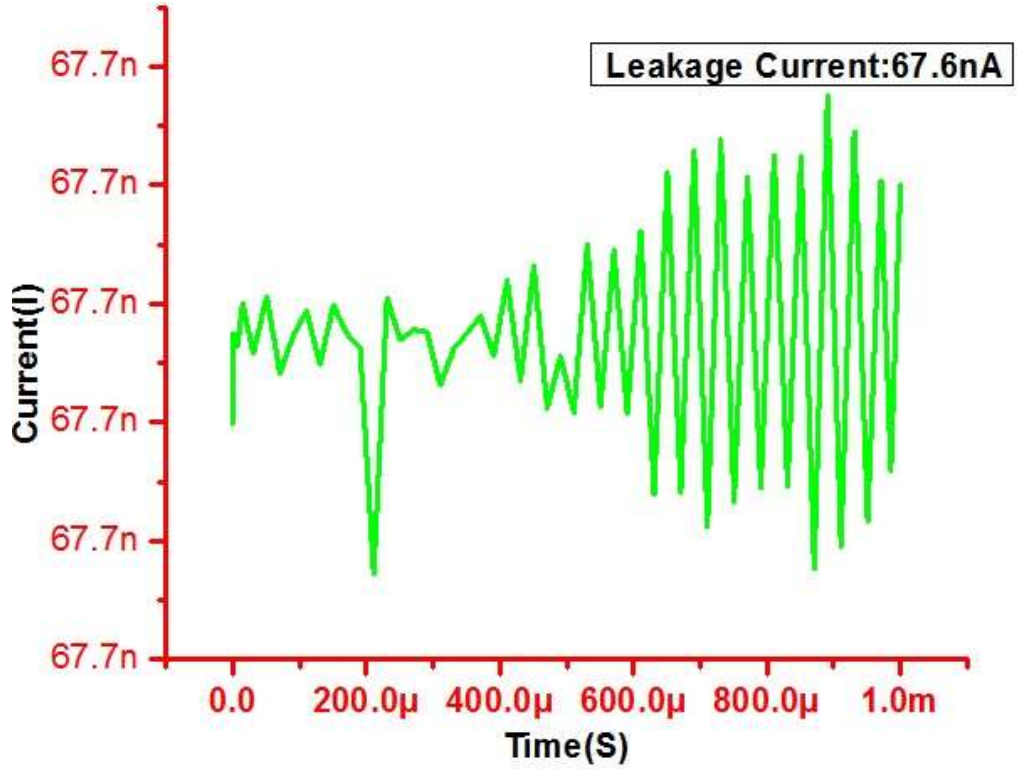

Figure 3.26: Leakage Current in 12 T SRAM

SNM of CMOS based 12T SRAM cell is 340mV at 45nm technology as seen in Figure 3.27.

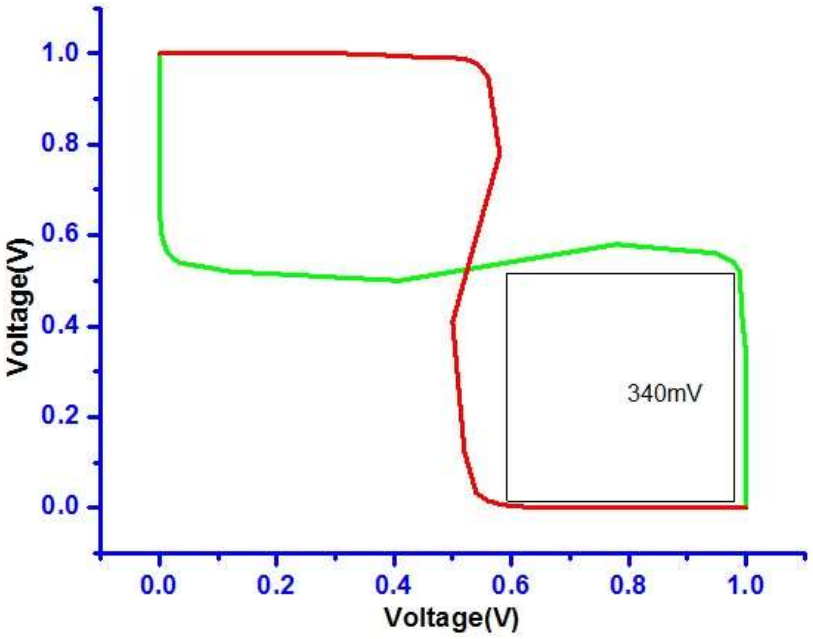

Figure 3.27: SNM of 12T SRAM

3.7 Result Analysis of SRAM cell for different Transistor Topologies

Table 3.1: Performance Comparison CMOS SRAM Cell

S.No	SRAM cell	Power Consumption (nW)	Leakage Current (nA)	Power Dissipated (µW)	SNM (mV)
1	6T	22	61	15.4	271
2	7T	20	59.7	12.8	290
3	8T	25	62.9	22.3	310
4	9T	28	64.9	34.6	327
5	10T	30	65.4	42.7	330
6	12T	33	67.6	51.3	340

From the result of the 45nm CMOS based SRAM cell it is evident that the power dissipation is high for higher order SRAM cell and also it is seen that they have more susceptibility in SNM in comparison to the lower order SRAM cells. The 7T SRAM cell has a bit better power consumption and dissipation of 20nW and 12.8µW compared to other SRAM cells as the has only one transistor extra than the conventional 6T SRAM but there is a difference in the functionality of the cell which makes it better than 6T SRAM. Compared to all the transistor topologies 7T SRAM is better not

only in terms of power but also in terms of area as number of transistors are less than other topologies.

3.8 Conclusion of Chapter

In this chapter a detailed evaluation of CMOS based SRAM cells is done in terms of static noise margin, Leakage current, power consumption and power dissipation, Subthreshold leakage currents for 6T, 7T, 8T, 9T, 10T, 12T at 45nm CMOS technology and comparison of the above parameters is done where the leakage currents are 61nA,59.7nA,62.9nA,64.9nA,65.4nA,67.6nA respectively and power dissipation is found to be 15.4µW,12.8 µW ,22.3 µW ,34.6 µW ,42.7 µW ,51.3 µW respectively and found that 7T SRAM has better performance among all the transistor topologies.

CHAPTER 4
DESIGN AND ANALYSIS OF FINFET BASED SRAM CELL

SRAMs are an important embedded part of the memory in any portable device. The SRAMs have become an integral part of the present-day memories as the device size is decreasing. Specifically, in biomedical applications like wireless body area networks, the low power SRAMs are an emerging trend. Since it is required to have low power devices reduction in power is the main criterion for any kind of VLSI device and it can be done by reducing the size and also the supply voltages. There appears to be not at all feasible alternatives of remaining out using the conventional MOSFET with down scaling from 65nm to 45nm or further smaller nodes. Rigorous Short Channel Effects (SCE) like Drain Induced Barrier Lowering (DIBL), Vth roll off , rising leakage currents like sub-threshold S/D leakage, hot carrier effects and gate direct tunneling leakage that effect in device performance degradation are afflicting the industry [115].

Dropping the V_{DD} helps decrease hot carrier effects and power however deteriorates the performance, which can be enhanced by dropping Vth but it degrades Source/Drain leakage. To rise suitable channel control by the gate and decline DIBL, the oxide width can be reduced but this augments the gate leakage. Resolving one problem directs to another. Definitely, it is felt that as a substitute of planar MOSFETs.The alternate way is to use a FinFET device when the technology is scaled beyond 65nm to have reduced leakage currents and remove short channel effect [116].

4.1 FinFET based 6T SRAM cell

Optimization of FinFET is required for better stability and condensed power feeding. This can be achieved by varying the supply, H_{fin} and also varying the threshold voltages. However, reducing the supply voltage (V_{DD}) below parametric variations has a robust harmful effect on the SRAM stability. Memories are essential to have low power dissipation and short access times, therefore FinFET SRAM cells are used. The FinFET devices are having low power dissipation .so the SRAM with FinFET has different functionality unlike the conventional SRAM here as shown in figure 4.1 the SRAM has N3, N4 access transistors which have to be always ON for read and write process since they are the connectivity between the cross-coupled transistors acting as inverters and the Word, Bit and Bit_b line [119].

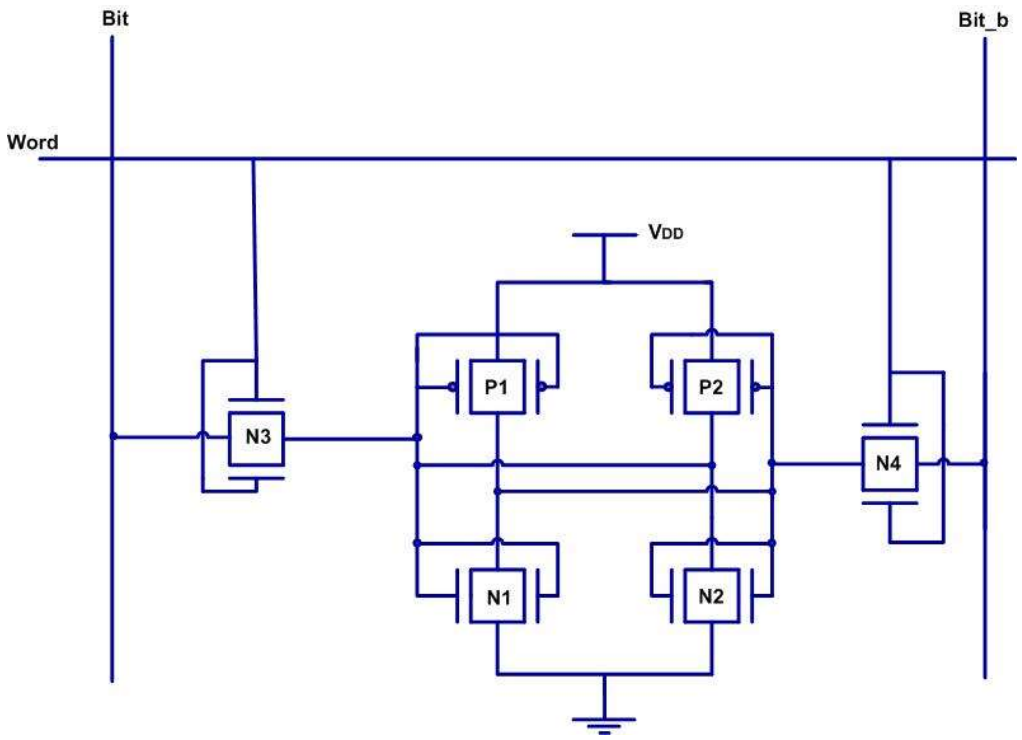

Figure 4.1: FinFET based 6T SRAM

4.2 SRAM operation

SRAM has three different modes of operations read, write and hold. The SRAM cell must have better performance to operate in read and write mode.

4.2.1 Read Operation

In this, operation takes place only by using single transistor pair. The read process takes place when both bit line and bit_b line are set and by setting P2 ON and N2 OFF the data falls and it rises when the condition is vice versa. This process takes place when word line is maintained by the access transistors N3 and N4

4.2.2 Write Operation

In this the data is supplied to the bit line and bit_b, subject to the data to be written both the lines are assigned with data which is opposite in nature. The word line is then triggered so that the data written is stored. The write operation can be benefited by increasing the number of fingers of the FinFET, but not in all cases.

4.2.3 Hold Operation

In this state there is no connectivity between the word line, bit line and bit_b with the cross-coupled devices as the transistors N3 and N4 are the OFF-inverter transistors support each other to maintain the data as long as possible

4.3 Performance Parameters

4.3.1 Static Noise Margin (SNM)

During read operation the invulnerability by the cell to flip it is categorized using Static Noise Margin (SNM). It is evaluated by the biggest square side inside the FinFET measured during the read condition (wl = VDD and wbl = wblb = VDD) based on SRAM cross-coupled inverter [89].To calculate the stability in SRAM bit cells Static Noise Margin parameter is used. FinFETs used in SRAM cells, SNM is dependent on the selection of the V_{th}. High value of V_{th} represents that these devices drive small current resulting the write operation to be complex, thereby, increasing the value of SNM. One method is to use high V_{th} devices at the cost of performance to achieve a low power cell with high stability. [90].

4.3.2 Power Dissipation

Power dissipated in the FinFET SRAM cell shows the effectiveness of the cell in portable memory devices. Low leakage current and SCE‘s in FinFET device, low power dissipation are elementary benefits of this cell. In SRAM cell the power dissipation is added although a high driving current cuts down access time [121].

4.3.3 Power Consumption

Embedded large SRAM arrays occupy a major segment of application processor with overall power. In an SRAM array power consumption contains very elongated idle periods and small active periods. Standby power consumption is the major concern for large arrays. Thus, in large memory’s reducing the leakage become indispensable for applications based on low power. Leakage in cell is usually expressed by long channel length or high threshold voltage of a transistor. Cell area is negatively impacted by long channel length. In addition the use of long channel length is to amplify the bit line ‘wl‘ and bit line bar ‘wbl‘ capacitances, that increases the

power and access time. Hence length of longer channel is used for calculating the power consumption during different write process. [123]. at particular operation when transistor is in ON condition, we can calculate current and voltage. Due to low current at read operation an access time is impacted negatively by a high threshold voltage. Though, both the margins read and write are improved. While in NMOS transistor a high threshold will be pulled down that increase the trip point and PMOS will decrease. whereas the pull-down device has a capability of current driving that is greater than PMOS and increase in the NMOS threshold voltage will have a larger impact on voltage at trip and have larger write and read margins [124].

The leakage Current of FinFET based 6T SRAM cell is 51.31nA and the power dissipated is 35.91nW.The leakage current and power dissipation is as shown in figure 4.2 and 4.3 respectively

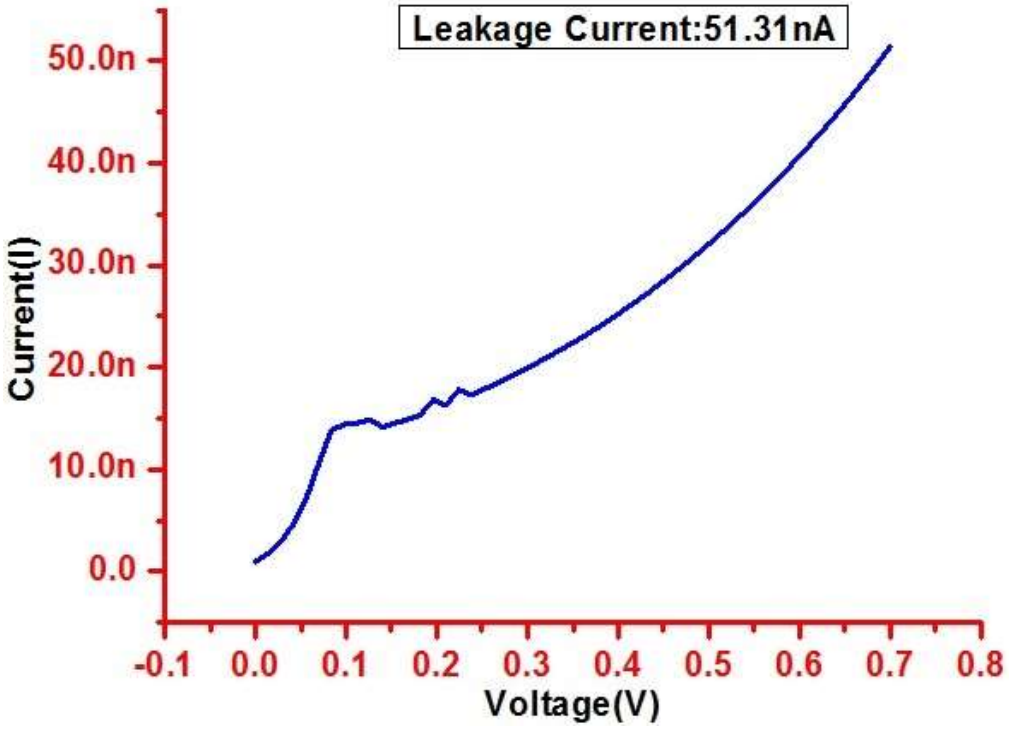

Figure 4.2: Leakage Current of FinFET based 6T SRAM

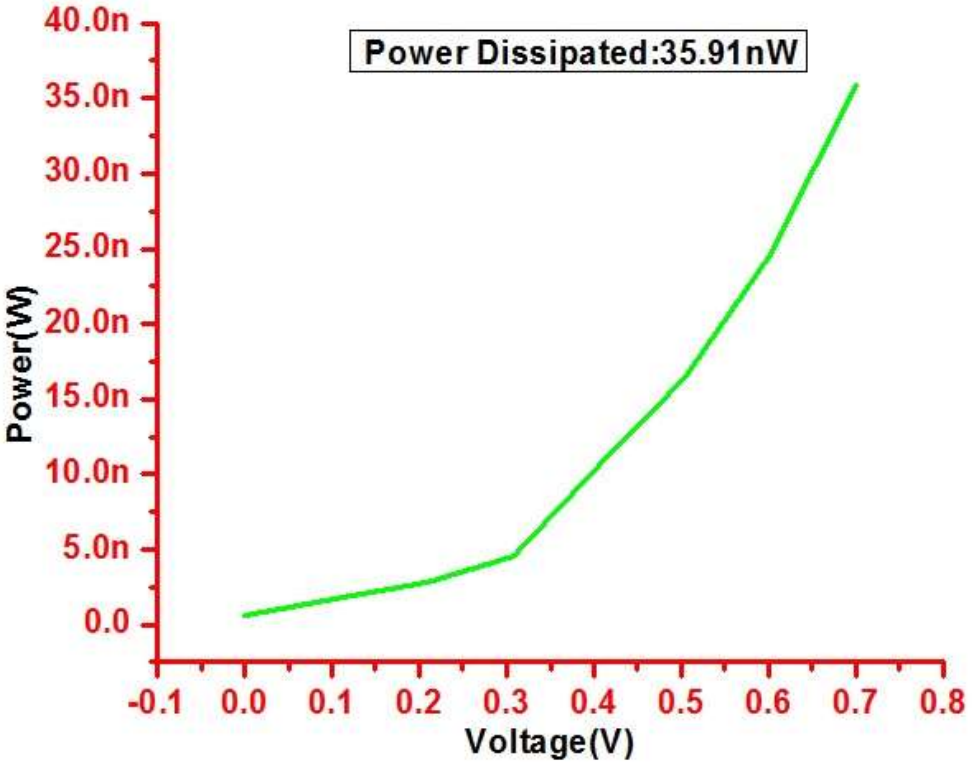

Figure 4.3: Power Dissipated of FinFET based 6T SRAM

The Static Noise margin of the 6T SRAM is 280mv which is shown in figure 4.4

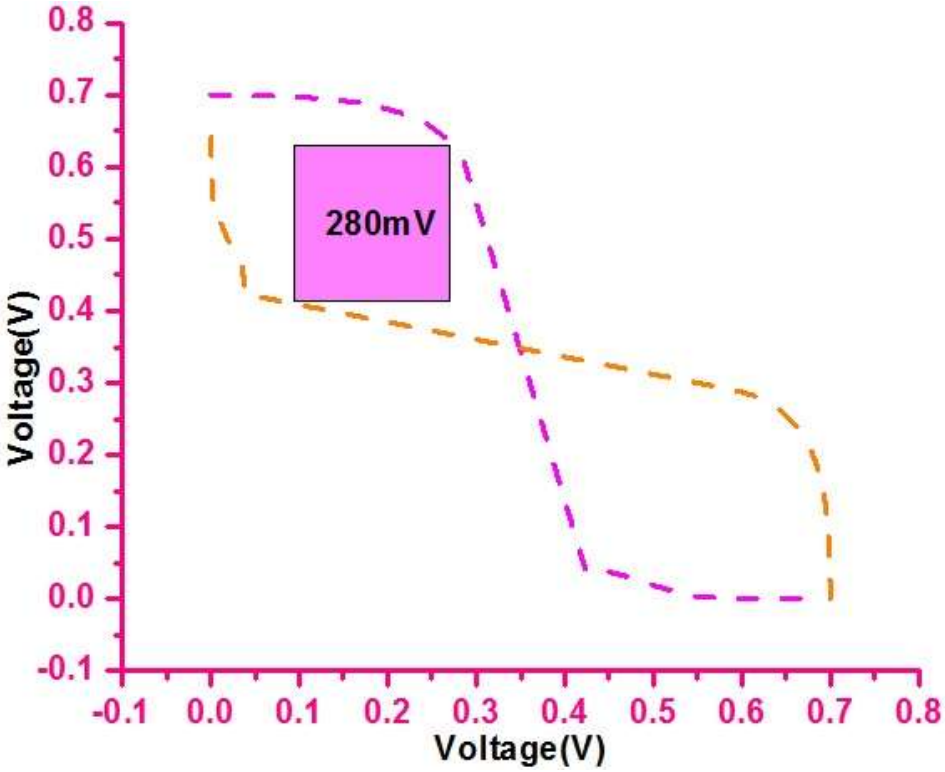

Figure 4.4 : 6T SRAM SNM

4.4 Design of Proposed FinFET Based 7T SRAM Cell

A fundamental goal for proposing a 7T SRAM cell is to device abundant Read Steadiness and SNMs. A structure of proposed 7T based SRAM is represented in Figure 4.5. A new SRAM based cell is comprises of 7 transistors that utilizes one RL, WL, and BL. Moreover, writing the data to a cell we utilize WL and BL and we don't utilize RL. While reading process we utilize BL and RL and we don't utilize WL. A 7T based SRAM cell employs single BL & WL or RL. Whereas a 6T SRAM based cell will require all three bit lines and it consumes more power compared to 7T based SRAM cell.[136]

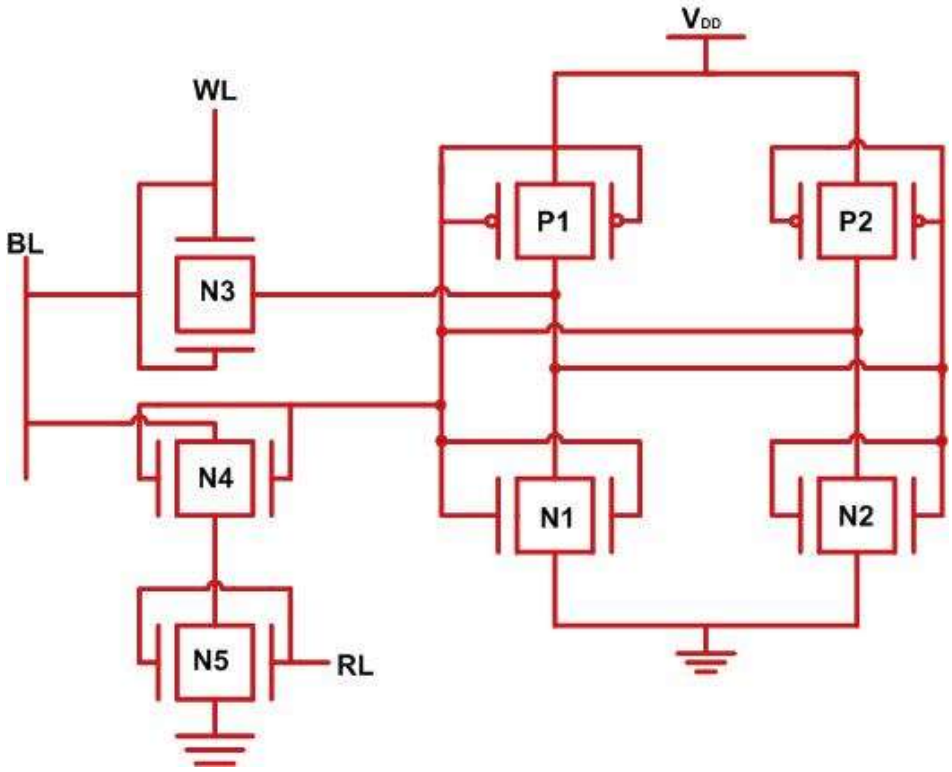

Figure 4.5: Proposed FinFET based 7T SRAM

As 7T based SRAM Cell will always utilize one BL and a controlling the various operations is reduced. Thus, by using only one BL we can decrease a voltage used for switching BL transistor ON and OFF to across 50%, on GND where one BL is enough for reading the data compared to two BL. A BL is 50% charged for a particular time instead of charging it for write activity. I1n this situation an equivalent likelihood of writing a 1 or 0. The proposed 7T SRAM cell uses dual transistors NMOS4 and NMOS5 by a load resistor for reading a data.

Operations of 7T SRAM

A) Write

During the write process, the information to be written is stacked with BL and then WL is enabled. The transistor N3 permits BL to suppress the SC, so that the cell is written with essential information. BL should be charged to VDD for writing ‘1’ in to the SC. In event that ‘o’ has to be written, BL is low, and WL will be level of power supply. RL is not active in Write mode.

B) Read

The information in the cell can be read with the BL which is already-charged to VDD. Once initially charged then bit line RL is triggered. Relying on whether BL will discharge or not and holds command charge, information saved within 7T SC is set. If there is a discharge in BL by increasing a read line to supply voltage, and 7T based SC will hold ‘0’. If BL holds charge then data stored will be ‘1’, and during read process word line will turn into inactive state.

Consider the 7T SC holds a ‘0’ primarily. The two transistors NMOS4 and NMOS5 will be ON with bit line that charges towards VDD, and pulling RL towards V_{DD}. Since the data stored is ‘0’ the transistor NMOS4 will be ON and as RL is at VDD the transistor NMOS5 is ON. Currently, BL has a connection to ground via NMOS4 and NMOS5 by discharging to logic ‘0’ specifying data stored is ‘0’. Consider that 7T SC is storing ‘1’.RL is increased to V_{DD} by pre-charging the BL, NMOS4 will be OFF, NMOS5 will be ON. Since Q_b is at ‘0’, NMOS4 is OFF and because RL is at V_{DD} NMOS5 is ON. The data Stored is shown as ‘1’ as there is no path for BL to decrease to 0 levels.

C) Hold

In this state, the SRAM maintains the data till the power supply is ON. Depending on the data stored i.e. if data contained in the cell is ‘1’ then Q will be at V_{DD} and Qb will be at ‘0V’ and vice versa if the stored data is ‘0’.

The proposed 7T SRAM cell has leakage current of 50.26nA and Power dissipation of 35.22nW which can be seen in the figures 4.6 and 4.7 respectively.

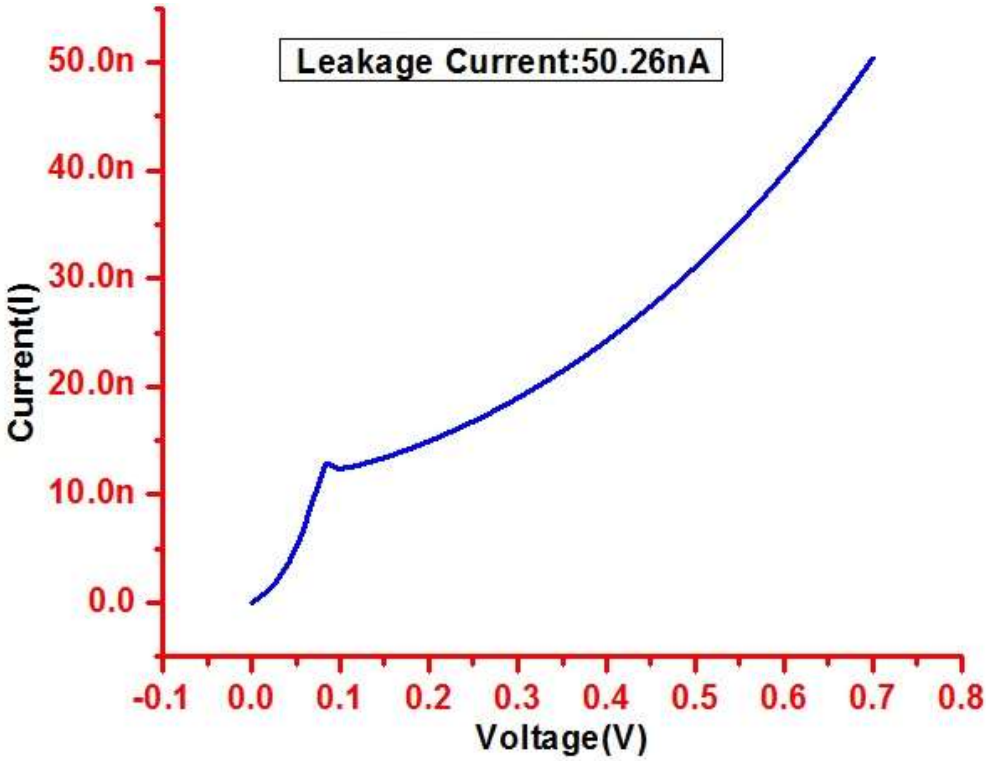

Figure 4.6: Leakage Current of Proposed 7T SRAM

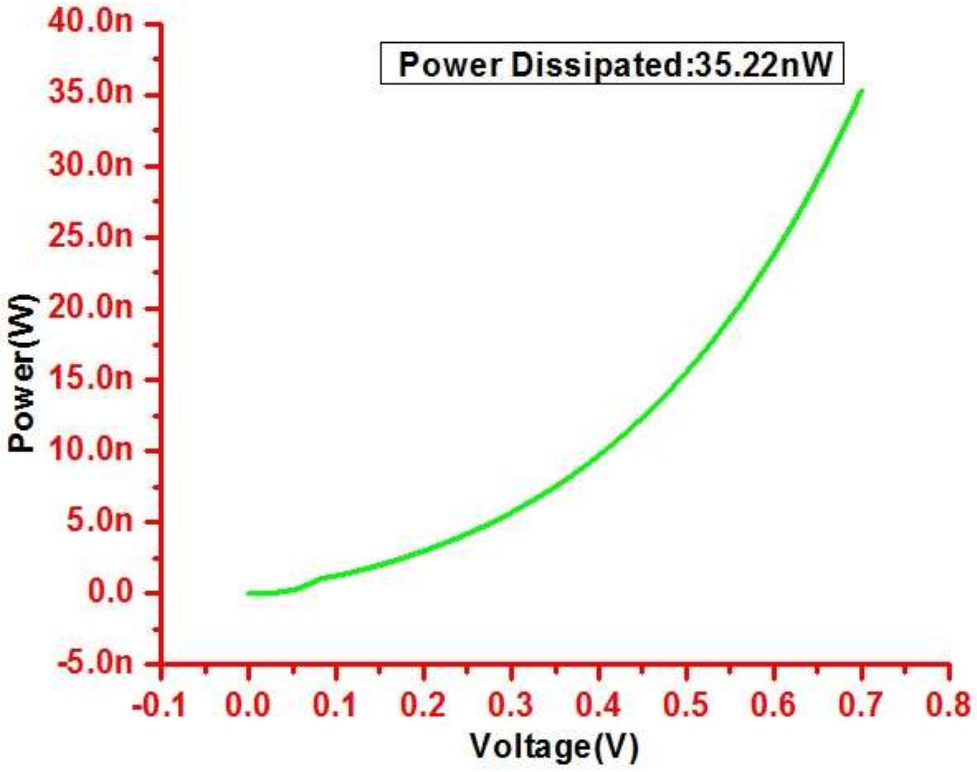

Figure 4.7: Power Dissipation of 7T SRAM

The SNM ratio of the proposed 7T SRAM cell is 291mV which is a bit less than the 8T SRAM cell. The SNM ratio here is showing the cell stability in performing read and write operations, in an 8T SRAM the extra transistor is useful in increasing that SNM, apart from the stability the power consumption and area also should be considered so SNM in case of 7T SRAM is a bit compromised which is shown in figure 4.8.

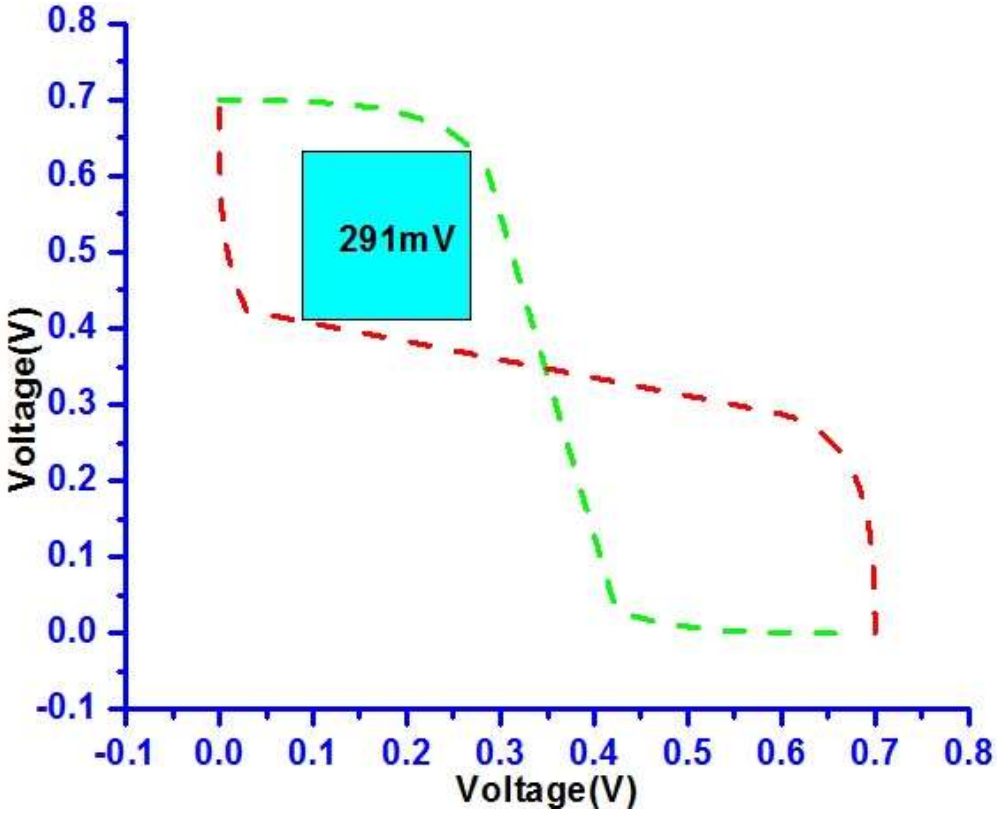

Figure 4.8: SNM of 7T SRAM cell

The subthreshold leakage current of N type and P type FinFET devices individually is simulated and it is found to be 2.84pA and 2.04pA respectively and is shown in figures 4.9 and 4.10

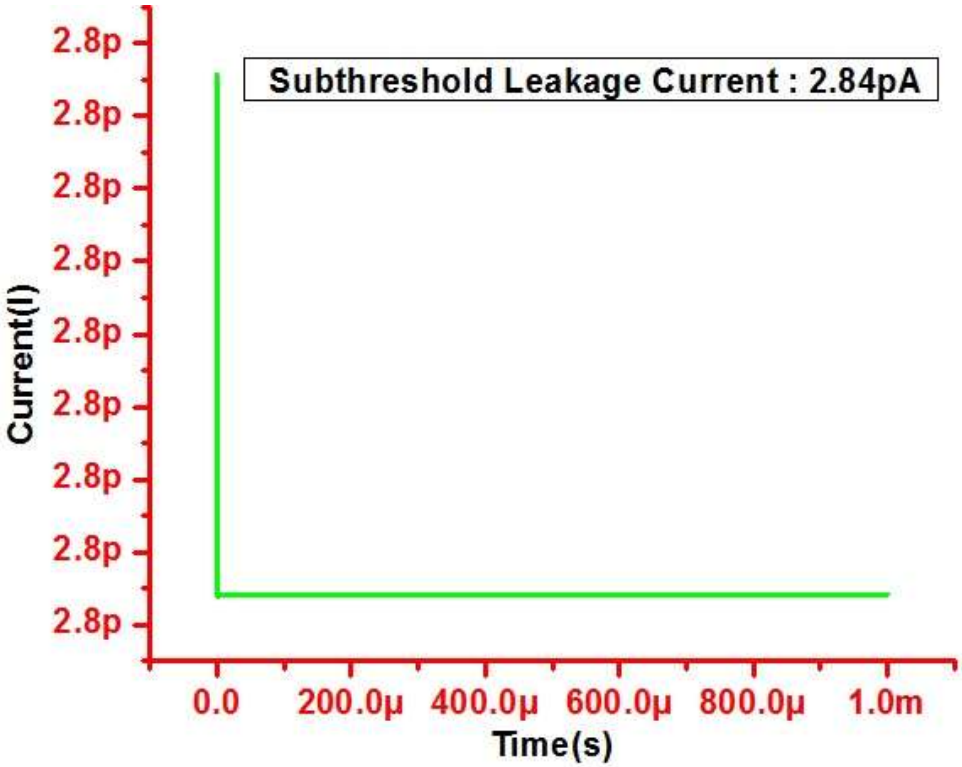

Figure 4.9: Subthreshold leakage in N type FinFET

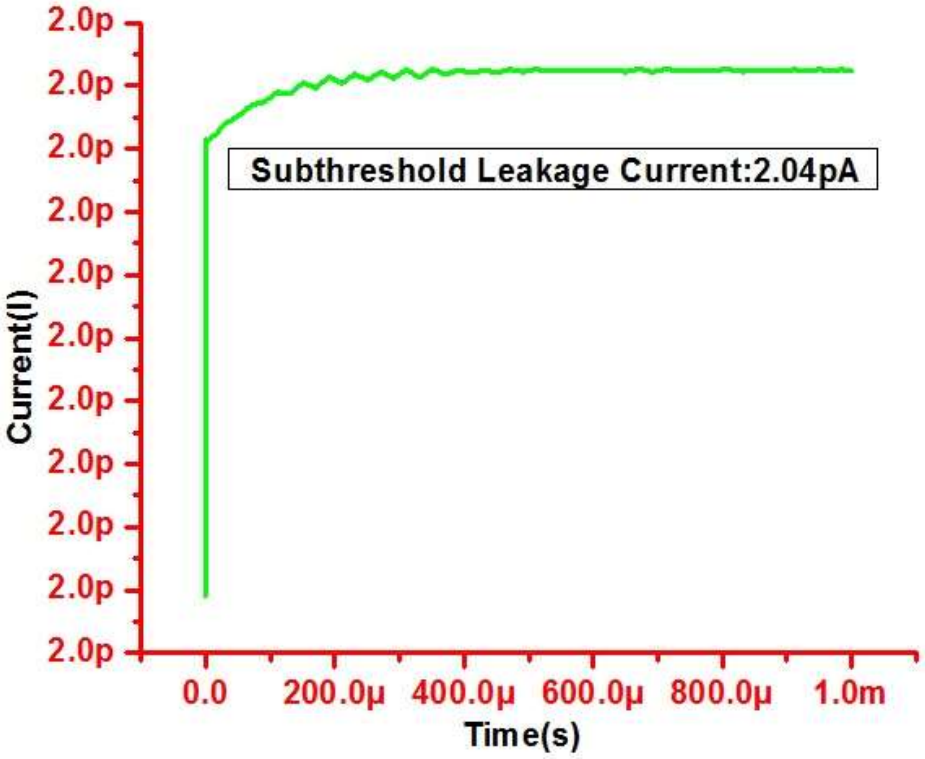

Figure 4.10: Subthreshold leakage in P type FinFET

4.5 FinFET Based 8T SRAM Cell

A 6T SRAM cell has a fundamental problem of processes such as read and write which doesn't match with each other. Whereas cell that has low read SNM values will have a write ability of improved version and vice-versa. Consequently, when both the operations read and write are decoupled from each other, then the VLSI designers will have more flexibility for optimizing the operations independently. To overcome the problem, a proposed 8T SRAM cell will isolate the read operations from write operation to achieve a good stability by enabling the lower voltage. Figure 4.11. Exhibits an 8T SRAM bit cell. For 6T SRAM cell, two FET's are added to provide the reading of data that doesn't affect the cell nodes. Hence it requires separate lines for both read and write (RWL and WWL) and will accommodate two operations based on respective lines as shown in Fig 4.11. The reading of data is carried out by RBL charging and activating the word line. At node Q a bit '1' is stored and transistor N6 is turned ON and that provides low resistance path for allowing the current to flow through read bit line towards GND [137]. During the failure a read disturb is ignored under the worst condition of FinFET based 8T SRAM cell.

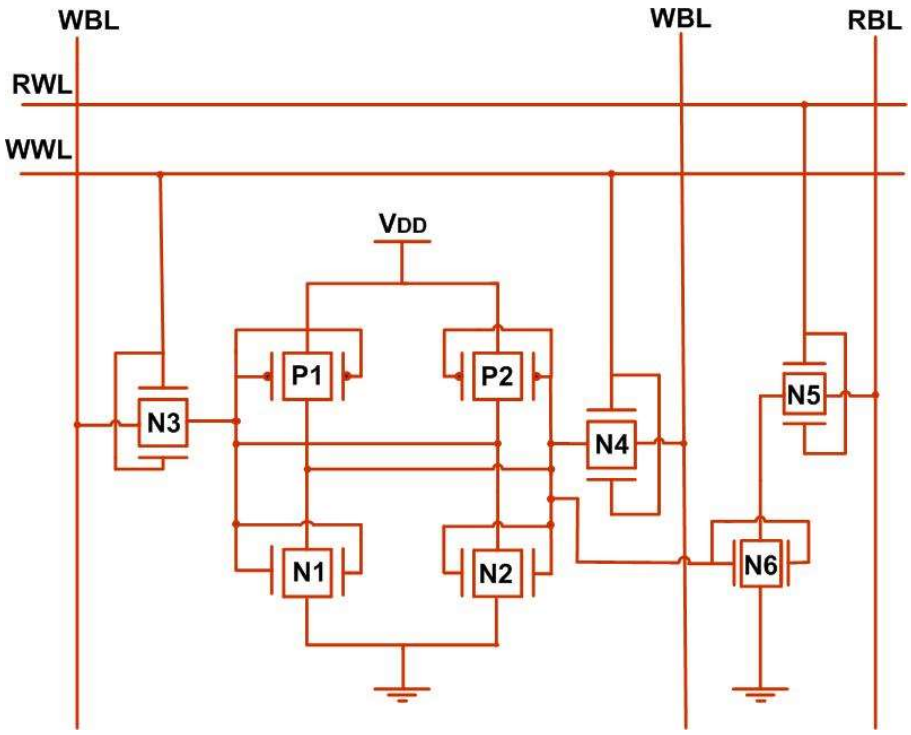

Figure 4.11: FinFET based 8T SRAM

The development in SNM and reduction in power that got dissipated and leakage current of projected FinFET based 8T based SRAM cell as compared to MOSFET based 8T based SRAM cell validate our design approach.

The static noise margin for FinFET based 6T SRAM cell is 280mV whereas for FinFET based 8T SRAM cell is depicted in Figure 4.14 a remarkable stability enhancement can be achieved without a trade-off in performance as a read access is still done by two stacked nFETs. Leakage current and power dissipation of 8T SRAM cell is 52.63nA and 36.84 nW respectively which is shown in Figure 4.12 and Figure 4.13 respectively.

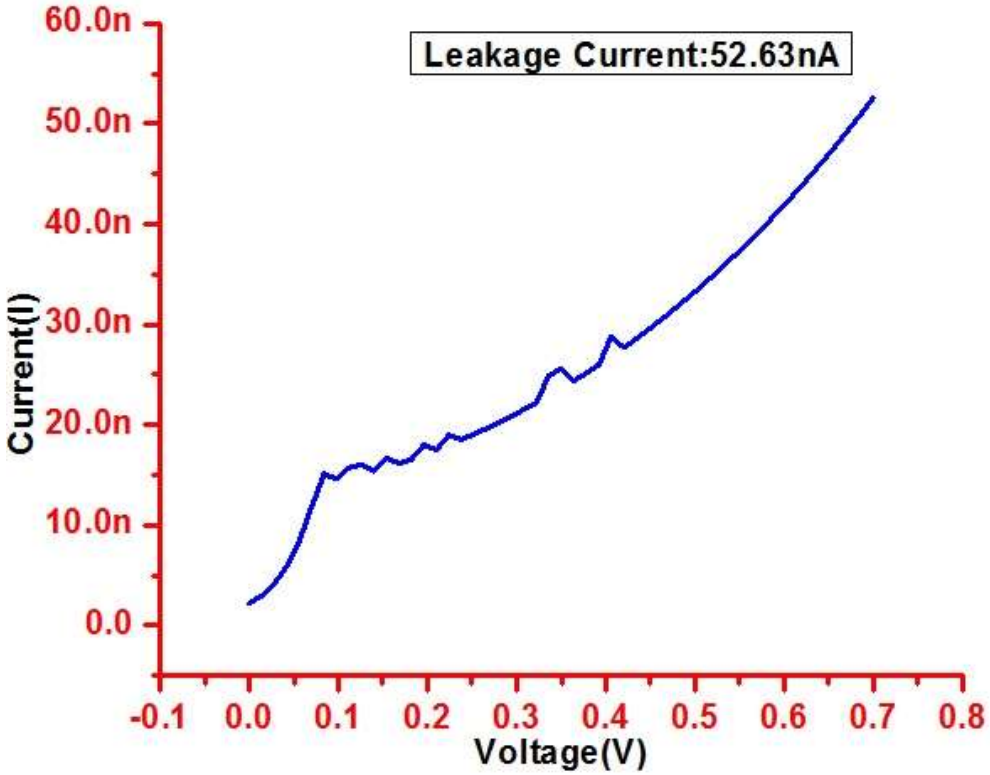

Figure 4.12: Leakage Current of 8T SRAM

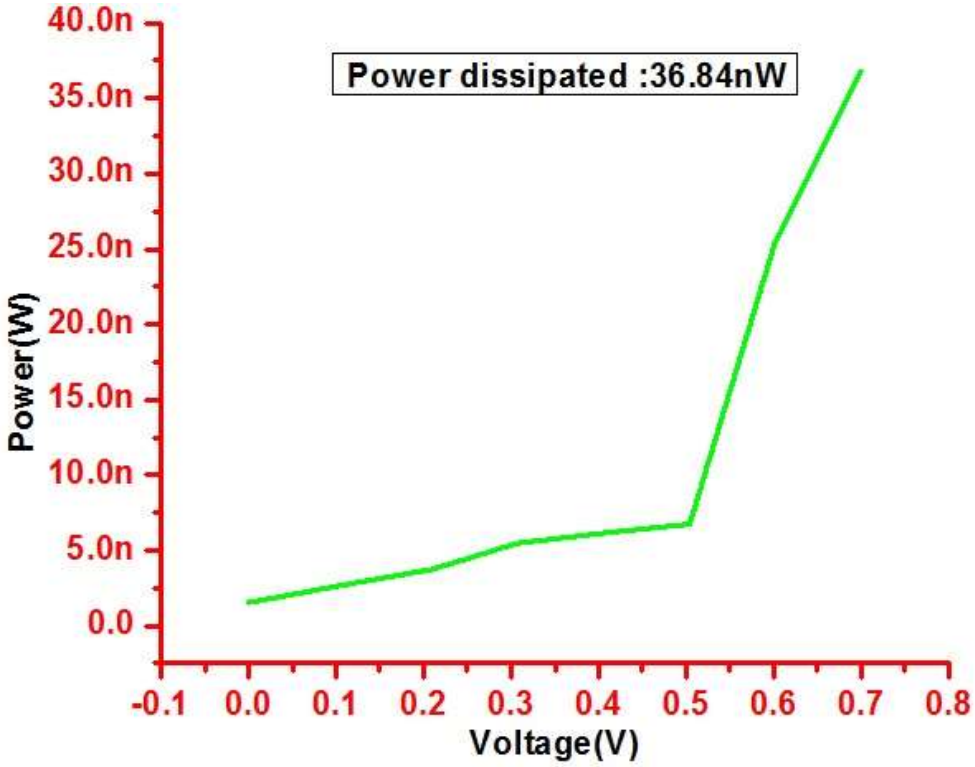

Figure 4.13: Power dissipation of Current of 8T SRAM

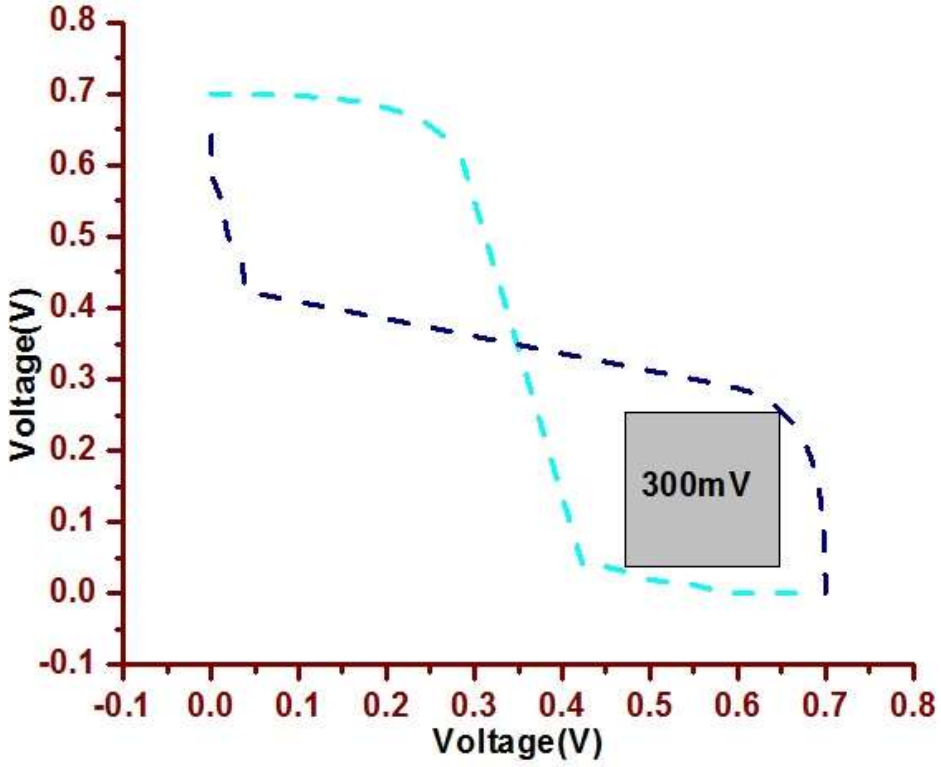

Figure 4.14: SNM of 8T SRAM

4.6 FinFET Based 9T SRAM Cell

An initial design of 9T SRAM is introduced in figure 4.15 and it is shown below. The design structure is similar to 8T SRAM cell structure with transistors M1 to M6 unaffected as in 6T based SRAM cell. In cell write access happens by transistor write access from the WBL and WBLB. Read access happens by a read access happens by a read access transistor and it is controlled by RWL. RBL is pre-charged for reading the data. RWL for read is different from a WWL for an 8T SRAM cell. The problem of leakage is observed on RBL that cause to change the data during read operation. Therefore, bit line should be kept high, but it will fall to zero, because of leakage in bit line due to the cells that are unassessed. This problem allows 8T SRAM cell to work for low power applications. Hence problem is resolved in 9T SRAM cell with an extra transistor M9 that is added between two transistors M7 and M8. So that the leakage observed in bit line is reduced by a method called stack effect. [138]

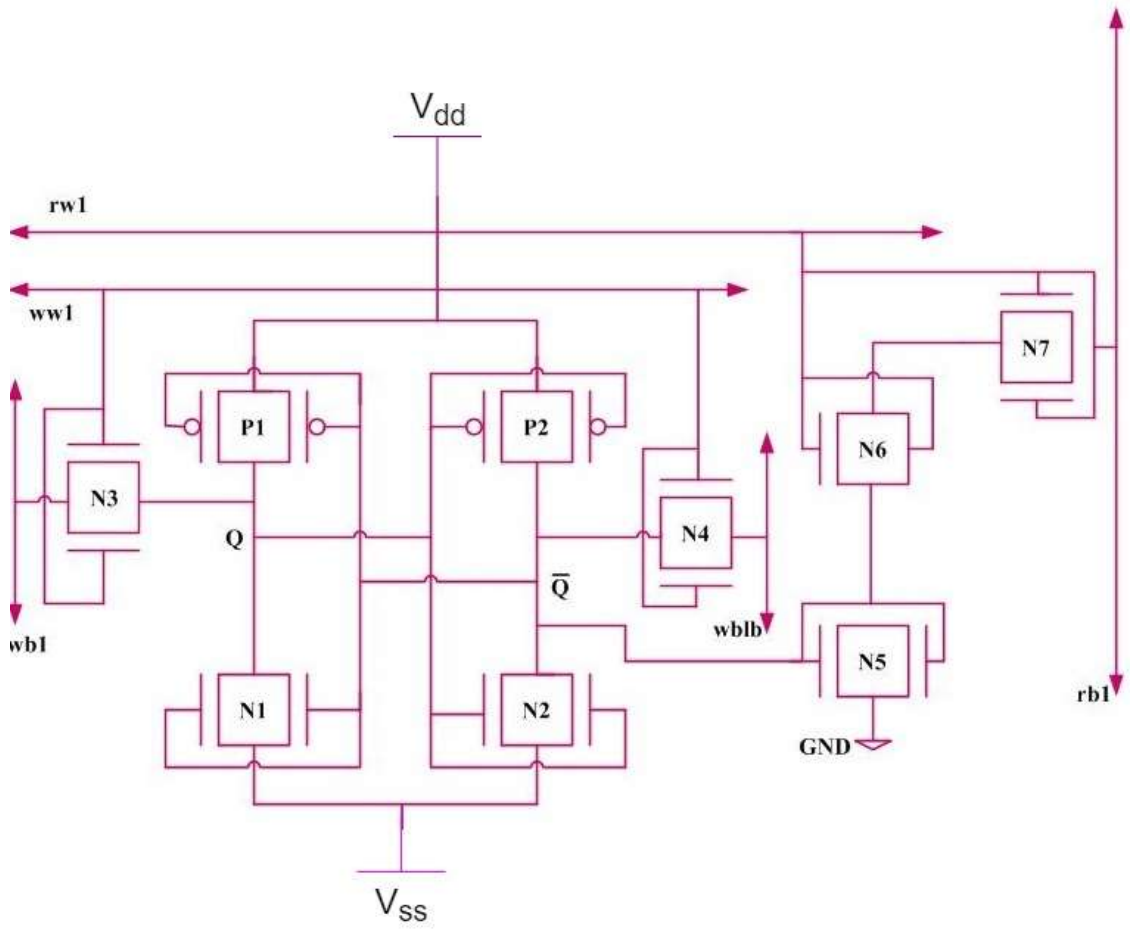

Figure 4.15: FinFET based 9T SRAM

Here at each gate leakage current gets affected by input pattern. The transistor leakage in stack is due to input pattern and total amount of transistors. In 9T based SRAM will have effect of stacking when transistors are in OFF state and are in series connection. Thus, the upper transistor has a source voltage that is greater than lower transistor that are in stack. Therefore, threshold voltage increases at high voltage provided due to upper transistor. Hence this increase of threshold voltage will decrease the leakage current.

The threshold voltage is increased due to higher voltage of the upper transistor. This increment of the threshold voltage reduces the leakage. Hence, this reduction is called stack effect. The leakage current of 52.87nA and power dissipation of 37.1nW for FinFET based 9T SRAM cell is shown in Figure 4.16 and Figure 4.17 respectively. And the SNM is 270mV as shown in Figure 4.18.

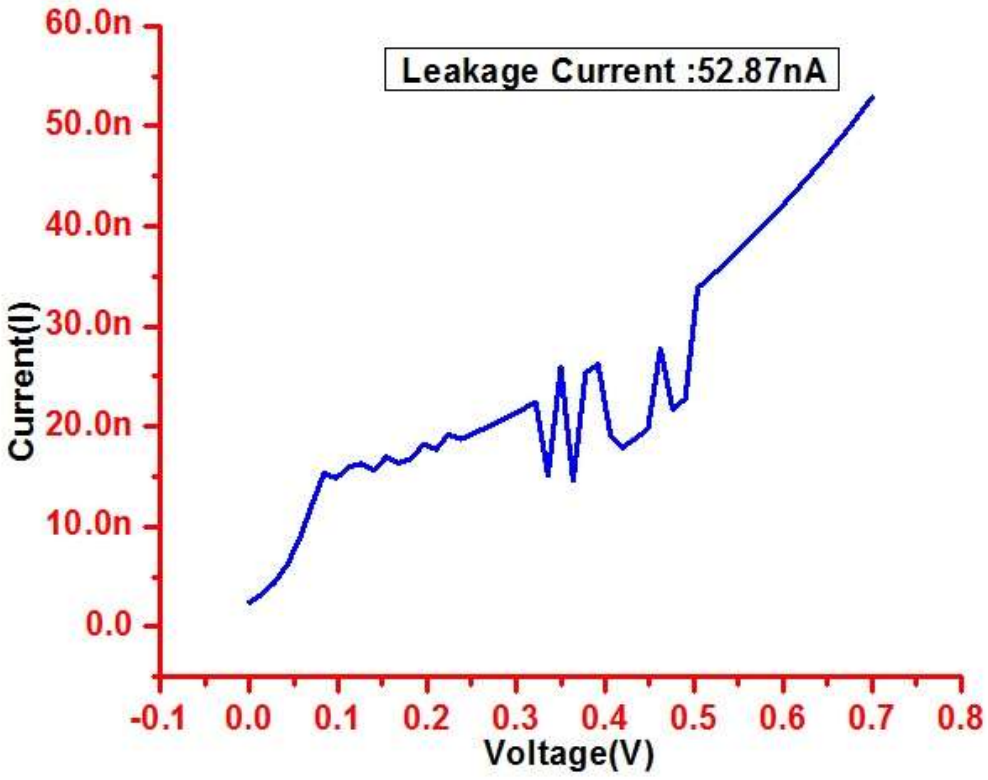

Figure 4.16: Leakage current of 9T SRAM

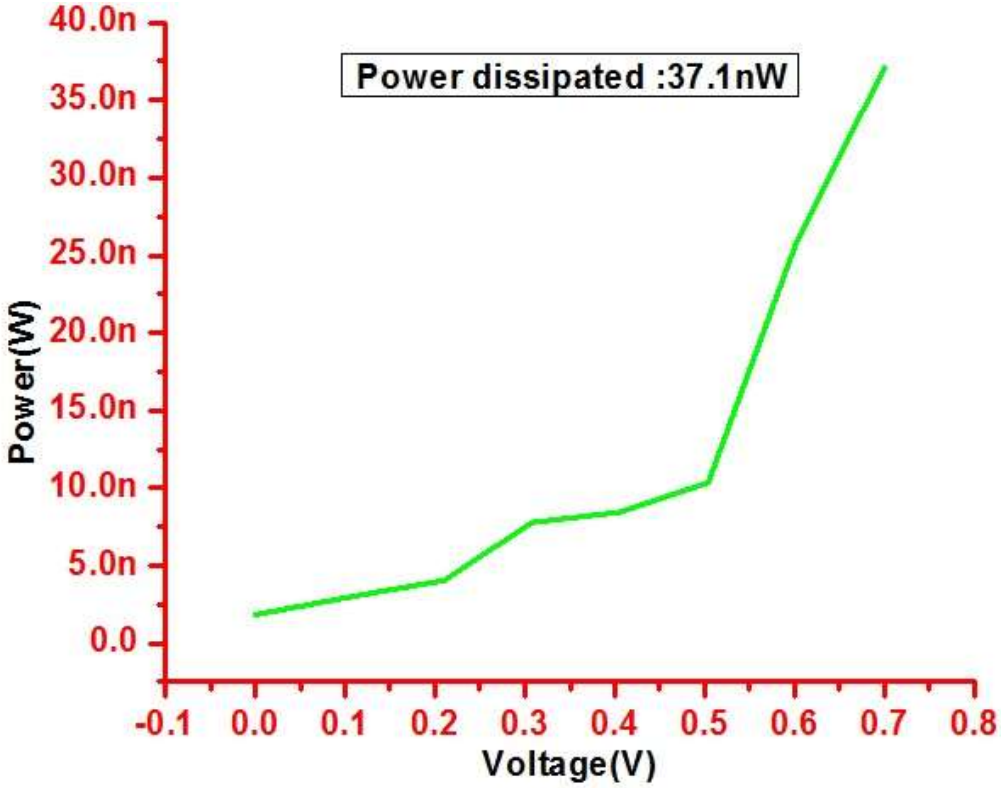

Figure 4.17: Power dissipated of 9T SRAM

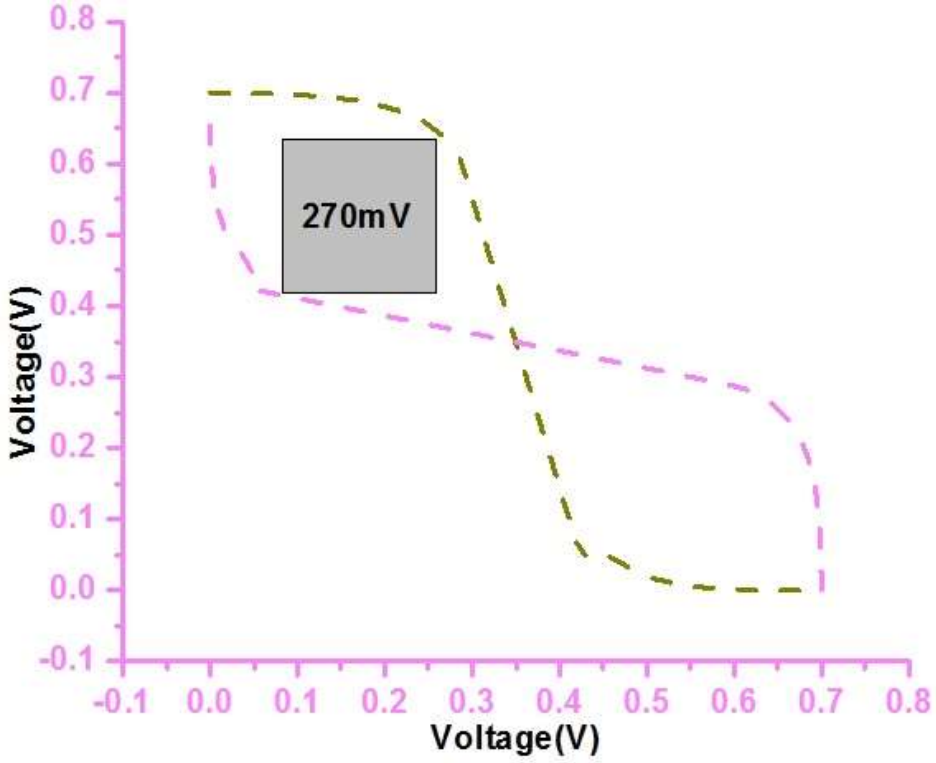

Figure 4.18: SNM of 9T SRAM

4.7 10T SRAM CELL DESIGN

The requirement for further reducing a leakage current and dissipation of power led to a development of 10T based SRAM. Here in this data nodes are completely decoupled from both the access read, write. The 10T based SRAM bit cell that is designed [96] and shown in Figure 4.19. It makes use of transistors M7–M10 for reducing leakage current when compared with 9T based SRAM. M10 will drastically reduce the leakage power[122]. This Leakage current, power dissipation for FinFET based 10T SRAM cell is shown in Figure 4.20 and Figure 4.21 respectively. And the SNM is 267mV as shown in figure 4.22.

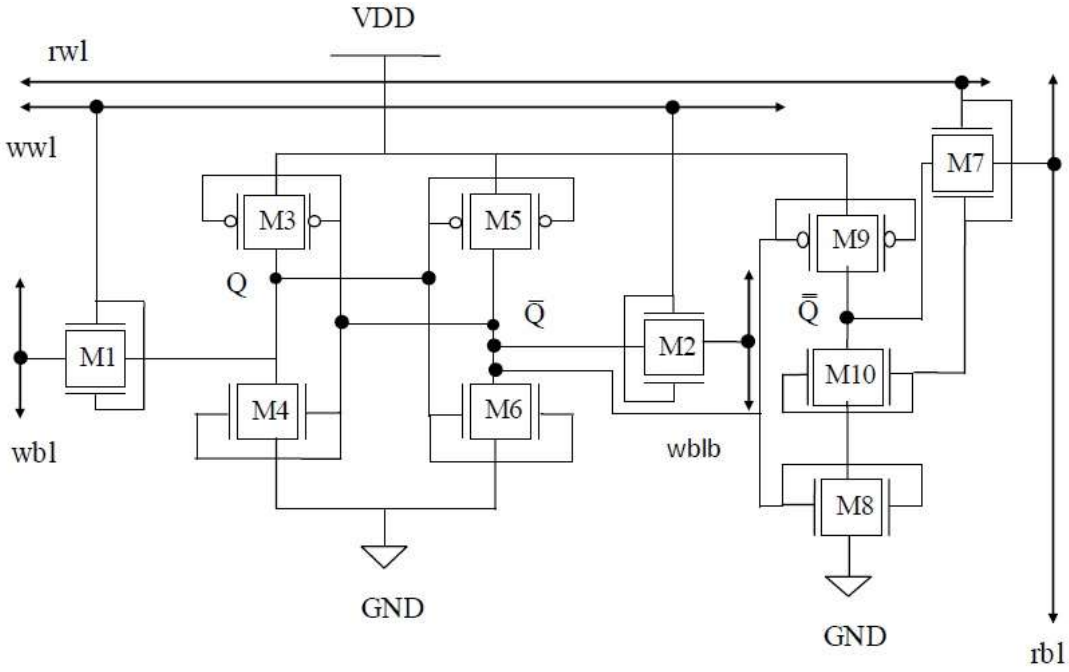

Figure 4.19: FinFET based 10T SRAM

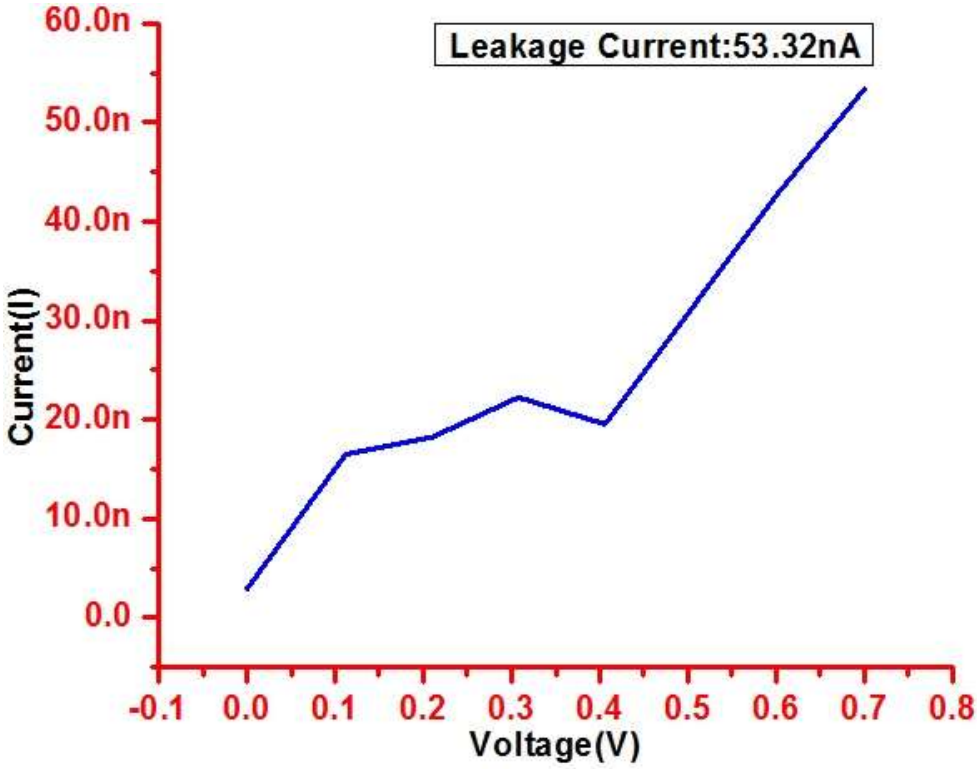

Figure 4.20: Leakage Current of 10T SRAM

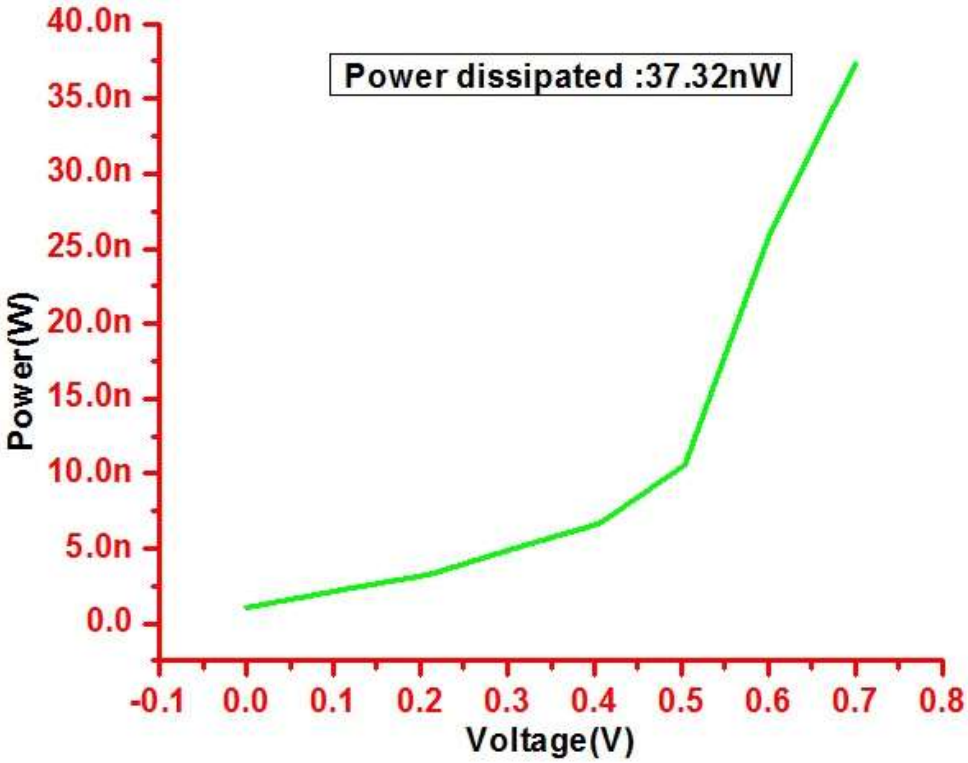

Figure 4.21: Power dissipated of 10T SRAM

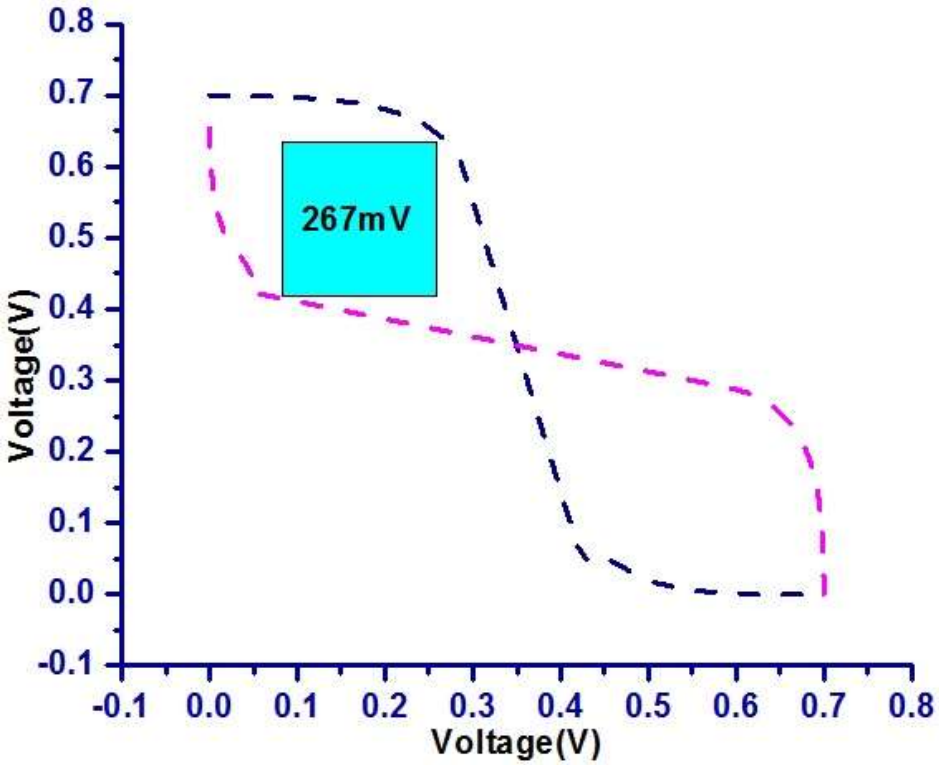

Figure 4.22: SNM of 10T SRAM

4.8 12T SRAM CELL DESIGN

A 12T based SRAM have a differential cross point data aware cut off having a write assists are discussed for operating it at low voltages [98]. A bit cell will internally cut off the VDD to either left cell or right cell by half and weakens the pull up circuit of bit-cell. In write operation subject to data in an assist to discharge of storage mode. This will improve writing ability by not adding any other components and write assist transistor, timing control and boosting circuit as shown in figure 4.23. And it illustrates the design of 12T based SRAM. It consists of transistors M3, M7, M4, M5, M8 and M6, and differential read operations and write operation transistors M9, M1, M11, M10, M2 and M12. Write Word-Line a (wwla), Bit-Line (wbl), Write Word- Line B (wwlb), and Bit-Line Bar (wblb) are column-based and Read Word-Line (rwl) and Virtual Ground (VGND) are row-based.

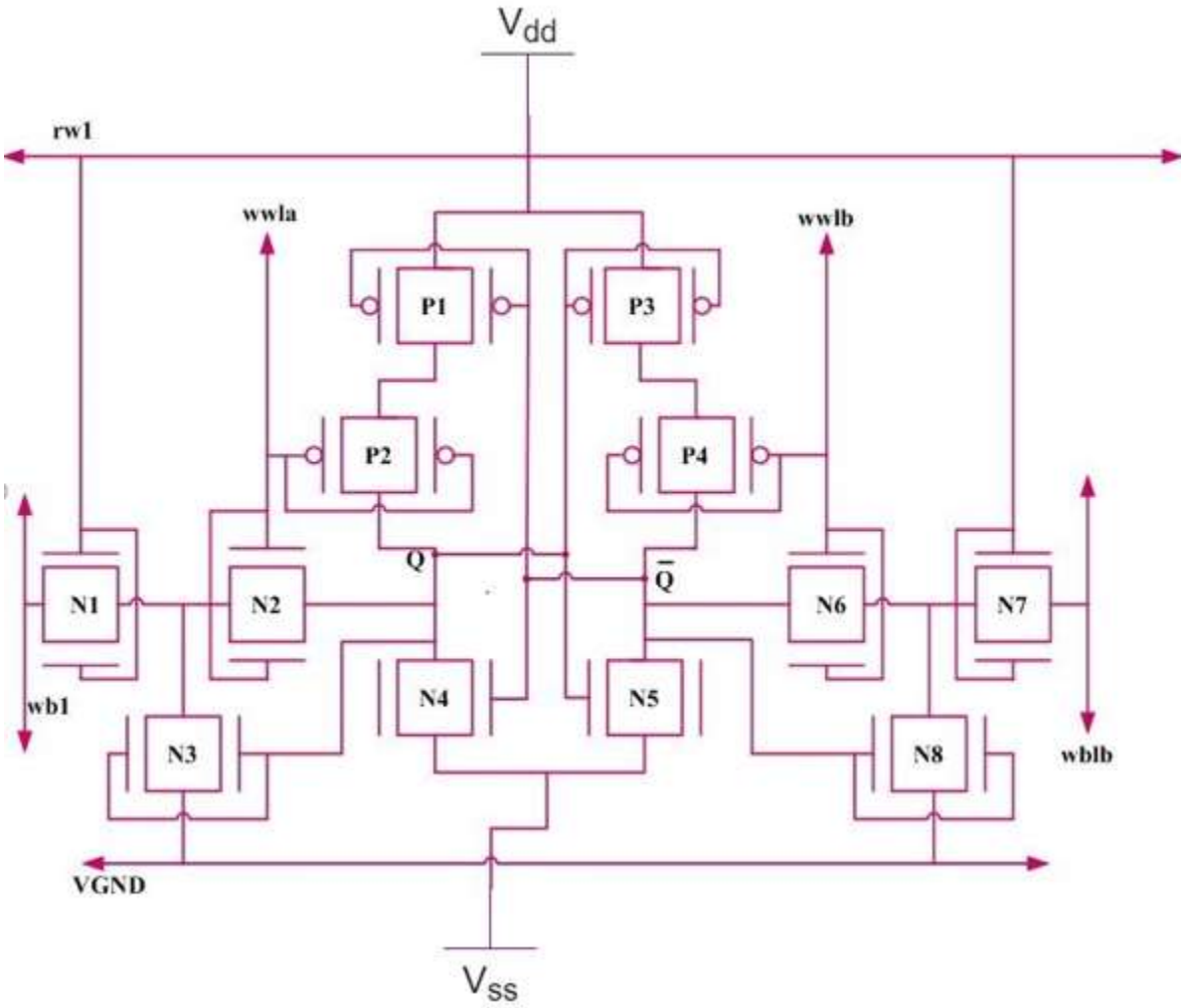

Figure 4.23: FinFET based 12 T SRAM

The leakage current and power dissipated for FinFET based 12T SRAM cell is shown in Figure 4.24 and Figure 4.25 respectively. The SNM is 232mV as shown in figure 4.26.

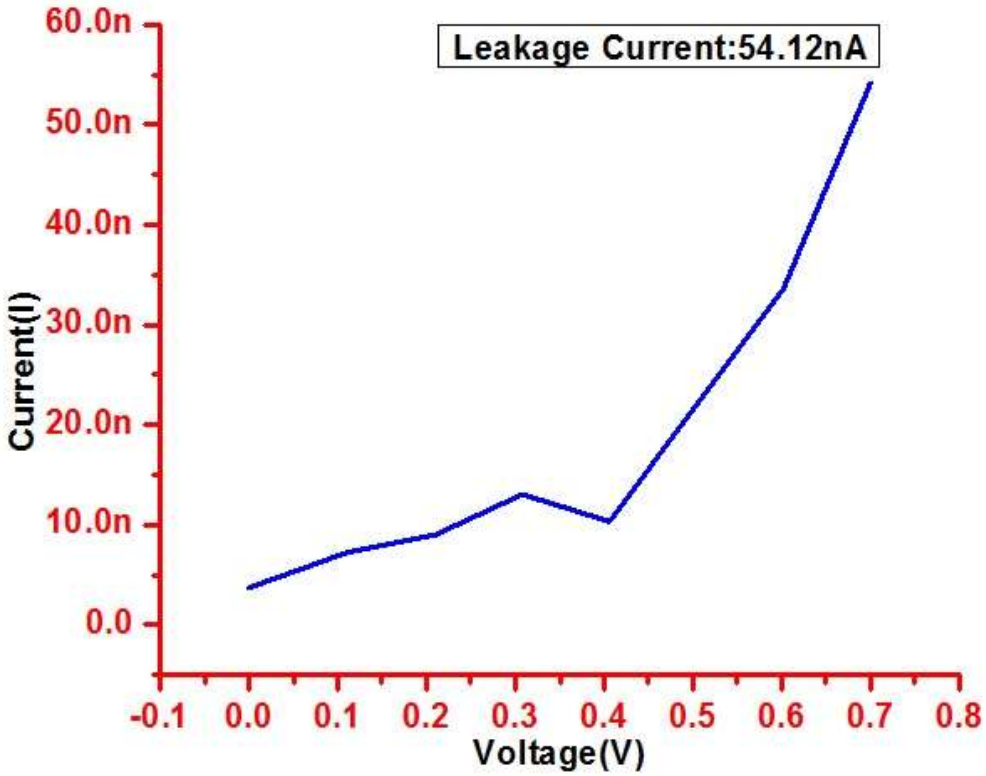

Figure 4.24: Leakage current of 12T SRAM

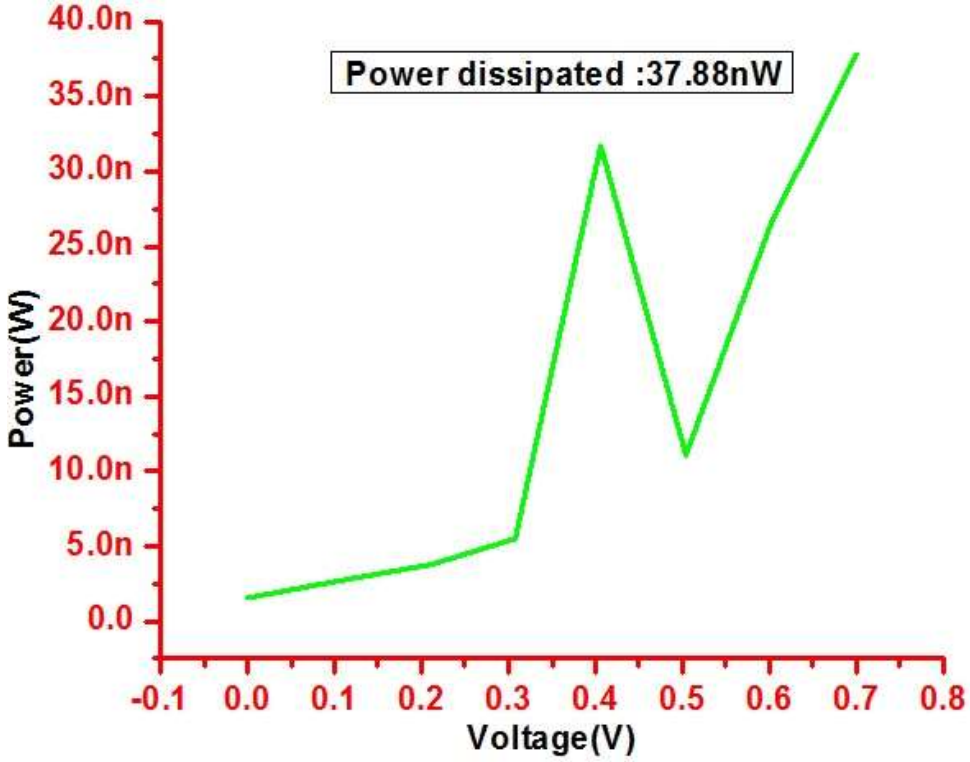

Figure 4.25: Power Dissipation of 12T SRAM

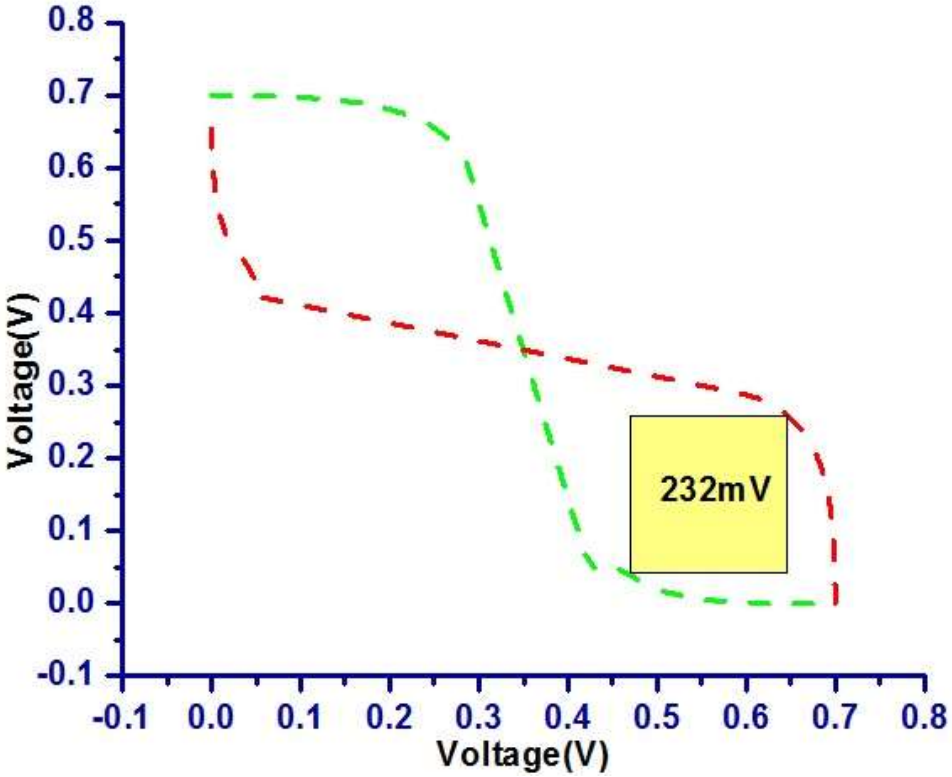

Figure 4.26: SNM of 12T SRAM

4.9 Analysis of FinFET Based SRAM Cell

The Leakage Currents and power dissipation for SRAM cells (6T, 7T, 8T, 9T, 10T, and 12T) are calculated and the power consumption of all these SRAM cells have been evaluated .It is done for both 45nm CMOS and 18 nm FINFET devices and it is found that the FinFET based SRAM has better presentation in terms of Power and better stability in terms of SNM ratios. It is also found that the proposed 7T SRAM cell has better performance in terms of both Power handling capability and SNM as it has only one transistor more than the conventional SRAM it is also better in terms of area.

Table 4.1: Performance Comparison of CMOS and FinFET based SRAMs

SRAM	45nm CMOS			18nm FinFET		
	Leakage Current (nA)	Power Dissipation (µW)	Power Consumption (nW)	Leakage Current (nA)	Power Dissipation (nW)	Power Consumption (nW)
6T	61	15.4	22	51.3	35.91	16.23
7T	59.7	12.8	20	50.26	35.22	12.71
8T	62.9	22.3	25	52.63	36.84	13.13
9T	64.9	34.6	28	52.87	37.1	13.87
10T	65.4	42.7	30	53.32	37.32	14.26
12T	67.6	51.3	33	54.12	37.88	14.63

4.10 Conclusion of Chapter

In this chapter SRAM is designed by using 18nm FinFET technology ,and the SRAM is designed in 6T , 7T ,8T ,9T ,10T ,12T topologies and leakage current is 51.31nA , 50.26nA , 52.63nA , 52.87nA , 53.32nA , 54.12nA respectively and the power dissipation is 35.91nW, 35.22nW, 36.84nW, 37.1nW, 37.32nW, 37.88nW respectively. Its performance is compared with that of the same topologies designed in 45nm CMOS technology. The leakage currents and power consumption and dissipation of these SRAM cells are compared. It is found that the 7T SRAM has better performance than other SRAM because of the proposed design in which the power consumption is reduced by 40% because of the reduced switching activity employed in the design.

CHAPTER 5
LEAKAGE CURRENTS AND ITS REDUCTION TECHNIQUES

5.1 Introduction

In today's world one of the mostly used digital electronic component is semiconductor memories. Where it has built in memory that offers accessing of data on ease from any memory location in random manner. When semiconductor memories are compared with other memories it will have fast access time and for reading or writing the data it need few nanoseconds. CMOS provides unavailable task for length of the channel beyond 65nm. [139]

SRAM based cells (6T, 7T, 8T, 9T, 10T, 12T) having different structures are compared based on power dissipated and speed. A 7T based SRAM which is stable and having two ports is designed at 90nm technology for ultra-low power operations at dynamic noise margin for read (7X). For 20nm submission technology designers are much concerned about stability and consumption of power. MOSFET devices like FinFET has greater potential of overcoming the limitations like controlling the gate terminal over the channel region and providing a reduced effect on drain. CMOS technology is completely replaced by FinFET technology and SRAM based devices designed on it have a large channel flexibility and has more control of gate terminal over the channel. [140].

When MOSFET is compared with FINFET it has less leakage current. Therefore, a FinFET circuit which has smart and efficient memories incorporated in it for exploring future applications. [141]. Here for FinFET devices there will be low SCE and has low leakage power and current are easily scalable. As technology is scaling down further, there is reduced in supply voltage and dynamic power is sustained. Moreover, scaling of components will result in increase of power consumption because of leakage current.

In integrated circuits the power dissipated is high and has a greater significant during the scaling of technology. For portable devices the power dissipation will degrades the lifetime of battery. Moreover, increase in power dissipation will limit the scaling the technology continuously and its high power density. In present chapter, consumption of power is modelled and identified. Various methods are implemented for leakage reduction of 7T based SRAM as discussed in sec5.2. Techniques are designed for reducing the leakage current produced by subthreshold is discussed below in section 5.3. Here a proposed method is implemented on advanced SRAM cell is presented

in section 5.4., simulation result and the novelty of the proposed technique are discussed and presented in section 5.5 and 5.6 respectively. Chapter conclusion in session 5.7.

5.2 Leakage Reduction Techniques for 7T SRAM Cell

High performance circuits design paths are prevented by high power dissipation. A battery supplies an amount of energy and circuit designers require minimizing the power dissipation [142].In 7T based SRAM cell a single bit line will have low power consumption because of its functionality when it is compared with a 6T based SRAM and few other SRAMs. Still the power consumption can be further decreased by decreasing the leakage currents.Inorder to reduce the leakage currents many techniques have been proposed like

- Multi-threshold CMOS (MTCMOS) Technique
- Adaptive Voltage Level Technique (AVL)
- Drowsy-Cache Technique
- Proposed Self-Controllable Voltage Level Technique (SVL)

5.2.1 Multi-threshold CMOS (MTCMOS) Technique

In CMOS based chip technology its variation represents the multi threshold that consists of transistors with dual threshold voltage (Vth) for optimizing the power and delay. In MOSFET transistor multiple threshold voltage is the voltage at the gate terminal at which these formation of inversion layer at an interface between body and oxide layer. Hence devices with lower threshold voltage will switch fast and also minimize clock periods on critical delay paths. The drawback of lower threshold voltage device is that it has a high leakage power. Therefore in order to overcome this limitation of leakage a higher threshold voltage device are used that has a less static power. Typically by using higher threshold voltage device static leakage is reduced 10 times when compared to lower threshold voltage devices. [143].

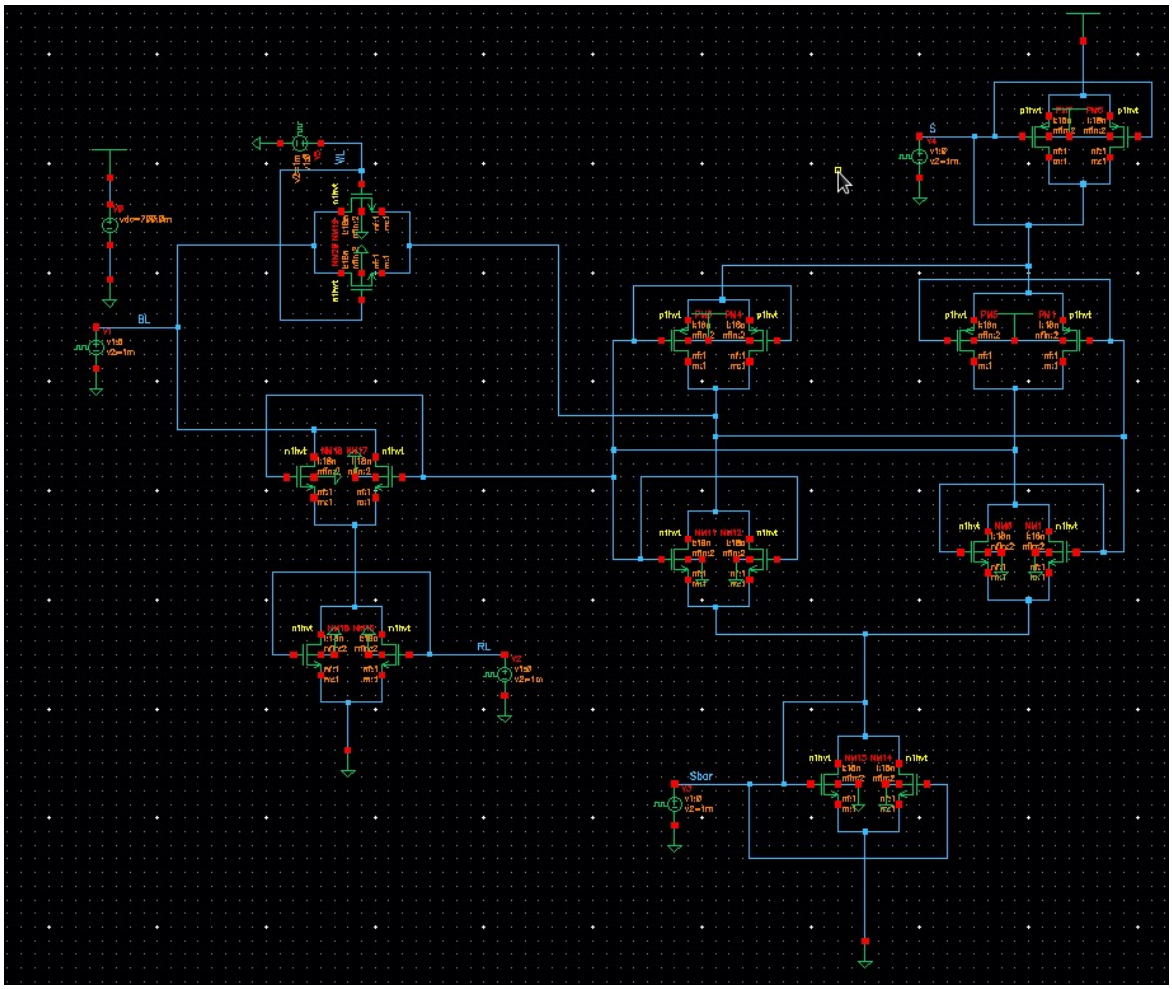

Figure 5.1(a): 7T SRAM with MTCMOS Technique Cadence tool View

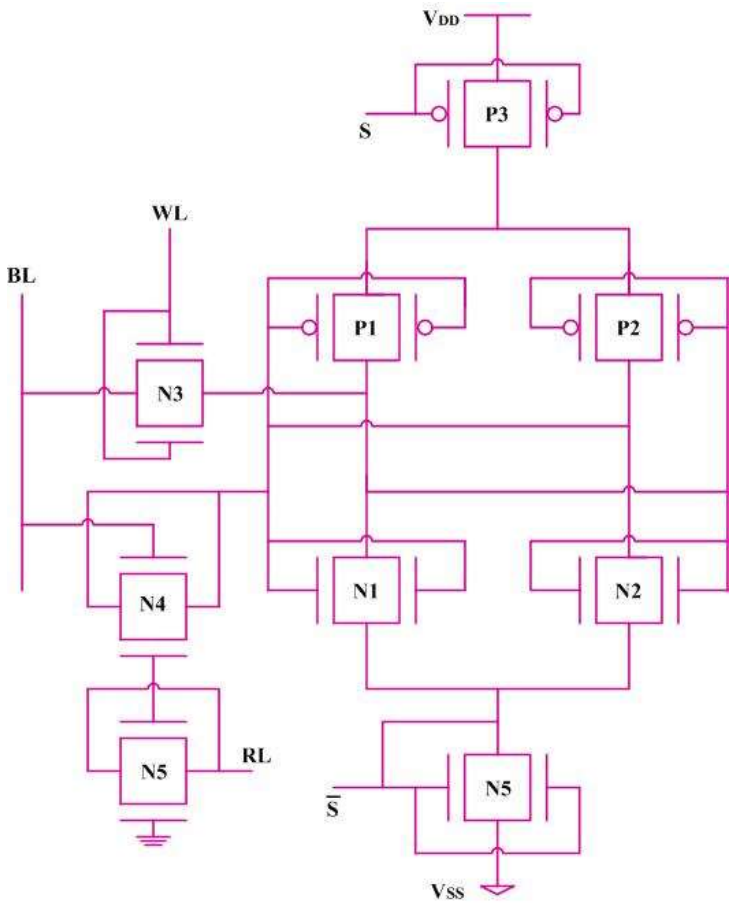

Figure 5.1(b): 7T SRAM with MTCMOS Technique

In multi threshold CMOS technique, lower threshold voltage transistors are separated from supply by sleep transistor having a higher threshold voltage that is present at top and bottom of the circuit. Figure 5.1. Illustrates transistor that has lower threshold voltage used for logic design. The sleep signal controls a sleep transistor. When transistor is in active mode, a sleep signal will be distorted and results in switching ON the higher threshold voltage transistor and will supply power virtually and GND to the lower threshold voltage. When designed circuit becomes inactive, a step signal will be asserted and force the transistor having the higher threshold voltage to move in cutoff region that will disconnect its power to lower threshold voltage. It causes a lower current at threshold region from power towards the GND. During standby mode, the waveforms of power dissipated and leakage current of 7T based SRAM is implemented by using multiple threshold CMOS techniques that are displayed in below figure 5.2 and figure 5.3 respectively. The waveform clearly represents remarkable leakage current reduction by 75.9% and reduction in power by 70.1% as compared to normal FinFET model 7T based SRAM. Here a major limitation of multiple threshold CMOS circuit is sizing and portioning of sleep transistor in large circuits.

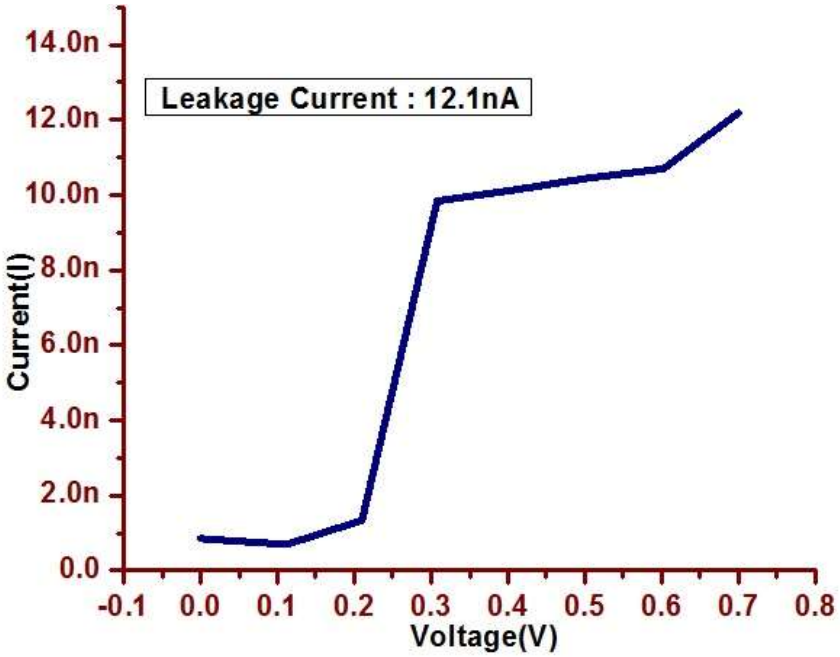

Figure 5.2: Leakage Current in 7T SRAM with MTCMOS technique

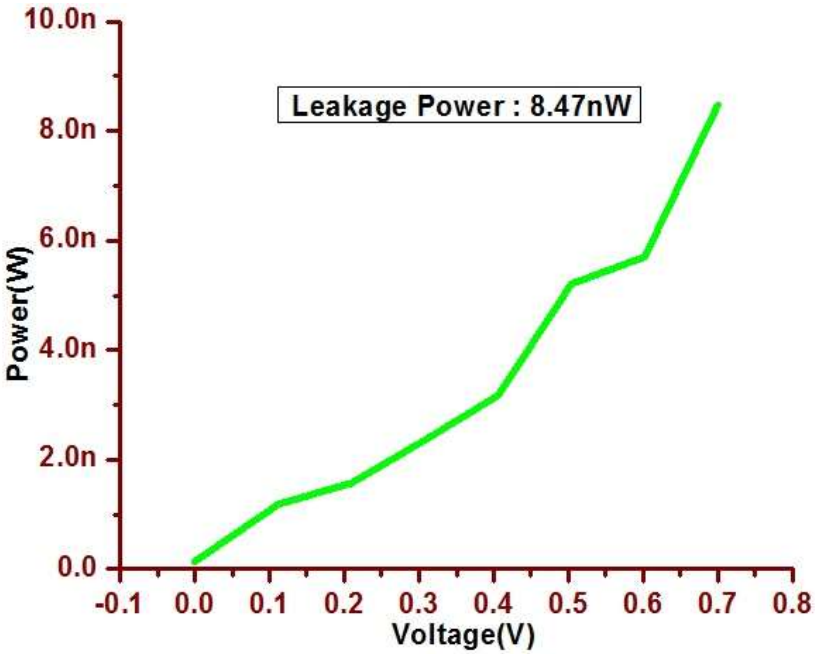

Figure 5.3: Leakage Power in 7T SRAM with MTCMOS technique

5.2.2 Adaptive Voltage Level Technique (AVL)

Adaptive Voltage Level based technique is another approach for minimizing a leakage current and leakage power on a shorted gate DG FinFET SRAM cell. As seen in figure 5.4, an approach is to combine technique of adaptive voltage level scaling done at supply voltage for reducing the supply

provided to circuit in static mode and Adaptive voltage level scaling done at ground when circuit is at inactive mode. [144] by reduction in power supply and increase in ground potential a reduction in leakage power is achieved. In AVLS, during active mode, we apply a full voltage supply i.e., VDD to SRAM cell. Whereas, during inactive mode, we apply a reduced amount of supply voltage. It results leakage current reduction by the access transistors and it make bit lines to float. In AVLG, increased voltage is provided during the standby mode while, in the active mode, a 0V is provided at the GND mode. [145].

Here above scheme is like to diode cache design that is used to control the SRAM leakages, and here the design has diode that has a higher threshold transistor for increasing the ground level to standby mode [144]. Waveforms of leakage current and leakage power of FinFET model for 6T based SRAM is employed by AVL technique and shown below in figure 5.5 and Figure.5.6. The waveform clearly represents significant reduction in leakage current by 77.5% and leakage power by 72.81% when compare to normal FinFET based 6T SRAM cell.

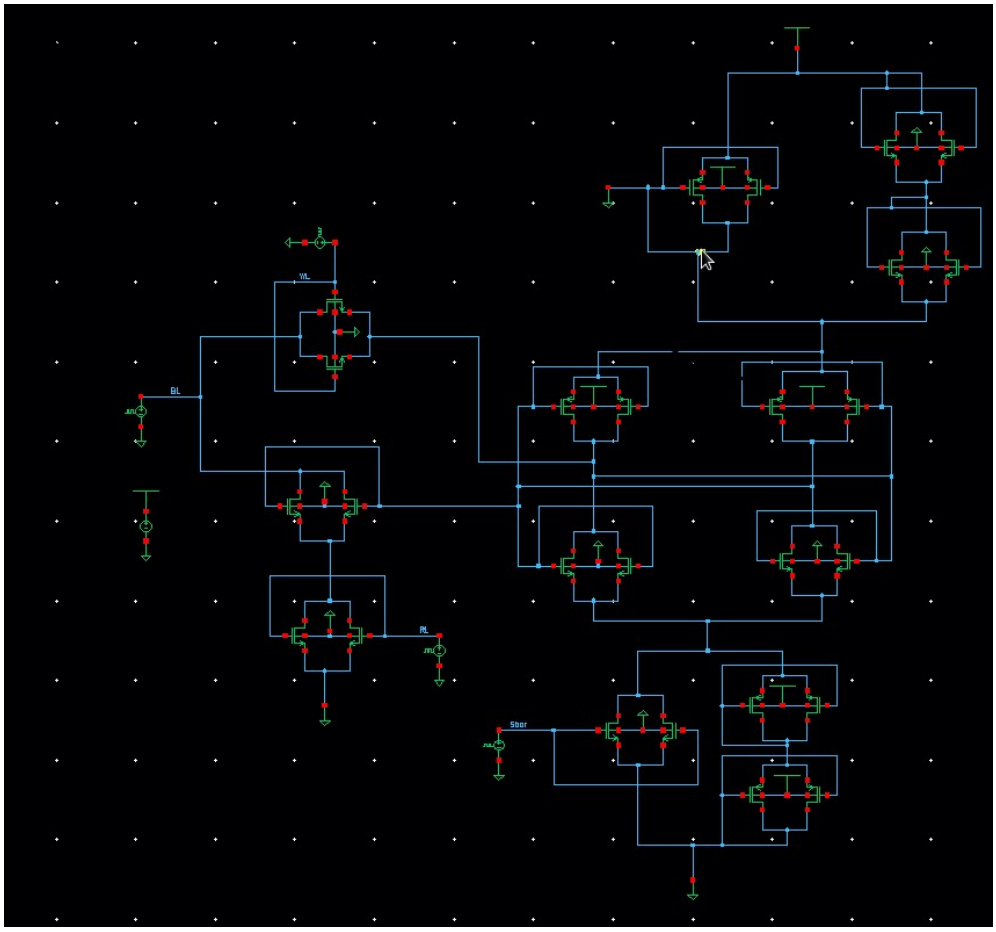

Figure 5.4(a): 7T SRAM with AVL technique in cadence View

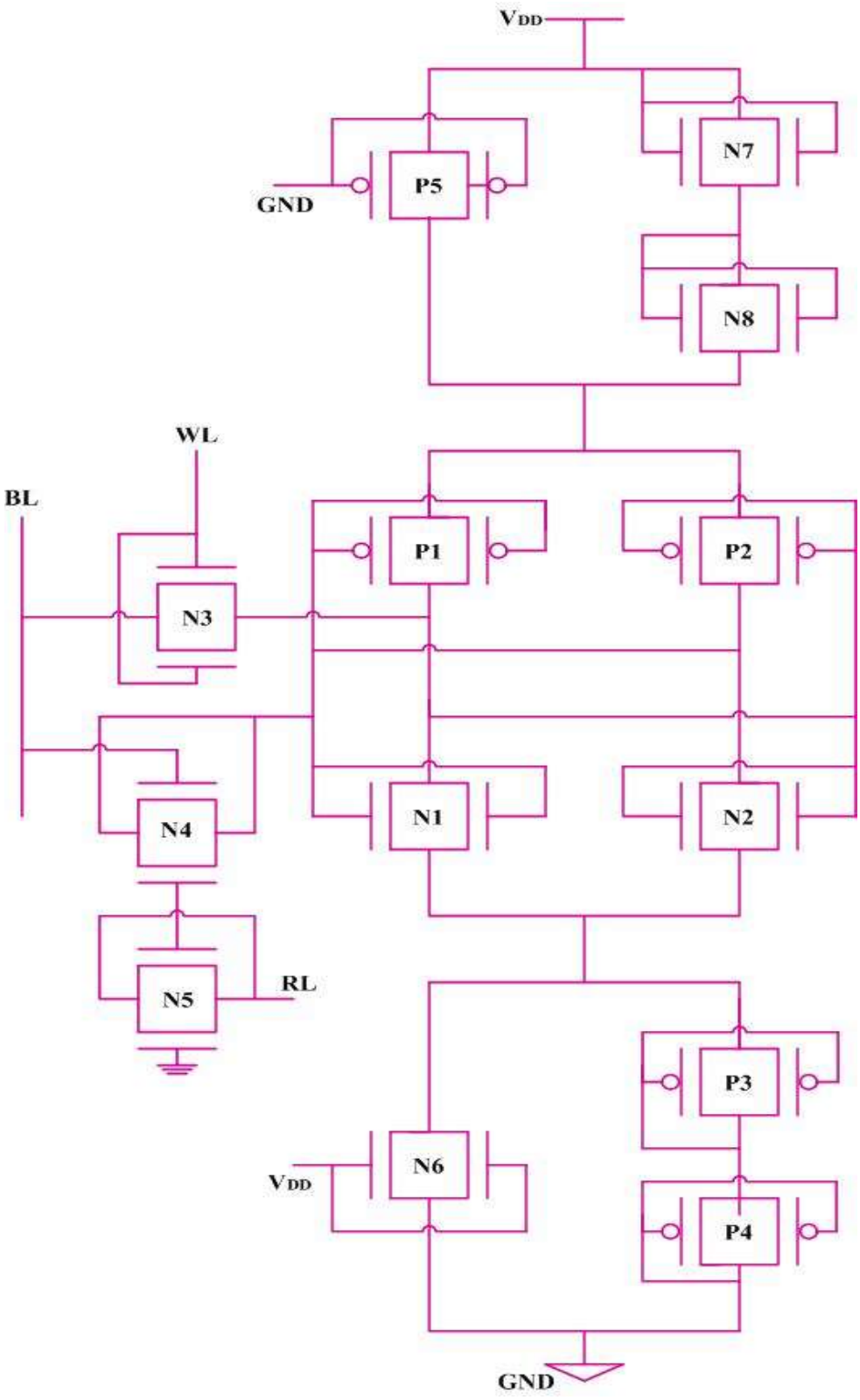

Figure 5.4(b): 7T SRAM with AVL technique

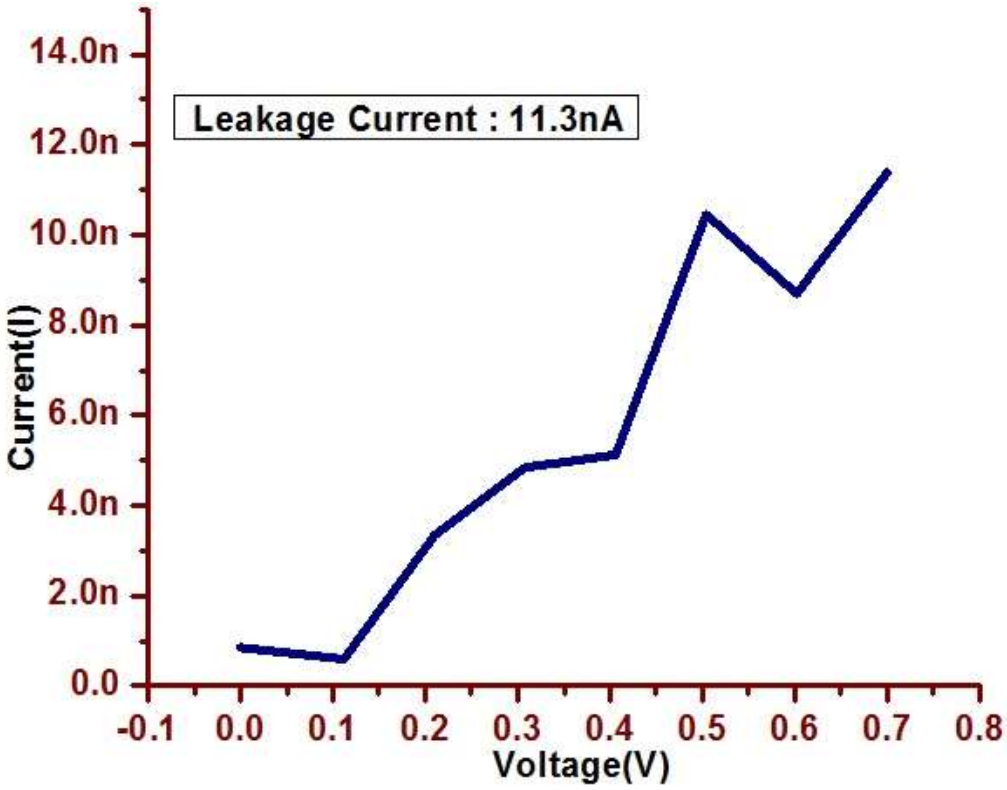

Figure 5.5: Leakage Current in 7T SRAM using AVL Technique

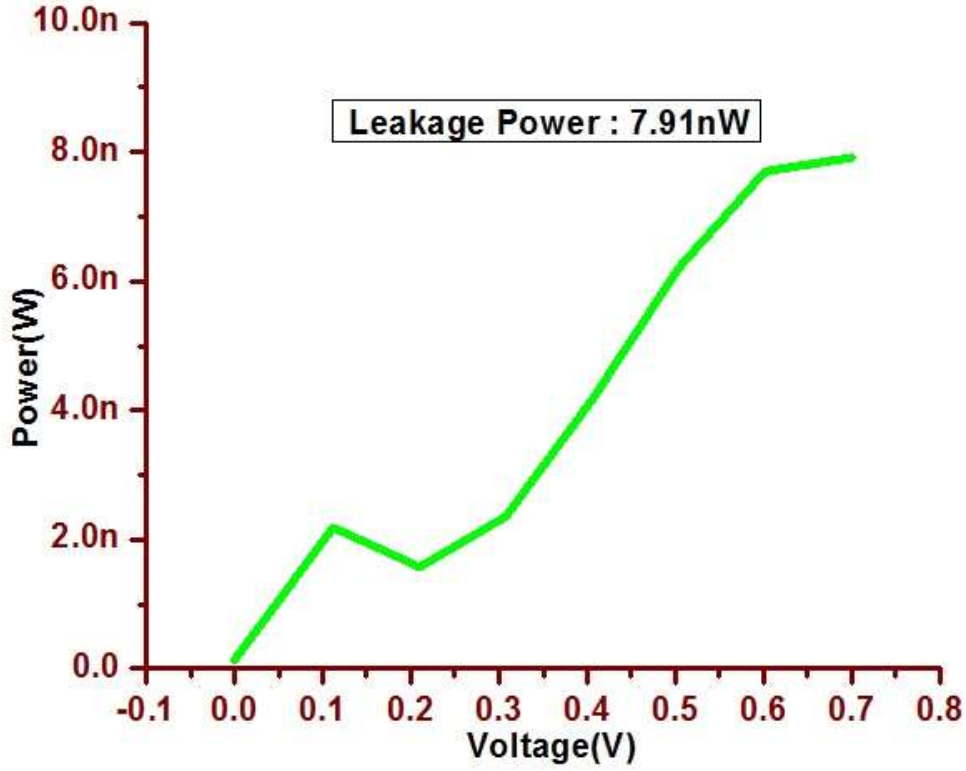

Figure 5.6: Leakage Power of 7T SRAM using AVL technique

5.2.3 Drowsy-Cache Technique

In this method we apply a lower supply voltage to SRAM cell during hold operation. For present memory we use dual supply voltages. When transistor is in active mode we apply a higher supply voltage for read/write operations. Since by decreasing VDD there will be decrease in leakage current, and lower VDD will be used. In case of standby mode and higher supply voltage for reducing the SRAM leakage [146]. Hence simultaneous reduction of leakages will decrease the leakage power quadratically and there will be improvement in performance of designed circuit. Waveform of leakage current implemented by DCT is shown below in figure.5.7 and in similar way waveform of leaking power, Leakage Current are represented in figure5.8 and figure5.9. The waveform clearly represent significant reduction in leakage power by 81.3% and leakage current by 82.6% compare to normal FinFET based 7T SRAM cell.

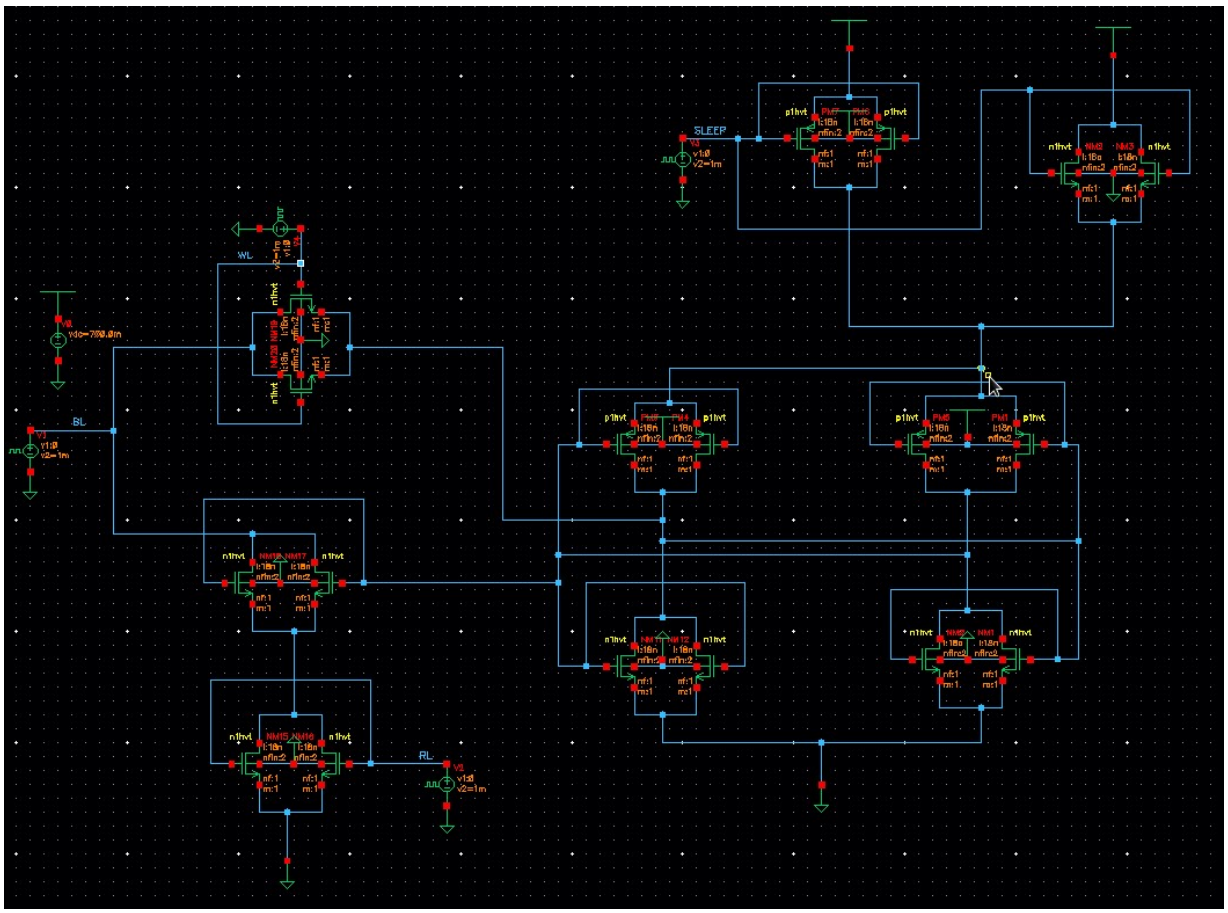

Figure 5.7(a): 7T SRAM in Drowsy-Cache Technique Cadence View

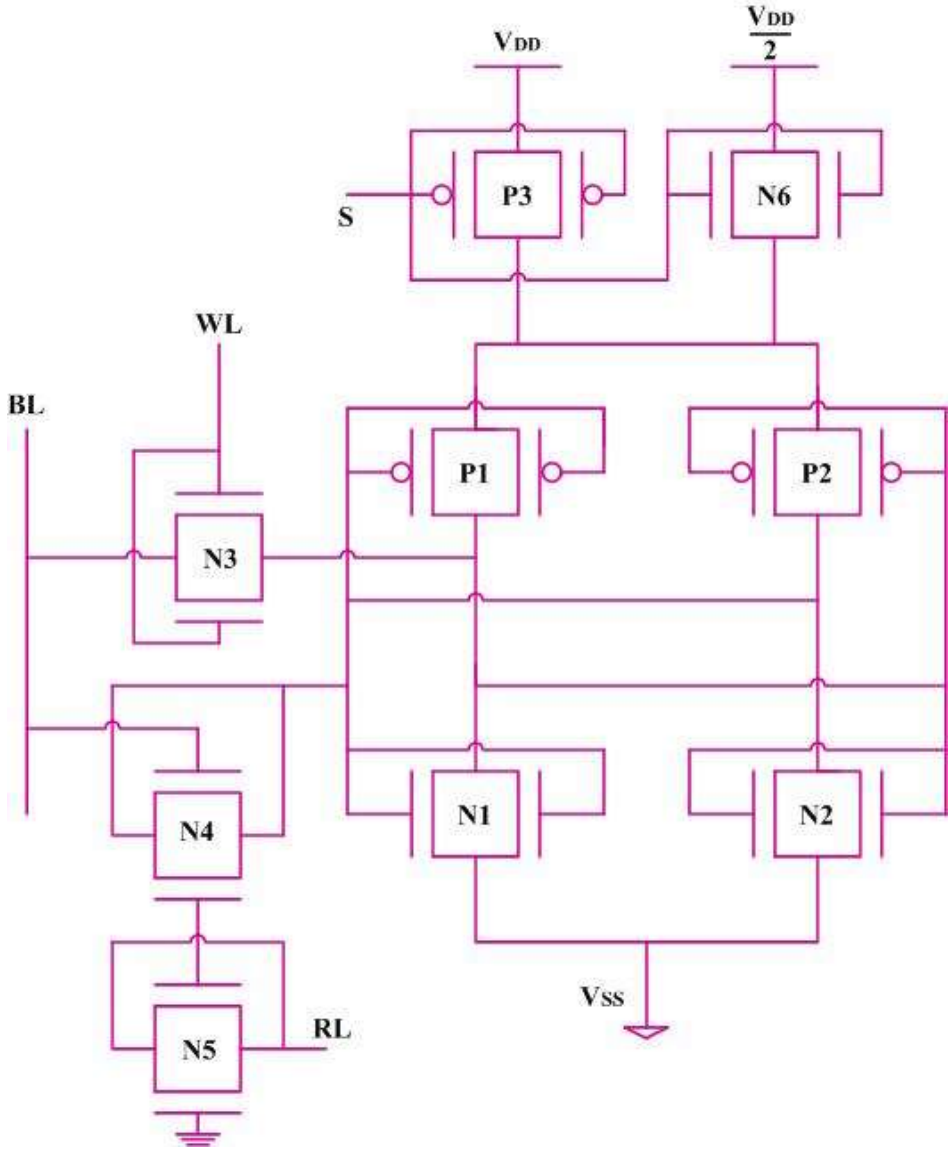

Figure 5.7(b): 7T SRAM in Drowsy-Cache Technique

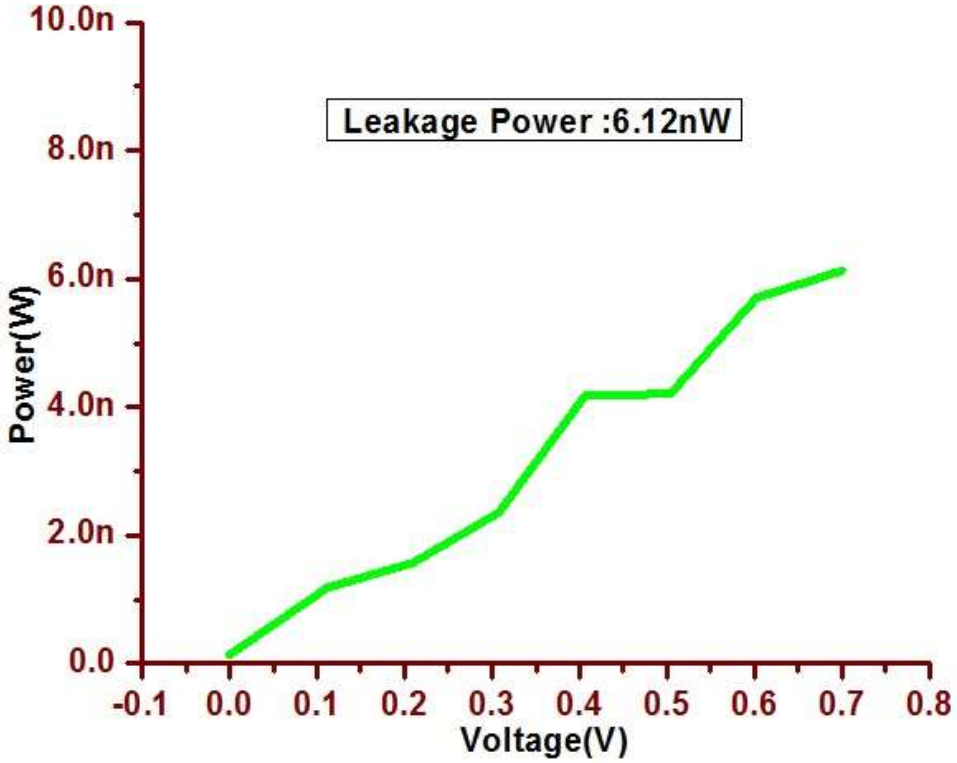

Figure 5.8: Leakage Power of 7T SRAM in Drowsy cache Technique

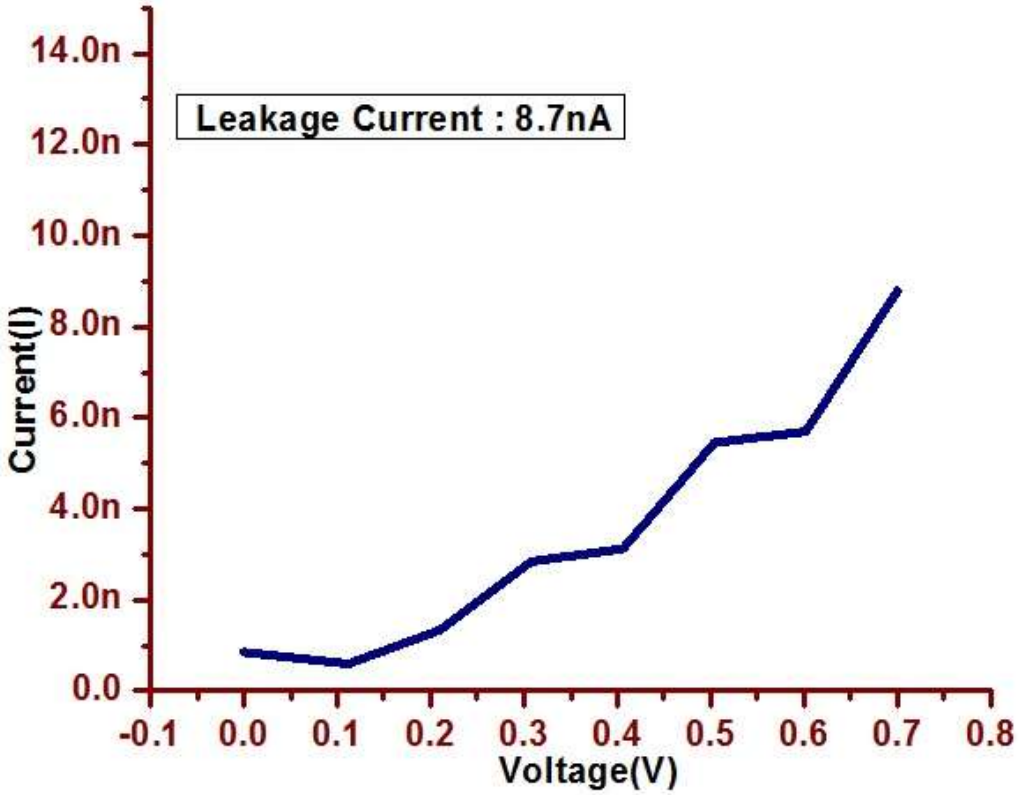

Figure 5.9: Leakage Current of 7T SRAM in Drowsy cache Technique

5.2.4 Proposed Self-Controllable Voltage Level Technique (SVL)

Various approaches are used for reducing the power and to maintain the device performance at speed. A SVL design circuit is used for decreasing the power and for improving the device performance. Here we generate a minimum or maximum voltage supply, and minimum or maximum ground voltage for increasing the speed of operation. When there is a switching among standby mode and active mode here the circuit has three levels of design such as lower SVL, upper SVL and a combination of both lower and upper SVL.

5.2.4.1 Lower self-controllable voltage level (LSVL):

Here LSVL design consist of single n-channel FinFET and dual p-channel FinFET arranged in proper configuration among a GND level and VSS level. A model of FinFET structures with 7T based SRAM cell is shown in below figure 5.10. The present circuit will supply the voltage VSS to design circuit by transistor M8 and moreover the supply voltage is provided to 7T based SRAM by using transistor P3, P4. In LSVL circuit low voltage is connected to CSB of 7T based SRAM and transistor P4 is ON and transistor N6 is OFF. So that the supply voltage is connected to 7T based SRAM. In Dynamic mode, a low voltage is given by CSB at GND level and in idle mode it is increased to virtual ground. Whereas the above technique is same as DFS structure proposed for leakages at sub-edge and controlling the signals in FinFET model of 7T based SRAM [147]. Hence this method will decrease the flow of leakage current by transistor N1, P2 and N4. The design outcome is expressed by reduction of subthreshold current. The leakage current is 27.6nA and leakage power is 19.32nW which is shown in Figure 5.11 and figure 5.12.

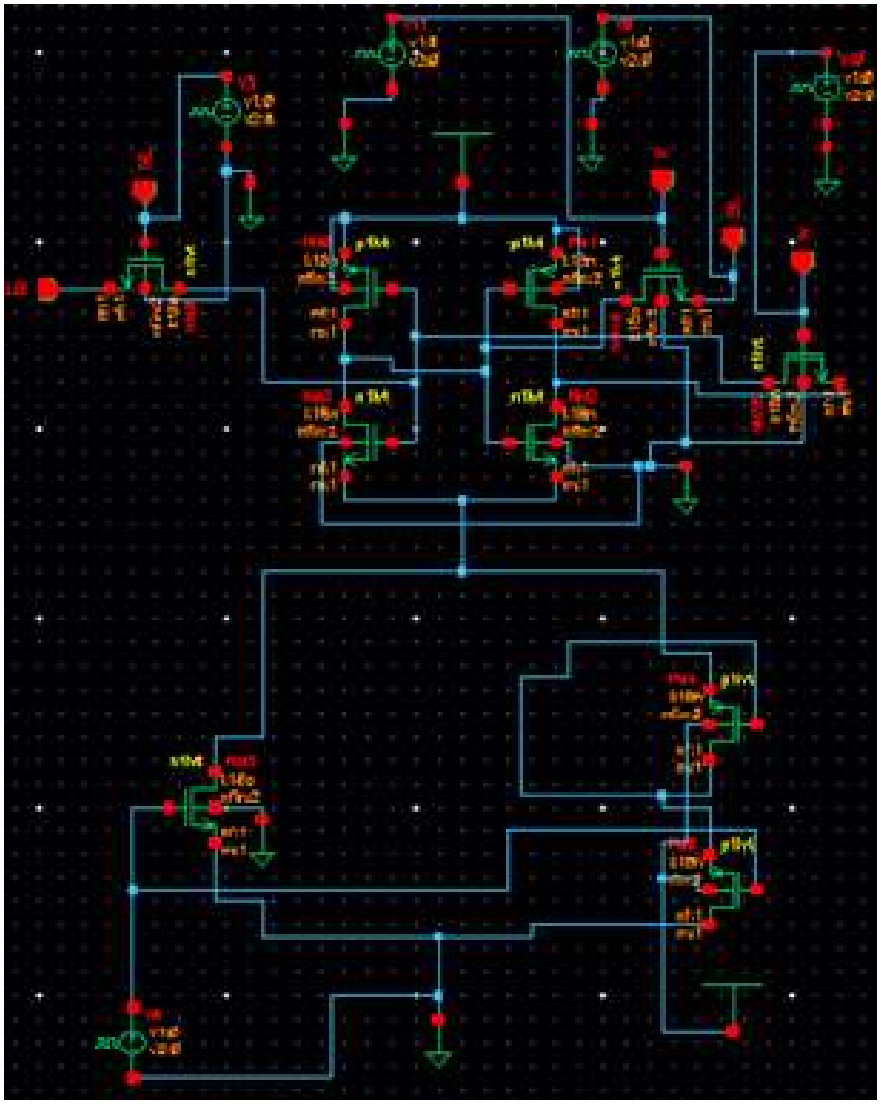

Figure 5.10(a): 7T SRAM with LSVL technique in Cadence view

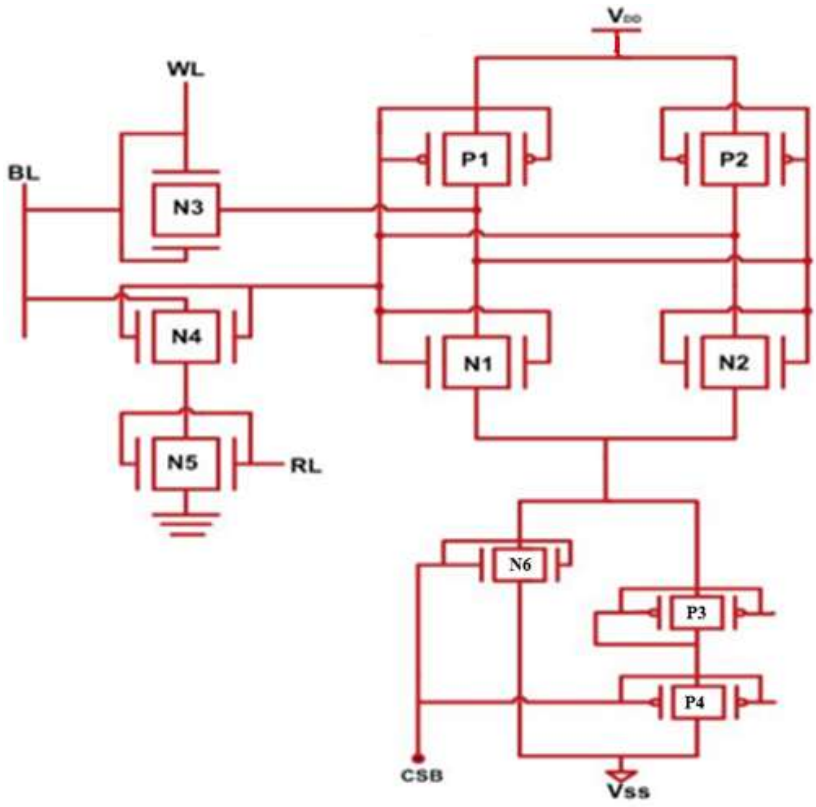

Figure 5.10(b): 7T SRAM with LSVL technique

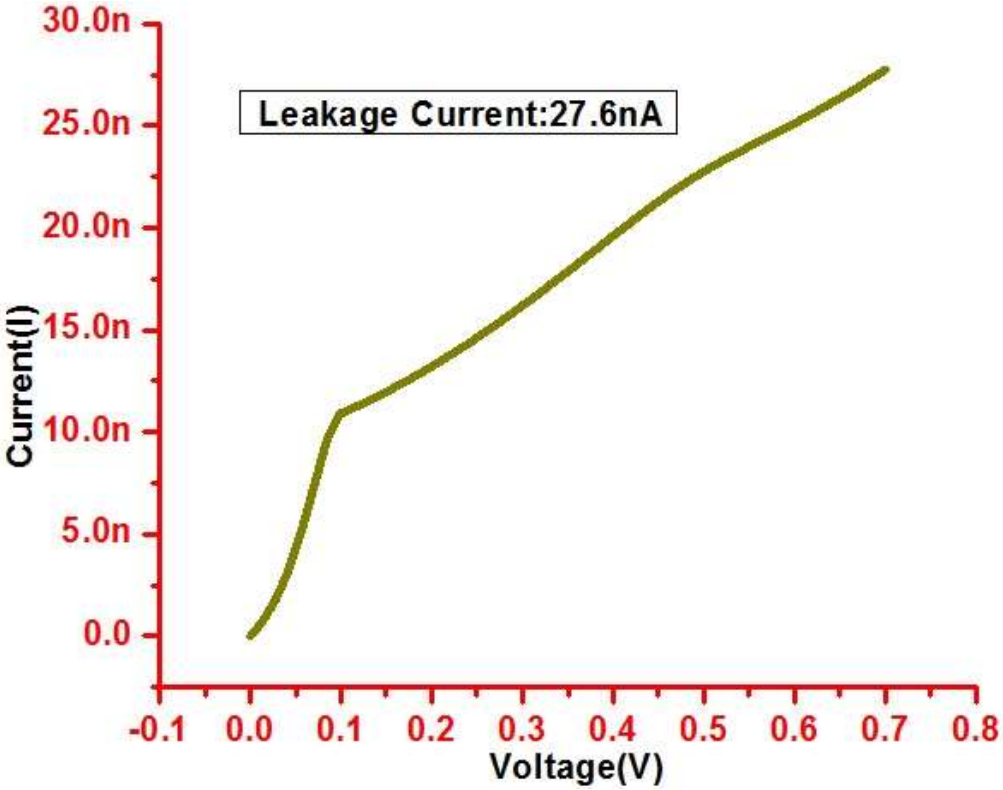

Figure 5.11: Leakage Current in 7T SRAM using LSVL technique

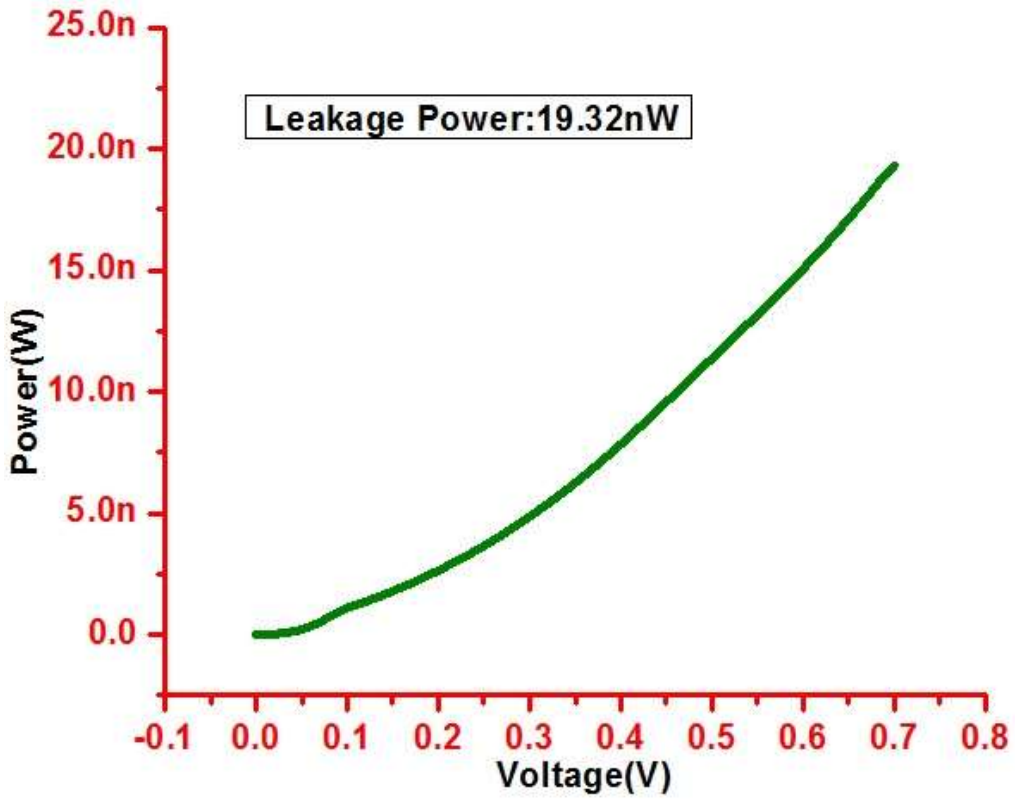

Figure 5.12: Leakage Power in 7T SRAM using LSVL technique

5.2.4.2 Upper self-controllable voltage level (USVL)

A USVL design consists of one p-channel and dual n-channel FinFET transistor arranged in systematic fashion as shown in below figure5.13. Here p-channel ON transistor get associate with VDD at dynamic mode of operation, and during sleep mode a n-channel will be ON. Here in this design a full VDD is connected to 7T cell during dynamic mode, while VDD level is reduced to Vd during sleep mode. At first, we check the leakage current impact. Based on simulation, N2 transistor gate voltage is decreased and there is a reduction in leakage current produced at gate terminal. At N1 transistor a low gate voltage appears because of the reduction in channel voltage than the leakage current at gate. Whereas the N4 transistor leakage current at gate remains unchanged. P5 transistor of p-channel will not have a large leakage current that utilizes USVL design. The present method is best method for leakage reduction. By using N1 and P2 transistor the sub-edge leakage current is decreased and it is unaltered over transistor N4. In order to outline the USVL consequences, the dual gate leakages produced by N4, N5 access transistor remains unchanged and current design is more effective for decreasing the leakage current at gate. The leakage current and power generated by the circuit are shown in Figure 5.14 and 5.15 respectively.

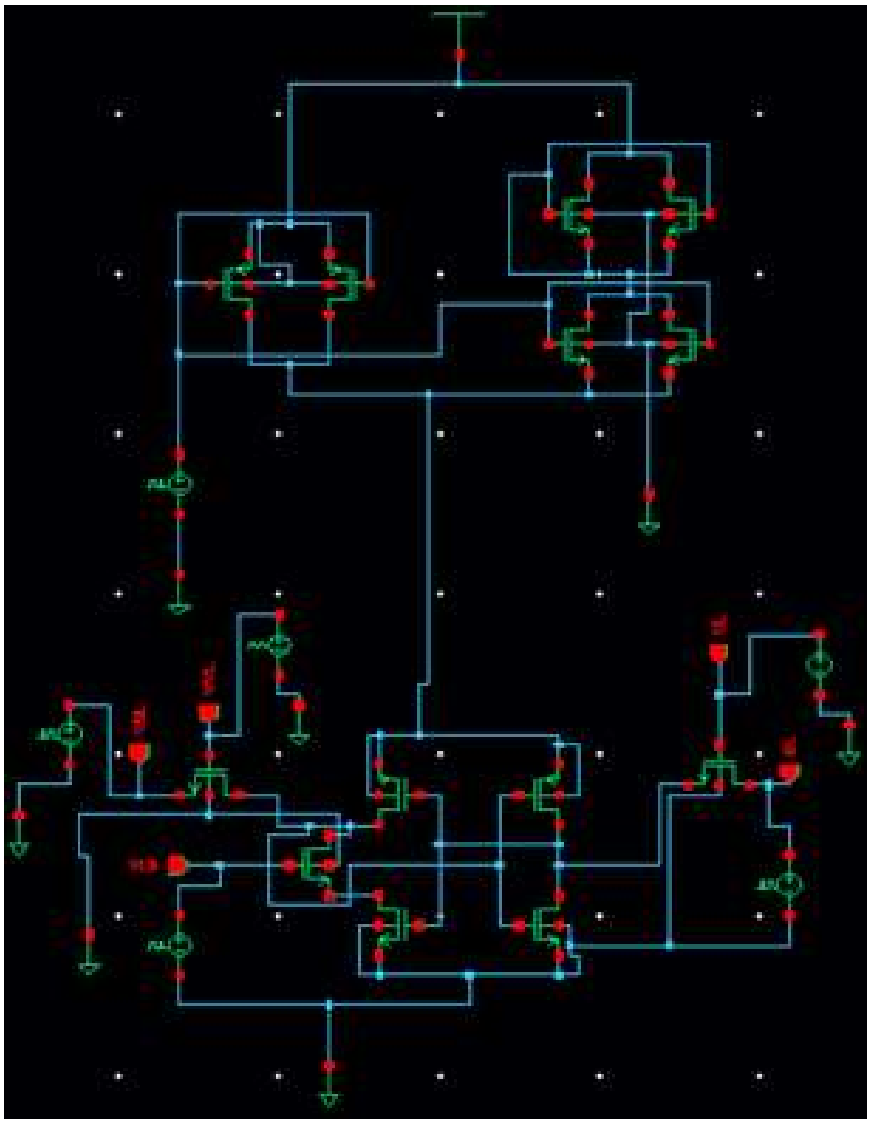

Figure 5.13(a): 7T SRAM with USVL Technique in cadence

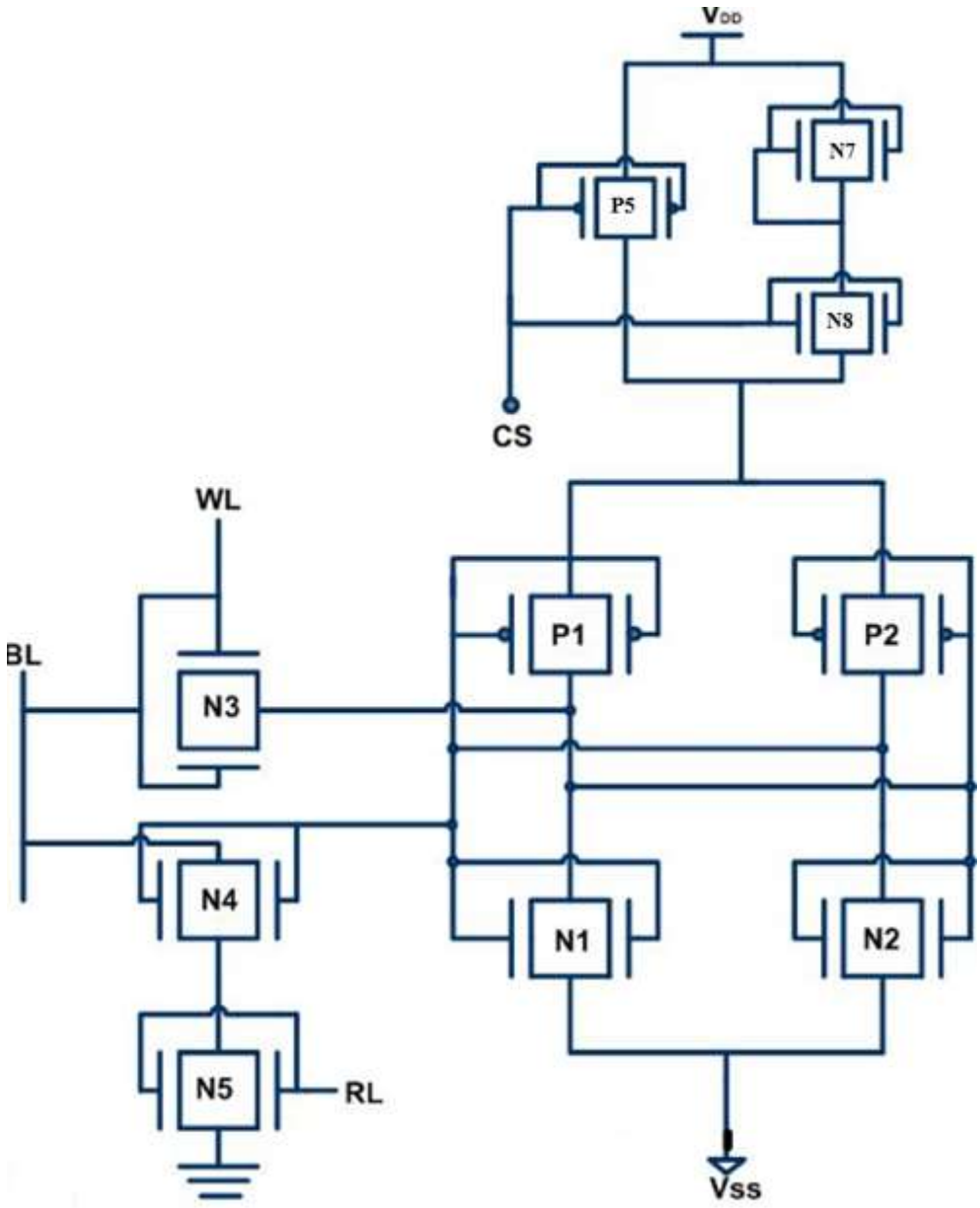

Figure 5.13(b): 7T SRAM with USVL Technique

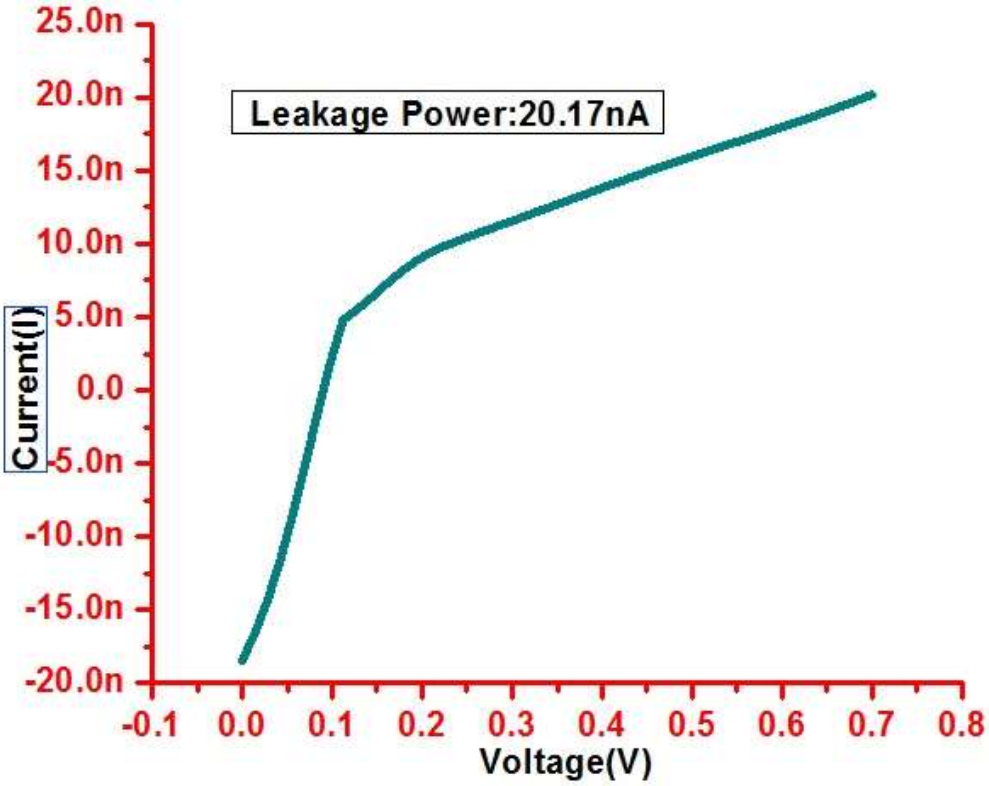

Figure 5.14: Leakage Current in 7T SRAM with USVL technique

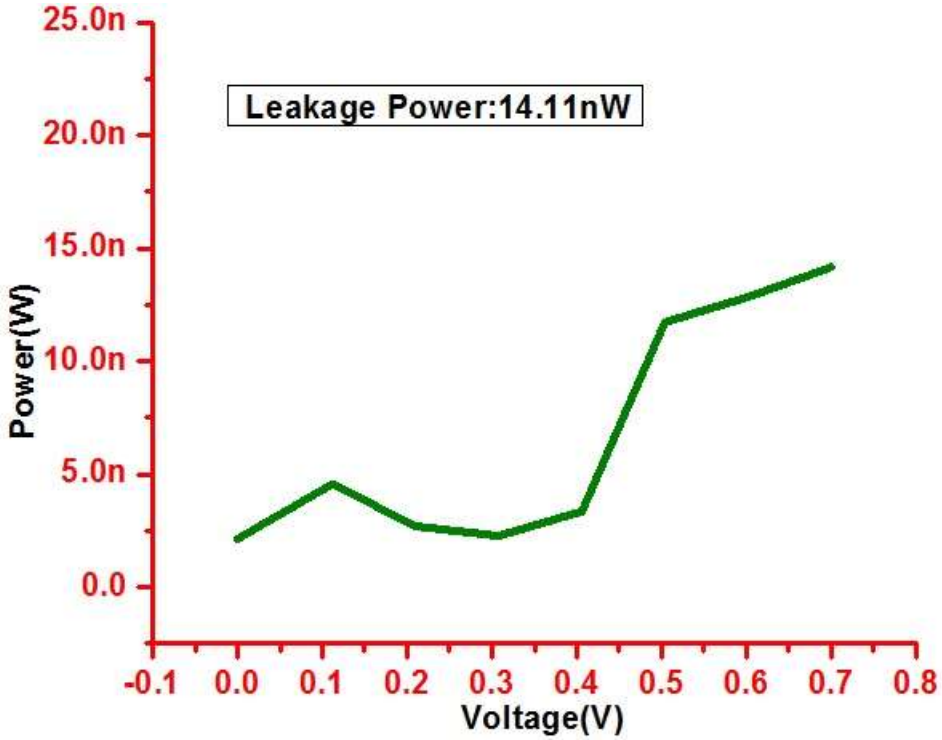

Figure 5.15: Leakage Power in 7T SRAM with USVL technique

5.2.4.3 Combined USVL and LSVL

The present method employs a combination of both single USVL and LSVL designs as shown in Figure5.16. As the current design will decrease the leakage power and current too much significant value. A schematic model of FinFET 7T based SRAM is shown below that utilize both individual design. In present method both technologies are used for 7T SRAM design based on FinFET. By using this method VDD is decreased to 0.35 V and at GND increased by 0.25V.Since applying both the methods combined the leakage current is reduced by 84.9% and leakage power is reduced by 87.3% which are shown in figures 5.17 and 5.18.

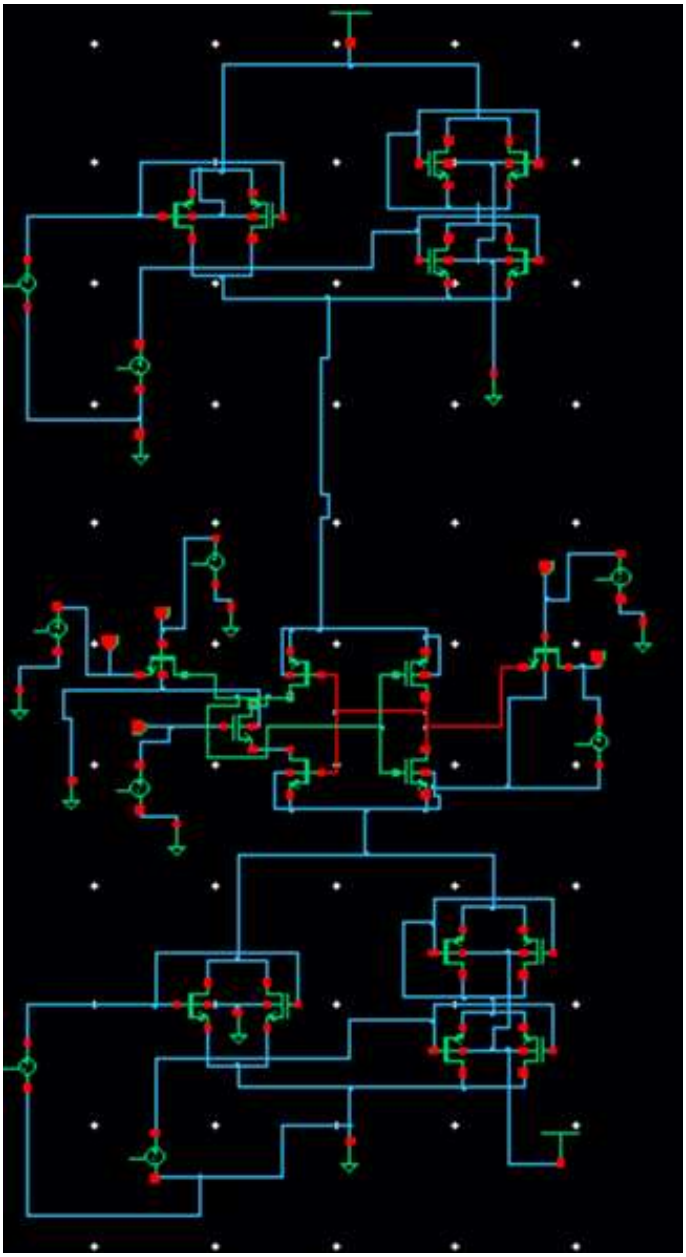

Figure 5.16(a): 7T SRAM with SVL Technique in Cadence view

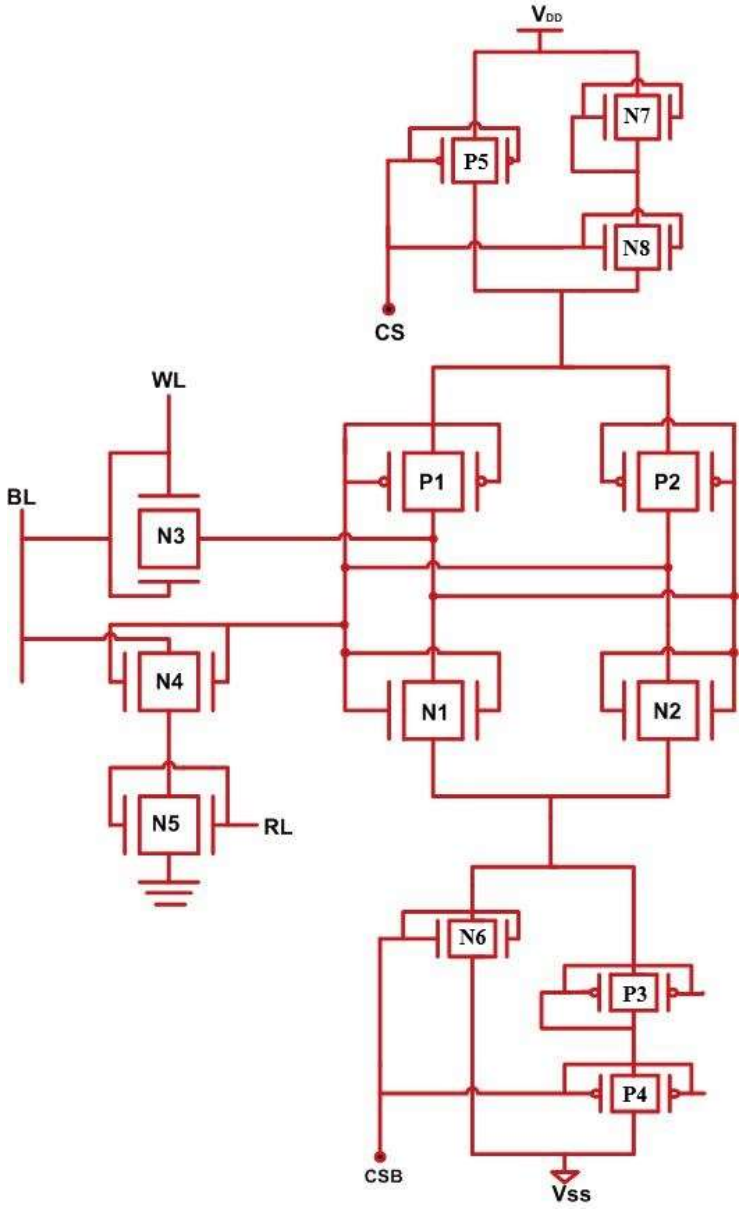

Figure 5.16(b): 7T SRAM with SVL Technique

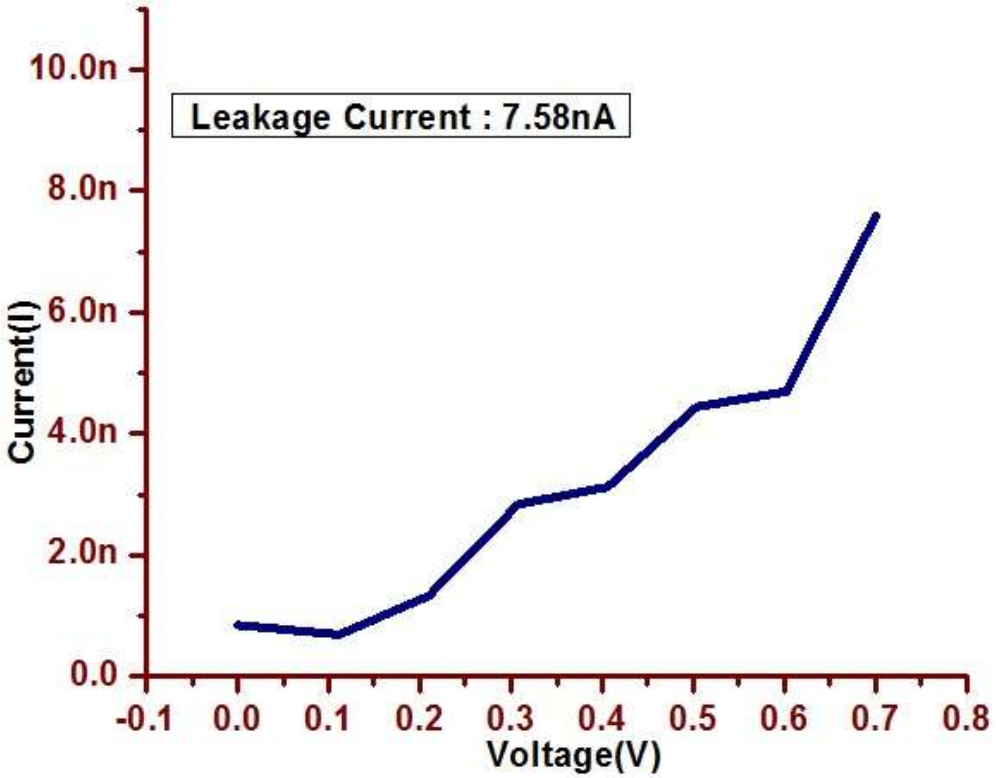

Figure 5.17: Leakage Current of 7T SRAM using SVL Technique

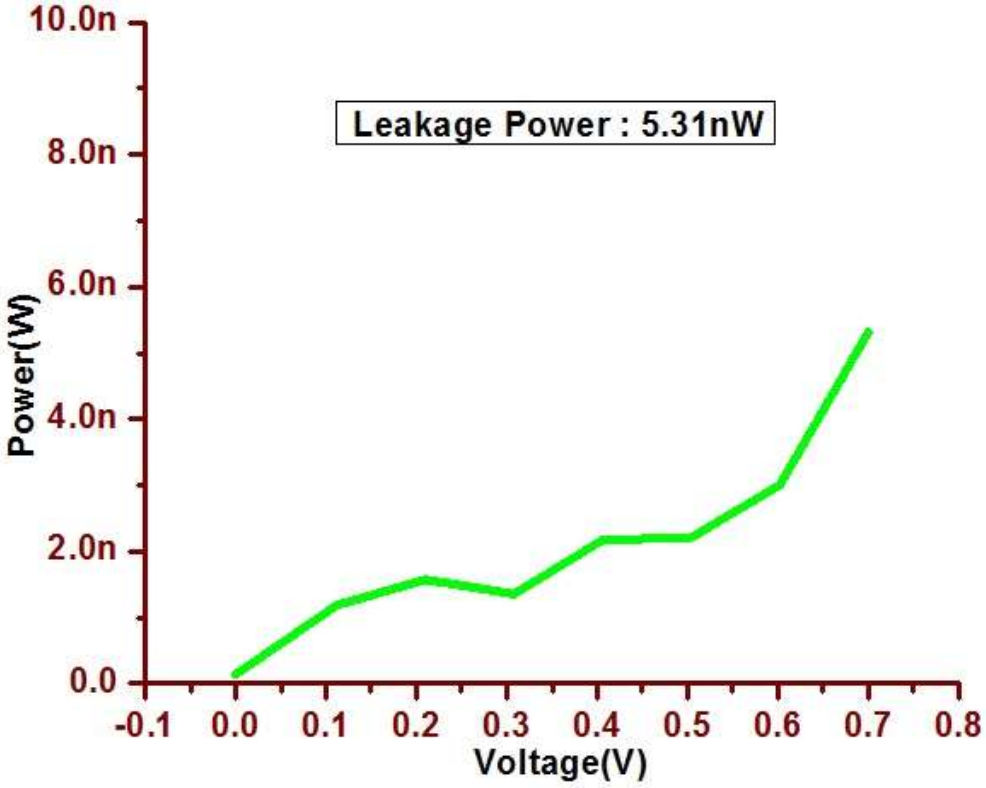

Figure 5.18: Leakage Power of 7T SRAM using SVL Technique

5.3 Proposed Leakage Reduction Technique Implementation on Different FinFET Based SRAM Cells

5.3.1 Self-controllable voltage level (SVL) Technique Implementation on FinFET based 6T SRAM

A proposed SVL method has been earlier expounded in section 5.2.4. The detailed discussion of 6T based SRAM is shown below in Figure 5.19. Waveforms related to leakage current and power are shown below in figure 5.20 and figure 5.21. A waveform clearly represents the noteworthy leakage current and power reduction by 80.9% and 78.2% when compared with a basic FinFET based 6T SRAM.

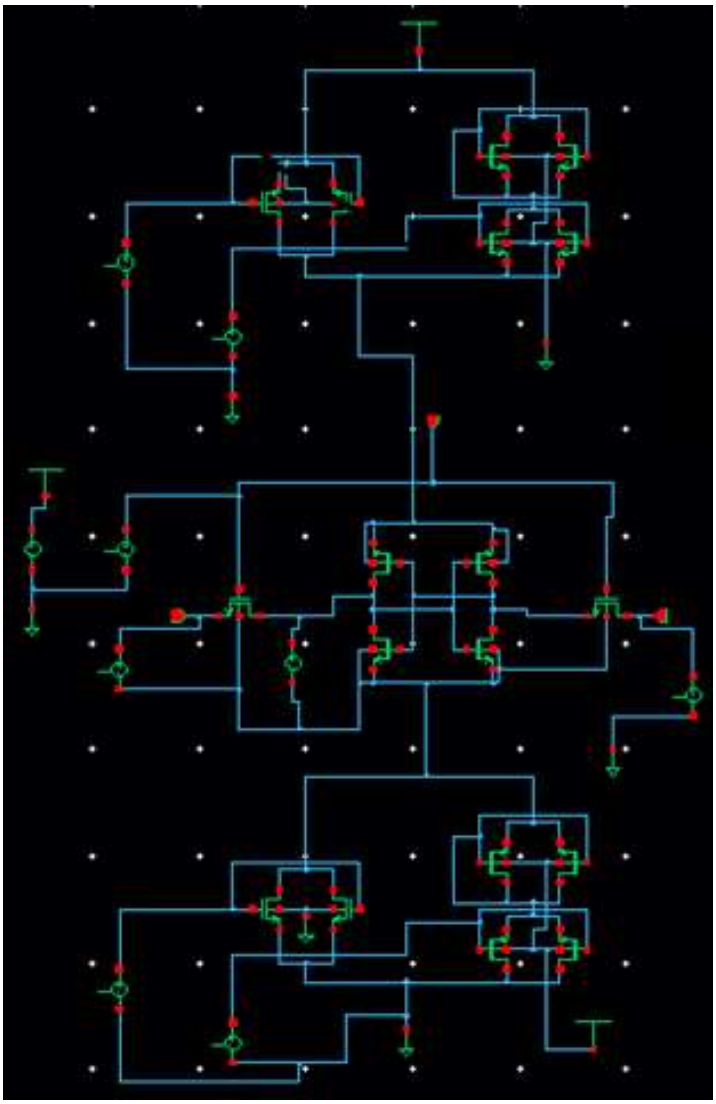

Figure 5.19(a): 6T SRAM with SVL technique in Cadence view

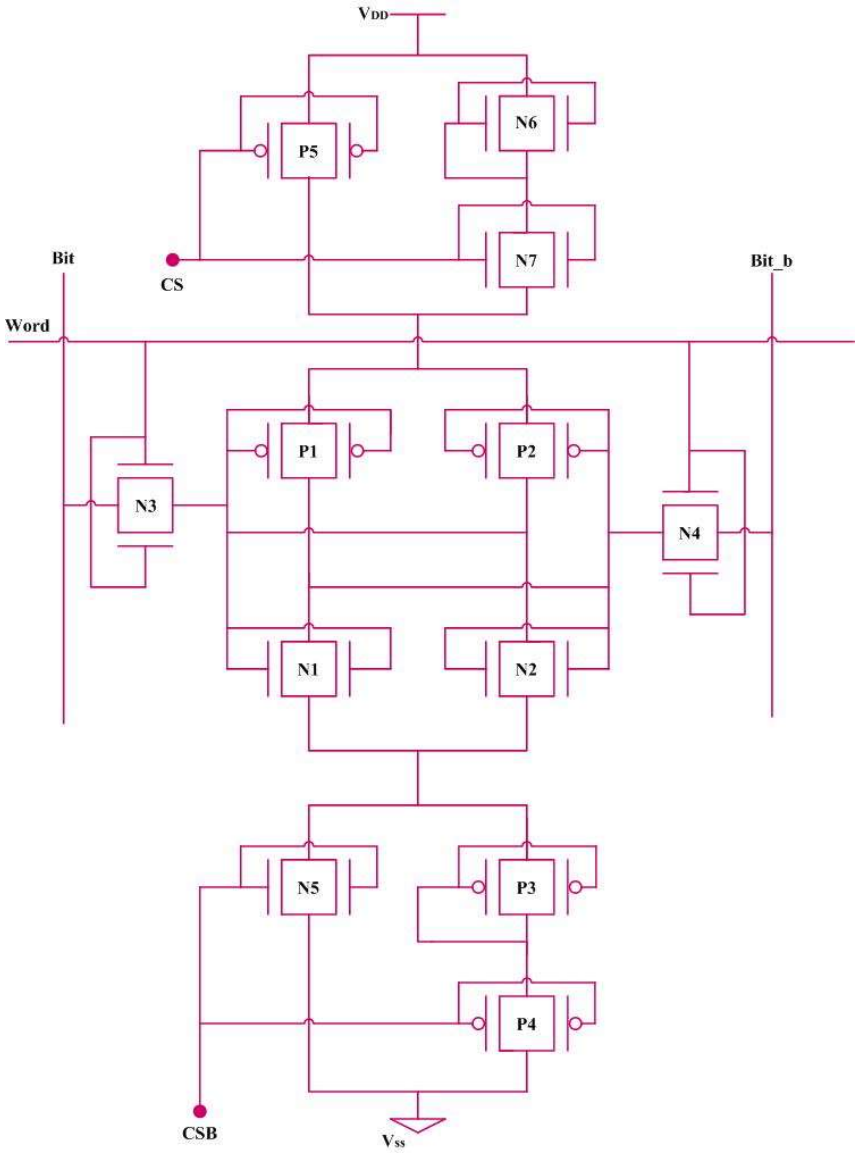

Figure 5.19(b): 6T SRAM with SVL technique

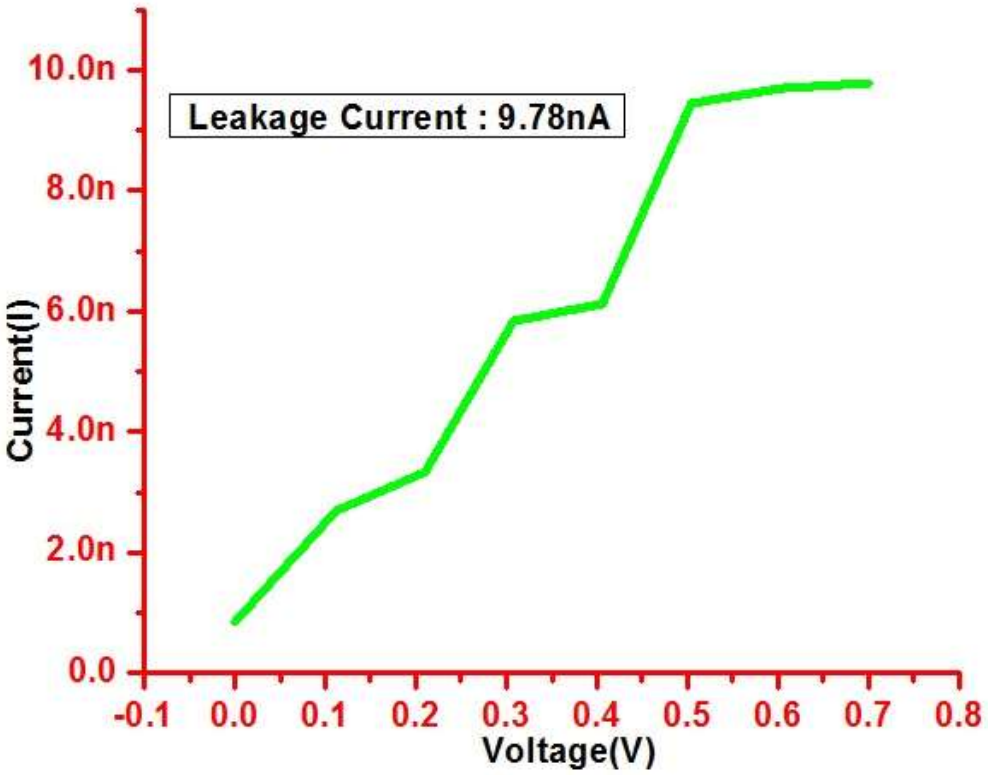

Figure 5.20: Leakage Current in 6T SRAM with SVL Technique

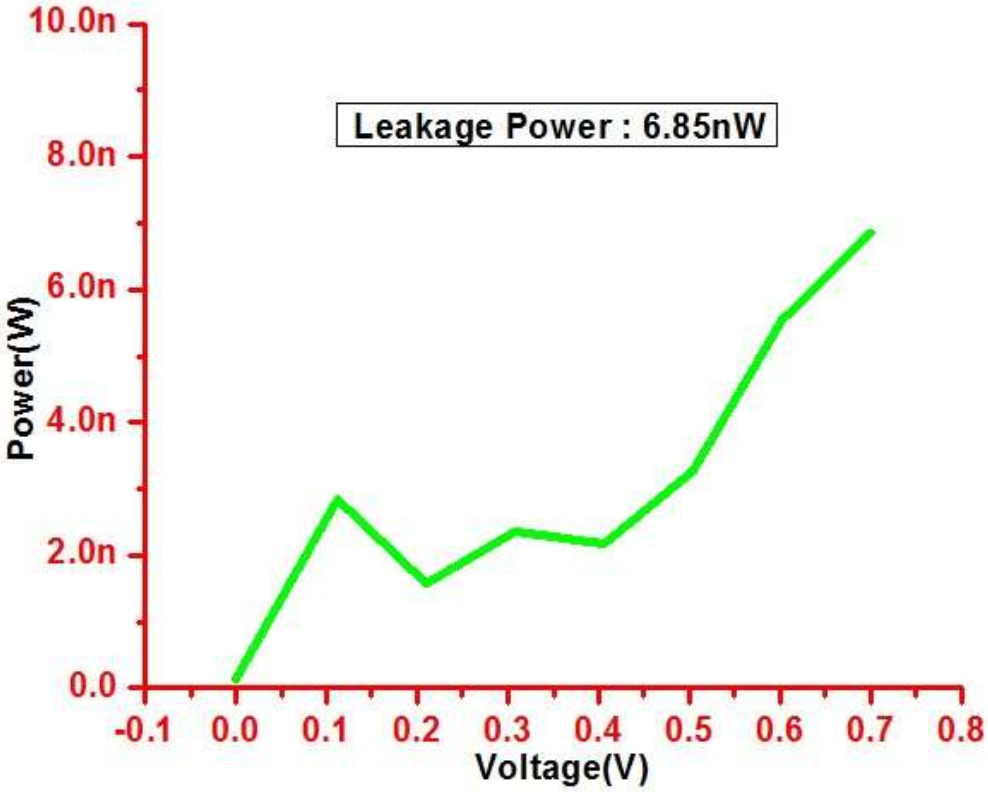

Figure 5.21: Leakage Power in 6T SRAM with SVL Technique

5.3.2 Self-controllable voltage level (SVL) Technique Implementation on FinFET based 8T SRAM

A proposed SVL method has been earlier expounded in section 5.2.4. The detailed description of 8T based SRAM shown below figure 5.22. A FinFET model of 8T based SRAM waveforms for leakage current and leakage power are exhibited in figure.5.23, figure 5.24. The waveform clearly describes that there is a leakage current reduction of 81.52% and leakage power reduction of 80.2% when compared to FinFET model of 8T based SRAM.

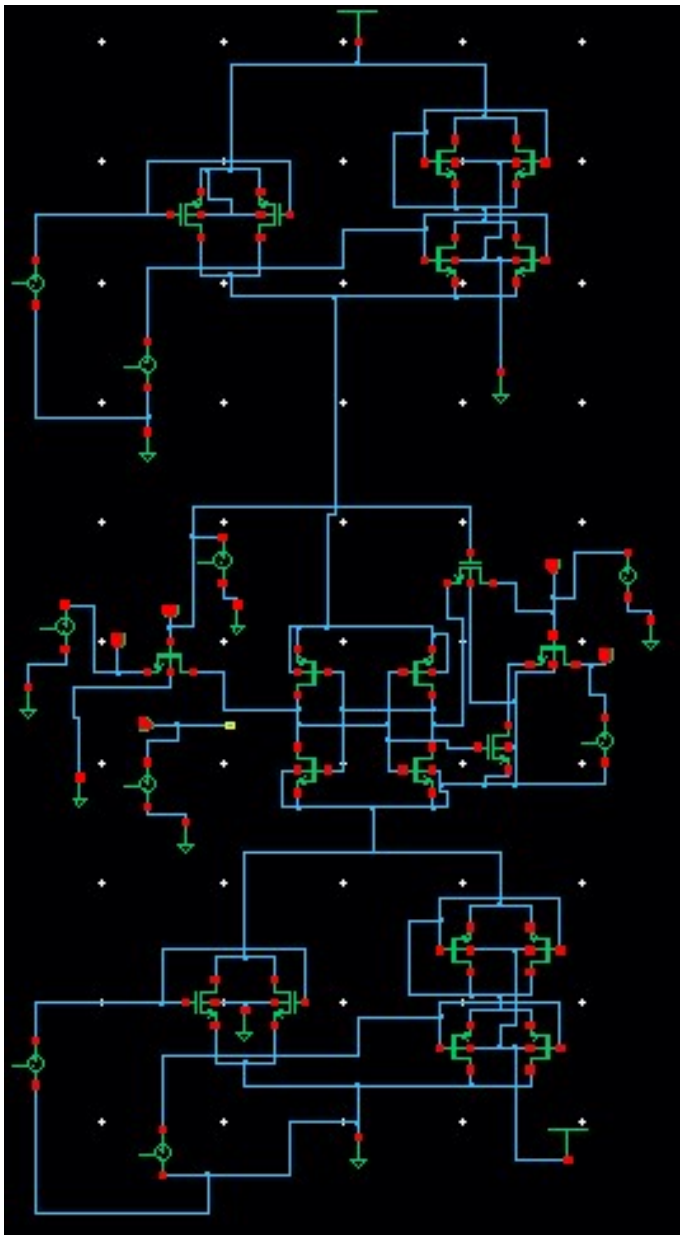

Figure 5.22(a): 8T SRAM with SVL technique in Cadence view

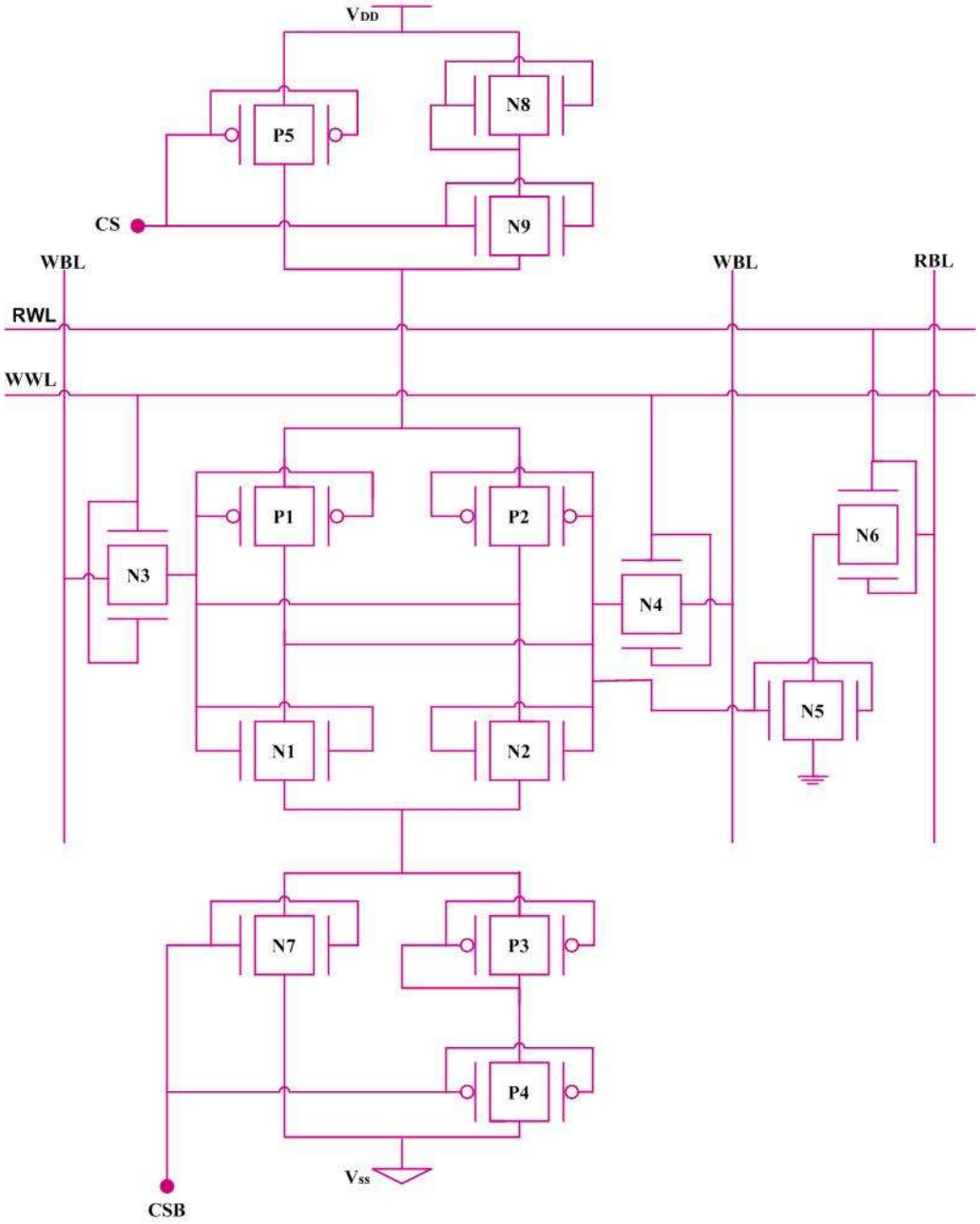

Figure 5.22(b): 8T SRAM with SVL technique

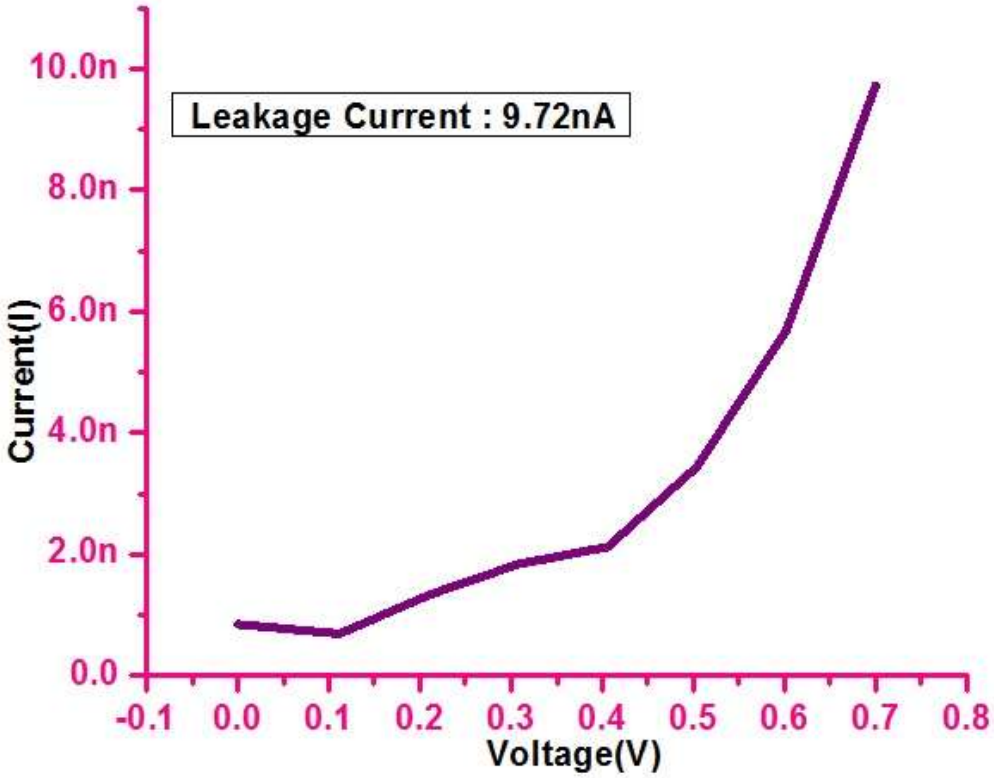

Figure 5.23: Leakage Current of 8T SRAM with SVL technique

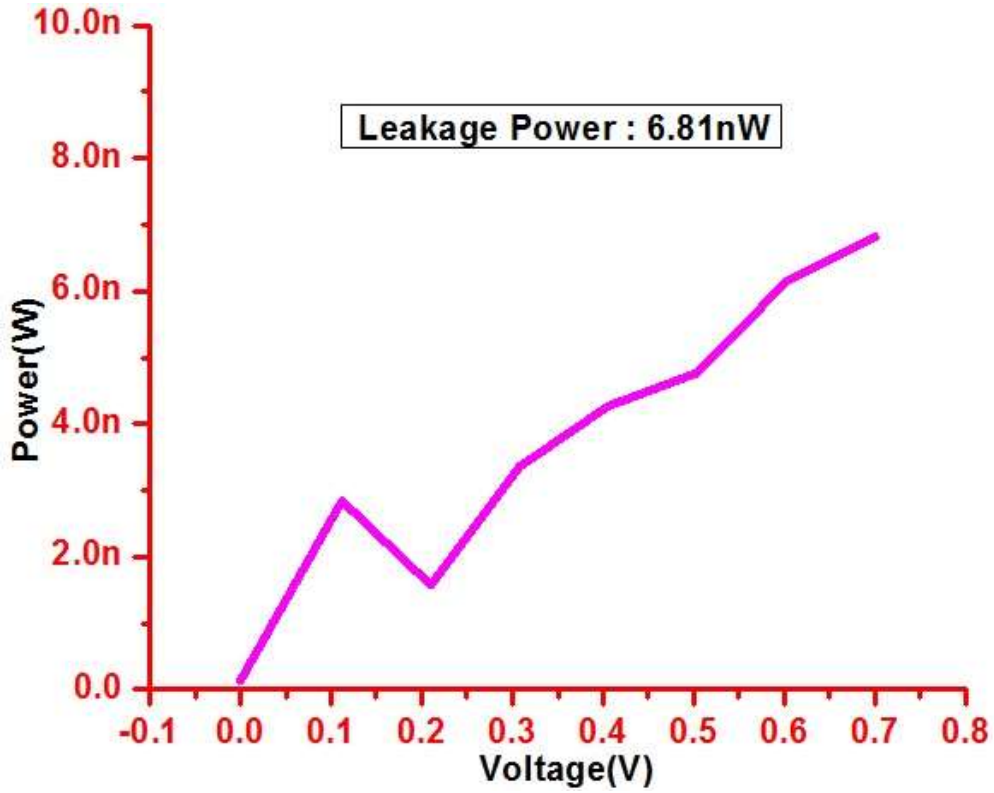

Figure 5.24: Leakage power of 8T SRAM with SVL technique

5.3.3 Self-controllable voltage level (SVL) Technique Implementation on FinFET based 9T SRAM

This technique has been explained in session 5.2.4 and a detailed description of the 9T SRAM cell is presented in previous chapters. The proposed SVL circuit connected to the FinFET based 9T SRAM cell is shown in Figure 5.25. Waveform of leakage current is displayed in figure.5.26 and waveform of leakage power is displayed in figure.5.27. The waveform clearly represents the leakage current reduction by 81.3% and leakage power reduction by 82.1%, when compared with normal FinFET model of 9T based SRAM cell.

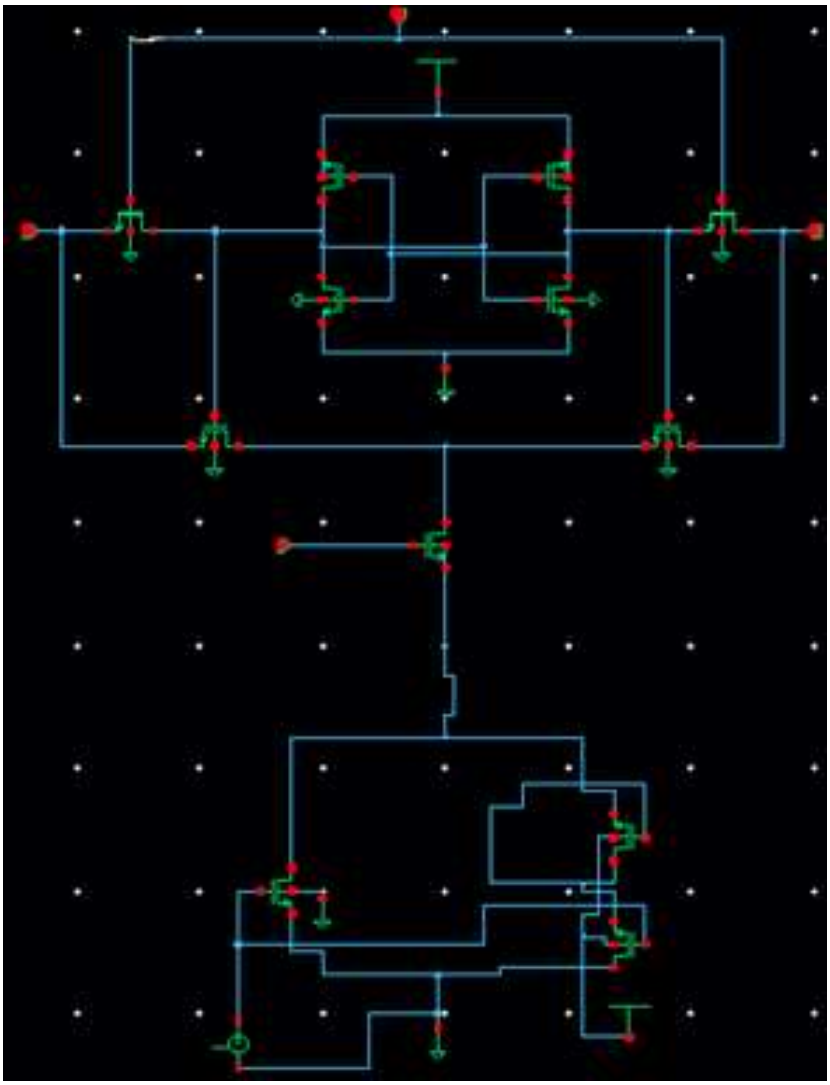

Figure 5.25(a): 9T SRAM with SVL technique in Cadence view

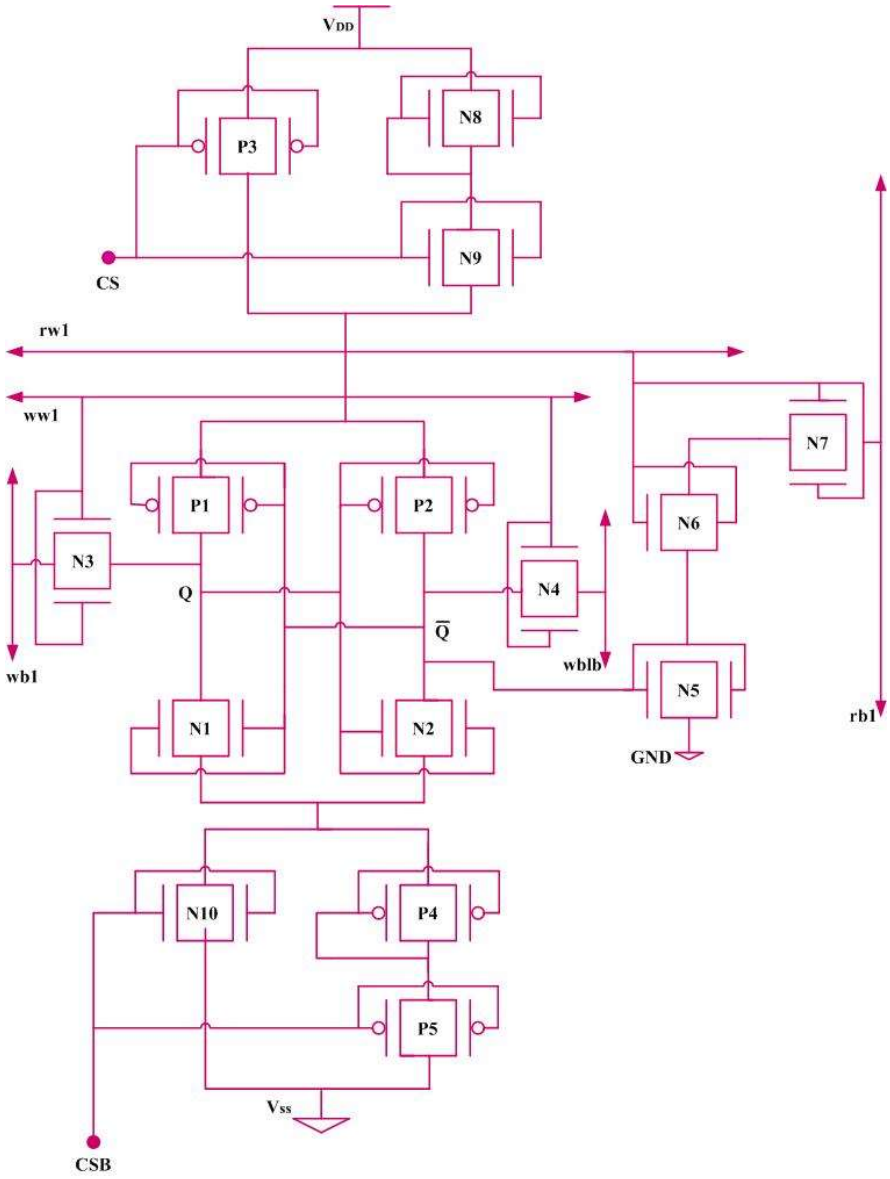

Figure 5.25(b): 9T SRAM with SVL technique

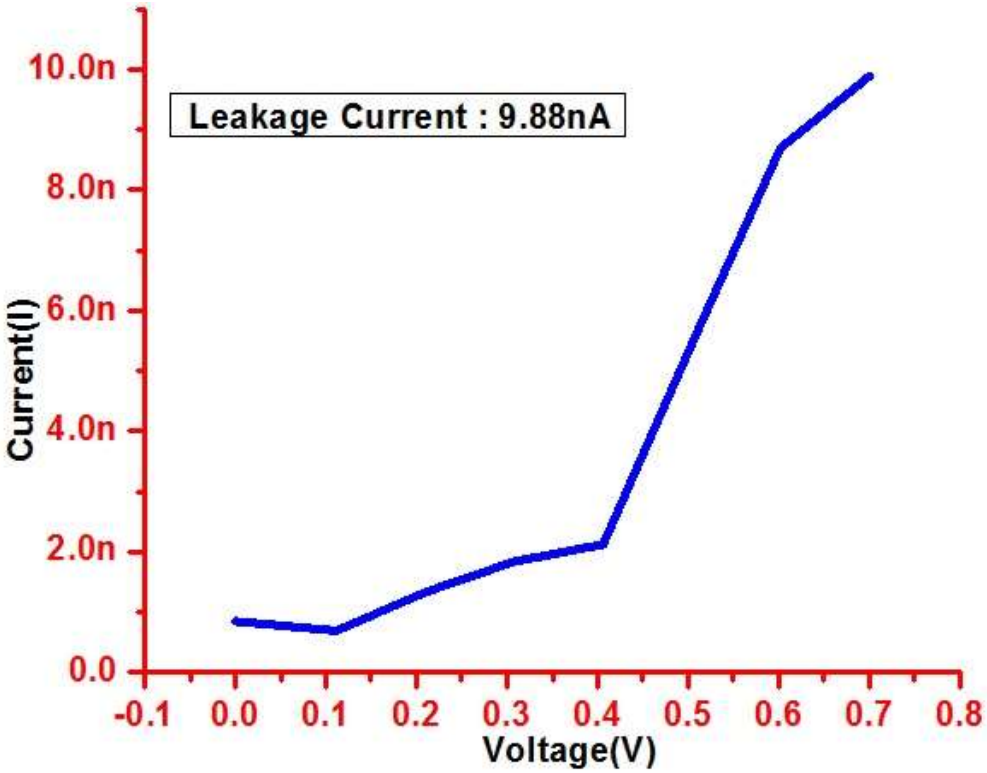

Figure 5.26: Leakage Current of 9T SRAM with SVL technique

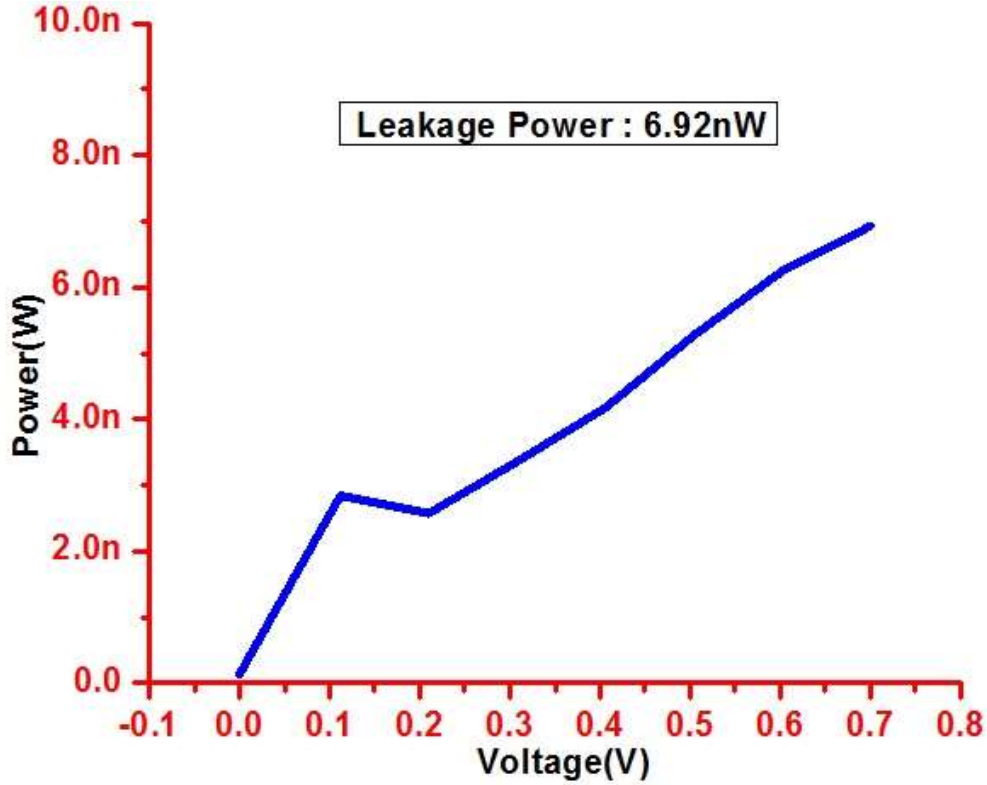

Figure 5.27: Leakage Power of 9T SRAM with SVL technique

5.3.4 Self-controllable voltage level (SVL) Technique Implementation on FinFET based 10T SRAM

A proposed method called SVL is discussed in session 5.2.4. The proposed design is connected to FinFET model 1OT based SRAM as shown in figure.5.28. Waveforms of leakage current is shown in figure.5.29 and waveform of leakage power is shown in fig.5.30 of FinFET model of 10T based SRAM. Here waveform clearly represents the leakage current reduction by 82.75% and leakage power reduction by 80.72% when compared to simple 10 T based SRAM cell.

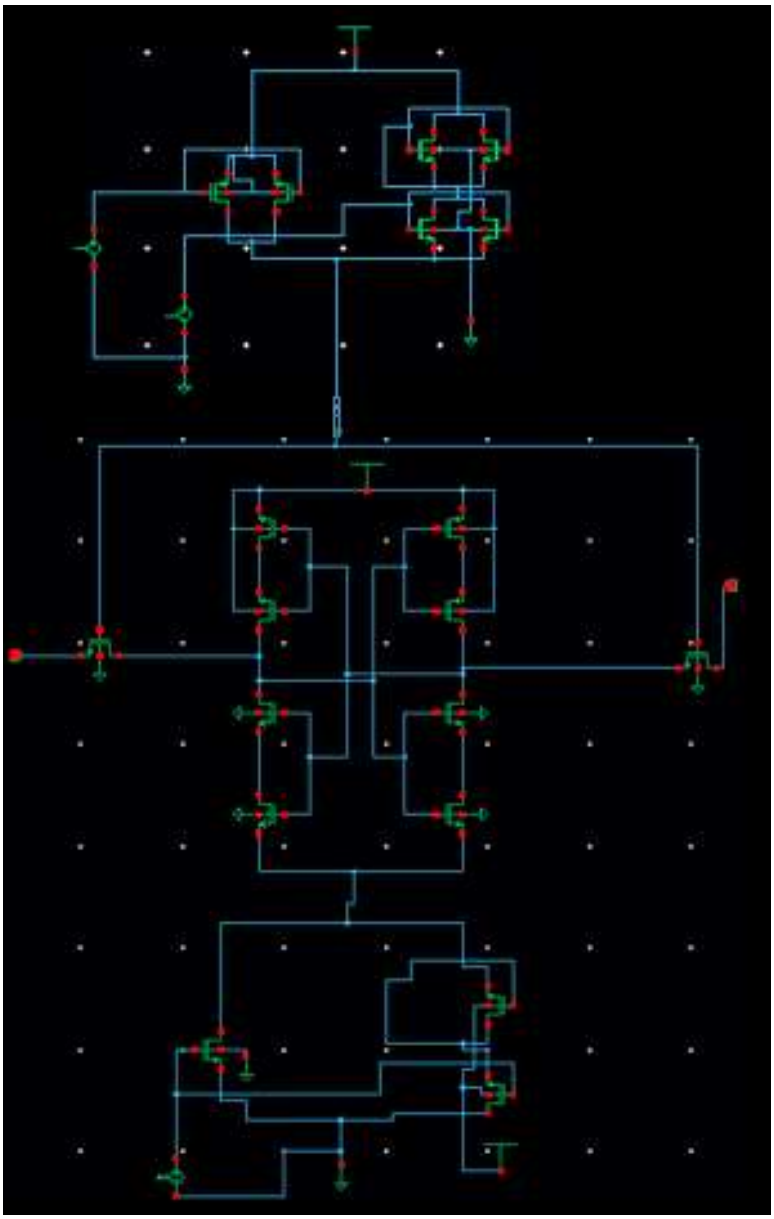

Figure 5.28(a): 10T SRAM with SVL Technique in Cadence view

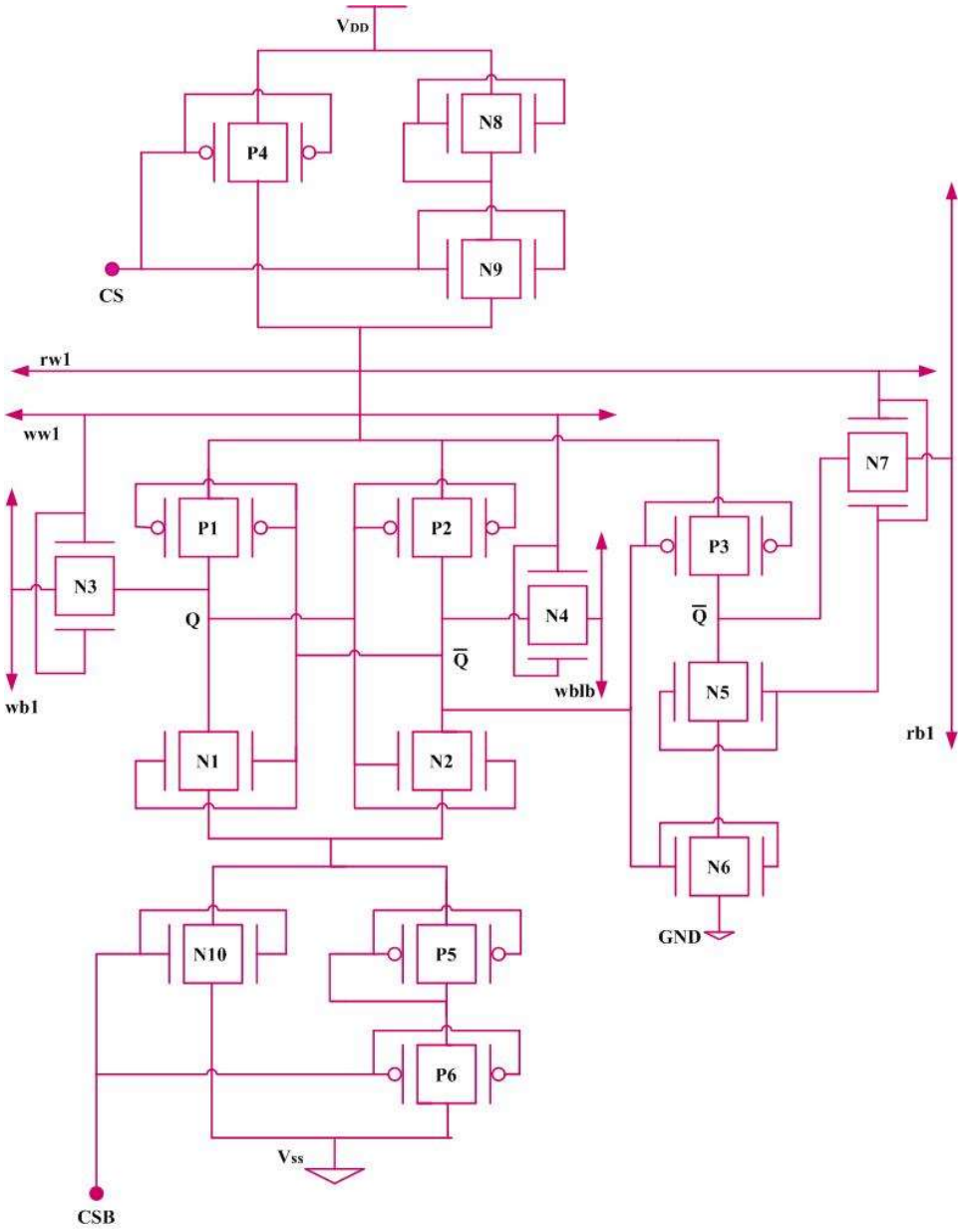

Figure 5.28(b): 10T SRAM with SVL Technique

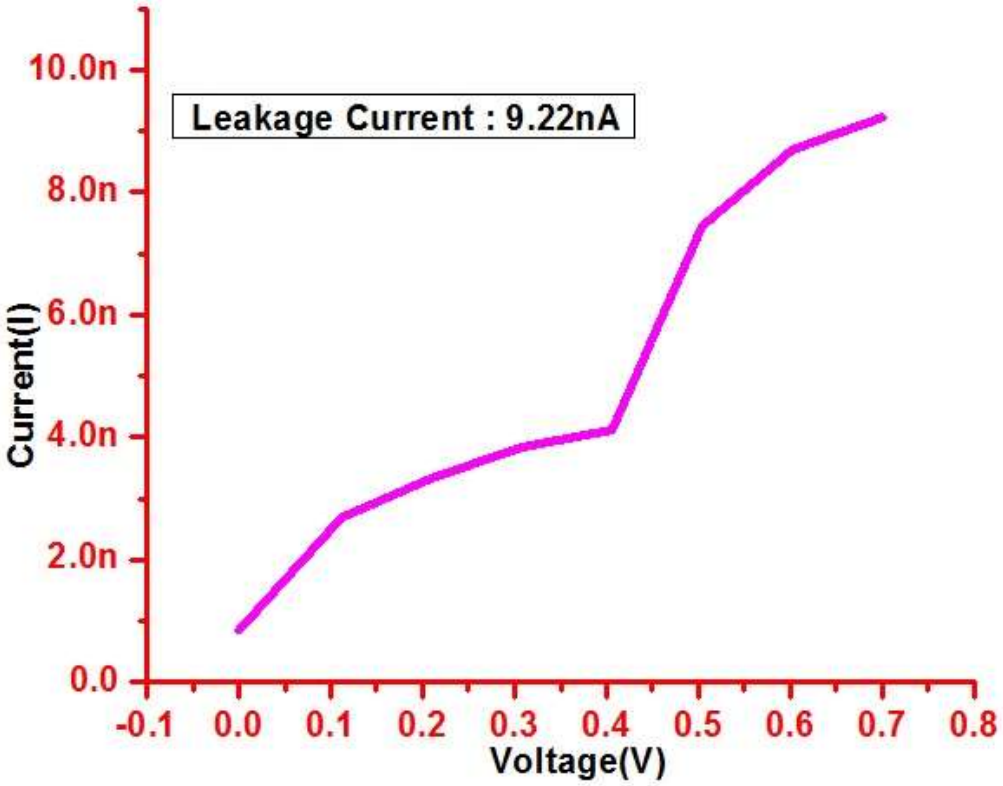

Figure 5.29: Leakage Current of 10T SRAM with SVL technique

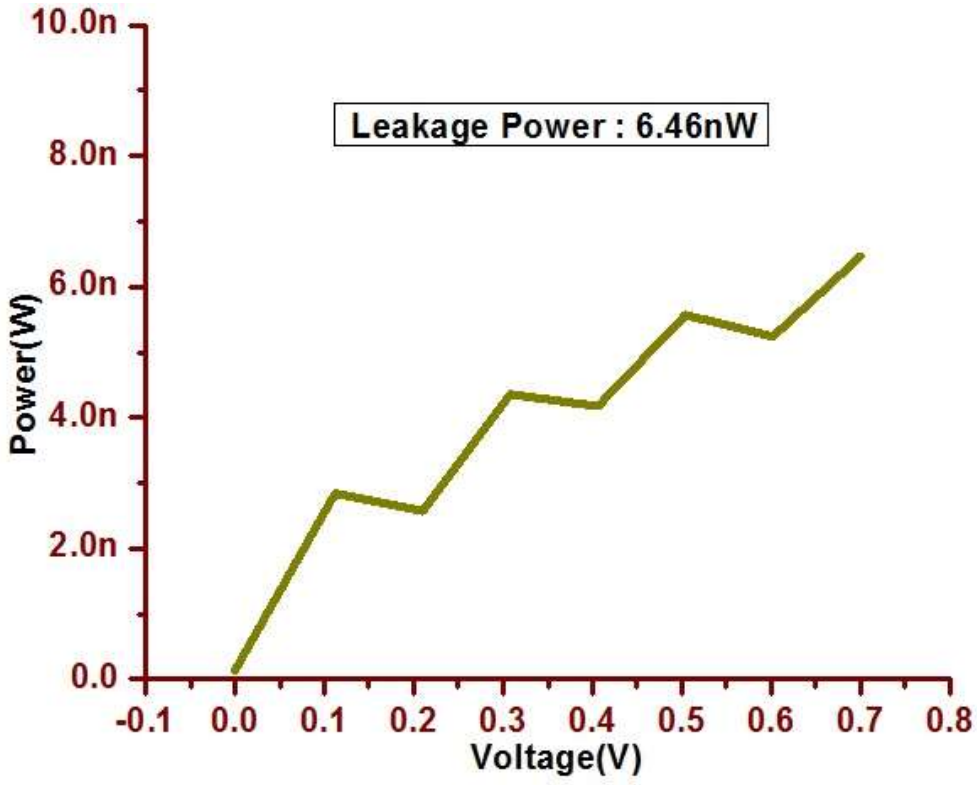

Figure 5.30: Leakage Power of 10T SRAM with SVL technique

5.3.5 Self-controllable voltage level (SVL) Technique Implementation on FinFET based 12T SRAM

The proposed Drowsy-Cache technique has been explained in detail in session 5.2.4.The proposed SVL circuit connected to FinFET model 12T based SRAM is shown below in figure 5.31. Waveform of leakage current is shown in figure.5.32 and leakage power in figure 5.33.The waveform clearly represents a leakage current reduction of 83.3% and leakage power reduction of 84.1% when compared with a FinFET model 12T based SRAM.

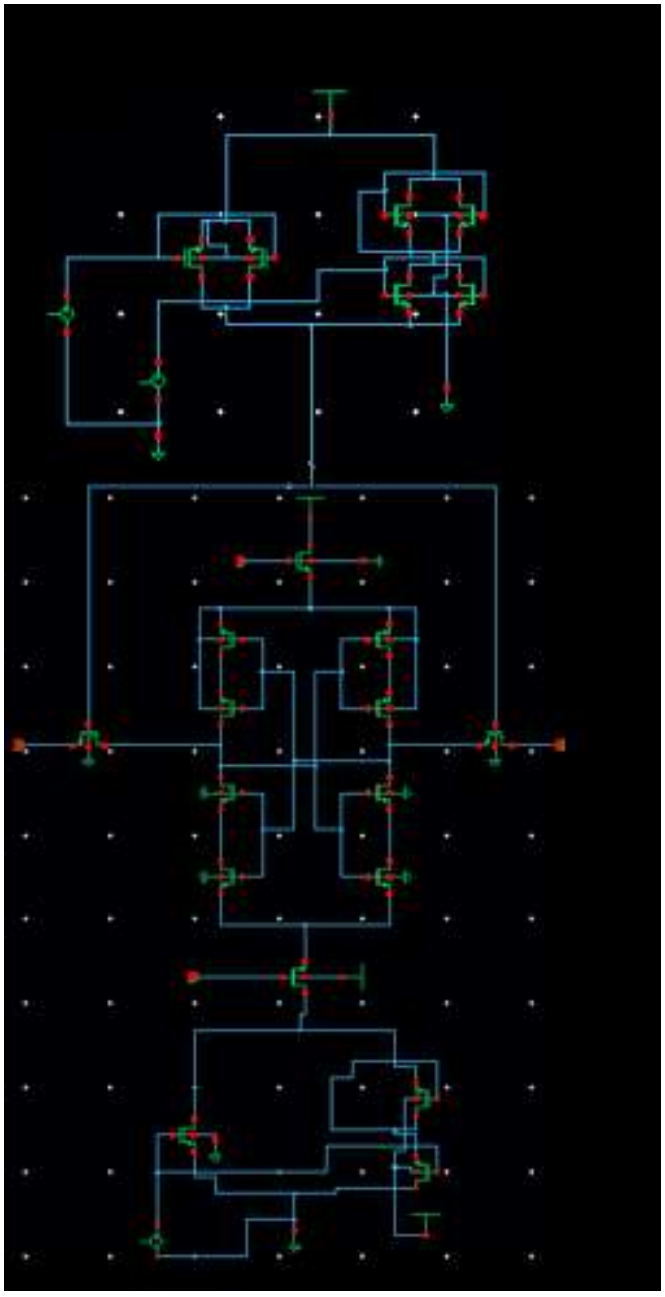

Figure 5.31(a): 12T SRAM with SVL technique in cadence view

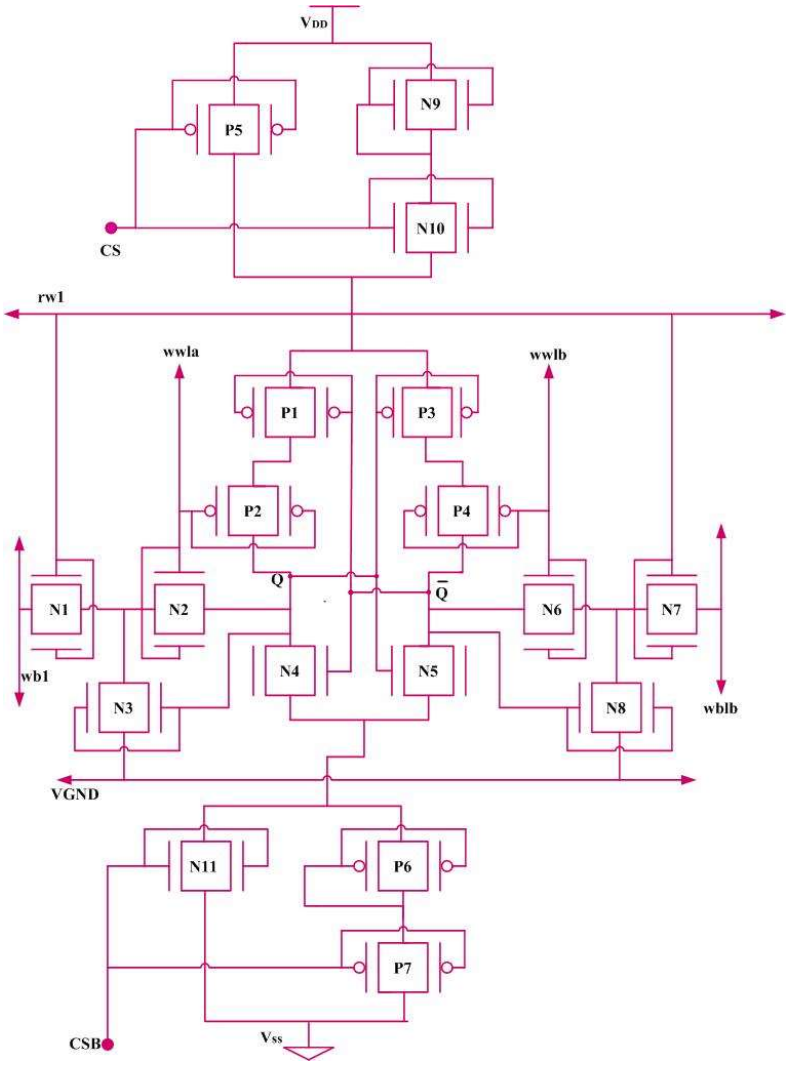
VDD
P5
N9
N10
CS
rw1
wwla
wwlb
P1
P3
P2
P4
Q
Q̄
N1
N2
N6
N7
wb1
N4
N5
N3
N8
wblb
VGND
N11
P6
P7
CSB
Vss

Figure 5.31(b): 12T SRAM with SVL technique

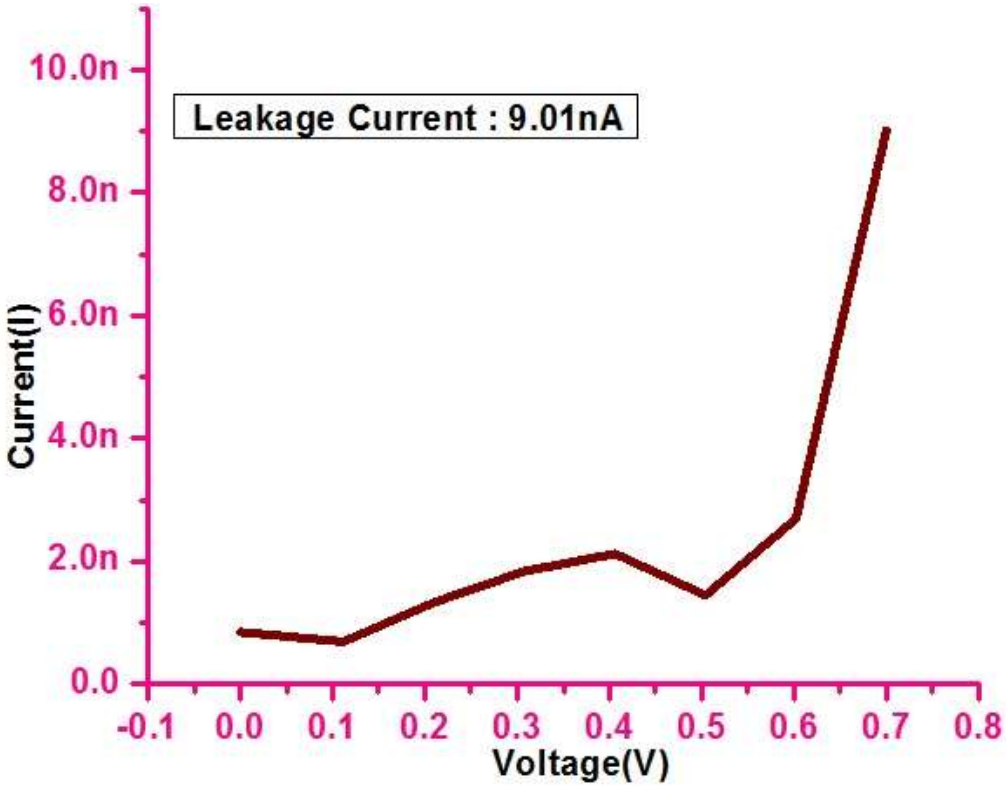

Figure 5.32: Leakage current of 12T SRAM with SVL technique

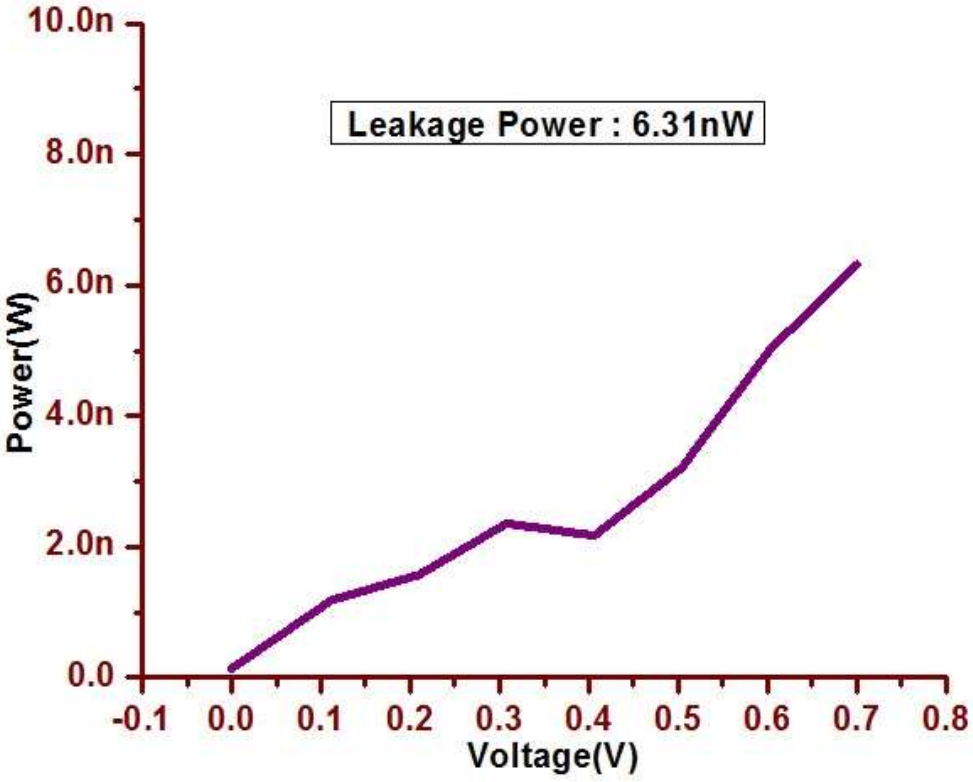

Figure 5.33: Leakage Power of 12T SRAM with SVL technique

5.4 Result Analysis

The different leakage reduction techniques such as MTCMOS, AVL, and Drowsy–cache and the proposed SVL are implemented and the leakage current and leakage power are calculated for the proposed design of 7T SRAM and it is found that the SVL technique provides the better performance than the other techniques where it has reduced the leakage current by 84.9% and leakage power by 87.3% and the proposed technique of SVL is also implemented for other 6T , 7T , 8T ,9T,10T,12T SRAMs and found to have better power dissipation and leakage current. All the results were implemented with 18nm FinFET technology. The Table 5.1 shows the leakage power and current for 7T SRAM when applied with different leakage reduction techniques. And Table 5.2 gives the comparison of leakage current and power for different transistor topologies with SVL leakage reduction technique where we can see a drastic change in leakage currents and leakage power for the SRAM with and without using techniques.

Table 5.1: Comparison of Leakage current and leakage power of 7T SRAM with different techniques

Leakage reduction Techniques	Leakage Current Without technique	Leakage current with technique	Leakage Power Without Technique	Leakage Power With Technique
MTCMOS	50.26nA	12.1nA	35.22nW	8.47nW
AVL		11.3nA		7.91nW
Drowsy-cache		8.7nA		6.12nW
SVL		7.58nA		5.31nW

Table 5.2: Comparison of the leakage power and leakage current with proposed SVL technique applied to different transistor SRAM

SRAM Cells	Leakage Current Without technique (nA)	Leakage current with technique (nA)	Leakage Power Without Technique (nW)	Leakage Power With Technique (nW)
6T	51.31	9.78	35.91	6.85
8T	52.63	9.72	36.84	6.81
9T	52.87	9.88	37.1	6.92
10T	53.32	9.22	37.32	6.46

12T	54.12	9.01	37.88	6.31

Table 5.3: Comparison of 7T SRAM with other Published Papers

Leakage Power (7T SRAM cell)				Total Power Consumption(ON+OFF state Power consumption)		
Ensan et.al[148]	Kushwah et.al[149]	Vandana et.al[150]	Proposed 7T SRAM	Without technique	With technique	
					Read operation	Write Operation
69.1nW	26.63nW	20.95nW	5.3nW	11.9nW	8.08nW	7.52nW

5.5 Advantage of Proposed Leakage Reduction Technique

The Key benefit of the proposed SVL leakage reduction technique is reducing the leakage current and power by maintaining the virtual ground and virtual supply in idle mode through the control signal. The USVL is responsible for reducing the subthreshold leakage and the LSVL is responsible for reducing the gate tunneling leakage and also the subthreshold leakage, by combining both the techniques it is possible to decrease the leakage current to a maximum extent in comparison to other type of leakage reduction techniques.

5.6 Chapter Summary

In this chapter the leakage reduction techniques are applied to the proposed 7T SRAM cell and by applying the SVL technique the leakage current is reduced by 84.9% and the leakage power is reduced by 87.3% in comparison to the 7T SRAM without applying the technique .whereas by applying MTCMOS method the leakage current is reduced by 75.9% and power by 70.1% and by AVL technique the leakage power has come down to 72.8% and current by 77.5% and another technique drowsy cache has brought down the leakage current by 82.6% and leakage power by 81.3% in comparison to 7T SRAM based on FinFET. It is evident that of all the techniques the SVL is better.

And the Proposed SVL method is applied to the circuits of other transistor topologies and it is found that the leakage current of 6T SRAM has reduced by 80.9% and power by 78.2%.and the 8T SRAM has a reduction of 81.5% of leakage current and 80.2% of leakage power. The 9T has 81.3% and 82.1% of reduction in leakage current and leakage power.10T and 12T SRAMs have 82.75%,80.72% and 83.3%,84.1% of the leakage current and leakage power respectively when compared to the 6T , 8T,9T,10T,12T FinFET based SRAMs respectively.

CHAPTER 6

PROCESS VARIATION, TEMPERATURE EFFECTS ON LOW POWER SRAM CELL AND LAYOUTS

6.1 FINFET Process Variation

Digital integrated circuit that are successfully designed will have some complications for optimizing the specification of different designs. Parameters like speed, silicon area, testability, power dissipation and design effort. [151]. Such approach of design intrinsically presumes that transistor properties like physical and electrical are deterministic, thus that predict the lifetime of the device. However, as silicon technology is moving towards sub nano regime below 50nm, transistor will act as deterministic. During the manufacturing process there will be fluctuations in device that pose serious problem in nano meter regime. Till 0-35um technology variation in process will provide problem in IC industry. Circuits predominantly are immune to process variations that are negligible when compared to general size of device. As there is a growth between optical wavelength and size of device during lithographic process that is scaled down below 65nm will provide a severe issue for various parameters. [151].

Integrated circuit functioning gets affected by variation observed in various process parameters and it is seriously affects the dimension of transistor that are continuously scaled. Such variations in parameters will affect the memory circuit in various ways. Based on such variations it experiences the failure of stability. Thus, the limitations observed in process variation will not only affect the physical structure but also degradation of device, and that result in scaling of technology to become worst. Employing a non si alternatives to resolve the issues faced due to traditional si based technology and it may not be the right choice. Whereas miniature device that are non-silicon will have an effect of different process variation. So to overcome this problem we need to design ICs such that it will automatically correct the issues been faced [152].

6.1.1 Device Parameters

The degradation in the functionality of integrated circuits is mainly because several process variation parameters such as length of channel, transistor width, thickness of oxide, flat band condition, threshold voltage, bit line voltage, word line voltage, power supply voltage etc. These variation affect the SRAM at device level, circuit level and material level.

6.1.2 Process Variations at Device Level

The characteristic variation of a device at time t=0sec is because of variation in spatial process. Thus it can be subdivided into two main components: inter die, intra die [152]. It is clarified by a chip example which is designed at a particular speed as shown below in figure.6.1. it displays a speed of chip that follow distribution at each point. Its behavior relates at t=0s, Intra die variations refer to transistor strength variation in same die. Whereas if variations are among different die of different run, wafers and lot then it is called parametric variation and it comes under inter die variation. It is due to the fluctuations in width (w), length (L), flat band conditions and thickness of oxide (tox) etc. [153]. Whereas RDF's i.e., Random Dopant Fluctuations and LER i.e., line edge roughness will cause the parameters and will come under intra die random variation [154-157]

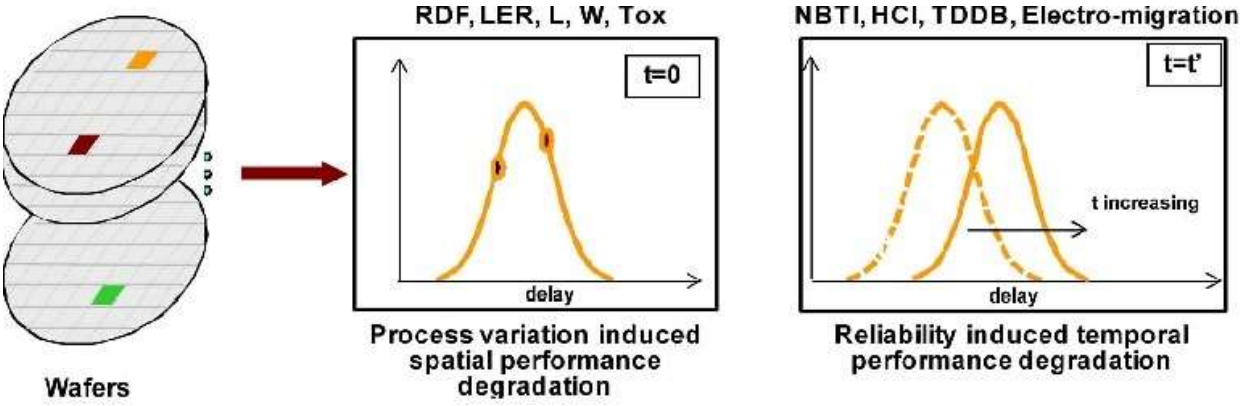

Figure 6.1: Process Variation

Since several decades we are effectively using lithography method for fabrication. Figure 6.2. displays a trend in advancement of technology of optical based lithography and size. In current technology nano scale regime is below 65nm, where the device size is small compared to wavelength of light. Hence, actual layout printing is very difficult and it get worst as the fabrication

procedure is carried out with different process. Few the process and its corresponding sources are given below [158]:

- wafer: reflectivity, topography
- reticle: critical dimensional, defects, proximity effects, error
- stepper: lens aberrations lens heating, dose, focus
- etch: flow rate , pressure, power
- resist: refractive index, thickness,
- develop: rinse, time, temperature,
- environment: pressure, humidity

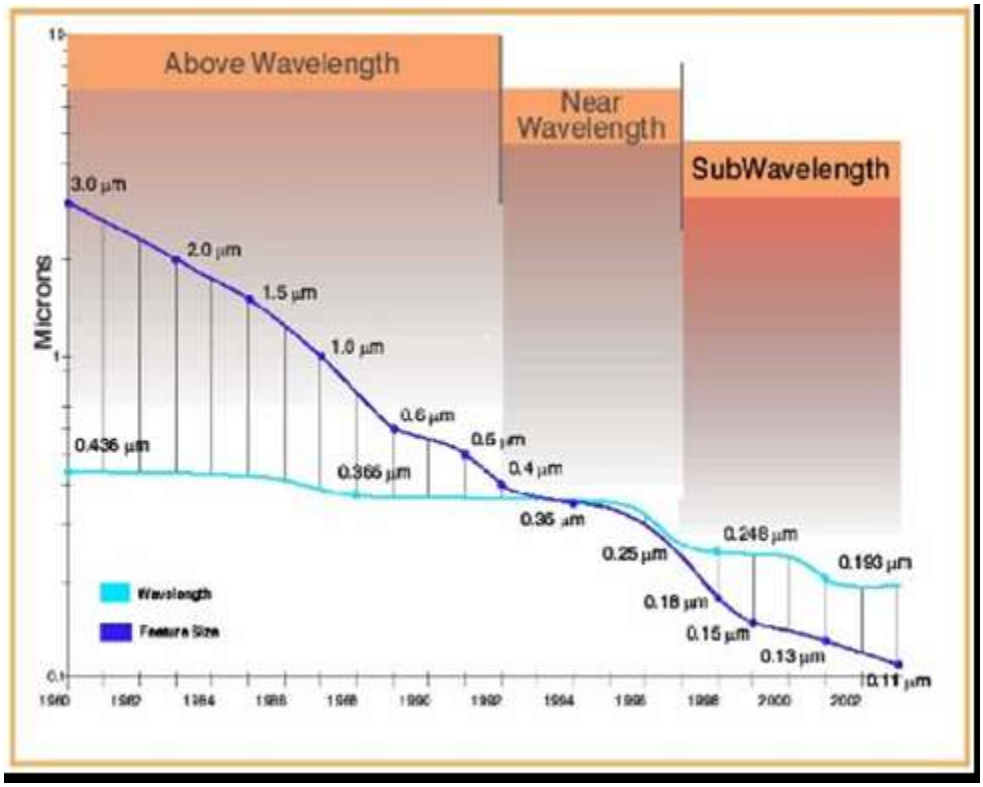

Figure 6.2:Scaling trends

When the above method is manufactured it results in various fluctuations among W,L,Vth, tox and also dopant atom concentration, irregularities inline edge. Here fluctuation in length is distance from source to drain that makes the potential of channel more prominent to electric field at drain

terminal. Due to this potential a gate terminal is needed for channel inverting and will reduce the length of gate and electric field near the channel will get increased [159].

In fig 6.3 a, during old generations of technology like 0.35, 0.25 and 0.18um, total number of doped atoms at channel was of order 1000. Hence, if we do small change in location and number of dopants used was not acceptable. However, in CMOS devices that are scaled at 65nm, 45nm, the required number of doped atoms would be small in order of 50 to 100 as illustrated below in fig 6.3(b) and fig.6.3(c). so, due to the variation in dopant atom across channel has shown a larger impact. It consists of few statistical fluctuations that will translate a variation of threshold voltage A FinFET based threshold voltage is defined by gate voltage that is enough for inverting all channel Fin structure [160].

Few systems design that doesn't follow the process variation considerations will fail to meet few desired requirements like power, timing, quality and stability specifications. If an example is considered where a chip is designed that runs at speed of 2GHz and will tend to work at 1 GHz which is worthless. Though, it can follow the design that will uphold the variations and their impact on various process parameters. Few designs are inefficient based on area and time that are beneficial.

Process variations issues are addressed in two methods i.e., designing the architectures and circuits which are immune to various process variation and controlling the existing process technology. Hence, we can select the first method instead of second method as it is expensive and in few cases it is more difficult to change the circuits of design. It is noted that new emerging devices suffers from various variations. Therefore, getting awareness on various process variation methods has become important in modern digital systems.

6.2 EFFECT OF TEMPERATURE

The change in temperatures will affect the performance of transistors, these temperatures need not be an external source but few transistors are affected by temperatures inside the device also. The variations in the transistors needs to be analyzed by proposing different models known as process corners. In transistors, the process variation to the attributes of a transistor such as a length, oxide thickness, and width is done during the fabrication of a circuit. The amount of process variation is marked at reduced process nodes (< 65 nm) as there is a change in the variation to a larger extent

of full dimension or width of a device as it approaches the fundamental dimension of atom size and wavelength light for patterning lithography mask.

Process variation affects the output performance of a circuit as it causes predictable and measurable variance mostly in the analog circuit because of mismatch. The overall yield of the device gets effected if variance causes measure or stimulated performance to decrease below or to increase above the given specification for a particular device. In SRAM data retention voltage signifies the least source voltage which it takes to store the arbitrary state in SRAM cells. The data retention voltages can be plotted using butterfly curves. In SRAM cell cross-coupled inverters with positive feedback are used to hold state on two opposite storage nodes at small source voltages there occur retention failure due to applied low voltage weakens the cross coupled inverters which are positive feedback. Due to unequal process variation transition is observed at lower voltages from written state to other states where it becomes inevitable [161]

Here the analysis of 6T, 7T, 8T SRAM is done by varying the functionality of transistors in different modes. Process corners represent positioning of transistors where each type of transistor is positioned with fast or slow functioning and also there is a typical functionality where both transistors work in typical typical mode.

6.3 Result Analysis of Process Variation

The SRAM's are designed and simulated with Cadence Virtuoso at 18nm FinFET technology. In order to check the Data retention voltage versus respect to the change in Temperature at each process corner the process corner analysis is done by varying the temperatures form -20 ^{0}C to 120 ^{0}C.Here Data Retention Voltage is holding of a zero value and checking the leakage current in the circuit at the output end. The temperature versus Voltage curves for different process corners are shown in the Figure 6.3, Figure 6.4, Figure 6.5 and values are tabulated in Table 6.1, Table 6.2, and Table 6.3 for 6T, 7T and 8T SRAM cells respectively.

Table 6.1: Data Retention Voltage vs Temperature in 6T SRAM

Temp	Voltage (mV)				
°C	SS	SF	FS	TT	FF
-20	23.5885	52.4157	20.9511	38.3875	55.197
0	29.0906	59.5881	24.3898	43.6537	60.0212
20	34.7408	67.1595	28.1928	49.1447	64.9686
40	39.3259	73.1666	31.5519	53.5781	68.9416
60	43.6832	78.6202	34.9581	57.7519	72.6577
80	47.8733	83.5807	38.4093	61.7347	76.1446
100	51.9479	88.027	41.9015	65.5748	79.4012
120	55.953	91.5858	45.4333	69.2991	82.4082

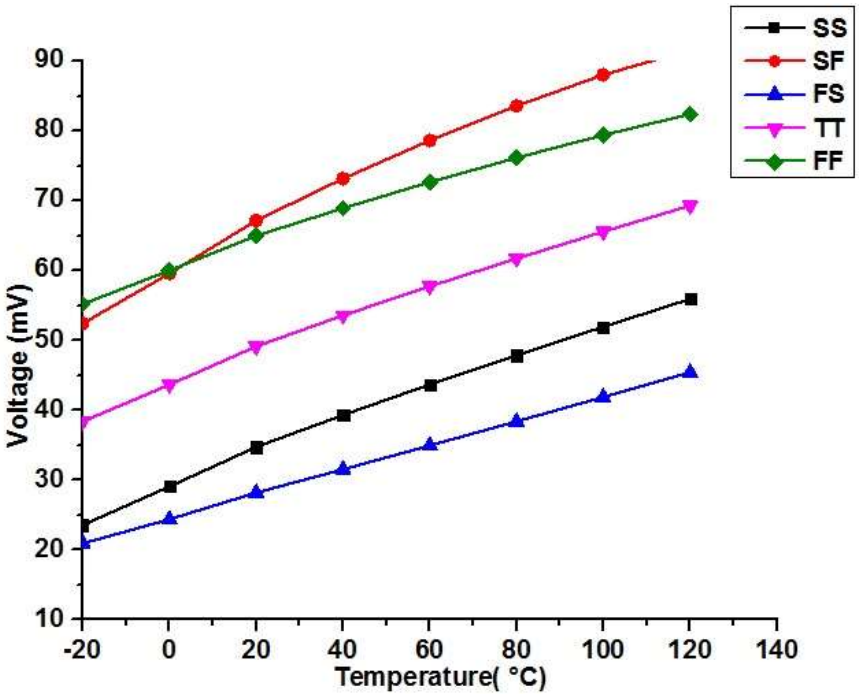

Figure 6.3: Data Retention Voltage vs Temperature in 6T SRAM

At -20 ^{O}C in SS corner, the change in Data retention voltage is low at lower temperatures and increases with the increase of temperature. Here in SS corner, the Data retention voltage increases initially and then is constant from 27 ^{O}C onwards up to some temperature and then increases as the temperature becomes high. The mobility in both the devices N- type /P-type decreases in the beginning affecting a reduction in the current-carrying ability of the devices. Thus, resulting in leakage voltage through both the devices to increase. And, the SRAM is able to retain the data at low voltages. Hence, Data retention voltage increases with increase in temperature. The change in temperature from -20^{O}C to 27 ^{O}C has an increase of 65% in Data retention voltage in 6T SRAM,

53% in 7T SRAM and 57% in 8T SRAM as can be seen in Figures 6.3, 6.4, 6.5 and as the temperature is increased from 27 ^{O}C to 120^{O}C the Voltage increase further by 70.3% in 6T SRAM and by 54.5% for both 7T and 8T SRAM.

Table 6.2 : Data Retention Voltage vs Temperature in 7T SRAM

Temp	Voltage(mV)				
°C	SS	SF	FS	TT	FF
-20	2.65629	6.69384	1.82613	3.54197	4.41194
0	3.45011	7.83808	2.40656	4.40774	5.34138
20	4.4668	9.15295	3.16545	5.47421	6.52523
40	5.42484	10.3138	3.93041	6.48901	7.67502
60	6.44522	11.494	4.80736	7.58954	8.92198
80	7.53427	12.6896	5.80765	8.78194	10.2473
100	8.69834	13.8968	6.93485	10.0603	11.6307
120	9.94403	15.1159	8.18114	11.4106	13.0548

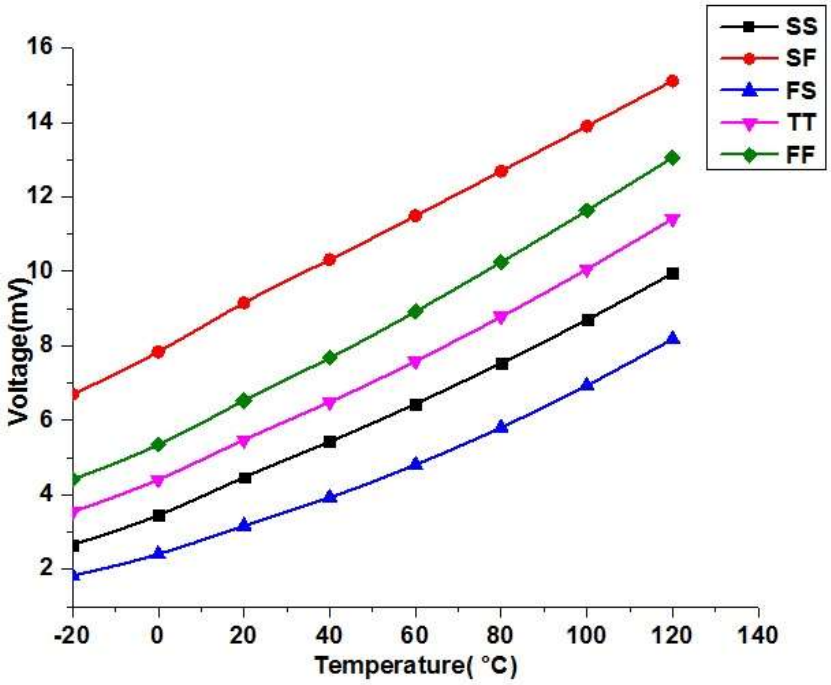

Figure 6.4: Data Retention Voltage vs Temperature in 7T SRAM

FS denotes fast NFETs and slow PFETs the Data retention voltage has least values in this corner. Here, the NFET is Faster than PFET and the current-carrying capability of NFET is greater than

PFET. Further, NFET loses its current carrying capability as the mobility decrease with increase of temperature. Here the as the pull up device is slow it cannot increase the output voltage to a maximum value but instead as the pull down device is faster the output voltage should be near to ground which is making the data retention to be at minimum value as the temperature is increasing. Instead Data retention voltage is increasing with increase in temperature due to the leakage currents in the device. The increase in the data retention voltage is about 46% in 6T SRAM and about 22% for both 7T and 8T SRAM cell.

Table 6.3: Data Retention Voltage vs Temperature in 8T SRAM

Temp (°C)	Voltage(mV)				
	SS	SF	FS	TT	FF
-20	4.4	11.28	2.97	5.83	7.3
0	5.69	13.16	3.92	7.28	8.85
20	7.37	15.24	5.17	9.07	10.81
40	8.98	16.96	6.44	10.77	12.67
60	10.69	18.61	7.89	12.59	14.65
80	12.52	20.21	9.54	14.53	16.68
100	14.44	21.79	11.4	16.55	18.75
120	16.47	23.38	13.44	18.63	20.84

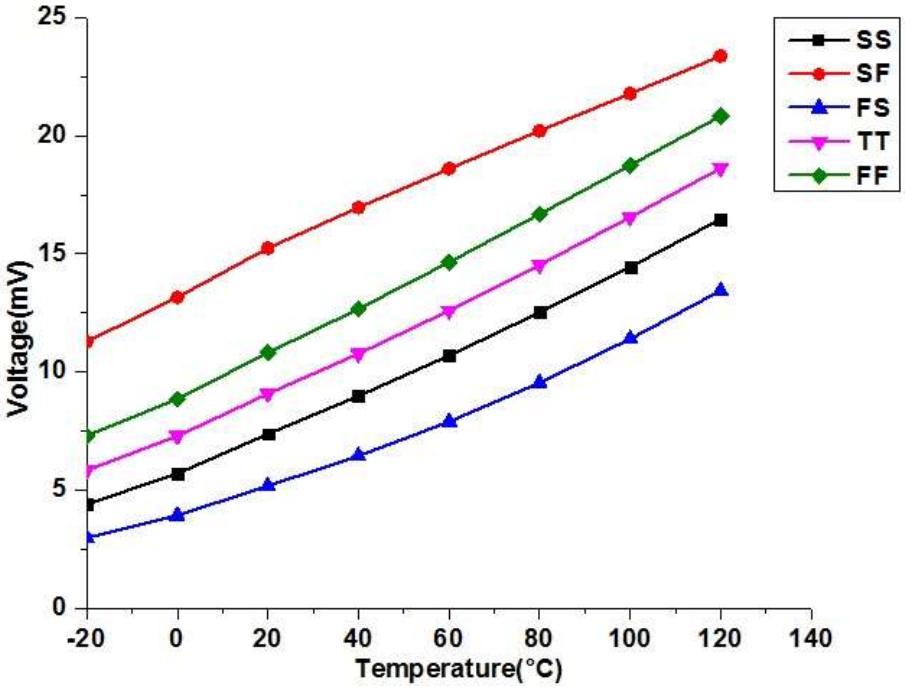

Figure 6.5: Data Retention Voltage vs Temperature in 8T SRAM

When the device is in TT Corner as the transistors are in typical mode and in FF Corner as both the transistors are in stronger mode there is similar change in Data retention voltage in device as the temperature increases in both the cases there is an increase of 31% for both 7T and 8T SRAM‘s and an increase of around 58-60% in 6T SRAM cell as the temperature increase from -20 ^{O}C to 120 ^{O}C.

Table 6.4: Leakage Power vs Process Corners

Process Corners	LEAKAGE POWER(nW)			
	6TSRAM [161]	6T SRAM	7TSRAM	8TSRAM
TT	44.34	6.85	5.3	6.8
SF	42.20	7.85	4.5	5.8
FS	47.00	6.79	6.1	7.2
SS	29.12	3.85	1.7	2.83
FF	66.72	17.81	19.5	20.3

In Table 6. 4, leakage power analysis for different SRAM topologies 6T, 7T and 8T are shown and it is evident that 7T SRAM at all corners has least leakage power. Figure 6.6 shows a graphical comparison of SRAM cell leakage power at different corners and it concludes that the leakage power is minimum when the device is operated in SS Corner in all 6T, 7T and 8T SRAM cells. At TT corner also the leakage power loss is lesser compared to SF, FS and FF corners. So in order to have less leakage power the idle mode of operation is TT corner as we cannot operate the device in SS corner as the speed of the device is also an important constraint and in this corner the device is operated in slow-slow configuration. And also in SF corner though it is less still the operation of the device is not proper as both the devices are not operated evenly.

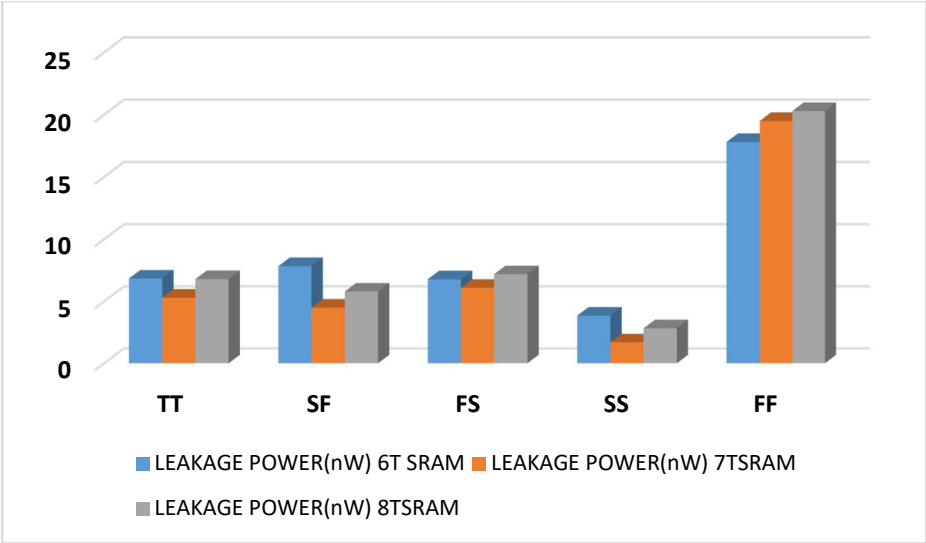

Figure 6.6: Leakage Power vs Process Corners

6.3 Cell Area and Layout

The two utmost significant assets of a memory collection are its functionality and density. Functionality is certain for bulky memory groupings provided that adequately enormous design limitations, which are decided by the supply voltage, device sizing and slightly, by the assortment of transistor threshold voltages. Even though upsizing the transistors upsurges the noise limits, it surges the cell area thus sinking the density.

Here the layout of 7T, 6T, 8T SRAM with the final design along with the leakage reduction circuit is drawn using cadence virtuoso layout editor and DRC check is done. The layouts are shown in Figures 6.7,6.8,6.9 respectively. The area is calculated according to the design rules where the area of 6T SRAM is 1.079 $\mu M^{2,}$ area of 7T SRAM cell is 1.25 μM^2 and the area of 8T SRAM cell is 1.28 μM^2 as shown in Table 6.5.

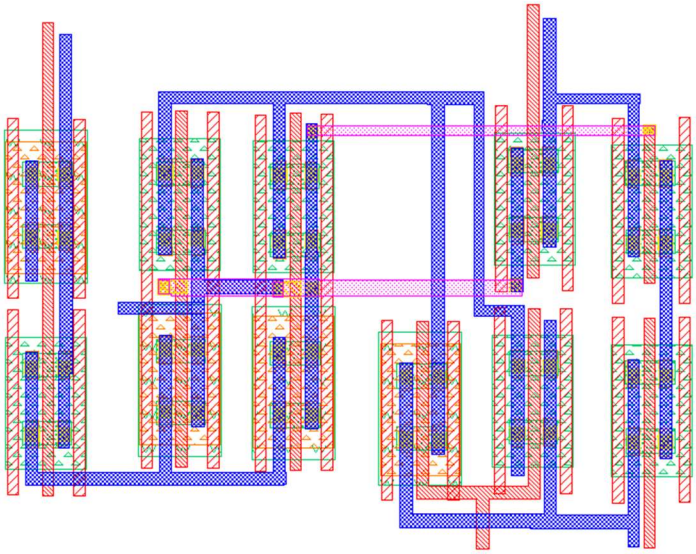

Figure 6.7: Layout 7T SRAM Cell

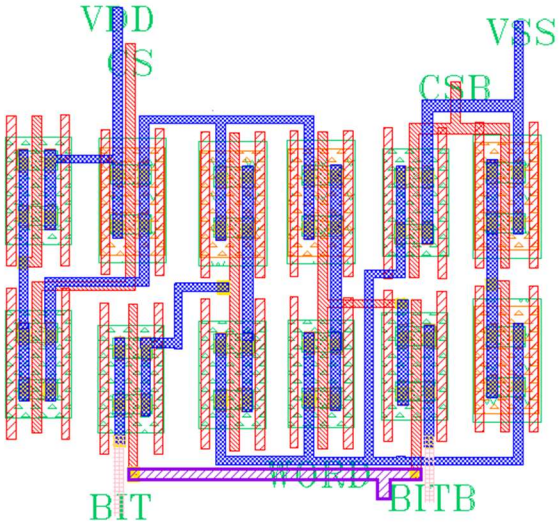

Figure 6.8: Layout of 6T SRAM cell

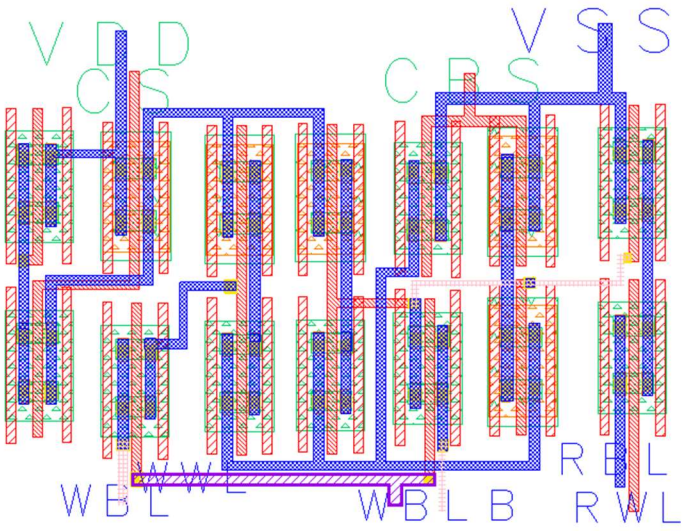

Figure 6.9: Layout of 8T SRAM cell

Table 6.5: Area of SRAMs

S.No	SRAM	Area(μM^2)
1	6T	0.83*1.3
2	7T	0.83*1.51
3	8T	0.83*1.55

6.5 Chapter Conclusion

In this Chapter the process variation analysis is done for 6T, 7T and 8T SRAM cells related to the data retention voltage is minimum at low temperature and becomes constant as temperature increases and increases with the temperature. In FS mode the Data retention voltage is less for all three configurations, whatever voltage shown here is the leakage voltage and also it is found that whenever the device is operated in TT corner it has least leakage power compared to all other corners as both the transistors in this configuration operate evenly. Among all SRAM topologies 7T SRAM cell based on 18nm FinFET technology, have shown minimum power consumptions at all TT, SF, FS and FF corners. The layout of 6T, 7T, 8T are drawn and found the area to be 1.07, 1.2533, 1.286μM^2 respectively.

Chapter-7

Conclusion and Future Scope

7.1 CONCLUSION

In this thesis an 18nm FinFET based SRAM is designed. Here as the device is in 18nm which is a very less dimension there will be problems associated with the reduction of size which leads to leakage currents because of which the device performance is degraded.Inorder to address the problems associated with device scaling here a double gated FinFET is proposed which reduces the problems such as short channel effects, leakage up to a maximum extent. The other advantages of using FinFET is its fabrication process which is easier in comparison with MOSFETs and also the device packaging etc.

In this thesis better a better understanding of FinFET device is provided and also a FinFET based SRAM cell with low power and high stability is designed which also low leakage in comparison to CMOS has based SRAMs.The FinFET based SRAM is designed in 18nm using cadence virtuoso and better simulation results are obtained when compared to SRAM designed in CMOS 45nm technology.Inorder to reduce the leakage currents a SRAM model has been proposed that reduces the leakage currents drastically and the SRAM has better performance in comparison with CMOS based SRAM.

Here in the beginning the primary focus was to select the better SRAM cell for which the simulations of leakage current, power dissipation, leakage currents and SNM ratios of 6T, 7T, 8T, 9T, 10T and 12T SRAMs in both CMOS and FINFET technology were done. And it is found that the 18nm FinFET based 7T SRAM has better results with leakage current of 50.26nA, power dissipation of 35.22nW, power consumption of 11.9nW and SNM of 291mV.

Further for reducing the leakage different leakage reduction techniques were tested and found that the SVL technique has better performance in reducing the leakage. When this SVL technique is applied to FinFET based 7T SRAM cell it reduced the leakage current by 84.9% and the leakage power by 87.3%.This reduction in leakage is because of the USVL and LSVL which individually contribute by reducing the subthreshold leakage and also the gate tunneling leakage .

Later the device performance is verified by different parametric variations where the circuit is tested at different temperatures and with the transistors operated in different process corners. It is found that with increase of temperature the data retention voltage is also increasing and in TT mode of operation the device has better performance.

The proposed design is widely used in different applications such as Processors, Signal processing, mobile technology and body area networks in portable biomedical devices etc.

7.2 FUTURE SCOPE

We have given the results based on the research, but since no work is complete as there is lot of scope for improvising .So here are some possibilities of implementation which can be considered in future

- Here the analysis of FinFET at the circuit level is done further device level modifications can be done considering different materials.
- Here a FinFET based SRAM is designed in 18nm and simulated further the technology can be scaled beyond 18nm.
- A significant reduction in leakage current was possible with the proposed reduction techniques in future when technology is scaled further new reduction techniques will be required to reduce leakage.
- Apart from the discussed leakage reduction techniques there may be some more techniques which can be considered.
- The process variation is done only with respect to temperature and process corners, other parameters can also be considered when working at device level.
- The layout was done and DRC was checked so further LVS can be done.
- A more efficient Low power SRAM can be designed by reducing the supply voltage and also by adding an extra sense amplifier in the circuitry to boost the performance.

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Research Publications

1. "Leakage Reduction in 18 nm FinFET based 7T SRAM Cell Using Self Controllable Voltage Level Technique", Wireless Personal Communications -2020**(SCI).**
2. "Design of Low Power 7T SRAM Cell for portable Biomedical Applications", International Conference on Smart Electronics and Communication (ICOSEC)-2020 **IEEE Digital Explorer (Scopus).**
3. "Comparative Analysis of Leakage Power in 18nm 7T and 8T SRAM cell Implemented with SVL Technique", International Conference on Intelligent Engineering and Management (ICIEM)-2020 **IEEE Digital Explorer (Scopus).**
4. "Design of 7T SRAM cell using FinFET technology", Advanced VLSI Design and Testability, CRC Taylor and Francis Group-2020 **(Scopus).**
5. "Implementation of CMOS SRAM Cells in 7, 8, 10 and12-Transistor Topologies and their Performance Comparison", International Journal of Engineering and Advanced Technology-2019**(Scopus).**
6. "Performance Comparison of 6T, 7T Bit-Line SRAM Cell on 18 nm FinFET with CMOS Technology" Journal of The Institution of Engineers (India): Series B (IEIB)-Under minor review **(Scopus).**
7. "Process Evaluation in FinFET based 7T SRAM cell', Analog Integrated Circuits & Signal Processing (ALOG)-Under Review **(SCI).**
8. "Comprehensive Analysis of SRAM Cell Architectures with 18nm FinFET for Low Power Applications", Journal of Silicon, Springer Nature-Under Review **(SCI).**