DESIGN OF A NARROW BAND GAP MATERIAL HETEROJUNCTION TUNNEL FIELD EFFECT TRANSISTOR WITH IMPROVED SHORT CHANNEL PARAMETERS

A Thesis

Submitted in partial fulfillment of the requirements for the

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By

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Supervised By

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DECLARATION

I hereby declare that the work being presented in this thesis report entitled "**DESIGN OF A NARROW BAND GAP MATERIAL HETEROJUNCTION TUNNEL FIELD EFFECT TRANSISTOR WITH IMPROVED SHORT CHANNEL PARAMETERS**", is an authentic record of my own work carried out in fulfilment of requirements for the award of degree of Doctor of Philosophy in Electronics & Electrical Engineering at Lovely Professional University, Phagwara under the supervision of **Dr. Sanjeet Kumar Sinha**, Associate Professor, Department of Electronics and Communication Engineering. The matter presented in this thesis has not been submitted elsewhere in part or fully to any other University or Institute for the award of any degree.

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This is to certify that **Irfan Ahmad Pindoo (Registration Number: 41700104)** has completed objective formulation of his thesis titled, **"DESIGN OF A NARROW BAND GAP MATERIAL HETEROJUNCTION TUNNEL FIELD EFFECT TRANSISTOR WITH IMPROVED SHORT CHANNEL PARAMETERS"** for the award of degree of Doctor of Philosophy in Electronics & Electrical Engineering at Lovely Professional University, Phagwara under my guidance and supervision. The matter presented in this thesis has not been submitted elsewhere in part or fully to any other University or Institute for the award of any degree.

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ABSTRACT

The device dimensions have now crossed the nanometer scale, thanks to continuous advances in complementary metal oxide semiconductor (CMOS) technology. This miniaturization has been made possible with the scaling of the device parameters as per Dennard's rule of scaling. As the size of the transistors go below 100 nm due to the scaling, it becomes a tough task for a transistor to switch the state form OFF to ON or vice-versa, without the significant power dissipation. Further, some short channel effects are also getting introduced like a drain induced barrier lowering, leakage current, subthreshold slope conduction, etc. into a picture. Thus, it becomes difficult to switch from OFF state to ON state while maintaining smaller supply voltages. This is mostly due to a metal oxide semiconductor field effect transistor's physical limitations (MOSFET). The current transport mechanism in a MOSFET is based on the thermal injection of electrons. Thus, it can be concluded that the simple miniaturization of transistors with the continuous CMOS scaling will not help in improving energy efficiency. This has compelled researchers to explore the new architectures with better performance and also explore new materials, e.g., non-silicon and others, so as to overcome the limitations available in the conventional MOSFET technology.

Tunnel Field Effect Transistors (TFET) have been presented by researchers as a potential device that can replace MOSFETs in future. TFET functions on the basis of band to band tunneling phenomenon, rather than the thermal generation of electrons. So, it becomes possible to achieve a steeper subthreshold swing, thus removing limitation of a conventional MOSFET. However, simple silicon based p-i-n gated TFET structures suffered from low ON current (I_{ON}) and higher subthreshold swing. To overcome these limitations, new architectures, materials have been explored in the past. Double gated TFET structure with high-k dielectric materials were used to enhance the performance characteristics of an ON current in TFETs. Addition of the pocket layer at the source has also been earlier to boost the ON current in TFETs. Higher source doping have also been suggested by many to increase ON current by many folds. However, leakage current also rise thus putting a constraint on this method. Heterojunction structures have also been

explored, where low energy band gap materials are used at the source region. This increases the ON current as the effective band gap reduces thus allowing higher band to band tunneling. The materials being explored are InGaAs, InP, GaAs, GaAsSb, InAs, etc. Such structures have been successful in achieving high ON current along with a steeper subthreshold swing. However, the poor quality interface, trapped charges in the oxide layer, and other defects still pose some serious challenges during the fabrication of such structures.

The other limitation in TFET structures is the ambipolar current. In a TFET, unlike a MOSFET, the drain and source terminals are oppositely doped. Thus, if a positive gate to source V_{GS} voltage is applied, tunneling would happen at the gate-source junction. But, if the negative gate to source V_{GS} voltage is applied the tunneling would happen at the drain side as well. The leakage current would get increased. So, to overcome this limitation in TFETs, several device architectures have been proposed earlier, such as, gate-drain overlap, low-drain doping, asymmetry between source and drain. Although such structures have reported the reduction in the ambipolar transport, but the low ON current would be the trade-off parameter.

Furthermore, it was learnt that tunnel FETs can be used in several applications like A/D converters, memories, low power analog circuits, sensors, and various other application areas. However, due to its ability of operating a lower supply voltages and obtaining higher sensitivity have compelled researchers to explore TFETs for the use of biosensors in the bio-medical field for the early disease diagnosis. This is done by the study of the biomarkers while screening the patient for various diagnostic tests. Many of the TFET based biosensors have been reported by the researchers. However, the structures like ion sensitive field effect transistor, conventional DG TFET experience performance degradation due to the short channel effects and ultra sharp doping profile.

Based on the prospective of the tunnel FETs and the major limitations and challenges that researchers have faced, we have formulated the objectives of our thesis. An effort has been made to enhance the overall performance of the device by addressing its limitations. The

brief description regarding the objectives and the work done to achieve the objectives have been summarized as under:

Objective 1: Achieve high I_{ON}/I_{OFF} ratio using narrow band gap heterostructure junction TFET

TFETs are considered to be one of the strong candidates which can replace MOSFETs in the future, so it is incumbent to ensure that TFETs have an ON current of the order of 100 μA/μm, while maintaining (I_{ON}/I_{OFF}) ratio of around 10^6, for lower gate voltages. However, the limitation of TFETs is that due to its inherent physical phenomenon of band to band tunneling (BTBT), it supports low ON current. Therefore, the conventional TFET structures suffer with the major limitation of low ON current. In order to overcome this disadvantage, a lot of research is now-a days focused on boosting the ON current of the TFET.

For achieving this objective, the aim has been to explore all the heterojunction TFET devices. With literature review, it was concluded that SiGe would be a better choice when compared to the other material like InGaAs, InP, etc., as these materials suffer from interfacial defects, which ultimately degrades the subthreshold swing of the device. Moreover, it was found that the OFF current was also high for SiGe based device. Then the techniques like, hetero dielectric layer and the use of buried oxide layer was explored to improve the performance of our proposed devise. The device being proposed demonstrates a better results in terms of the $\frac{I_{ON}}{I_{OFF}}$ ratio. The value comes around 3.72×10^{10} which is considerably high, when compared to the most of the existing architectures.

Objective 2: To decrease the subthreshold slope for steeper transition of the device

The current flows in the MOSFET on the basis of thermally generated electrons. The sub threshold swing is the parameter that indicates the steepness with which the given transistor turns ON from the state or vice versa. Once the gate voltage on which a device operates becomes very low, it means that the transition is required to be very sharp. However, it has been observed in the MOSFET technology that the subthreshold swing lesser than 60

mV/decade is not achievable. Wile as in the practical circuits, it is often worse than 60 mV/decade, and can rise even up to more than 100 mV/decade. One of the excellent features of TFET is that it is possible that the subthreshold swing can be achieved as lesser than 60 mV/decade due to its different current transport mechanism which is based on band to band tunneling (BTBT).

In order to achieve this objective, we have explored different techniques used by researchers to make the transition steeper from ON to OFF state or vice versa. For our device, since the material being used was heterojunction, so a large band gap material was used from the drain region, to reduce the OFF current, while as the lower energy band gap material was used at the source region, so that we can achieve higher tunneling at the source-channel interface region. Besides, the minimum tunneling width is also desirable for obtaining a lesser subthreshold swing. For the proposed device, average subthreshold swing has been calculated as 28.57 mV/decade.

Objective 3: Reducing the effect of short channel parameters in device performance:

Short Channel effects have proved to be a major bottleneck in the sub nanometer devices. Our aim in the research has been to minimize the parameters like drain induced barrier lowering, subthreshold conduction, etc. Although heterojunction structures provide a larger ON state current, they suffer from large tunneling leakage due to the small bandgap at short channel lengths.

To achieve this objective, energy band gap was one of the parameters on which we laid a focus upon. By default the off current in Ge based material remains high. So, we calibrated the molar fraction x of $Si_{1-x}Ge_x$ so as to optimize the values of I_{ON} and I_{OFF} of the device. Moreover, it was observed that the short channel parameter effects reduce, when the drain-source voltage is decreased. The value of DIBL obtained in our device is of the order of 3.636 mV at 50 nm length and 2.222 mV at 40 nm length. Moreover,

threshold voltage obtained at the drain current of 10^{-7} is about 0.256 V at 50 nm length and 0.248 at 40 nm length.

Objective 4: Reduction of the ambipolar current transport in Tunnel FETs

The other serious limitation in a conventional TFET is that of an ambipolar conduction. If the TFET structure is given a negative gate voltage, again due to BTBT at the interface of drain-channel, the drain current begins to flow. This phenomenon is called as ambipolar transport. This limitation restricts the use of TFETs in a complementary devices for digital applications. Our objective has been to reduce this limitation in TFETs.

For achieving this objective, the source terminal has been kept at the higher doping as compared to that of the drain terminal. A sharp doping profile on the source side was required to achieve high ON current. BTBT will be repressed by lower drain doping, when the negative gate-source voltage is being applied at the gate terminal. Besides, a buried oxide layer has also been used in our proposed device. An effort has been made to suppress the ambipolar current up to $V_{GS} = -0.3$ volts.

Objective 5: Increased Sensitivity of Tunnel FET Biosensors for biomolecules

The biosensors which were designed with MOSFET and ISFET were unable to detect the biomolecules which were positively or negatively charged. Further, the amount of current carried by ISFET is dependent on the charge density of biomolecules on the surface of the gate region. Therefore, if the size of the biomolecule is small, it cannot be detected by the FET based sensor. The situation remains the same whether the biomolecule is charged or uncharged. Moreover, the short channel effects, the scaling difficulties and the thermal injection transport mechanism of FETs degrade the performance of such sensors. Thus, the focus of the researchers is now to explore new technologies in a FET based biosensors. Tunnel FET based biosensors is on such example.

To achieve this objective, we have introduced a nano gap cavity below the gate terminal for the binding of the biomolecules. The nanogap cavity of 30 nm length has been created just below the gate terminal for the conjugation of the biomolecules. The highest $\frac{I_{ON}}{I_{OFF}}$ ratio achieved was 1.68 × 108 (with I_{ON}= 2.308 × 10^{-6} and I_{OFF} = 1.374× 10^{-14}). The results have been compared with the double gated SiGe source based heterojunction TFET and few other designs. The cavities help in conjugating biomolecules and hence detect their dielectric constants and the currents that they carry. The presence of biomolecules will cause the device's electrical parameters to change, and that would be detected by changes in the characteristics of the device. Charge density inside the cavity region and the variations in the dielectric constant reflect biomolecule conjugation. The barrier between the source and the channel is reduced when biomolecules are trapped within the cavity, therefore changes the BTBT current. Due to the introduction of biomolecules, the tunneling barrier width will decrease as the dielectric constant increases. This will lead to an increase in an ON current.

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Irfan Ahmad Pindoo

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I_{ON}	On current
I_{OFF}	Off current
V_{Th}	Threshold Voltage
V_{GS}	Gate to source voltage
L_g	Gate length
C_{ox}	Oxide capacitance
P_S	Static power dissipation
P_D	Dynamic power dissipation
V_{DD}	Supply voltage
C_L	Load capacitance
α	Switching probability
f	Device operational frequency
e	Electronic charge
h	Planck's constant
$f_s(E)$	Source fermi energy function
$f_d(E)$	Drain fermi energy function
T_{tot}	Transmission function
ħ	Reduced Planck constant
m^*	Reduced mass of an electron
E_g^*	Effective energy band gap
$\Delta\Phi$	Energy overlap window
$\in_{Si}$	Electrical permittivity of silicon material
$\in_{ox}$	Electrical permittivity of oxide layer
t_{ox}	Oxide thickness
t_{Si}	Silicon body thickness
I_D	Drain current

Ψ	Wave function
$\boldsymbol{\Psi}(x)$	Denotes the spatial component of $\boldsymbol{\Psi}(x,\mathrm{t})$ which is a function of only x
$\boldsymbol{\Psi}(t)$	Denotes the temporal component of $\boldsymbol{\Psi}(x,\mathrm{t})$ which is a function of only t
$D(E)$	Density of State
T	Temperature
k	Boltzmann constant
SS	Subthreshold swing
$f_F(E)$	Fermi–Dirac distribution function
G^{BB}	Generation rate
μ	Mobility
$E_{\perp}$	Transverse component of the electrical field.
N_S	Doping at the source region
N_D	Doping at the drain region
N_{ch}	Doping at the channel region
E	Electrical field
C_D	Depletion capacitance
$V_{D_{SAT}}$	Supply voltage during saturation mode
$V_{D_{LIN}}$	Supply voltage during linear mode
$V_{T_{LIN}}$	Threshold voltage during linear mode
$V_{T_{SAT}}$	Threshold voltage during saturation mode
ϕ	Gate work function
C_{GS}	Gate-source capacitance
C_{GD}	Gate-drain capacitance
C_{GG}	Total gate capacitance
f_T	Cut-off frequency
GBP	Gain Bandwidth product

g_m	Transconductance
g_m/I_{DS}	Device efficiency
V_T	Thermal voltage

LIST OF ABBREVIATIONS

BOX	Buried oxide layer
BTBT	band to band tunneling
CMOS	complementary metal oxide semiconductor
DD	Drift-diffusion
DGTFET	Double gated Tunnel Field Effect Transistor
DIBL	drain induced barrier lowering
GBP	Gain-bandwidth product
IC	Integrated Circuit
JLTFET	Junction less Tunnel Field Effect Transistor
LTFET	Lateral Tunnel Field Effect Transistor
MOSFET	metal oxide semiconductor field effect transistor
NEGF	Non energy green function
NMOS	N channel metal oxide semiconductor
PDA	Personal Digital Assistant
PMI	Physical Model Interface
PMOS	P channel metal oxide semiconductor
QC	Quantum confinement
RF	Radio frequency
SCE	Short channel effects
SOI	Silicon on Insulator
SRH	Shockley-Read-Hall
SS	Subthreshold swing
TCAD	Technology computer-aided design
TFET	Tunnel Field Effect Transistor
VLSI	Very Large Scale Integrated Circuit
VTFET	Vertical Tunnel Field Effect Transistor

CHAPTER 1: INTRODUCTION

Over the last four decades, electronics have evolved from bulky vacuum tubes to lighter and lower-cost bipolar junction transistors, unipolar FETs, and now CMOS technology. The reason that one technology was superseded by the other was when their power consumption became excessively high [1, 2]. By increasing power density and the number of transistors in a given IC, CMOS scaling faces several challenges. Therefore, the need arises to explore new emerging devices that can improve the limitations of CMOS technology and can be seen as a future and successor of conventional MOSFET [3, 4]. The methods of scaling are by decreasing gate length L_G and increasing oxide capacitance C_{ox} such that the current I_{ON} increases. However, even using optimized materials, sometimes result in short channel effects.

1.1 Basics of Conventional MOSFETs

A MOSFET is the structure consisting of the base material as a silicon called as body or substrate. It is the foundation over which whole device would be constructed. Over the substrate, a thin silicon dioxide layer is deposited over the material. The drain and the source are being doped with the same type of the material. The source and the drain terminals are attached through the metallic contacts. The gate terminal is made up of polysilicon and remains insulated from the channel due to the SiO_2 layer. MOSFETs can be of two categories: n-channel MOSFET and p-channel MOSFET. The drain and source regions of an n-channel MOSFET are heavily doped with n+ type dopants, as a result the current conduction would be due to the electrons as charge carriers. While as, in the p-channel MOSFET, The drain and source are both heavily doped with p+ style dopants., as a result the current conduction would be due to the holes as charge carriers [5, 6]. The cross sectional diagram provided in figure 1.1 represents both N-channel and P-channel MOSFETs.

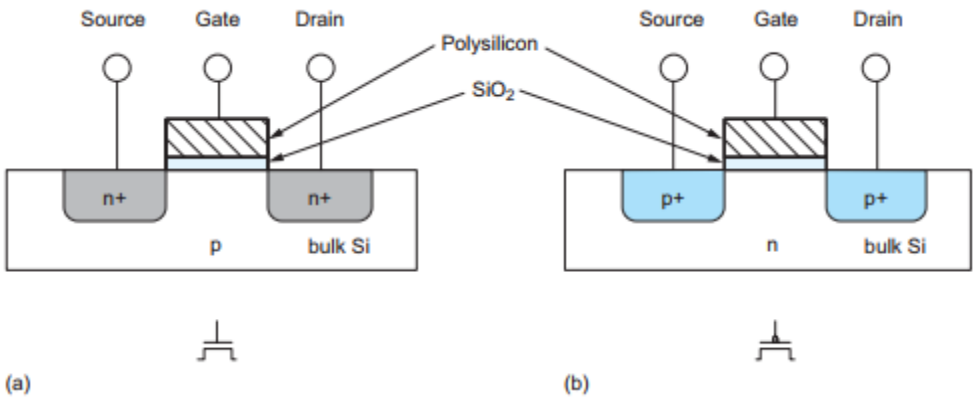


Figure 1.1. MOS transistor (a) n-channel (b) p-channel

The current conduction from source terminal to drain is controlled by the application of the gate-source voltage. The p-type substrate is used in NMOS transistors and is usually connected to the ground. The voltage at drain side would be greater as compared to the source. Due to the absence of the channel, no current would flow from source to drain if the gate-source voltage was zero. Therefore, we assume the transistor is turned off. If the voltage at gate is gradually increased, an electric field is developed across the channel, as a result free electrons are attracted at the Si-SiO_2 interface. When a gate voltage becomes sufficiently high, a situation is created where the number of free electrons available in the channel is greater than the number of holes in the p-substrate. This phenomenon is referred as an inversion. Now that, the channel has become N-type electrons can move from the source side to the drain terminal, and there would be rise in the drain current.

Similarly the n-type substrate of a PMOS transistor is normally connected to the drain voltage. The voltage at drain side would be lesser than that of the source. If the gate-source voltage is zero or even at the positive voltage, then no current would travel from source to drain, due to absence of the channel. Thus, we assume that the transistor has turned off. When the voltage applied at gate is in negative (lesser than 0 volt), an electric field is developed across the channel, as a result free holes are attracted at the Si-SiO_2 interface. When a gate voltage becomes sufficiently negative in magnitude, a situation is created where the amount of free holes at the channel outnumbers the electron numbers available

in the n-substrate. Again, the channel has become inverted (p-type), it would be feasible for holes to move from the source to the drain terminal, and drain current starts to rise.

Thus, whenever the gate voltage applied is higher than the MOSFET's threshold voltage, a strong channel inversion occurs below the gate. The material used to build the MOS structure determines the threshold voltage. There occurs a deposition of holes in PMOS and electrons in NMOS below the gate. Then, the drain voltage sweeps the charge carriers, and hence the current flows in the MOSFET.

One of the applications of the MOSFET is that, they act as a switch when operated under cut-off and saturation regions. As an ideal switch, it is expected that when a transistor is turned off, it does not dissipate any power, and when turned on, it would deliver a large amount of current. However, the MOSFET used in practical applications exhibit a small leakage current as well, thus even when turned OFF, some power would get consumed. It is referred as static power dissipation (P_s), and is represented by:

$$P_S = V_{DD} I_{OFF} \tag{1.1}$$

In the above equation, V_{DD} represents the supply voltage and I_{OFF} represents the leakage current. Besides, When a MOSFET transitions from ON to OFF state or vice versa, a significant power gets consumed as well. This type of power consumption is called as dynamic power dissipation (PD) and is given by the following relation:

$$P_D = V_{DD}^2 C_L \alpha f \tag{1.2}$$

In the above equation, V_{DD} represents the supply voltage, f denotes operational frequency, C_L is the load capacitance and α is the switching probability. C_L represents the combination of the input capacitances and interconnect capacitances [5].

1.2 CMOS Scaling

CMOS scaling is the process in which the dimensions of the MOSFET are decreased in such a manner that the functionality of the device does not get affected. Scaling MOS transistors is the process of reducing the overall dimensions of devices as much as

technology allows while maintaining the geometric ratios similar to as in larger devices. The scaling theory was put forward by Dennard in 1974 [7].

Until recent past, the main aim of researchers in the MOSFET technology has been to miniaturize the size of the transistors, so that more and more components can be accommodated on a given area. This would also increase the functionality of the given chip, as the number of operations it can perform would increase as represented in figure 1.2. This exponential trend in miniaturization was predicted by G. Moore, which states: "After every 18 months, the number of components in an integrated circuit doubles". From the past five decades, Moore's law has stood true and this law is being seen as a benchmark of industry progress [8]. Moreover, the advantages of the CMOS scaling are that the input capacitance of the MOSFET decreases and the current driving capability of MOSFET increases. However, the constraint remains that despite the fact that the drive current of MOSFETs increases, but because of its limitation due to the short channel effects, the OFF current also rises due to the shorter gate length [9]. As a result of the increase in OFF current, an increase in the static power dissipation occurs. The aggressive pace at which the CMOS scaling is done, it is predicted by the researchers that the range of static power dissipation in conventional MOSFETs will soon surpass the range of dynamic power dissipation.

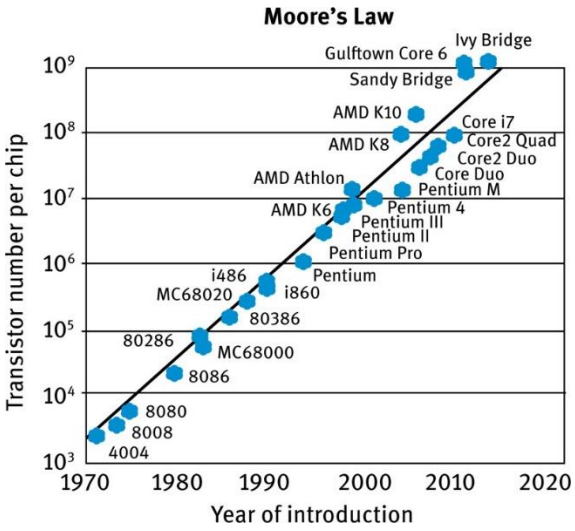


Figure 1.2 Illustration of Moore's law [10]

The other major limitation of static power dissipation is that it would drain large power from the battery even when the device is turned OFF. This would result in the draining of the battery although the device is not in use. For a handheld devices like PDA, smartphones, etc., it would be detrimental in terms of their battery performance. Furthermore, the static power dissipation would also result in the heat getting produced in the IC resulting in the temperature rise, although the gadget might have been optimized for the best performance with respect to the ambient room temperature. Equations (1.1) and (1.2) provides us some parameters with which the power dissipation could be reduced. However, the fundamental limitation of MOSFET is that: to increase current by tenfold, around 60 mV of voltage is required (ideally). This constraint occurs due to the Maxwell-Boltzmann distribution, and is more popularly referred as "Boltzmann tyranny". It is important in the MOSFET to achieve the current in the range of around ($\sim 10^4$ to 10^6) so that OFF state can be distinguished from ON state. Thus, accordingly we can say, that the minimum amount of supply voltage required would be $60 \times \log (10^6) = 360$ mV. This results also indicates that if the supply voltage is scaled aggressively to a smaller value, it would be extremely difficult to distinguish between the OFF-ON switching. This would prevent the MOSFET to act as a switch. Therefore, we can conclude that due to the "Boltzmann tyranny" the conventional MOSFETs cannot be used as a switch at ultra-low supply voltages.

1.3 Short Channel Effects in MOSFET

The reasons for the occurrence of short channel effects in the MOSFET are as follows: (1) Limitations on electron drift characteristics (2) When the channel length is shortened, the threshold voltage changes. By definition, a short channel device is one in which the channel length and the depletion region thickness is almost off the same order in magnitude [11, 12]. As the channel length decreases, the lateral electrical field increases. For lower field values, the drift velocity is directly proportional to the electrical field, but as the electrical field increases, it begins to saturate. It is known as velocity saturation, and has a major impact on short channel MOSFETs' current voltage characteristics. [13-15].

1.3.1. Drain Induced Barrier Lowering Effect

In the long channel MOSFET, the source to drain channel is exclusively controlled by the gate voltage. Barrier height at source to channel modulates the gate voltage, causing the electrons to drift from the source to the drain. But, due to CMOS scaling, the channel length is shortened aggressively, thus the drain-channel and the source-channel interface interact with each other. So the gate voltage regulates the height of the barrier between the source and the channel. The electron energy levels would be reduced, as well as the source to channel barrier height as shown in figure 1.3. This leads to the phenomena called as drain induced barrier lowering (DIBL) effect. The result would be an increase in the leakage current [16-18]. This effect is not so prominent in long channel devices simply because there is no interaction between the two depletion regions.

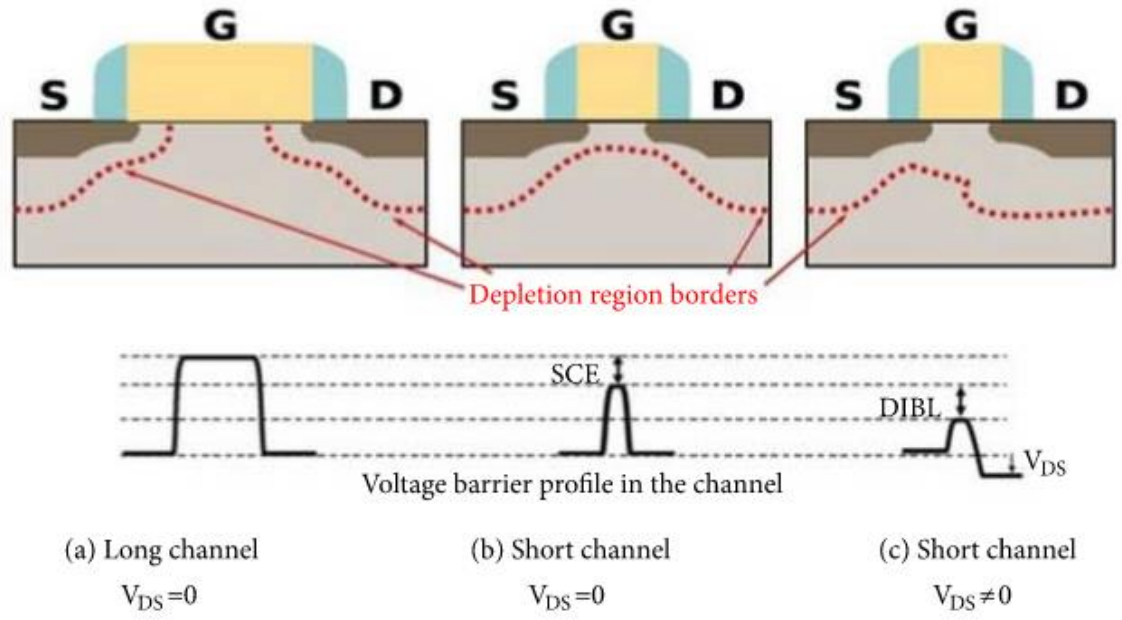


Figure 1.3 DIBL effect in MOSFET [19]

1.3.2. Threshold Voltage Roll-off

Because of the heavy doping at drain and source regions of MOSFET, there is an overlap with the p-channel substrate. Since the gate length has already been shortened due to the scaling, so the width of the depletion junctions become significant. As a result, the channel is not any longer solely controlled by the applied gate voltage. Besides, the control over

the charge on the channel by the gate voltage also reduce. In comparison to an undepleted MOS capacitor, the voltage required to invert the channel is significantly lower. The "threshold voltage roll-off" is a well-known short channel effect that results in a decrease in threshold voltage as gate length decreases [20].

The potential barrier is decreased although gate-source voltage is less than the threshold voltage, allowing current to flow across source and drain. The subthreshold current ($V_{GS}<V_{T0}$) is the current that flows in the channel under such conditions. The approximate equation for subthreshold current is given by:

$$I_D(weak) = I_{ON} e^{(V_{GS}-V_{ON}).\left(\frac{q}{nkT}\right)} \tag{1.3}$$

From the equation, it can be identified that the subthreshold current has the exponential dependence on both the drain and the gate voltages. A lower V_T would mean significant rise in the subthreshold leakage current. Thus, if the threshold voltage roll-off occurs, the OFF current would increase exponentially. This would decrease the I_{ON}/I_{OFF} ratio significantly as well [21].

1.3.3. Boltzmann Tyranny

A steep transition is required from ON to OFF state in the current, and vise - versa, for any device to act as a switch. However, as discussed at the beginning of the chapter, a fundamental limit for the rate at which current changes in accordance to the applied gate voltage is characterized by thermal current transport across the source–channel barrier height in case of a MOSFET.

An ideal MOSFET switch, should do a smooth and abrupt transition from ON state to OFF state, when voltage at gate terminal is lesser to the threshold voltage and should go from OFF state to ON state, when the voltage at gate side is higher than the threshold voltage as shown in figure 1.4. Subthreshold swing is the important parameter which measures the degree of abruptness of the transition from ON state of the transistor to the OFF state, and vice versa. It represents the minimum quantity of gate voltage needed to ten-fold the drain current [22].

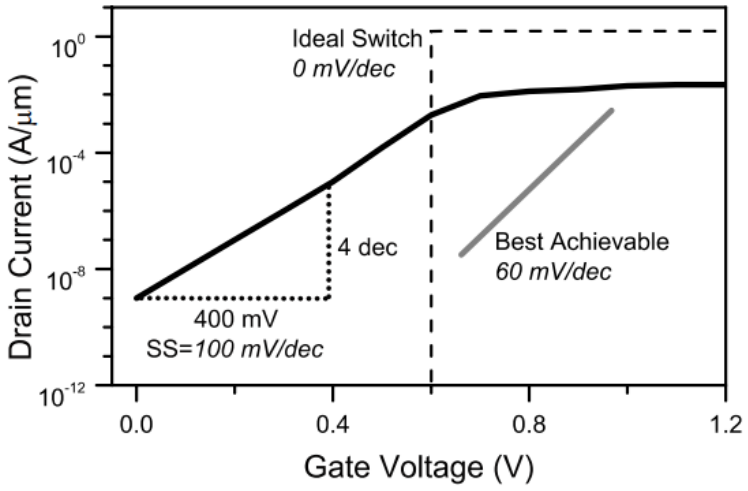


Figure 1.4 A typical NMOS switch's characteristics and a comparison to an ideal switch (shown in dashed line)

1.4 Evolving FET Devices

In the earlier discussion, we have explained the basics of MOSFET, the various short channel effects that arise because of the continuous scaling, the limitation in terms of the thermal injection mechanism of current transport in MOSFET, unable to have a sharp doping profile, etc. All these shortcomings prevents the use of MOSFETs at sub-10 nm scale regime. Thus, researchers have explored the alternate technologies based on different mechanisms like BTBT, impact ionization, etc. to improve performance [4, 23, 24].

This in turn provides a lot of scope for the researchers to explore the new fields and develop the novel technologies in order to possibly replace conventional MOSFETs in future. TFET is one such novel device which can be explored with respect to its characteristics and the performance and would prove as one of the strong candidates to substitute conventional MOSFET in future.

CHAPTER 2: TUNNEL FILED EFFECT TRANSISTORS

2.1 Basics of Tunnel Field Effect Transistors

2.1.1. TFET Structure

The basic TFET is a gated reverse biased P-I-N structure. Both N-type, as well as P-type TFETs, are illustrated in figure 2.1. The opposite doping of drain and source terminals is most distinguishing feature of TFETs. This feature is in contrast to a conventional MOSFET where drain and source terminals are interchangeable due to the same doped structure. The breakdown of a reverse biased p-n junction occurs due to two mechanisms: impact ionization and BTBT. Both require high electrical field and induces a significant current change corresponding to a small change in the voltage. Here we explore steep slopes by studying TFETs. As evident in the figure, for a p-type TFET p^+ doping is done from drain side and n^+ doping is done from source side. For n-type doped, the type of dopant is reversed for the drain and the source. Moreover, the channel is formed of an intrinsic semiconductor or low doped n-type or p-type semiconductor.

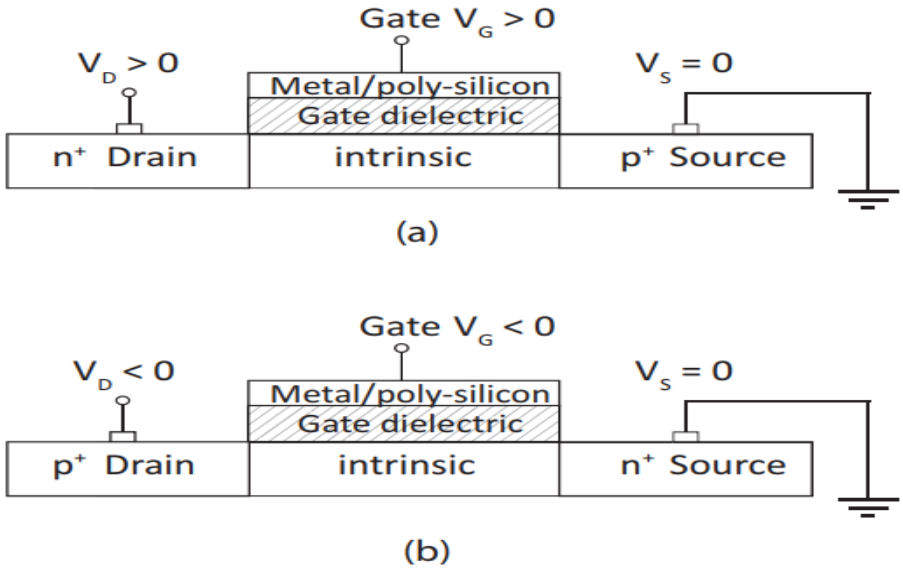


Figure 2.1 Biasing method and structure of: (a) n- TFET (b) p- TFET

Figure 2.1 represents the biasing methods of n-TFET and p-TFET. The source is grounded in an n-TFET, and the drain and gate terminals are both provided a positive voltage. Electrons are the dominant charge carriers inside, and flow of electrons is from the source terminal toward the drain terminal along the channel. While as in p-TFET, negative voltage is given to drain and gate terminals after source being grounded. Holes are the dominant charge carriers inside, and flow of electrons is from the source terminal toward the drain terminal along the channel. Both the types of TFET have a current transport mechanism being directed by band to band tunneling phenomenon (BTBT).

There are a few issues with this conventional design, like ambipolar behavior and weak drive current when compared to CMOS technology. To improve the parameters of a TFET, a double gate TFET (DGTFET) is implemented. n^+ doping is done from drain side and p^+ doping is done from source side. To suppress ambipolar behavior of TFET the source terminal is kept at the higher doping as compared to that of the drain terminal. Moreover, to attain greater ON current, a sharp doping profile on the source side is needed. The silicon body thickness is kept small to increase ON current. Since the gate is present on the two sides of the structure, its control over the channel is improved. The tunneling current improves nearly by the double as compared to single gated lateral TFET structure [25-28].

2.1.2. TFET Operation

The band diagrams given in figure 2.2 represents the OFF condition and the ON condition for n-type TFET. The TFET is said to be in the OFF condition if gate to source voltage is nearer to zero. Valence band in the source lies below the channel's conduction band. In this case, BTBT is inhibited resulting in extremely low drain current. As the gate voltage is increased gradually, the carrier density gets modulated due to the gate voltage which in turn pushes down the conduction band in the channel. When the gate voltage becomes sufficiently high, bending of the band occurs at the source, as a result, the channel's conduction band gets aligned with the source's valence band. Electrons from source's valence band start to tunnel to the channel's conduction band. The positive drain bias voltage further sweeps these tunneled electrons towards the drain terminal. This explains the operation of n- type TFET.

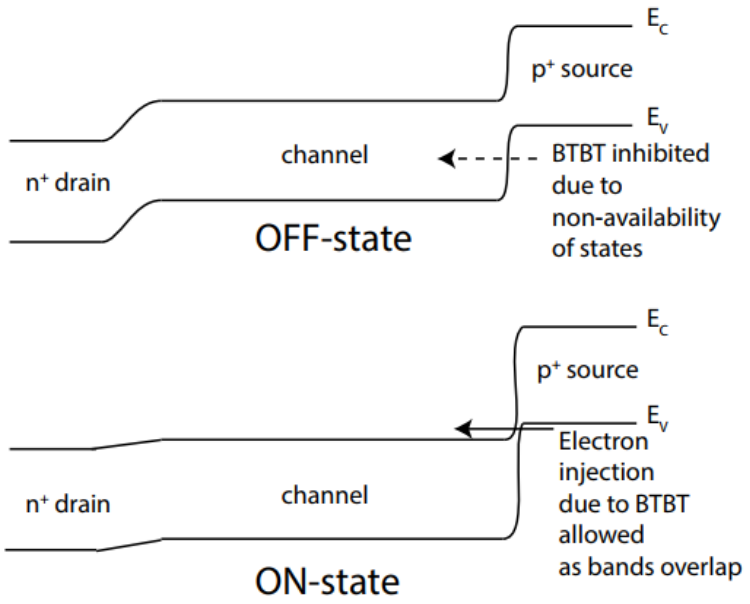


Figure 2.2 Representation of an OFF state and ON state in n-type TFET.

It's worth noting that, unlike MOSFETs, TFETs are ambipolar devices. Hence, if the negative voltage is applied then the behaviour of the device would be like holes behaving as the dominant charge carriers essentially making the device p-type.

When a TFET is turned OFF, all the drain voltage drops across channel region and across the channel to drain and source to channel depletion region widths. While as, when the TFET is turned ON due to the sufficient amount of gate to source voltage, the channel resistance is significantly reduced as an inversion layer is formed. As a result, the large lateral electrical field is developed at interface of source-channel, thus, creating superior bending of bands at the source to channel interface. As a consequence, electrons from the source terminal would be injected into the channel region.

Landauer equation is used to obtain an equation for a drain current in a TFET analytically. It represents one-dimensional energy-conservation transport and is quite popular for nano scale integration devices. By performing an integration of the Landauer equation over the

energy range, we can obtain a drain current in the TFET [29, 30]. The electrons which are apart of energy overlap window of ΔΦ only can contribute to the significant drain current.

$$I_D = \frac{4|e|}{h} \sum_{k_{trans}} T_{tot} k_{trans} \int_0^{\Delta\emptyset} dE \left(f_s(E) - f_d(E)\right) \tag{2.1}$$

In the above equation, f_s and f_d represent the source and the drain fermi functions, and T_{tot} is the transmission function, e denotes the electronic charge while h represents the Planck's constant. Total transmission function T_{tot} is a parameter on which there is a heavy reliance of the drain current. The scattering event in the TFET can be due to tunneling and scattering within the channel, but, band to band tunneling (BTBT) is the dominant one, so we write

$$T_{tot} \approx T_{BTBT} \tag{2.2}$$

In the equation, BTBT represents tunnelling probability, and can be calculated by considering the barrier region as a triangular, as given in figure 2.3, and applying KWB approximation.

Considering a triangular barrier, the equation for the tunneling probability can be represented as:

$$P_t = \exp\left[-\frac{4\sqrt{2m}}{3\hbar F}(U_0 - E)^{\frac{3}{2}}\right] \tag{2.3}$$

In the equation, P_t denotes the tunneling probability, $(U_0 - E)$ denotes the difference between the particle's energy and the height of the barrier, m is the particle's mass, ħ is the reduced Planck constant and F is the electric field in the region. By utilizing equation (2.3), we can find out the tunneling probability of the device represented in figure 2.3 as:

$$T_{BTBT} = \exp\left[-\frac{4\sqrt{2m^*}}{3|e|\hbar F}\left(E_g^*\right)^{\frac{3}{2}}\right] \tag{2.4}$$

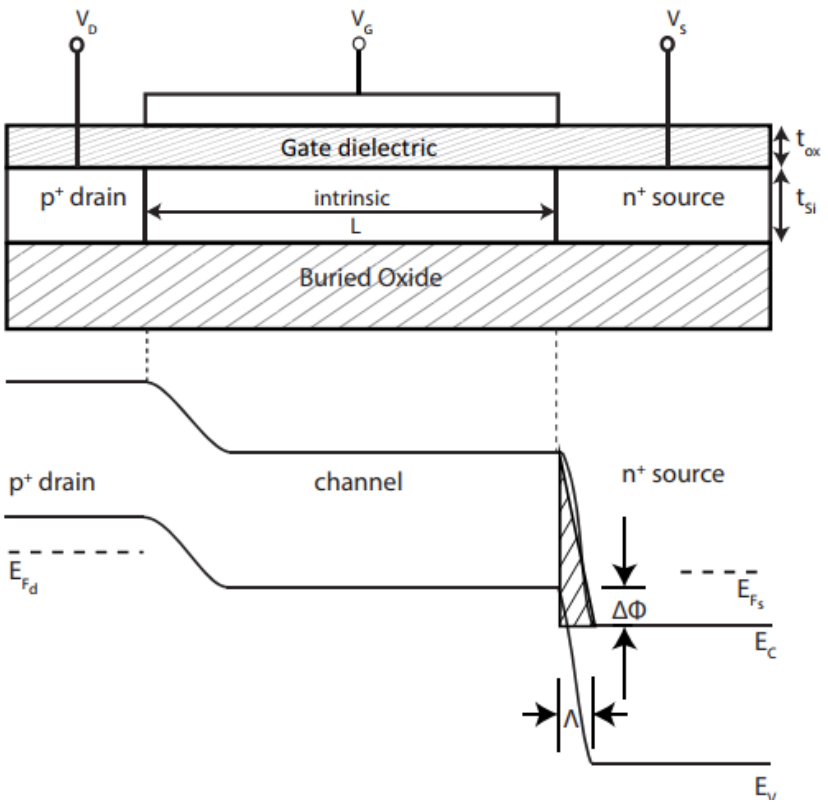


Figure 2.3 Representation of p-type SOI TFET. The Energy band diagram depicts the triangular barrier approximation at the source

The effective bandgap, can therefore be expressed as [30]:

$$E_g^* = E_g + 2\frac{\hbar^2 k_{trans}^2}{2m^*} \tag{2.5}$$

In the given region, the electrical field is represented as:

$$F = \frac{E_g + \Delta\emptyset}{\Lambda} \tag{2.6}$$

where Λ denotes the transition region width at the interface of source to channel.

So, it can be written:

$$T_{BTBT} \approx \exp\left[-\frac{4\sqrt{2m^*}E_g^{\frac{3}{2}}}{3|e|\hbar\left(E_g^* + \Delta\Phi\right)}\sqrt{\frac{\epsilon_{Si}}{\epsilon_{ox}}t_{ox}t_{Si}}\right] \quad (2.7)$$

Equation (2.1) demonstrates that the drain current is approximately **proportional** to the energy overlap window $\Delta\Phi$ and T_{BTBT}. Thus, from eq. (2.7), we can say that:

$$I_D \propto \exp\left[-\frac{4\sqrt{2m^*}E_g^{\frac{3}{2}}}{3|e|\hbar\left(E_g^* + \Delta\Phi\right)}\sqrt{\frac{\epsilon_{Si}}{\epsilon_{ox}}t_{ox}t_{Si}}\right]\Delta\Phi \quad (2.8)$$

2.2 Quantum tunneling phenomenon in TFETs

During the early 20th century, when the physicists performed the experiments at the atomic level, the results were quite astonishing. For example, the wave-particle duality was established based on the experiment of black body radiation and photoelectric effect. New theories were being put forward by physicists, like, Broglie's wave-particle duality principle, Bohr's atomic model, the Heisenberg uncertainty principle, and the Schrodinger equation etc. These theories were at times contrary to the classical physics, however they were backed by strong experimental evidences and hence were gradually accepted by the scientists by accepting the inadequacies in the classical physics.

In contrast to classical physics, the value of any physical quantity is calculated probabilistically in quantum mechanics. In fact, the phenomenon of BTBT is also possible because of the probabilistic behavior of nature. Newton's laws of motion is widely used in classical mechanics to determine the position or state of any particle, given its initial state and forces being applied are known. The similar kind of analogy is applicable to quantum mechanics as well. We can use, Schrodinger's quantum, equations to explain the nature of the wave function and how it varies with respect to time [31, 32]. However, the wave function representations are just probabilities or the expectation value. The Schrödinger equation is given for a particle restricted through the x-axis, as:

$$i\hbar\frac{\partial\Psi}{\partial t} = -\frac{\hbar^2}{2m}\frac{\partial^2\Psi}{\partial x^2} + V\Psi \quad (2.9)$$

In the equation, i represents an imaginary number, t is time, Ψ is the wave function, V denotes potential energy and *x* is the position along the x-axis. Schrodinger's equations can be used to find out the value of the wave function Ψ. The particle's expectation values can be calculated as below:

$$\langle x \rangle = \int_{-\infty}^{+\infty} x|\Psi(x,\mathrm{t})|^2 \mathrm{d}x \tag{2.10}$$

The Schrodinger's equation can be solved with the method of separation of variables, when the energy potential function V is time independent. The wave function of the Schrödinger equation can be expressed as:

$$\boldsymbol{\Psi}(x,\mathrm{t}) = \psi(x)\, \varphi(t) \tag{2.11}$$

where $\psi(x)$ denotes the spatial component of $\boldsymbol{\Psi}(x,\mathrm{t})$ which is a function of only x, while φ (t) denotes temporal component of $\boldsymbol{\Psi}(x,\mathrm{t})$ which is a function of only t. Thus, following equations can be derived:

$$\varphi(\mathrm{t}) = \mathrm{e}^{-\frac{\mathrm{iEt}}{\hbar}} \tag{2.12}$$

$$\frac{\hbar^2}{2\mathrm{m}} \frac{\partial^2 \Psi}{\partial x^2} + (\mathrm{E} - \mathrm{V})\psi = 0 \tag{2.13}$$

This equation represents the steady-state form of the Schrodinger equation. Equation (2.9) can be solved with the above equation, provided that the potential profile is independent of time. The solution that can be obtained for equation (2.13) won't be unique. Therefore, each solution would correspond to the specific value of the energy E_n. Consequently, the eigenvalues are the energy values E_n for which the Schrodinger Equation (2.13) can be solved and the respective wave functions (Ψ_n) represent the Eigen functions.

2.3 Subthreshold swing in TFET

Steeper subthreshold swing is one of the most significant and the desired characteristics of the TFET, which distinguishes it from the conventional MOSFET. The energy band diagram in the subthreshold region at two separate gate voltages is shown in figure 2.4.

The transport of the current in the MOSFET is by the thermal injection of charge carriers from source towards drain with an application of sufficient gate voltage. Only those carriers which are having energies greater than Φ_{max} at the source's exponential tail would add to the current near the subthreshold zone [33, 34]. In a conventional MOSFET, the drain current is proportional to source "Fermi–Dirac distribution function" $f_s(E)$ density of state $D(E)$, and the velocity of the carriers $v(E)$ (E representing the electron energy) [34]:

$$\mathrm{I_d} \propto \int \mathrm{dE.\, D(E).\, v(E).\, f_s(E).} \tag{2.14}$$

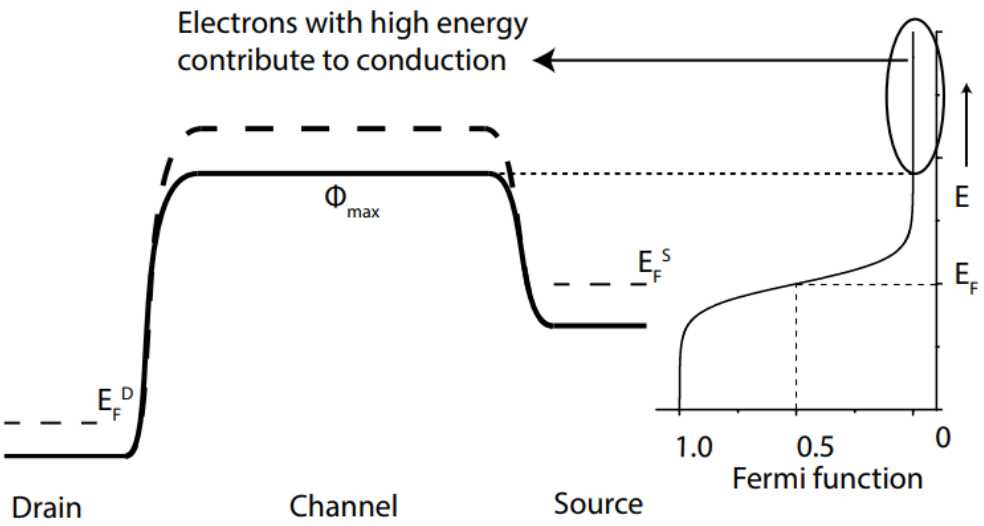


Figure 2.4 Representation of conduction band at two separate gate voltages in the MOSFET

A Boltzmann approximation can be used to derive the source Fermi–Dirac distribution function $\mathrm{f_s(E)}$ in the exponential tail region:

$$\mathrm{f_s(E)} \approx \exp\left(-\frac{\mathrm{E} - \mathrm{E_F^s}}{\mathrm{kT}}\right) \tag{2.15}$$

In the above equation, E_F^S represents Fermi energy level at the source, T denotes the temperature and k represents the Boltzmann constant. The product of $D(E) \times v(E)$ can be

considered as the constant for simplicity purpose, assuming just one spatial direction of transport. Likewise, it can be assumed for a MOSFET that whenever the gate to source voltage changes, there would be shift in the conduction band. Thus, it can be written:

$$\frac{\partial I_d}{\partial V_{GS}} = |e|\frac{dI_d}{dE} \tag{2.16}$$

where e represents the electronic charge. Using Equation (2.15) and Equation (2.16), in an ideal MOSFET, the subthreshold swing can be calculated as:

$$SS = \left(\frac{\partial \log(I_d)}{\partial V_{GS}}\right)^{-1} = \ln(10)\left(\frac{1}{I_d}\frac{\partial I_d}{\partial V_{GS}}\right)^{-1} \approx \ln(10)\frac{kT}{e} \tag{2.17}$$

For a conventional MOSFET, an ideal value of subthreshold swing at the room temperature is around 60 mV/decade, which is also being depicted from equation (2.17). The experimental results of the subthreshold swing for a MOSFET would have been worse than that of equation (2.17) simply because the gate voltage control over the potential of the channel and profile of the conduction band will be imperfect.

Equation (2.17) also illustrates that as the temperature rises, there would be an increase in the ideal subthreshold swing. The Fermi–Dirac distribution function $f_F(E)$ can be written by the following expression:

$$f_F(E) = \frac{1}{1 + exp\left(\frac{E - E_F}{kT}\right)} \tag{2.18}$$

The temperature's effect on the distribution function of Fermi-Dirac is shown in the figure 2.5. The probability of carriers occupying higher energy states would increase as the temperature would rise. In a conventional MOSFET, the subthreshold current is caused by higher-energy carriers across the energy barrier. As a result, the temperature-dependent enlargement of the Fermi–Dirac distribution function of the carriers is responsible for the limit defined in Equation (2.17). Now we'll look at how TFETs get around this limitation.

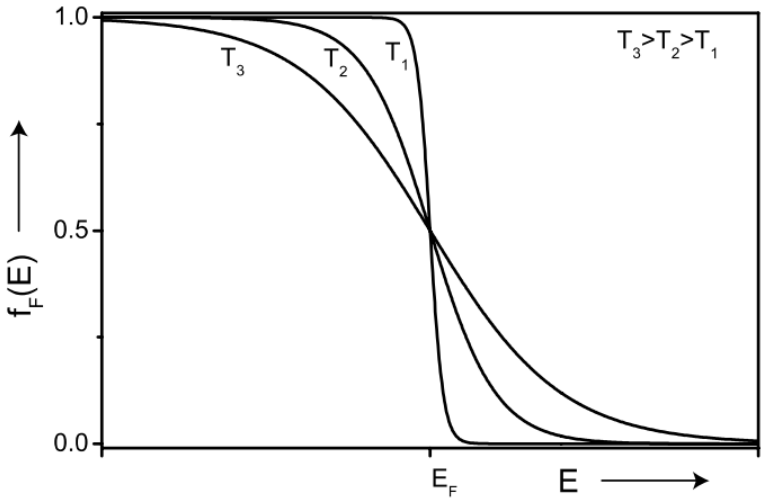


Figure 2.5 Fermi–Dirac distribution at different temperatures T_3, T_2 and T_1. As the temperature rises, the exponential tail becomes more prominent [35]

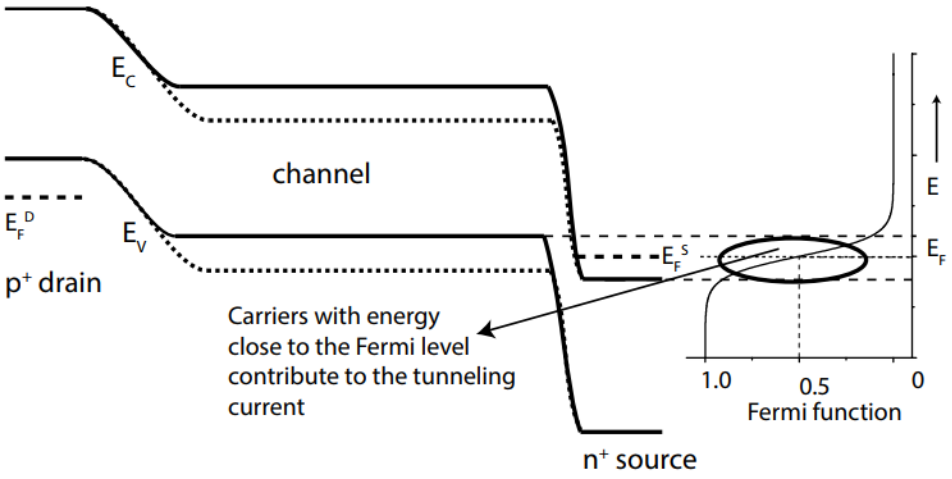


Figure 2.6 Band diagram at subthreshold region of p-type TFET at two different gate voltages [34].

The energy band diagram in subthreshold region of a p-TFET, at two separate gate voltages is shown in figure 2.6. The holes would tunnel into the channel, whenever a negative gate voltage is given, as at source, the channel is drawn above conduction band. If the valence band is lower than the conduction band, no tunnelling occurs. The channel prevents carriers from tunneling with energy in the Fermi– Dirac distribution's high-energy tail. The Fermi–Dirac distribution's low-energy tail is cut off at the source contact by the semiconductor

bandgap as shown in figure 2.7. When the channel's valence band gets aligned with source's conduction band, however, BTBT is activated, causing the state to switch from OFF condition to ON state abruptly.

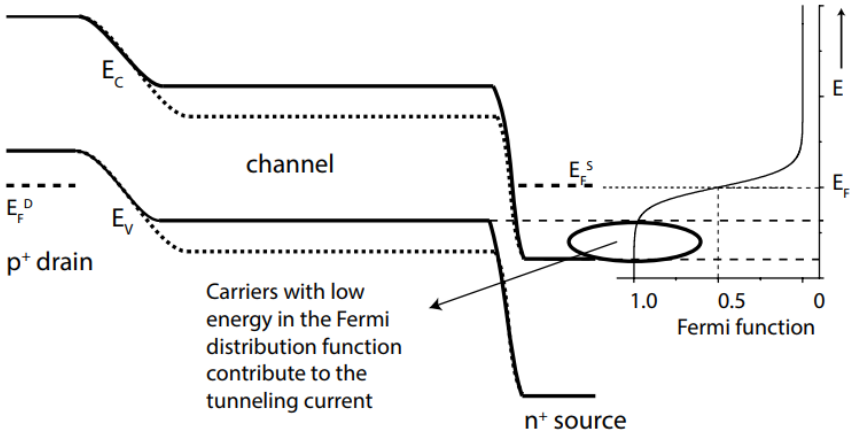


Figure 2.7 Representation of Energy band diagram when the Fermi energy level is high from the source side in TFET [34].

2.4 Ambipolar Current in a TFET

In a TFET, there are two tunnelling junctions: first at the drain–channel interface while as second at source-channel interface. Usually, in a TFET, the BTBT is suppressed in the drain-channel junction by reducing the doping of the drain terminal or by means of some other methods. When the TFET is symmetric, that is, when the doping concentration remains on the source and drain sides but in the opposite manner, the TFET exhibits ambipolar behaviour [36-38]. Ambipolar behaviour denotes the presence of n-type behaviour in the same TFET, when the main contribution to the current transport is due to electrons and a p-type behavior at the same drain voltage V_{DS} when the main contribution to the current transport is due to electrons. For an n-TFET, if the gate to source voltage is positive, there would be a tunneling phenomenon at the source region side, while as if the applied gate to source voltage is negative, at that time again there would be a tunneling phenomenon at the drain side, while maintaining the same drain source voltage.

When V_{GS} is positive, as it is in the DGTFET's regular n-type mode of operation, the valence band, conduction band get aligned on source side. When V_{GS} is negative, however, on the drain side, the bands are matched, as a consequence of which there is a BTBT from the drain side. Thus, it can be observed that whenever V_{GS} is positive, electrons are the primary cause of conduction and the conduction is primarily owing to the holes when V_{GS} is negative.

In a TFET, there would be a rise in the OFF current due to the ambipolar current. If the energy band gap is smaller, then the rise in I_{OFF} because of the ambipolar current is even worse. Thus, the ambipolar current would dominate the thermal leakage current in such devices in the OFF-state. As a consequence, the ambient current rather than the thermal leakage current controls the OFF-state current.

CHAPTER 3: LITERATURE REVIEW OF TUNNEL FET STRUCTURES

3.1 Introduction

The aggressive scaling in MOSFETs increases the static power dissipation of the device at a fast rate, so much, that it may overcome the dynamic power dissipation after few years. This led researchers to explore the alternate semiconductor devices so as to improve the performance and reduce power dissipation of devices. Other alternate devices being proposed were Impact ionization FET, Ferroelectric FET, feedback FET, etc. [39-45]. One such device that we will discuss in this chapter are Tunnel Field effect transistors (TFETs). TFETs have also evolved with time with different types of current boosting mechanism techniques, so as to boost their ON current and achieve steeper subthreshold slope. The detailed discussion on these techniques will be done in upcoming sections.

3.2 All Silicon TFETs

Due to the phenomenon of BTBT in TFETs, they offer low off current and lesser than 60 mV/decade subthreshold swing, but, it was found that the silicon based conventional TFETs offer a low current much lesser than that of MOSFETs. This is the most significant disadvantage of TFETs, and TFETs will not be able to be used in traditional CMOS circuits until this problem is resolved. As a consequence, TFETs have been the focus of a lot of research with the goal of increasing their I_{ON}. The major methods suggested by researchers to improve the performance of TFETs include a high-κ gate dielectric [25], thinner body, thin dielectric, abrupt doping profile, high source doping, etc.

Adrian M. Ionescu & Heike Riel [3]: Investigated TFETs for device optimizations. Heterostructures were proposed to optimize both p-type and n-type TFETs to offer Complementary TFET. To achieve it moderate doping was suggested.

Seabugh A, and Zhang Q [4]: compares the performance of the tunnel FETs with that of MOSFET. It discusses the ability of the tunnel FETs for obtaining the steeper subthreshold swing. It explains the tunneling mechanism under which tunneling of electrons from the valence band to the conduction band takes place under reverse bias. It discusses the mathematical relations for 1-D and 2–D transport equations. It mentions that by employing a gate with a stronger electrostatic control, transistor geometry can be optimized.

Haensh W, E.J. Nowak, et al [1]: provides an overview regarding how continuous scaling of CMOS devices is limiting the performance of the MOSFET, and is introducing short channel effects like increased static power dissipation and subthreshold leakage current. According to authors, questions have been raised regarding CMOS scaling, and it is the high time when researchers should look beyond CMOS for the improved performance. The author has suggested the use of the multigate device in order to have an improved control over channel by the gate. Structures like FinFET and trigate devices could be explored in this area.

Qin Zhang, Wei Zhao and Alan Seabaugh [46]: proposed a new SOI tunnel transistor, in order to beat the 60 mV/decade limitation of MOSFET. A lateral p^+n^+ junction was used in an ultra thin semiconductor body, and the gate was aligned towards the p side so as to have a control on the electrostatic potential.

Sung Hwan Kim, et al [47]: This paper focused in changing the paradigm from all Silicon TFETs to use of Germanium as a source. Experimentally, they have proved that very high I_{ON}/I_{OFF} ratio is achievable. The band alignment is still a challenging issue.

Choi W.Y. and Lee [48]: have implemented hetero gate tunnel FETs for better performance and low power consumption. The device was found to decrease the ambipolar current as well. At the source region, a gate insulator with high-κ material is used. The paper has also discussed improved fabrication methods. The device has been simulated for the channel length of 50 nm. Increased high-κ dielectric thickness from the source region, gradual doping profile, and spacers at the sides structures are the main factors for increasing ON current and reducing ambipolar conduction.

Hao Lu and Alan Seabaugh [49]: Authors have made a comparison of the tunnel FET drain current per unit width with respect to the gate-source voltage. General observations were that the use of Group III –V materials would increase the ON current owing to their narrower band gap energy, and other materials available are TMDs, carbon nano tubes, graphene ribbons, etc. They have found that there lies a disparity between the simulated and the experimental subthreshold characteristics. It has been attributed due to the negligence of non-ideality factors, defect assisted tunneling and interfacial defects.

Wang, Hilsenbeck, et al [50]: In this work, the complementary tunneling transistors were fabricated with CMOS technology for the very first time. This structure works with symmetric values of gate voltage and drain voltage, which are necessary for CTFET logic circuit configuration. The TFET can be used for both positive and negative V_{GS}. Since TFETs have a different structure and operating theory than MOSFETs, it is possible to scale them up to 20 nm channel lengths, without any major degradation in their OFF currents.

Jung-Shik Jang and Woo Young Choi [51]: looked into the effect of ambipolar current on device performance. When a device is being studied for a shorter gate lengths, then controlling the leakage current becomes more important. A novel parameter: ambipolarity factor (v) was introduced in order to parameterize the effect quantitatively when it comes to gate oxide thickness, drain and channel doping concentrations. Gate leakage were ignored during the ATLAS simulation. The device has been studied at 50 nm channel length, and a drain doping of 10^{20}. It was suggested that in order to suppress the ambipolar behaviour TFETs must have thick gate oxide, should operate at a lower supply voltage and should be doped lightly at the drain terminal. ON current was found to be the trade-off parameter for improving ambipolar current in tunnel FETs.

3.2.1. Thickness and Dielectric Constant:

The tunneling current is supposed to increase if the gate oxide thickness is reduced or the gate material's dielectric constant is increased, presuming that all other factors in Launderer’s equation described above remain the same. As both terms are related to drain

current exponentially, so the rise in the current is expected to be super linear. This has been stated by several research groups [25, 52-55]. The BTBT rate controls the physics of TFETs, so they are distinct from those of conventional MOSFETs. As a result, the device's sensitivity to changes in technical parameters would most likely differ, potentially posing new technical challenges.

Boucart [28]: had estimated that the performance of TFET will be lesser sensitive towards gate length scaling and doping fluctuations than conventional CMOS transistors. Controlling the high-gate mechanism, the film thickness in ultra - thin SOI applications, and the abruptness of injecting charge carriers at the tunnel junction, on the other hand, is critical for developing future TFETs with consistent characteristics that require much fewer parameter variations than CMOS devices.

Use of high-κ gate is also popularly now a days used in TFETs to increase the ON current. It is because, it allows us not to decrease the physical thickness of the gate beyond certain limit. High-κ gate materials like Hafnium oxide have been used comprehensively for boosting the ON present by the researchers.

Boucart K., Ionescu A.M, [56]: A novel design of doubled gated tunnel FET was proposed. In this architecture the dielectric being used for the gate was of high-κ. The average subthreshold swing obtained with the device was around 57 mV/decade. It was observed that a tunnel FET with gate dielectric of high κ would be having a smaller subthreshold swing, when compared with the use of SiO_2. The device simulations had been performed over the gate length of 50 nm. From the mathematical relations, it has been signified that the high-κ dielectrics support higher tunneling rate. It's because the increased gate capacitance improves electrical coupling between the tunnelling junction and the gate. The effect of temperature on system characteristics was also investigated by the authors. It was found out that, while the OFF current varies with the rise in the temperature, but from the ON current side, the changes are very scanty. Thus, it could be concluded that I_{ON}/I_{OFF} ratio would get degraded at the higher temperature.

Toh E.H, Wang G.H, et al [26, 55]: implemented the double gated tunnel FET with SiGe as the source. It was established that the narrower energy band gap of SiGe plays a dominant role in tunneling of electrons. The average subthreshold achieved is around 29 mV/decade. It was also suggested that SiGe heterojunction should be placed at the left of the gate to reap the additional benefits of higher BTBT rate. However, it was found that the device suffers from the ambipolar current whenever a negative gate to source voltage was applied.

Seung Kim, Woo Young [57]: have studied the effect of gate dielectric constant on the device. It was established that, in comparison to the MOSFETs, tunnel FETs are more sensitive to local gate dielectric constant variations.

3.2.2. Multiple Gates:

Multiple gate structures have been suggested by the researchers in order to have better gate controlled terminal over the channel. In order to improve the I_{ON}/I_{OFF} ratio in TFETs, it is incumbent to understand the relation between gate voltage and channel potential. Gate all around gate wrap-around gate structures have been demonstrated experimentally to boost the drain current [58-62].

Seongjae Cho, Jae Sung Lee, et al [58]: Gate all around tunnel FET has been implemented at varied gate lengths. The different parameters analyzed were: transconductance, gate-source capacitance, gate-drain capacitance and inversion layer length. It was established that the f_T of GAA TFET depends on $1/L_G$, and hence provides a path for future TFET research for RF applications

Jaya Madan, Rishu Chaujar [59]: The paper is combining the good features of gate-drain underlapping and cylindrical gate all around TFET. The source pocket has been used to increase the tunneling rate, and therefore the ON current of the device. The purpose of using gate drain underlapping is to suppress the ambipolar current and decrease the parasitic capacitance. It was observed that the analog/RF performance of device also got improved.

S. Guha and P. Pachal [63]: has implemented SiGe heterojunction source based double gate TFET. The device has been investigated for analog/RF performance as well as ambipolar current conduction. The channel thickness at the center is greater than the rest of the channel. This increases the controllability of the gate, thus leading to higher tunneling current. The narrow channel near the drain reduces the ambipolar current. Authors have also developed a Verilog-A model for studying the circuit level performance of the device by realizing a common source amplifier circuit

3.2.3. Use of Spacers:

The potential barrier is lowered by electrical field fringing at source/drain and channel, resulting in a lower threshold voltage (V) and increased sub-threshold swing. This effect is more prominent in lesser than 100 nm MOSFET devices with high-κ gate dielectrics (κ > 25) and worsens as κ increases. In high-K dielectrics, fringing is increased as the vertical electrical field decreases as indicated by the continuity of the charge. But, effect of the fringing fields is extremely advantageous in tunnel FET. As long as the tunnelling current controlled by a gate is lower, the off-current is determined using the p-i-n diode leakage current. It can therefore be claimed that, in comparison to traditional MOSFETs, the fringing field effect has a substantial positive effect on the TFET performance [64-68].

When using gate dielectrics with very high dielectric constants, however, the fringing field effect greatly compensates for this effect. The rise in the minimum width of the tunnel in the TFET is also due to the growth of the fringe fields. Since the minimum tunnel width defines the TFET's I_{ON}, as the spacer material's dielectric constant increases, TFET's I_{ON} degrades significantly. The dielectric constant of the spacer material increases as the dielectric constant of the spacer material increases, as a result, the fringe field rises the electrical field through the tunnelling junction in the TFET with SiGe source and decreases the minimum tunnelling width, improving the I_{ON}. The width of the spacer is also essential in controlling the TFET output.

Avik C. and Abhijit Malik [68]: A tunnel FET has been investigated with a changing dielectric constant and the spacer width. It was established that the device characteristics

are less spacer dependent when there is more doping at the source region or a gate–source overlap. The device has been simulated for 50 nm channel length.

Mohd Adil, Naushad Alam, et al [69]: have investigated the use of asymmetric dual- κ spacers for enhancing the ON current. On the gate line, there is a high-k spacer, and on the source side, there is a low-k spacer. It has been implemented on junction less TFET. The minimum subthreshold swing achieved is 40 mV/decade with a high $\frac{I_{ON}}{I_{OFF}}$ ratio of 10^8.

Martin Schlosser, Krishna K. et al [64]: have studied the effect of high-κ gate dielectric in TFETs, have compared its results with the use of silicon dioxide. While in the conventional MOSFET, the fringing effect degrades the performance, it also yields a much greater on-current that is similar to practical conventional MOSFETs, as well as a tunnel FET subthreshold slope that is less than minimum possible values with that of MOSFET.

H.G. Virani, and Anil Kottantharayil [67]: have studied the influence of high κ spacers for boosting the ON current in SiGe-Si based heterojunction TFETs. The ON state current is shown to be enhanced through the spacer without affecting the subthreshold swing or the OFF current. Using a drain side overlap along with a high κ spacer will reduce the OFF state current even further.

J. Y. Young, J.H. Seo, et al [70]: have investigated the effect of spacer dielectrics for germanium (Ge) based tunnel FETs. The minimum subthreshold swing achieved is 50 mV/decade. In the Ge-TFET having a low κ-spacer, a sharp bend banding between the source-side channel and the source junction is modeled to a narrow tunnelling barrier with higher I_{ON} and I_{OFF}. The paper also shows the relation of the spacer dielectrics with the total gate capacitance of the device, which is the combination of source and drain region parasitic capacitances.

3.3 Group III–V-semiconductor-based TFETs

By the combination of group III metallic elements with the non-metallic elements of group V, we can obtain III-V semiconductor compounds. Researchers are looking into several

III-V compounds for use in TFETs, including the following examples: InGaAs, InP, GaAsSb, InAs, GaSb, etc. These semiconductors are usually referred to as III-V TFETs [71-77]. The alternate way for improving I_{ON} and SS is to use low band-gap materials and low effective mass. Group III–V materials are especially appealing in this regard as they have a low tunneling mass and allow for a variety of band-edge alignments. The I_{ON} and I_{OFF} in III-V TFETs are both high because of the smaller bandgap of III-V semiconductors. The III-V semiconductors are therefore commonly used in TFETs as heterojunctions in such a way that high I_{ON} and low I_{OFF} can be achieved simultaneously.

H. Zhao, Y. Chen et al [78]: Authors have used the technique of atomic layer deposited gate oxides in InGaAs tunnel FET for boosting the ON current. Different materials for gate oxides were used, however, Al_2O_3/HfO_2 bilayer gate oxides significantly improved subthreshold swing. The minimum subthreshold swing achieved is about 86 mV/decade. This has been attributed to the dependency of the ON current on the electron density rather than the channel electron mobility.

Hongliang Lu, Bin Lu, et al [79]: have implemented InAs/Si based tunnel FET for improving ON state current and the subthreshold swing. An analytical potential model was developed at the channel length of 50 nm for the drain current.

Tarek Ameen, Hasemeddin, et al [80]: have proposed alloy engineered nitride heterostructures for boosting the ON current. A piezoelectric polarization field is crested in a nitride heterojunction due to the lattice mismatch, and that results in an increased ON current. However, thermally generated hot charge carriers degrade the subthreshold characteristics through the quantum well states at the heterojunction interface. Alloy engineered nitride TFET can minimize this effect and have shown promising result in the low power area with applied drain voltage lesser than 0.5 volts.

S. Sant and A. Schenk [72]: In this paper heterostructure used is $In_{0.53}Ga_{0.47}As$ / InP. It has a smaller band gap which results in an improved tunnel rate. Ambipolar leakage is reduced by the channel/drain content InP big bandgap. This alloy was found to be lattice matched.

Prabhat Kumar Dubey and Brajesh Kumar Kaushik [81]: T shape group III-V InP/InGaAs heterojunction TFET has been implemented and its electrical characteristics have been studied. The device has been compared with the lateral TFETs and it has been found that there is about 4.3 times improvement in the drive current and around 4 times improvement in the transconductance. $\frac{I_{ON}}{I_{OFF}}$ ratio obtained was 3.72×10^7 at 0.3 V supply voltage. A buried oxide layer of aluminum oxide (Al_2O_3) has been used. The quantum effects have not been included in the study. The device also suppresses the ambipolar current due to the overlapping of the drain and the metal gate. The overlapping depletes the drain region for the negative gate voltages. It is established that although *InAs/GaSb* heterojunctions also improve the ON current, they degrade the OFF current and subthreshold swing in TFETs. While designing a hetero-structure, lower band gap material should be used at the source terminal and higher band gap material should be used at the drain terminal.

Xiaoling Duan, Jincheng Zhang, et al [82]: have studied a gate engineered InGaN doping-less tunnel FET. Such structures have a relatively simpler fabrication process when compared to the doped TFETs because of the absence of the junction. The fraction of Indium used is about 0.75 due to its almost similar energy band gap as that of silicon. The device has been simulated for 50 nm channel length. The average subthreshold swing obtained for the device is about 41.3 mV/decade. The body thickness of the device is 10 nm, so the quantum mechanical effects have not been studied. It claims that when thickness of the body is less than 10 nm, a quantum confinement model should be enabled. The analog/RF performance analysis has also been carried out for parameters like cut-off frequency, total gate capacitance, etc. The cut-off frequency obtained for the device is 119 GHz.

S. Mookerjea, D. Mohata, T. Mayer, et al [83]: In this paper $In_{0.53}Ga_{0.47}As$ TFET has been fabricated using Molecular Beam Epitaxy. This paper focusses on the temperature dependence of drain current with respect to gate voltage. Temperature has been varied from 0 kelvin to 300 kelvin. It has been found that there exists a strong temperature dependence

in the subthreshold region, due to which subthreshold swing degrades with the rise of temperature. As gate voltage increases further, temperature sensitivity becomes weak.

3.4 Germanium as a material

Chemically, the properties of germanium are comparable to those of silicon, and they are generally compatible with current CMOS processes. For the last few decades, researchers have been drawn to germanium because of its higher carrier mobility than silicon. Germanium has a bandgap of 0.67 eV, which would be less than the bandgap of silicon. [84-86]. As a result, in a germanium-based MOSFET, the leakage current is strong due to BTBT [87]. However, fact that germanium has a smaller direct bandgap than silicon makes it a successful choice for TFET applications. The I_{ON} in a TFET based on germanium is higher than the order of magnitude in a TFET based on silicon with a similar structure because germanium supports inherently higher band-to-band tunnelling than silicon [55]. This has allowed researchers to integrate TFET structures with germanium. A traditional TFET based solely on germanium, on the other hand, has a high and unacceptably high I_{OFF}. As a consequence, in germanium-based TFETs, techniques that can hold the I_{OFF} under control are unavoidably used. I_{OFF} can be reduced by using a lower drain doping or by the use of a short gate [27, 88].

3.5 Carbon based Tunnel FETs

Carbon nanotubes and nanoribbons of graphene are desirable materials being used in TFETs. Their charge carriers have a low effective mass, a small and direct bandgap, and because of the ultrathin body, the gate has superior electrostatic control over the channel, making them one of the best materials and system geometry options.

Appenzeller et al. [33] in 2004 demonstrated the very first TFET with a subthreshold swing of less than 60 mV per decade using a CNT structure. Two separate gates were used in their system to control the electrostatics in the carbon nanotube. For the first time, a SS of 40 mV per decade was reached, but the ON current obtained was poor due to the carriers needing to tunnel between two barriers. However, using graphene nanoribbons for a

realistic implementation, the effect of transport properties and line edge roughness on the bandgap on TFET performance must be taken into account.

Luisier and Klimeck [89] discovered that when the edges are rougher, the off current increases rapidly due to a reduction in the graphene nanoribbon bandgap and an improvement in the leakage of the source-to-drain tunneling through the potential barrier of the gate. This results in a degradation of SS and I_{ON}/I_{OFF}, which is no longer adequate, and thus, the switching behaviour of TFET graphene nanoribbons is reduced. Theoretical research thus far has shown that graphene nanoribbon TFETs have a good prospect, while important technological challenges need to be met for practical implementation.

Fiori and Iannaccone [90]: have proposed Bilayer graphene as a feasible alternative to graphene nanoribbons in the fabrication of TFETs.

S. O. Koswatta, M. S. Lundstrom, and D. E. Nikonov [91]: explored the use of carbon nano tube based FETs. It proposed a novel way of removing the high dielectric gate oxide from the source/ drain region. Due to that, fringing effects can be avoided that was leading to a band bending at the junction. Another advantage proposed was that the device capacitance remains smaller until higher gate voltage is applied.

3.6 Tunneling Junction:

3.6.1. Source Doping:

The source doping profile has a substantial effect at the source to channel junction on tunneling barrier, which controls the I_{ON} through the TFET [92-94]. For a TFET, the I_{ON} is extremely dependent on tunneling junction properties, especially from the source terminal. The ON current in the DGTFET increases as the source doping concentration increases. A large rise in the source doping concentration would lead to a decrease in the tunnel barrier distance. Whereas a traditional MOSFET shows lower sensitivity to doping profile, the subthreshold swing and the I_{ON} are ultra-sensitive to the doping profile in a TFET.

Reducing the dopant profile, thus optimizing it, is an essential feature of designing the TFET structure [95].

3.6.2. Use of Pockets:

Another way to go for an even higher I_{ON} is to use a heavily doped source pocket in the TFET [96-100]. The pocket and the source regions are doped with opposite type of dopants. PNPN TFETs feature a n^+ pocket on the source side. This n^+ depletion is optimally adjusted so that the pockets have the same width and are uniformly doped. It is vital that the fully depleted pocket is retained throughout the operation of the PNPN TFET. At the source, the tunnelling width gets decreased due to the addition of a thin completely depleted n^+ layer. As a result, the lateral electric field is increased. This allows for an increase in the I_{ON} and the subthreshold slope in the PNPN TFET [96, 97]. Jaya Madan and Rishu Chaujar [101] have used n^+ source pocket based PIN-GAA TFET in order to examine the effect of interface trap charge density and temperature on device characteristics by numerical simulations. The parallel E_y and normal E_x components of the electric field, is increased when donor trap charges are present, according to the findings. The increased E_y raises the electron BTBT rate defects as well as the gate leakage present, lowering the device's reliability. Further, it was observed that I_{OFF} is severely degraded by the existence of donor trap charges.

3.6.3. Vertical TFETs:

The researchers have also explored the vertical tunneling device [102-108]. The vertical TFET (VTFET) has a distinct principle of operation as opposed to the conventional lateral TFET (LTFET), and nearly all recent studies have been devoted to learning about it. Although both the types of TFETs (Type TFET and VTFET) use BTBT, the tunneling is in a perpendicular direction on the oxide-Si interface in the VTFET whereas it is in a parallel manner on the oxide-Si interface in the LTFET. Additionally, the VTFET provides many advantages over the LTFET. One such advantage is a steeper subthreshold slope, which allows the regulation of tunneling through gate voltage. Because of the steep

subthreshold slope, the OFF current is low and the capacity for low power operation is present.

The VTFET's operation is built on the concept of BTBT, which is the same as LTFET. When a positive bias is applied to the gate and drain terminal, while keeping the source grounded, the transistors are represented as being NMOS. When the gate voltage is at a specific level (V_T), a current tunneling path will be established from the body to the channel, and from there, it will flow to the drain.

K. K. Bhuwalka et al [102]: It proposed a vertical PIN structure grown via Molecular Beam Epitaxy. Vertical TFETs have a quick exponential increase in current, low off-state leakage currents, and I-V characteristics that are nearly temperature independent. However, the limitation of the proposed design was low ON current.

K. K. Bhuwalka et al [103]: It proposed certain changes in conventional V-TFET design. It replaced the heavily doped δp^+ Silicon layer by a δp^+ Si-Ge layer at the p-source end. As the Valence Band was elevated above the Conduction Band, this allowed for more control over both tunneling barrier width and height. This resulted in an increase of tunneling probability. However, there was no substantial improvement in ON current.

R. Rooyackers et al [104]: This paper focused on the complementary hetero junction vertical TFETs. During device fabrication, a sacrificial source layer is used. The source is replaced by a low band gap material suitable for n-TFETs after the gate stack is formed (or p-TFET), such as $Si_{1-x}Ge_x$ to form Hetero junction over the silicon Channel. However, it involves complicated fabrication processes.

Wang P.Y. and Tsui [109]: have proposed a novel epitaxial tunnel layer (ETL) structure that supports vertical tunneling. By using low energy band gap materials in the ETL layer enhances the current in ON state. Si_xGe_{1-x} heterojunction material has been used for the ETL, and the ON current obtained is of the order of 10^5 to 10^{10}. The author has specified that due to the lack of the proper models, quantum confinement effects are rarely discussed

in the literature, and are quite often ignored during the modelling. Authors have concluded that the subthreshold swing may degrade due to the quantization effect.

S.Y. Kim, W.Y. Choi et al [110]: have implemented silicon based L shaped channel type tunnel FET keeping scaling issues into consideration. Furthermore, whereas traditional TFETs have tunneling current directions that are parallel to the channel, L-shaped TFETs have BTBT that is perpendicular to the direction of channel. In order to inhibit ambipolar activity, drain regions are lightly doped. It has been proven that L-shaped TFETs have a more abrupt on/off transition than traditional TFETs, implying that the average subthreshold swing is lower in L shaped TFETs. However, the device suffers from the corner effect at the source region, which may increase the leakage current.

Shupeng Chen, H. Liu, et al [111]: Analog/RF analysis of silicon based dual source tunnel FET has been performed. A concept of dual source is being introduced in order to enhance the tunneling with increased tunneling area. The device was studied and compared with U shaped TFET and lateral TFET as well. Some analog parameters being studied were cut-off frequency, gain-bandwidth, gate-source capacitance, gate-drain capacitance, etc.

Ashita, Sajad A. Loan [112]: have presented gate over source channel TFET. Within the source and channel regions, it provides a vertical tunnelling direction. Furthermore, it speeds up the thinning of the lateral tunnelling barrier between source and channel regions. The paper suggests that the lateral barrier between channel and the source exists which results in a higher ON current.

W. Wang, et al [113]: have implemented U shaped channel based tunnel FET to reduce the leakage currents. A Si delta layer with n+ doping was introduced under the source region in order to enhance the drain ON current during tunneling. The inserted delta layer shortens the BTBT path, increases the tunnelling area, and therefore improves device's tunneling rate. Minimum subthreshold swing obtained is 34 mV /decade and high $\frac{I_{ON}}{I_{OFF}}$ ratio of 10^8 is achieved at the drain voltage of 1 volt.

Sunny Anand and R.K. Sarin [114]: Authors have implemented SiGe source based doping less TFET device. Its analog/RF performance has been investigated and compared with conventional Si doping less TFET. The drive current was found to be increased up to the order of 10^{12}. However, the average subthreshold swing is around 64.79 mV /decade. The device simulations have been performed on a channel length of 50 nm.

Haiwu Xie, and Hongxia Liu [115]: have simulated a tunnel FET structure with double source and U shape gate. SiGe pocket has been used for boosting the ON current. The average subthreshold swing obtained is about 35 mV/decade with $\frac{I_{ON}}{I_{OFF}}$ ratio reaching upto 10^{11} which is very high. The device has been simulated at the gate height of 40 nm. The analog/RF performance study has also been carried out. The values for gate source capacitance and gate drain capacitances are 0.87 fF/μm and 0.67 fF/μm at $V_{DS} = 1\,V$. Accordingly, the cut-off frequency (f_T) and gain bandwidth have been found out as 25.7 GHz and 22.5 GHz. These values are higher than what is achievable with UTFET which are, 3.56 GHz and 3.06 GHz, respectively.

M.R. Tripathy, A.K. Singh, et al [116]: have presented a comparative study of various vertical tunnel FET structures with pockets: all-Si heterojunction TFET, $In_{0.53}Ga_{0.47}As$/Si heterojunction TFET, and GaSb/Si heterojunction TFET. The purpose of using narrow band gap materials at the source is to reduce the tunnel width so as to increase the tunneling at the source-channel heterojunction. A high κ dielectric material Al_2O_3 has been used as a gate oxide instead of SiO_2 to achieve higher ON current. Use of GaSb with Si or $In_{0.53}Ga_{0.47}As$ with SI may result in the creation of defects at the heterojunction because of lattice and thermal co-efficient mismatching. The DC as well as RF performance has been studied. It has been shown that III-V/Si TFETs could achieve better SS (below 40mV/decade) and higher I_{ON}/I_{OFF} ratio (10^9 to 10^{11}).

A.K.Singh, M.R. Tripathy, et al [117]: implemented heterojunction (HJ) partial ground plane (PGP) TFET with SELBOX for improving the ION/IOFF current ratio of the TFET. The material used for the source is Ge. The effect of the temperature on the DC parameters such as transfer characteristics, threshold voltage and subthreshold swing (SS) of the given

device. The highest electrical field obtained is 3.2×10^6 V/μm, resulting in the highest tunneling current. Inclusion of PGP reduces the floating body effect on the performance of SOI devices. The RF performances in terms of parasitic capacitances and cut-off frequency characteristics of the PGP SELBOX TFET have been compared with other TFET devices. The effect of temperature on the performances of the proposed PGP SELBOX TFET structure is shown to be minimal over the conventional SELBOX TFET and SOI TFET devices.

3.7 Junctionless TFETs:

Recently, based on Lilienfeld's initial transistor design [118, 119], a junction less field effect transistor (JLFET) was proposed and fabricated. In comparison with MOSFET, a JLFET channel has the same doping concentration and structure as that for drain and the source. There is an absence of a p–n junction in this device since there is no lateral concentration gradient in the conduction layer. Additionally, this device has no metallurgical junction, thus reducing the manufacturing difficulty, enhancing electrical properties, and minimizing variability compared to MOSFETs [120-123]. However, even though the JLFET provides better electrical properties and is less complex, the SS (subthreshold slope) of a MOSFET is still limited. Alternative transistors have been suggested to be able to reach lower SS (60 mV/decade at room temperature) due to low overall power demand. A summary of a few of the significant research papers is provided below:

Jagadesh Kumar, and Sindhu Janardhanan [94]: reported the doping-less tunnel FET which works using the charge plasma concept. No doping at the drain and source regions is required, hence eliminating the need for the creation of abrupt junctions for efficient tunneling. Appropriate work functions are required at the source and drain electrodes. Hafnium is used as the drain metal electrode and platinum is used as the source metal electrode. Doping-less TFET fabrication eliminates the need for high-temperature doping/annealing processes, reducing the thermal budget and allowing for the fabrication of TFETs on single crystal silicon-on-glass substrates produced by wafer scale epitaxial

transfer. Since no higher temperature is required, this makes junction less TFETs suitable for displays, and biosensors. The device has been simulated for the 50 nm channel length.

Abdi and Jagadeesh Kumar [98]: A technique was suggested that uses the charge plasma principle to create an in-built N+ pocket without the requirement for a separate implantation. The device has been simulated for the 50 nm channel length. Looking at the conventional PNPN tunnel FET it was realized that this increases the fabrication complexity since, in the vertical TFETs N+ pocket requires either epitaxial growth or implantation in planar TFETs.

B. Ghosh and M. W. Akram [124]: A novel method presented in this paper is junction less TFET. The benefits discovered are that they are easier to manufacture, have improved electrical properties, and have less variability than MOSFETs. To improve channel controllability, double gate technology is being used. Idea was to convert JL-FET structure into a JL- TFET structure without any physical doping. However, Subthreshold Swing is still on the lower side. It has been proposed that high-κ dielectric gate materials be used for TFETs to improve their ON current and subthreshold swing.

3.8 Problem Statement and Research Gaps:

Out of the various techniques discussed in the research papers above, we have selected SiGe based heterojunction tunnel field effect transistor (TFET) device for this thesis work. There were various motivations for selecting this area of research work. Some of them are being listed below:

1. Although TFETs are being extensively studied and thought of as a replacement of MOSFET in the future, still the various TFET architectural devices support low drive currents, when compared to conventional MOSFETs. Many of the methods to boost the ON current also sometimes leads an increase of the OFF current as well. Consequently, the ratio of I_{ON}/I_{OFF} turns out to be low again [1, 26, 51, 102]. So, in our thesis work, we have focused on using such a material that would provide higher tunneling current at the source-channel junction so as to increase the ON

current, but at the same time would prevent the tunneling at the drain-channel junctions to prevent the rise of the leakage current.

2. When we explored the literature ON the TFET device, it was learnt that, in contrast to the conventional MOSFETs, the doping of the source and the drain regions should be of opposite dopants. For example, if we consider an n-type TFET, then the source region should be doped p-type while the drain region should be doped n-type. Thus, source and drain regions are not interchangeable with what we observe in MOSFETs. The effect of this property is that, if we apply a negative gate voltage to the TFET, then there would be a current transport due to the band to band tunneling at the drain-channel junction, with dominant charge carriers being holes. This would mean a higher OFF current [28, 125]. We have tried to address that issue as well in our research work while maintaining the high I_{ON} current and a steeper subthreshold swing.
3. It was observed that although it is theoretically possible to achieve a sub 60 mv/decade subthreshold swing in TFETs, still many of the conventional Si based TFET devices couldn't attain this value. We also learnt that although the Group III-Group V compounds like InGaAs, InP, InAs, GaAsSb, etc. are also being used extensively for obtaining the higher ON current, however, they suffer from a problem of the poor quality interface during fabrication [47, 104]. If the junction is not abrupt, it results in the formation of interface charges getting trapped and other defects [49, 80]. The result is that the subthreshold swing gets deteriorated, thus makes its use challenging. So, we have looked for SiGe based heterojunction structure, as its compatibility with current design technology would be similar to that of a silicon and the amount of the Germanium composition can always be controlled by molar fraction variations of the compound.

CHAPTER 4: MODEL TOOLS, METHODOLOGY AND RESEARCH PROCESS

4.1 Models Included and the Underlying Physics:

All the research work has been carried out using the Visual TCAD software by Cogenda (License Version 1.9.2.3). The software supports the GUI mode as well as the scripting mode for creating a structure. Since the tool is being used extensively for explaining the device characteristics of the proposed TFET structure, As a result, understanding the underlying physics and the models used to run the simulations is critical.

In order to perform the analysis of TFET on a Visual TCAD, it is important to enable the band to band tunneling model, so that we can accurately capture the tunneling phenomenon of our device. The BTBT model available in Visual TCAD is based on Kane's model [126, 127]. The carrier generation by band to band tunneling G^{BB} is expressed as:

$$G^{BB} = A.BTBT.\frac{E^2}{\sqrt{E_g}}.\exp\left(-B.BTBT.\frac{E_g^{3/2}}{E}\right) \tag{4.1}$$

In the equation A.BTBT and B.BTBT are the constants which can be calibrated based on the empirical parameters involved in the device architecture, E represents the electrical field and E_g denotes the energy band gap.

Drift-Diffusion model has been used for the semiconductor device simulation of the charge carriers (electrons and holes), and is almost a standard model, being following in various other popular simulators [128]. The primary function DDML1 is based on Poisson's partial differential equation:

$$\nabla.\varepsilon\nabla\Psi = -q(p - n + N_D^+ - N_A^-) \tag{4.2}$$

In the equation, Ψ represents the surface potential.

When the device is of shorter channel length, then Energy-balance Model available in the GENIUS tool must be incorporated during the analysis. For a carrier recombination

mechanism, a combination of Shockley-Read-Hall (SRH), Auger and Direct Recombinations are being utilized:

$$U = U_n = U_p = U_{SRH} + U_{dir} + U_{Auger} \tag{4.3}$$

Where, $U_{SRH}, U_{dir}, U_{Auger}$ are given by:

$$U_{SRH} = \frac{pn - n_{ie}^2}{\tau_p \left[n + n_{ie} exp\left(\frac{ETRAP}{kT_L}\right)\right] + \tau_n \left[p + n_{ie} exp\left(\frac{-ETRAP}{kT_L}\right)\right]} \tag{4.4}$$

$$\tau_n = \frac{TAUN0}{1 + \frac{N_{total}}{N_{SRHN}}} \tag{4.5}$$

$$\tau_p = \frac{TAUP0}{1 + \frac{N_{total}}{N_{SRHP}}} \tag{4.6}$$

$$U_{Auger} = AUGN(pn^2 - nn_{ie}^2) + AUGP(np^2 - pn_{ie}^2) \tag{4.7}$$

$$U_{dir} = DIRECT(np - n_{ie}^2) \tag{4.8}$$

The default values of the recombination parameters used in our Visual TCAD are as follows [129]:

Table 4-1 Recombination parameters default values

Parameter	Unit	Silicon	GaAs	Ge
ETRAP	eV	0	0	0
DIRECT	cm^3s^{-1}	1.1e-14	7.2e-10	6.41e-14
AUGN	cm^6s^{-1}	1.1e-30	1e-30	1e-30
AUGP	cm^6s^{-1}	0.3e-30	1e-29	1e-30
TAUNO	s	1e-7	5e-9	1e-7
TAUPO	s	1e-7	3e-6	1e-7
NSRHN	cm^{-3}	5e16	5e-17	5e16
NSRHP	cm^{-3}	5e16	5e-17	5e16

One of the most critical characteristics of the carrier transport model is carrier mobility. An expanded mobility model has helped to increase the capability of even smaller sub-micron devices. Mobility modelling is typically performed as low-field, high-field, and MOS

inversion layer mobility. If the electric field increases, the carrier mobility decreases so it is no longer possible for the carriers to accumulate the energy to take part in several scattering processes. The mean drift velocity now increases more slowly than before, at a slower rate per unit of increase in the electric field. Eventually, the velocity will stop increasing as more applied force is used, but it will reach a constant velocity when the applied force is maximized. The symbol $vsat$ commonly denotes this constant velocity. For energetic carriers, impurity scattering is not that important, and therefore $vsat$ is mainly determined by the temperature of the lattice. Since our TFET device is based on BTBT, therefore, a very high electrical field is generated at the source-channel tunneling junction. For accurate simulation of MOS devices, these effects must be accounted for. Because a comprehensive mobility model can account for physical processes such as quantum effect and velocity overshoot, which are not described by DD, it can be seen that DD doesn't encompass everything that can be understood about physical mechanisms.

The Bulk mobility model is applicable for low electrical field devices. In addition to the family of mobility models that was described above, unified mobility models are another choice. The effects of transverse and parallel E-fields are combined in these mobility models, which are integral parts of their architecture. In light of these results, it is recommended that these models be used for silicon MOSFET simulations. At the same time, however, unified models are only applicable to a small number of components, such as Si and SiGe. We have considered Lombardi's mobility model during our simulation. The Lombardi mobility model defines the mobility of carriers in the MOSFET inversion layer using an analytical model [130]. The Lombardi model is made up of three sections.

i. Bulk mobility μ_b which is doping dependent plays the key role in contributing to the ionized impurity scattering.
ii. The acoustic phonon scattering μ_{ac} mobility degradation observed in the inversion layer. Because of quantum confinement at the interface, this mobility degradation is mainly determined by the transverse electric field.
iii. The scattering of surface roughness due to mobility degradation, known as μ_{sr}. In this case, the functionality also relies on the transverse electric field.

So, we write:

$$\mu_s^{-1} = \mu_b^{-1} + \mu_{ac}^{-1} + \mu_{sr}^{-1} \tag{4.9}$$

where,

$$\mu_b = \mu_0 exp\left(-\frac{P_C}{N_{tot}}\right) + \frac{\mu_{max} - \mu_0}{1 + (N_{tot}/C_r)^{\alpha}} - \frac{\mu_1}{1 + (C_s/C_r)^{\beta}} \tag{4.10}$$

$$\mu_{ac} = \frac{B}{E_{\perp}} + \frac{C.N_{total}^{\lambda}}{T\sqrt[3]{E_{\perp}}} \tag{4.11}$$

$E_{\perp}$ represents the transverse component of the electrical field.

$$\mu_{sr} = \frac{D}{E_{\perp}^{\gamma}} \tag{4.12}$$

4.2 Device Calibration

The TCAD tool has first been calibrated according to the experimental data being used in the demonstration of hetero-gate dielectric tunneling field effect transistors [48] and has been plotted in figure .Kane's band to band tunneling model has been enabled. For energetic carriers, impurity scattering is not that important, and therefore $vsat$ is mainly determined by the temperature of the lattice. Since our TFET device is based on BTBT, therefore, a very high electrical field is generated at the source-channel tunneling junction. For accurate simulation of MOS devices, these effects must be accounted for. To consider high field mobility, Lombardi mobility model has been used. Bandgap narrowing model has also been included for device analysis so that heavily doping effects may be taken into consideration. Drift-Diffusion model has been used for the semiconductor device simulation of the charge carriers (electrons and holes), and is almost a standard model, being following in various other popular simulators. When the device is of shorter channel length, then Energy-balance Model available in the GENIUS tool must be incorporated during the analysis. For a carrier recombination mechanism, a combination of Shockley-Read-Hall (SRH), Auger and Direct Recombinations are being utilized. The electron-hole tunneling current is calculated by WKB integral. Device parameters used for the simulation

of this manuscript are similar as used for from the experimental data of [48]. The TCAD tool has first been calibrated according to the experimental data being used in the demonstration of hetero-gate dielectric tunneling field effect transistors as shown in figure 4.1.It can be observed that the proposed device shows the steeper subthreshold swing, with the drain current slope in agreement to the experimental data.

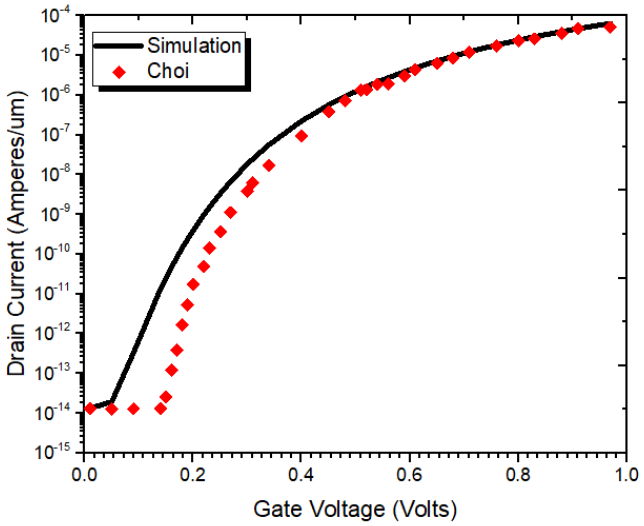
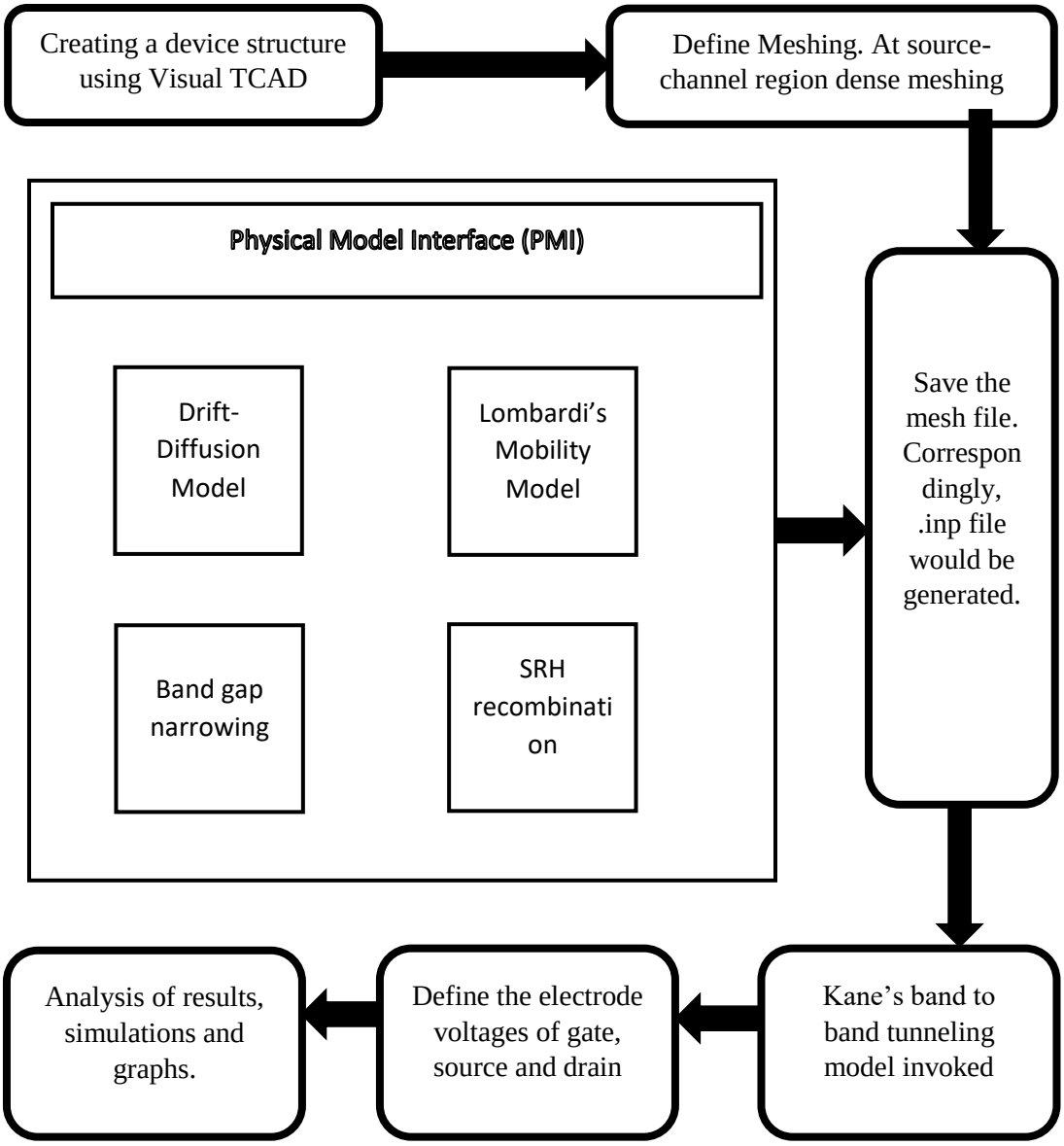


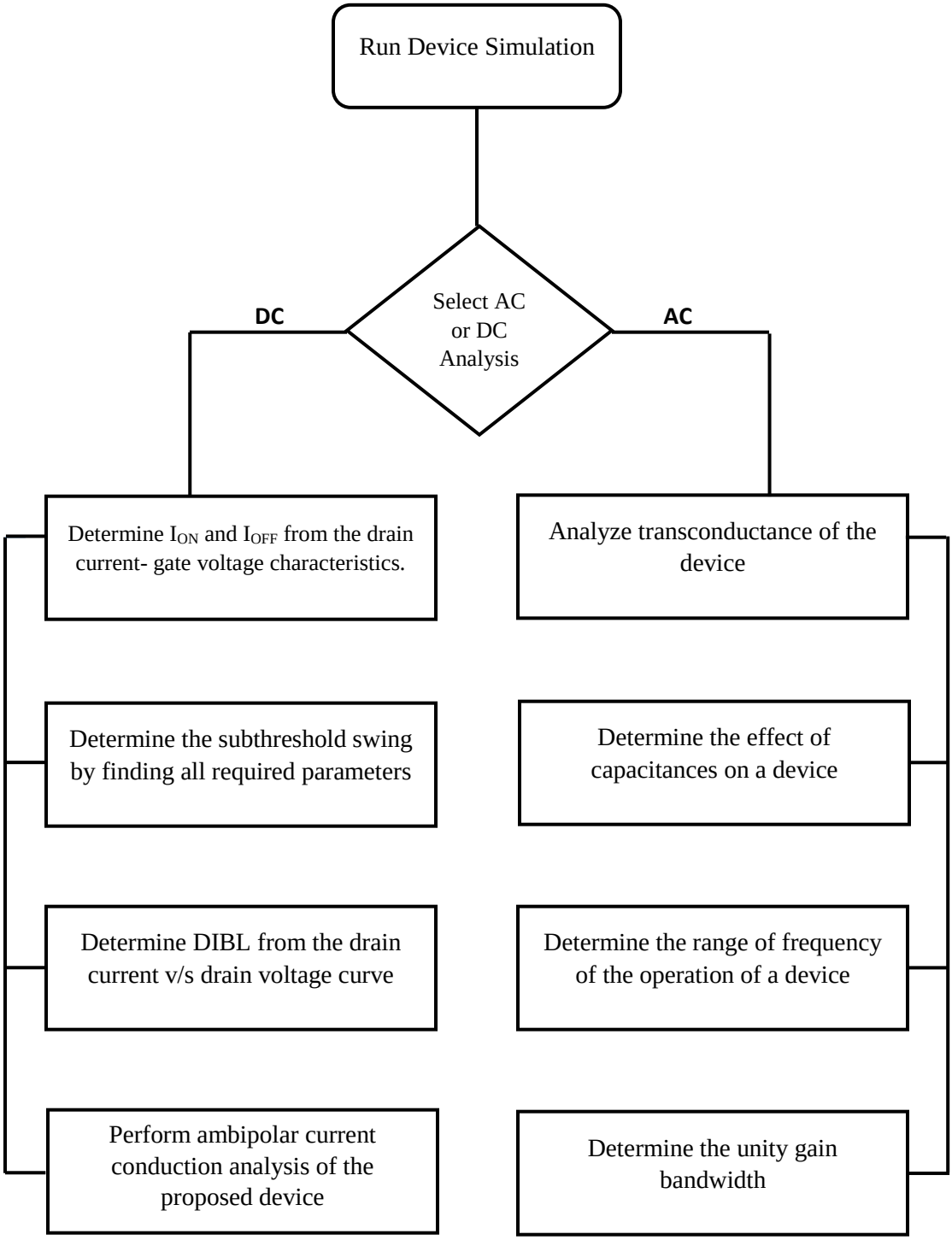
Figure 4.1 Calibration of the device with [43] representing I_D-V_{GS} characteristics

4.3 Methodology followed for carrying out the work:



The flow diagram discusses the process followed wile simulating the device in TCAD. Dense meshing is required at the source channel interface for enabling higher band to band tunneling. Various models briefed in section 4.2 need to be invoked for getting the results and carry out the analysis.

4.4 Sequence of steps followed in the Visual TCAD:



The flow chart describes the simulation of the device under two broad categories of DC analysis and AC analysis. In order to determine the ON current, OFF current and the I_{ON}/I_{OFF} ratio of the device DC analysis need to be carried out by setting the drain, source and gate voltages under "device simulation". When the drain current v/s gate voltage characteristics curve is plotted on the log scale, ON current and OFF current values become differentiable and therefore I_{ON}/I_{OFF} ratio can be calculated accordingly. The other parameters need to be calculated to determine subthreshold swing as well so as to measure the amount of steepness of the proposed structure. The device needs to be studied under linear and the saturation regions to understand the phenomenon of DIBL. Moreover, to study the analog/RF performance of the device AC analysis plays very important role. The parameters like transconductance, device efficiency, unity gain frequency, gate-drain capacitance, gate-source capacitance, etc. of the device are explored during the analysis.

CHAPTER 5: ELECTRICAL CHARACTERISTICS OF PROPOSED HETEROJUNCTION TFET

5.1 Introduction

The TFET structures being implemented on the tool would be summarized in this chapter. We would first study the transfer characteristics of the single-gated TFET, and would then compare it with the double gated Tunnel FET device. This would provide us insights regarding the role of the gate voltage to grasp the tighter control over the channel. Moreover, the conventional TFET structures being implemented have been compared with the heterojunction TFET device. In the later sections, we would present the proposed TFET structure and discuss its transfer characteristics and electrical characteristics.

5.2 Implementation of Previous TFET Structures and a Comparison

In the TFET structure given in figure 5.1, the source terminal has been heavily doped with p+, the channel is lightly doped/intrinsic and the drain terminal is heavily doped with n+. P+ has been heavily doped into the source terminal, and the channel is lightly doped n, and heavy doping of n+ done from drain terminal. The doping concentration was increased at the source side to minimize ambipolarity. If gate voltage applied is negative to the gate terminal, BTBT will be inhibited by lower drain doping.. The values of device parameters have been provided in table 5.1. Figure 5.2 represents the energy band diagram of the device at V_{GS}= 0 V (representing the OFF state) and V_{GS}=1.2 V (representing the ON state). When the low gate voltage is applied, the source's valence band lies below the conduction band of the channel. The consequence is that the BTBT is inhibited making the TFET turn OFF due to the low amount of drain current. When the voltage at gate is increased, band bending happens at the source side, as a consequence, the source's valence band is aligned, allowing electrons to tunnel from the source to the channel. This results in an increase in the flow of drain current as shown in the I_D-V_{GS} transfer characteristics graph of figure 5.3. The plot

shown represents the log axis on the y-scale, so that the range of I_{ON} and I_{OFF} can be determined from the graph.

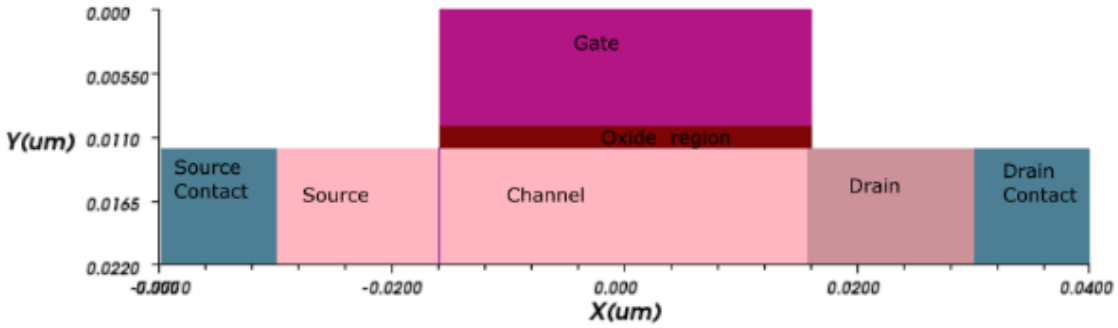


Figure 5.1 Schematic of Single gated TFET

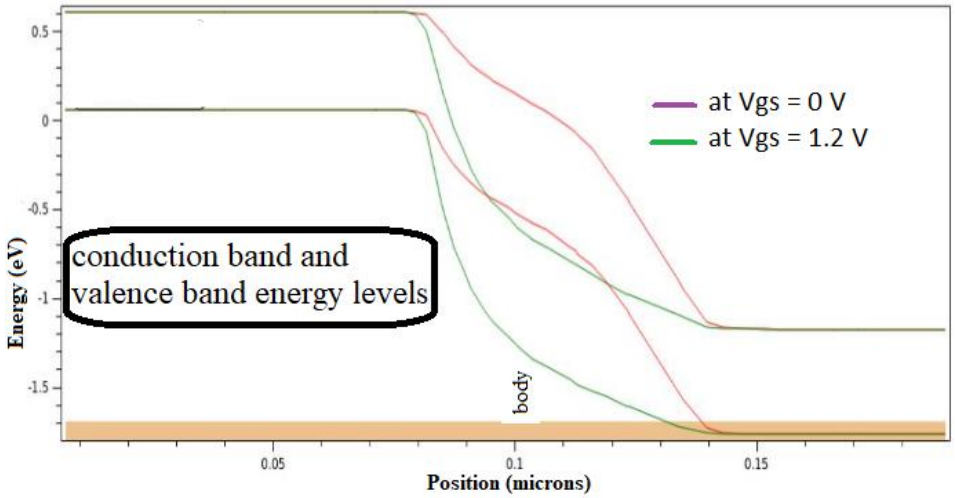


Figure 5.2 Energy Band Diagram of a single gate TFET

When the device is turned ON with sufficient gate voltage, then the drain current would be increased even further if the drain-source voltage was increased, as more and more electrons will travel from the source towards the drain. The figure shows the comparison curves for V_{DS} = 0.3 V, 0.6 V, 0.9 V, and 1.2 V (V_{DS} represents the drain voltage). Leakage current is lowest when V_{DS} is set to 0.3 V, and higher when V_{DS} is set to 1.2 V. Figure 5.4 illustrates the drain characteristics of a TFET. The voltage at the drain has been swept from 0 Volts to 1.2 Volts. The drain current begins to increase linearly and saturates when drain voltage exceeds $V_{GS} - V_T$, where V_{GS} represents the gate-source voltage and V_T represents

the threshold voltage. Although the leakage current of such a device seems low, on the other hand, driving current capability and ON current are both less.

Table 5-1 Parameter values for the simulated devices

Parameter	**Value**	**Units**
Gate Length	30	nm
Source Length	15	nm
Drain Length	15	nm
Channel length	30	nm
Oxide thickness	2	Nm
Source doping	1e+20	/cm^3
Drain doping	1e+19	/cm^3
Channel doping	1e+16	/cm^3

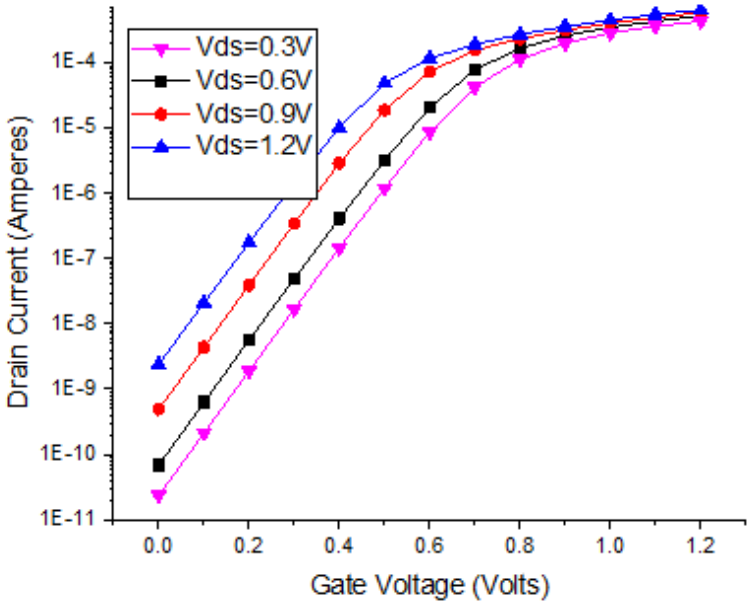


Figure 5.3 log I_D v/s V_{GS} curve for Single Gate TFET

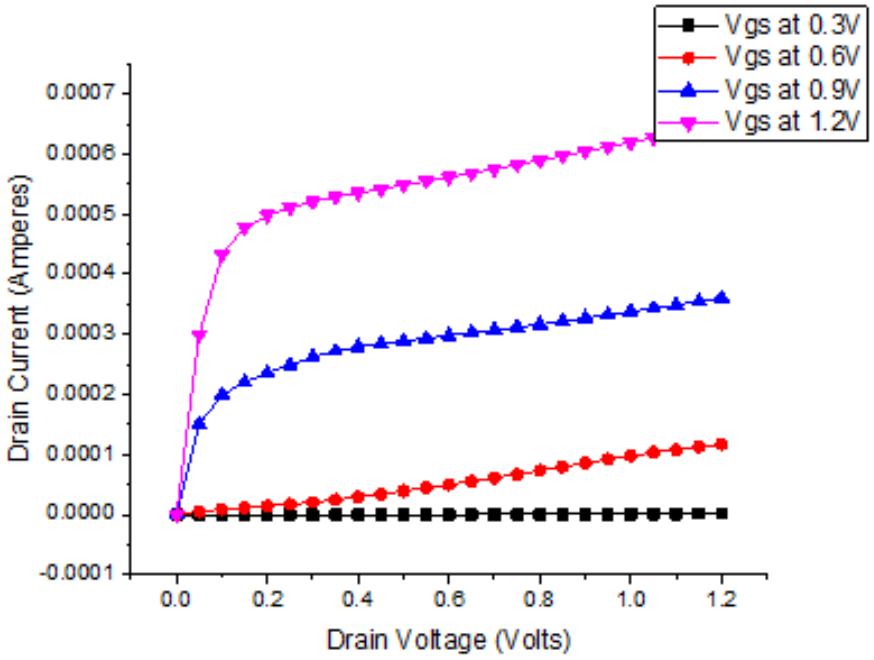


Figure 5.4 I_D v/s V_{DS} curve for Single Gate TFET

In the TFET structure given in figure 5.5, the gate is available on both sides of the device, thereby giving the structure greater electrostatic control over the channel. In context to double gated transistors, the drive current is improved almost by a factor of two. It also means that the gate capacitance is doubled compared to a single gate. At a given transistor width, for an equal power-delay product double gated devices need to operate at half times lesser voltage than that of a single gate device. To achieve the same C goal. the drive current should be, in a single gate system at $V_{DD}/2$, 1/2 times that of the drive current. The band diagram in figure 5.6 suggests that the BTBT is enabled only when the sufficient gate voltage is provided to allow the electrons to flow to the conduction band in the channel from the source's valence band.

The I_D-V_{GS} characteristics graph of the double gated TFET is given in figure 5.7. The graph again depicts that the drain current does increase when a sufficient gate voltage is applied for creating an inversion layer. For different values of the drain voltage, transfer of electrons from source to drain enhances, leading to the higher ON current. Furthermore,

the I_D-V_{DS} drain characteristics of the device have been plotted in figure 5.8. Again, for a given sufficient gate voltage, it can be shown that, there is a linear dependence of the drain current on the drain voltage, until it saturates at the point of $V_{DS} > + V_{GS} - V_{TH}$.

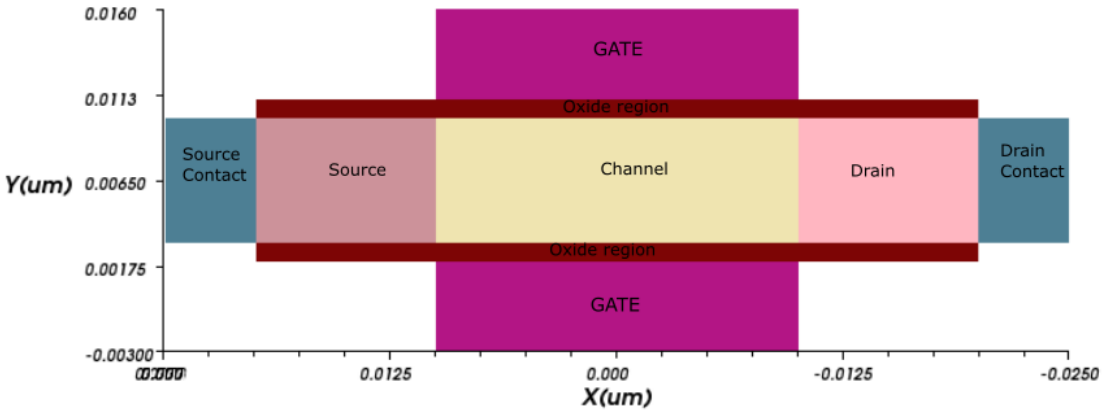


Figure 5.5 Schematic of double gated TFET

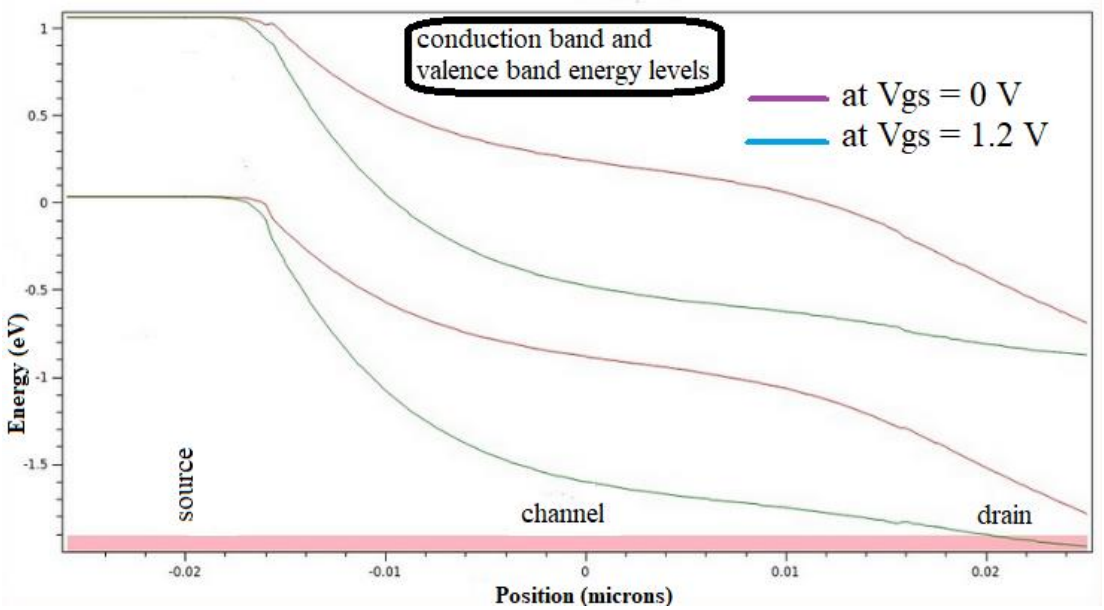


Figure 5.6 Band diagram of double gated TFET structure

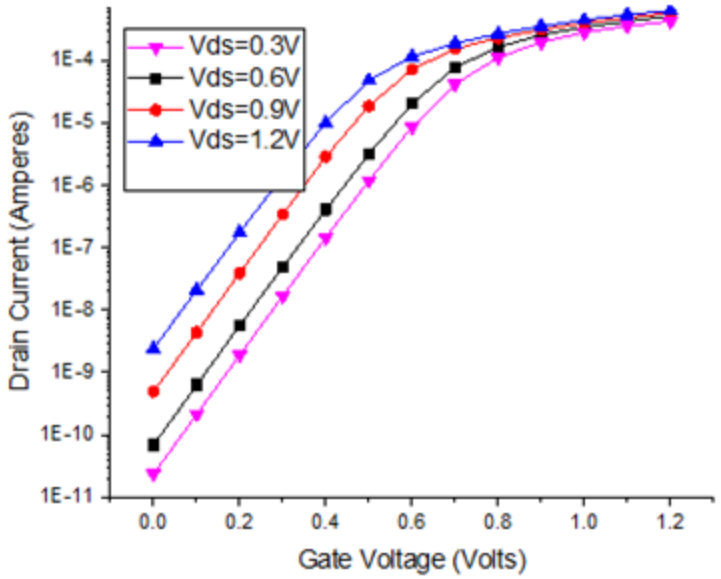


Figure 5.7 log I_D-V_{GS} characteristics of double gated TFET structure

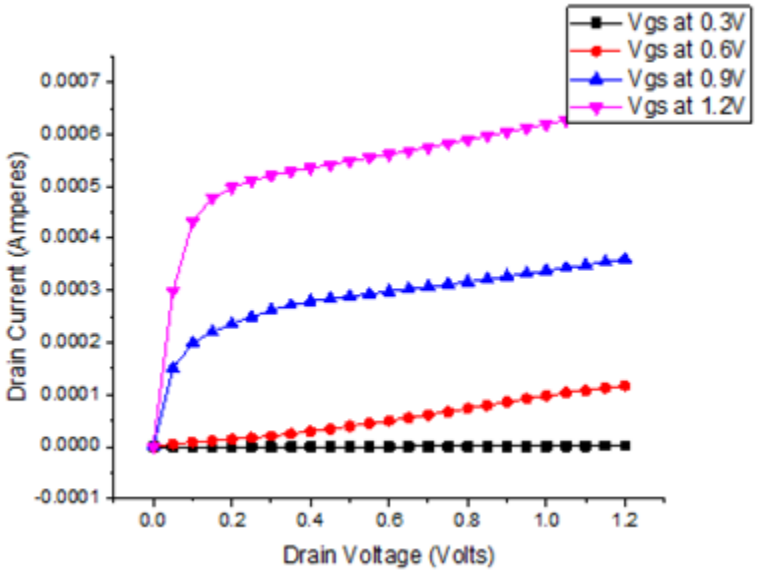


Figure 5.8 I_D-V_{GS} characteristics of double gated TFET structure

The comparison of the drain current values obtained for single and double gated TFETs are plotted in the graph shown in figure 5.9.

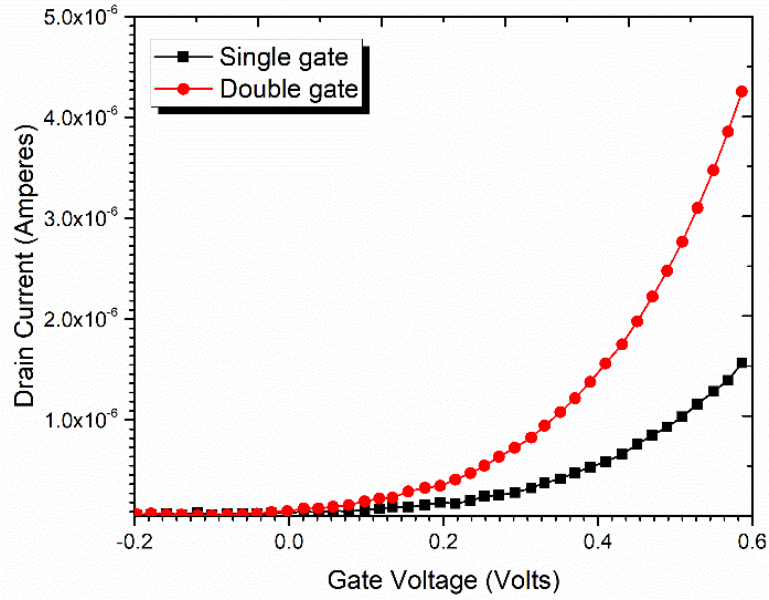


Figure 5.9 I_D-V_{GS} comparison curves for single and double gate TFET.

5.3 Implementation of proposed SiGe based heterojunction based TFET

5.3.1. Device Architecture and Simulation Set up

SiGe is one of the most attractive material systems for TFET applications due to its flexibility, mature synthesis techniques, and controllable bandgap. The controllable bandgap allows for effective tunnelling injection as well as ambipolar conduction suppression. The proposed SiGe based heterostructure tunnel FET has been shown in Fig. 5.10. The material used at source region is $Si_{1-x}Ge_x$, where x is a molar concentration of Germanium. The use of a compound SiGe material ensures a low energy band gap from the source side, thus decreasing the width of the tunneling. The drain current will increase as a result of this. The source and the drain terminals are attached through the metallic contacts. The gate terminal is made up of polysilicon and remains insulated from the channel due to the SiO_2 layer. The impact of using polysilicon is to align the gate mask during the fabrication process such that the parasitic capacitances are reduced. The other advantage is that the smaller threshold voltage could be obtained. The spacers have been used at the source and the drain side to enhance the ON current. The dense meshing must be done at the source channel tunneling junction so that BTBT is enhanced, as depicted in

figure 5.11. Moreover, a hetero-dielectric buried oxide (BOX) layer has been used just below the channel to suppress the ambipolar transport during negative gate-source voltage. High-*k* dielectric gate material has been partially included at the source region to increase ON current and to reduce the ambipolar current, a silicon dioxide has been used as a dielectric at the drain side. The Schrodinger-Poisson solver can be used to rigorously treat quantum confinement (QC), but the computational burden makes it unsuitable for device optimization. As a result, the treatment of QC is as follows: The electron density in the channel is so low in the low current regime that the redistribution of electrons due to QC does not affect the electrostatic potential profile As a result, QC has been ignored in the research.

All the device simulations have been performed on a licensed version of Visual TCAD (version 1.9.2-3). Kane's local band to band tunneling model has been enabled. To take high field mobility into consideration, Lombardi mobility model has been used. Band gap narrowing model has also been included for device analysis so that heavy doping effects may be taken into consideration.

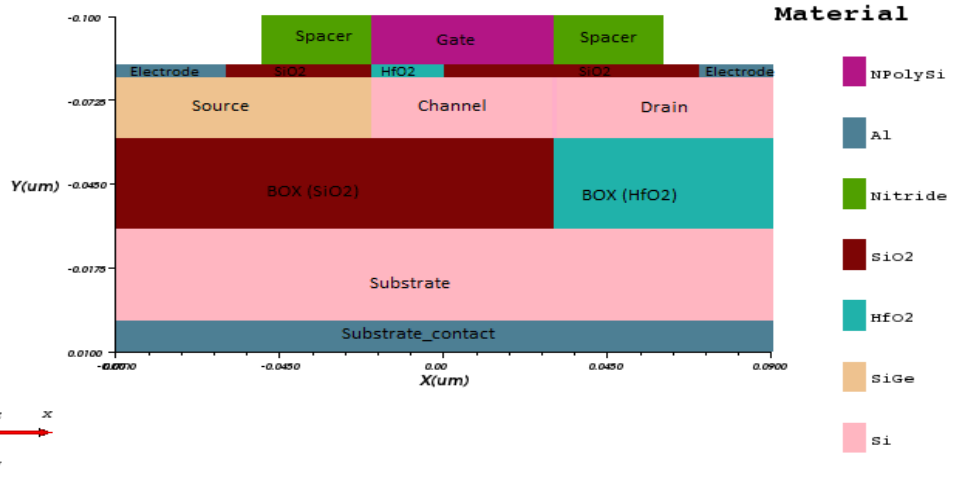


Figure 5.10 Proposed SiGe based heterostructure tunnel FET

Shockley-Read-Hall recombination and Fermi Dirac statistics models have also been included during the simulation. The values of work function, length of spacers, the material of spacers, and length of high-κ dielectric material have been optimized by running

rigorous simulations. Device parameters used for the simulation purpose have been provided in Table 5.2 given below.

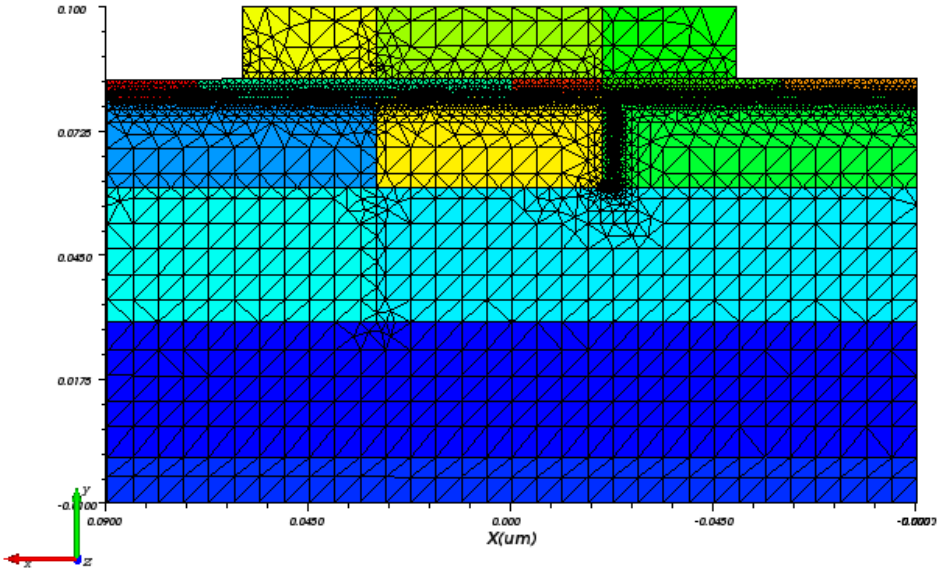


Figure 5.11 Representation of dense meshing at the source-channel tunneling junction of the device

Table 5-2 Device Parameter and their values used during the simulation

Region	Material	Length	Doping
Gate	NPolySi	50 nm	-
Source	SiGe	70 nm	5×10^{20} cm^{-3} (p^+-type)
Channel	Si	50 nm	1×10^{15} cm^{-3} (p-type)
Drain	Si	60 nm	5×10^{18} cm^{-3} (n-type)
Spacer	Nitride	30 nm	-
High-k gate insulator	HfO_2	20 nm	-
BOX layer	SiO_2+HfO_2	120 + 60 nm	-

5.4 Electrical Characteristics of the device:

This section focuses on explaining the electrical characteristics of the proposed SiGe based heterostructure tunnel FET. For optimization of various parameters, simulations have been carried out on the structure.

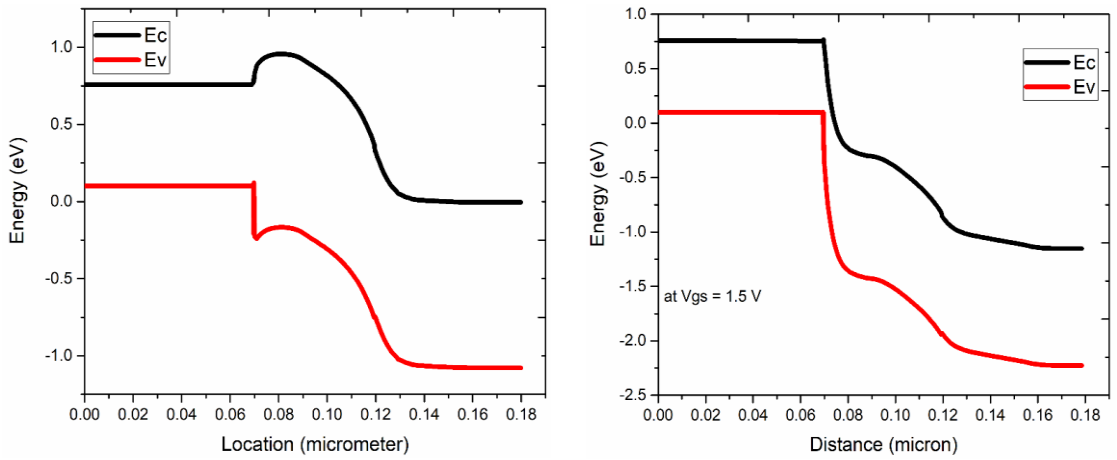
Here we shall discuss the tunneling rate of the device, transfer characteristics, and the subthreshold swing parameter of the device.

5.4.1. Energy Band Diagram

Kane's tunneling model has been utilized to find band to band tunneling rate for a given semiconductor, and can be expressed as:

$$G^{BB} = A.BTBT.\frac{E^2}{\sqrt{E_g}}.\exp\left(-B.BTBT.\frac{E_g^{3/2}}{E}\right) \quad (5.1)$$

Here A.BTBT and B.BTBT are empirical fitting parameters, E denotes the electrical field and E_g represents the energy band gap. Figure 5.12 shows the energy band diagram for a proposed device. When no gate-source voltage (V_{GS}) is applied, BTBT is inhibited, hence device remains in OFF state when $V_{GS} = 0\,V$ as shown in figure 5.12(a). When a sufficiently high gate-source voltage is applied, band bending occurs at source and electrons get tunnelled from valence band of the source to the conduction band of the channel, hence turning the TFET device ON. Figure 5.12(b) shows band bending at V_{GS} = 1.5 V.



(a) (b)

Figure 5.12 SiGe based TFET energy band diagram (a) at V_{GS} = 0 V (b) at V_{GS} = 1.5 V

5.4.2. Electrical Field and Surface Potential of the device

Figure 5.13 shows the variation of an electrical field with the application of gate-source voltage. As the gate voltage is increased from V_{GS}= 0 V to V_{GS}= 1.5 V, the electrical field increases. Figure 5.14 shows the surface potential of the device. It is evident from the figure that the potential at the source junction is low. While proceeding towards the drain junction, the surface potential increases. Moreover, the surface potential increases as gate-source voltage is increased, as seen in the graph.

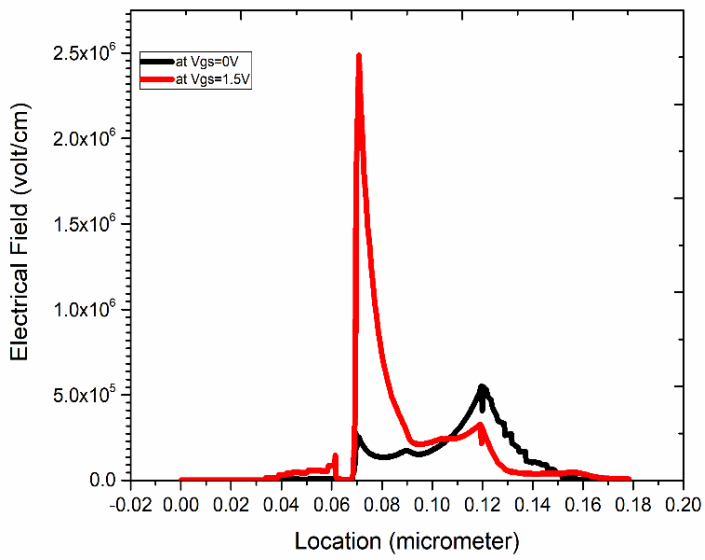


Figure 5.13 Electric Field Variations at the source

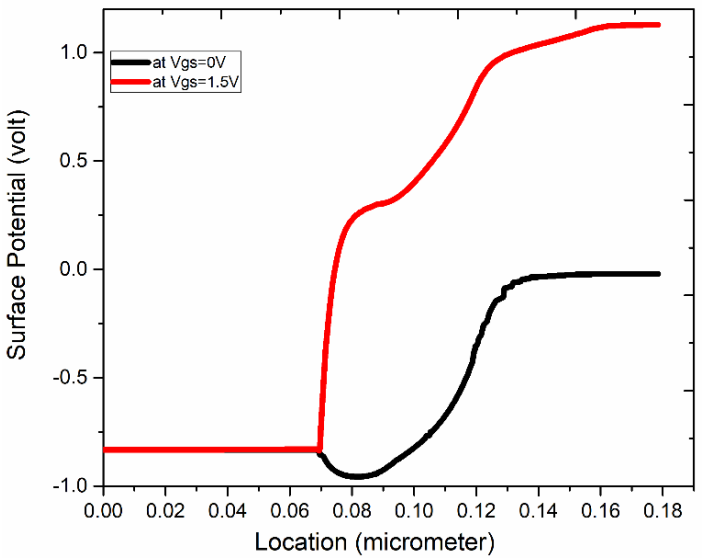


Figure 5.14 Surface Potential of a device

5.4.3. Transfer Characteristics: Drain Current v/s Gate-Source Voltage

Figure 5.15 represents the transfer characteristics of SiGe based heterostructure tunnel FET. During the simulation, the gate-source voltage has been varied from – 0.5 V to 1.5 V. While as, the drain-source voltage has been kept constant for one simulation. Figure 5.16 represents variation in a drain current for different drain source voltages on a log scale. It is clear from the figure that as gate-source voltage is increased, the drain current also increases. As long as TFET is in the linear region, with an increase in drain source voltage (V_{DS}) the drain current increases. However, when the TFET moves toward the saturation region, the drain current remains ideally constant and will have no effect of V_{DS}. Practically, a small increase in I_{DS} occurs in response to an increase in V_{DS}, due to the fact that the resistance of inversion layers decreases as the length of the inverted channel is shortened. From figure 5.16, it has been measured that at V_{DS} = 0.05 V, I_{ON}/I_{OFF} ratio obtained is 2.34×10^{10}, while as, at V_{DS} = 1.2 V, I_{ON}/I_{OFF} ratio obtained is 3.72×10^{10}. The results obtained for the drain current- gate voltage characteristics have also been compared with the existing TFET structures of different architectures like DGTFET, JLTFET, and the vertically L shaped gate and U shaped channel devices. All the device simulations have been performed at the drain voltage of volt. Figure 5.17 depicts that the ON current of the proposed device is significantly higher. The type of material used by researchers for these respective devices and the values of the average subthreshold swing is provided in Table 5.3.

Figure 5.18 plots the I_{ON}/I_{OFF} of all those devices which have been compared in Table 5-3. The value obtained for our device is well above the ITRS requirements. It might appear that devices like JLTFET could result in higher I_{ON}/I_{OFF} ratios, but it must be noted that such devices are having subthreshold swing values on the higher side. So, there is a trade-off regarding the steepness of the device. Figure 5.19 plots the subthreshold swing values of the devices being compared. It is evident that the subthreshold swing has deteriorated in structures like InGaN, L shaped gate TFETs, and a few junctionless TFETs.

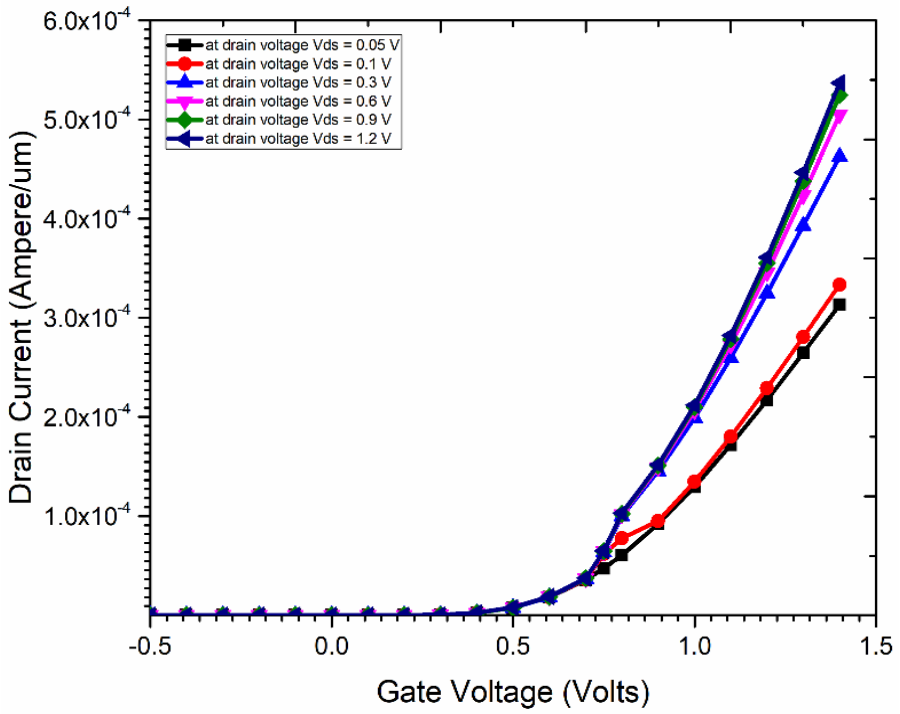


Figure 5.15 Transfer characteristics I_D vs V_{GS} of a device.

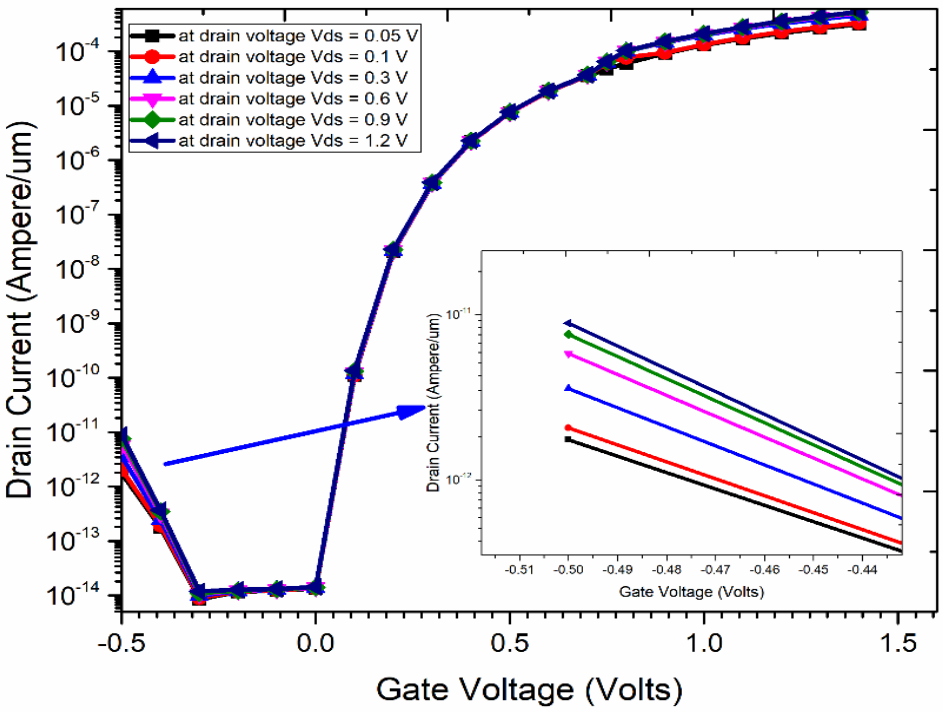


Figure 5.16 log I_D vs V_{GS} Transfer characteristics of a device

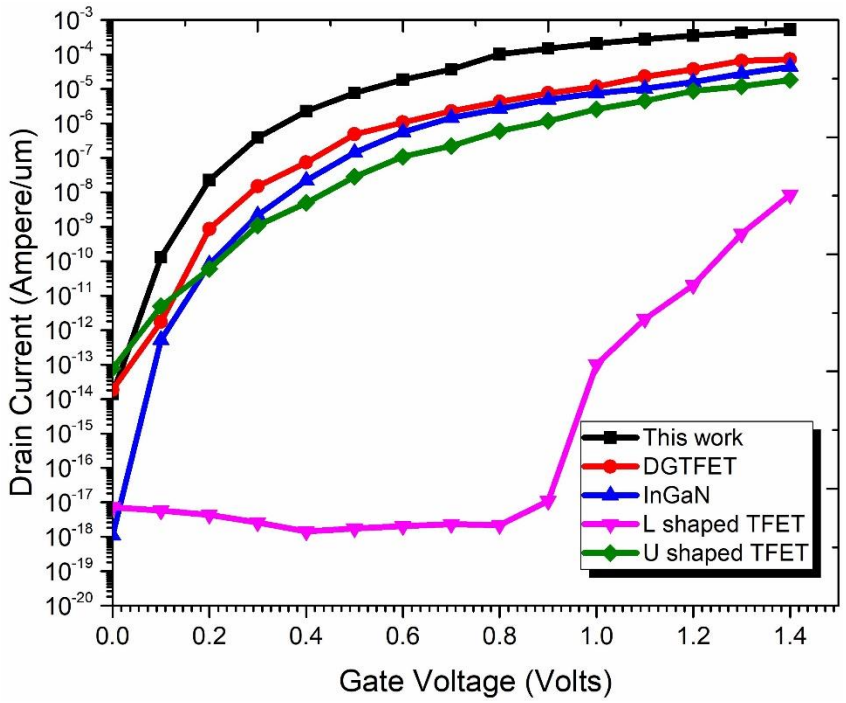


Figure 5.17 Comparison of the work with conventional DGTFET, Group III-V and vertical tunnel FET devices

Table 5-3 Comparison of existing TFET architectures with the proposed device at the drain voltage of 1 volts

Reference	**Year**	**Device**	**Material**	**I_{ON} (A/μm)**	**I_{ON}/I_{OFF}**	**SS_{avg} (mV/decade)**
Boucart [25]	2007	DGTFET	Si	1E+05	2E+09	57
Toh [55]	2007	DGTEFT	Si	1.18E-05	6.32E+08	25
Jagadeesh [94]	2013	JLTFET	Si	1.1E-05	1.10E+12	≈100
Kim [110]	2012	L shaped TFET	Si	8.53E-09	1.18E+09	68.07
Anand [114]	2016	JLTFET	SiGe	4.88E-05	6.91E+12	64.79
Xiaoling [82]	2018	JLTFET	InGaN	0.8E-05	6.86E+12	41.3
Haiwu Xie [115]	2020	U shaped TFET	SiGe	1.59E-05	4.63E+11	35
Tripathy [116]	2020	VTFET	Si	1.45E-07	7.8E+09	67
Singh [117]	2020	PGPTFET	Si/Ge	3.04E-05	1.54E+11	47
This work	2020	HDB TFET	SiGe	0.537E-03	3.70E+10	28.57

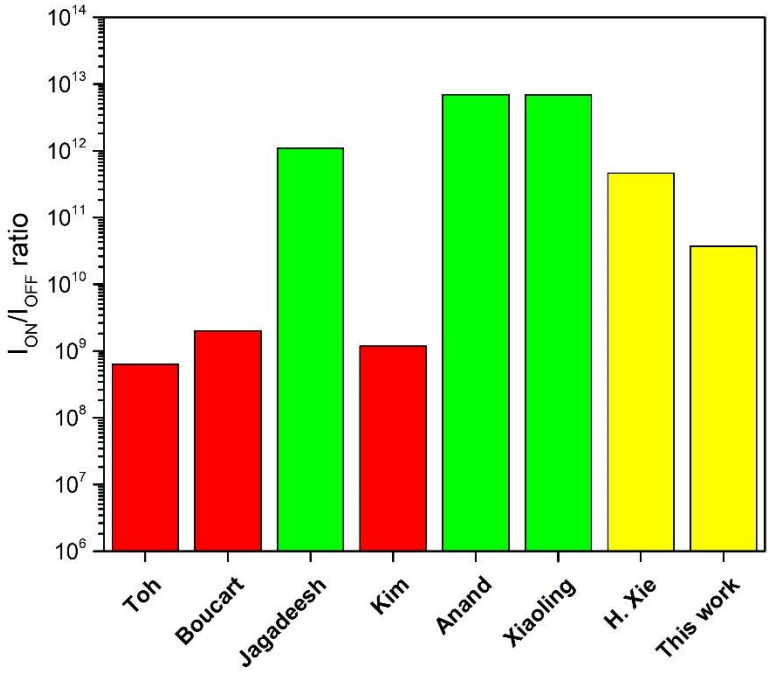


Figure 5.18 Comparison of I_{ON}/I_{OFF} for various TFET device architectures

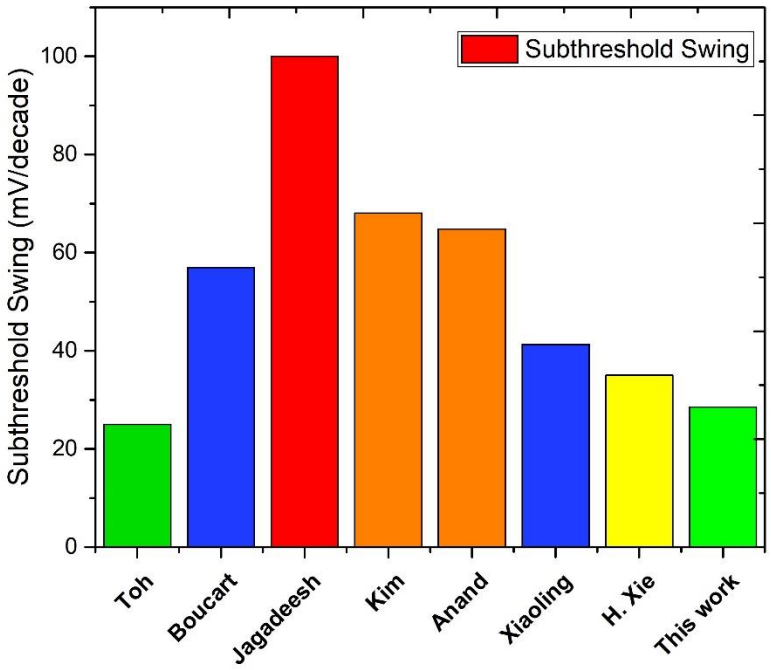


Figure 5.19 Comparison of subthreshold swings for various TFET device architectures

5.4.4. Subthreshold Swing

The amount of gate voltage needed to increase the drain current by 10 folds is called as subthreshold swing and its units are mV/decade. This parameter must be as small as possible so that even a little variation in gate to source (V_{GS}) voltage can produce larger variation in the drain current, thus making a transistor suitable for low voltage operation.

The subthreshold swing in terms of the drain current is expressed as:

$$S = \frac{dV_G}{d\psi_s}\frac{d\psi_s}{d(\log_{10} I_D)} \cong \left(1 + \frac{C_d}{C_{ox}}\right)\ln 10\,\frac{kT}{q} \tag{5.2}$$

Where V_G denotes the gate voltage, Ψ_s represents the surface potential, I_D is the drain current, C_d denotes the depletion capacitance, C_{ox} is the oxide capacitance and $^{kT}/_{q}$ is the thermal voltage. For a MOSFET the ideal value that can be achieved is 60 mV/decade.

We have calculated the average subthreshold swing of the proposed device as per the following expression:

$$SS_{avg} = \frac{V_{TH} - V_{OFF}}{log\left(\frac{I_{TH}}{I_{OFF}}\right)} \tag{5.3}$$

Here V_{TH} represents the threshold voltage, V_{OFF} is the gate to the source (V_{GS}) voltage at the minimum drain current, whereas, I_{TH} and I_{OFF} represents drain currents at V_{TH} and V_{OFF} respectively. We have calculated threshold voltage using the constant current method. The threshold voltage has been found out as 0.27 Volts. From log I_D vs V_{GS}, the required parameters can be found out. For the proposed device, the average subthreshold swing has been calculated as 28.57 mV/decade.

5.5 Short Channel Parameter Study Of SiGe Based TFET Structure

5.5.1. Drain Induced Barrier Lowering

Figure 5.20 shows the drain current transfer characteristics of the device. The device shows an excellent subthreshold swing of 28.57 mV/decade and maintains I_{ON}/I_{OFF} ratio of 3.72×10^{10}. Furthermore, drain induced barrier lowering (DIBL) has been calculated

by observing the linear I_D vs V_{GS} curve at the linear and the saturation mode as shown in figure 5.21. DIBL is a short-channel effect mechanism in which the depletion region widens with an increase of drain voltage and thus lowers the potential barrier at the source in short channel devices. DIBL obtained in our device is of the order of 3.636 mV at the channel length of 50 nm. The threshold voltage of a device has been found out by using a constant current method, and the gate voltage has been noted at the drain current value of 10^{-7} A/µm, as can be seen in figure 5.22 Thus, it can be said that the short channel effect of DIBL is greatly restrained in our proposed design. The equation used for DIBL calculation is given as:

$$\mathrm{DIBL} = \frac{V_{T_{LIN}} - V_{T_{SAT}}}{V_{D_{SAT}} - V_{D_{LIN}}} \tag{5.4}$$

Where $V_{D_{SAT}}$ and $V_{D_{LIN}}$ are the supply voltages at the saturation and the linear mode. $V_{T_{LIN}}$ and $V_{T_{SAT}}$ are the voltages obtained using the constant current method at the linear and the saturation mode, respectively.

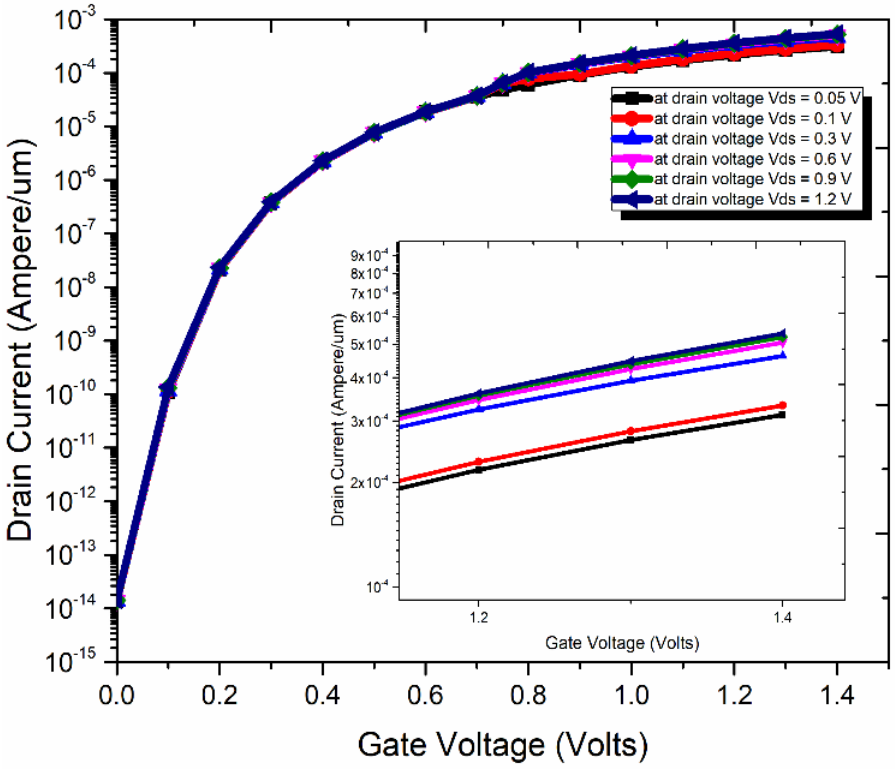


Figure 5.20 I_D-V_{GS} Transfer characteristics curve

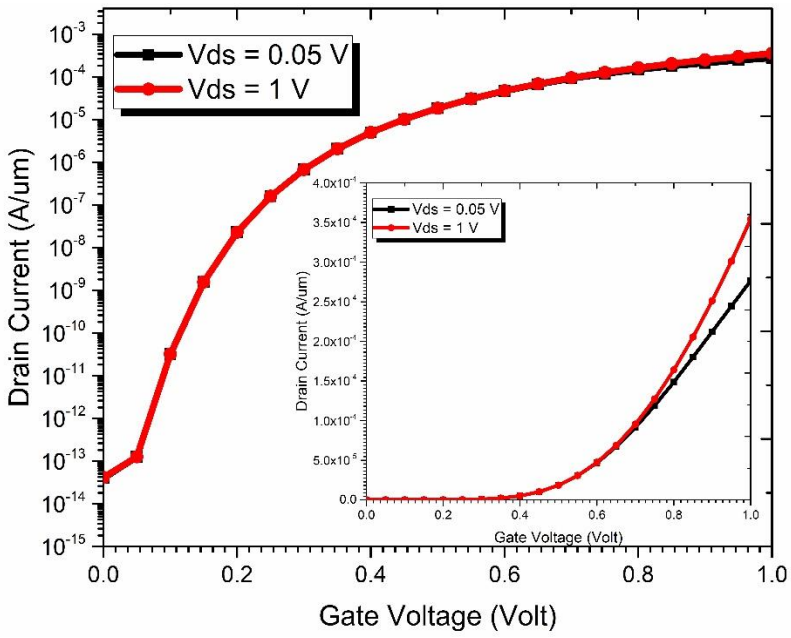


Figure 5.21 Graph extraction at linear and saturation regions.

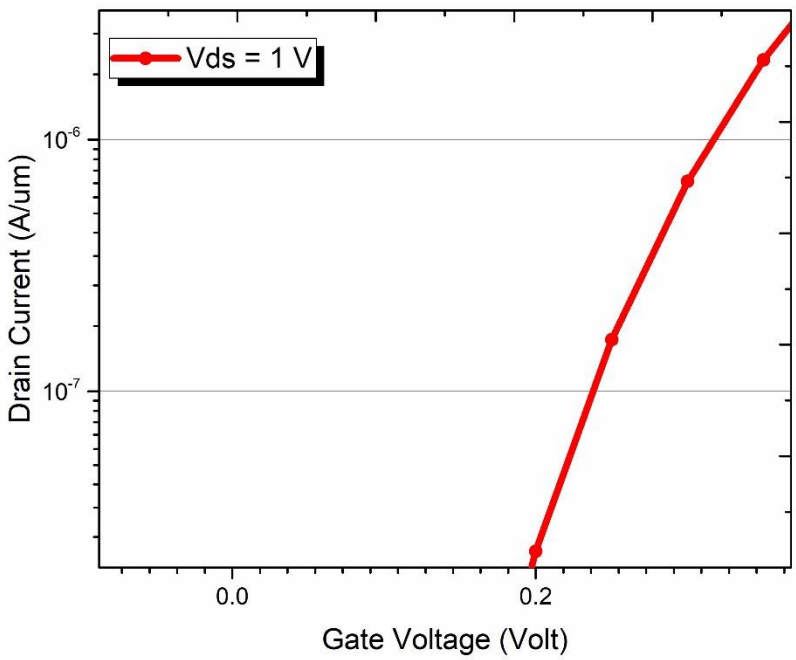


Figure 5.22 Calculation of DIBL with constant current method (drain current of 10^{-7})

Furthermore, when the gate length was scaled to 40 nm, DIBL obtained was about 2.222 mV. The procedure for finding the values can be observed from figure 5.23.

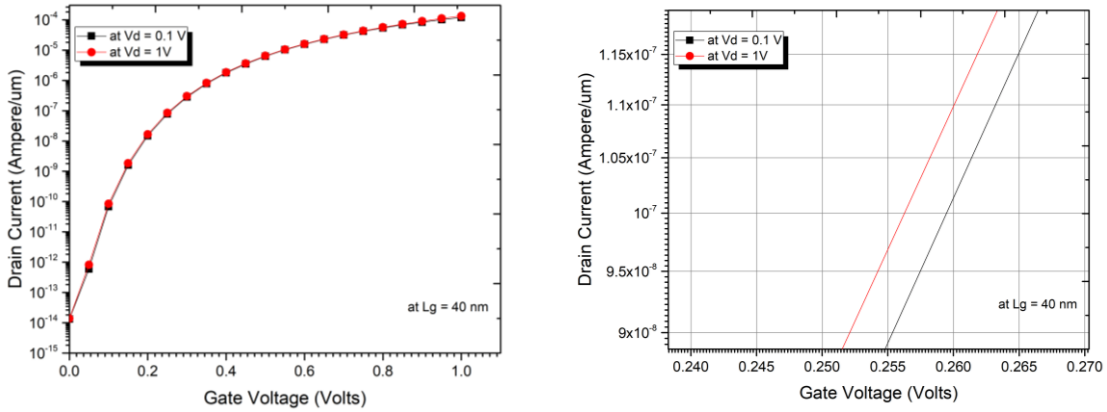


Figure 5.23. DIBL calculation with constant current method at L_g == 40 nm. (a) Log scale (b) Zoom in of image at 10^{-7} drain current.

5.6 Suppression of Ambipolar Transport

The doping level concentrations in the drain and the source regions are one of the distinctions between a MOSFET and a TFET. In TFETs, the opposite type of doping is done at the drain and the source regions. So, when a negative gate voltage is applied band to band tunneling occurs at the drain-channel junction. This results in the rise of the leakage current. The same phenomenon is observable in conventional TFETs [3, 110, 131, 132]. However, in our proposed device, a buried oxide (BOX) layer of 30 nm thickness has been used. It results in the depletion of the drain region at drain-channel interface. It can be seen from figure 5.24, the ambipolar current is suppressed up to $V_{GS} = -0.3$ volts.

The techniques like low-κ spacers, gate-drain overlap, and low drain doping have been used by the earlier researchers to reduce the ambipolar conduction in TFETs. However, during fabrication most of these methods present complexities resulting in low ON current. Scaling below 30 nm is difficult to achieve with the gate-drain overlap method. In our study, we have implemented the structure with the hetero dielectric buried oxide layer

(BOX). In this way, it would be possible to scale down the proposed structure below 10 nm as well without any serious degradation in the ON current. The graph in figure 5.25 compares the results obtained with the conventional silicon based TFET device and the vertical tunneling device, L shaped gate TFET, and the lateral TFET device.

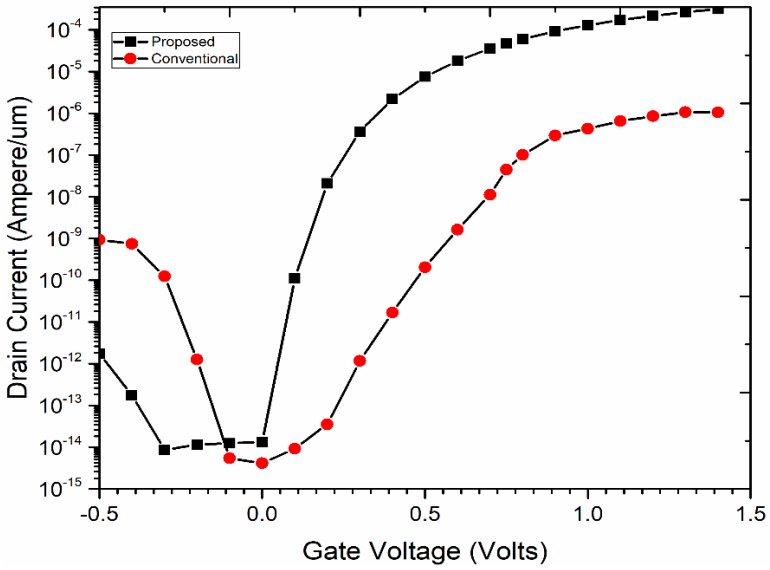


Figure 5.24 comparison of ambipolar current with conventional TFET device

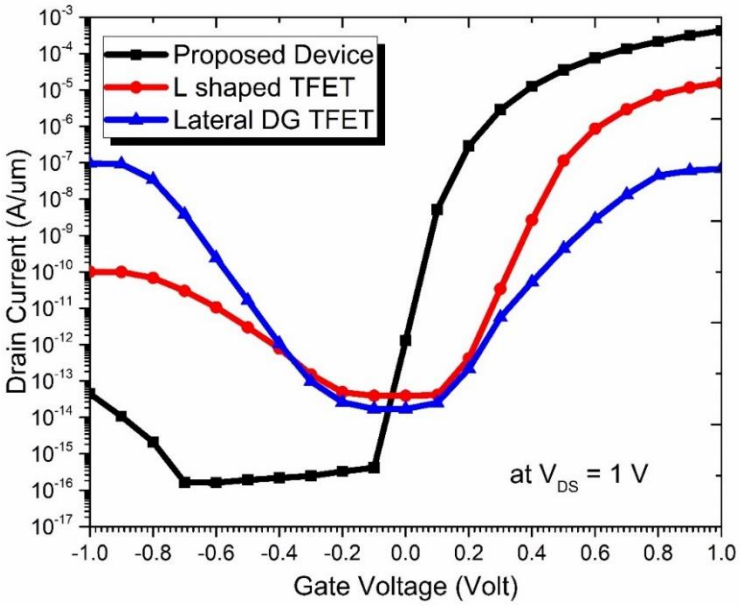


Figure 5.25 comparison of ambipolar current with DGTFET and L-shaped TFET device

CHAPTER 6: PARAMETER VARIATIONS OF SiGe BASED TFET STRUCTURE

6.1 Introduction

As technology progresses, process-induced variations result in the change of electrical characteristics in the device. The fluctuations in these devices' electrical properties caused by process-induced variations in channel length, silicon thin film thickness, and gate oxide thickness must be predicted and accordingly controlled to improve device reliability [133-136]. In traditional TFET structures, the fluctuation in the ON-current is found to be substantial and therefore an effort should be made to reduce it. The process parameters considered in our study are work function, molar fraction variation of SiGe source material, spacer length variation, gate dielectric layer variation, buried oxide layer material variation [57, 137, 138].

6.2 Work Function Variation of Gate Material

Work function can be defined as the minimum amount of energy required to knock out an electron to the outside surface. For our simulation purpose, we have varied the work function in the range of 4.1 eV to 4.7 eV. The corresponding drain current characteristics obtained have been plotted in figure 6.1. The inset graph of the figure demonstrates that the ON current decreases with an increase in the gate work function. However, the OFF current deterioration is maximum at $\phi = 4.17$ eV, and can be observed from the log curve of drain characteristics in figure 6.1. Thus, it can be deduced that decreasing the gate work function can have a serious impact on the OFF current of a device. However, with a small trade-off in the ON current, we can significantly decrease the OFF current by using a high gate work function. The variations in the ON and OFF currents with the change in the work function values are shown in figure 6.2. The OFF current is lowest at the gate work function of $\phi = 4.7$ eV. The highest I_{ON}/I_{OFF} ratio of 1.516×10^{10} has been obtained at $\phi = 4.7$ eV.

The work function of the device also determines the threshold voltage. In order to adjust the V_{TH}, it is important to have a tunable work function. Therefore, a gate material with a

work function that places its Fermi level close to the middle of the silicon band gap is desired so that the work function difference between the gate electrode and the near intrinsic silicon film can be adjusted to optimize the threshold voltages.

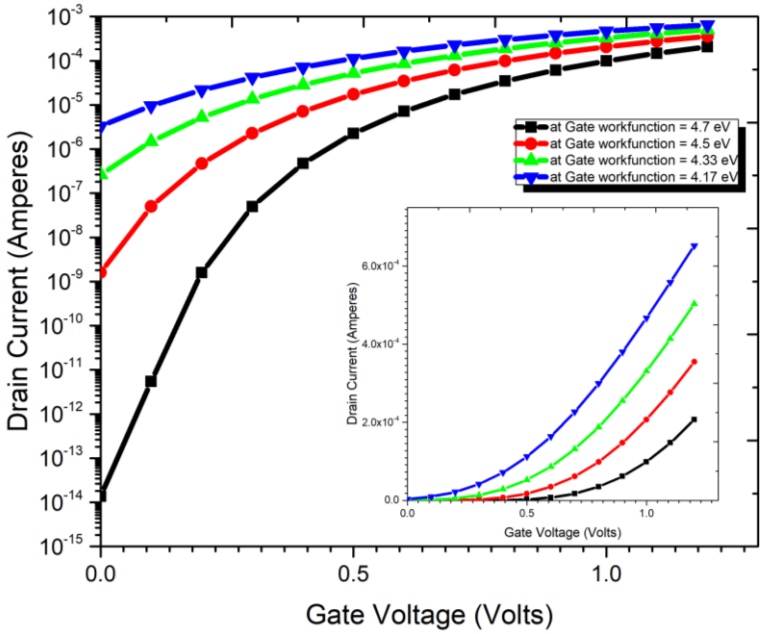


Figure 6.1 Work function variation for the device

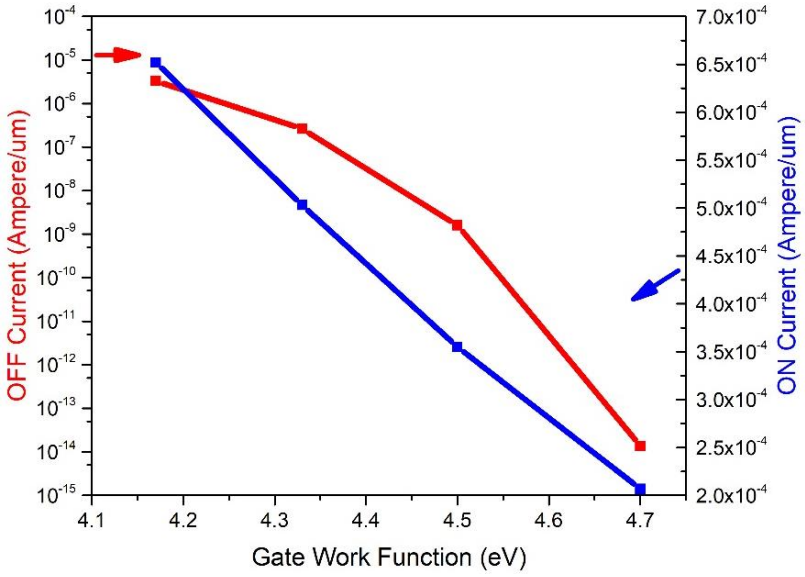


Figure 6.2 ON current and OFF current variations with gate work function

6.3 Molar Function Variation of $Si_{1-x}Ge_x$ at the Source Region

TFETs with silicon as a material suffers from low ON current and high subthreshold swing. The reason for this is the high energy band gap of silicon. To counter this, Germanium has been a choice for many researchers. Germanium has comparatively a smaller energy band gap so results in the enhancement of ON current. However, the limitation of such structures is that the OFF current also increases, which puts a serious constraint on its use. To maintain high I_{ON} and low I_{OFF} simultaneously, $Si_{1-x}Ge_x$ has been used as source material. The performance of the device is affected by varying the molar fraction x. The drain current variation with changes in the molar fraction x is shown in figure 6.3. The graph clearly shows that the ON current increases as the molar concentration x of Germanium is changed. It is due to the more contribution of Germanium, which results in the smaller width due to the smaller energy band gap. This results in the higher band to band tunneling, thus increasing the drain current. With the variation of molar concentration x, the effect on the OFF current is evident from figure 6.4. Since the reverse leakage current in Germanium is 1000 times more than that of Silicon, so the OFF current will also increase as the percentage composition of Germanium content is increased. It can be observed that the minimum OFF current at V_{GS} = 0 V is 1.33×10^{-14} at a molar fraction $x = 0.65$. The variations in the I_{ON}/I_{OFF} currents with the change in the molar fraction are depicted in figure 6.5.

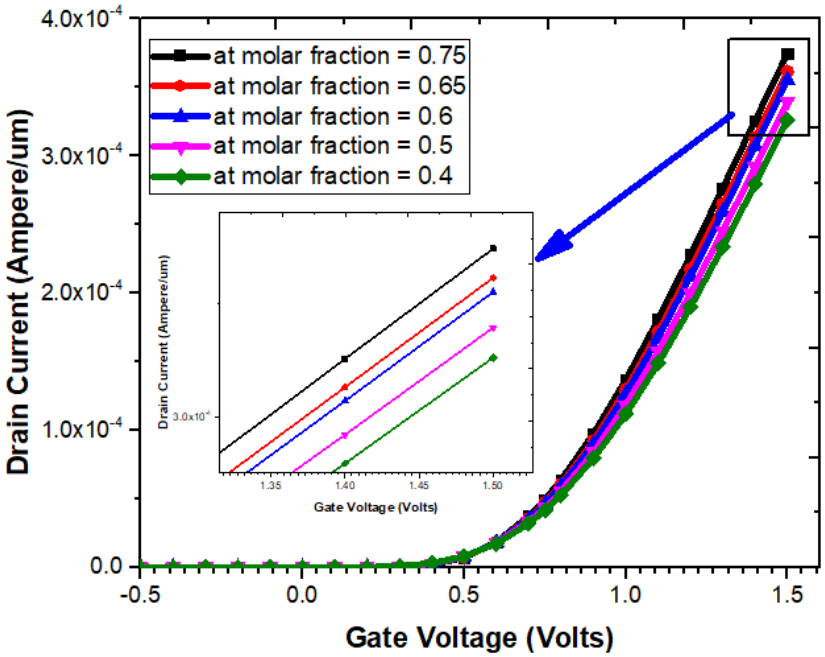


Figure 6.3 Drain current characteristics with molar fraction variation

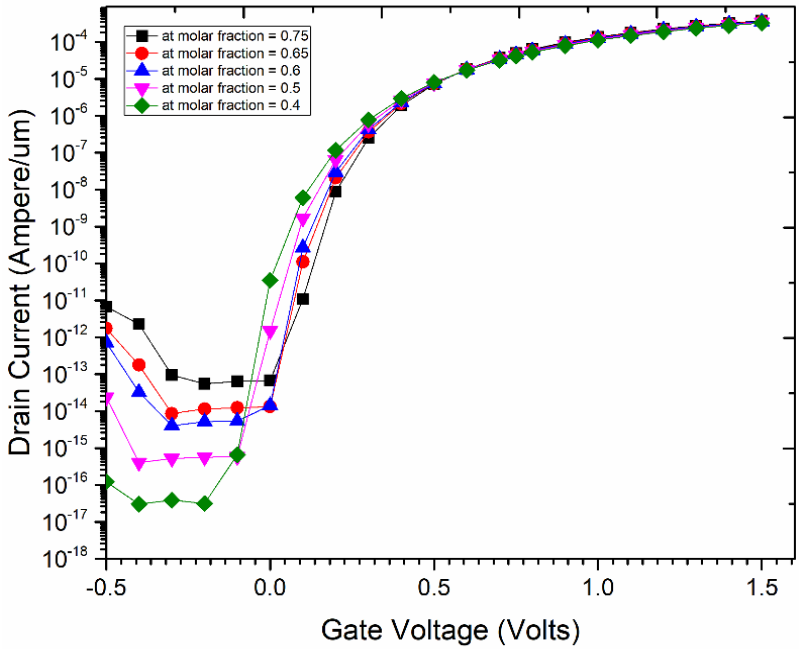


Figure 6.4 Drain current characteristics with molar fraction variation on (a) Linear scale (b) Log scale

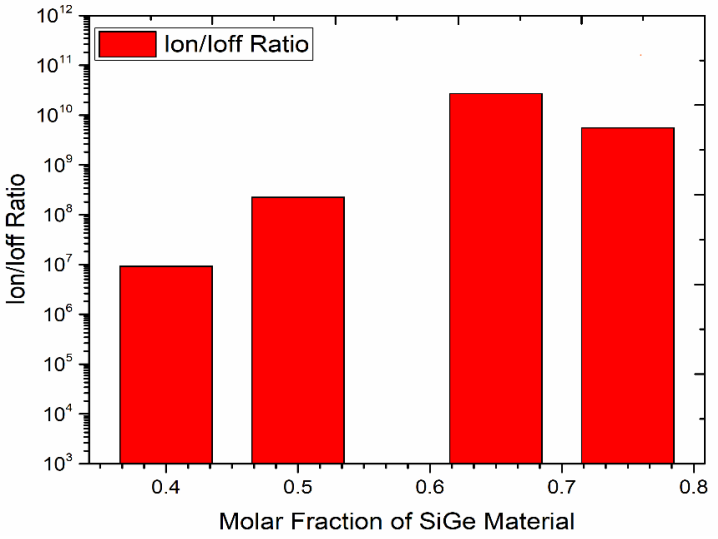


Figure 6.5 I_{ON}/I_{OFF} ratio changes with molar fraction variation

6.4 Spacer Length Variation at the source and the drain regions

The use of spacers enhance the ON state current due to the fringing fields. We have studied the impact of the length of spacers on the device structure. On a traditional MOSFET and a TFET, the effect of using a gate insulator made of high dielectric is different. The fringing field generated by the materials with high-gate dielectric constants results in fringing induced barrier lowering [64], which has been shown to degrade the performance of semiconductors. Because of the different current transport mechanisms, it's possible to increase the I_{ON} of a TFET. In a TFET, electrons from the source's valence band tunnel into the conduction band of adjacent region. The more the value of κ in the spacer, the more would be the band lowering at the source-tunnel region. At any set value of κ, there is more prominence in lowering the band nearer to the tunneling junction. When one gets closer to the source, the same decreases. Due to the band lowering, depletion regions are formed near the edge of the gate in the source. The paper mentions, because of the development of depletion regions near the surface, the holes are pulled toward the body and away from the surface. When a high-spacer is used, carrier tunneling occurs inside the body rather than near the surface, resulting in I_{ON} degradation [68]. Tunnel width and the electrical field around the tunneling junction, once again, decide the device current. The fringing field that

occurs as a result of the spacer dielectric lowering the band causes a variation both in terms of the maximum electrical field at the tunneling junction and the width of the tunnel. Due to the addition of the spacers, the ON current increases to the proposed structure as evident from figure 6.6. The drain current has been plotted on the log scale for the different spacer lengths. Increasing spacer length beyond 30 nm degrades I_{ON}/I_{OFF} ratio as has been illustrated in figure 6.7. A maximum I_{ON}/I_{OFF} ratio of 3.72×10^{10} is obtained at the spacer length of 30 nm and can be observed in figure 6.8. It is because of the larger bending of the bands due to the fringing fields through the spacer. The outcome is an increased electrical field which therefore leads to more tunneling as per equation (2.8).

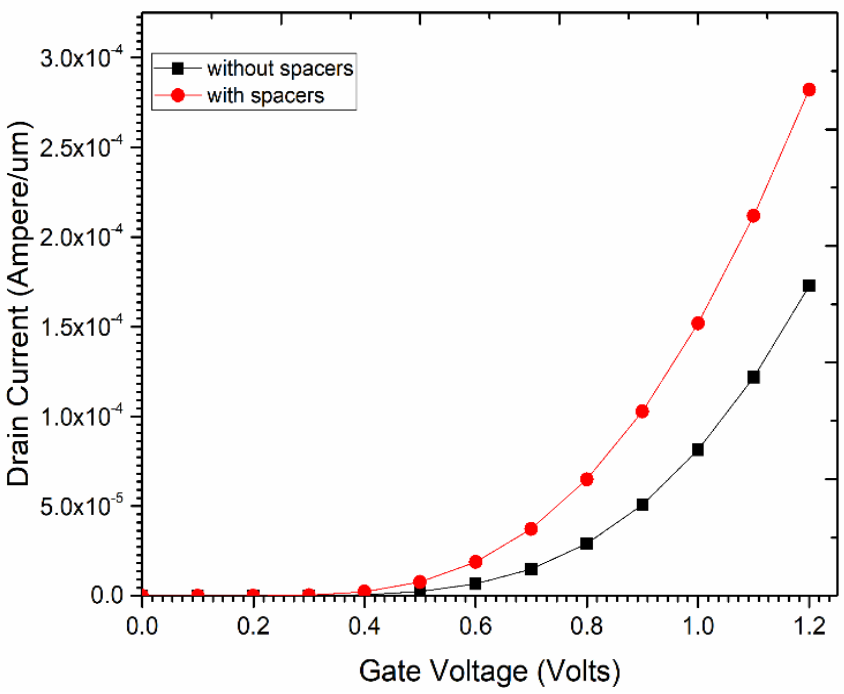


Figure 6.6 Comparison of Drain current with and without spacers

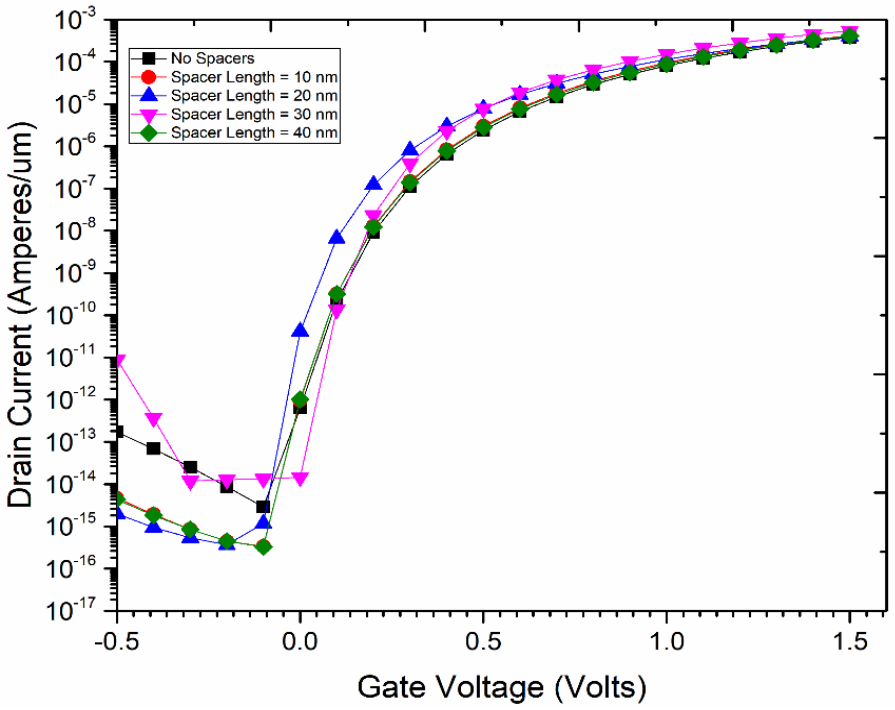


Figure 6.7 Spacer length variation effect on drain current

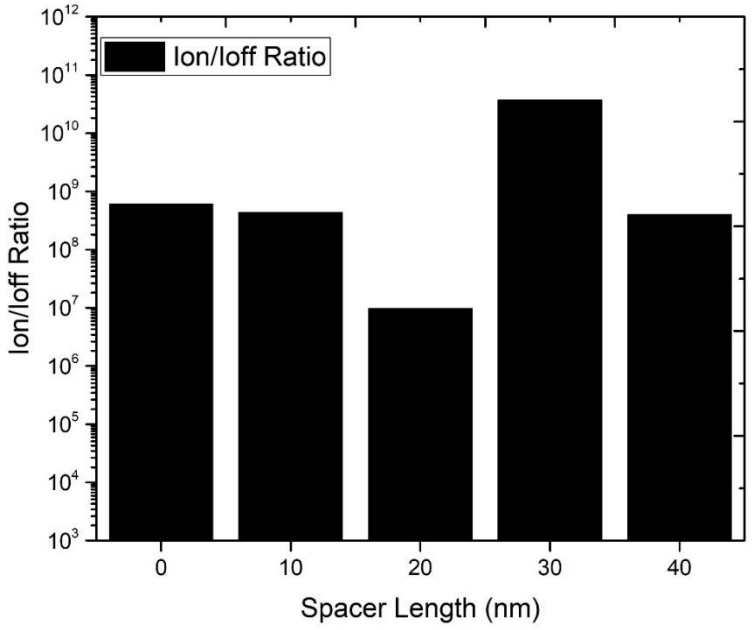


Figure 6.8 I_{ON}/I_{OFF} ratio changes with spacer length variation

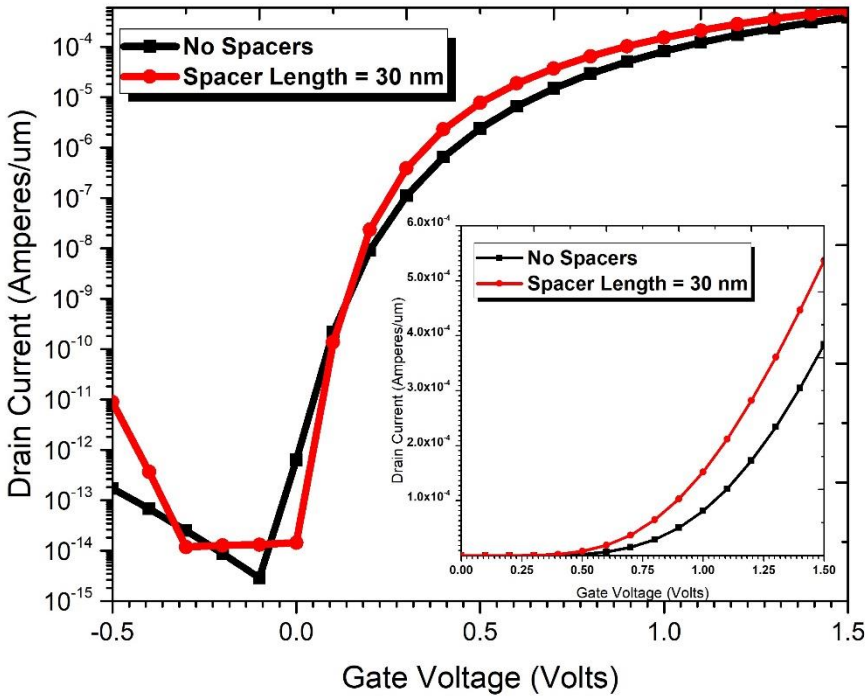


Figure 6.9 I_{ON}/I_{OFF} ratio changes with spacer length

6.5 Gate Dielectric layer Material Variations

We have also investigated about the type of the material to be used as a gate dielectric so as to optimize our results. The simulations have been carried by considering, a gate dielectric made of silicon dioxide (SiO_2) only (low-k material,$k = 3.9$), hafnium oxide (HfO_2) only (high-k material, $k = 22$) and a partially filled SiO_2+HfO_2 hetero dielectric gate material. Figure 6.10 compares the drain characteristics for such variations in the proposed structure. It is evident that, better ON current is obtained when a hetero dielectric gate material is used. It is because I_{ON} is determined by the overlapping of the gate-source region with the high-k material. While as, I_{OFF} is determined by the overlapping of the gate-drain region with the low-k material making tunneling phenomenon difficult to occur. Thus, a better I_{ON}/I_{OFF} ratio of 3.32×10^{10} is obtained when a hetero dielectric gate material is used, as represented in figure 6.11.

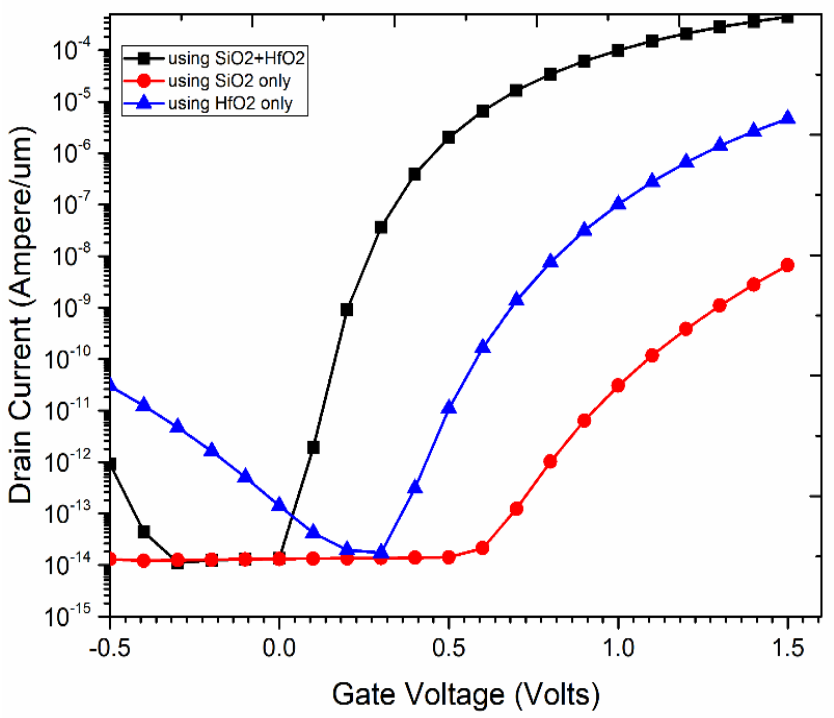


Figure 6.10 Drain current characteristics with variations in gate dielectric material

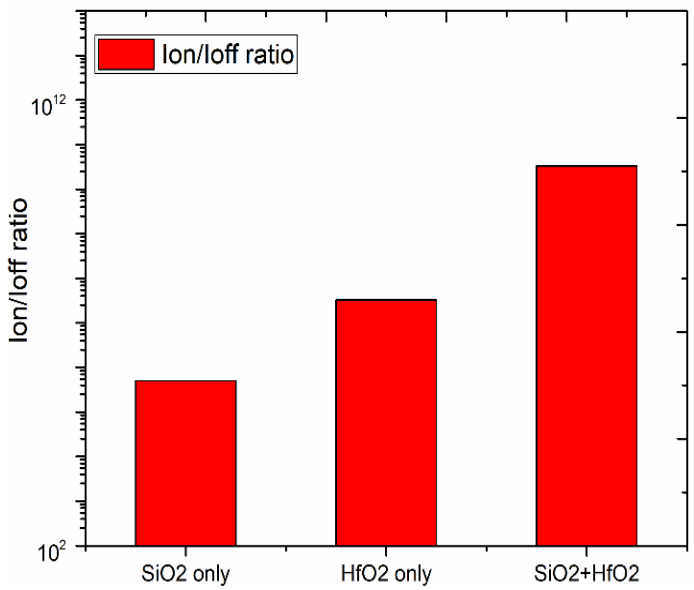


Figure 6.11 Variations in I_{ON}/I_{OFF} ratio

6.6 Buried Oxide Layer Material Variations

The other serious limitation in a conventional TFET is that of ambipolar conduction. If the gate is supplied with negative voltage in the TFET structure, again the drain current starts to flow due to the BTBT at the drain-channel interface. This phenomenon is called as ambipolar transport. In order to minimize the effect of ambipolar transport in a TFET, a hetero-dielectric BOX layer has been utilized. A high-k material at the drain region inhibits band to band tunneling when a negative gate-source (V_{GS}) voltage is applied. The increase in the ON current can be seen from the inset curve of figure 6.12. Moreover, it is observed from figure 6.12 that up to gate-source voltage $V_{GS} = -0.3\,V$ the ambipolar current is suppressed. The hetero dielectric BOX being used aids the depletion of the channel-drain interface region thus increasing the tunneling barrier width. This decreases ambipolar current at the drain region. THE highest I_{ON}/I_{OFF} ratio of 3.72×10^{10} is obtained when a BOX made of SiO_2+HfO_2 material is used.

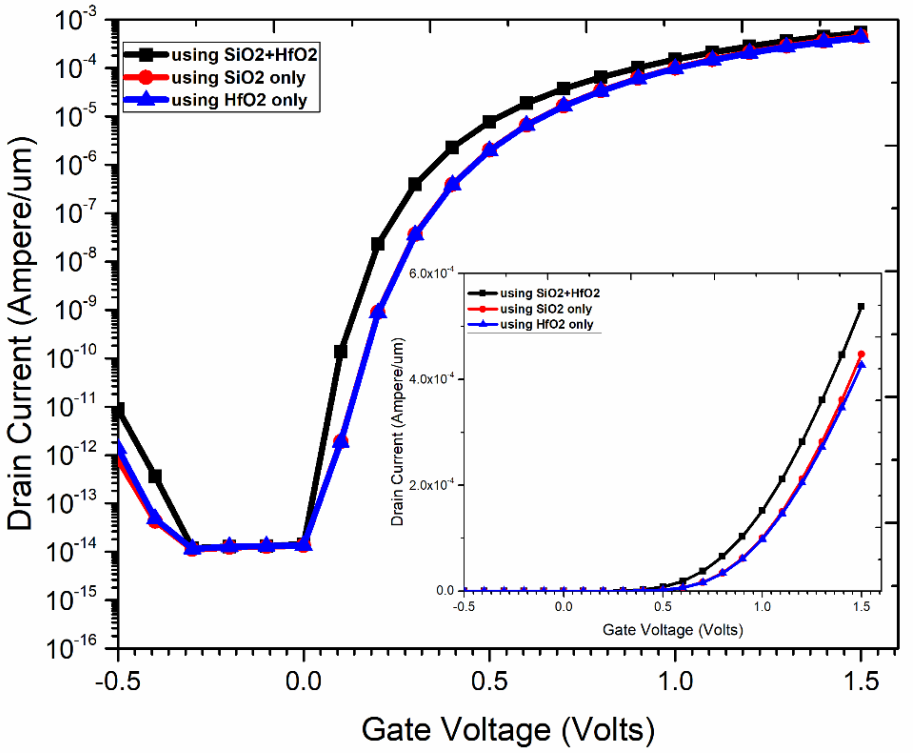


Figure 6.12 Drain current characteristics with variations in BOX layer

CHAPTER 7: STUDY OF ANALOG PERFORMANCE AND TEMPERATURE VARIATIONS IN SiGe SOURCE BASED TFET STRUCTURE

7.1 Introduction

In this chapter, we have discussed the analog/RF analysis of SiGe source based heterojunction Tunnel FET. The parameters being studied: transconductance (gm), device efficiency (g_m/I_D), gate source capacitance (C_{GS}), gate drain capacitance (C_{GD}), cut-off frequency (f_T), and gain-bandwidth product (GBP). DC, as well as AC simulations, have been performed on the proposed device. We have achieved an ON current of 0.537 µA/µm and OFF current of 13 fA/µm, thus achieving I_{ON}/I_{OFF} ratio of 3.72×10^{10}. We have also performed temperature analysis of the analog/RF parameters. We have also investigated the device for the temperature analysis in terms of drain current and capacitance calculations. We have observed that the OFF currents are strongly dependent on the temperature. All the simulations have been performed on Visual TCAD (licensed version 1.9.2-3).

7.2 RF/Analog Parameter Analysis of SiGe source based Heterojunction TFET structure:

7.2.1. Transconductance and Device Efficiency of the device:

Transconductance is a critical parameter in terms of analog performance. It represents the change in the output drain current to the variations in a gate voltage. It is clear from figure 7.1 that at the lower voltages, the transconductance increases with the increase of a gate voltage. However, at the higher voltages, it is observed that g_m decreases due to mobility degradation. Mathematically, we define transconductance as:

$$g_m = \frac{dI_D}{dV_{GS}}(at\ Constant\ V_{DS}) \tag{7.1}$$

Transconductance to output drain current (g_m/I_{DS}) or device efficiency is another useful parameter for analog/RF applications. Figure 7.2 plots device efficiency of the device against the drain current for the device. The improvements in the device efficiency is attributed to the increase in the transconductance of the device. g_m/I_{DS} ratio obtained

shows that the device is capable of providing high energy efficiency at lower gate voltages, that is a significant parameter for low power analog/RF applications [12, 111, 114, 139]. From equation, g_m/I_{DS} can be expressed as:

$$\frac{\mathrm{g_m}}{\mathrm{I_{DS}}} = \frac{1}{\mathrm{I_{DS}}}\frac{\partial \mathrm{I_{DS}}}{\partial \mathrm{V_{GS}}}$$

and subthreshold swing (SS) is given by:

$$\frac{1}{SS} = \frac{\partial \ln(I_{DS})}{\partial V_{GS}} = \frac{1}{\ln 10}\frac{\partial \ln(I_{DS})}{\partial V_{GS}} = \frac{1}{\ln 10}\frac{1}{I_{DS}}\frac{\partial I_{DS}}{\partial V_{GS}} = \frac{1}{\ln 10}\frac{1}{I_{DS}}g_m$$

$$\text{or,} \qquad \frac{1}{\mathrm{SS}} = \frac{1}{\ln 10}\frac{\mathrm{g_m}}{\mathrm{I_{DS}}}$$

$$\text{Therefore,} \qquad \frac{\mathrm{g_m}}{\mathrm{I_{DS}}} = \frac{\ln 10}{\mathrm{SS}} \tag{7.2}$$

Hence, from Eq. (7.2), the theoretical limit of g_m/I_{DS} is about 38.3 V^{-1}. However, since TFET based structure has been employed in this paper with an excellent subthreshold swing of 28.57 mV/decade, thus increasing the device efficiency tremendously. From equation (7.2), by substituting the value of the average subthreshold swing, the value of device efficiency g_m/I_{DS} comes out to be 80.59 V^{-1}, which is more than twice the value achievable with the MOSFET structure. Thus, larger values of g_m/I_{DS} than that of a MOSFET is achievable with TFET structure Also, there is no noted difference with the variations in the drain voltage.

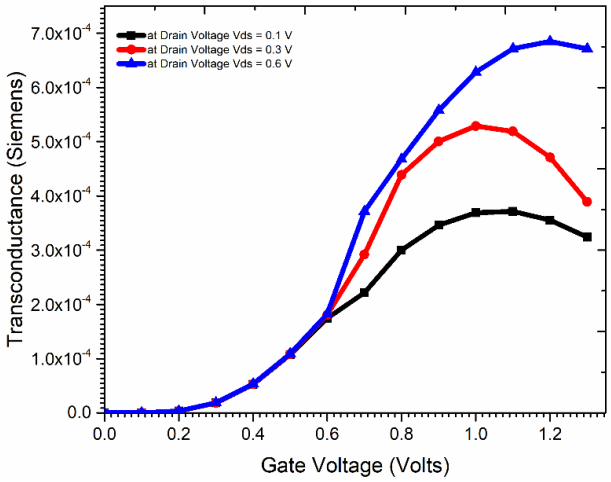


Figure 7.1 Transconductance vs Gate voltage curve

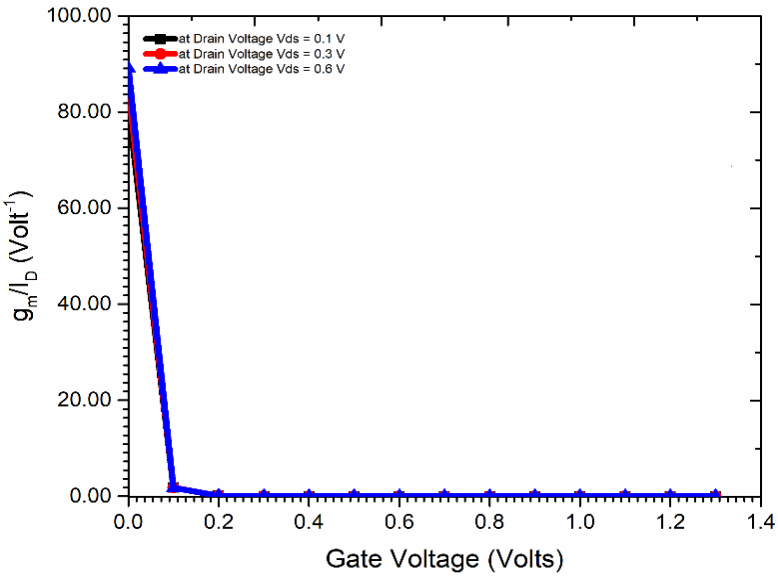


Figure 7.2 Device Efficiency g_m/I_D vs Gate Voltage curve

7.2.2. Gate-Source Capacitance and Gate-Drain Capacitance of the device:

Parasitic capacitances play a critical role in the determination of the propagation delay and the high frequency response of the device. For complete insights, both gate-source capacitance (C_{GS}) and gate-drain capacitance (C_{GD}) are taken into a consideration. For a heterojunction TFET, C_{GD} dominates overall capacitance. The parasitic capacitances can be reduced under following circumstances [140, 141]: (1) materials with lower density of states (2) materials with low band gap (3) device engineering in gate insulator or drain-underlap. In the proposed design, low-κ and high-κ dielectrics have been used at the drain and the source side respectively, for decreasing the contribution of C_{GD}. The variance of the gate-drain capacitance as a function of gate voltage is shown in figure 7.3. It is clear from the figure that C_{GD} increases with the increase of V_{GS} due to the development of the inversion layer from the drain towards the source region.

Figure 7.4 shows gate-source capacitance variations with gate voltage. The electron concentration on the source side determines C_{GS}. It can be observed that C_{GS} decreases with an increase in gate voltage V_{GS}. It is because the coupling between the gate and the source decreases because of the increased inversion layer. C_{GS} values obtained are lesser than that of C_{GD}. The calculation of total gate capacitance can be determined by summing up gate-

source (C_{GS}) and gate-drain capacitances (C_{GD}). The values of the capacitance obtained lie in the range of 0.1 to 1 femtoFarads.

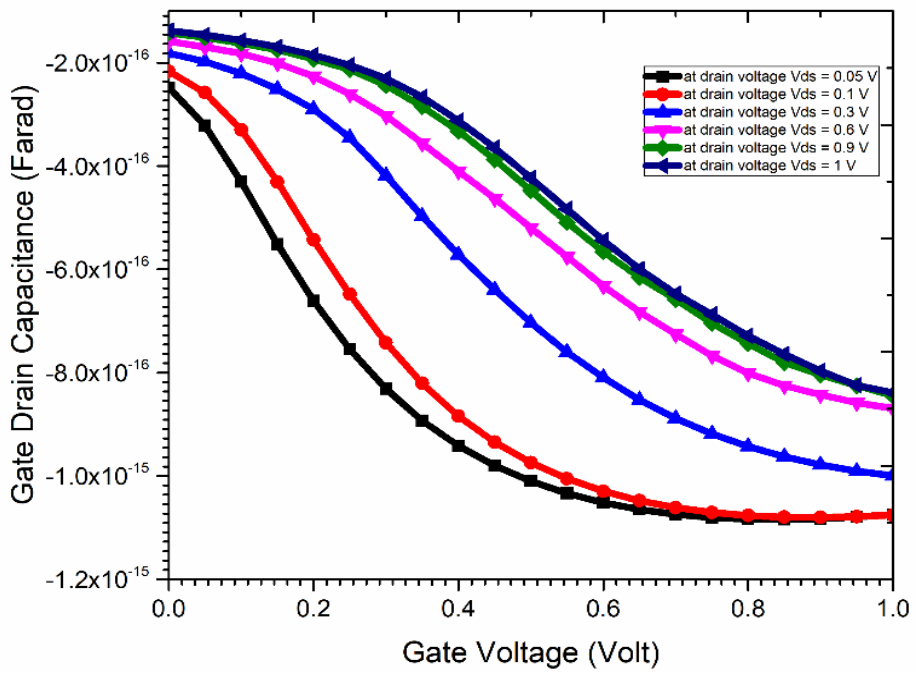


Figure 7.3 Gate-Drain capacitance curve

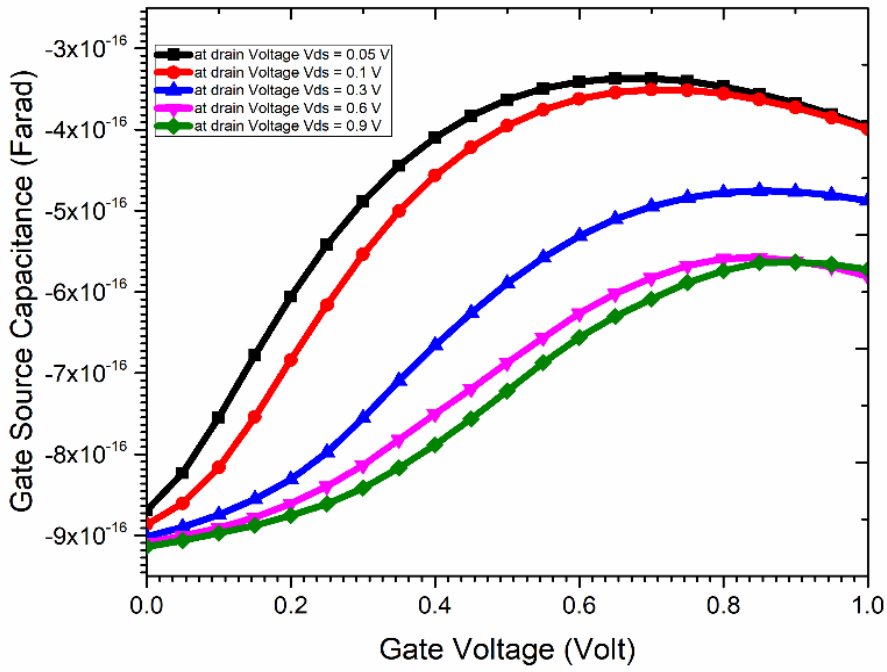


Figure 7.4 Gate-Source capacitance curve

7.2.3. Cut-off Frequency and gain-bandwidth product calculation of the device

The cut off frequency (f_T) is another vital parameter of interest that represents the frequency range up to which a device can be amplified. It is defined as the frequency at which gain becomes unity. For better RF applications, f_T must be as high as possible. The value of cut off frequency is given by:

$$f_T = \frac{g_m}{2\pi C_{GD}\sqrt{1 + 2C_{GD}/C_{GS}}} \cong \frac{g_m}{2\pi(C_{GS} + C_{GD})}$$

$$\cong \frac{g_m}{2\pi C_{GG}} \tag{7.3}$$

Thus, any increase in a parasitic capacitances would decrease the cut-off frequency. It can also be deduced from the given equation that with an increase in g_m, the cut-off frequency increases as well. This is mainly attributed to injection of charges from the source and the increase in band to band tunneling. The higher mobility for a device can be achieved if a drain voltage is increased. This in turn improves the transconductance of the device. Similarly, the gate capacitance C_{GG} also reduces with an increase in drain source voltage. Thus, the increase of g_m and the decrease of C_{GG} leads to the higher cut-off frequency for the device. Figure 7.5 indicates that the cut off frequency of the device lies in the Gigahertz (GHz) range. Figure 7.6 demonstrates the gain-bandwidth product of the device. This parameter represents the trade-off between the bandwidth and the gain, and is calculated as follows:

$$GBP = \frac{g_m}{2\pi C_{GD} \times 10} = \frac{g_m}{20\pi C_{GD}} \tag{7.4}$$

The values obtained can be compared with the work of others in Table 7-1.

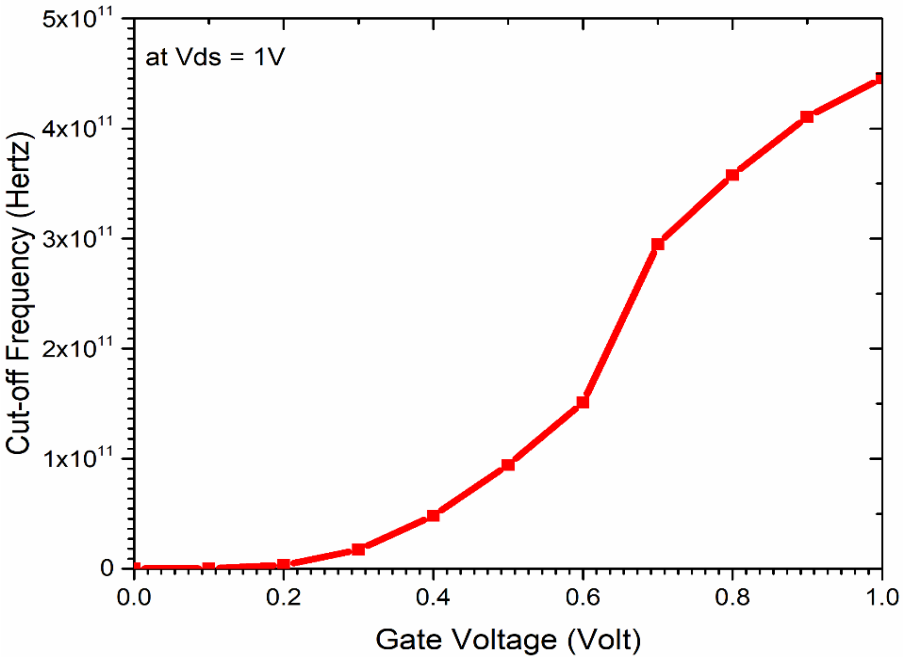


Figure 7.5 Cut-off frequency curve

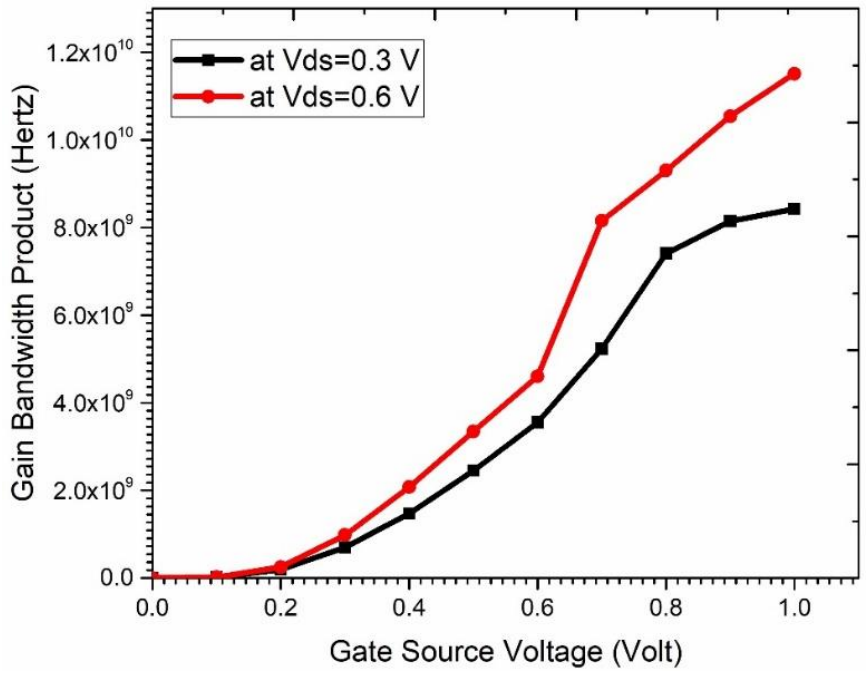


Figure 7.6 Gain Bandwidth Product Plot

Table 7-1 Comparison of the analog parameters of the proposed device with other existing TFET structures

Reference	**Year**	**Device**	**DIBL**	**Transconductance (milli-Siemens)**	**Cut-off frequency (GHz)**	**Gate source capacitance (femto-Farad)**	**Gate source capacitance (femto-Farad)**	**Gain Bandwidth product (GHz)**
Anand [114]	2016	DGTEFT	98.22 mV	0.4	≅ 500	Not reported	Not reported	15
Chander [142]	2017	Heterojunction SOI TFET	11 mV	0.11	7.6	0.3	2	0.87
Chen et al [111]	2018	TGTFET	Not reported	0.232	11.9	0.7	3.7	2.3
This work	2020	HDB TFET	3.636 mV	0.68	446	0.387	0.964	126
%ge change	[114] [140] [111]	-	-96.29 -66.94 NA	70 518.18 193.1	-10.8 5768.4 3467.9	NA 29 -44.71	NA -51.8 -73.95	740 1438 5378.3

7.3 Temperature Variations Analysis of the proposed Device:

The variations with temperature from a range of 200 K to 400 K are performed on the drain current. It is clear from figure 7.7 and figure 7.8 that the ON current is not affected by temperature variations. It is due to weak dependency of BTBT on the temperature. However, it can be seen that the OFF current strongly varies with temperature.

7.3.1. Effect on I_D-V_{GS} Transfer Characteristics

Since the energy bandgap depends on the temperature, it is therefore implied that the drain is also dependent on temperature because the rate at which tunneling occurs depends on the energy bandgap of the material [143].

To study the effect of temperature on the transfer characteristics, the device has been simulated for the temperature range of 200 K to 400 K. The gate voltage has been swept from 0 V to 1.2 V. The drain voltage has been kept constant for a particular simulation. Different drain voltages applied are V_{DS} = 0.2 V, V_{DS} = 0.4 V, V_{DS} = 0.6 V and V_{DS} = 0.8 V and the results obtained have been plotted in figures 7.7, 7.8, 7.9, and 7.10 respectively.

It has been discovered that OFF current of the device increases with rise in the temperature. This is attributed to the trap assisted tunneling and the recombination of charge carriers when the device is in the OFF state. The related traps are defect states located within the bandgap of the source and channel materials, as well as defects located at the interfaces between dielectrics and semiconductors. Tunneling from the source's valence band to the trap state below the channel's conduction band occurs first, followed by thermal excitation of the electron from the trap state to the conduction band. However, dependency is less in the ON current. The comparison with homojunction TFET has been performed at same device parameters in figure 7.11, but instead of conventional silicon, SiGe is being used in our device. The ON current can been seen as less dependent on temperature variations in a homojunction TFET as well, but the magnitude of the ON current is very less in them, and hence becomes a limiting factor.

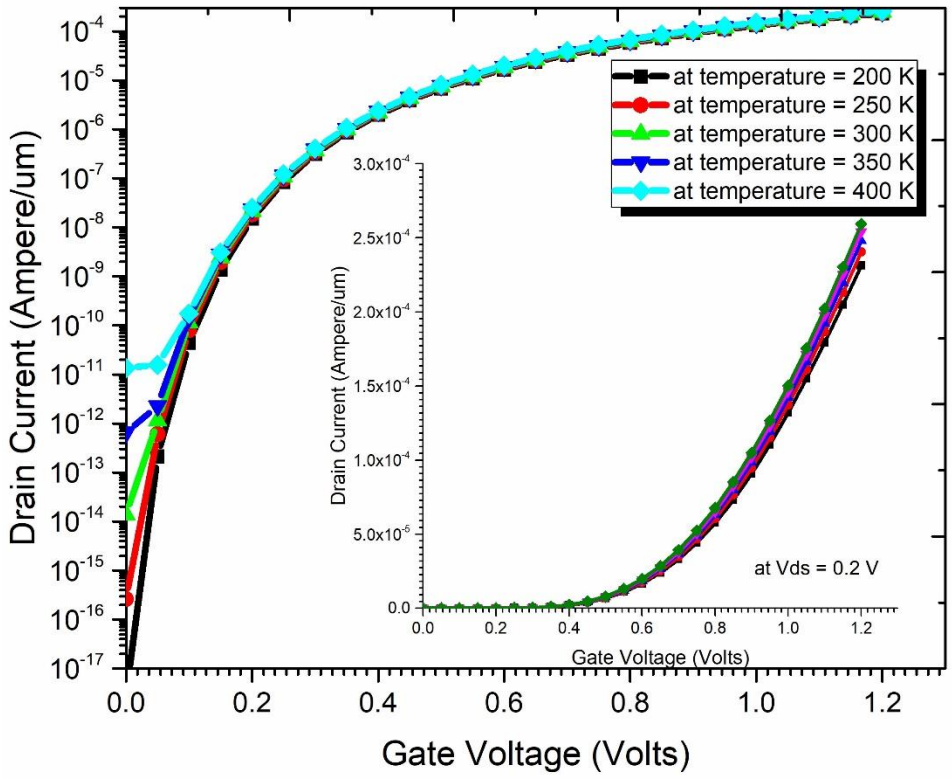


Figure 7.7 Temperature variations in I_D-V_{GS} Transfer characteristics curve at V_{DS} = 0.2 V

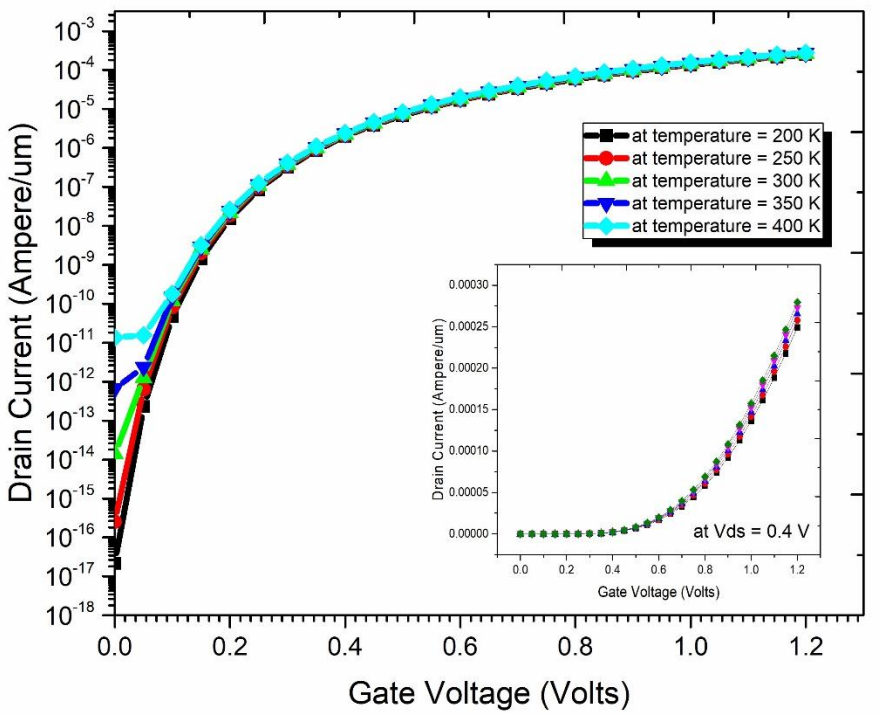


Figure 7.8 Temperature variations in log I_D-V_{GS} Transfer characteristics curve V_{DS} = 0.4 V

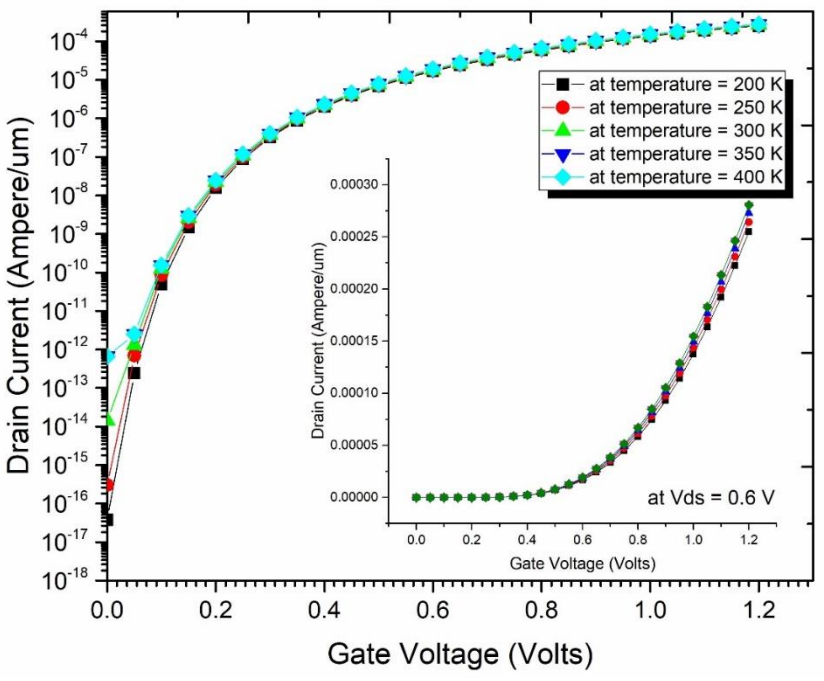


Figure 7.9 Temperature variations in I_D-V_{GS} Transfer characteristics curve V_{DS} = 0.6 V

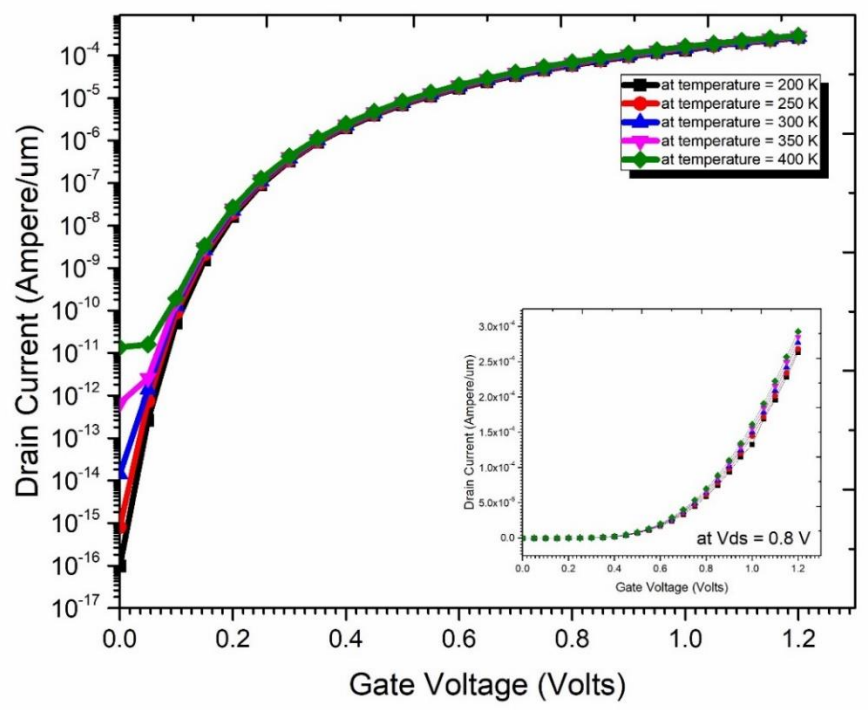


Figure 7.10 Temperature variations in log I_D-V_{GS} Transfer characteristics curve V_{DS} = 0.8 V

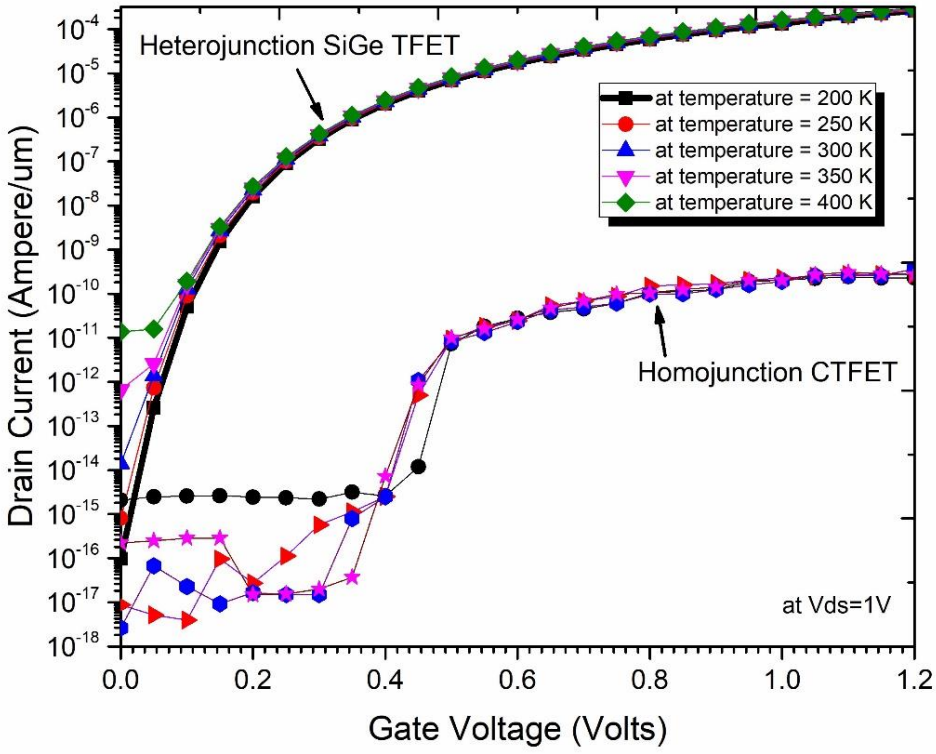


Figure 7.11 Temperature variations comparison with the homojunction TFET device

Furthermore, it has been observed that with the rise in temperature ON current slowly increases, as illustrated in figure 7.12. However, the rise in the OFF current is comparatively higher but values are still within ITRS requirements as shown in figure 7.13. The simulation has been carried for different drain-source voltages. It can be realized that ON current rises with an increase in temperature. Besides, it can be noted that the OFF current remains independent of variations in drain-source voltages (except at lower temperatures, T = 200 K). Therefore, it is clear that the I_{ON}/I_{OFF} ratio is independent of drain-source voltage. However, with temperature rise, the ratio degrades due to the variations in the OFF current.

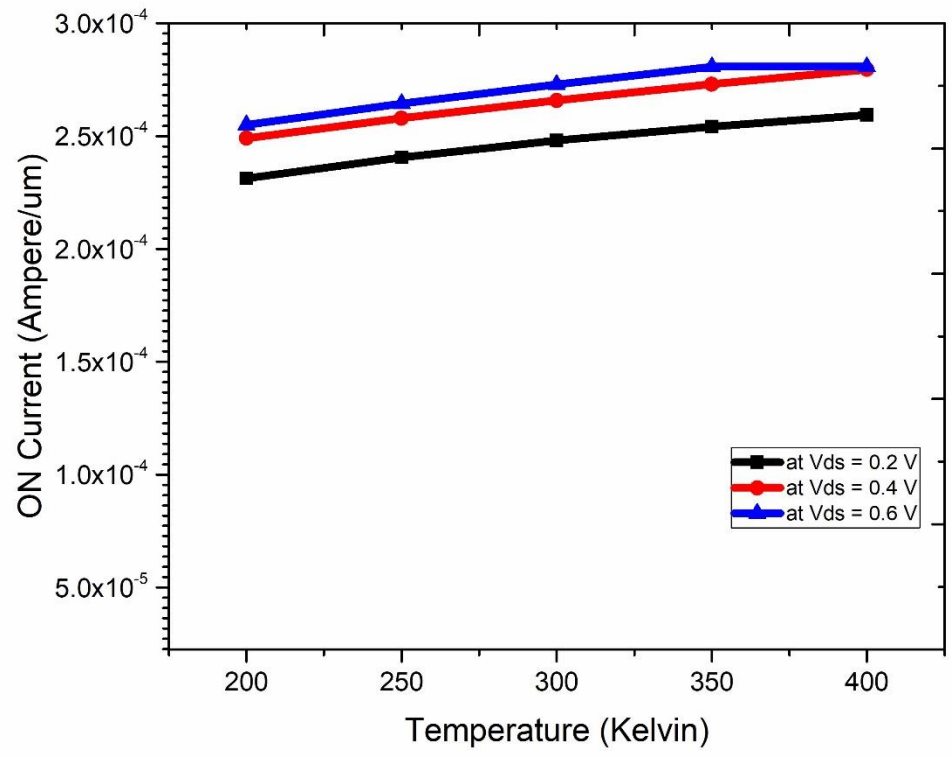


Figure 7.12 Temperature variations in ON current of the device

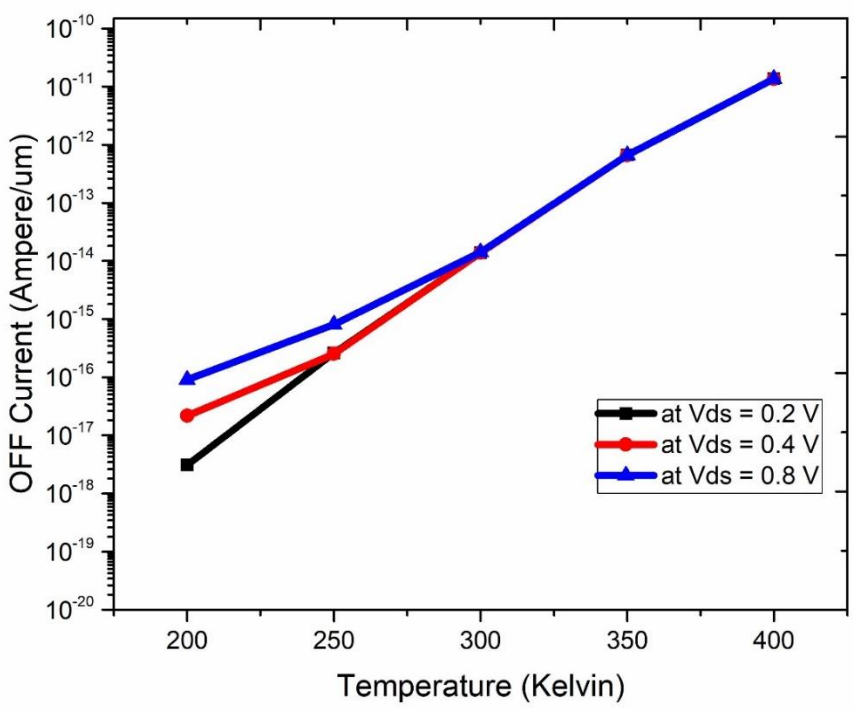


Figure 7.13 Temperature variations in OFF current of the device

7.3.2. Energy band gap variations

With the rise in temperature, energy band gap E_g decreases in the material. This has been attributed to the decrease in the potential due to the increased interatomic spacing. The temperature dependence of energy gap can be understood by the following equation:

$$E_g(T) = E_g(0) - \frac{\alpha T^2}{T + \beta} \tag{7.5}$$

where α, β and $E_g(0)$ are fitting parameters for a material. For a molar fraction of $x = 0.65$ for SiGe, the values calculated are as follows: $\alpha = 4.756\times10^{-4}$ eV/K, β = 375.35 K, and $E_g(0)$= 0.89 eV. The device has analyzed for 200 K to 400 K temperature range. The variations obtained are given in figure 7.14. The simulations have been carried out at drain-source voltages of 0.4 V and 0.8 V, respectively. It is evident from the figure that energy band gap is weakly dependent on temperature variations.

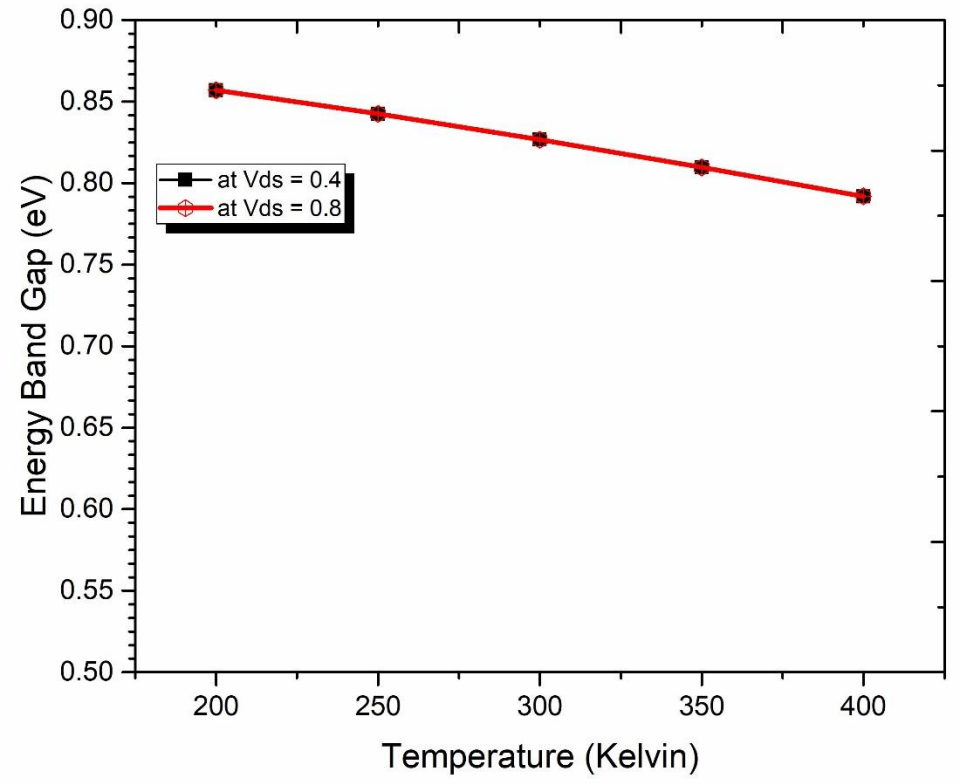


Figure 7.14 Temperature variations in the Energy band gap

7.3.3. Variations in subthreshold Swing

Subthreshold swing is the parameter that provides the idea about the amount by which the gate-source voltage should be increased so that there is one decade of rise in the output drain current. We have calculated the average threshold swing values at different temperatures for the proposed device, and the values obtained have been plotted in figure 7.15. The given figure establishes that the minimum subthreshold swing is obtained when the temperature is lowest (200 K) and the value gradually increases with an increase in the temperature. Similarly, as drain-source voltage gets increased, subthreshold swing again increases. However, the important point to note is that the average subthreshold swing remains well within the range of around 60 mV/decade (except when the temperature reaches 400 K). The lowest average subthreshold swing value is achieved at V_{DS} = 0.2 V and T = 200 Kelvin, and the value obtained is 14.41 mV/decade. At ambient room

temperature (T = 300 K), the minimum and maximum values obtained are 19.5 mV/decade and 58.3 mV/decade, respectively.

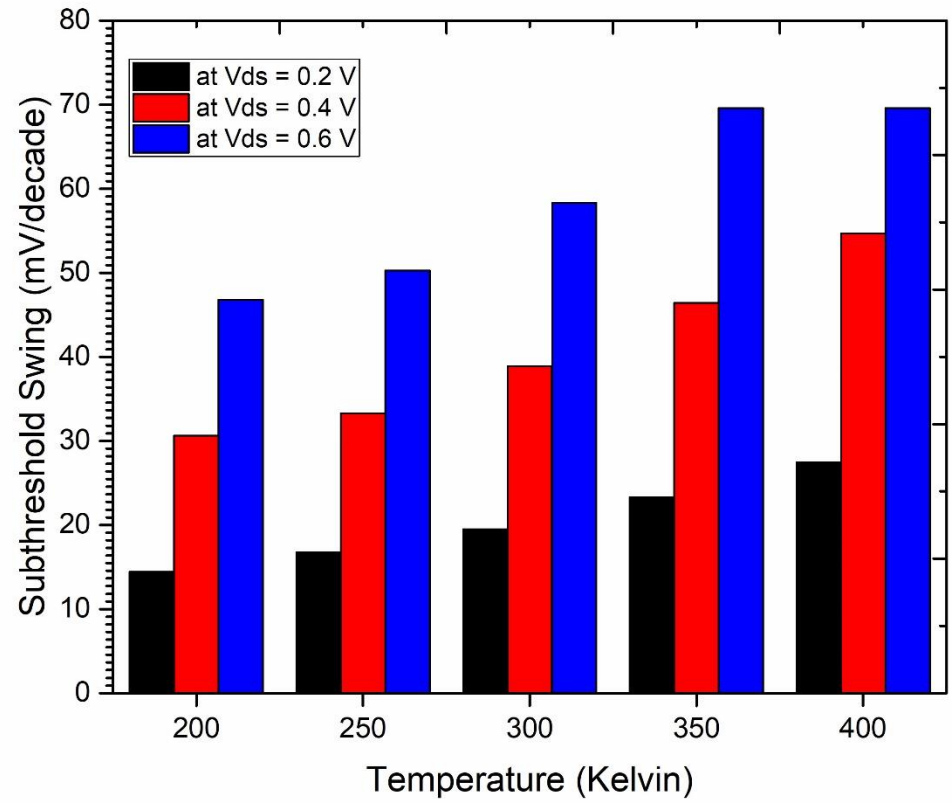


Figure 7.15 Temperature variations in the subthreshold swing

7.3.4. Variations in gate capacitance

Furthermore, we have also performed the temperature analysis of the capacitance parameters. It can be observed from the figure 7.16 and figure 7.17 that both the capacitances remain weakly dependent on the temperature at lower voltages, and shows a slight increase in the values at higher gate voltages. In TFETs, electrons enter the channel from the source through tunneling, which is temperature independent in theory, implying that the current should be significantly less temperature dependent. The changes are more visible for the ON current when compared to the OFF current. With an increase in the drain-source voltage, most of the drop occurs across the source end, leading to the reduction in the tunnel barrier height. It can be observed from the graph that there is a rapid decrease in the gate drain capacitance with an increase in V_{DS} above the saturation voltage. It happens due to the increase in the potential drop between the channel and the drain

region. Overall, it can be deduced that C_{GS} and C_{GD} have a negligible effect on temperature variations.

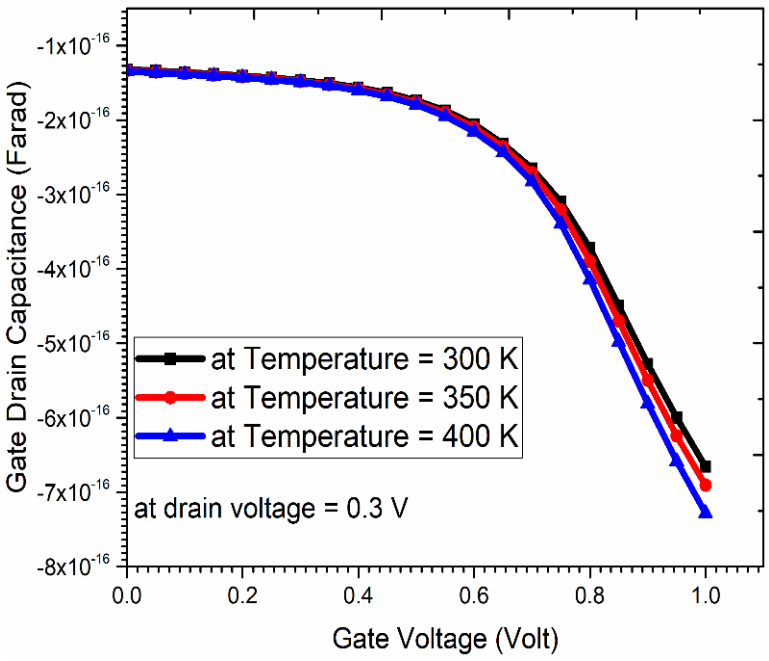


Figure 7.16 Temperature variations in Gate-Drain capacitance curve

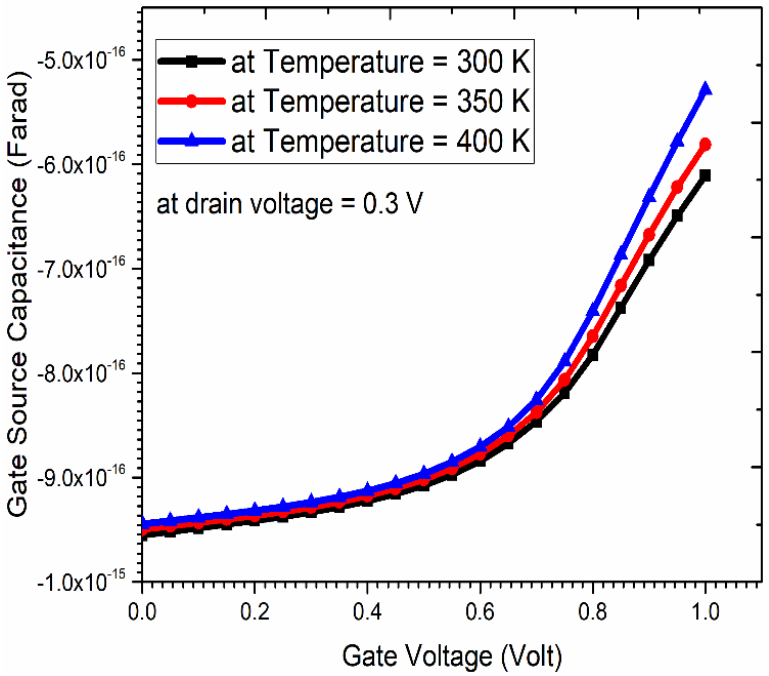


Figure 7.17 Temperature variations in Gate-Source capacitance curve

7.4 Conclusion

In this chapter, we have investigated the RF/analog performance of the SiGe source based hetero gate dielectric tunnel device. The improvements have been observed in the values of drive current, transconductance, device efficiency g_m/I_D, gate-drain capacitance (C_{GD}), gate-source capacitance (C_{GS}), cut-off frequency (f_T), and gain-bandwidth product (GBP). Besides, it has been established that the transconductance, cut-off frequency, gain-bandwidth product values obtained in this work are significantly high compared to the existing tunnel FET structures. Further, Miller capacitances (C_{GS} and C_{GD}) have been studied, and it was found that the gate-drain capacitance (C_{GD}) is the dominant factor in the Miller capacitance. The values of gate-source capacitance (0.387 fF/μm) and gate-drain capacitance (0.964 fF/μm) have also been significantly reduced. Therefore, while considering all the parameter values of the proposed structure, it can be concluded that this device can be useful for many analog and digital low-power applications.

CHAPTER 8: INCREASED SENSITIVITY OF TFET BIOSENSORS BASED ON SiGe HETEROJUNCTION SOURCE

8.1 Introduction

Analytical devices that convert biological response into an electrical signal are known as biosensors. They determine the concentration of the substance by an interaction of a biological element with the analyte. Various types of biosensors are typically based on electronic, electrochemical, optical or piezoelectric principles. For instance, piezoelectric biosensors are based on principle of change in an electrical voltage with an applied stress on the crystal. While as, in case of electrochemical biosensors, a change in an electrical quantity like voltage or current is sensed and interpreted. Semiconductor based biosensors have witnessed a substantial growth due to the development in Semiconductor Technology and its application in various fields. FET based (Field Effect Transistor) sensor was developed in 1970.

Clark and Lyon [144] introduced biosensors in 1962, and since then it has found applications in industrial, biomedical and healthcare applications. Among various biosensing devices available, FET type biosensors are found attractive because of its sensitivity, easy operation, low cost, mass production, high speed and requirement of a minute samples for testing. Bergveld [145] initially reported the principle of ion-sensitive biosensor (ISFET) based on the conventional MOSFET in 1970. This concept was used for the study of enzyme FETs. Caras et al. [146, 147] demonstrated very first time the use of a FET-biosensor for use of Penicillin in 1980. Various other papers have demonstrated the capabilities of a FET biosensor with different molecular targets [148] like amino acids [149], nucleotides and cells [150].

Biosensors with ultra-sensitivity are in demand as they can be potentially used in the area of healthcare for precision medicine, early detection, genetic diagnosis, etc., and are therefore viewed as a promising device for the next-generation point-of-care testing (POCT). It is term that defines conducting of medical tests outside the laboratory, near or

premises of a patient [151]. Glucometers are one of the examples where testing is done at patient's home rather than a laboratory. Moreover, this process is simple, as no training would be required to operate the device, and quick, as it would decrease the time taken to produce results.

FET-based sensors are derived from ISFET in which the changes in the electrical properties (voltage or current) happen due to the movement of charged molecules between the gate dielectric and the ionic solution [152]. ISFET produces good results if the biomolecule is charged. However, the limitation of FET-based sensors is that they lack the detection of biomolecules that are positively or negatively charged. With the recent advancements in the research, to address the challenges of traditional CMOS technology, new devices are being investigated [92]. In that regard, TFETs are gaining traction as a possible replacement for traditional gate engineered MOSFETs due to their exceptional performance in terms of subthreshold swing, Higher I_{ON}/I_{OFF} ratio, low power dissipation and higher sensitivity [153, 154]. This superior performance is possible in a TFET because it relies on band to band tunneling instead of a thermionic injection [155-157]. Dielectrically modulated TFET based biosensor structures have been reported by few researchers [158-162]

8.2 Principles of FET based biosensing:

8.2.1. MOSFET

MOSFET is a fundamental building block for FET-based biosensing. The MOS transistor takes up less silicon region than the bipolar junction transistor (BJT) and can be fabricated in fewer processing steps. MOSFET is a four terminal device containing the source (S), the drain (D), the gate (G) and the substrate or body (B) as shown in figures 8.1 (a) and (b). The output drain current is controlled by the input gate voltage (V_{GS}). For n-type MOSFET the current conduction is due to the electrons while as for p-type MOSFET the current conduction is due to the holes. Positive gate voltage (+ V_{GS}) is required to turn ON n-type MOSFET, while as negative gate voltage (- V_{GS}) is required to turn ON p-type MOSFET. With an application of a gate bias the electric field will be directed towards the substrate.

When the gate voltage extends up to the threshold voltage (V_{TH}), sufficient number of minority carriers are attracted towards the channel creating an inversion layer. This ultimately contributes to current across the channel.

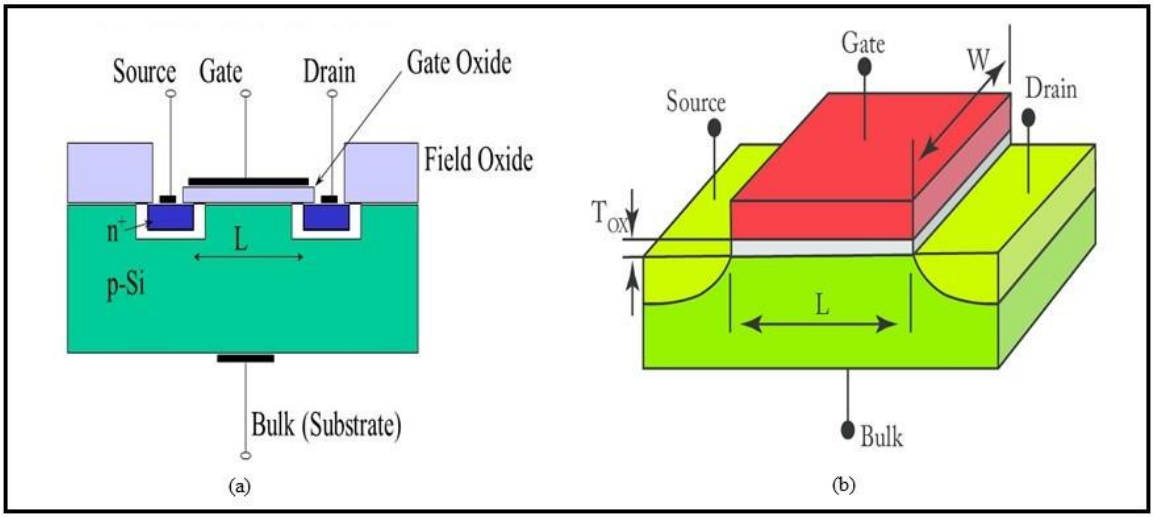


Figure 8.1 The MOSFET Structure (a) cross sectional view of n-type MOSFET (b) Physical structure of n-type MOSFET

The output drain current (I_D) for a saturation region in a MOSFET can be found by following equation:

$$I_D = \frac{1}{2}\frac{\mu_n C_{ox} W}{L}(V_{GS} - V_{TH})^2 \tag{8.1}$$

where,

μ_n is electron mobility, C_{ox} is oxide-capacitance, W is the width of the gate and L is the gate length.

The surface charge density of the conjugated biomolecule affects the applied input gate voltage. As a result, molecules to be probed must adhere or stick to the active sensing layer in order for biomolecules to be detected using FET.

An additional factor of biomolecular potential (V_{bio}) will also affect the drain current. If negatively charged biomolecules conjugate to the surface of n-type MOSFET , the drain current would decrease, while as, if positively charged biomolecules conjugate to the surface of n-type MOSFET, the drain current would increase. So, equation (1) can be modified as:

$$I_D = \frac{1}{2}\frac{\mu_n C_{ox} W}{L}(V_{GS} - V_{TH} + V_{bio})^2 \qquad (8.2)$$

8.2.2. ISFET

ISFET stands for Ion Sensitive field effect transistor. These are the novel integrated devices used for measuring the concentration of ion solutions. The ISFET and MOSFET are similar in various aspects, except that a solution acts as a gate electrode in an ISFET. The magnitude of the current carried by ISFET device depends on the density of charge for biomolecules on the gate surface. The cross sectional diagram is provided in figure 8.2.

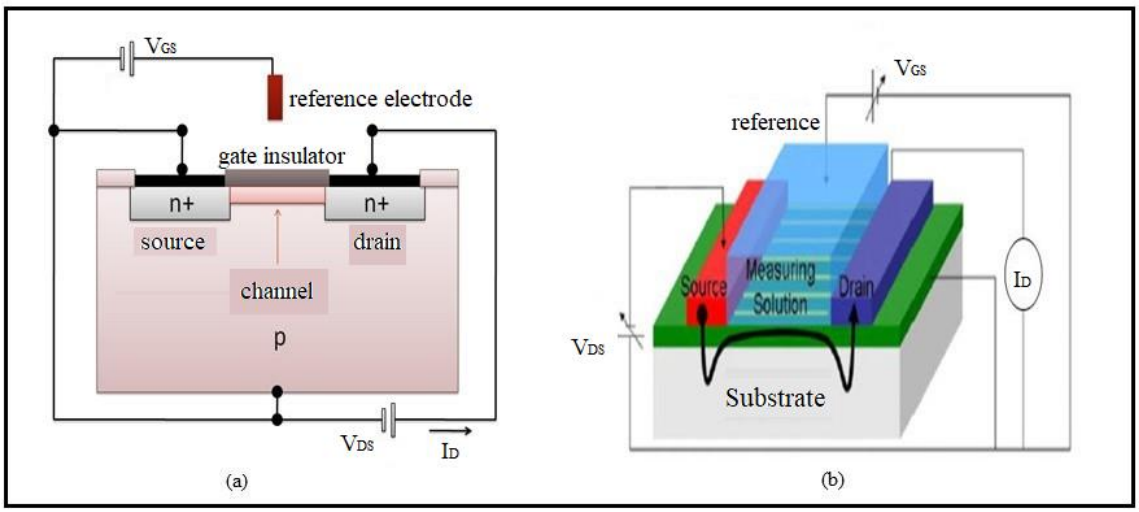


Figure 8.2 The ISFET Structure (a) n-type ISFET cross sectional view (b) Physical structure of n-type ISFET

8.2.3. Silicon Nanowire FET

Nanostructures like nanowires have also been studied for a biosensing from last decade, as their diameters are similar to the sizes of the chemical and biological organisms to be detected. Because of the larger "surface-to-volume ratio" and the smaller size of Silicon Nanowire (SiNW), Just a few biological micromolecules have the ability to monitor carrier distribution through the entire cross sectional conduction pathway. This enhances the sensitivity of a silicon nanowire than that of an ISFET. The Silicon nanowire connected between the source and the drain serves as the sensing component of the device. Figure 8.3 represents the SiNW based biosensor. A solid state biosensor based on SiNW was introduced first by Cui et al. [163]. Since then various researchers have demonstrated its ability to detect nuclei acids, proteins and viruses with increased sensitivity.

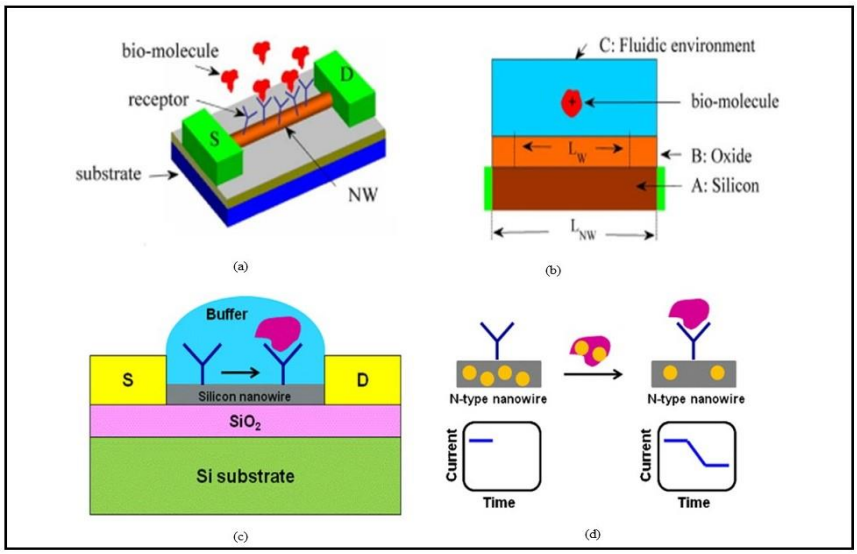


Figure 8.3 (a) Representation of nanowire biosensor (b) Demonstration of three regions (c) Immobilization of a receptor molecule on the SiNW surface (d) When a negatively charged target molecule binds to the receptor, the conductance of n-type doped SiNW decreases.

8.2.4. Carbon Nanotubes

Carbon nanotubes are cylindrical graphite sheets with nanoscale diameters and a high length-to-diameter ratio. They are made of carbon atoms linked in hexagonal shape and each carbon atom is linked to three other carbon atoms with a covalent bond. The ends can be open or closed. Single walled carbon nanotubes (with a diameter of less than 1 nm) are

composed of single-atom rolled graphite layers. While as, multi-walled carbon nanotubes (with diameters reaching more than 100 nm) consist of multiple rolled graphite sheets as shown in figure 8.4. Due to its properties like low weight material, ultra strength, highly conductive, carbon nanotubes are found highly attractive in numerous applications.

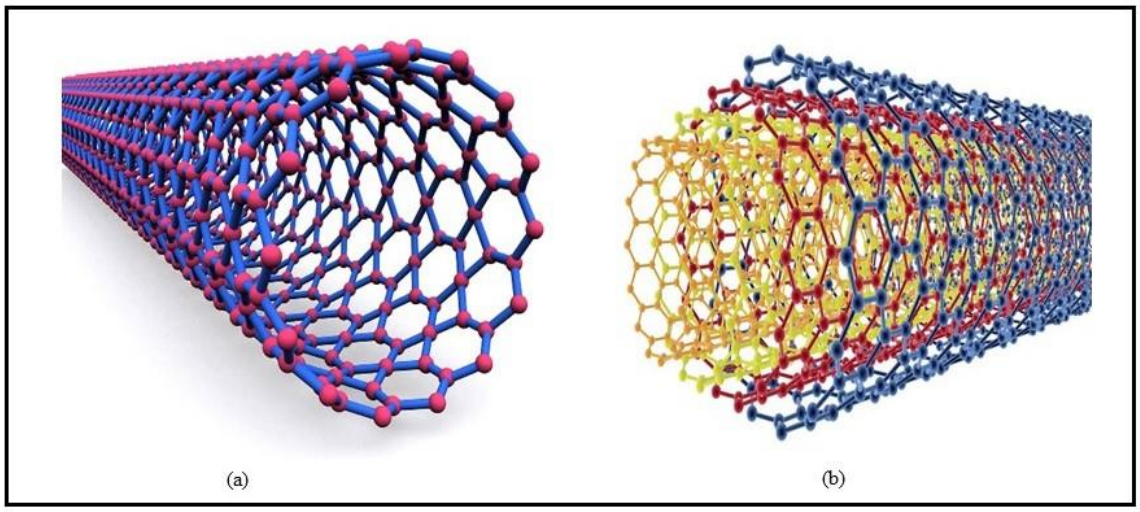


Figure 8.4 (a) Single walled CNT (SWCNT) (b) Multi walled CNT (MWCNT)

CNT based biosensors offer following advantages: (1) Owing to its wide surface to volume ratio, it has a high sensitivity. (2) faster response time due to its faster electron-transfer kinetics (3) highly stable and higher durability. These advantages have compelled researchers to investigate and explore this device further. The idea for CNT biosensor originated from the original works of Clark [144] in 1962. As illustrated in Figure, CNT-based biosensors are made up of two main components: biological sensitive element and an electrode. The CNT along with biomolecules, such as proteins, enzymes, tissues, etc. are acting as a biological sensitive element. While as, the transducer converts concentration of conjugated biomolecules into a detectable signals like current for test and the detection. CNT biosensors can be chemical, physical or FET based. At present, most of the CNT biosensor research is based on electrochemical biosensors in which chemical changes are converted into an electrical signal. The hollow structure of carbon nanotubes is used to adsorb an enzyme. Physical type CNT biosensor rely on optical and piezo resistive properties. Detecting biomolecules using near infra-red light finds application in

biomedical field. CNTs possess excellent luminescence properties. Glucose detection using sensing mechanism of CNT optical sensor is illustrated in [164].

Smaller molecules cannot be detected by the conventional FET, irrespective of the molecule being charged or uncharged. However, CNT FETs are sensitive towards the minute electrical changes in biomolecules. CNT-based FET biosensors have been widely used for the biological molecules like proteins, enzymes, hormones, etc. [165, 166]. Star et al [167] demonstrated the detection of specific protein binding using CNT-based FET. The process flow has been provided in figure 8.5.

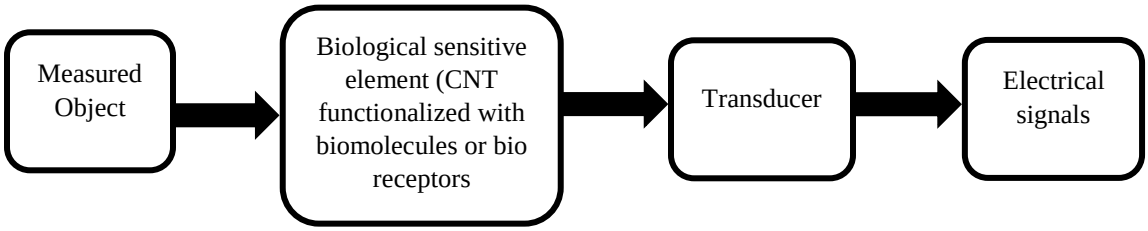


Figure 8.5 Step wise description of CNT based sensors

8.3 TFET Based Biosensor

CMOS scaling technology has been successfully used to increase power density and achieve faster integration. Dennard in 1974 [7] showed that basic operation in a MOSFET can be retained if the device's parameters are scaled in compliance with those conditions

The relation for the power dissipation in a CMOS during the transition from off to on state or vice versa is given by:

$$P = C_L {V_{DD}}^2 f \tag{8.3}$$

where C_L is the load capacitance and f is the operating frequency. This equation clearly indicates that power dissipation will reduce quadratically if the supply voltage is decreased. Gordon Moore had proposed that number of transistors on a given IC would get doubled by every 18 months. From last 50 years an exponential growth has been witnessed in the chip density on a given IC. However, as the transistor size kept on getting smaller, as small

as 10 nm, lot of heat gets generated , which tends to increase the leakage currents as well. Moreover, no exponential growth can continue incessantly and the same is true for Moore's law. The limitation in FET based biosensors was their inability to detect neutral charged particles. Thus a cavity in the modified MOSFET architecture was created in the dielectric material for biomolecule trapping was proposed [168].

Being inexpensive, quick in response, and label free, the electrical detection of biomolecules using FET based sensors has become attractive. As discussed earlier, many semiconductor based devices have been used to implement such structures (ISFET, carbon nanotubes, Silicon nanowires, etc.). The dielectric (oxide) layer of the semiconductor device is made functionalized with specific receptors, which then attract particular target molecule (referred as conjugation). It produces a gating effect and results in a change of electrical properties like current, etc. Sensitivity is measured by the degree of response of FET to the gating effect. Higher the response, higher the sensitivity of the FET. In terms of current, sensitivity is a measure of ratio change in the drain current due to change of concentration due to biomolecule conjugation to the drain current before conjugation. This effect is more prominent in the subthreshold region, which remains a limiting factor of conventional FET based sensors due to the Boltzmann tyranny.

However, with the aggressive scaling, FET has some limitations like short channel effect (SCE), subthreshold current, etc. [169, 170]. Due to the physical limits in a MOSFET, subthreshold swing cannot be reduced beyond 60 mV/decade and leakage current is also found to be high due to subthreshold conduction.

The expression for the subthreshold swing is given by:

$$S = \frac{dV_G}{d\varphi_s}\,\frac{d\varphi_s}{d(\log_{10} I_D)} \cong \left(1 + \frac{C_d}{C_{ox}}\right) \ln 10\ \frac{kT}{q} \tag{8.4}$$

.

The sensitivity and response time of traditional FET (CFET) based biosensors are severely limited as a result of this drawback. With the current research being focused on exploring

novel devices to overcome the limitations of current CMOS technology, TFETs (Tunnel Field Effect Transistors) are seen as one of the solutions to this problem. The reason for improved performance in a TFET is that it is based on BTBT [28, 92]. Superior thresholds can be achieved by employing TFETs for highly efficient biosensors [157]. In this regard, a dielectric-modulated TFET (DM-TFET) has been reported [159]. The sensitivity of DM-TFET is higher in comparison to DM-FET. The response time is another significant parameter to consider when assessing the efficiency of a biosensor. It's the amount of time taken to reach the optimal degree of sensitivity. Achieving low subthreshold means the response time of the device is quicker, which in turn means higher sensitivity. Since, TFET biosensors are having a capability to reduce subthreshold swings well below 60 mV/decade as illustrated in figure 8.6 because of its quantum tunneling effect phenomenon, as a result, they will significantly reduce response time.

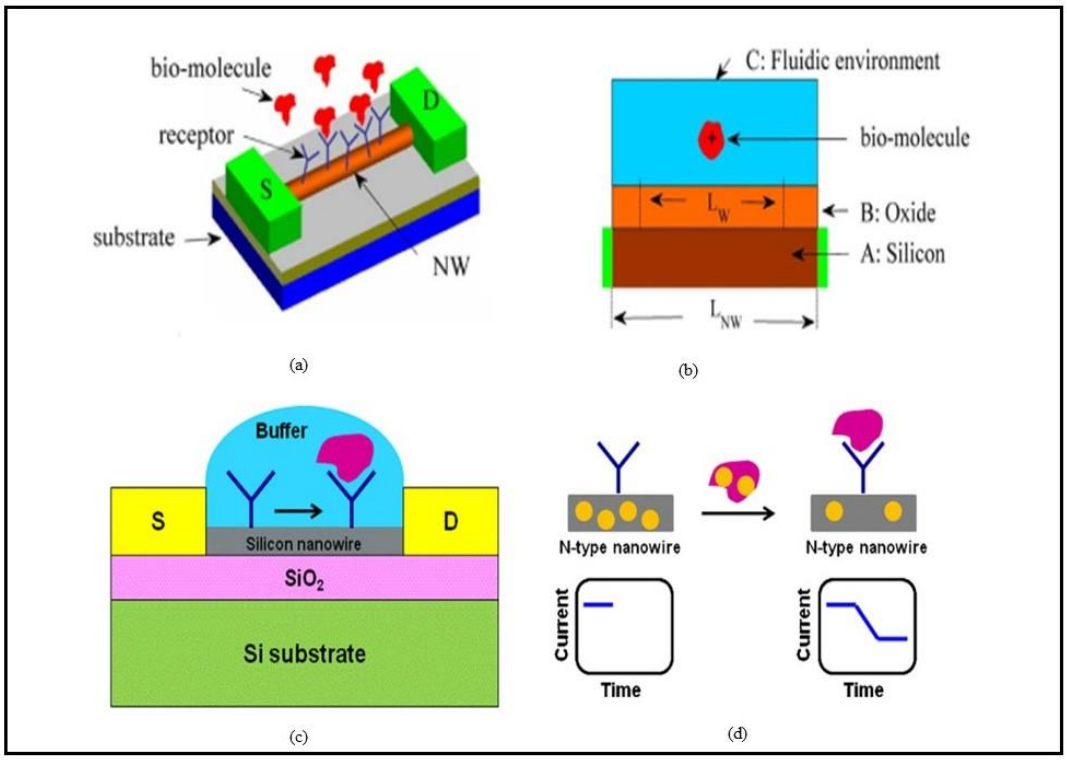


Figure 8.6 (a) Transfer characteristics of MOSFET representing increase in an OFF current exponentially (10 folds increase for every 60mV at T=300K). (b) Comparison of MOSFET, Silicon Bulk TFET, multi-gate devices (MuG) and SiGe TFET. (c) For a sub-thermal swing, the minimum switching energy and the

corresponding voltage supply are needed at the same I_{ON}/I_{OFF} (d) Steep swing in TFET offering better energy efficiency for low voltage operations [3]

8.3.1. TFET device architecture and simulation setup

Here we would discuss two device architectures, the dielectrically modulated TFET biosensor with SiGe as the source material and the proposed heterodielectric BOX TFET structure with a nanogap cavity. The inspiration for the work on biosensors has been taken from [158-160, 171]. The benefits of dielectric modulation are combined with the intrinsic superior characteristics of a TFET in this transistor. The schematic details of the DM-TEFT structure are provided in figure 8.7. Here we will discuss the performance and develop a comprehensive understanding of this device.

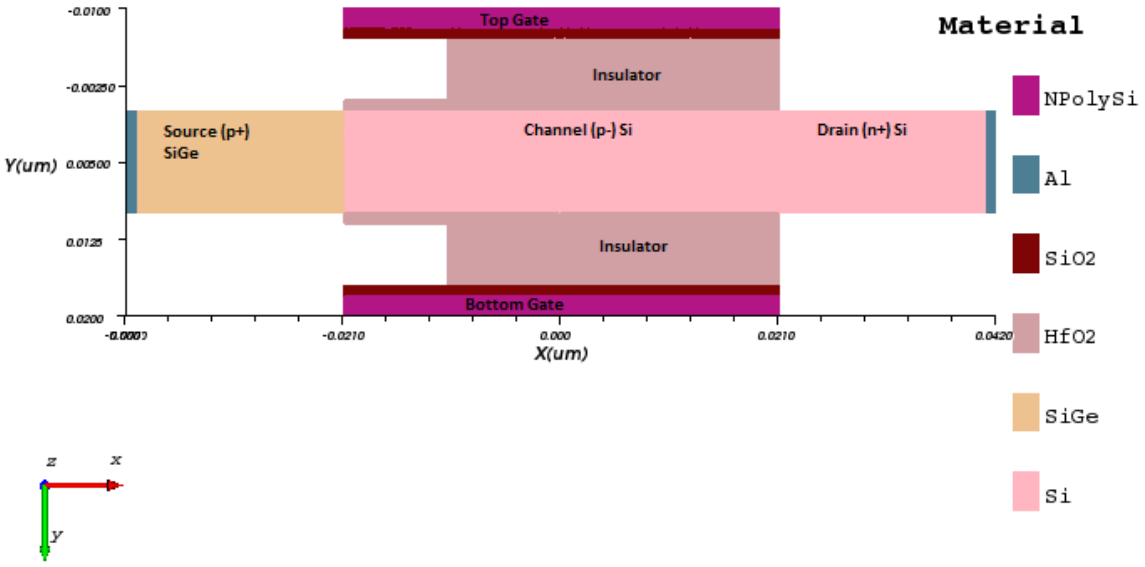


Figure 8.7 Schematic of Dielectrically modulated TFET

The length of source and drain region is kept at 20 nm. The gate length considered is 42 nm. Doping for the source region is 5×10^{19} cm^{-3} (p+ type), the channel region as 1×10^{15} cm^{-3} (p type) and drain region as 5×10^{19} cm^{-3} (p+). A 1 nm gap of insulator is available within the cavity so as to prevent leakage currents. Gate to source voltage (V_{GS}) has been swept from 0 V to 1.2 V in the steps of 0.05, while as the work function for a gate electrode has been fixed at 4.17 Volts. To enhance the tunneling phenomenon, Silicon-

Germanium (SiGe) heterojunction source has been used with a Ge composition as x = 0.5 for optimal values.

The double gated TFET structure has been considered during device simulation. It leads to a better control of the gate over the channel [28] and achieve high ON current. Silicon-Germanium has been used as source material. With an increase in the Ge composition, there would be a rise in ON as well as OFF current. Figure 8.8 illustrates the comparison of the energy diagrams for a conventional MOSFET based on thermal injection and Tunnel FET device based on tunneling phenomenon.

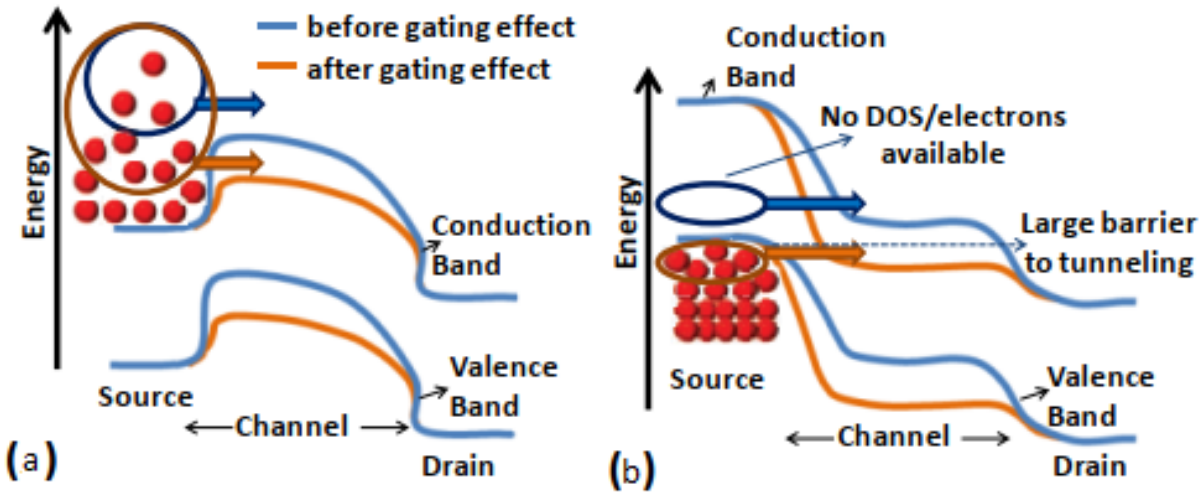


Figure 8.8 Energy band profile of (a) Conventional FET (b) Tunnel FET demonstrating band to band tunneling (BTBT) phenomenon between channel's conduction band and source's valence band. Once the bio biomolecules are trapped due to the gating effect, the bands bend down reducing the barrier the channel and the source, therefore increasing the BTBT current.

Furthermore, we have also implemented the proposed hetero gate dielectric hetero BOX based SiGe heterojunction tunnel FET as a biosensor structure. It was observed that the sensitivity of the device is improved, owing to high $\frac{I_{ON}}{I_{OFF}}$ ratio and a steeper subthreshold swing obtained for the device. The nanogap cavity of 30 nm length has been created just below the gate terminal for the conjugation of the biomolecules, as provided in figure 8.9. The biomolecules would get trapped inside the cavities, and would change the gate

electrode characteristics, thereby transforming the electrochemical reactions into an electrical signal.

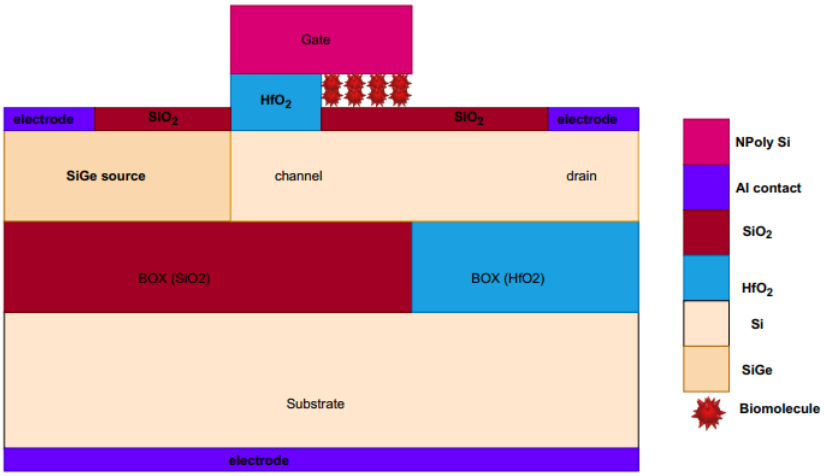


Figure 8.9 Hetero gate dielectric hetero BOX based proposed SiGe heterojunction biosensor

8.3.2. Results and Discussions

There are two types of biomolecules, neutral and charged. Different biomolecules are having different dielectric constants. Various values of the dielectric constant used in the simulation represent neutral biomolecules, while as, the dielectric constant as well as the charge density would be used for the representation of charged biomolecules. Trapping of biomolecules inside the cavity reduces the barrier between the source and the channel, therefore changes the BTBT current.

Figure 8.10 represents the drain current characteristics for the cavity length of 30 nm. The value of the dielectric constant κ has been varied from 1 to 25, so that a diverse range of neutral biological molecules could bound into the cavity. For example, deoxyribonucleic acid has a range of κ as 1-64, biotin streptavidin has a κ of 2.1, charged amino acids such as Lys, Arg, Glu and Asp have κ ranging from 11 to 25.6, gluten, keratin and zein have κ ranging from 5 to 10. While performing the simulations, the values of κ have been selected

while taking all these numbers into the consideration. Various materials selected for neutral biomolecule conjugation are air (κ = 1.00), Teflon (κ = 2.1), epoxy (κ = 2.5), SiO_2 (κ = 3.9), Nitride (κ = 7) and HfO_2 (κ = 20 to 26). When the value of κ is varied from 0 to 26, it is observed that there is a small variation in the ON current, as observed in figure 8.11.

Biosensors transform a biological or physical reaction into an electrical signal in order to detect biological molecules in the environment. This was accomplished in our design by adding cavities on the source side of the device's top and bottom regions. The source region is considered because the band to band tunneling will mainly be happening at the source junction. The cavities help in conjugating biomolecules and hence detect their dielectric constants and the currents that they carry. The presence of biomolecule would cause changes in the device's electrical parameters, which would be identified by changes in the device's characteristics. In this work, variations in the dielectric constant and/or charge density inside the cavity region reflect biomolecule conjugation. Just one of the parameters has been adjusted once to see how it affects the sensor's sensitivity.

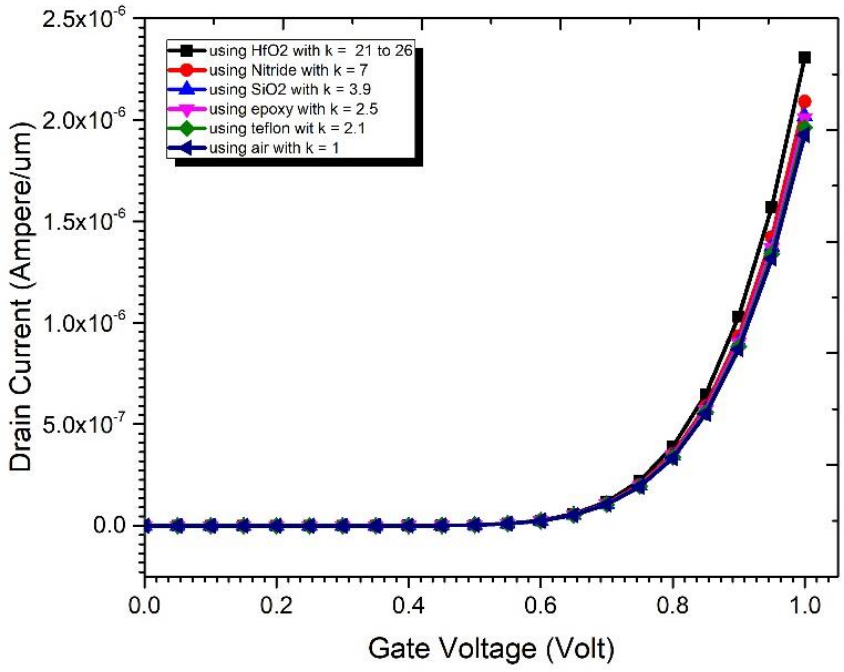


Figure 8.10 Drain Current characteristics representing the effect of neutral biomolecules at the cavity length of 30 nm

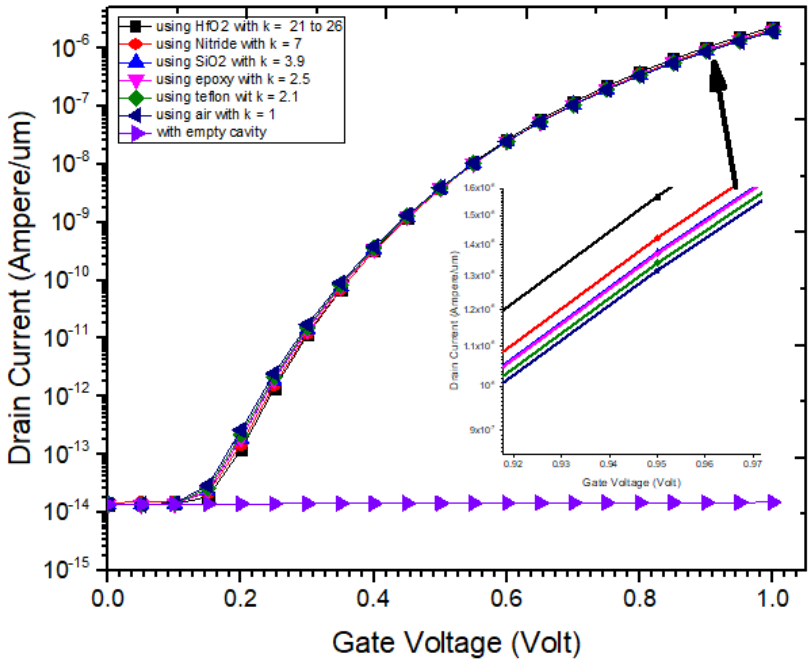


Figure 8.11 Drain Current characteristics on the log scale representing the effect of neutral biomolecules at the cavity length of 30 nm

Further it was found that when the nano gap cavity length was reduced to 20 nm, there was a rise in the ON current. This is attributed to the stronger band to band tunneling at the source channel junction with the decrease in the tunneling width. The results obtained have been summarized below in Table 8.1.

Table 8-1 Comparison of device parameters at 30 nm and 20 nm cavity length

Material	At 30 nm nano gap cavity			At 20 nm nano gap cavity		
	I_{ON}	**I_{OFF}**	**I_{ON}/I_{OFF}**	**I_{ON}**	**I_{OFF}**	**I_{ON}/I_{OFF}**
HfO_2	1.57×10^{-6}	1.374×10^{-14}	1.142×10^{8}	2.682×10^{-6}	1.3769×10^{-14}	1.947×10^{8}
Nitride	2.090×10^{-6}	1.488×10^{-14}	1.404×10^{8}	1.382×10^{-6}	1.74×10^{-14}	1.259×10^{8}
SiO_2	2.017×10^{-6}	1.36×10^{-14}	1.1483×10^{8}	2.4368×10^{-6}	1.3859×10^{-14}	1.758×10^{8}
Epoxy	2.009×10^{-6}	1.361×10^{-14}	1.477×10^{8}	2.435×10^{-6}	1.386×10^{-14}	1.756×10^{8}
Teflon	1.9637×10^{-6}	1.3644×10^{-14}	1.439×10^{8}	2.4044×10^{-6}	1.388×10^{-14}	1.732×10^{8}

Due to the introduction of biomolecules, with an increase in the dielectric constant, the tunnelling barrier width narrows [171, 172]. This will lead to an increase in an ON current. The effect of such structures on energy band diagram is given in figure 8.12. For the charged biomolecules trapped under the gates, the drain current increases. This is due to the decrease in the barrier width between the valence band of the source and the conduction band of the channel. Figure 8.13 demonstrates the change in the drain current when charged biomolecules are immobilized under the gate. Figure 8.14 provides the comparison of the drain current sensitivity with the p-i-n and p-n-p-n type FET biosensors as reported in [159]

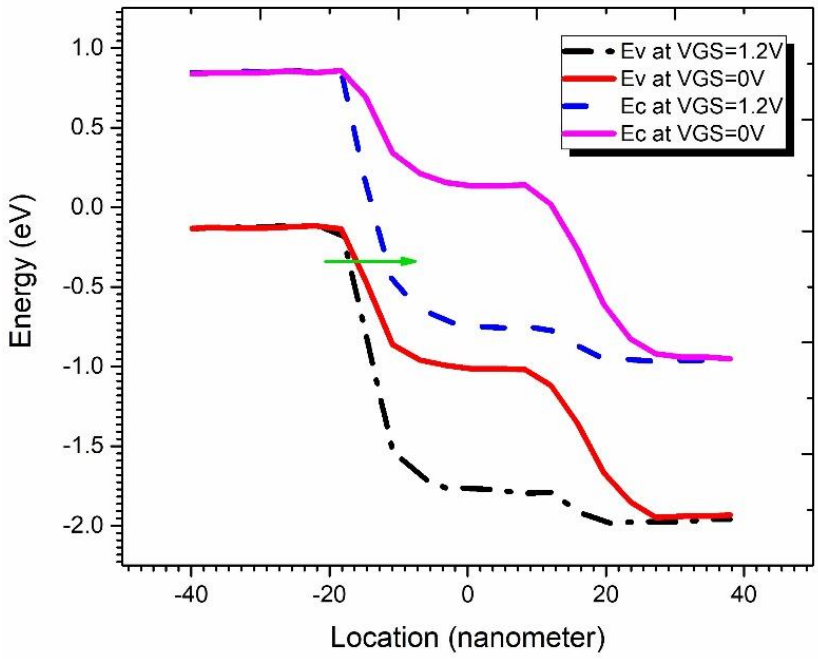


Figure 8.12 Energy band diagram for double gate DMTFET

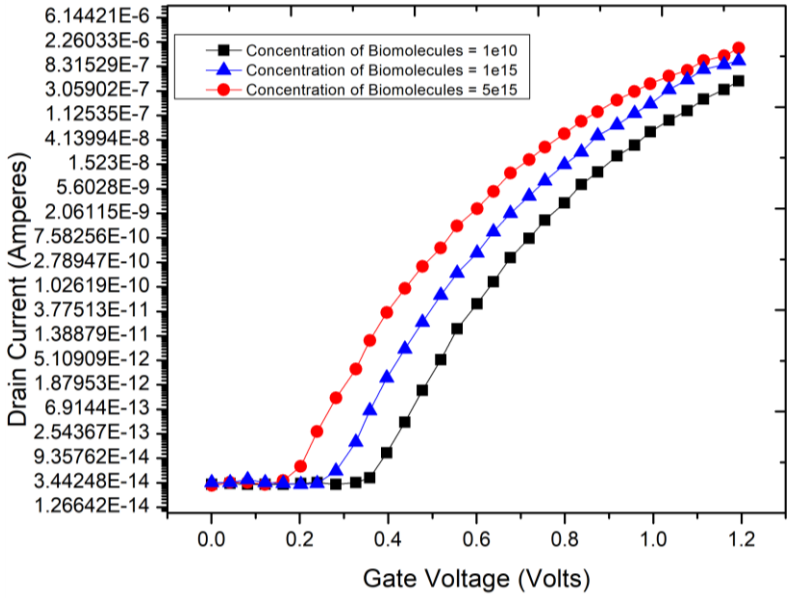


Figure 8.13 Comparison of the sensitivity of MOSFET and TFET based biosensors

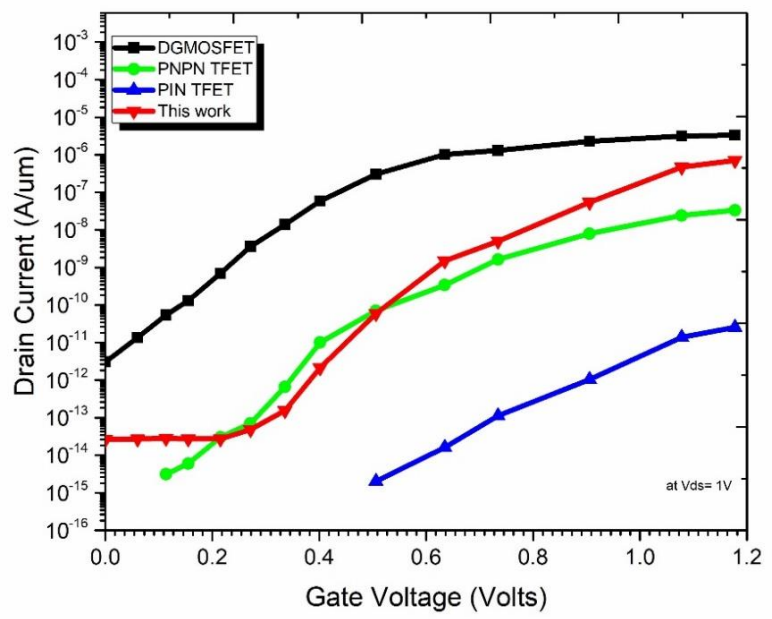


Figure 8.14 Variation of a drain current with concentration of biomolecules

The performance of a biosensor will be determined by the drain current sensitivity, which is given by:

$$S_{current} = \frac{I_D^{bio} - I_D}{I_D}$$

Where $S_{current}$ is the drain current sensitivity, I_D is the drain current before biomolecule conjugation and I_D^{bio} is the drain current after biomolecule conjugation. For the proposed HDBOX TFET biosensor, by substituting the values for the above equation we get: $S_{current} = \frac{(2.30809\times10^{-6})-(1.49087\times10^{-14})}{(1.49087\times10^{-14})} = 1.548 \times 10^{8}$

The comparison of the drain current sensitivity and I_{ON}/I_{OFF} ratio obtained in the proposed biosensor has been compared with the work of other researchers in table 8.2 below:

Table 8-2 Sensitivity comparison of the proposed biosensor with other research works

Parameters	**Ref. [136]**	**Ref. [171]**	**Ref. [172]**	**This work**
$\mathbf{S_{current}}$	1.934×10^3	3.0×10^2	1.0×10^5	1.548×10^8
$\mathbf{I_{ON}/I_{OFF}}$	1.09×10^{10}	1.0×10^9	1.0×10^6	1.947×10^8

The variations in the drain current sensitivity for DM TFET is illustrated for cavity length of 5 nm. Figure 8.15 represents the effect of the biomolecule conjugation by taking the effect of variations in the dielectric constant of a material. It is evident that the ON current is improved for high-K dielectrics. Different materials with varied gate dielectrics have been selected for the comparison. The curves show that the OFF current also increases with ON current improvements.

While running the simulation for the hetero-gate dielectric BOX based TFET, the device parameters have been kept same as it was used in the earlier cases. In this way, the advantages of high $\frac{I_{ON}}{I_{OFF}}$ ratio and a steeper subthreshold swing is retained. The gate work function provided is 4.7 eV. Band to band tunneling is enabled at the source channel junction. The gate- source voltage has been varied from 0 Volt to 1 Volt with a step size of 0.1 Volt, while as the drain source voltage has been kept constant at 1 Volt. It was observed that the higher dielectric constant provides the better drain current, which leads

to the better sensitivity. The drain source voltage has been kept at 1V. The highest $\frac{I_{ON}}{I_{OFF}}$ ratio achieved was 1.68×10^{8} (with $I_{ON}= 2.308 \times 10^{-6}$ and $I_{OFF} = 1.374\times 10^{-14}$). The results obtained have been compared with the SiGe DM-TFET and have been plotted in figure 8.16.

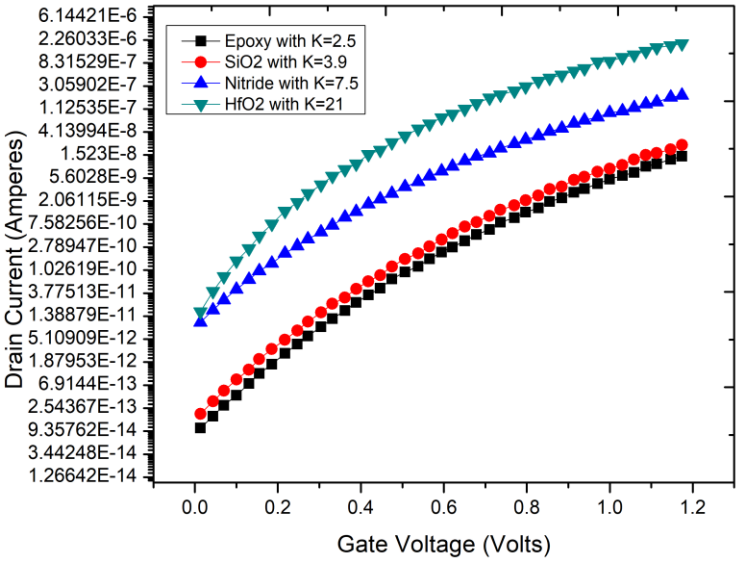


Figure 8.15 Variations in the drain current sensitivity with variation in Dielectric constant

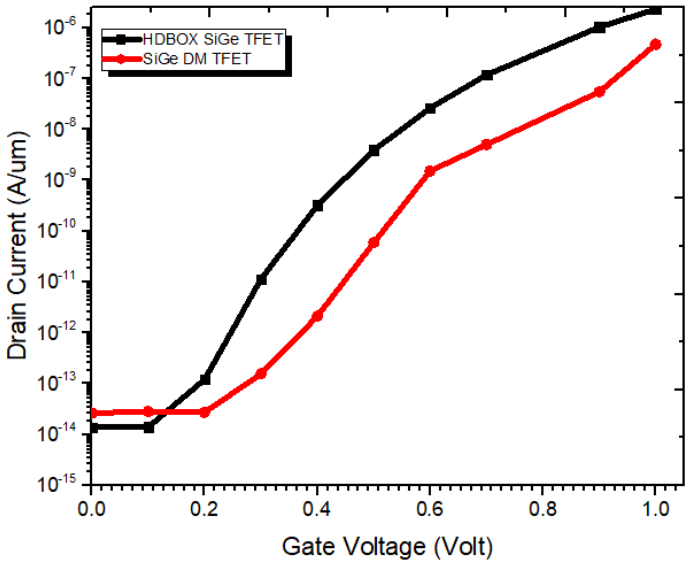


Figure 8.16 Drain current sensitivity of HDBOX SiGe TFET and SiGe DM TFET biosensor

8.4 Challenges

Due to the surface charge density of biomolecules, the electric field is screened out beyond the certain distance called as Debye screening length. The limit of detection in FET biosensors is closely correlated with Debye screening duration between the gate surface and the analyte solution. Thus, the accuracy of FET biosensors is strongly dependent on Debye distance. This is considered as one of the critical problems in FET biosensors. The electrostatic potential decreases exponentially towards zero due to differences in the surface charge density of the analyte molecules due to the screening effect. This critical length scale is called "Debye screening length" (λ_D). Thus, while designing FET biosensors, this critical effect must be taken into a consideration.

Moreover, the issue regarding size and the concentration of molecules also affects the effective detecting capability of a FET biosensor. Nowadays, biocompatible and wearable equipments are a point of focus for next generation devices. So, various other factors like impedance matching, high signal to noise ratio will also influence the characteristics of FET biosensors.

CHAPTER 9: CONCLUSION AND FUTURE SCOPE OF THE WORK

9.1 Conclusion

The conventional MOSFET has been the device of the choice for the designers for the fabrication of integrated circuits. However, due to the continuous scaling, the miniaturization of transistors leads to the degradation of the performance. This is mainly attributed to increased levels of static power dissipation and the effect of short channel parameters which become dominant at the smaller channel lengths. The work carried out in this thesis deals with the study of the heterojunction SiGe based tunnel FET device architecture as a potential replacement of the conventional MOS technology in the future. The tunnel FETs operate under the mechanism of band to band tunneling unlike the thermal carrier transport of the MOSFET technology. So, it was possible to achieve the subthreshold swing of the device lesser than 60 mV/decade so as to allow steeper transition. The research work carried out can be divided into five parts:

1. Study of the electrical characteristics of the proposed device. This includes the understanding of the underlying physics about the energy band diagrams and the surface potential. During, this course of study, the aim was to increase the $\frac{I_{ON}}{I_{OFF}}$ ratio and obtain a steeper subthreshold swing. These two characteristics are vital for the tunnel FET, if they have to be in par with the conventional CMOS technology.
2. Study of the short channel parameters of the proposed device. This includes the understanding of few short cannel parameters like, drain induced barrier lowering (DIBL) and the threshold voltage roll-off. In order to reduce the leakage currents, such parameters needed to be addressed.
3. Study of the ambipolar current transport in conventional tunnel FET. This includes the understanding of the ambipolar behaviour of the tunnel FET when a negative gate to source voltage is applied to the devices. This parameter is directly linked with the OFF current of the device, and was therefore an important parameter to study for improving the over all $\frac{I_{ON}}{I_{OFF}}$ ratio of TFETs.

4. Study of the analog performance of our proposed device. This includes the understanding of parameters which are important from the perspective of analog applications of the proposed device, for instance, transconductance, gain, cut-off frequency, etc.
5. Use of SiGe based heterojunction TFET as a biosensor for increased sensitivity to the charged or neutral biomolecules for the early detection and diagnosis of diseases. Detection of the biomolecules is evaluated with the changes in the value of the dielectric constant or an increase in the doping concentration.

From our studies, the significant contributions made are as follows:

1. The proposed device shows better performance in terms of the $\frac{I_{ON}}{I_{OFF}}$ ratio. The value comes around 3.72×10^{10} which is considerably high, when compared to the most of the existing architectures.
2. The lower subthreshold swing has often remained a challenging task in TFETs. In order to break the "Boltzmann tyranny" which is existent in MOSFETs, it was essential to devise an architecture with a lower subthreshold swing. For the proposed device, average subthreshold swing has been calculated as 28.57 mV/decade.
3. An effort has been made in regards to alleviating the short channel parameter effects in tunnel FET. The parameters being studied were, drain induced barrier lowering (DIBL) and the threshold voltage roll-off. The value of DIBL obtained in our device is 3.636 mV.
4. The effect of the ambipolar behaviour of the tunnel FET has also been studied. It results in the serious degradation of the OFF current hence limits the performance of TFET devices. By employing a buried oxide layer in our proposed device, an effort has been made to suppress the ambipolar current up to $V_{GS} = -0.3$ volts.
5. The analog performance of the proposed device has also been taken into the consideration while carrying the research work. Transconductance (g_m) is one such parameter which is a deciding factor for determining the gain of the device.

The value of g_m obtained is about 0.68 milli-Siemens, which is better from analog perspective. Moreover, since the subthreshold swing obtained for the proposed device is lesser, thus the device efficiency $\frac{g_m}{I_D} = \frac{ln10}{SS}$ becomes high.

6. Study of gate-source and gate-drain parasitic capacitances, as they play a critical role for determining the propagation delay and the high frequency behaviour of the device. Their variations with respect to the gate voltage have been understood. The range of the capacitances obtained was in the range of 0.1 to 1 femto-Farads.
7. Parameter variation analysis of the device has been performed as well. This is important because, as the technology progresses, there would be fluctuations in the electrical characteristics of the device. So, it becomes incumbent for a researcher that to improve the device reliability, the values being estimated are under control.
8. The cut-off frequency is another important parameter which determines the frequency range up to which a device can be amplified. For an analog design, it is must be as high as possible. For the proposed device, the value of f_T is around 446 GHz and is strongly dependent upon the gate capacitance and the transconductance.
9. Reduced electrical field at the drain-source tunneling junction. Use of high-κ dielectric material, hafnium oxide HfO_2 from the source-channel tunneling was effective for achieving it. Moreover, the source doping was on the higher side when compared to that of the drain region, so that asymmetry is maintained between these two terminals.
10. The device has also been studied under the variations in the temperature. This is important because, the energy gap of the material is dependent on the temperature and the mechanism of the band to band tunneling may get affected due to this property. So, we performed the temperature analysis from 200 Kelvin to 400 Kelvin for the performance of the drain current. We found out that ON current does not get affected with temperature variations. However, OFF current has a strong dependence on the temperature, and may degrade the overall $\frac{I_{ON}}{I_{OFF}}$ ratio at higher temperatures.

11. Study of operating principles and the working mechanism of various types of FET-based biosensors. Various critical illness diseases can be detected and treated early by identifying specific biomarkers using FET based biosensors and the same has been studied in this work. Study of operating principles and the working mechanism of various types of FET-based biosensors. The sensitivity of the biosensor has been improved by enhancing the sensitivity of the biosensor, owing to high $\frac{I_{ON}}{I_{OFF}}$ ratio and a steeper subthreshold swing obtained for the device. The nanogap cavity of 30 nm length has been created just below the gate terminal for the conjugation of the biomolecules. The highest $\frac{I_{ON}}{I_{OFF}}$ ratio achieved was 1.68×10^{8} (with $I_{ON}= 2.308 \times 10^{-6}$ and $I_{OFF} = 1.374\times 10^{-14}$). Results reveal that TFET based biosensor offers many advantages over FET based biosensors. The optimized value of drain current (sensitivity) has been obtained with an increase in doping concentrations or the dielectric constant at the gate region.

9.2 Future Scope of the Work

The current research has been conducted by studying the n-type proposed TFET structure. The research can be carried forward with the study of its counterpart, p-type TFET. This would pave a way for designing a complementary TFET device. Further, a compact model could be developed for the device using Verilog A which can be then exported to circuit simulation software like Cadence Virtuoso for performing circuit-level analysis of the device. The device being studied has been simulated by using the Kane's band to band tunneling model. In future, in order to perform the rigorous calculations, quantum simulation models like non energy green function (NEGF), atomistic simulations could also be tried, although it is computationally very laborious and frequently suffers from convergence issues. In terms of the biomedical applications, a TFET based biosensor is also an interesting topic of research, where the properties of the TFET can be utilized to improve the sensitivity of the biosensors in use. From the comprehensive study, it is concluded that the detection of biomolecules with the change of their dielectric constant is a good scope for future generation researchers. Moreover, TFET device plays a crucial role

for point of care application for getting accurate and reliable results because of its improved performance. Overall, it can be said that the tunnel FETs have an immense potential in terms of research, be it in terms of improving the device characteristics or in terms of digital and analog low power applications.

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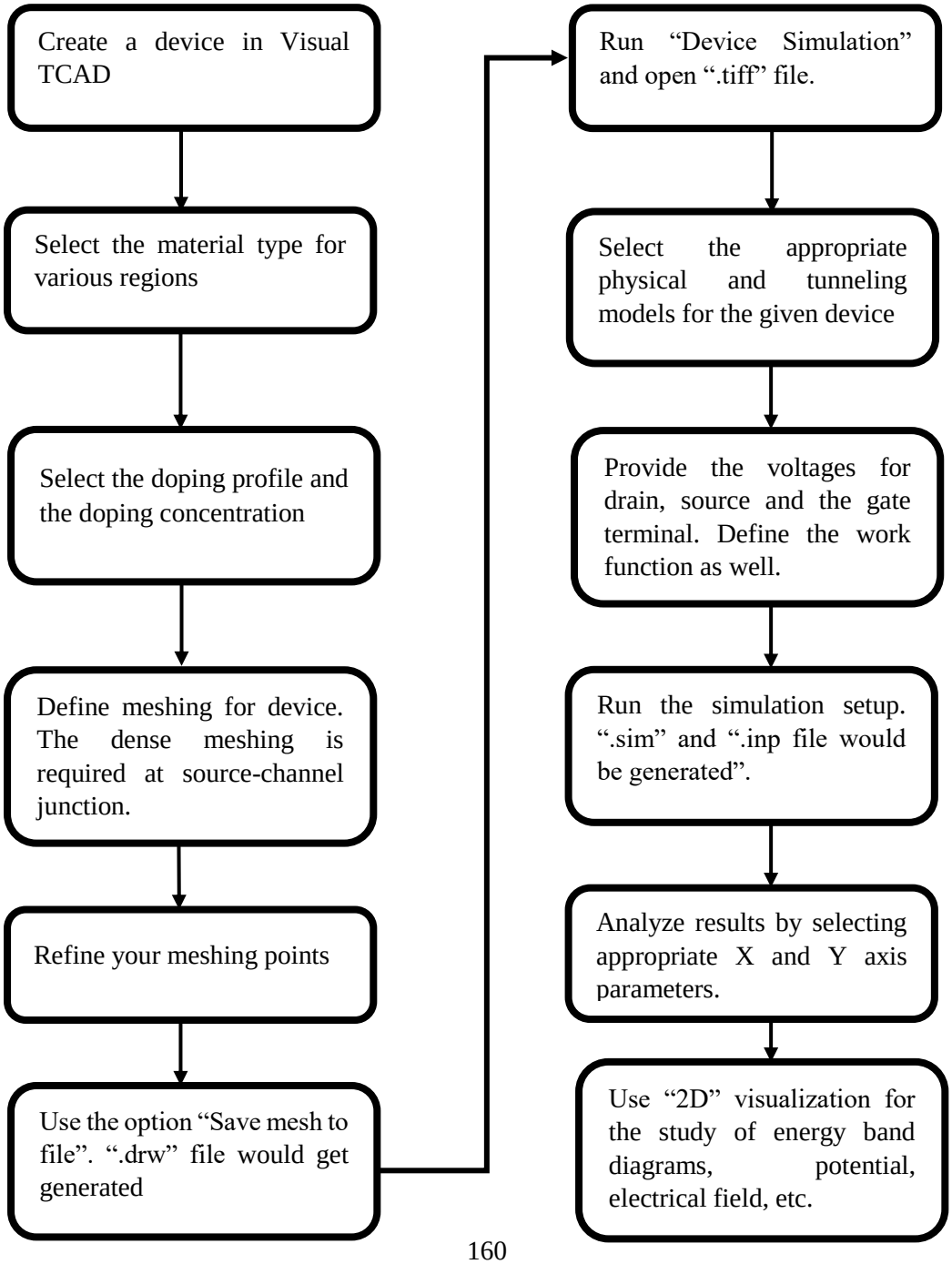
APPENDIX

A1: Visual TCAD Simulation Basics

In this appendix, we would provide a work flow for the simulation of the device.



A2: Few data points of the proposed device:

TABLE A2.1: $logI_D\ v/s\ V_{GS}$ transfer characteristics of the device

Gate Voltage (Volts)	**Drain Current (A/μm)**					
	$V_D = 0.05V$	$V_D = 0.1V$	$V_D = 0.3V$	$V_D = 0.6V$	$V_D = 0.9V$	$V_D = 1.2V$
-0.5	1.75E-12	2.07E-12	3.57E-12	5.81E-12	7.60E-12	8.89E-12
-0.4	1.78E-13	1.94E-13	2.49E-13	3.15E-13	3.49E-13	3.68E-13
-0.3	8.58E-15	9.05E-15	9.92E-15	1.07E-14	1.11E-14	1.19E-14
-0.2	1.15E-14	1.18E-14	1.20E-14	1.22E-14	1.24E-14	1.27E-14
-0.1	1.24E-14	1.26E-14	1.27E-14	1.29E-14	1.29E-14	1.32E-14
-0	1.34E-14	1.36E-14	1.38E-14	1.40E-14	1.42E-14	1.44E-14
0.1	1.11E-10	1.12E-10	1.17E-10	1.25E-10	1.31E-10	1.37E-10
0.2	2.09E-08	2.10E-08	2.16E-08	2.23E-08	2.29E-08	2.33E-08
0.3	3.65E-07	3.67E-07	3.72E-07	3.80E-07	3.86E-07	3.91E-07
0.4	2.19E-06	2.20E-06	2.22E-06	2.25E-06	2.28E-06	2.30E-06
0.5	7.47E-06	7.49E-06	7.55E-06	7.62E-06	7.69E-06	7.74E-06
0.6	1.82E-05	1.83E-05	1.85E-05	1.86E-05	1.87E-05	1.88E-05
0.7	3.58E-05	3.62E-05	3.67E-05	3.70E-05	3.72E-05	3.74E-05
0.75	4.73E-05	6.18E-05	6.36E-05	6.43E-05	6.47E-05	6.50E-05
0.8	6.05E-05	7.75E-05	9.99E-05	0.000102	0.000102	0.000103
0.9	9.21E-05	9.50E-05	0.000145	0.000149	0.000151	0.000152
1	0.00013	0.000135	0.000199	0.000207	0.00021	0.000212
1.1	0.000172	0.00018	0.00026	0.000273	0.000279	0.000282
1.2	0.000217	0.000229	0.000325	0.000346	0.000355	0.000361
1.3	0.000265	0.000281	0.000393	0.000424	0.000438	0.000447
1.4	0.000313	0.000333	0.000463	0.000505	0.000525	0.000537

TABLE A2.2: Work Function variation of the device

Gate Voltage (Volts)	**Drain Current (A/μm)**			
	WF = 4.7	WF = 4.5	WF = 4.33	WF = 4.17
-0.5	2.07E-12	9.05E-15	1.24E-14	9.75E-14
-0.4	1.94E-13	1.18E-14	1.30E-14	8.06E-10
-0.3	9.05E-15	1.26E-14	9.02E-12	5.84E-08
-0.2	1.18E-14	1.36E-14	6.22E-09	6.81E-07
-0.1	1.26E-14	1.12E-10	1.80E-07	3.32E-06
0	1.36E-14	2.10E-08	1.38E-06	1.01E-05
0.1	1.12E-10	3.67E-07	5.41E-06	2.29E-05
0.2	2.10E-08	2.20E-06	1.44E-05	4.31E-05
0.3	3.67E-07	7.49E-06	3.00E-05	5.61E-05
0.4	2.20E-06	1.83E-05	5.33E-05	7.10E-05
0.5	7.49E-06	3.62E-05	6.79E-05	0.000106
0.6	1.83E-05	6.18E-05	8.43E-05	0.000148
0.65	3.62E-05	7.75E-05	0.000122	0.000194
0.7	6.18E-05	9.50E-05	0.000166	0.000244
0.8	7.75E-05	0.000135	0.000214	0.000296
0.9	9.50E-05	0.00018	0.000265	0.000349
1	0.000135	0.000229	0.000318	0.000402
1.1	0.00018	0.000281	0.00037	0.000454
1.2	0.000229	0.000333	0.000423	0.000504
1.3	0.000281	0.000386	0.000474	0.000553
1.4	0.000333	0.000439	0.000524	0.0006
1.5	0.000389	0.000489	0.000572	0.000644

TABLE A2.3: Dielectric material variation of the device

Gate Voltage (Volts)	**Drain Current (A/μm)**			
	Epoxy	Hafnium	Nitride	Teflon
0	3.76E-11	4.75E-11	4.18E-11	3.51E-11
0.1	6.23E-09	7.37E-09	6.72E-09	5.94E-09
0.2	1.17E-07	1.34E-07	1.24E-07	1.13E-07
0.3	7.84E-07	8.70E-07	8.21E-07	7.61E-07
0.4	2.96E-06	3.23E-06	3.08E-06	2.89E-06
0.5	7.97E-06	8.59E-06	8.25E-06	7.80E-06
0.6	1.72E-05	1.84E-05	1.78E-05	1.69E-05
0.7	3.22E-05	3.41E-05	3.30E-05	3.16E-05
0.8	5.41E-05	5.72E-05	5.55E-05	5.33E-05
0.9	8.43E-05	8.87E-05	8.62E-05	8.31E-05
1	0.000123	0.000129	0.000126	0.000122
1.1	0.000172	0.00018	0.000175	0.00017
1.2	0.00023	0.000239	0.000234	0.000227

LIST OF PUBLICATIONS

International Journals:

1. Pindoo, I.A., Sinha, S.K. & Chander, S. "Improvement of Electrical Characteristics of SiGe Source Based Tunnel FET Device". Springer, *Silicon* (August. 2020). https://doi.org/10.1007/s12633-020-00674-0
2. Pindoo, I.A., Sinha, S.K. "Increased Sensitivity of Biosensors using Evolutionary Algorithm for Bio-Medical Applications". *Radioelectron. Commun.Syst.* **63,** 308–318 (June, 2020). https://doi.org/10.3103/S0735272720060047
3. Pindoo, I.A., Sinha, S.K. & Chander, S, "Analog/RF Performance Analysis of Heterojunction Tunnel FET with Temperature Analysis" Springer, *Applied Physics A* 127, 748 (2021). https://doi.org/10.1007/s00339-021-04891-1
4. **Submitted:** Pindoo, I.A., Sinha, S.K., **"**Effect of Spacer Dielectrics on Device Performance of a SiGe Based Heterojunction", 2021, *Int. J. of Nano and Biomaterials*, Inderscience Publications

International Conferences:

1. I.A. Pindoo and S. K. Sinha, "Hetero-gate Dielectric with Hetero Dielectric BOX for Suppressing Ambipolar Current in Tunnel FETs," *IEEE International Conference on Intelligent Engineering and Management (ICIEM)*, London, UK, 17-19 June, 2020, pp. 44-47, 10.1109/ICIEM48762.2020.9160161
2. I.A. Pindoo, S. K. Sinha and S. L. Tripathi, "Performance Analysis of Double Gate Heterojunction Tunnel Field Effect Transistor," *2019 IEEE International Conference on Cutting-edge Technologies in Engineering (ICon-CuTE)*, Uttar Pradesh, India, 14-16 November, 2019, pp. 28-32, 10.1109/ICon-CuTE47290.2019.8991467
3. I.A. Pindoo and S. K. Sinha, "Temperature Variation Analysis of SiGe Source based Heterojunction Tunnel", *4th IEEE International conference on Devices for Integrated Circuit (DevIC)*, Kalyani, India, 19-20 May, 2021, pp. 251-255, 10.1109/DevIC50843.2021.9455857