DESIGN AND OPTIMIZATION OF LOW POWER HIGH PERFORMANCE TRIPLE GATE FINFET FOR SUB 22nm TECHNOLOGY

Thesis Submitted for the Award of the Degree of

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By

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2023

DECLARATION

I, hereby declared that the presented work in the thesis entitled "**DESIGN AND OPTIMIZATION OF LOW POWER HIGH PERFORMANCE TRIPLE GATE FINFET FOR SUB 22nm TECHNOLOGY**" in fulfilment of degree of **Doctor of Philosophy (Ph. D.)** is outcome of research work carried out by me under the supervision Dr Suman Lata Tripathi, working as Professor in the School of Electronics and Electrical Engineering of Lovely Professional University, Punjab, India. In keeping with general practice of reporting scientific observations, due acknowledgements have been made whenever work described here has been based on findings of other investigator. This work has not been submitted in part or full to any other University or Institute for the award of any degree.

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CERTIFICATE

This is to certify that the work reported in the Ph.D. thesis entitled "**DESIGN AND OPTIMIZATION OF LOW POWER HIGH PERFORMANCE TRIPLE GATE FINFET FOR SUB 22nm TECHNOLOGY** " submitted in fulfillment of the requirement for the reward of degree of **Doctor of Philosophy (Ph.D.)** in the Electronics and Communication Engineering, is a research work carried out by Kalasapati Bindu Madhavi, 41900188 is bonafide record of her original work carried out under my supervision and that no part of thesis has been submitted for any other degree, diploma or equivalent course.

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ABSTRACT

The substantial short channel effects of the typical MOSFET transistor have made scaling progressively challenging. Reduced performance and greater average power consumption result from scaling down the width and length of MOS devices is observed. Therefore, a viable alternative to bulk MOS at the nanoscale is fin-type field effect transistors (FinFET). This device is chosen as the fabrication process followed for a FinFET design is essentially as same as for a traditional MOS transistor.

A double gate or triple gate structure is formed by the gate being positioned on either two or three sides of a channel that is constructed on a substrate. Integrated Circuits are benefitted significantly from the FinFET transistor innovation. Higher current drive capability and Low Power Consumption are the major advantages of multi gate MOSFETs. FinFETs can readily replace MOSFETs in near future due to the similar designing method. The quasi-planar structure of FinFETs is also the part of the double gate (DG) transistor family. As the channel is constructed perpendicular to the wafer and the current trajectory is parallel to it, they are termed as quasi-planar. FinFET through its multi gate terminals tends to provide a variety of design options for the users, including the ability to individually for regulating or shorting them. The thin silicon body and two electrically connected gates of the FinFET are widely recognized for lowering the short channel effects that has proved in the literature.

My work mainly focused on the three technologies, namely 10nm, 18nm and 22nm. By using Cogenda Visual TCAD, the device all the trees technologies of triple-gate FinFET are designed, examined and simulated and evaluated the electrical characteristics. The device performance optimization is done by analyzing drain current characteristics at different channel lengths, oxides, different doping levels and different temperatures for the proposed 10nm and 22nm Triple gate FinFET . The electrostatic behavior is also evaluated which include electrical behavior, surface potential, electron as well as hole density characteristics from device framework that are displayed. A tri gate 18nm FinFET has been implemented for bio sensing techniques. . Also in this work, the performance of the 18nm triple gate FinFET device is analyzed with different cavity lengths such as 5nm, 7nm and 10nm. The observation shows that the OFF current becomes small when cavity length decreases. Thus a high sensitive 18nm triple gate FinFET is designed with highly threshold voltage and I_{ON}/I_{OFF} current ratio with several dielectric constants of both neutral and charged molecules

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Kalasapati Bindu Madhavi

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I_{ON}	On current
I_{OFF}	Off current
V_{Th}	Threshold Voltage
V_{GS}	Gate to source voltage
V_{DS}	Drain to source voltage
L_g	Gate length
C_{ox}	Oxide capacitance
P_S	Static power dissipation
P_D	Dynamic power dissipation
V_{DD}	Supply voltage
C_L	Load capacitance
α	Switching probability
f	Device operational frequency
e	Electronic charge
h	Planck's constant
t_{ox}	Oxide thickness
t_{Si}	Silicon body thickness
I_D	Drain current
T	Temperature
k	Boltzmann constant
SS	Subthreshold swing
μ	Mobility
$E_{\perp}$	Transverse component of the electrical field.
N_S	Doping at the source region
N_D	Doping at the drain region
N_{ch}	Doping at the channel region

L_{ch}	Channel Length
E	Electrical field
C_D	Depletion capacitance
$V_{D_{SAT}}$	Supply voltage during saturation mode
$V_{D_{LIN}}$	Supply voltage during linear mode
$V_{T_{LIN}}$	Threshold voltage during linear mode
$V_{T_{SAT}}$	Threshold voltage during saturation mode
ϕ	Gate work function
C_{GS}	Gate-source capacitance
C_{GD}	Gate-drain capacitance
C_{GG}	Total gate capacitance
f_T	Cut-off frequency
g_m	Transconductance
g_m/I_{DS}	Device efficiency
V_T	Thermal voltage

LIST OF ABBREVIATIONS

BOX	Buried oxide layer
CMOS	complementary metal oxide semiconductor
DD	Drift-diffusion
DG FinFET	Double gated Fin Field Effect Transistor
TG FinFET	Triple Gated Fin Field Effect Transistor
DIBL	drain induced barrier lowering
GBP	Gain-bandwidth product
IC	Integrated Circuit
VLSI	Very Large Scale Integrated Circuit
FinFET	Fin Field Effect Transistor
JL FinFET	Junction less Fin Field Effect Transistor
IG FinFET	Insulated Gate Field Effect Transistor
MOSFET	metal oxide semiconductor field effect transistor
NMOS	N channel metal oxide semiconductor
PDA	Personal Digital Assistant
PMI	Physical Model Interface
PMOS	P channel metal oxide semiconductor
QC	Quantum confinement
RF	Radio frequency
SCE	Short channel effects
SOI	Silicon on Insulator
SS	Subthreshold swing
TCAD	Technology computer-aided design

CHAPTER 1: INTRODUCTION

The familiarity and expansion of MOSFET technology for digital and power approaches are operated by two main benefits over bipolar junction transistors. Among those advantages is the effort to utilize the Metal-oxide semiconductor Field-Effect Transistor (MOSFET) devices in high-frequency switching implementations. Metal-oxide semiconductor Field-Effect Transistors are easy to operate due to their regulated electrode being isolated from current conducting silicon; hence, constant ON current is inessential. After metal-oxide semiconductor Field-Effect Transistors are switched on, their drive current is almost zero. Therefore, regulating the power and corresponding storage period in metal-oxide semiconductor Field-Effect Transistor is highly decreased. This firstly removes the model trade-off in between on-state voltage drop that is inversely proportional to overflow control charge and switch-off period. As an output, MOSFET technology assures the utilization of simpler and highly beneficial drive circuits with important economic advantages compared to bipolar devices. [1]

1.1 About Conventional MOSFETs: A MOSFET is the structure consisting of the base material as silicon called as body or substrate. It is the foundation over which whole device would be constructed. Over the substrate, a thin silicon dioxide layer is deposited over the material. The drain and the source are being doped with the same type of the material. The source and the drain terminals are attached through the metallic contacts. The gate terminal is made up of polysilicon and remains insulated from the channel due to the SiO_2 layer.[2]

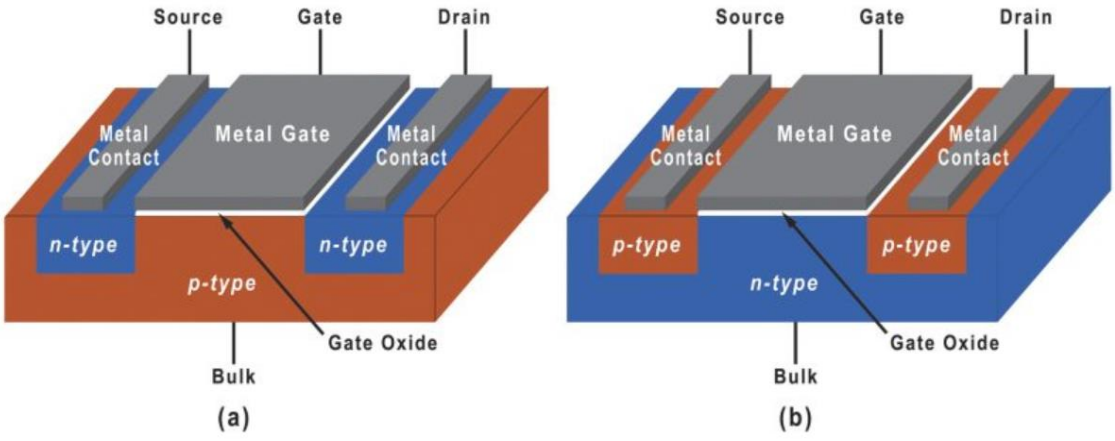


Fig 1.1 MOSFET (a) n-channel (b) p-channel

MOSFETs can be of two categories: n-channel and p-channel Metal-Oxide Semiconductor Field-Effect Transistor. The drain and source regions of an n-channel Metal-Oxide Semiconductor

Field-Effect Transistor are greatly doped with n+ type dopants, as a result the current conduction would be due to the electrons as charge carriers. While, in the p- channel MOSFET, the drain and source are both heavily doped with p+ style dopants, as a result the current conduction would be due to the holes as charge carriers [3]. The cross sectional diagram provided in figure 1.1 represents both N-channel and P-channel MOSFETs.

The current conduction from source terminal to drain is controlled by the application of thegate-source voltage. The p-type substrate is used in NMOS transistors and is usually connected to the ground. The voltage at drain side would be greater as compared to the source. Due to the absence of the channel, no current would flow from source to drain if the gate-source voltage was zero. Therefore, we assume the transistors do not operate. If the gate to source voltage is gradually increased, an electric field is developed across the channel; as a result free electrons are attracted at Si-SiO_2 interface. When a gate voltage becomes sufficiently high, a situation is created where the number of free electrons available in the channel is greater than the number of holes in the p-substrate. This phenomenon is referred as an inversion. Now that, the channel has become N-type electrons can move from the source side to the drain terminal, and there would be rise in the drain current.

Similarly the n-type substrate of a PMOS transistor is normally connected to the drain voltage. The voltage at drain side would be lesser than that of the source. If the gate-sourcevoltage is zero or even at the positive voltage, then no current would travel from source todrain, due to absence of the channel. Thus, we assume that the transistor has turned off. When the voltage applied at gate is in negative, an electric field is developed across the channel; as a result free holes are attracted at Si-SiO_2 interface. When a gate voltage becomes sufficiently negative in magnitude, a situation is created where the amount of free holes at the channel outnumbers the electron numbers available in the n-substrate. Again, the channel has become inverted (p-type), it would be feasible for holes to move from the source to the drain terminal, and drain current starts to rise. Thus, whenever the gate voltage applied is higher than the MOSFET's threshold voltage, astrong channel inversion occurs below the gate. The material used to build the MOS structure determines the threshold voltage. There occurs a deposition of holes in PMOS and electrons in NMOS below the gate. Then, the drain voltage sweeps the charge carriers,and hence the current flows in the MOSFET. [4, 5]

Figures 1.2 and 1.3 presents a standard form of ultra thin type of MOSFET and a double-gate MOSFET. The framework of double gate is reversed by continuing the gate leakage current in its inexpensive form.

All gate electrodes in the transistor are self-aligned using standard lithography techniques. Dynamic Metal Oxide Semiconductor logic circuits are utilized in faster Very Large Scale Integrated chips to reach the greatest device implementation. Noise is the main problem in the structure of dynamic logic circuits. In the deep sub-micron region, the noise margin of dynamic logic circuits is inexpensive and highly expected to leads to logical failure. Dynamic logic circuits have various noise sources such as charge sharing noise, leakage noise, crosstalk noise, power and ground noise, substrate noise, etc. [6].

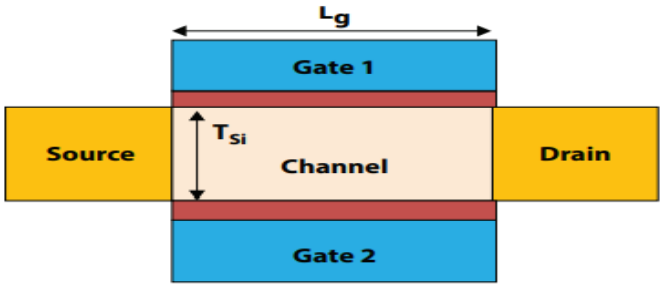


Fig 1.2 Double gate MOSFET

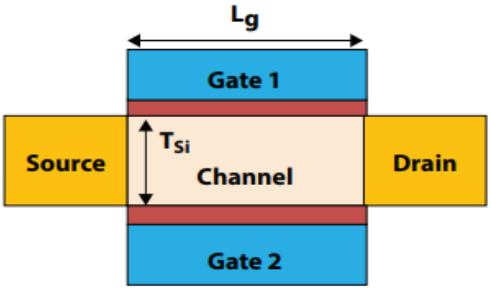


Fig 1.3 Planar Double Gate MOSFET

One of the applications of the MOSFET is that, they act as a switch when operated under cut-off and saturation regions. As an ideal switch, it is expected that when a transistor is turned off, it does not dissipate any power, and when turned on, it would deliver a large amount of current. However, the MOSFET used in practical applications exhibit a small leakage current as well, thus even when turned OFF, some power would get consumed. It is referred as static power dissipation (P_S), and is represented by:

$$P_s = V_{DD} I_{OFF} \quad \text{.....(1.1)}$$

In the above equation, V_{DD} represents the supply voltage and I_{OFF} represents the leakage current. Besides, When a MOSFET transitions from ON to OFF state or vice versa, a significant power gets consumed as well. This type of power consumption is called as dynamic power dissipation (PD) and is given by the following relation:

$$P_D = V_{DD}^2 C_L \alpha f \quad \text{.....(1.2)}$$

In the above equation, V_{DD} represents the supply voltage, f denotes operational frequency, C_L is the load capacitance and α is the switching probability. C_L represents the combination of the input capacitances and interconnects capacitances [7].

1.2 Scaling of CMOS Technology: Scaling of the standard MOSFET transistor becomes very tough due to its high short-channel impacts. Reducing the width and length of MOS device measurements causes lower implementation and higher average power utilization. Dynamic MOS logic circuits are utilized in faster executed Very Large Scale Integrated chips to reach the greatest device execution.

Noise is the main problem in structure of dynamic logic circuits. [8] At present the main goal of the researchers in the MOSFET technology has been to miniaturize the size of the transistors, so that more and more components can be accommodated on a given area. This would also increase the functionality of the given chip, as the number of operations it can perform would increase as represented in figure 1.4.

This exponential trend in miniaturization was predicted by G. Moore, which states: "After every 18 months, the number of components in an integrated circuit doubles". From the past five decades, Moore's law has stood true and this law is being seen as a benchmarkof industry progress [8]. Moreover, the advantages of the CMOS scaling are that the input capacitance of the MOSFET decreases and the current driving capability of MOSFET increase. However, the constraint remains as it is, instead of the fact that the driven current of MOSFETs increases, but because of its limitation due to the short channel effects, the I_{OFF} also rises due to the shorter gate length [9].

As a result of the increase in I_{OFF}, an increase in the power dissipation occurs statistically. The aggressive pace at which the CMOS scaling is done, it is predicted by the researchers that the range of dissipation observed in static power in conventional MOSFETs will soon overcome the range of dynamic power dissipation. The other major limitation of static power dissipation is that it would drain large power from the battery even when the device is turned OFF. This would result in the draining of the battery although the device is not in use.

For a hand held devices like PDA, smart phones, etc., it would be detrimental in terms of their battery performance. Furthermore, the static power dissipation would also result in the heat getting produced in the IC resulting in the temperature rise, although the gadget might have been optimized for the best performancewith respect to the ambient room temperature.

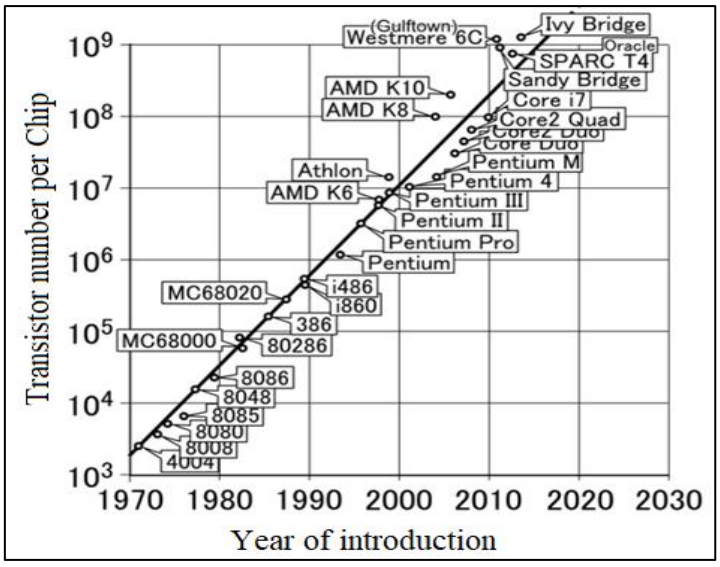


Fig 1.4 Illustration of Moore's law [10]

Equations (1.1) and (1.2) provide us someparameters with which the power dissipation could be reduced. However, the fundamentallimitation of MOSFET is that: to increase current by tenfold, around 60 mV of voltage is required (ideally). This constraint occurs due to the Maxwell-Boltzmann distribution, andis more popularly referred as "Boltzmann tyranny". It is important in the MOSFET to achieve the current in the range of around ($\sim 10^4$ to 10^6) so that OFF state can be distinguished from ON state. Thus, accordingly we can say, that the minimum amount of supply voltage required would be $60 \times \log(10^6) = 360$ mV. This result also indicates thatif the supply voltage is scaled aggressively to a smaller value, it would be extremely difficult to distinguish between the OFF-ON switching. This would prevent the MOSFETto act as a switch. Therefore, we can conclude that due to the "Boltzmann tyranny" the conventional MOSFETs cannot be used as a switch at ultra-low supply voltages. [11]

1.3 Advanced FET Devices: Advanced mobile and computing systems are innovating at a considerable value of delivering high implementation in lower form factors with great power capabilities. Hence, at the beginning of the integrated circuit industry, model metrics like execution, power, area, value, and time to market stayed the same. [12] Actually, with every recent technology generation, there is Moore's Law about optimizing those aspects to construct the portable feasible transistor size. If Gordon Moore had laid out his law back in 1965, he would have realized about 50 parts of the design. Recent chips contain billions of transistors and model teams' efforts for better, faster, cheaper products. Fin Field Effect Transistor (FIN FET) is a transistor structure initially implemented by Chenming Hu and his colleagues at the University of California at Berkeley that effort to get rid of least kinds of SCE (Short Channel Effect).

At the beginning, Fin Field Effect Transistor was informed to utilize Silicon-On-Insulator (SOI).SOI FIN Field Effect Transistor with thick oxide on top of fin is known as “Double-Gate” and on sides is known as “Triple-Gate” Fin Field Effect Transistors.

1.4 Fin shaped Field Effect Transistors (FinFET): A viable alternative to bulk MOS at the nanoscale is fin-type field effect transistors (FinFET). This is so because the fabrication process for a FinFET is essentially the same as for a traditional MOS transistor. A multigate gadget is a fin-shaped field-effect transistor (FinFET). A double gate or triple gate architecture is formed by the gate being positioned on two or three of the channel's sides, in this type of MOSFET it is constructed on a substrate. FinFET transistor approaches in Integrated Circuits have more substantial advantages than the more common planar approach. The main benefits of multi gate MOSFETs are their increased current drive capabilities and reduced power usage. [13]

FinFETs could readily replace MOSFETs in the further future due to the identical fabrication method. The quasi-planar structure of FinFETs makes them members of the double gate (DG) transistor family [6]. They are referred to as quasi-planar because the channel is constructed perpendicular to the wafer and the current trajectory is parallel to it. FinFETs' gate terminals provide a variety of design options, including the ability to individually regulate or short them. The thin silicon body and two electrically connected gates of the FinFET are widely known for suppressing the short channel consequences in the literature. [14]

FinFETs' wide range of design possibilities and improved channel management provide low power solutions with increased noise tolerance. A multi-gate device known as a FinFET is a form of MOSFET (metal-oxide-semiconductor field-effect transistor) which is constructed upon a substrate with gates positioned on two, three, or four of the channel's sides to create a double gate structure[10,15]. When it comes to designing integrated circuits, FinFET transistor architecture has many more important advantages than the more common planar approach. It has been noted that every two years, a particular silicon region doubles in transistor count. Design choices for FinFETs comprise 3D designs that just resemble fins and 2D and 3D architectures that extend over the substrate. FinFET produces superior efficiency with less power loss and lower threshold voltages.

FinFET technology plays a pivotal role in advancing health monitoring and biomedical applications by offering improved power efficiency, miniaturization, high performance, sensitivity, biocompatibility, multi-functionality, flexibility, and signal integrity [16]. These characteristics make FinFETs well-suited for the development of innovative and efficient solutions in the field of healthcare technology.

Due to reduced leakage power consumption, additional FinFET may be integrated into an identical chip zone. Therefore, it can be inferred from the development of FinFET technology which will proceed in a specific way. A comparison of triple-gate (TG-FinFET) and planner DG having vertical (DG-FinFET) Fin shaped double-gate architectures is shown in Figures 1.5 and 1.6 In this planar substrate, the channel would perform a small amount of leakage current when the device is in the OFF state. The gate's length in FinFETs is equidistant from the channel's thickness. [17, 18]

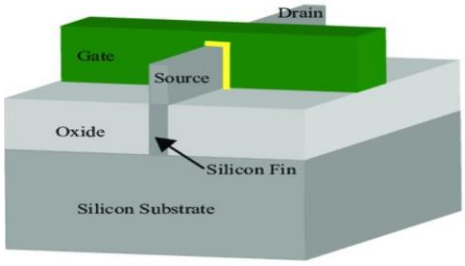


Fig 1.5 3D Structure of FinFET

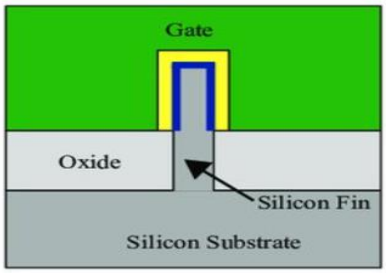


Fig 1.6 Cross Sectional View of FinFET

FinFETs become more prioritised with the advancement of MOSFETs, as the channel length of the devices has always steadily decreased to allow for the production of small, quick devices. The requirement of FinFETs is for more compact, smaller devices and is highlighted by the MOSFET-related metrics, which also gives the reason that why the MOSFET is an unsuitable option for those applications. The gate electrode's length is its shorter portion, and its breadth is its longer portion. The short-channel impacts become more pronounced when a MOSFET's channel length decreases.

1.5 Short Channel Effects in MOSFET: The reasons for the occurrence of short channel effects in the MOSFET are as follows:

(1)Electron drift characteristics limitations

(2) When the length of the channel is shortened, the threshold voltage changes.

By definition, a short channel device is one in which the channel length **a**nd the depletion region thickness is almost off the same order in magnitude [19 20]. As the channel length decreases, the lateral electrical field increases. For lower field values, the drift velocity is directly proportional to the electrical field, but as the electrical field increases, it begins to saturate. It is known as velocity saturation, and has a major impact on short channel MOSFETs' current voltage characteristics. [21]

1.5.1 Drain Induced Barrier Lowering Effect: In the long channel MOSFET, the source to drain channel is exclusively controlled by the gate voltage. Barrier height at source to channel modulates the gate voltage, causing the electrons to drift from the source to the drain. But, due to CMOS scaling, the channel length is shortened aggressively, thus the drain-channel and the source-channel interface interact with each other. So the gate voltage regulates the height of the obstacle between the source and the channel. The electron energy levels would be reduced, as well as the source to channel barrier height as shown in figure 1.7. This leads to the phenomena called as drain induced barrier lowering (DIBL) effect. The result would be an increase in the leakage current [22-24]. This effect is not so prominent in long channel devices simply because there is no interaction between the two depletion regions.

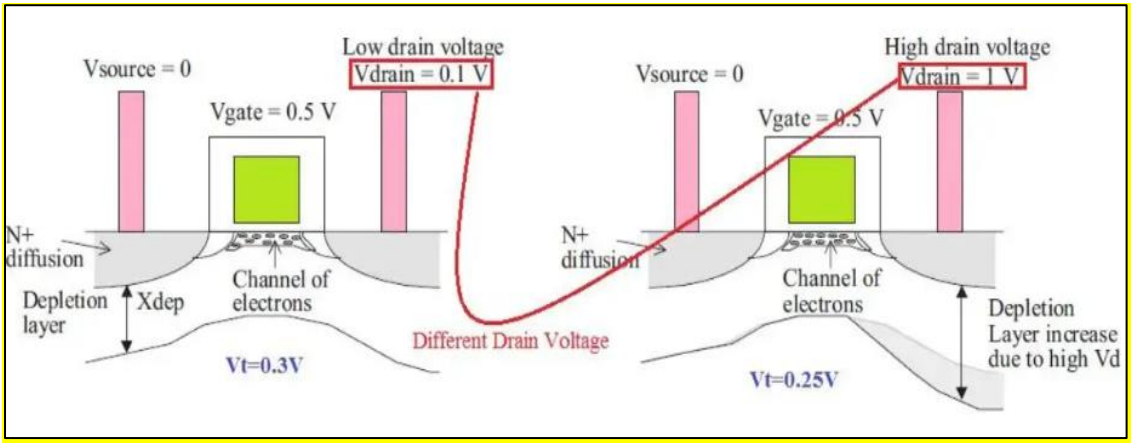


Fig 1.7 DIBL effect in MOSFET [24]

Because of the heavy doping at drain and source regions of MOSFET, there is an overlap with the p-channel substrate. Since the gate length has already been shortened due to the scaling, so the width of the depletion junctions becomes significant. As a result, the channel is not any longer solely controlled by the applied gate voltage. Besides, the control over the charge on the channel by the gate voltage also reduces. In comparison to a non-depleted MOS capacitor, the voltage required to invert the channel is significantly lower.

The “threshold voltage roll-off” is a well-known short channel effect that exhibits the decrease in threshold voltage as gate length decreases [25]. The potential barrier is decreased although gate-source voltage is lesser than the threshold voltage V_{th}, allowing current to flow across source and drain. The subthreshold current ($V_{gs}<V_{th}$) is the current that flows in the channel under such conditions. A steep transition is required from ON to OFF state in the current, and vice - versa, for any device to act as a switch. However, as discussed at the beginning of the chapter, a fundamental limit for the rate at which current changes in accordance to the applied

gate voltage is characterized by thermal current transport across the source–channel barrier height in case of a MOSFET.

An ideal MOSFET switch should do a smooth and abrupt transition from ON position to OFF position, when voltage at gate terminal is lesser to the threshold voltage and should go from OFF state to ON state, when the voltage at gate side is higher than the threshold voltage asshown in Figure 1.8. Subthreshold swing is important feature which measures the degree of abruptness of the transition from ON position of the transistor to the OFF position, and vice versa. It represents the minimum quantity of gate voltage needed to ten-fold the draincurrent [26].

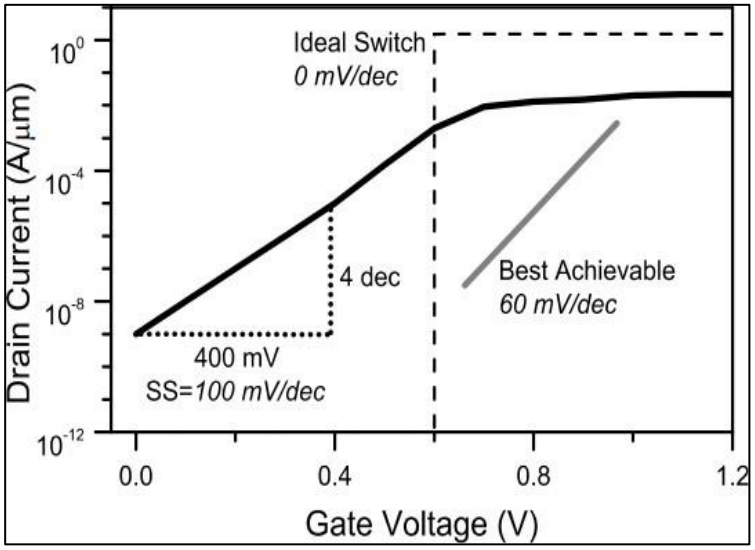


Figure 1.8 Typical NMOS switch's characteristics and a comparison to an ideal switch

1.5.2 Effect of quantum tunneling: Tunnel effect of the quantum is a quantum desire that arises, if those particles travel along the barrier that, according to assumptions of conventional physics, would be hard to travel [27].

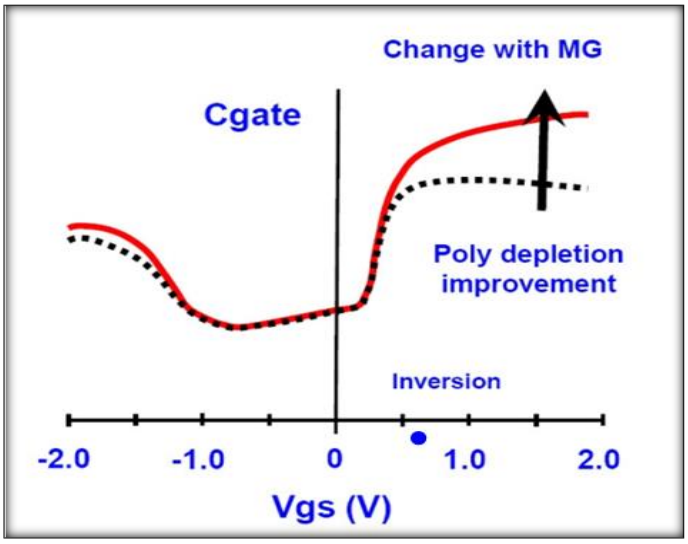


Fig. 1.9 Poly depletion improvement over metal gate. [27]

A quantum tunneling process has a n source and p drain. The band to band tunneling effect gives the FinFET design a new scaling component. This serves as the method through which this FinFET architecture operates. By overlapping the area of the gate as well as drain and contributing to the high channel doping, the e-h pair produced by a quantum to quantum tunnel effect. [37]

1.5.3 Surface scattering: Surface mobility changes from being independent of the electric field to being more longitudinally dependent as the channel length is reduced. Within the restricted inversion layer of a MOSFET, the carrier transport is contained.

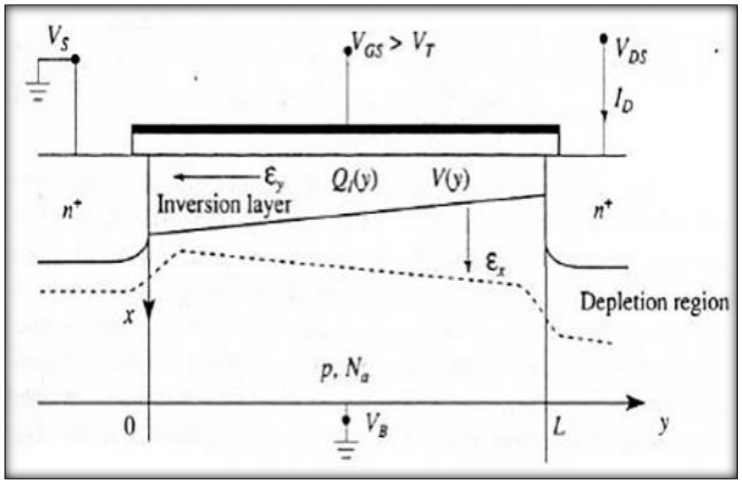


Fig. 1.10 Surface Scattering Phenomenon in FINFET [28]

Reduced mobility is a result of surface scattering. Moving parallel to the contact is challenging for the electrons. This is necessary to ensure mean surface mobility is almost equal to average bulk mobility. Electrons that are propelled toward the interface collide with objects, causing surface scattering. [28]

1.5.4 Velocity saturation: Trans conductance in saturation state is decreased by velocity saturation. The maximum carrier velocity, or saturation velocity, is reached in the existence of a high electric field.

The transistor enters a state referred to as velocity saturation when this happens. The increasing rate of extremely energetic electron scattering, mostly brought on by optical phonon emission, results in velocity saturation, which lengthens the time that carriers must travel along the channel. [29]

1.5.5 Impact ionization: This typically happens as a result of the high electron velocities present in strong longitudinal fields, which can cause impact ionization to produce electron hole pairs. The impact upon silicon and also the ionization of a electron hole pairs results in impact ionization. As a rule, the drain attracts the majority of the electrons; the parasitic substrate power

is created whenever the holes enter the substrate. An N-P-N transistor's base can also function in the space among the source and drain. [30] The source is as same as the emitter, while the drain is as same as the collector.

The usual reverse biasing substrate to the source of P-N junction could conduct if the source collects the holes and the resulting hole current results in a voltage drop of around.6V in a substrate material. Then, in a manner similar to how electrons are injected from an emitter to a base, the substrate can receive electrons from emitter. They can gather adequate energy as they go in the direction of drain to form novel electron hole pairs. If a few of the electrons generated by powerful fields transverse, the situation might deteriorate further, the drain field and enter the substrate, damaging other chipset components. [31]

1.5.6 Hot electron effect: This phenomenon happens whenever electrons or holes inside a semiconductor device acquire a lot of kinetic energy as a result of a strong electric field. Due to their higher initial mobility, hot electrons are more likely than hot holes. Hot carrier Effects are caused by hot carriers that are introduced or trapped in specific regions and lead to unfavorable device behavior and degradation. [32] The electric field of a channel gets stronger as the gadgets' sizes get smaller. As a result, a significant portion of the channel length is taken up by the high field zone close to the drain terminal.

The hot electron effect results from this, which over time causes the device parameters to degrade. While the device is being scaled down, this impact produces impediments. Peak currents are greater in FinFETs due to higher drive current and device densities. Because of this, the voltage drop on a big SoC depends on the package resonance and the resistance of the power grid. (L), described as identical to IR + L (di/dt), becomes extremely important. Hot electrons play a crucial role in the operation circumstances of hot electron effect premised over FinFET. The creation of hot electrons cannot be stopped because they are constantly available during regular functioning.

The primary cause of the hot electron phenomenon is the intensity of a strong electric field present in channel sector as a result of the systems enlarging size. The gate oxide may degrade as a result.A 100 mV decrease represents about 10% of the supply for planar transistors running at a 1V supply. When a FinFET working voltage is lower, the same 100mV drop represents a considerably larger portion of the supply voltage.

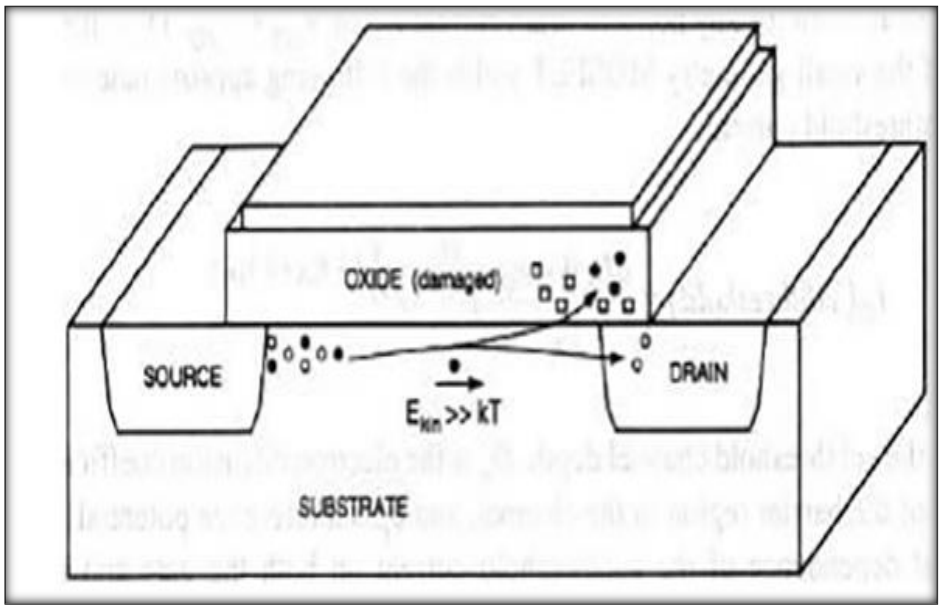


Fig. 1.11 Hot Electron Effect in FINFET [33]

As a result, the chip's operational headroom and noise tolerance are reduced, and for power noise evaluation, higher accuracy standards are required. These requirements include more reliability in power grid extraction, modeling switching currents while taking package/PCB impedance into consideration.

In addition to advantages FinFET provide, Elevated temperatures and issues with electro migration (EM) are caused by the smaller connection sizes, smaller connections, and higher power densities and voltage. Due to EM limitations, designers are that are introduced or trapped in specific region, s substantially more constrained in terms of device dimensions and via/wire routing.

Thermal effects such as self-heating are caused by the elevated FinFET temperatures. The predicted lifetime of electronics and metal layers typically degrades 3X to 5X for every 25°C raise in temperature. It is crucial to consider the outcomes of a precise thermal analysis in order to find real EM weaknesses in a design. The mean time to failure decreases as temperature increases. This necessitates tight coordination along a foundry as well as satisfying its "sign-off" credential criteria having complicated regulations of EM for enhanced process nodes.[33]

1.6 FinFET Design and Analysis:

The FinFET device's construction includes a silicon fin. Both of the substrate's edges of a silicon insulator are located of this silicon fin. This gadget typically has two gates that can be activated individually. The FinFET can be configured in a variety of ways, as illustrated in Figure 1.12

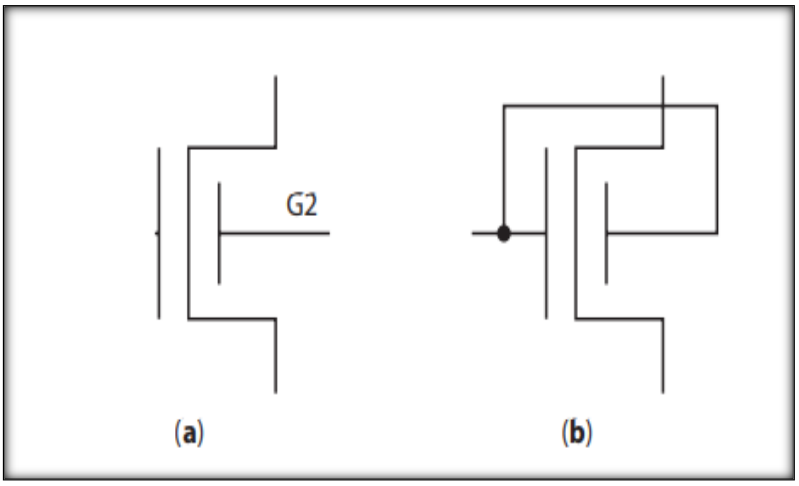


Fig. 1.12 (a) IG FinFET Symbol (b) Shorted Gate

This characteristic would change V_{gs} in an n-type FinFET device. Therefore, swing deterioration as well as drain-induced barrier was reduced in single-gate state in FinFET devices compared to double-gate state. The device's effective electrical width is determined by the height of the fins. Variations in device width are directly related to variations in fin height. The proportion of deviation in device width will be the same for all fin-based devices.

To meet or excel the efficient width of the FinFET device, fins must be extremely tall in size. Fin width control is poor whereas if the chosen fin's diameter is minimal then the range of flexible optical lithography also decreases. Additionally, the process's line edge roughness (LER) causes a significant amount of local fin width variation (LWR).[34] With more fin-thickness, the threshold voltage decreases.

Along with the capacitive coupling among gate as well as channel area, the surface potential for shorter channel lengths is also influenced by the resistance at the drain/fin and source/fin junctions. With enhanced fin thickness, the drain/fin and source/fin junction impedances decrease as breadth of drain/fin and source/fin depletion zones enhances. Whenever a finding, as the film thickness grows, the threshold voltage getting low as a result of an enhancement in gate to surface prospective coupling.

Threshold voltage's impact is minimized with greater fin thickness. The origin and drain resistivity at the junction across the lowering the length of the channel, the capacitive coupling between the gate and channel area, and the surface potential all have an impact. As the breadth of a source and drain/depletion area expands with an increment in fin thickness, the capacitance at a source and drain junction drop. Therefore, it is noted that an increase in fin thickness corresponds to a rise in voltage drop, leading to an augmented coupling between the gate and surface potential.

In the comparison of FinFET and Bulk CMOS at lower supply voltages, the I_{ON}/I_{OFF} ratio favors the former, whereas at higher supply voltages, the latter exhibits a larger I_{ON}/I_{OFF} ratio. As a result, the I_{OFF} of the bulk CMOS is lower than that of the FinFET, and the I_{ON} of the FinFET is higher than that of the bulk CMOS. To undertake device optimization and help engineers who integrate devices and processes, a TCAD tool is required. In order to evaluate the transistor's random variation efficiency employing noise-like resistivity domain approach using 3-D gadget TCAD simulations, FinFET or Tri-gate transistors below the 20nm technology node must make heavy use of 3D TCAD simulations.[35]

SCE is principally caused by the drain induced barrier lowering (DIBL) consequence, that decreases the edge voltage because channel length decreases. The SOI gadget, however, SCE is affected by thin film thickness, thin film doping thickness, and substrate biasing, as well as covering oxide thickness. SCE is brought on by parasitic electric forces out from source and drain areas, that finally have an impact on the drain current.

It is anticipated that with a MOSFET, the gate will ultimately have control over the channel, hence regulating the drain current. SCE, in which the length of channel is within the sequence of a source and drains sections, originates from gate not having total management over the channel. In a FinFET, the gate completely controls the channel because it surrounds it like a fin In terms of performance metrics; FinFET and bulk MOSFET are compared in Table 1.1. [36]

Table 1.1: Comparative study of MOSFET and FinFET.

Parameter Name	Bulk MOSFET	FinFET
SCE	In this case, gate has complete control over the channel.	A gate surrounds the channel on all sides.
Quantum Tunneling	More power is used, while less channel doping	Low power consumption and high channel doping
Hot Electron Effect	Electrons won't get accelerated in this channel	The operational circumstances include electrons as a fundamental component.

1.7 Applications of FinFET:

Low-Power Applications:

In CMOS-based electronic circuit architecture for reduced implementations, the inclusion of FinFET as a possible replacement for conventional MOSFET. With nFinFET and pFinFET in place of traditional MOSFETs, a variety of digital uses could be achieved. TCAD is also useful for the design and evaluation of CMOS-based implementations that use more sophisticated FETs, such as FinFET.[37]

FinFET-Based Digital Circuit Design:

In CMOS VLSI circuit design, the FinFET can take the place of conventional n-MOSFET and p-MOSFET.

It makes it simple to construct a variety of mixtures and sequential circuit implementations for reduced and fast processes. [38]

FinFET-Based Memory Design:

To extend battery life, smart gadgets require huge memories containing SRAM and DRAM cells which employ minimal power. For a smart device such as a laptop, a phone, and various portables and wearables, the layout of SRAM cell featuring 7nm innovation node created is practical. [39]

FinFET-Based Biosensors:

Similar to existing DGMSFET-based biosensors, FinFET may be employed for bio-medical purposes by incorporating a nano gap cavity sector behind sided gate. The newly inserted cavity region exhibits a significant shift in the device's electrical properties due to the dielectric modulation caused by variations in the presence of bio-species. To find out if a biomolecule is present, these alterations can be quantified and observed.

A biosensor built on a GaAs FinFET was suggested, with a cavity region between the source drain and gate regions. It was demonstrated that an enhancement in the cavity region's dielectric constant enhances the surface current in the ON state. Changes in the bio-species existing in the cavity [40] zone affect the dielectric constant's value.

The FinFET transistor architecture has the potential to revitalize the chip market. It would do this by lessening the impact of short channels. About 25 years ago, in the late 1980s, multi-gate MOSFET research began. Hieda et al. suggested the first multi-gate transistor in 1987. Designers learned from it that a silicon-based transistor's entirely depleted body helps enhance switching since the body bias effect is reduced. In the following two years, Hisamoto et al. successfully demonstrated DELTA, a prototype FinFET in bulk silicon. A team from the University of

California, Berkeley, lead by Dr. Chenming Hu, suggested a novel transistor construction in 2004[15] that would lessen leakage current. The Berkeley investigators suggested that by maintaining the gate impedance nearer to the entire channel, a thin-body MOSFET construction would manage SCE and minimize leakage.[4] Some studies have evaluated how the sources of variability affect the device's I_{OFF} and I_{ON} currents as well as how they affect the threshold voltage.

Random distribution of dopants (RDD) is a primary reason for flexibility in bulk CMOS technology, according to Gold Standard Simulations (GSS) Limited [13]. However, RDD's contribution to FinFET innovation has been drastically decreased as a result of the minimal channel doping. Additionally, FinFETs need to take into account the effects of flaws such as LER and GER.

Metal Gate Granularity (MGG) has been identified using greater metal gates as the primary driver of statistical variability in node 45nm innovation. Due to the metal's polycrystalline form, the surface voltage has experienced working function fluctuations (WFF) due to disturbances that are locally created. WFF is formed in the form its granules are arranged, in accordance with the relying of the metal gate [14].The gates produced during the optimal manufacturing period for metal entrance hardware feature new metal which is equally distributed and has little variance in functional capacity.

However, in actual production, metal gate devices are typically supplied via metals with a variety of hastily fitted blades, indicating greater W_{FIN} variability. It is determined that variations in restricted voltage caused by the granularity of the metal entrance are closer to Gaussian distribution and that standard deviation directly correlates to the diameter of the metal grains.

Despite the edge voltage, the strong WFIN influence is seen in the recent investigations, particularly in the fluxes of I_{ON} and I_{OFF} [41]

1.8 Physical Models:

The actual methods of every substance are stacked together in Genius' actual model interface next to the replica structure (PMI). The approaches may be considered using PMI order. Additionally established here are model borders.

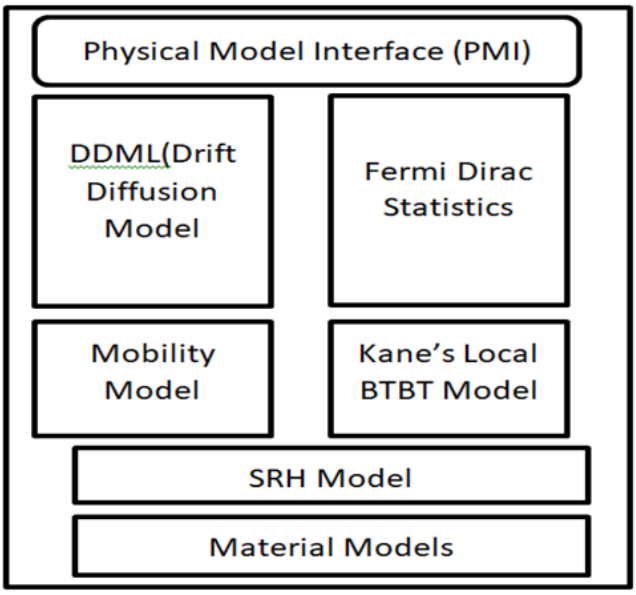


Fig. 1.13 Physical Models

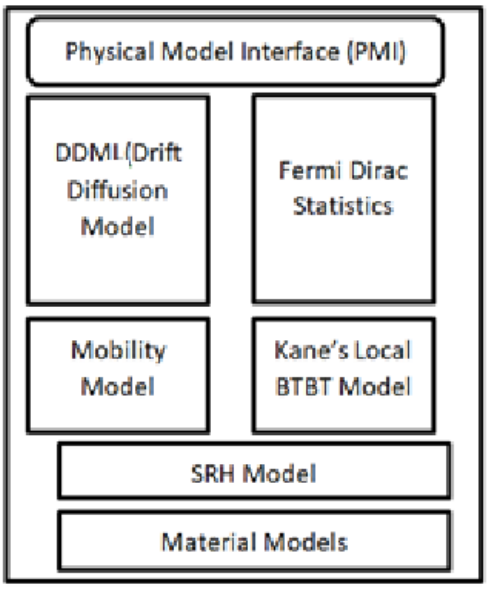


Fig. 1.14 Fabrication process

With the Physical Model Interface (PMI), Genius' main program will be able to access the numerous material-explicit models. In Genius, every supported file contains corresponding dynamic loadable library (DLL) entry located within $(GENIUS DIR)/lib/index directory. Every DLL record includes every model relevant to that data.

A default model lacking a PMI order will be laid for each type of model. In the event that the customer submits at least one PMI order, Genius would sequentially stack specified illustrated and assign it to the predefined region. An alternative is for the customer to give the PMI model a list of their own unique mathematical and string boundaries. As an illustration, the bounds of the snare design will be organized and stacked in the future commands for the Silicon location. The PMI order may be employed to modify each model's unique bunch bounds. In "Versatility Models," each portability model's representation and the limits of comparison are clear.

1.9 Scaling limits of TG FinFET structure: Figure 1.15 depicts the impact of the effectiveness of the gate-length to the fin thickness ratio (L_{eff}/T_{fin}). With a falling ratio (L_{eff}/T_{fin})., DIBL and subthreshold swing (SS) rise. For the same SCEs, this ratio can be decreased to less than 1.5, unlike DG FinFET.

The SCEs may exceed allowable limits when this ratio gets closer to 1. The TG FinFET architecture has greater scaling possibilities than DG FinFET structure, for this reason.

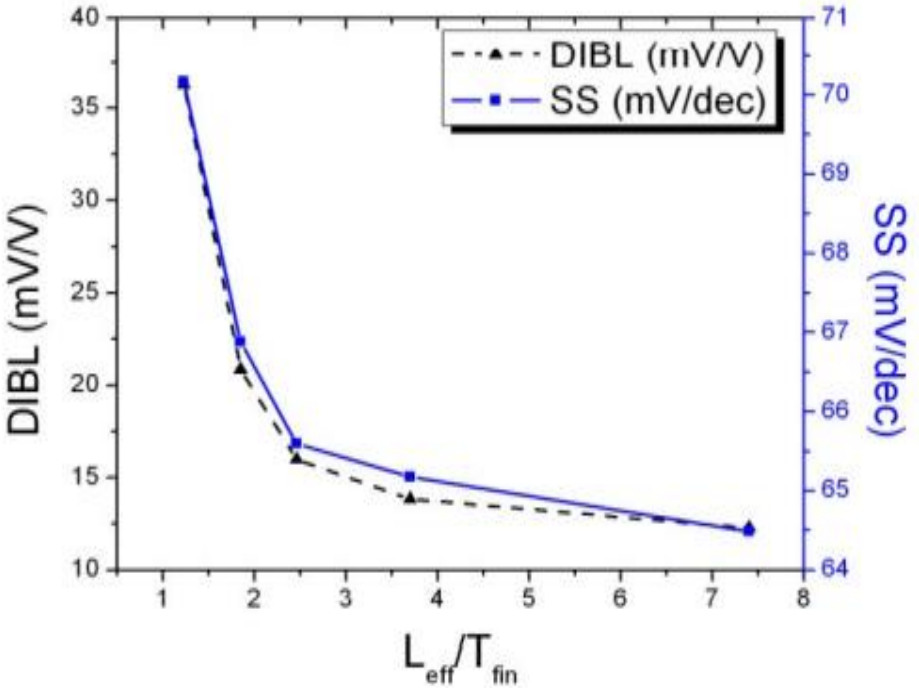


Fig 1.15 Effects of (L_{eff}/T_{fin}) ratio variation on SCEs at 30nm of H_{fin} [42]

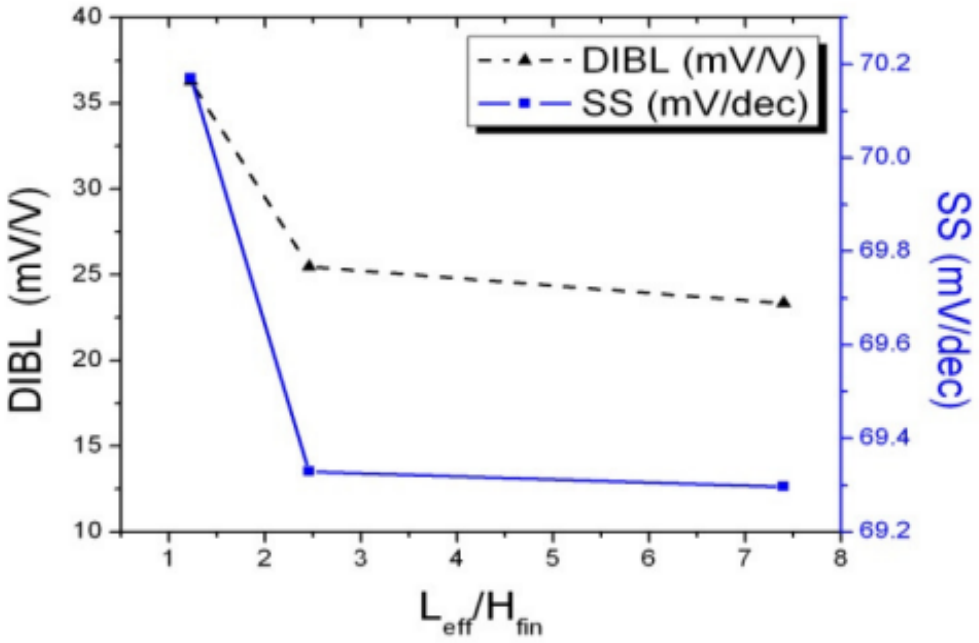


Fig 1.16 Effects of (L_{eff}/H_{fin}) ratio variation on SCEs at 30nm of T_{fin} [42]

Fig.2.7 displays the impact of the effective gate length to fin height ratio upon SCEs. While DIBL and subthreshold swing (SS) rise as the ratio (L_{eff}/T_{fin}). falls, the increase is less than it is for the ratio (H_{eff}/T_{fin}).). This is because fin thickness, as opposed to fin-height, is highly susceptible to SCEs. It is possible to raise fin height while maintaining an acceptable SCE value to obtain more on-current than fin thickness.[43]

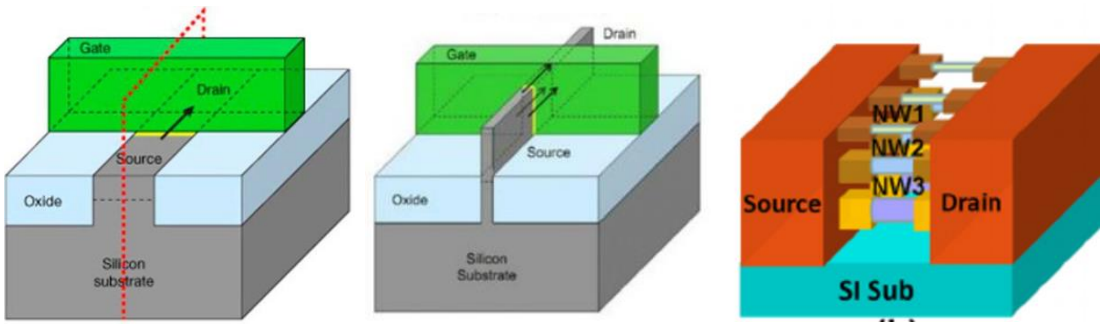
1.10 Chapter Conclusion: This chapter concludes that the field-effect transistor technology is the major contribution in developing the modern electronics industry. This technology reduces the short channel effects that promote the continuous upgradation in the FinFET technology. Also this chapter deals about the different types of FinFETs depending on the applications. It focuses on the emerging history of FinFETs and current technology of fin structure, also briefed about the challenges and issues in the technology. Physical models and fabrication process to develop FinFET are clearly explained. And finally applications and the scaling limits of triple gate FinFET structure. The collated understanding of the FinFET device with respect the bulk and SOI MOSFET has been carried out by exploring the various FinFET structures is considered. To understand the different methodologies and applications of FinFETs, literature survey has done in the next chapter.

CHAPTER 2: LITERATURE REVIEW AND METHODOLOGY

2.1 Introduction: Fin engineering is crucial for balancing the altitude of fin, fin and oxide thickness, and various channel lengths are in need to reduce I_{OFF} leakage current and increase I_{ON} current in electronic systems. The source and drain regions are linked to the ends of the vertical silicon fins which make up the channel region in FinFET structures. This vertical fin is surrounded by the gate area. MOS channels have been constructed along the circuit's two sides and on the peak surface of the fin. By building the MOS channel on the surface of a fin wafer rather than in a wafer beneath the gate, the effects of a short channel in the FinFET are avoided.

Additional electrostatic control over the charge carriers exists since the gate is positioned along the channel region. In compared to planar devices, the height of the fin shows a higher current drive per each unit area for the FinFETs. The number of fins in a FinFET transistor is inversely correlated with the current density. Since substantial doping is not necessary in these FinFET, their susceptibility to RDD variations is reduced. [44]

A silicon oxide film's equivalent oxide thickness, which is often expressed in nano meters (nm), is the thickness at which it offers the identical electrical efficiency as the currently being utilized high-performance material. The phrase is frequently used to refer to field effect a transistor that depends on a material pad that acts as an electrical insulator among a gate and a doped semiconducting area. It has been common practice to increase device performance through insulating pad thickness reduction in silicon oxide. Leakage current remained a concern as the insulating pad's thickness neared 5–10 nm, necessitating the use of alternative materials. These novel materials had a reduced equivalent oxide thickness, which allowed them to maintain the required gate oxide thickness to reduce leakage current all while accelerating switching. For instance, a material ten times thicker than silicon oxide with a dielectric constant of 39 (as opposed to 3.9 for silicon oxide) might achieve the same capacitance and good performance while reducing the amount of electron leakage across the dielectric pad[45]. To put it another way, to get equivalent performance while taking into consideration leakage current, a SiO_2 film with a texture one-tenth that of the greater might be required. For gate-all- around devices, hafnium oxide and, more recently, Aluminium oxide are two commonly utilized high-gate dielectrics.[45]



Planar FET **FinFET** **GAAFET**

Fig 2.1 Different FinFET Structures

2.2 Future FinFETs: RFID (radio frequency identification) as well as IoT (internet of things) systems are among the applications for which the FinFET-based adders are built. If they could be integrated at the server and device ends, artificial intelligence (AI) and the Internet of Things (IoT) can offer advantages and possible prospects. IoT is now integrated with growing AI technology, which aids businesses in making intelligent judgments and avoiding any human interaction. In order to address manufacturing-related challenges, the field of semiconductor devices has recently focused on ML (machine learning) applications. [46]

As an illustration, ML is used to forecast the variability process, estimate the error rate of software, and anticipate the place of the damaged bridge in FinFET. The overall ionizing dosage of this trap refers to its effect on dielectric areas. However, even though the majority of current work concentrates on the impact of displacement damage, this does not necessarily imply that displacement destruction is more substantial than the overall ionizing dose.

Additionally, the impact of the overall ionizing dosage is equally essential, and ML approaches can be used to estimate the impact of a single trap. In line with this development, machine learning (ML) was used for research because this can be used to faithfully reproduce point defect FinFET TCAD information. V_{dd} is lowered while employing a reduced innovation node, which can reduce dissipation and boost circuit speed. It may be inferred from the simulated findings using the 7nm FinFET innovation node which FinFET-relied adders of 7nm provide adders employing alternative innovation nodes better speed and reduced consumption of power. In portable gadgets where there is a limited budget for power and speed usage, this given adder circuit was employed.

As a result, it is crucial for researching the circuits that use FinFET devices in ultra-low power applications. DRAM (dynamic random access memory) specifications are becoming more and more in demand due to block chain, AI & ML, and automotive generations.[46]

2.3 Existing FinFETs:

Kumar H., Jethwa M.K., Porwal A., Dhavse R., Devre H.M., Parekh R [47]: This paper focused on the impact of channel composition on different performance characteristics of FinFET. Channel materials such as semiconductors like Germanium (Ge), Indium Nitride (GaN), and Silicon (Si) have utilized by them in designing process. The impact of the multiple channel materials on different indicators, such as temperature, drain-induced barrier lowering (DIBL), trans conductance (g_m), threshold voltage (V_{th}), and Subthreshold swing (SS) are analyzed.

Anuj Chhabraa, Ajay Kumarb, Rishu Chaujara [48]: This study introduces a novel FinFET structure based on GaAs that performs better than existing FinFET structures. Here, for the first time, a thorough examination of device features is investigated along with a stress evaluation of the suggested device structure. In addition, the relationship between linearity and stress effect is examined. Observations indicate that adding stress to FinFET enhanced device efficiency (TGF) to 49.36%, intrinsic gain (Av) to 17.23%, and I_{ON} to 159.2%, all of which are particularly advantageous for reduced power applications.

Mahmood Uddin Mohammed, Athiya Nizam, Liaquat Ali, Masud H. Chowdhury: This work mainly explaining that how the number of transistors has expanded exponentially that increases the usage of the power of the contemporary digital system. Additionally, at least a technology node, the SCEs causes the operation of traditional CMOS devices to decline. To assess process changes and ascertain the resilience of SRAM designs, Monte Carlo simulations are run on the SRAM cells. Using 7 nm innovation, simulations were performed in HSPICE.

Kusuma, Rambabu, and VK Hanumantha Rao Talari.[50]: This paper considered the different oxides such as SiO_2, HfO_2 and Si_3N_4 that were used in the design and analysis of FinFETs to achieve higher I_{ON}/I_{OFF} ratios and smaller leakage currents than traditional FinFETs. HfO_2 and Si_3N_4 have shown remarkable performance out of all setups. In three dimensional (3D) simulations utilizing Visual TCAD, the drift-diffusion approach and quantum approaches are also employed.

R. Kumar, S. L. Tripathi and M. Singh Adhikari [51]: This paper is focused to obtain improved subthreshold performance in DG-MOSFET that are built with distinct gate overlaps or under-lap zones in both symmetric and asymmetric topologies.
On a Visually TCAD 2D and 3D circuit simulator, the suggested DG-MOSFET is constructed and studied.

Y. T. Roh and H. C. Lee [52]: This paper is detailed that, when compared to conventional Bulk devices, the FinFET technology provides a non-doped channel with enhanced DIBL and well-managed access resistances. It has been established for global variability, which is unaffected by the SOI film thickness.

Kumar, S., Yadav, D. S., Saraswat, S., Parmar, N., Sharma, R., & Kumar, A[53]: This paper focused on In-depth analysis of the devices' transfer properties, employing DC and analog/RF characteristics, it was possible to calculate the (g_m), trans conductance generation factor (TGF), (g_{ds}), cutoff frequency and parasitic capacitance (C_{gd}, C_{gs}). By creating a high potential there at source/channel interface that reduced HCEs, DIBL and SCEs and boosted drain current, the trans conductance of the described device was enhanced. Reduced power dissipation is the outcome of the suggested device's extremely low parasitic capacitance.

Bhattacharya, S., Tripathi, S. L., & Kamboj, V. K [54]: In this work, the tunnel field effect transistor is offered as a potent low-power substitute for the MOSFET. The main drawbacks of TFET circuits, like lowering the ON-positioned current and a lesser I_{ON}/I_{OFF} ratio, are resolved by changes to the material and architectural composition. The device is four times optimized to produce the ideal shape and size, and it is found to deliver outstanding results with less power consumption.

Li, Chao-Chieh, Min-Shueh Yuan, Chia-Chun Liao, Chih-Hsien Chang, Yu-Tso Lin, Tsung-Hsien Tsai, Tien-Chien Huang [55]: This paper has introduced **a** new technique was used to make up for tracking-bank resolution so that it could retain their quantization noise stage across such huge TR. In a fractional-N ADPLL operation, a new method is used to solve the meta stability resolution problem. This topology has a less area of 0.034mm^2, broad TR of 56.5% and appreciable noise rejection of 1.8%/V, which results in FOMs with normalized TR and area (FOM TA) of -262dB and -247dB, respectively.

S. Sai, S., Alivelu Manga, N., & Sekhar, P.C. **[56]:** In this study, 45nm CMOS as well as 22nm FinFET innovation are used to develop and simulate combinational circuits such encoders, decoders, and Johnson ring counters. According to the simulation findings, when an encoder, decoder, or Johnson counter was developed using 22nm FinFET innovation, the power dissipation fell by approximately 93%, 89%, and 95%, respectively. The delay is also lessened. In 45nm CMOS as well as 22nm FinFET technologies, combinational circuits such encoders, decoders, and Johnson ring counters are built and simulated.

Lee, In-Geun, Hyeon-Bhin Jo, Ji-Min Baek, Sang-Tae Lee, Su-Min Choi, Hyo-Jin Kim, Wan-Soo Park [57]: In order to study the effects of scale upon fin-width (W_{fin}) and equivalent oxide thickness (EOT)at gate lengths less than 100 nm, the author created TG sub-100 nm In0.53Ga0.47As MOSFETs using a bi-layer Al_2O_3/HfO_2 gate stacking. For In0.53Ga0.47As tri-gate MOSFETs having a 60 nm length of gate of, EOT and W_{fin} scaling were successful in enhancing electrostatic immunity such SS and DIBL. When comparing to InGaAs MOSFETs planar with the EOT as well as identical gate stack, In0.53Ga0.47As Tri-Gate MOSFET reliability characterization shows a somewhat poorer VT degradation at 300K. This is a result of the sidewall contacts at both ends of the etched fin.

L. H. Brendler, A. L. Zimpeck[58] ; This work gives **t**he effectiveness of logic cells is influenced by the transistor configuration. In order to reduce space, delay, and power, complicated logic cells may be used. However, given the growing importance of nanoscale problems like process variability as well as radiation damage, it is also vital to take these things into account while designing logic levels. It is explained why the parameter which may define process variability was selected. Additionally, the analysis is performed using various transistor layouts and sizes to offer a foundation for a better comprehension of the outcomes. The experimental analysis takes into account two topologies for the number of logic gates implemented at the design phase in 7nm FinFET innovation: complicated gates as well as multi-phase employing fundamental gates. As expected, the optimum option for optimizing size, power usage, and performance under nominal conditions is to use complex gate architecture. The logic at multi-level structures made the functions at least 30% more resistant to the impacts of process variability and up to 50% lesser sensitive to transient failures. It is necessary to make a trade-off in light ofthe space and power limitations.

Srinivas, P.S.T.N., Kumar, A. and Tiwari, P.K[59]: This study provides a description of a TG Schottky-Barrier (TGSB) MOSFET's cutoff voltage by linking designs of symmetric as electrostatic potentials of DG-SB MOSFETs were determined. The middle of the bottom of the well as asymmetric double-gate SB MOSFET topologies, with weights assigned to each structure. considering light doping with in channel area and evanescent mode evaluation, the transition region is where the leakiest path in TGSB MOSFETs is found during the subthreshold domain of device operation. The virtual cathode potential, that is employed to determine the SB MOS devices' threshold voltage, is thought to represent the lowest potential method.

Vimala, P., and T. S. Arun Samuel [60] : This paper provides Trigate FinFET devices with various architectures than SMG as well as DMG FinFET system architectures in regard to electrical characteristics including Single Material Gate (SMG) FinFET, Double Material Gate (DMG), and Triple Material Gate (TMG) FinFET, have undergone a thorough comparative performance analysis. characteristics including buried oxide (BOX) thickness, Oxide thickness, doping concentration, The numerical simulation findings from Sentaurus TCAD's 3-D system simulator were employed to verify findings of the suggested (TCAD) software. According to simulation outcomes, TMG system architecture perform better characteristics are described using the Silvaco Atlas Technology Computer-Aided Design including electric field, surface potential, as well as drain current. In addition, the TMG FinFET circuit architecture has superior transconductance of 0.28 A/V in comparison to 0.21 μA/V, 0.24 μA/V of SMG and DMG FinFET.

Suman Lata Tripathi and Shobith Saxena[61]: This paper detailed that because of increased leakage current as well as constant power utilization per semiconductor unit area under 20nm technological node, transistor miniaturisation places thermal restrictions on MOSFET architectures. The scope of future scaling trends is increased by the ability for tunnel FET to decrease static consumption of power to build beneath 20nm innocation while maintaining thermal constraints. It is suggested to develop an unsymmetrical Ge-$Si_{0.7}Ge_{0.3}$ hetero type junction tunnel FET having varied oxide thicknesses on the origin and drain sides. Due of the comparable lattice structures of Ge and Si, the suggested device may be easily manufactured. Pt/HfO_2 serves as the gate contacting material, and the gate has a 15 nm gate length, an I_{ON}/I_{OFF} ratio larger than 108 is attained in nHTFETs. The same method also results in a reduction of the parasitic BJT effect in the OFF state circumstance.

Jino Ramson, S. R., Jackuline Moni, D., Alfred Kirubaraj, A., & Senith, S. [62]: This paper designed a DG based n-FinFET as well as modeled at 22nm and 20nm innovation. In double gate nFinFET, the various gate metals of Aluminum, Molybdenum and Gold of dielectric thickness 1nm were used. By using the hafnium oxide which possess the maximum k dielectric constant as the gate dielectric to reduce the leakage current and can improve the performance of the device. It is shown that integrationof Gold gate metal and hafnium oxide has a maximal I_{ON} /I_{OFF} ratio than the Aluminum. So it improves the device performance.

A. Kumar and J. N. Roy[63]: This paper mainly focused on electrical characteristics of nanoscale devices such as DG and TG FETs up to channel length of 10nm. The simulation tool used is Cogenda Visual T CAD tool and observed the effects of variation in the device parameters with and without Quantum Mechanical Effect.

D. Gola, B. Singh and P. K. Tiwari [64]: This work provides the Conduction path potential, current, thresholdvoltage, and DIBL, swing along with substrate bias as well as SISP impacts, were used to derive the sub threshold domain framework. Cogenda Visual T CAD software serves as the 3Dsimulator. It has been discovered that substrate bias and SISP effect could be used as additional parameters to adjust the subthreshold current as well as SCEs in TG-MOSFET.

F. Forero, H. Villacorta, M. Renovell and V. Champac [65] : This study examines entire open gate faults' electrical behavior. It is established that the traditional models, referred to as interconnect open (IO), andsingle open (SO) which were previously put forth for CMOS innovation, are insufficient for FinFET innovation. New specialized defect topologies known as "subset full open gate defect" are produced by current FinFET-relied logic cells utilizing multi finger and multi-fin layout approaches.

W. You, P. Su and C. Hu [66]: This study evaluated the functionality of VLSI subsystem- level logical circuits relying on metal electric insulator–semiconductor (MFIS) negative- capacitance FinFETs (NC-FinFETs). They have compared the functionality of logic circuits using 14nm ULP NC-FinFETs vs. FinFETs in terms of standby-power, switching-energy, and latency using a short-channel NC-FinFET little design.

Mishra, Subrat, Hussam Amrouch, Jerin Joe, Chetan K. Dabhi, Karansingh Thakor, Yogesh S. Chauhan, Joerg Henkel, and Souvik Mahapatra [67].*:* This paper mainly focusses on the influence of negatively biased temperature instability (NBTI) on the functionality and the built in power of the digitally logical circuits using the 14nm

technology node FinFET innovation is evaluated in this research using a thorough simulation approach. The older type and newer type device properties are determined using fully calibrated computer-aided design simulations. Timing deterioration of several benchmark circuits is created, examined, and contrasted with ring oscillator findings.

Convertino, Clarissa, Cezar Zota, Saurabh Sant, Felix Eltes, Marilyne Sousa, Daniele Caimi, Andreas Schenk, and Lukas Czornomaz [68]: This study demonstrates that the use of digital etching to incorporate source-drain sidewalls spacer together with doped elongation is what causes the strong off-state performance. The outcomes show that further reducing the gate length as well as fin width could increase the coming performance.

Rashed, Mahbub, Shibly Ahmed, Navneet Jain, Juhan Kim, Sushama Davar, Pala Balasubramaniam, James Blatchford, Ravi Todi [69]: This research shows that multi-dimensional discovery and trade-off analysis at an early stage of technology development call for a deeper comprehension of the procedures, lithography, device, digital, analogue, and memory design restrictions, in addition to application- and system-level implications.

Beckers A, Jazaeri F, Enz C. [70]: This study examines a commercial 28-nm bulk CMOS technique that operates at cryogenic temperatures through experimental inquiry, compact modeling, and reduced physics-based modeling. To get a set of analytical formulas for the electrostatic profiles and the texture of the freeze-out phase, a new body-partitioning techniqueis presented.

Chetanchugh, Vishal Narula, Suman LataTripathi, Balwinder Raj [71] : In this article, the variability of several parameters, including I_{ON}/I_{OFF}, Sub threshold slope, and DIBL, is examined in relation to changes in gate length. The leakage current parameter, therefore, becomes substantial as we approach a gate length of 12nm and will be no longer disregarded going forward. This effort would provide a chance to further investigate the mesh spacing parameters and gate work function modifications in order to improve the device's properties at ever-shorter gate lengths.

R. R. Thakur, P. Singh, S. S. Kiran and A. K. Singh [72]: This study presents the optimization of a cutting-edge 22nm FinFET transistor innovation for its use in diverse semiconductor systems and applications. When compared to the usual, the device's short channel effects were discovered tobe significantly suppressed.

Due to the positive results obtained for the SS and DIBL, the impacts of drain bias upon that device's functionality and durability under high drain bias are also being examined.

Paliwoda, Peter, Prashanth P. Manik, Dhruv Singh, Zakariae Chbili, Andreas Kerber, Jeffrey Johnson, and Durgamadhab Misra [73]: This work provides the three alternative measuring approaches are described in this study to FinFET electrical characterization self-heating at the wafer layer.

Results are validated and heater-sensor temperature gradients are interpreted using heat transport finite component simulations. The various sensor kinds are created to employ system gate resistance (RG) itself, the adjacent pn-junction forward bias ,or threshold voltage (V_{th}) of a neighboring FET. According to the report, self-heating is 35% understated when detected at a nearby device.

Gong, Huiqi, Kai Ni, En Xia Zhang, Andrew L. Sternberg, John A. Kozub, Kaitlyn L. Ryder, Ryan F. Keller [74]: The single-event transient behavior of InGaAs FinFETs having various finwidths is investigated in this article utilizing pulsed laser and heavy ion irradiation. In both settings, gadgets with wider fins gather more charge. The sensitive volume is determined by quantum-well architectures, which restrict charge absorption in the channel. According to simulations, devices with varying fin widths produce a similar amount of charge when exposed to radiation, but wider fin devices gather more charge due to their greater channel volumes.

Yanambaka, V. P., Mohanty, S. P., & Kougianos, E. [75] : In the context of nanoscale technology, this research suggests that FinFETs offer attractive alternatives to bulk CMOS. A contrast among a CMOS VCO as well as FinFET relied VCO is offered, along with an analysis of design difficulties. The FinFET technology was examined in this research with regard to handle variance in mixed signal layouts there at the circuit level, and a qualitative and numerical comparison between CMOS and FinFET techniques is presented.

S. Mangesh, P. K. Chopra and K. K. Sain [76]: In this study, we simulate the charge carrier quantum confinement in the SOI FINFET device. Under strong inversion conditions, the quantum corrected drift-diffusion models and the classical drift-diffusion method are compared to examine quantum confinement effect in device. According to the simulation results, short channel SOI MOSFET performance is not affected by quantum confinement or mobility deterioration. Leakage status has actually changed for the better.

A. M. Bughio, and S. Donati Guerrieri [77]: This article addresses the variability of such a new mixer topology by utilizing the recently discovered effective physics-based sensitivity evaluation of FinFETs with in IG configuration. This underlines once more how very desirable IG mixers are for RF applications. Utilizing the unusual structure of the multi-fin IG FinFET, novel architectures for balancing or double-balanced mixers might also be constructed.

2.4 Biosensor FinFETs: FET biosensors (Bio-FET) for biological applications have advanced in recent years due to changes in FET properties and alterations to the architectures of bio- receptors. This review's analysis and summary of noteworthy works on the two aforementioned features first offers reflection on this advancement. The former involves creating innovative materials for FET transducers and creating unheard-of nanostructures, while the latter focuses mostly on creating condensed molecules as bio-probes. Then, based on the present circumstances as well as the high demand for Bio-FET in clinical trials for illness detection, a future viewpoint on FET-biosensor research is also forecasted. From these angles, it is anticipated that Bio-FET which have countless advantages, would keep improving to become one of the foremost promising technologies for biological applications.

Indu Sarangadharan, Anil Kumar Pulikkathodi, Chia-Ho Chu, Yen-Wen Chen, AbiralRegmi, Pei-Chi Chen, Chen-Pin Hsu, and Yu-Lin Wang [78] study of the important FET sensor technologies enhanced for biosensing techniques. The author focuses in particular on examination of highly field gated Bio-FET enhanced for the direct identification of object analytics in physiological salt conditions and small test pre-treatments. Many biomedical techniques like Identification of nucleotides in buffer, identification of proteins in buffer, serum, and whole blood, whole cell- based sensor, and differentiation of living tissue are described in this analysis original research article. An integrated portable biosensor method implementation depends on a highly field gated Bio-FET that describes ability for medical techniques in point-of-care and home-care detections.

Rhiannan Forsyth, AnithaDevadoss ID and Owen J. Guy. [79] concentrating on explanation of latest implements in domain of bio affinity-based G-FET sensors, by which the binding the event in-between a bio-receptor and a target element is conveyed at the G-FET surface like an electrical signal. Exact as well as dependable identification and quantification of these target analytes are important in the diagnosis of several disorders, so the careful design of the G-FET is essential.

Considering a few restrictions of the sensor platform, like Debye-Huckel monitoring and system surface area, is basic in enhancing better bioelectronics for techniques in medical configuration.

Xiaofeng Gong, Rui Zhao, Xiaomei Yu [80] describes the development of multi-Silicon-Nano Wire FET (SiNW-FET) biosensors that can detect DNA and proteins with extreme sensitivity. The description involves the production of single, double, and quad-SiNW-FETs on a single chip using a basic top-down fabrication method. Differentiated from the single-SiNW-FET, multi-SiNW-FET biosensor exhibits a maximum capability to reduce noise by average currents of source-drain. The sensor was able to detect the norovirus DNA as well as IgG at concentrations under 1 fM and 10 fM, correspondingly.

Terse-Thakoor, Trupti, Sushmee Badhulika, and Ashok Mulchandani [81] discusses a silk fibroin-encapsulated G-FET enzyme-based biosensor that utilizes silk protein as that of the system substrate and a medium for immobilizing the enzyme. As glucose is oxidized by glucose oxidize immobilized on the silk fibroin film as in G-field effect transistor, conductance variation and Dirac point shift of the G transistor help identify glucose molecules. Due to the fibroin-encapsulated G-FET enzymatic biosensors being biocompatible, stretchable, and enduring constant, it maintains high attraction for compatible, wearable, and implantable interpreted glucose detecting techniques.

David J. Baek, Sung-Jin Choi, Jae-HyukAhn, Jee-Yeon Kim, and Yang-Kyu Choi [82] directs electrical detection of antibody and antigen binding of avian influenza virus demonstrated by a DG- Fin FET-derived biosensor. An easy identification technique is used in that the impact of charge from bio-molecules is monitored by a threshold voltage (VT) shift. It's distinctive model enables the channel to be insulated from noise from bio-molecules which is difficult for nano gap FET biosensors. The suggested deviceis CMOS compatible and the most reproducible and monolithic integration with readout circuits can be achieved.

Islam, Md Saiful, and Abbas Z. Kouzani [83] describes DNA recognition by using a double-gate field effect transistor (DGFET). Additionally, an examination of sensitivity and Signal to Noise Ratio (SNR) is performed for various outputs of analyte, buffer ion concentration, pH, stable reaction, etc. Sensitivity that is demonstrated by modification of drain current enhances non- linearity later, particular outcome (~1nM) of analyte concentrations and reduces non-linearity with buffer ion concentrations.

Anyhow, sensitivity is linearly connected to fluid gate voltage. SNR is developed with most analyte concentrations and receptor densities.

Ahn, Jae-Hyuk, Jee-Yeon Kim, Cheulhee Jung, Dong-Il Moon, Sung-Jin Choi, Chang-Hoon Kim, Kyung-Bok Lee, Hyun Gyu Park, and Yang-Kyu Choi. [84] This paper introduced a new biosensor relied on a standalone DG-Fin FET is presented during initial period. It consists of a Si-NW performed on bulk substrates, floating gate of charge detecting, and control over the gate for driving the current. The identification of charged polymers and Deoxyribonucleic Acid is to recognize of the breast cancer is presented in this paper.

Martens, K., Santermans, S., Gupta, M., Hellings, G., Wuytens, R., Du Bois [85]: This paper focusses on a crucial component for achieving single-molecule detection has been put into place, and a 36 mV statistical significant signal caused by PNA-DNA hybridization has also been seen. For a salinity of 1.5 mm and a DNA density of 8x1012 cm-2, this yields in identification of around 200 molecules for the shortest device size (131950 nm). Last but not least, it is expected that single-molecule identification for silicon FinFETs with sub-70 nm gate lengths in lower-alkalinity electrolyte conditions will be practical having SNR> 5.

Kashyap, M. P., Gudaghe, H., & Chaujar, R. [86] : This article offers a thorough analysis illustrating the di-electric type of modulated bio-sensors using the Truncated-Fin (TF) FinFET as the key element. Following the realization of the results' improvements, further research is carried out to determine the ideal design for TF-FinFET-based biosensors. The undesirable density of the charge that immobilizes the inner side of the cavity is therefore changed in real-time in order to compete with it from itself. The switching ratio and sensitivity of Truncated FinFET type of biosensors with longer cavity lengths were higher (Specifically, at a 100x and a 2x augmentation, correspondingly). By altering the charge density connected to biomolecules, different figures of merit are also compared. The label free characterization of TF-FinFET premised biosensor is developed with improved findings in regards of the capacity to identify the diseases by recognizing their relating biomolecules, rendering it a superior choice between its competitors.

Rigante, Sara, Paolo Livi, Alexandru Rusu, Yihui Chen, Antonios Bazigos, Andreas Hierlemann, and Adrian M. Ionescu [87]: worked on two hybrid FinFET-based circuits that can perform both signal conditioning and sensing.

The initial circuit is a ring oscillator, and the frequency of its oscillation is dependent on the concentration of the analyser, or the voltage drop in liquid. For variable measurements, the second is an adjustable gain pseudo-differential amplifier. According to what we know, there are no FinFET-based circuits that combine bio sensing and readout at this time.

Namrata Mendiratta, Suman Lata Tripathi, Sanjeev kumar, Padmanaban and Eklas Hossain [88]: In compared to other possibilities, MOSFET premised biosensors are utilized for effectively detecting a variety of enzymes, chemicals, infections, and antigens. FET based biosensors make it simple to identify diseases intheir early stages.

Goel, S. Rewari, S. Verma and R. S. Gupta [89]: To determine its suitability for use in the biomedical field for the identification of neutral species in particular proteins and DNA molecules, the Dielectric Restrained (TG GAA) Triple Metal Gate All around MOSFET is being researched as bio- sensor (Biotin & Streptavidin). The oxide layer's cavity has been filled with nanoparticles that have varying biomolecular concentrations and permitivities. Then, in order to incorporate the MOSFET's sensitivity, the variation in threshold voltage (V_{th}) and drain current (Ids) are investigated. The functionality of the TG GAA MOSFET has been contrasted with that of the Single Metal GAA (SG GAA) and Dual Metal GAA (DG GAA) MOSFETs. Due to its compliance with the CMOS procedure of next si-based Lab over Chip Devices and its improved sensitivity, nano gap integrated TGGAA MOSFET is favorable from the perspective of integration.

2.5 Junction less FinFETs : Depletion-based and tunnel-based JLTs are the two basic categories into which JL transistors can be separated. The size of the depletion layer, that is governed by the imposed gate voltage, determines how much electrical current can flow through depletion-based devices. Band-to-band tunneling (BTBT) controls the electrical current in devices with tunnel architectures. A single gate JL transistor is referred to as such when it regulates the device's current flow from the head of the channel. A DG junction less transistor is one that has an additional gate below the channel. A gate electrode that completely encircles the transistor's channel, which may be either cylindrical or rectangular, is what distinguishes GAA JLTs from other types of JLTs. The term "JL nanowire" refers to a transistor channel that resembles a nanotube. The term "JL FinFET" refers to an electronic component that has a fin-shaped transistor.

Biswas, K., Sarkar, A. & Sarkar, C.K[90].: An examination of the effects of the Gate's work function and the geometrical characteristics of the fins, such as the fin aspect ratio, or Fin height/width in relation to the JL bulk's key electrical efficiency characteristics When a FinFET is being considered for a System-on-Chip application (SoC), it is discovered that the device exhibits improved I_{ON}, I_{OFF}, and I_{ON}/I_{OFF} ratio. This study establishes the impact of fin aspect ratio and the material type of the gate work functionality on system efficiency. The results of this investigation will help to create FinFETs that perform better for their respective applications.

Bharath Sreenivasulu V. and Narendar Vadthiya [91]: In this study, utilizing a hetero-dielectric oxide based gate stack to improve the device's sub-threshold performance, they investigated the effects of different dielectric single k as well as dual spacers on improved Junction-less (JL) FinFET at nano-regime. The effects of spacer scaling on DC and analogue functionality at L_G = 10nm for TG FinFETs at gate lengths of 7 nm, 5 nm, and 3 nm were investigated.

Reddy, M. Nomitha, and Deepak Kumar Panda [92]: In comparison to IM FinFET, this paper demonstrates that JL FinFET offers a greater reaction as a phosphine gas sensor in regards of variation in Threshold Voltage (V_{th}), trans-conductance (g_m), and output conductance (g_d).Depending on the evaluation of the sensing parameters, either a JL or an IM FinFET can be utilized to detect phosphine gas. In comparison to the JL FinFET gas sensor, these latter factorslead to better outcomes in the IM FinFET.

2.6 Research Gaps identified:

Out of the various techniques discussed in the research papers above, Silicon based triple gate FinFET device is analyzed in different aspects for this thesis work. There were various motivations for selecting this area of research work. Some of them are being listed below:

1. Further research into FinFETs is required to solve particular data analysis issues that have been seen in the device, as features must be double-patterned (using additional masks) to print appropriately at 20nm and less. Layout-dependent consequences start to show up around 28 nm or above and get worse as the process node size increases. Potential resistivity variances of 50 times or more among the top and bottom metal sheets.
2. Our thoughts on a few issues related to the study of FinFETs, particularly the effort required to increase speed and formulate the decrease of area utilizing Dynamic Threshold Voltage approach can maximize the conversion gain and

minimize the Sensitivity towards physical parameters as in FETs are constructed using a polysilicon gate that encircles the source/drain as well as body (diffusion) regions of the transistor. Since this electric field penetrates in three directions instead of just one, like in a planar gate, it can completely empty the channel in this fashion.

3. Fabrication of FinFET device needs an additional masking at the time of printing under 20nm design technology

4. Layout designing below 28nm increasing more complication due to requirement of additional nodes. Also for all the low level process nodal operations, observed that Electro-migration will dramatically increases.

5. Characterization and Modeling of 18nm triple gate FinFET with varying bio molecule quantities and permittivity within the oxide layer with different biomolecules at different dielectric constants.

6. Decreasing the quantum confinement effect under strong inversion conditions and to further investigate the mesh spacing factors and different gate work functions in order to improve the device's properties at shorter gate lengths.

7. Different hurdles are identified in the advancement of the sensing system that leads to the reduction in the performance.

8. Low power application of FinFET in Biomedical sensing operations and detection of symptoms of any disease using FinFET based biosensors.

9. Proposed dielectric modulation in FinFET for label free biomolecule detection using Visual TCAD simulation tool that giving rise to high-sensitive device due to the introduction of several biomolecules at smaller channel lengths.

10. To obtain the high device performance, it is required to maintain lower device-to-device performance difference in the bio sensing. This challenge is referring to the degradation in the electrical characterization of the different types of sensors in the form of chip.

11. The bio-sensing device designed in the array is required for effective design to minimize the current leakage and the dissipation of the power.

12. The fabrication process of the FinFET device can be easily achieved when all the heights of the fin are considered to be equal. Otherwise, users may face different challenging factors in design layouts.

13. The property of self-heating effect of FinFET device leads to increase in the flicker noise for high K dielectrics that in turn reduces the matched behavior that become

serious concern for analog circuit design.

14. Every individual FinFET Bio Sensor may have different fin widths to detect different bio molecules that may give rise to different molecular concentration ranges.

2.7 Objectives framed:

Objective 1: Design and Performance evaluation of Low Power Triple gate FinFET for sub 22nm technology node

The simulation of sub-22 nm FinFET is carried out that is affected by the physical variability process is implemented to evaluate the performance of Low Power Triple gate FinFET for sub 22nm technology node and therefore evaluated the impact of electrical characteristics such as I_{ON} and I_{OFF}, I_{ON}/I_{IOFF} ratio, DIBL, Subthreshold slope, Threshold voltage in the physical variability process by using Cogenda Visual TCAD (Exploratory Data Analysis) tool. Predictive data on the behavior of FinFET technology, in particular for FinFET from a 22nm innovation to a 10nm technology, is supplied within the I_{ON} and I_{OFF} while taking the impacts variability of process into account.

Transfer characteristics are plotted by varying the drain voltage from 0.05V to 1V, with consistent source, channel, and drain doping levels of 10^19/cm^3, and the gate-to-source voltage ranging from 0 to 1V. Observations indicate that as the gate-to-source voltage increases, the device transitions to I_{ON} at a higher drain current, as evidenced by the transfer characteristics. Valuable insights into I_{ON} and I_{OFF} are gleaned by taking procedural variability into account when analyzing the performance of FinFET innovation, particularly in the transition from a 22nm design to a 10nm technology.

Objective 2:Analysis of process parameter variation such as Temperature Effect, Channel Length, Doping, Oxide Thickness and W/L Ratio for high stability FinFET

In order to achieve this objective, the 10nm and 22nm FinFET technology nodes are analyzed with the process parameter variation by varying the different performance parameters such as Temperature, Channel length, Oxide materials and different doping levels and calculated W/L ratio.

It was noted that 10 nm channel length FinFETs have improved gate control over the channel and decreased leakage current as compared to 22nm Technology node. With changes in electrical parameters, the I_{ON}/I_{IOFF} ratio rises, resulting in a high-stability FinFET device. The relationship between the W/L ratio and trans-conductance (gm), which is determined as the ratio of a change in gate-source voltage to the change in drain current, shows that a greater W/L ratio corresponds to a larger current.

Objective 3: Performance optimization of proposed Triple Gate FinFET with addition of new materials for Source/Drain/Channel region.

The metal contacts with variety of materials which includes the elements like aluminum, copper and platinum at different metal gate work functions, are integrated on a 10nm FinFET in order to achieve this goal.

According to the result evaluation, as that the work function of metal contact at gate is raised to larger levels, the device behaves more favorably and its efficiency improves as the OFF-state leakage current is decreased. The electrical properties of the FinFET device are shown improvement, according to the comparative examination of performance attributes of various dielectric values.

Objective 4: Design and analysis of proposed Triple gate FinFET for biomedical sensing operations

In order to achieve this objective, the effect of different types of biomolecules such as Keratin, Gluten, Zein and Biotin on the performance parameters of the 3 fin 18nm TG FinFET 3D device is observed. The sensitivity of the 18nm triple gate FinFET device is analyzed by different di-electric materials by allowing various types of bio-molecules in to the cavity. The suggested device gives the most ON and OFF currents of order 10^{-4} A/µm and 10^{-18} A/µm and I_{ON}/I_{IOFF} ratio of 10^{12} respectively. Deflection in V_{th} was observed to be ΔV_{th}=0.54 V and ΔV_{th}=0.23 V for values of K = 10 and 1 respectively. Even though, different implementation aspects like subthreshold slope, drain-induced impedance reduction and central capability are examined for suggested system.

Dielectric constant as well as cavity distance can be changed to analyze the biosensor execution. The I_{OFF} decreases with minimization of cavity length. Hence, the I_{ON}/I_{IOFF} ratio is observed as greater for a shorter cavity distance. It is finalized, which the sensitivity of bio-sensor is high by absorbing most-dielectric constant protein bio-molecules in cavity area. It is an important level toward the understanding of multiple molecules sensing with fully integrated silicon FinFET Transistors.

2.8 Methodology followed for carrying out the work: Fin Field Effect Transistor dimensional features are defined by the width and height of the fin. The gate length derived explains the "critical design dimension" that divides the nodes of the drain and source. A vertical fin is estimated over substrates from one side of the fin to the other to allow an interface between the three sides of the channel or fin. This builds the control over the channel electrically, helping to decrease Short Channel Effects (SCE) and leakage currents, thereby achieving higher on-current.

The device's functional channel length is described by adding W_{fin} and H_{fin} twice. The flow diagram discusses the process followed while simulating the device in TCAD in figure 2.2.

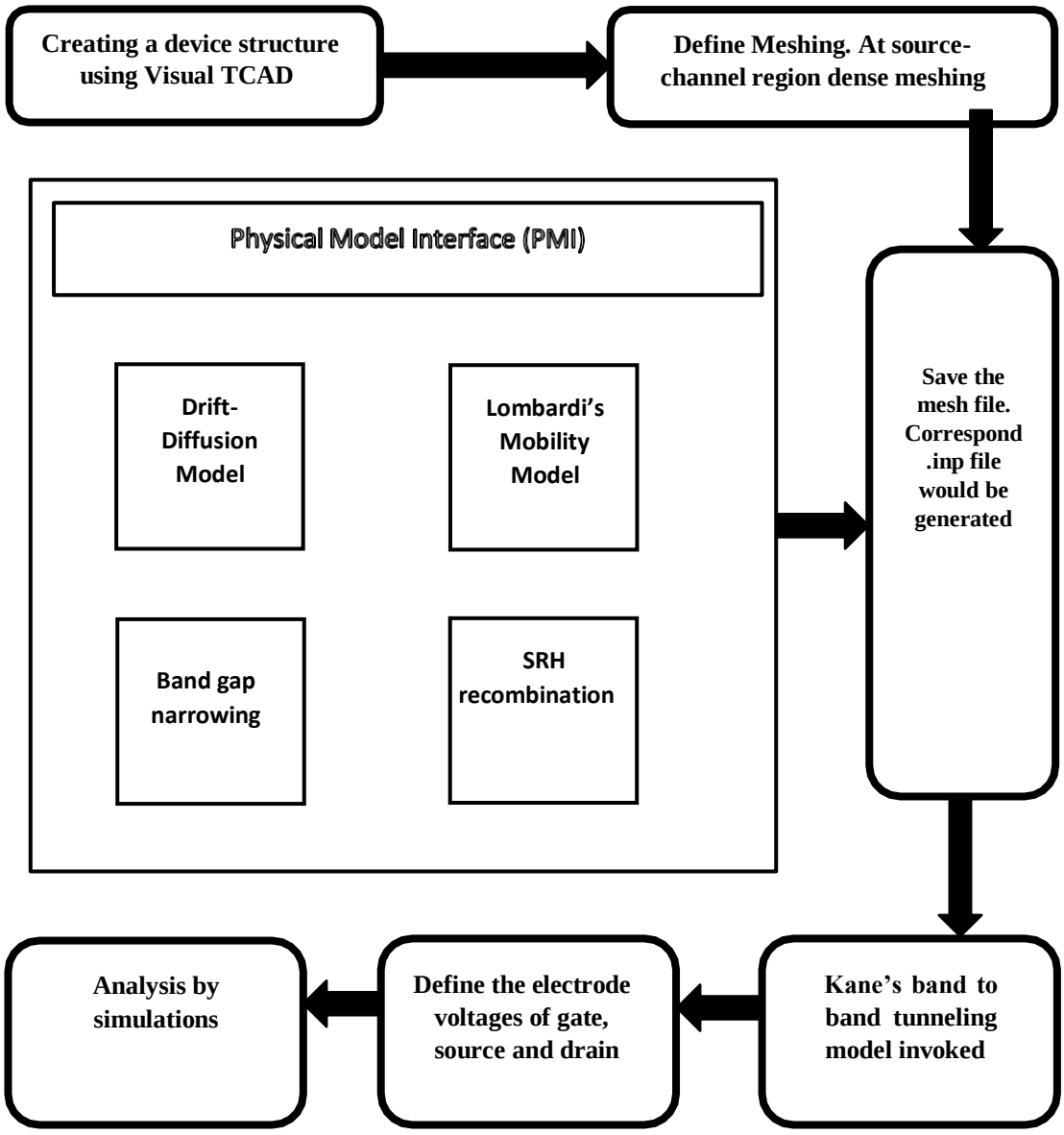


Fig. 2.2 Methodology

The device should be structured in TCAD proceeding earlier to the characterization of the device. Device modeling ended in a few steps, first defining the regions and selecting the materials used for the design.

Later, nitride spacers must be positioned to prevent lateral diffusion and modeling system contacts must be explained. Later conclusion of the first and second steps, the source doping concentration and drain areas are explained if the circuit modeling and doping are ended,

and later the system must mesh the two presented meshes being local and global meshing. Global meshing is used to cover the entire device while local meshing is used to enclose the junctions. Meshing is final step for earlier characterization of the device, later achievable meshing the command to examine the modeled device must be checked.

Fin Field Effect Transistor dimensional borderlines are height and balance thickness; the drawn gate length represents the "basic plan measurement" that is the center of the discrete source and channels. It directly gives high power authority and helps to reduce Short Channel Effects and spillage flow, thus achieving high on-flow. The length of the active channel of the device is determined by the balance thickness.

Deploying a gadget in TCAD is required earlier for imaging of the gadget. A gadget screen should be viable, but strides along with a locales classified and the planning is done as per the choosing the materials to be utilized. Then it is necessary to place nitride spacers to avoid parallel diffusion and the presented device contacts can be classified. [99] Later conclusion of mentioned steps of source group and channel, region doping will be classified. Work on the gadget lattice should be done after the gadget display and doping are done. The two presented lattices are neighborhood and global arrangement.

The flow chart describes the simulation of the device under two broad categories of DC analysis and AC analysis. In order to determine the ON current, IOFF and the I_{ON}/I_{OFF} ratio of the device DC analysis need to be carried out by setting the drain, source and gate voltages under "device simulation". When the drain current v/s gate voltage characteristics curve is plotted on the log scale, ON current and IOFF values become differentiable and therefore I_{ON}/I_{OFF} ratio can be calculated accordingly.

The other parameters need to be calculated to determine subthreshold swing as well so as to measurethe amount of steepness of the proposed structure. The device needs to be studied under linear and the saturation regions to understand the phenomenon of DIBL[100].

2.9 Sequence of steps followed in the Visual TCAD:

To study the analog/RF performance of the device, AC analysis plays very important role. [93] The parameters like trans-conductance, device efficiency, unity gain frequency, gate-drain capacitance, gate-source capacitance, etc. of the device are explored.

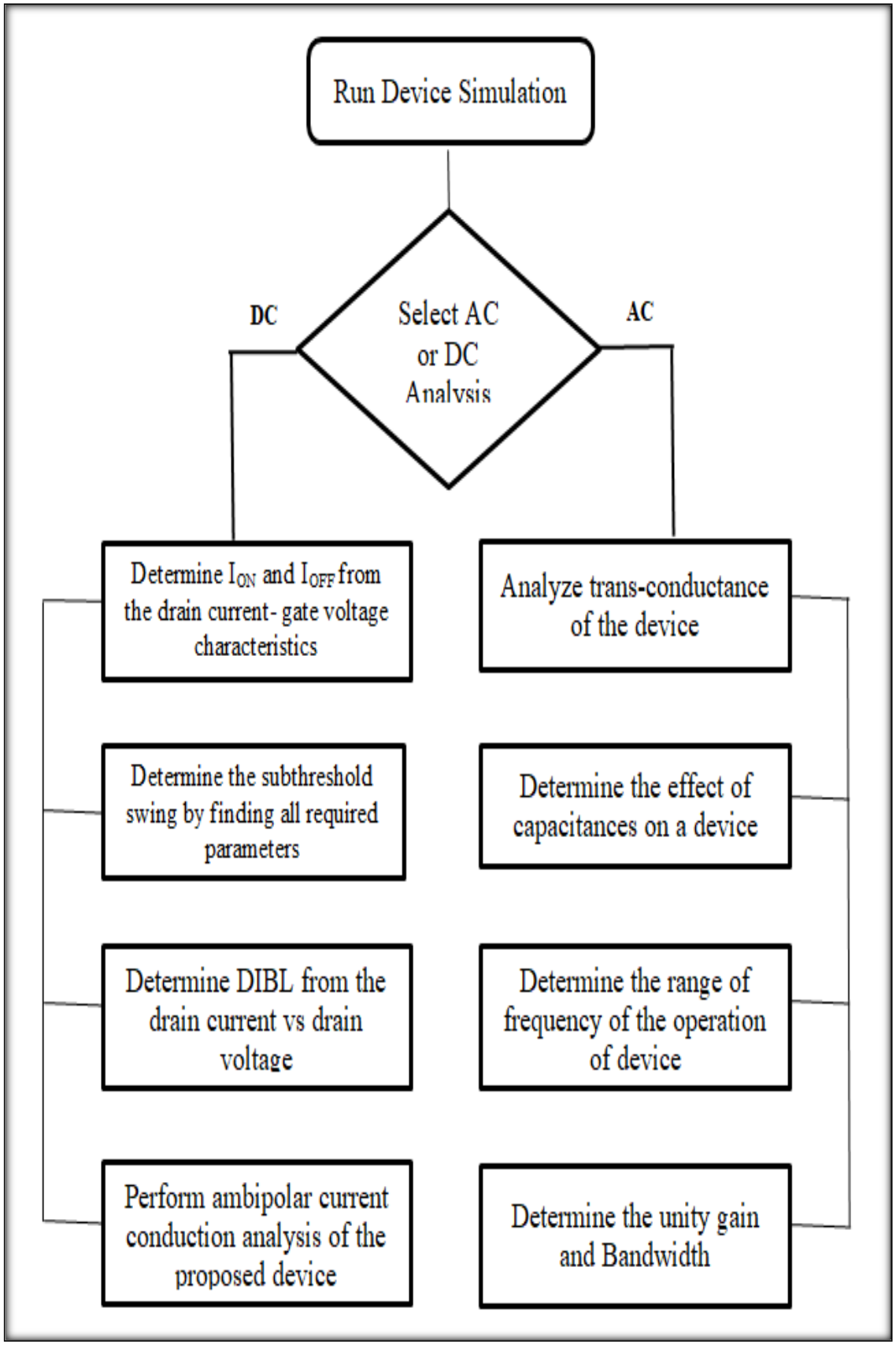


Fig. 2.3 Flow chart for simulation [93]

2.10 Chapter Conclusion: The usage of the conventional MOSFET have been decreased as the updated technology is letting the innovators to update with new electronic switches for appreciable performance at very lower power consumption and remarkable reduction in short channel effects (SCE). Observed the increase in the gate control over the channel by using FinFET multi-gate level technology. This chapter briefing the literature survey of different papers worked on different MOSFETs in various areas. The research gaps are identified from the survey to understand the FinFET technologies that have been addressed to explore the research discontinuity. In order to understand the better insight about the issues of the FinFET technology related to the circuit design and manufacturing are clearly mentioned in the survey of different works. Hence from the research gaps identified through literature survey, the four objectives are framed to meet the final objective of my thesis. The first objective that deals with the analysis of 22nm FinFET performance characteristics such I_{ON}, I_{OFF}, I_{ON}/I_{OFF} ration, DIBL, Subthreshold slope are analyzed using Visual TCAD in the next chapter.

CHAPTER 3: PERFORMANCE EVALUATION OF LOW POWER TRIPLE GATE FINFET FOR SUB 22nm TECHNOLOGY NODE

3.1 Introduction to Sub 22nm Technology:

In sub-22nm node planar bulk CMOS technology is changed by applicants for Multi Gate Field Effect Transistors (MuGFETs) because of the development in electrostatics as well as short channel execution. When transistors are in the OFF position, a multi-gate circuit develops driven current by reducing leakage current. The transistor will be framed on a Silicon On Insulator or bulk silicon substrate. At the present time, several choices for multiple gate devices are suggested. Short Channel Effect controls fin devices are unique in industrial approaches and are differentiated with others completely. [94,95]

The most important methods to increase execution according to lesser scattering, mobility of carrier are eventually higher ON current is analyzed by strain engineering of Tri-gate and DG-Fin Field Effect Transistor. A Double Gate-Fin Field Effect Transistor (DG-FinFET) is similar to a Fin Field Effect Transistor, because of a convention that was suggested by recent research.

Moreover, Fin technology is required to maximize I_{ON} and minimize I_{OFF} leakage current (balancing of height, channel length, Fin as well as oxide width. In Fin Field Effect Transistor of sub-22nm technology the effect of different methods on their electrical nature should be ignored if the bulk Complementary Metal Oxide Semiconductor operates extremely reactive to functions the variability. The main task objective is to check scaling impacts on ON and IOFF in the range related to the Fin Field Effect Transistor technologies from 20nm to 7nm.

The effect of the variability method on potential technical nodes can possibly be assessed by detecting the most important criteria of behavior relating to the Fin Field Effect Transistor method utilized in digital projects and spotting the need for examination of complete electrical characteristics in the visual TCAD improvement activities and tools by Fin Field Effect Transistor technology. [96]

3.2 Implementation using Visual TCAD tool: The robust calculation of sub-22 nm Fin Field Effect Transistors electrical specifications is impacted by physical variability. It is suggested to evaluate performance of Low Power Triple gate FinFET for sub 22nm technology node and therefore evaluated the impact of electrical characteristics such as ON and IOFFs, I_{ON}/I_{IOFF} ratio, DIBL , Subthreshold slope, Threshold voltage in the physical variability process by using Cogenda Visual TCAD (Exploratory Data Analysis) tool.

The nature of related information about the Fin Field Effect Transistor method, in particular, the examination of function variability impacts the Fin Field Effect Transistor from 22nm technology to 10nm technology is presented in I_{ON} and I_{IOFF}. I_d -V_{gs} shift parameters for various V_{ds} (0.0.5V-1V) as well as channel, source and drain doping (10^19 /cm^3) and V_{gs} - 0 to 1Volts. By I_d-V_{gs} shift parameters; it will be noticed that the V_{gs} increase, the circuit switch ON at greater I_D.

Those calculations help to understand the sources of variation affecting FinFET devices and identify important behavioral criteria for utilization of Fin Field Effect Transistor devices in digital models. The aim of focusing on I_{IOFF}s is highly affected by the influence of geometrical specifications on Fin Field Effect Transistor devices than ON current.[97-99]

3.2.1 The FinFET structure:

Fin engineering is required to reduce and increase the I_{ON} inrush current as well as I_{OFF} leakage current in digital devices that balances Fin height, width, channel length, and oxide width. A typical 22nm Fin Field Effect Transistor fabrication framework is presented in the figure 3.1. Fin Field Effect Transistor structure includes vertical Si fins which generate the channel region and whose ends are interconnected with source and drain regions on every side. The gate area wraps over this vertical fin. Both sides of the device and the fin are also generated above the layer of the Metal Oxide Semiconductor channel.[100]

Rather than making the Metal Oxide Semiconductor channel in the layer under the gate, which makes the layer of the fin wafers, it neglects the SCE in the Fin Field Effect Transistor. As the gate is displayed over the channel region, there is high electrostatic regulation above the charge carriers.

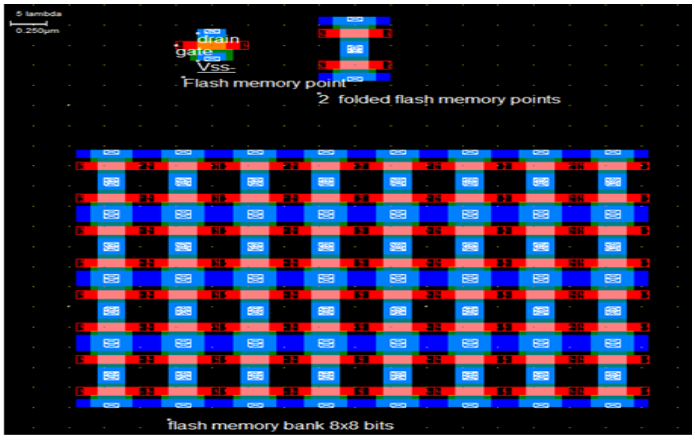


Fig. 3.1 22nm FINFET fabricated structure

Fin height per unit area shows a larger current drive for FinFET compared to planar circuits. The number of fins in a Fin Field Effect Transistor is equivalent to the current density.

These Fin Field Effect Transistors do not require more doping. Hence; they are less vulnerable to variations of RDD. Fin Field Effect Transistors have various frameworks with various gates as well as patterns. [101]. Height of the fin (H_{FIN}), width of the Fin (W_{FIN}) and length of the gate (L_g) are significant geometrics characteristics of Fin Field Effects Transistors. The fin-structured shape where the gates are fully extended into the framed area through depletion areas, suggests the free charge carriers that are unavailable to enable Short Channel Effect suppression in Fin Field Effect Transistors.

A high relation among the variation of the I_{ON} and the I_{OFF} and variation of threshold voltage was spotlighted presence of metal gate granularity. Work function factor is formed depending on the functioning operation of the metal depending on its grain orientation. In a perfect producing method, for the devices with metal gate contact, they are fabricated with equally aligned metal and with minimal ork function factor deviations. However, in the original production method, metal gate circuits are usually generated with metals with various work functions (Φm), which are unsystematically oriented, happening with higher differences in (work function) WF[101-103].

FinFET's measurement borders are classified by the height and width of the balance and "basic plan dimension" is the length of the draw gate separating centers of the source as well as channel. [38] A vertical blade impinges on the substrates as it passes from balance single side of the later to interface the balance or channel three sides. This provides higher electric charge directly as well as supports reducing spillage flow and SCE, thereby achieving higher on-flow.

The balance width determines the active channel length of the circuit [104]. Before this, they go for gadget imaging; they require showing the device in TCAD. Device display is available with strides from scratch, they have to categorize locales as well as choose the materials that are used for arrangement. After, they require placing nitride spacers to avoid parallel diffusion and to categorize the contacts of the displayed circuit [105]. Later the first two steps, they have to categorize doping group of source as well as channel regions, if doping and device display are complete they have to arrange the gadget globally into two lattices and neighbors. Used to cover the complete device internationally and enclose nearby partitions. The cross-section is considered the last advance at earlier the device description is effective after the lattice [106].

Table 3.1 Device model parameters for 22nm FinFET

PARAMETER	DIMENSION
Channel length [L_{ch}]	22nm
Gate length [L_G]	14nm
Drain, Source length [L_D , L_S]	10.5nm
Effective oxide thickness [T_{ox}]	2.8205nm
Fin thickness [T_{fin}]	4nm
Channel doping concentration, N_{Ch}	1e+15/cm^3
Doping concentration, N_{Sd}	1e+18/cm^3

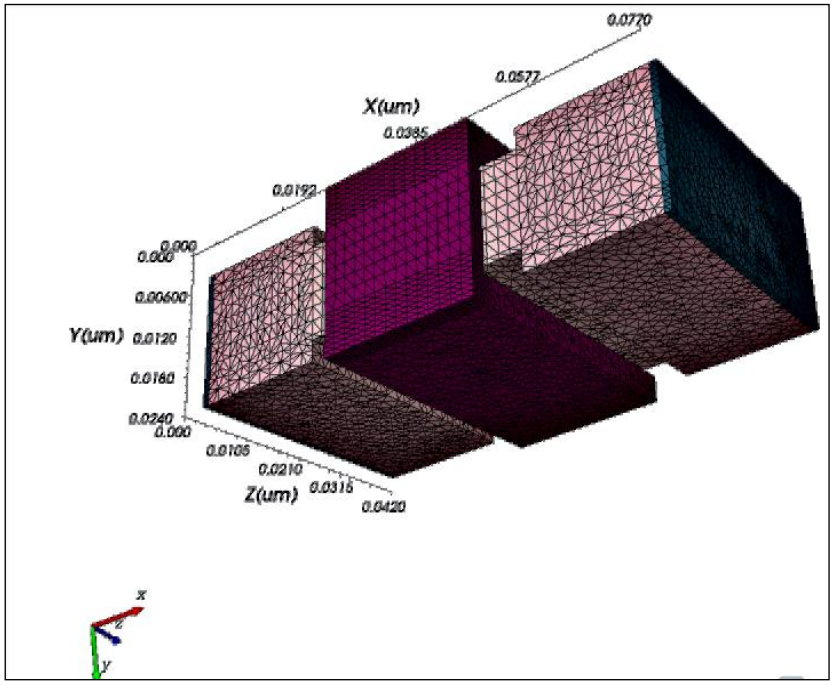


Fig. 3.2 3D structure of 22nm FinFET

Figure 3.2 is the structure of 22nm FinFET with SiO_2 as oxide layer, with the specifications mentioned in the Table 5.1. Here the nature of device is analysed by evaluating the performance parameters like threshold voltage, DIBL, the I_{ON}/I_{IOFF} ratio by varying V_{gs} from 0V-1V. The I_{ON}/I_{IOFF} ratio is obtained by varying different cavity lengths for better performance of FinFET.

3.2.2 Results and Discussions:

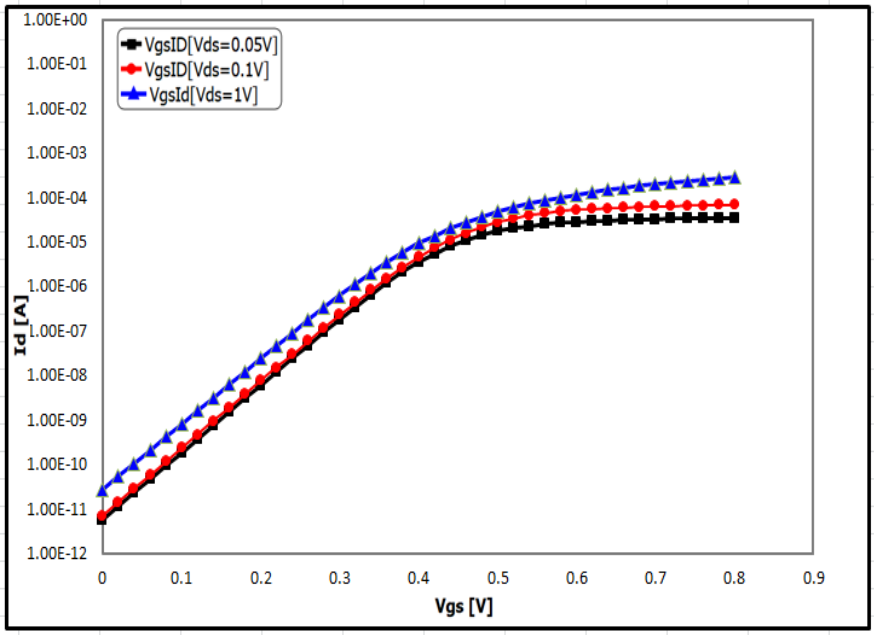


Fig 3.3 22nm FinFET I_d vs V_{gs}

In subthreshold (V_{gs}<V_t) region: $I_d = e^{\frac{qV_{gs}}{nkT}}$

Fig.3.3 Presents the I_d-V_{gs} Transfer specifications that differ from V_{ds} (0.05V-1V) as well as source, channel and drain doping (10^{19} /cm^3) and gate to source voltage ranges from 0 to 1V. By the drain current voltage gate to source transfer specifications; it is noticed from the graph that I_d is differing exponentially according to voltage gate to source and as it enhances, the circuit switches ON at greater I_d.

Fig.3.4 Presents I_d -V_{gs} Transfer Characteristics for 22nm Fin Field Effect Transistor graphed at normal temperature (300^0K) or lower as well as upper of normal temperature (250^0K - 350^0K). It is noticed that if V_{gs} differing from 0 to 1Volts and the growth in temperature, there is greater difference in I_{OFF} for Fin Field Effect Transistor and that is impacted by temperature difference is V_{th}. Because of growth in the temperature at 250^0K to 350^0K, the V_{th} reduces by fifteen percent for Fin Field Effect Transistor.

The device presents high affect on V_{th} because of difference in temperature in Fin Field Effect Transistor. Drain Current (I_d) differs exponentially ranges (10^{-11} to 10^{-5}mA) by rise in temperature. It presents the rise in voltage gate to source, the drain to saturation current (I_{ds}) of circuit reduces and becomes stable if temperature rises. The executions specifications are evaluated and presented in the Table 3.2.

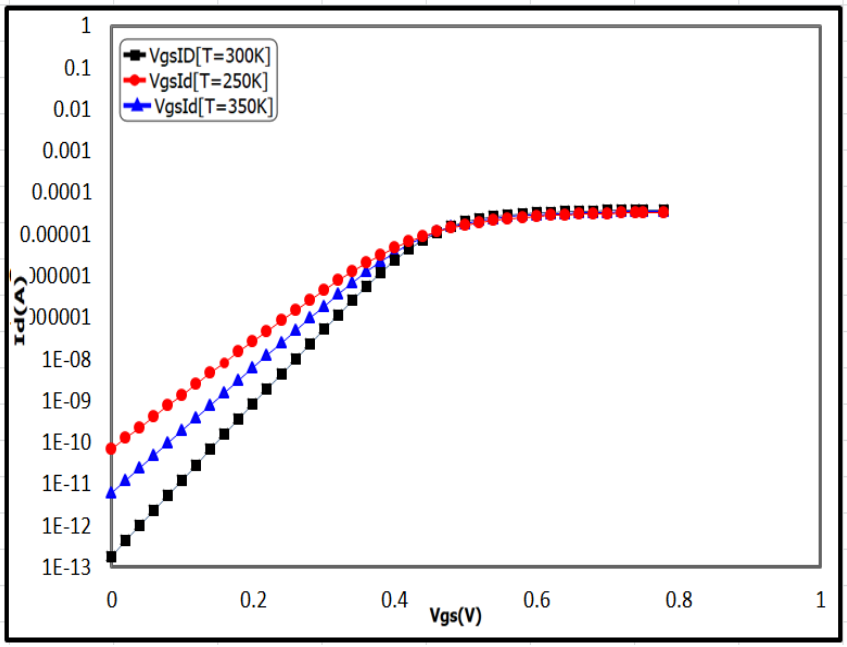


Fig. 3.4 22nm FinFET I_d vs V_{gs} at different temperature

Table 3.2 Performance Characteristics of 22nm FinFET

Length of the Channel		22nm
Performance Characteristics of 10nm FinFET	Threshold Voltage	0.46V
	Sub Threshold Slope	75mV/decade
	I_{ON}/I_{OFF} ratio	$0.71*10^6$
	DIBL	38.927mV/V
	C_{gs}	752pF
	C_{gd}	240pF
	g_m (Trans conductance)	42mA/V

Fig 3.5 presents results specification (I_d - V_{ds} plot) for 22nm Fin Field Effect Transistor if V_{gs} ranges from 0.1V to 1V and V_{ds} ranges from 0V-1.2Volts. On this graph, I_{ON} and outcome resistance are the two features, which arise from the high inversion area.

The I_{ON} rate is higher in Fin Field Effect Transistor as considered by Bulk MOSFET. As the channel for Fin Field Effect Transistor is arranged in three dimensions it shows higher outcome resistance. Due to this noticeable stability in gate is noticed and well saturation level with various gate biasing is indicated in the graph.

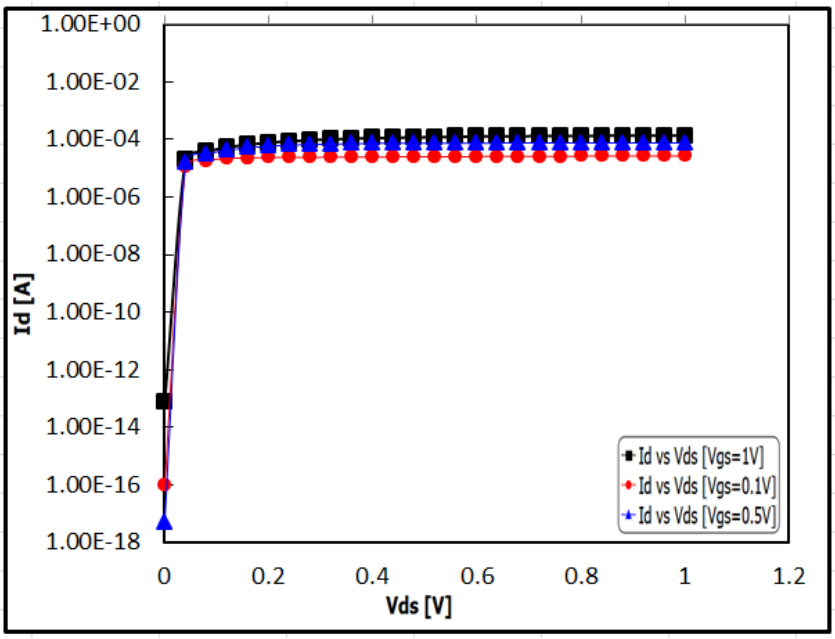


Fig.3.5 22nm FinFET I_d vs V_{ds} (V_{gs}= Const)

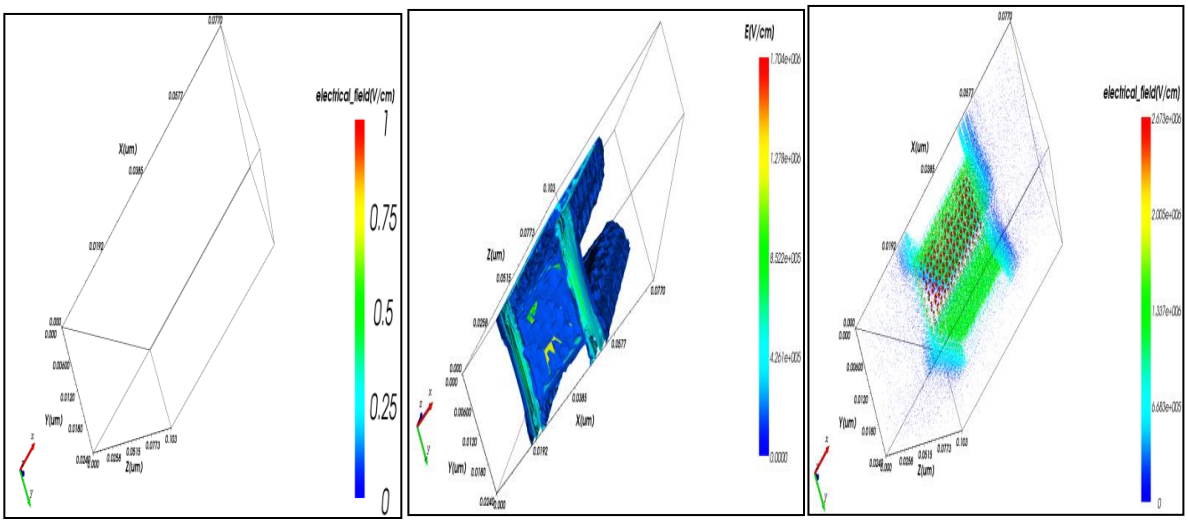


Fig 3.6 Electric Field (V/cm)

Figure 3.6 describes the comparative study of electrical field for 22nm FinFET along a path that is derived in the mid of the channel. It derives the electrical field at its average level which is relatively stronger for 3D 22nm FinFET that has shown with wrapped gate.

Figure 3.7 shows that the potential obtained for 22nm FinFET is in between -4.7V to -4.160V. Also the figures 3.8 and 3.9 give the dimensional view of electron and hole mobility. Therefore the forth trigate 22nm Fin Field Effect Transistor model is presented complex developments in device features such as layer potential, electric field, electron as well as opening versatility.

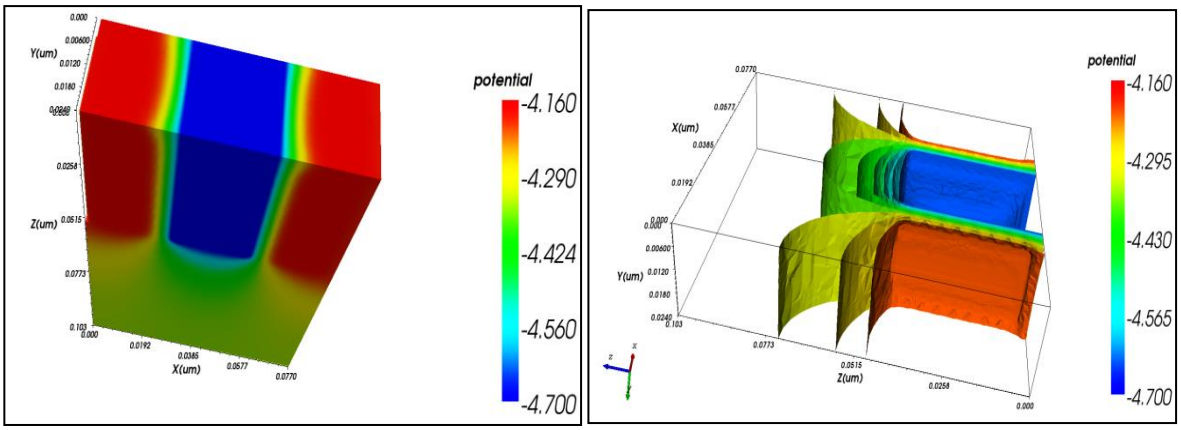


Fig 3.7 Surface Potential of 22nm FinFET

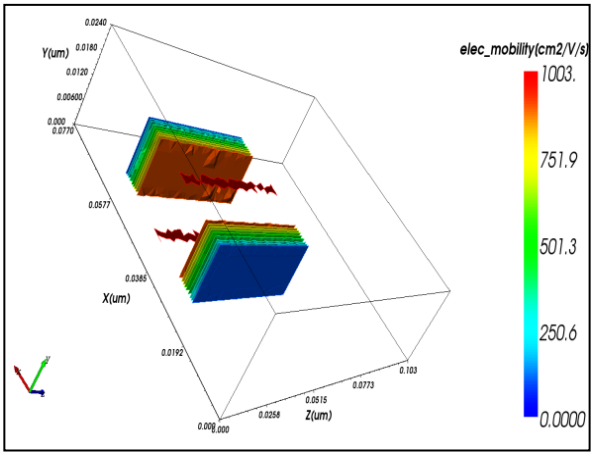


Fig 3.8 Electron Mobility

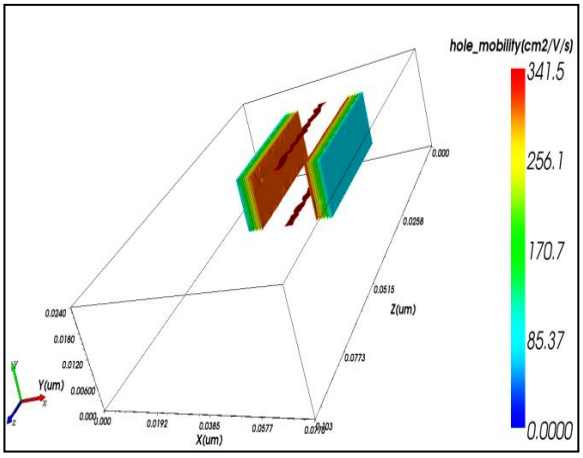


Fig 3.9 Hole Mobility

Threshold voltage V_{th}: It is the voltage needed on the Gate terminal of the enhancement type MOSFET to form a thin channel beneath the gate electrode (between Source & Drain terminals), so that the current can flow between both the terminals. So threshold voltage is the voltage needed to turn on the device. As the MOSFET is voltage controlled current source, the output current will depend on the gate voltage applied.

$$V_{th} = V_{FB} + 2\Phi_F + \frac{\sqrt{2\epsilon_s q N_a (2\Phi_F + V_{SB})}}{C_{ox}} = 0.5V \quad \text{.....(3.1)}$$

Subthreshold Slope: It is defined in the subthreshold region, where the drain current behavior is being controlled by the gate and is as same as to the exponential decrease in the current when the diode is operating in the forward bias. Hence the plot between the drain current and gate to source voltage with drain, source and other bulk voltages are fixed that gives approximately log linear behavior in the MOSFETs. Therefore to calculate, it is given by its slope known as subthreshold slope.

The subthreshold slope is given by the reciprocal of the subthreshold swing and is expressed as

$$\mathbf{S_s = ln(10)\frac{kT}{q}\left(1+\frac{C_d}{C_{ox}}\right)} \text{.....(3.2)}$$

A device characterized by steep subthreshold slope exhibits a faster transition between off (low current) and on (high current) states.

SS = dV_{gs}/ d($\log I_d$) mV/decade (>60mV/decade) = 75 mV/decade

I_{OFF} = Subthreshold Leakage current. $V_{gs<}V_{th}$

I_{ON}/I_{OFF} = ON and OFF Ratio = $2.3*10^{-5}/3.2*10^{-13}=0.71*10^{8}$

Drain Induced Barrier Length:

$$(DIBL)=\frac{\partial V_{gs}}{\partial V_{ds}} mV/V=1.0294*e^{-08}/1.00294*e^{-08}= 38.927mV/V$$

3.2.3 Short Channel Effects:

Subthreshold Swing

The value of V_G required to develop the I_D with ten folds is known as subthreshold swing and its measurement is mV/decade. The feature will be as small as feasible. Hence, the small variation in gate to source (V_{GS}) voltage will give larger variation in the I_D, therefore generating a transistor appropriated for lower voltage function.The subthreshold swing in terms of the drain current is expressed as:

$$\mathbf{S = ln\,10\frac{1}{\beta}\frac{dV_G}{d\varphi_s} = ln10\frac{kT}{q}\left(1+\frac{C_D}{C_{ox}}\right)} \text{.....(3.3)}$$

Where V_G specifies the gate voltage, T_s specifies surface potential, I_D denotes drain current, C_d represents the depletion capacitance, C_{ox} represents oxide capacitance and kT/q is thermal voltage. For a Metal Oxide Semiconductor Field Effect Transistor the perfect outcome that will be attained is 60mV/decade. The evaluated average sub-threshold swing of the suggested circuit in the following expression:

$$\mathbf{SS_{avg} = \frac{V_{th}-V_{OFF}}{\log(I_{th}-I_{OFF})}\ mV/decade} \text{.....(3.4)}$$

Here V_{th} represents the threshold voltage, V_{OFF} is V_{GS} at the lower I_D, whereas, I_{TH} and I_{OFF} shows the drain currents at V_{th} and V_{OFF} respectively. The V_{th} is evaluated by utilizing the stable present technique.The V_{th} is found as 0.5 Volts. From log drain current vs. gate to source voltage, the essential specifications are found. For the suggested circuit, the SS_{avg} isevaluated as 75mV/decade.

Drain Induced Barrier Lowering

The Graph presents an outstanding subthreshold swing of 75mV/decade and has an I_{ON}/I_{OFF} ratio of 0.71×10^{6}. Moreover, Drain Induced Barrier Lowering (DIBL) was evaluated by noticing linear drain current vs. gate to source voltage curve and saturation modes as presented in graph. Drain Induced Barrier Lowering is a SCE process in that the depletion region extends by the growth in drain voltage as well as reduces the potential barrier at source in short channel circuits. Drain Induced Barrier Lowering acquired in the circuit is the value of 38.927mV at the channel length of 22nm. The equation used for Drain Induced Barrier Lowering evaluation is given as:

$$\text{DIBL} = \frac{V_{TLIN} - V_{TSAT}}{V_{DSAT} - V_{DLIN}} \quad \textbf{.....(3.5)}$$

Where $V_{D}SAT$ and $V_{D}LIN$ are supply voltages at saturation and linear mode. $V_{T}LIN$ and $V_{T}SAT$ are voltages acquired by utilizing the stable current technique at linear and saturation mode, respectively.

3.3 Chapter Conclusion: To conclude the chapter, the analysis of the 22nm FinFET device encompasses both DC and AC aspects, considering a channel length of 22nm is done. The obtained results include a threshold voltage (V_{th}) of 0.46Volts for various gate biases (V_{gs}), ranging from 1.5V to 0V, corresponding to I_{ON} and I_{OFF}, and different constant voltages (V_{ds}). The calculation of the I_{ON} and I_{OFF} ratio, as well as the Drain-Induced Barrier Lowering (DIBL), is performed by leveraging circuit performance characteristics. The Drain-Induced Barrier Lowering and subthreshold swing of Tri-gate devices are computed and contrasted with the standard properties of a Fin Field Effect Transistor. The Triple-gate Fin Field Effect Transistor exhibits positive control over channel charges, maintains a relatively constant subthreshold slope, features a higher I_{ON}/I_{OFF} ratio, and experiences lower subthreshold leakage current. Consequently, it can be concluded that the tri-gate FinFET demonstrates a reduction in Short-Channel Effects (SCE) in an improved direction. Thus to improve the stability of FinFET in terms of I_{ON}/I_{OFF} ratio and other performance characteristics, a 10nm FinFET is introduced in the next chapter.

CHAPTER 4: ANALYSIS OF PROCESS PARAMETERS VARIATION FOR HIGH STABILITY 10nm FINFET

4.1 Introduction:

Longitudinal built gates, which are "critical design dimension" that divides the drain and source nodes, adjust the altitude and density of the fins on a FinFET device. Whether it connects all 3 edges of a channel or fin by going through one fin end to the next, vertical fin is extended above the substrate. Increased electrical channel control, reduction of SCE and leakage currents, and increased ON current are all results of this. W_{fin} and H_{fin} are added together to achieve the device's effective channel length. Before moving on to the characterization of the device, the device must be modeled in TCAD.

The device modeling will be finished in a series of phases, starting with the definition of the areas, followed by the selection of the materials and level of doping for the transistor framework. Placement of nitride spacer to stop lateral diffusion as well as fine-tuning modeling system connections must come next. Once the device modeling and doping have been finished, the source doping concentration as well as drain areas are determined. Two meshing options are then available: local meshing and global meshing.

While local meshing is used to cover junctions, global meshing is used to cover the whole device. The final stage before characterizing the device is meshing. Following a satisfactory meshing command, an inspection must be carried out to assess the modelled device.

The stature and balance thickness of the FinFETs define their dimensional bounds, and the sketched gate length describes their "basic plan measurement," which consists of segregated channel nodes and source [110]. If vertical one crosses from one balance side to next, it will be possible to connect towards the channels or the 3 balanced sides. High on-flow may be obtained by providing severe electrical authority over direct and sustains to lower SCE and spilling stream. Balance thickness determines the length of the device's powerful channel. Before, gadget representation was necessary in order to exhibit the device in TCAD.

Device display must be practical while supporting steps from the start, and locations should be characterized as well as the plan materials employed. After that, nitride spacers must be used to prevent parallel device spreading so that the exhibited device connections may be identified. Area doping could be identified when the aforementioned stages for source group as well as channel are finished. Work on the gadget lattice must be performed after the completion of gadget display and doping. Local and global fitting are two lattice options.

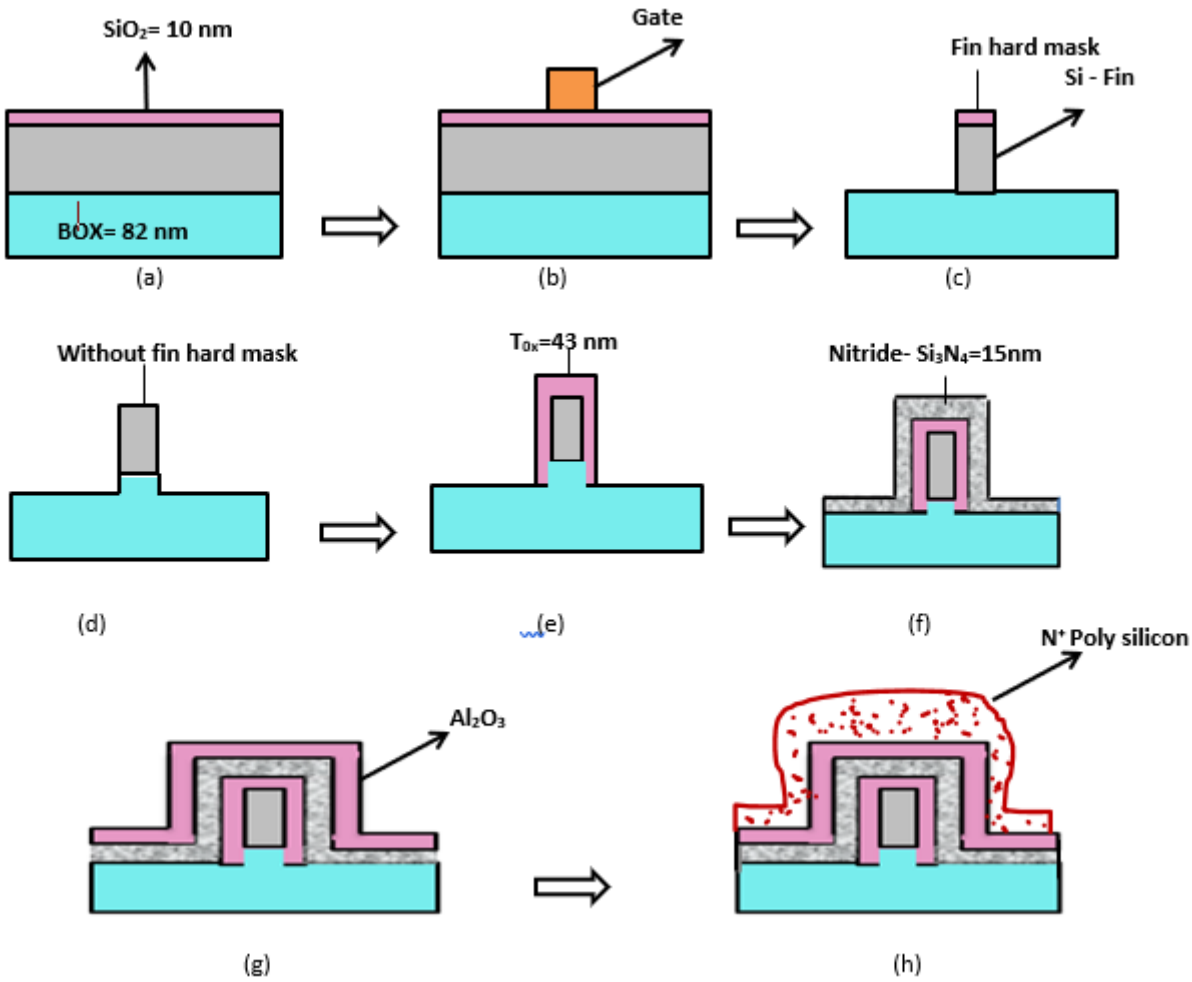


Fig 4.1: Schematic device fabrication process flow for triple gate 10nm FinFET.

Following are the manufacturing procedures for the suggested 10nm TG FinFET:

- Thermal oxidation method utilizes a box of SiO_2 that is 82 nm wide and 10 nm long.
- Next, a fin pattern is formed using an electron beam, then a channel length of 10 nm is formed using the etching procedure, next tunnel oxide T_{ox} was then formed using a thermal oxide process at 3000^{o}K.
- Nitride layer, a charge-trapping surface, was used to create spacers having a 4 nm width among the source, drain, as well as gate using reduced chemical vapour deposition.
- A 25 nm-wide layer of Aluminium (Al2O3) was deposited for such metal contacts between the drain and the source.
- Lastly, 10nm-wide N+ poly silicon was placed on Aluminium.

Equivalent Oxide Thickness: In order to rapidly compare various dielectric materials to silicon oxide dielectric, which is the industry standard, the EOT concept is useful, as follows:

$$EOT = t_{high\text{-}k}\left(\frac{K_{sio2}}{K_{high-k}}\right)$$

Where $t_{high\text{-}k}$ = material thickness in high-K grades

ITRS determines EOT (International Technology Roadmap for Semiconductor)

SiO_2 is chosen for 3nm.

Various High K materials are : Si_3N_3, TiO_2, ZnO_2, Al_2O_3, HfO_2 etc

By using above formula, the thicknesses of different High K materials are as follows:

ZnO_2 : $K_{ZnO2} = 16$; therefore $t_{ZnO2} = 12.307$nm

TiO_2 : $K_{TiO2} = 81$; therefore $t_{TiO2} = 62.3076$nm

HfO_2 : $K_{HfO2} = 21.25$; therefore $t_{HfO2} = 16.34$nm

Al_2O_3 : $K_{Al2O3} = 7$ to 9 ; therefore $t_{Al2O3} = 6.15$nm

4.2 Implementation of 10nm FinFET using Visual TCAD tool:

The 10nm FinFET's 3D architecture is depicted below in Figures 6.1 and 6.2, correspondingly, using various oxide materials, SiO_2 and HfO_2. The various model characteristics for the 10nm FinFET architecture are presented in Table 4.1.

Table 4.1 Device model parameters for 10nm FinFET

PARAMETER	**DIMENSION**
Channel length [L_{ch}]	**10nm**
Gate length [L_G]	**8nm**
Drain, Source length [L_D, L_S]	**3.5nm**
Effective oxide thickness [T_{ox}]	**2.8205nm**
Fin thickness [T_{fin}]	**4nm**
Channel doping concentration [N_{ch}]	**1e+15/cm^3**
Doping concentration [N_{sd}]	**1e+18/cm^3**

It is sometimes referred to as the proportion of changing gate-source voltage to fluctuating drain current and is important for trans conductance (gm). As a result, a higher W/L proportion causes large power at certain voltage of source.

The following is a Drain current of MOSFET formula for saturation:

$$I_d = \left(\frac{1}{2\mu CoW/L}\right)(V_{gs}\text{-}V_{th})^2 \qquad (4.1)$$

4.2.1 10nm FinFET Device structure with SiO_2 :

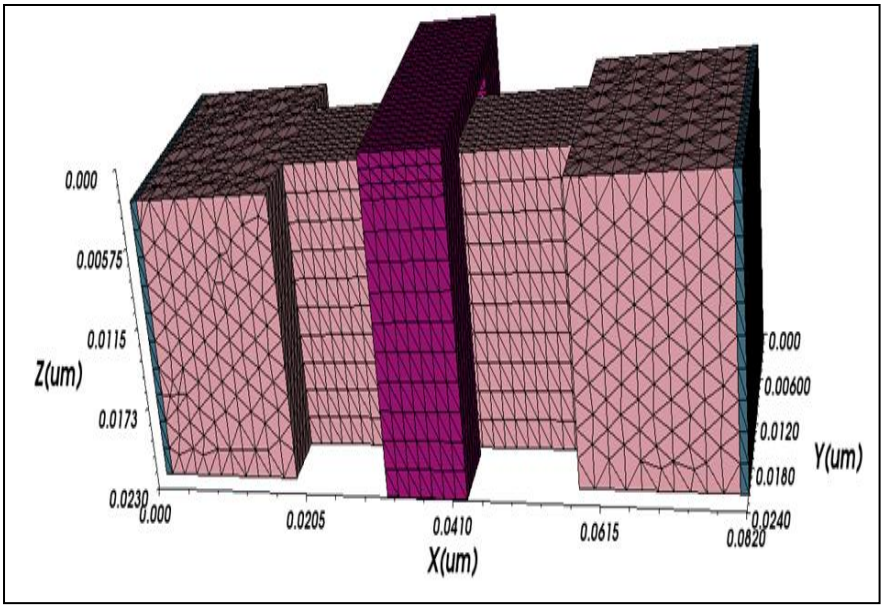


Fig 4.2 10nm FinFET Device with polysilicon and SiO_2

From Fig. 4.2, the geometrical measurements are :

The formula for the W/L ratio is -W/L Ratio = 0.082/0.010 = 8.2.

4.2.2 10nm FinFET Device structure with HfO_2 :

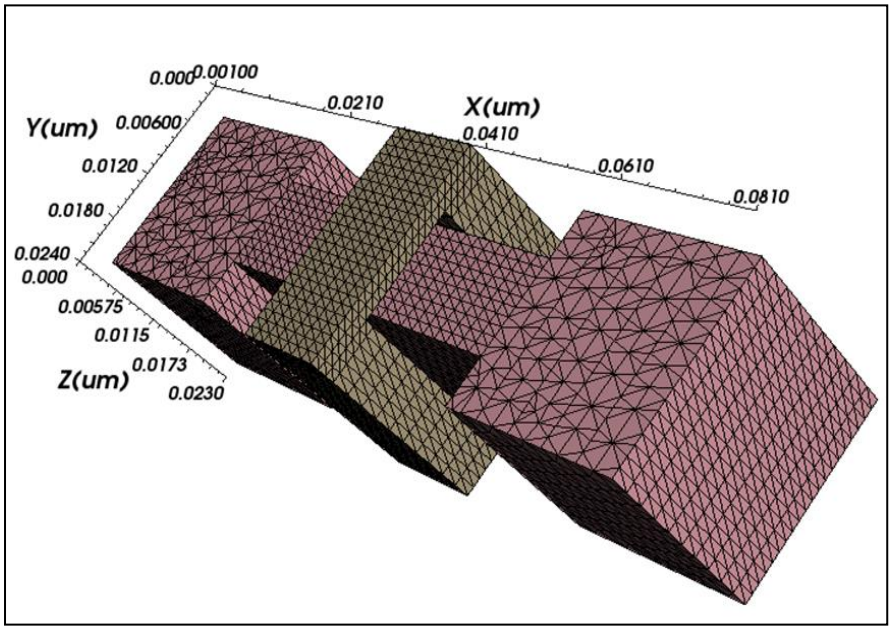


Fig 4.3 10nm FinFET Device with Electrode and HfO_2

The W/L ratio may be determined using the geometrical considerations displayed in Fig. 4.3, and this is represented by the following formula.

W/L Ratio = 0.080/0.010 = 8.

It is quite clear that once the oxide element was changed from SiO_2 to HfO_2, the W/L proportion decreased from 8.2 to 8.

4.3 Simulation Results and Discussions:

Regarding electrostatic channel energy under various conditions, electrostatic characterization of a FinFET was observed in this case. Second, different design characteristics, operating circumstances, contact elements, and oxide materials are tested together with the properties of the drain current.

4.3.1 Electrostatic behavior of 10nm FinFET

For gaining physical understanding of the device's structure, the fluctuation of surface potential is particularly important. This study presents and validates a detective surface potential framework as well as TG-FinFET threshold voltage using simulation findings that were really obtained and are displayed in Figures 4.4.

With the increased electrostatic behavior of 10nm FinFET, it has been shown that the TG FinFET architecture has increased short channel characteristics. With this device shape, the height and breadth of the fin have a significant impact on the electrostatic behavior of the FinFET gadget. The shift in peak value that N_{Ch} induces with an increment in channel doping concentration has a negligible effect upon that device's electrostatic behavior.

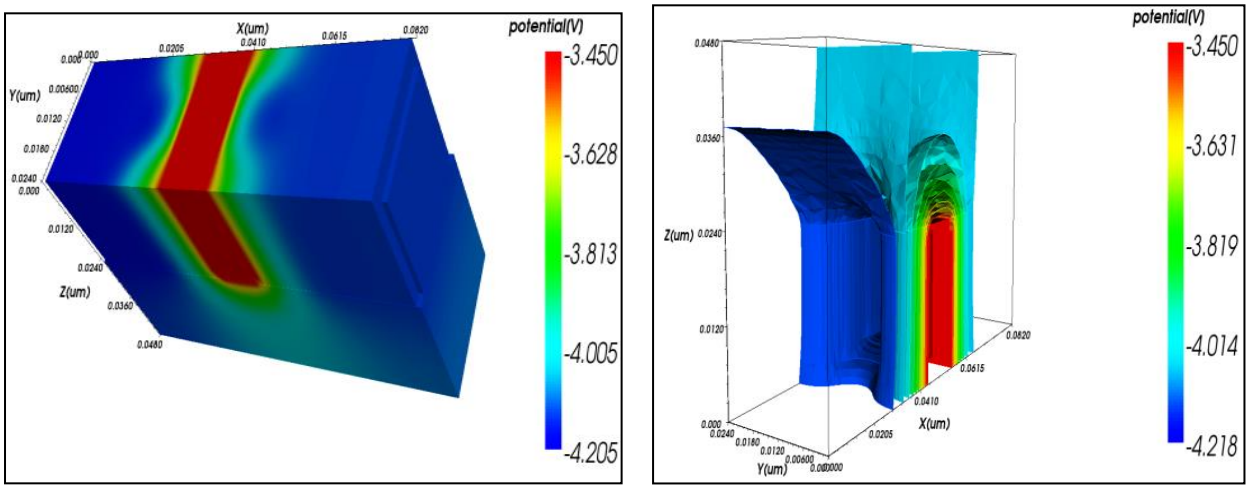


Fig. 4.4 Surface potential of 10nm FinFET

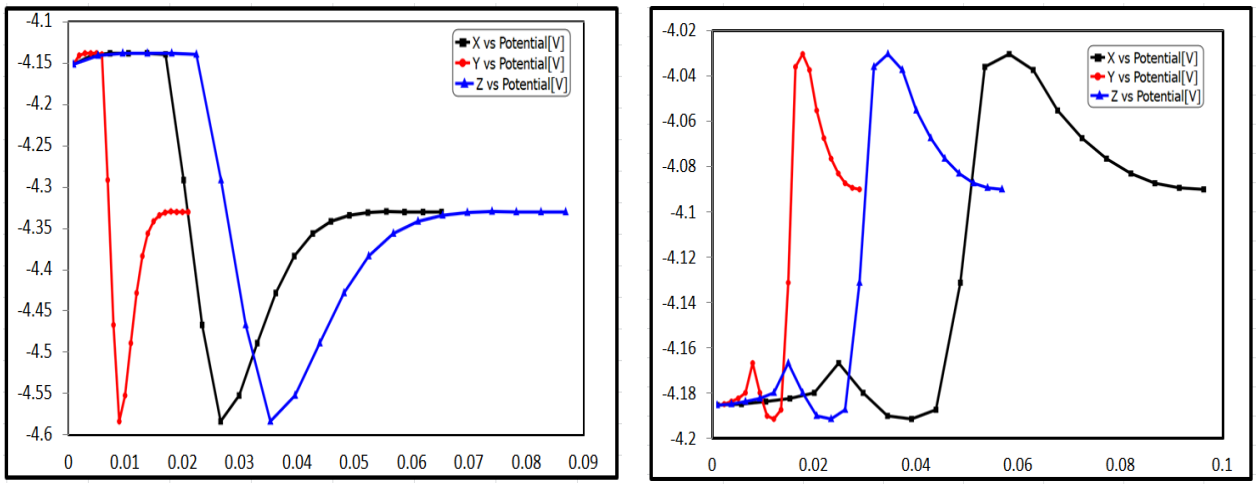


Fig. 4.5 Comparative plot for Potential of 10nm FinFET with SiO_2 and HfO_2

Figure 4.5 illustrates that when exclusively using the HfO_2 gate oxide, the ON-state current consistently registers higher values across all V_{GS} values compared to SiO_2. Additionally, an observable reduction in the threshold voltage occurs with an increase in the dielectric constant of the gate oxide, attributed to the increased gate capacitance. This enhancement in the coupling between the gate and the channel leads to an increase in the inversion charge density and a decrease in V_{th}, ultimately resulting in higher drain current.

Having 10nm thickness of SiO2, the TG 10nm FinFET architecture has since demonstrated notable increases in device characteristics including opening adaptability, electron, electric field, as well as surface current.

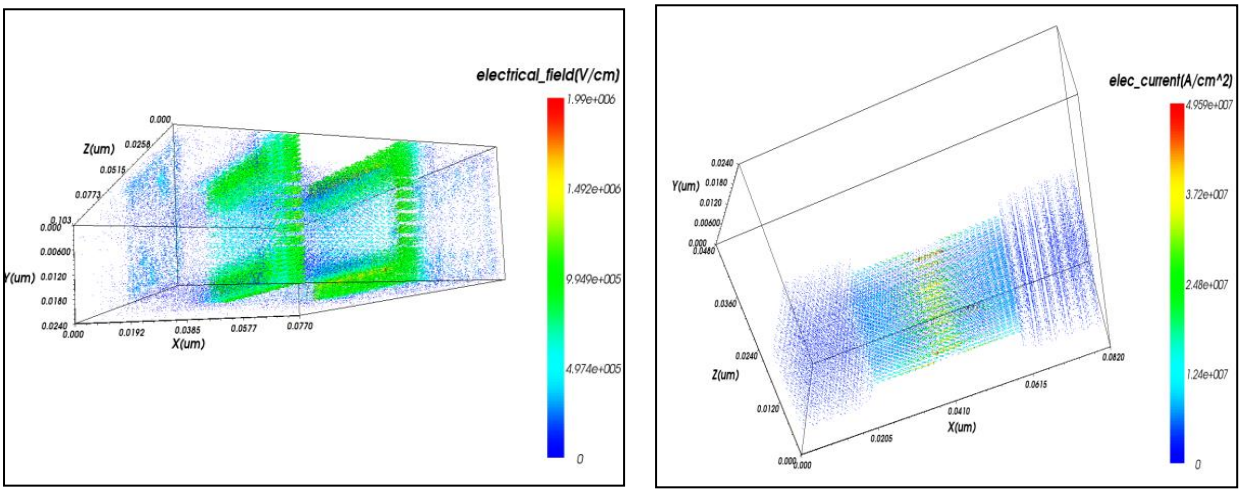


Fig. 4.6 Comparative study of Electric Field for 10nm FinFET with SiO_2 and HfO_2 .

In Fig. 4.6, the electromotive force for a 10nm FinFFT containing SiO_2 as well as HfO_2 oxide is compared, in addition to the electric field's strength and a straight line across the channel. The mean electric field is greater for 3D FinFETs with wrapped gates, as can be shown in Fig. 4.6

4.3.2 V-I Characteristics for 10nm FinFET:

Transfer Characteristics:

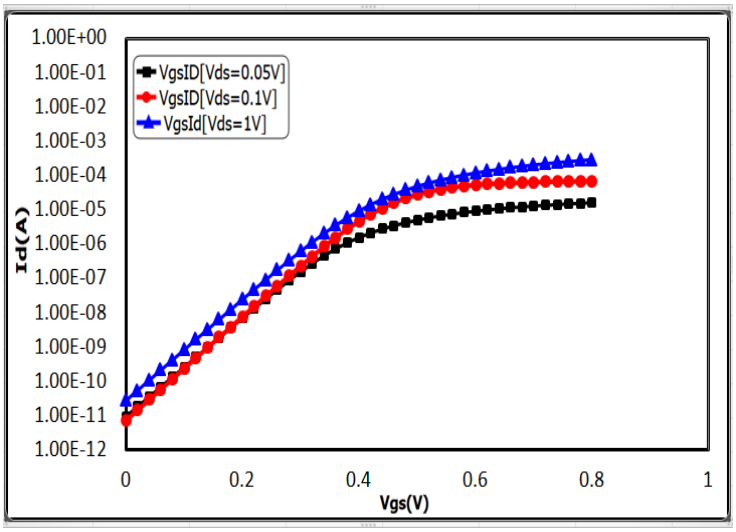


Fig. 4.7 10nm FinFET I_d vs V_{gs}

From this, it is evident that the current remains at zero in the device until and unless the gate to source voltage maintained at high compared to the threshold voltage V_{th}. Under this position, the device will create a path in the channel that will connect the drain and the source terminals.

Once V_{gs} crosses V_{th}, the current flow through the device increases and then saturates. From the above figure, it is shown that as gate to source voltage V_{gs} increases from 0V to 1V, note that OFF voltage is in order of 10^{-13} and ON current in the order of 10^{-5} with I_{ON}/ I_{IOFF} ratio 4.34* 10^{8}. It is evident that the current ratio is comparatively higher when compared to 10nm FinFET.

Output characteristics:

The electrons are drawn towards the surface when the drains to source energy V_{ds} upon that uppermost electrode rises from 0V to 1V. It is discovered that the surface density of electron increases density of surface hole at a specific voltage level, known as the threshold voltage. As illustrated in Figure 4.8, the surface also underwent an inversion there at threshold voltage, the initial substrate of a n-type inversion layer is reached by switching from p-type polarities. The negative charge inside that inversion barrier is combined with negative charge within the ionic acceptor layer to balance the positive electrical charge on the gate. It demonstrates that whenever the drain to source voltage V_{ds} is applied between 0V and 1V, the drain current I_d remains constant with an increment in gate to a source voltage V_{gs} of 0.1V, 0.75V, and 1V. Additionally, the 10nm FinFET's I_{OFF} is higher than the 22nm FinFET's because of the geometrical features.

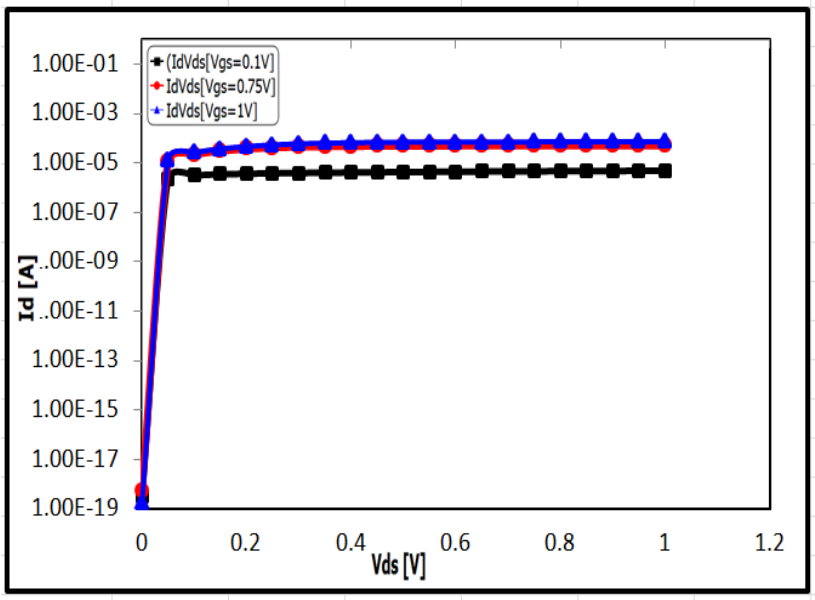


Fig.4.8 I_d vs V_{ds} (V_{gs}= Const) for 10nm FinFET

4.3.3 Analysis of process parameters of 10nm FinFET

Analysis of performance characteristics of 10nm FinFET with different channel lengths:

Mostly in I_d-V_{gs} graph beneath, which is displayed in Fig. 4.9, the analysis was performed with various channel lengths of 10nm and 22nm. It is evident that the 10nm channel width FinFET exhibits an increment in I_{ON}/I_{OFF} ratio along with improvements in the numerous different electrical

characteristics, leading to a highly stable FinFET device. Additionally, the gate control across the channel has improved, and at 10nm length, less leakage current is seen. Table 4.2 provides a comparison of efficiency metrics for various channel lengths.

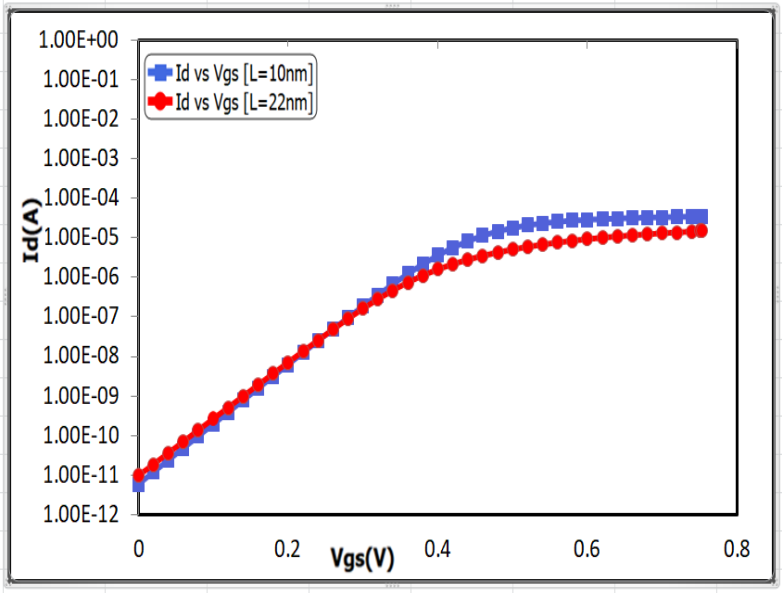


Fig. 4.9 I_d vs V_{gs} curve for different channel lengths

Table 4.2 Performance characteristics of two different channels

Performance Characteristics	10nm FinFET	22nm FinFET
Threshold Voltage	0.5V	0.46V
Sub Threshold Slope	72mV/decade	75 mV/decade
I_{ON}/I_{OFF} Ratio	$4.34*10^8$	$0.71*10^6$
C_{gs}	810pF	752pF
C_{gd}	260pF	240pF
g_m(Transconductance)	42mA/V	15mA/V
DIBL	60.03mV/V	38.927mv/V

In the sub-threshold (V_{gs}<V_{th}) region: $I_d = e^{\frac{qV_{gs}}{nkT}}$

As V_{gs} rises, it is evident from I_d-V_{gs} transfer attributes at which the device turns ON at greater I_d. The 10nm FinFET's subthreshold slope somewhat increased when length of channel was reduced from 22nm to 10m. The characteristics such as ON current and output resistance may be determined thanks to a strong inversion area in the FinFET. A FinFET with a 10nm length of channel, a high resistance to output, reduced channel length variation will have a higher ON current value. Because a FinFET's channel is encompassed by three dimensions, this form of transistor has superior gate control.

Analysis of 10nm FinFET with different temperatures of different performance characteristics:

Generally, the leakage current is observed due to direct tunneling of the electrons through gate oxide and gate leakage is insensitive towards temperature. It is evident that sub threshold leakage is having high impact due to the changes in the temperature.

The maximum portion of sub threshold leakage is nothing but the diffusion current of the minority carriers and their concentration is increased exponentially with temperature. Because of its higher temperature sensitivity, sub-threshold leakage is the prominent component of the total power consumption statistically at higher temperatures. The threshold voltage is lowered with an increment in the temperature that leads to a decrease in the ON current and hence I_{ON}/ I_{OFF} ratio decreases.

$$V_T = \emptyset_{ms} - \frac{kT}{q} ln\left(\frac{q^2 n_i t_{si} t_{ox}}{4\epsilon_{ox} KT}\right) \quad \text{.....(4.1)}$$

Features of 10nm FinFETs at various temperatures are given in Table 4.3 and the graph below, which shows how the gate to source voltage V_{gs} increased as temperature varied (measured in ^{0}C) and how drain current I_d remained unchanged from V_{gs} values varying among 0.55V and 1V. There is a discernible shift with in I_{IOFF} as a result of the temperature fluctuation. The threshold voltage is another significant performance characteristic whose change is influenced by temperature. The 10nm FinFET cutoff voltage lowers from 0.64V to 0.46V when temperature rises from -123.15°c to 126.85°c with the threshold voltage decreases by 15% for FinFET. This demonstrates that cutoff voltage is sensitive to changes in temperature than I_{IOFF}.

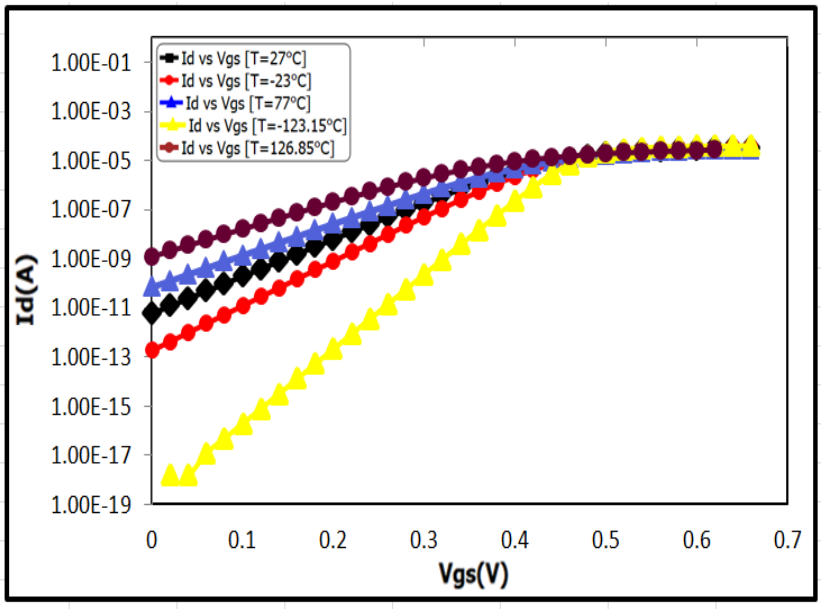


Fig. 4.10 Performance characteristics of 10nm FinFET at different temperatures

Table 4.3 Performance characteristics 10nm FinFET with temperature effect

Performance characteristics	Temperature in ^{0}C				
	-123.15^{0}C	-23^{0}C	27^{0}C	77^{0}C	126.85^{0}C
Threshold Voltage	0.53V	0.51V	0.5V	0.48V	0.44V
Sub Threshold Slope	82 mV/dec	81.2 mV/dec	72 mV/dec	74.5 mV/dec	72 mV/dec
I_{ON}/I_{OFF} Ratio	$8.6*10^8$	$5.08*10^8$	$4.34*10^8$	$0.48*10^6$	$0.07*10^6$
DIBL	36.06mV/V	37.05mV/V	60.03mV/V	41.03mV/V	43.08mV/V

However, the variance in drain current displays the smooth shift having a comparable curve type. It depicts that there is larger influence on V_{th}, because of the the change in temperature from negative to positive Celsius degree in FinFET. Drain Current I_d varies exponentially ranging from 10^{-11} to 10^{-5}mA with the increase in temperature. Also it is depicting that with the increase in the gate to source voltage, there is decrease in the saturation current of the FinFET, otherwise become constant at certain temperatures..

Estimation of performance characteristics of 10nm FinFET technology using different oxide materials:

When using the oxide substance HfO_2 instead of SiO_2, the 10nm FinFET's I_d-V_{gs} attributes significantly improve (see Fig.4.11). In Table 6.4, together all characteristics for both oxide materials have been determined and presented.

Since, EOT =$t_{high\text{-}k}\left(\frac{K_{sio2}}{K_{high-k}}\right)$

EOT is determined by ITRS, and 3nm is selected for SiO_2, where thigh-k is the thickness of t_{high} k material. Here, $KHfO_2$ = 21.25 and HfO_2 is employed as a high-k element to boost FinFET durability.

Therefore t_{high}-k of HfO_2 is determined as :

$t_{high\text{-}k} = \frac{3*21.25}{3.9}$ = 16.34nm

In the suggested device configuration, a higher dielectric constant substance called HfO_2 has been employed in place of SiO_2 to get out of some drawbacks. According to the simulation graph, the 10nm FinFET employing HfO_2 as the dielectric material performs superior in terms of drain current.

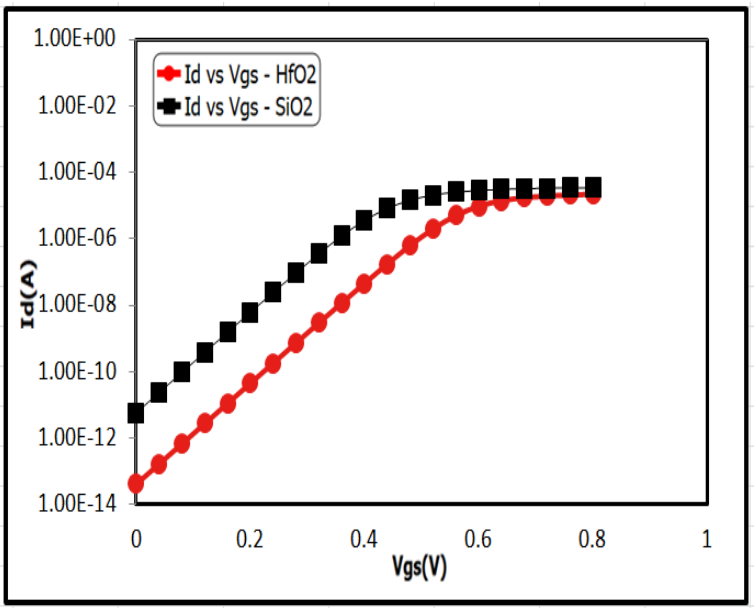


Fig. 4.11 Performance characteristics of 10nm FinFET with different oxide materials

Table 4.4 Performance characteristics 10nm FinFET with different oxide materials

Performance Characteristics	10nm FinFET (SiO_2) (3nm)	10nm FinFET (16.34nm)
Threshold Voltage	0.5V	0.3V
Sub Threshold Slope	72 mV/decade	86.8mV/decade
I_{ON}/I_{OFF} Ratio	$4.34*10^8$	$5.13*10^7$
DIBL	60.03mV/V	68.9mV/V

It is also clear from the simulation that changing the threshold voltage in relation to a gate work mechanism would improve the device's efficiency. The correct modification of a metal gate work mechanism in this case demonstrates a striking enhancement in the device architecture for any SCEs in FINFET.

Performance characteristics of 10nm FinFET analyzed with different doping levels:

As the doping increases in the channel, establishes the barrier between the source and drain. Also the more carriers will be injected into the channel being controlled by gate. Hence the threshold voltage will not be changing at higher drain voltages and therefore Drain induced barrier lowering is also suppressed. Hence the reduction of Drain induced barrier lowering is seen with the increase in the channel doping. The effect of doping in the channel on sub threshold slope is observed that as there is increase in the doping concentration, sub threshold slope is minimized.

Due to increase in the concentration of channel doping, charge sharing is minimized between the gate and drain with in the channel; also it generates a higher potential barrier between the source and drain. Because of this, the control of gate over the channel is observed electrostatically to a higher level and subthreshold slope has been reduced. With the increase of the doping levels of the channel of the FinFET device, there is reduction in the inversion charge density that in turn raises the level of threshold voltage giving rise to a decrease in the ON current. The current ratio has been shown appreciable improvement with the increase in the doping of the channel.

For FinFET innovation, the undoped channel is preferred. Generally little doping is advised in order to regulate the leakage current. Because of the high dopant need in the Source/Drain area, the device's series resistance is increased. This alters the shape of the device's fin. In order to solve this issue, in-situ epitaxial development is carried out between the source and drain area, whether or not eliminating the structure's fin.

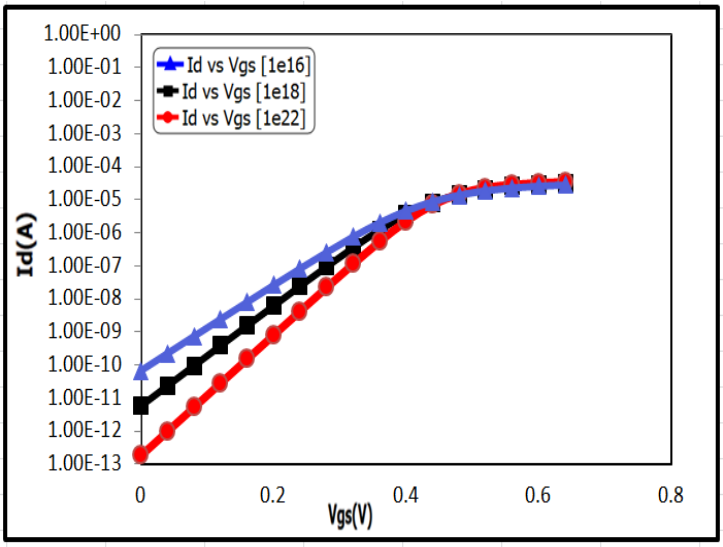


Fig. 4.12 I_d vs V_{gs} Characteristics with different Doping levels

Table 4.5. Performance characteristics of 10nm FinFET with different doping levels

Performance Characteristics	1E-16	1E-18	1E-20
Threshold Voltage	0.55V	0.5V	0.46V
Sub Threshold Slope	82 mV/decade	72 mV/decade	68.3 mV/decade
I_{ON}/I_{OFF} Ratio	$5.03*10^6$	$4.34*10^8$	$8.03*10^8$
DIBL	61.4mV/V	60.03mV/V	58.05mV/V

The evaluation of the I_d-V_{gs} graph in Fig. 4.12 was done with various levels of doping, including 1E-16, 1E-18, and 1E-20. It is seen that while the doping extent increases, there exists an increment in the I_{ON}/I_{OFF} ratio and consequently in many electrical characteristics, leading to a high-stability FinFET device.

In the above mentioned table 4.5, performance metrics at various degrees of doping are compared.

It demonstrates that the fins' increased height and high levels of doping would restrict the upper gate against being forced into a total depletion phase, which may be created over the fins with help of the lateral gate management. Also it is clear that as the doping levels increases, I_{ON}/I_{OFF} ratio is increasing, but the other parameters Threshold voltage, subthreshold slope and DIBL decreases

4.4 Chapter Conclusion: In conclusion, the reduced power as well as higher sub-threshold efficiency of 10nm TG FinFET design is examined. By using Cogenda Visual TCAD, the device 10nm triple-gate FinFET is designed, examined and simulated. The device performance optimization is done by analyzing drain current characteristic at different channel lengths, SiO_2 and HfO_2 oxides, different doping levels and different temperatures for the proposed 10nm Triple gate FinFET . The proposed device has shown appreciable improvement in I_{ON}/I_{OFF} ratio up to 10^8. The electrostatic behavior is also evaluated that include electrical behavior, surface voltage, electron, and hole concentration traits are derived from the displayed device architectures. In continuation of this, the same the high stable 10nm FinFET device is analyzed further with different contacts for source and drain and with different dielectric constants at low power consumption.

CHAPTER 5: ELECTRICAL CHARACTERIZATION OF 10nm FINFET FOR DIFFERENT CONTACTS AND DI-ELECTRIC CONSTANTS

5.1 Introduction:

A method for fabricating a transistor involves the presence of source, drain, and channel regions in silicon substrates, exposed through openings in a dielectric film. These openings lead to the channel area, featuring sidewall spacers. The process includes incorporating metal silicide in the source and drain regions, forming a high-K dielectric layer in the channel area, creating a metal gate film using the high-K dielectric layer, applying an initial metal liner film over the metal silicide in the source and drain regions, the gate film, and the sidewalls of the openings in the dielectric film. Also a subsequent metal film is formed by the initial metal liner film, with a width that fills the opening, followed by planarization of the initial metal liner film and the subsequent metal layer below the dielectric layer. This innovation introduces an alternative method where the channel not only shapes the high-K dielectric layer in the area but also establishes a metal gate layer on a dielectric film, executed prior to generating the metal silicide in the source and drain regions.

The FET comprises a semiconductor substrate of a specific type and a high-K dielectric layer situated on this substrate. A dielectric film with an initial width extends over the substrate, featuring an initial opening to the source region and subsequently to the drain region. Both the initial and next openings have a silicide layer on the source and drain regions, along with a third opening leading to the metal gate. These openings incorporate an initial metal layer on the first silicide layer below and on the sidewalls, and a second metal layer is positioned above the first metal, filling the first and second openings. The initial metal extends from the metal gate over the sidewalls of the initial and subsequent spacers and on the sidewalls of the third openings, while the second metal layer is positioned above the initial metal, loading the third openings.

5.2 Performance evaluation of 10nm FinFET using Visual TCAD tool

A 10nm FinFET is designed and implemented at different metal contacts such as Aluminum, Copper and Platinum with different metal gate work functions. Also 10nm FinFET is analyzed with the different materials for source, drain and gate are also simulated for high performance. Simulating the device has shown that with the increase in the metal gate work function to bigger levels has shown a appreciable increase in the performance of the FinFET and also decrease in the leakage current that has shown appreciable performance in the device. The comparative analysis of performance parameters of different dielectric values is calculated and observed that electrical characteristics of the 10nm FinFET device are improved.

5.2.1 SiGe based 10nm FinFET architecture:

SiGe is one of the most attractive material systems for FinFET applications due to its flexibility, mature synthesis techniques, and controllable bandgap. The controllable bandgap allows for effective tunneling injection as well as ambi-polar conduction suppression.

The proposed SiGe based FinFET is shown in Fig. 5.1. The matter utilized in the source area is $Si1 - xGex$, an x is the molar concentration of the Germanium. The utilization of SiGe mixture substance makes sure the lower energy band gap from source surface, thereby reducing channel thickness. The drain current will increase as a result of this. The source and the drain terminals are attached through the metallic contacts. The gate terminal is made up of polysilicon and remains insulated from the channel due to the SiO2 layer. The impact of using polysilicon is to align the gate mask during the fabrication process such that the parasitic capacitances are reduced. The other advantage is that the smaller threshold voltage could be obtained. Spacers are utilized at the source and drain. The spacers are utilized at source and drain surface to increase the ON current.

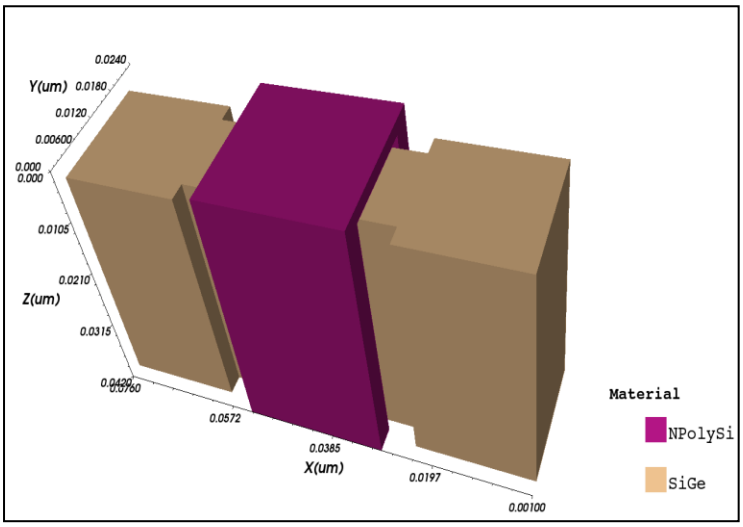


Fig 5.1 SiGe Based 10nm FinFET

Figure 5.1 is the structure of 10nm FinFET with SiO_2 as oxide layer and SiGe is replaced with silicon wafer for high performance of triple gate FinFET. Analyzed the device and evaluated the performance parameters like threshold voltage, the I_{ON}/I_{IOFF} ratio. Higher I_{ON}/I_{IOFF} ratio is observed for this device when compared to the device fabricated only with Silicon.

5.2.2 10nm FinFET 3D Structures with various contacts for source and drain materials:

Figure 5.2 are the structures of 10nm FinFET with SiO_2 as oxide layer and different metals like Copper and Platinum are utilized for source and drain material contacts for high performance of triple gate 10nm FinFET. Analyzed the device and evaluated the performance parameters like threshold voltage, the I_{ON}/I_{IOFF} ratio for various metal contacts. Higher I_{ON}/I_{IOFF} ratio is observed for this device fabricated using Copper as metal contact when compared with Aluminium and Platinum.

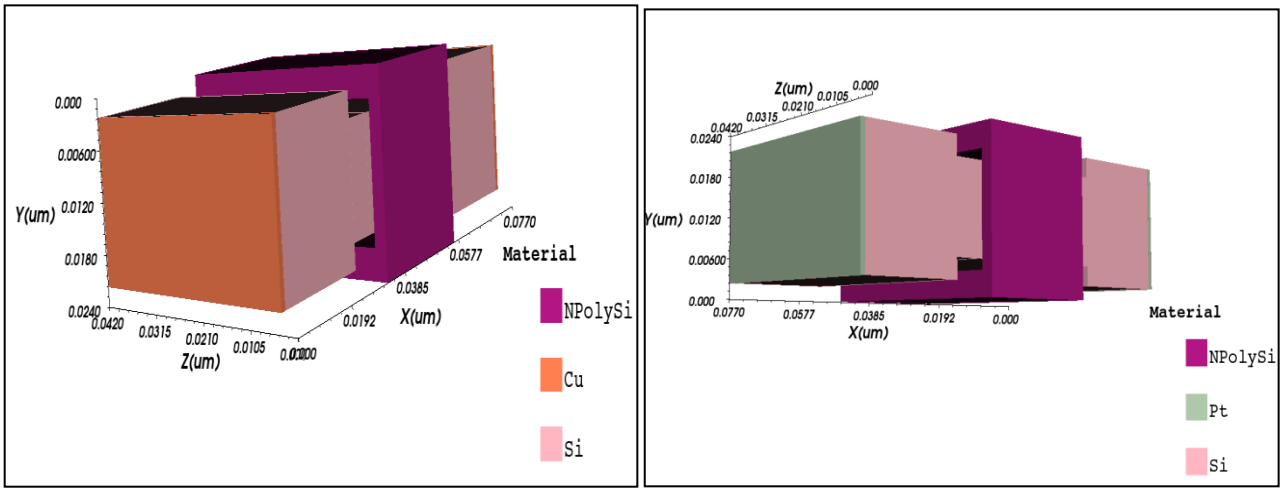


Fig 5.2 10nm FinFET with Copper and platinum as source and drain contacts

5.2.3 Surface Potential and Electric field:

Figure 5.4 shows the variation of an electrical field and surface potential with the application of gate to source voltage for SiGe based 10nm FinFET. As the gate voltage is increased from V_{gs}= 0V to V_{gs}= 1V, the electrical field increases. It is evident from the figure 5.4 that the potential at the source junction is low. While proceeding towards the drain junction, the surface potential increases. Moreover, the surface potential increases as gate-source voltage is increased.

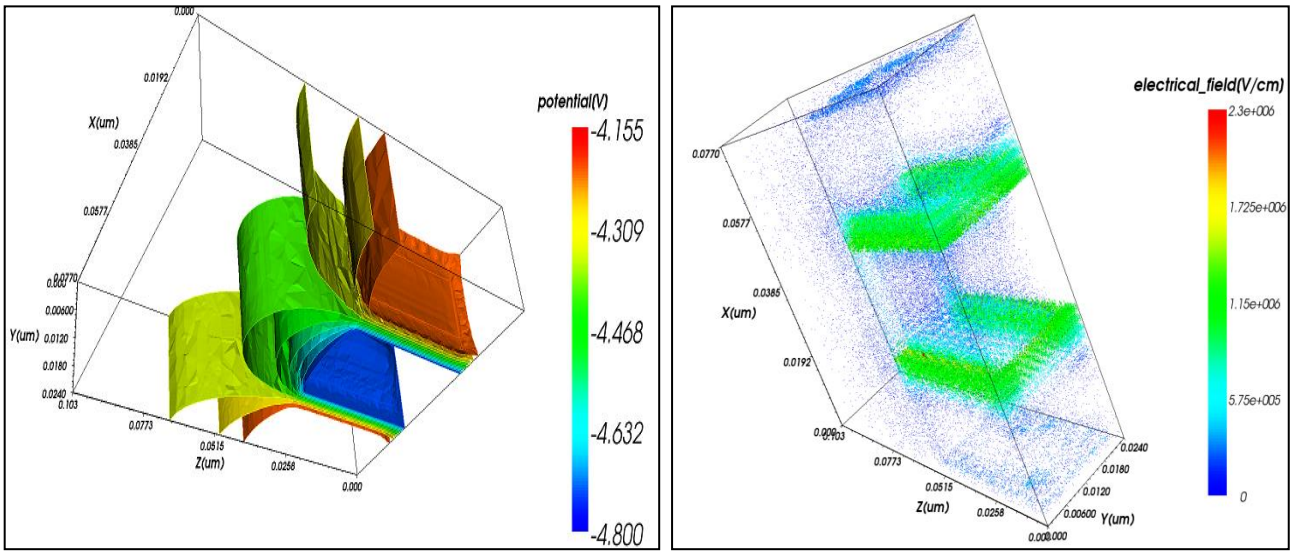


Fig. 5.3 Surface Potential and Electric field for SiGe based 10nm FinFET

Figure 5.3 shows the variation of an electrical field and surface potential with the application of gate to source voltage for 10nm FinFET with Copper as source and drain contacts. As the gate voltage is increased from V_{gs}= 0V to V_{gs}= 1V, the electrical field increases. It is evident from the figure 5.5 that the potential at the source junction is low. While proceeding towards the drain junction, the surface potential increases. Moreover, the surface potential increases as gate-source voltage is increased.

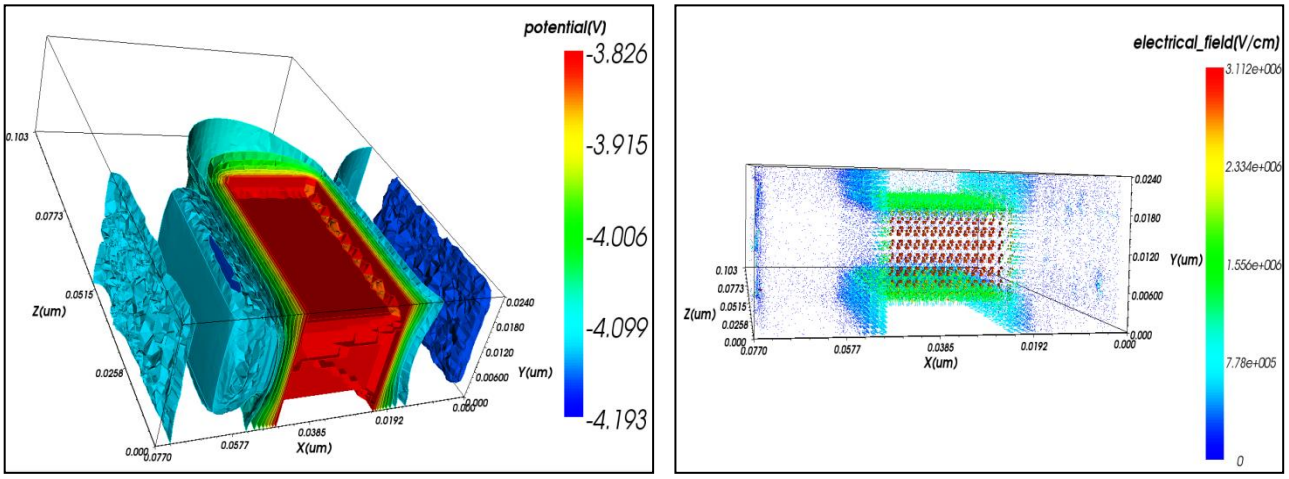


Fig. 5.4 Surface Potential and Electric field for 10nm FinFET with Copper as source and drain contacts

Figure 5.4 shows the variation of an electrical field and surface potential with the application of gate to source voltage for 10nm FinFET with Platinum as source and drain contacts. As the gate voltage is increased from V_{gs}= 0V to V_{gs}= 1V, the electrical field increases. It is evident from the figure 5.6 that the potential at the source junction is low. While proceeding towards the drain junction, the surface potential increases. Moreover, the surface potential increases as gate-source voltage is increased.

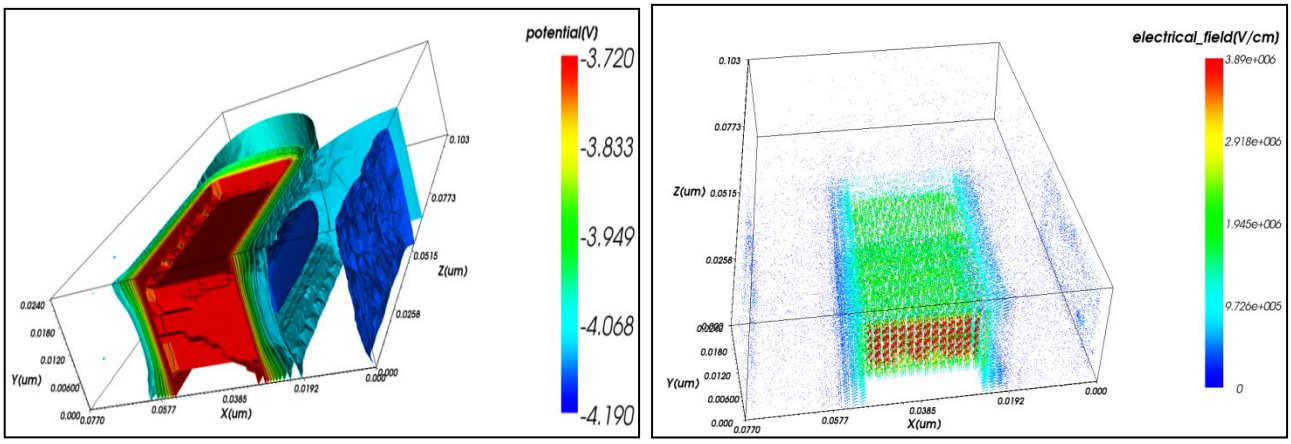


Fig.5.5 Surface Potential and Electric field for 10nm Fin FieldEffect Transistor with Platinum as source and drain contacts

5.2.4 Analysis of performance characteristics of 10nm Fin Field Effect Transistor with different contacts for source and drain materials:

In I_d-V_{gs} graph presented below in Fig.5.6, examination is made by Aluminum (Al) for the Source and drain substances by various contacts like Copper (Cu), Platinum (Pt). It is used as a metallic contact for copper source and can observe a growth in the drain I_{ON}/I_{OFF} ratio. Therefore it improves in different electric features, leads to a highly-stable Fin Field Effect Transistor device. The comparison of execution features for Source and drain substances at various contacts is given in the Table 5.1.

Metal contacts with various substances such as Al, Cu and Pt by various metal gate task operations were developed on 10nm Fin Field Effect Transistor. From simulations, as the metal gate task operation has been enhanced to high value, it presents respective development in the device's nature and therefore decreases OFF-state leakage current, which presents development in circuit execution.

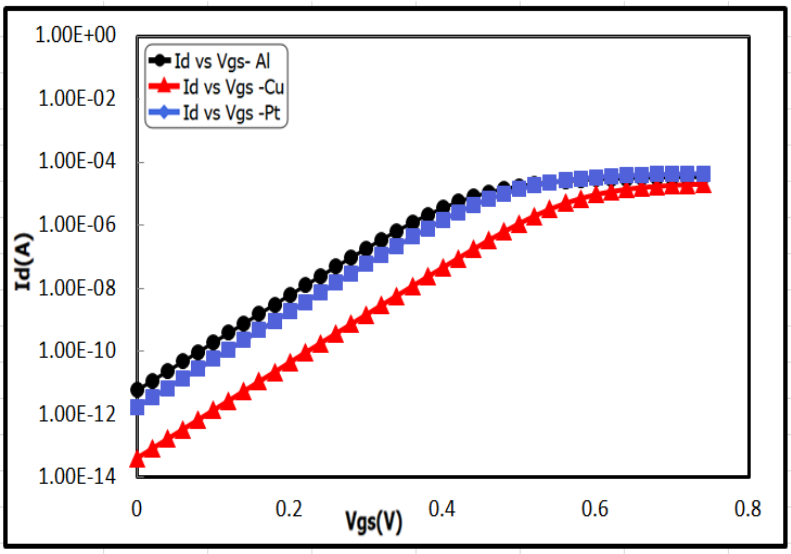


Fig. 5.6 I_d vs V_{gs} characteristics with different materials used for Source and Drain

Table 5.1 Performance characteristics of 10nm FinFET with different materials used for Source and Drain

Material used		Aluminum	Platinum	Copper
Performance Characteristics of 10nm FinFET	Threshold Voltage	0.5V	0.43V	0.58V
	Sub threshold Slope	72 mV/decade	74mV/dec	70 mV/dec
	I_{on}/I_{off} ratio	$4.34*10^8$	$25.60*10^8$	$50.84*10^8$
	DIBL	60.03mV/V	56.02 mV/V	53.36mV/V

5.2.5 Performance characteristics of 10nm FinFET analyzed with different dielectric values:

In Fig.5.8, I_d-V_{gs} graph is represented and it is noticed by growth in K value, with a development in the electrical parameters of the Fin Field Effect Transistor device. They have also examined the kind of substances utilized as gate dielectrics for the most effective use of the outputs. The simulations are taken by observing a gate dielectric formed with silicon dioxide (SiO_2), (low-*k* material, = 3.9), Hafnium oxide (HfO_2), (high-*k* material, *k* = 22) and a half loaded SiO_2+HfO_2 hetero dielectric gate substance.

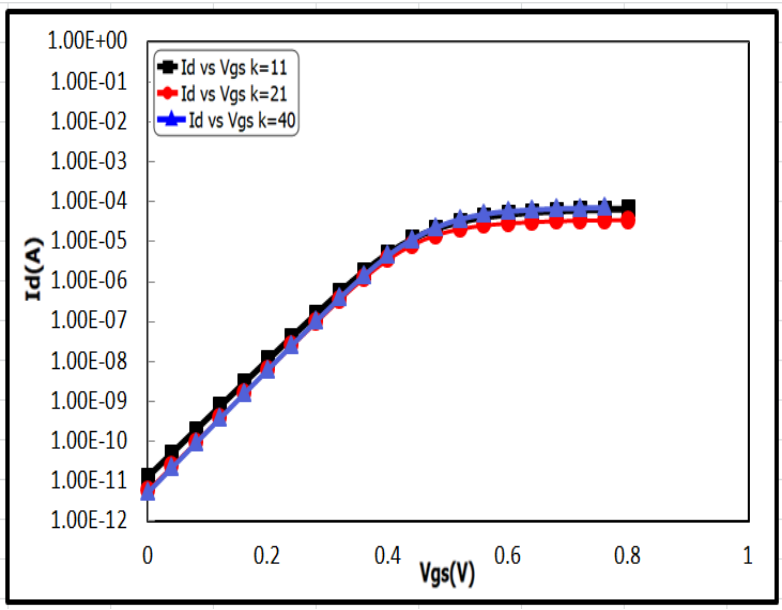


Fig. 5.7 I_d vs V_{gs} characteristics with different di-electric values

From the Figure 5.7, there is remarkable increase in I_{ON}/I_{OFF} ratio and power consumption got reduced with high K di-electric material in the FinFET. The leakage current is minimized due to static power consumption for FinFET at high K di-electric oxide material and the short channel effect can be minimized with the increase in K Value.

Figure 5.8 considers drain parameters to that difference in suggested framework, clearly showing that it is best at the moment when using the hetero dielectric gate material. The gate-source area of high-*k* substance is described by the overlap of the I_{ON}. However, the I_{OFF} is described by overlap of gate-drain area, with lower-*k* substance forming a tunneling circumstance that is hard to happen. Therefore, a better I_{ON}/I_{IOFF} ratio is acquired at 13.7×10^9 if using hetero dielectric gate material.

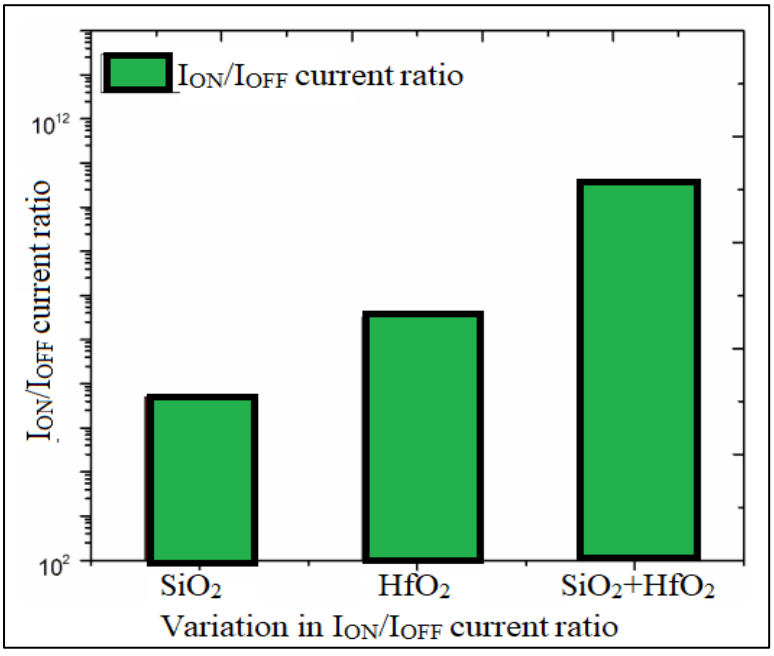


Fig 5.8 Variation in I_{ON}/I_{OFF} ratio Vs Oxides

Table 5.2 Performance characteristics of 10nm FinFET with different di-electric values

Dielectric constant		k=11	k=21	k=40
Performance Characteristics of 10nm FinFET	Threshold Voltage	0.4V	0.5V	0.42V
	Sub threshold Slope	80 mV/dec	72 mV/dec	70 mV/dec
	I_{on}/I_{off} ratio	$5.08x10^{7}$	$4.34*10^{8}$	$13.7x10^{8}$
	DIBL	64.06mV/V	60.03mV/V	56.22mV/V

The comparative analysis of various dielectric values execution features is evaluated and the table is calculated in Table 5.2. If the metal gate and semiconductor materials are situated within the dielectric, capacitance improves with an increase in the dielectric constant, K. Simultaneously; there is a notable reduction in power consumption, coupled with a significant improvement in the ION/IIOFF ratio, achieved by employing the highest-K dielectric material in the circuit. Static energy utilization decreases because of decreased leakage current for Fin Field Effect Transistor by high-k dielectric substance.

5.2.6 Analysis of Performance characteristics of 10nm FinFET with different Materials for Channel: In Fig.5.9, the I_d-V_{gs} graph represents and it is observed with Si, SiGe as materials for source and drain. There is growth in I_{ON}/I_{IOFF} ratio of the FinFET device modelled with SiGe as channel. It is evident that I_{ON}/I_{IOFF} ratio for SiGe based 10nm FinFET is comparatively large when compared to the FinFET with only Si.

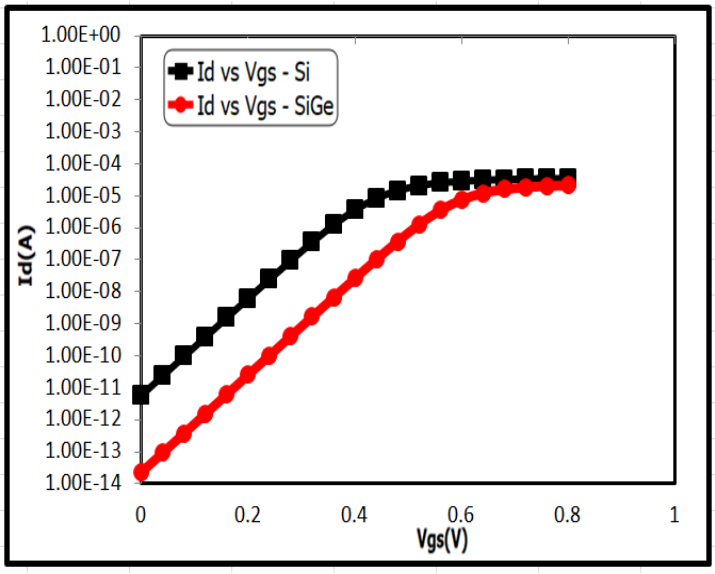


Fig. 5.9 I_d vs V_{gs} characteristics for SiGe and Si based 10nm FinFET

Table 5.3 Performance characteristics for SiGe and Si based 10nm FinFET

Materials used		Si	SiGe
Performance Characteristics of 10nm FinFET	Threshold Voltage	0.5V	0.58V
	Sub threshold Slope	72 mV/dec	52.5 mV/dec
	I_{on}/I_{off} ratio	$4.34*10^8$	$1.09*10^9$

The comparative analysis of performance parameters of SiGe and Si based 10nm FinFET is calculated and tabulated in table 7.3 It is observed that there reduction in power consumption and subthreshold slope for 10nm FinFET with SiGe as source and drain for high performance FinFET

5.2.7 Analysis of Performance characteristics of 10nm FinFET with different materials for Gate:

In Figure 5.10, I_d-V_{gs} graph, it is observed that there is an increase in I_{on}/I_{off} ratio of the FinFET device modelled with Electrode as Gate material when compared to N and P Poly silicon. The performance characteristics of different k outputs are assessed through a comparative analysis, and the corresponding values are presented in Table 5.4. It is observed that there is reduction in power consumption and subthreshold slope for 10nm FinFET with Electrode as Gate material for high performance FinFET. It is clearly noticed that the I_{ON}/I_{IOFF} ratio is greater for 10nm FinFET with Electrode as a gate material when compared to other materials.

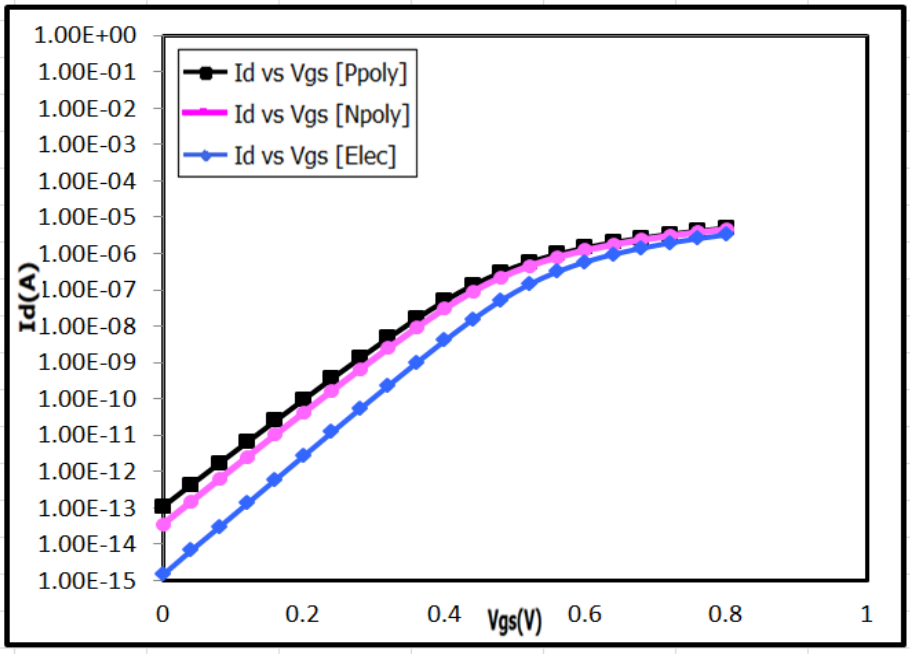


Fig. 5.10 I_d vs V_{gs} characteristics of 10nm FinFET with different Gate materials

Table 5.4 Performance characteristics of 10nm FinFET with different Gate materials

Materials used		P poly	N poly	Elec
Performance Characteristics of 10nm FinFET	Threshold Voltage	0.32V	0.5V	0.57V
	Sub threshold Slope	87.7 mV/dec	72 mV/dec	56.4 mV/dec
	I_{on}/I_{off} ratio	$1.17*10^6$	$4.34*10^8$	$1.02*10^9$

5.3 Chapter Conclusion: Hence to conclude, a 10nm triple-gate Fin Field Effect Transistor model is analyzed for minimum energy and high subthreshold execution. By using Cogenda Visual TCAD, the device 10nm triple-gate FinFET is designed, examined and simulated. The device performance optimization is done by analyzing drain current characteristic at various metal contacts for Source , drain and gate for the proposed 10nm Triple gate Fin Field Effect Transistor. The proposed device has shown appreciable improvement in the I_{ON}/I_{IOFF} ratio up to 10^{10}. The electrostatic nature is evaluated which include electric behavior, surface capability, electron and hole density characteristics from circuit framework that are presented. Now, to move on to the next level of applications of FinFET, 18nm triple gate FinFET for biomedical applications at low power is analyzed by various charged and neutral bio molecules in the coming chapter.

CHAPTER 6: 18nm TRIPLE GATE FINFETAS BIOSENSOR

6.1 Introduction:

Massive advances in Nano-electronics is an attraction for researchers to improve the most recent circuits for a variety of applications. Rising capabilities in emerging micro- and nanoscale biology technologies enable the development of next-generation biosensors with higher sensitivity and lower cost. With greatly improved methods, advanced biosensors can detect foreign and harmful toxins . Nanoscale biosensors are also very scalable and portable, making them ideal for examination and real-time detection. A variety of biosensors based on Field Effect Transistors devices are currently being improved and used in a variety of biomedical applications. A biological sensor is a system that detects and converts changes in its biological environment into a readable signal. The output of a biological sensor must be sensitive and specific. Estimations and examination of various aspects of a single cell are critical for absolute and clear understanding of heterogeneous cell populations. [111].

At the moment, higher throughput single molecular sensing is getting more popularity as a way to improve and enable important approaches in life sciences. Researchers believe that CMOS compatible silicon bio-FET sensors have demonstrated electrical sensing of various biomolecules with varying potentials within their scope. The SNR of a single molecule should be high enough to reduce bio-sensing to a single-molecule step. The main reason for increasing single-molecule SNR is to reduce device space.

Shortening the silicon FET gate length is critical not only for single-molecule detection but also for achieving high sensor mass and, as a result, throughput. When compared to the effects of DG Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) and conventional MOSFET exhibit higher I_{ON}/I_{OFF} ratio, bottom subthreshold swing, and immunity to short channel. FINFETs are those devices which have the most promising results, are one of several self-aligning mechanisms and frameworks that have been suggested to optimize the performance of double-gate devices. Due to their photosensitivity and compatibility with integrated circuits, FETs are now more suitable for use as photo detectors. [112].The specific interaction between the receptor and ligand is converted into an electric signal by a field effect transistor.

In a conventional FET biosensor model, the gate area of FET directly interacts with the receptor on the semiconductor channel area or gate metal. Transistor drain current is directly modulated by modifications in the forward receptor-ligand binding, in a manner similar to how a gate voltage is applied to control channel conductance. [113]

FinFETs are suitable for integration with detecting and readout devices on a related substrate because of their subthreshold swing and the fact that the I_{ON}/I_{OFF} ratio does not suffer from scaling. FET is a good design because of its superior architecture. In addition to other areas, it has observed techniques in electrical properties, mobile technology, digital Integrated Circuits (IC), gas, temperature, pH sensors, and biosensors. It can play a significant part in quick clinical detection due to its high sensitivity and versatility in analytical tests. The various biomolecules found in human bodies are made up of neutral biomolecules like biotin, streptavidin, keratin, glucose, and glutamine as well as charged biomolecules like deoxyribonucleic acid and ribonucleic acid. [114]

The Silicon-On-Insulator (SOI) wafers used for the Silicon-NW array sensors have a top layer of p-type silicon that is 55 nanometers wide and doped with boron (8-12 cm). A typical mainstream FinFET serves as the foundation of the mechanism. The width above the silicon was first reduced to thirty nanometers using sacrificial oxidation, and then SiO_2 was extracted using Diluted Hydro Fluoric acid (DHF). The multi-layer SiO_2/amorphous Si (-Si)/ Si_3N_4 was subsequently sequentially arranged after that.[115]

After that, hot H_3PO_4 solution was used to extract the top Si_3N_4 Hard Masks (HMs). A Si_3N_4 film with a width of 30 nm is placed, and the proper Si_3N_4 Reactive Ion Etch (RIE) is used to create the spacer. HM arrays of nanometer-sized Si_3N_4 spacers were then kept on top of the SiO_2 films after the inner core -Si material between the two Si_3N_4 spacers was extracted using Tetra Methyl Ammonium Hydroxide (TMAH). After using RIE methods of oxide and an ultra-thin silicon upper surface, arrays of Silicon NW were later produced by removing the top hard masks with diluted hydrofluoric acid. [116].Later, electrodes are formed using a negative resist method, and lift-off sputtering is used to deposit 100 nm wide Ti/Au layers.

Electrodes are spaced up to 2 mm apart to separate sample investigations from cell drops. To ensure signal recording at high sensitivity liquid conditions, an Atomic Layer Deposition (ALD) method was used to create a conformal 10 nm wide biocompatibility of the most-dielectric constant HfO2 surface. Non-invasive MSC recording is possible if the cells adhere better and the area of the Silicon nanowire detectors [117].

The Si flow cell was used in the Bio-Field Effect Transistor tests. Polytetrafluoroethylene (PTFE) and PolyVinyl Chloride (PVC) tubing connects cells to an electrolyte gate device's flow-by silver/AgCl reference electrode. A glass syringe is typically used to replace electrolyte fluid in cell flow (Figure. 8.2). In a probe station, a flow cell is used to electrically distinguish the Field Effect Transistor senso. [118, 119]

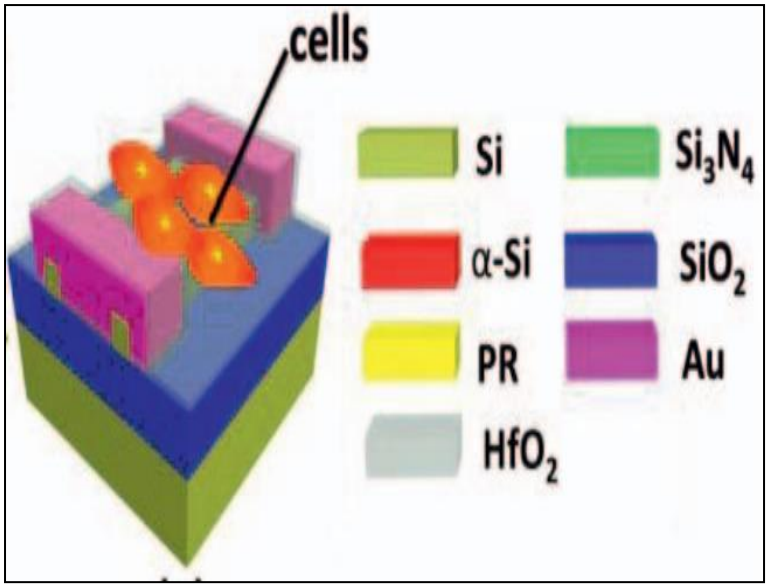


Fig. 6.1: Introduce cells adherence to the Hfo_2 dielectric surface

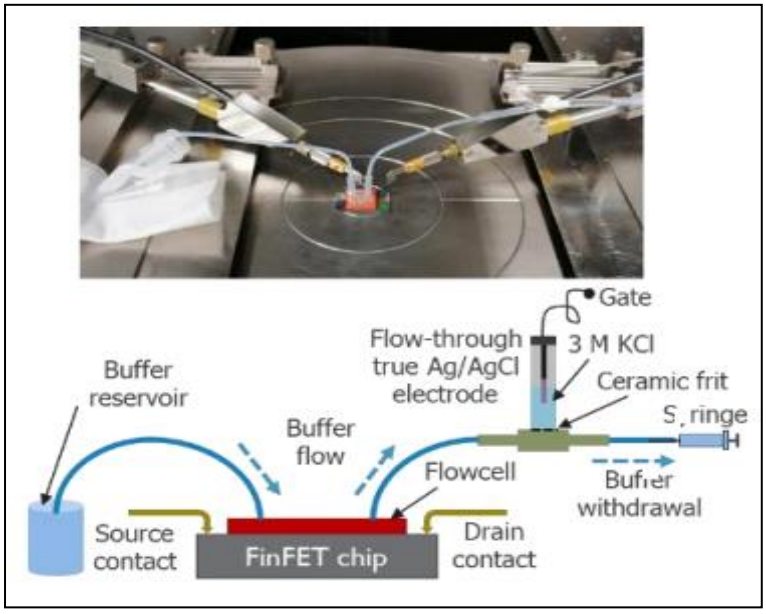


Fig. 6.2: Electrical setup illustrating the fluidic flow path and Ag/AgCl electrolyte gate contact

A close-complete median with V_T swing of 65 mV/dec up to 70 nm establishes the highly standard electrolytic gated FinFET. The average subthreshold voltage is around -0.3 Volts. For devices with a gate distance of 50 nm, V_T roll-off occurs due to the high VT swing and short-channel impacts. Because of the best electrostatic control, systems with smaller widths (13 nm) have less influence from short-channel effects on I_d-V_{gs} aspects. [119]

6.2 Methodology:

Arrays of highly uniform Si-NW with a thickness of 13nm are generated without any landing pads, which are suitable for integrating high Silicon nanowire sensors or achieving small system dimensions. Figure 6.3 shows a cross-sectional Transmission Electron Microscope (TEM) image of a Silicon Nanowire (NW) sensor.

A highly conformal and constant HfO_2 surface is observed, which contributes to better separation between the electrodes and the solution condition [120].

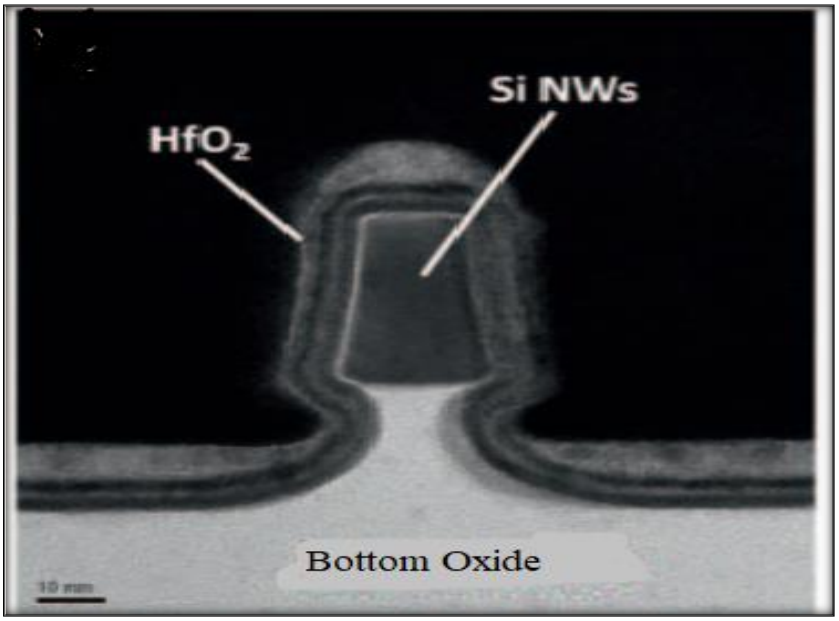


Fig. 6.3: Cross Sectional TEM Image of Si Nanowires Sensors, Conformal and Uniform HfO_2 Layer [120]

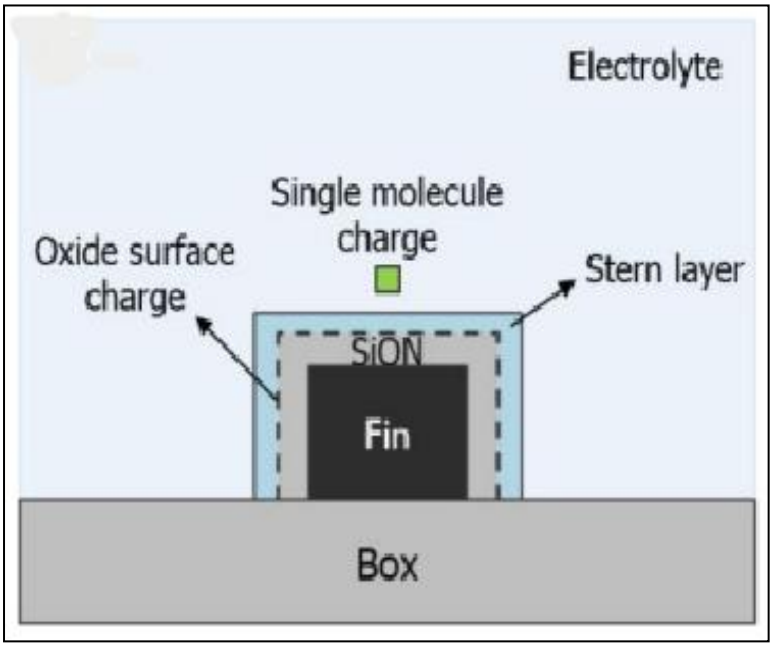


Fig.6.4: Schematic of the Cross Section of the FinFET Sensor used for the simulation of the Single-Molecule Signal-2D

In the simulations, electrolyte screening is determined by the Bickermann system, which employs modified Poisson-Boltzmann equations to design steric impacts and also assumes the Stern layer and it even takes into account the pH-dependent oxide surface charge.

For sub-70 nm Field Effect Transistor detectors in 1.5 mm PBS, a signal of 3 milli Volts is required, resulting in a Signal to Noise Ratio greater than 5, which is a better perspective for achieving single-molecule sensing with bio-Field Effect Transistor.[120]

6.3. Performance evaluation of 18nm triple gate FinFET using Visual TCAD tool:

A high doping profile at these junctions is needed to scale semiconductor devices under 20 nm. This gives the effects of simulations for a unique shape of FinFET for high-pace packages with germanium composition and gate and supply/drain connections. According to benchmarking statistics, while the present day density of FinFETs grows, the fast-channel behaviour improves. FinFETs with a excessive factor ratio provide extra present day according to unit vicinity with fewer horizontal geometry constraints, making them appropriate for occasions when conventional scaling has reached its bodily limits. The proposed FinFET at the 18 nm era node will increase low-energy and excessive-frequency performance, in line with the findings of the rigors.

Table 6.1: Physical parameters of 18nm FinFET as Biosensor

PARAMETER	DIMENSION
Channel length [L_{ch}]	18nm
Length of cavity[L_{cav}]	8nm
Drain, Source length [L_D , L_S]	3.5nm
SiO_2 thickness [T_{ox1}]	2.8205nm
HfO_2 thickness [T_{ox1}]	2.8205nm
Fin thickness [T_{fin}]	4nm
Channel doping concentration, N_{Ch}	1e+15/cm^3
Doping concentration, N_{Sd}	1e+18/cm^3

Table 6.1 details about the physical parameters of proposed 18nm triple gate FinFET architecture, that is used for bio sensing the bio molecules after introducing in to the cavity.

Table 6.2 details about the biomolecules Biotin, Keratin, Zein, Gluten, and Streptavidin with their bio thickness, bio permittivity are mentioned. These are induced into the air cavity of 18nm triple gate FinFET instead of oxide layer, to serve as a bio sensing element. By analyzing performance metrics like threshold voltage and the I_{ON}/I_{IOFF} ratio by varying different cavity lengths for better FinFET performance, the nature of the device can be determined with the introduction of bio molecules with different di electric constants and charges.

Table 6.2: Thickness and permitivity of Biomolecules

Biomolecules	Bio Thickness (T_{bio})	Bio Permitivity ($€_{bio}$)
Biotin	0.6nm	2.63
Streptavidin	6.1nm	2.1
Zein	-	5–7
Gluten	-	7
Keratin		8–10

6.3.1 Proposed 18nm FinFET 3D architecture:

Proposed 18nm triple gate FinFET is designed by using Visual TCAD simulation tool with Electrode as gate material, SiO_2 , HfO_2 as oxide materials and Nitride as spacers for high performance and low power applications as shown in the figure 6.5.

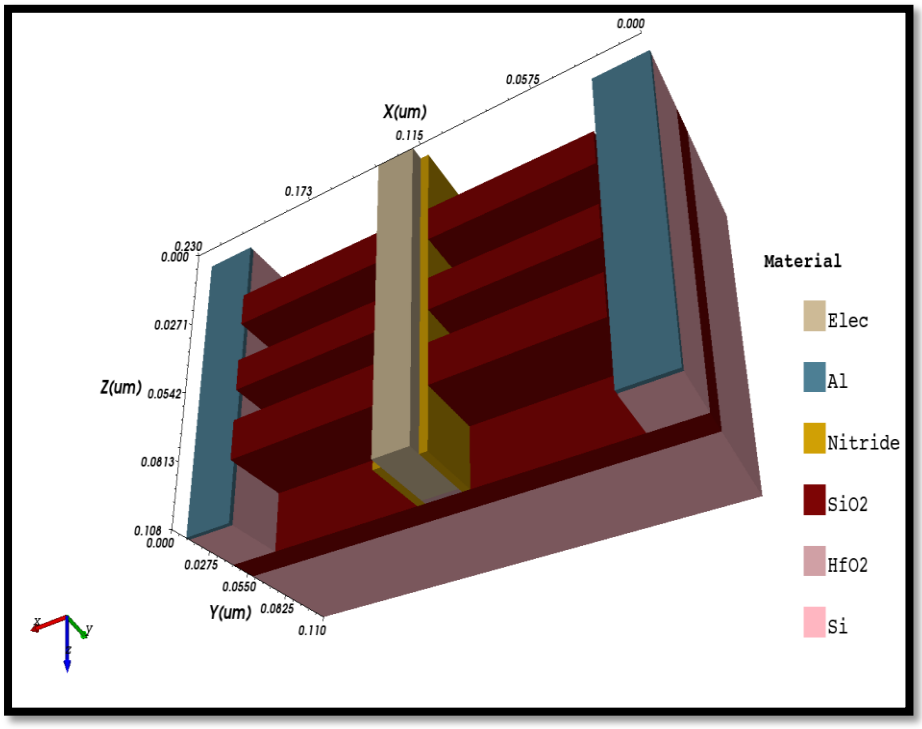


Fig. 6.5 3 fin structured triple gate 18nm FinFET with electrode as gate material and nitride as spacers.

6.3.2 3D structure of Cylindrical Nano wire: Figure 6.6 is the structure of Nano wire as Bio Sensor by introducing the bio molecules such as Biotin, Keratin, Zein, Gluten, and Streptavidin are biomolecules introduced in the air cavity that act as bio sensing element.

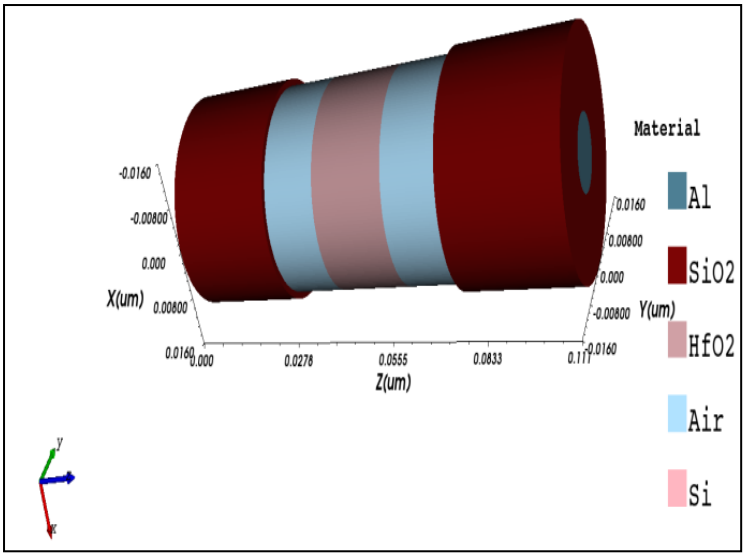


Fig 6.6 Cylindrical shaped Nanowire as biosensor

6.3.3 Performance parameters of proposed cylindrical Nano wire:

It is of the order 10^{-4} A for K = 10, established at V_{gs} =1 Volts, and I_{OFF} is measured at V_{gs} =0 Volts, V_{ds} =1 Volts, as can be seen in Fig. 6.11 and Table 6.3

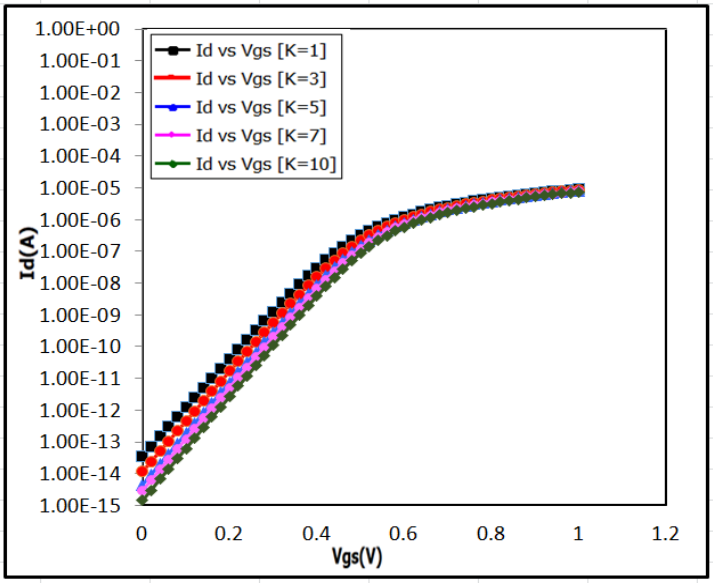


Fig. 6.11 Application of different bio molecules on Nano wire for cylindrical gate

Table 6.3 Application of different bio molecules on Nano wire for cylindrical gate

Di electric materials used		K=1	K=3	K=5	K=7	K=10
Performance Characteristics of 18nm FinFET	Threshold Voltage	0.3V	0.32V	0.34V	0.37V	0.44V
	Sub threshold Slope	75.4 mV/dec	63.5 mV/dec	61.9 mV/dec	58.6 mV/dec	50.2 mV/dec
	I_{ON}/I_{OFF} ratio	$1.19*10^8$	$3.06*10^8$	$1.32*10^9$	$5.03*10^9$	$7.86*10^9$

6.3.4 Proposed 18nm FinFET biosensor architecture:

Figure 6.7 is an 18nm FinFET device with oxide layers of SiO_2 and HfO_2. Biomolecules such as biotin, keratin, zein, gluten, and streptavidin are introduced as bio sensing elements. The device's nature can be determined by varying different cavity lengths for FinFET performance and evaluating performance parameters such as threshold voltage and the I_{ON}/I_{IOFF} ratio.

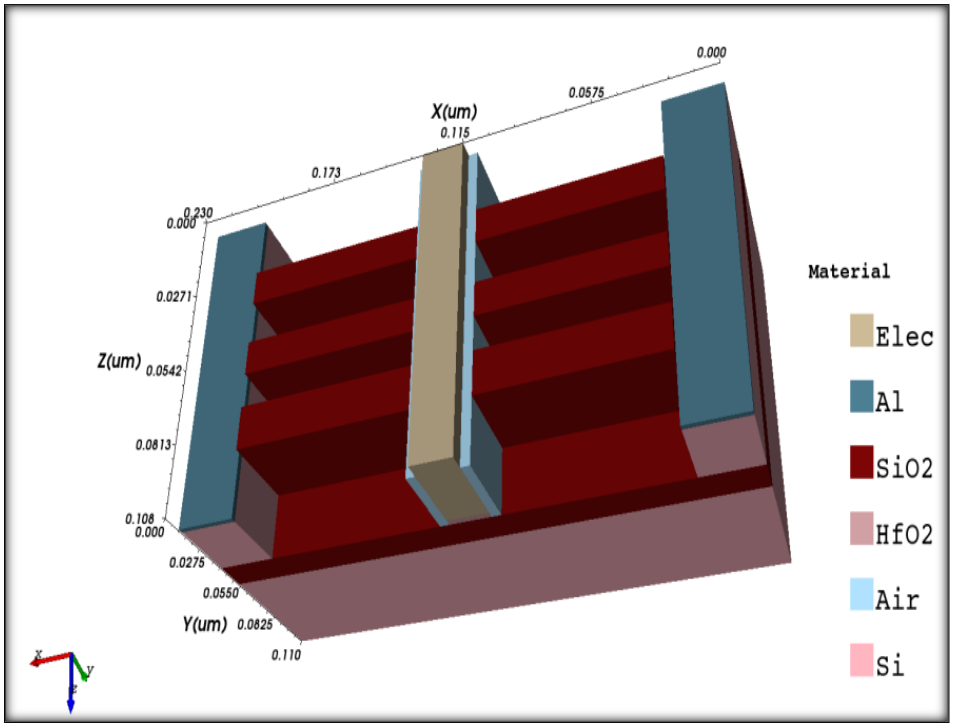


Fig 6.7 Triple gate 18nm FinFET as biosensor

6.3.5. Performance parameters of proposed 18nm triple gate FinFET biosensor:

Figures 6.8 for charged and neutral analytes that affect the positioned area, respectively, show the drain parameters of the proposed biosensor.

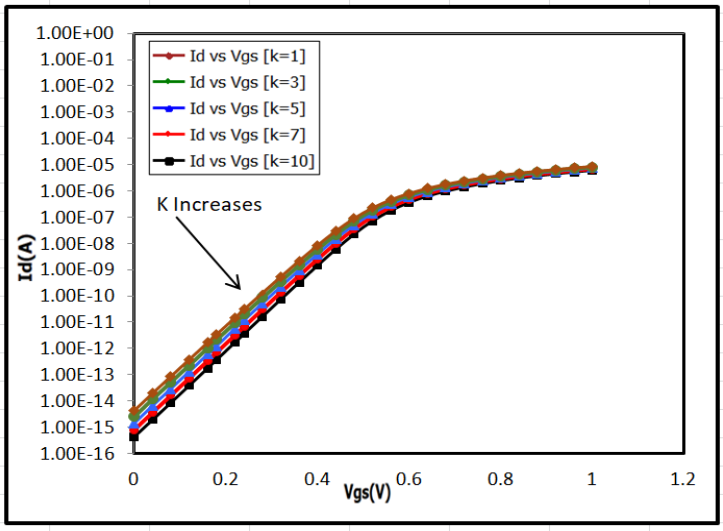


Fig 6.8 I_d-V_{gs} characteristics with various biomolecules of 18nm triple gate FinFET-based biosensor for different neutral biomolecules

When neutral biomolecules like biotin are later immobilized, the I_{OFF} abruptly decreases from 10^{-13} A/µm to 10^{-16} A/µm along with a slight change in ON current.

From the below Table 6.4, It is evident that I_{ON}/I_{OFF} ratio is increased from the order of 10^8 to 10^9. Also SCEs are predominantly reduced with the reduction in subthreshold slope. Also Maximum performance of the device as Bio Sensor is observed when the Keratin bio molecule is introduced with K= 10. The nature of the device is analyzed by evaluating performance parameters like threshold voltage, the I_{ON}/I_{IOFF} ratio by varying different cavity lengths for better FinFET performance. Figure 6.8 is an 18nm FinFET device, where the oxide layers of SiO_2 and HfO_2 are replaced with the biomolecules such as biotin, keratin, zein, gluten, and streptavidin to convert the device into bio-sensing device. The device's performance can be determined by varying different cavity lengths for triple gate FinFET and evaluating the performance parameters such as threshold voltage and the I_{ON}/I_{IOFF} ratio for high performance.

Table 6.4 Application of different neutral bio molecules on 3 fintriple gate 18nm FinFET with respect to di-electric constant

Materials used		K=1	K=3	K=5	K=7	K=10
Performance Characteristics of 18nm FinFET	Threshold Voltage	0.36V	0.4V	0.42V	0.43V	0.46V
	Sub threshold Slope	72.5 mV/dec	68.5 mV/dec	60.5 mV/dec	55.6 mV/ dec	50.8 mV/ dec
	I_{ON}/I_{OFF} ratio	$3.07*10^7$	$7.24*10^8$	$3.32*10^9$	$6.03*10^9$	$9.24*10^9$

The distance to the cavity is 5 nm. Effective gate control in the channel lowers I_{OFF} because the channel's carriers are severely depleted. Similarly, I_d-V_{gs} parameters are shown in Fig. 6.12 for suggested biosensors with neutral and charged analytes in the cavity area. From $1*10^{12}$ C/cm^2 to $2*10^{12}$ C/cm^2 are the positivity charges. I_{OFF} is seen to rise as positively charged molecules are shut down in the cavity region of the proposed n-type biosensor. This is due to decreased gate control over the channel and decreased width of the charged region in the channel's center. The I_{OFF} also increases for negatively charged molecules changing from - $2*10^{12}$ C/cm^2 to -10^{12} C/cm^2 at a constant dielectric constant. The same can be observed from the Table 6.5.

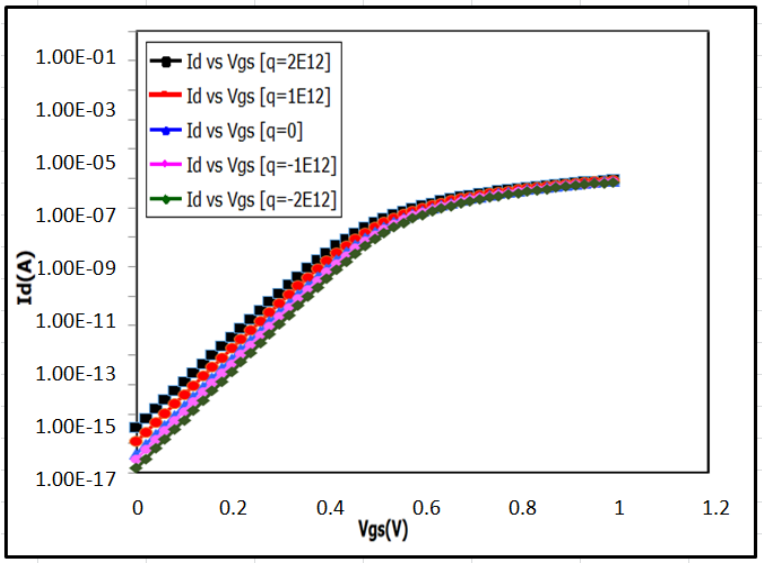


Fig 6.9 I_d-V_{gs} characteristics with various biomolecules of 18nm triple gate FinFET-based biosensor for both positive and negative charged biomolecules

Table 6.5 detailed about the performance parameters of 18nm triple gate FinFET, that has shown appreciable performance as the positive charge is introduced. I_{ON}/I_{OFF} ratio is increasing from the order of 10^7 to 10^9 as it moves from negative to positive charge.

Table 6.5. Application of different bio molecules on 3 fin triple gate 18nm finfet with respect to positive and negative charges

Materials used		q = 2E12	q = 1E12	q = 0	q = -1E12	q = -2E12
Performance Characteristics of 18nm FinFET	Threshold Voltage	0.3V	0.32V	0.44V	0.45V	0.45V
	Sub threshold Slope	64.4 mV/ dec	58.5 mV/ dec	50.2 mV/ dec	47.6 mV/ dec	46.2 mV/ dec
	I_{ON}/I_{OFF} ratio	$9.11*10^7$	$3.87*10^8$	$9.86*10^8$	$4.03*10^9$	$8.89*10^9$

Figure 6.10 is the 3 fin structured Triple gate FinFET, where the oxides are completely replaced with the air cavity. And therefore, there is a provision to introduce the bio molecules more effectively so as to improve the performance of the device that has been proposed as Bio Sensor. Also the noise and SCEs are suppressed with high K di-electric value at 10 of the Keratin molecule with the cavity length 5nm.

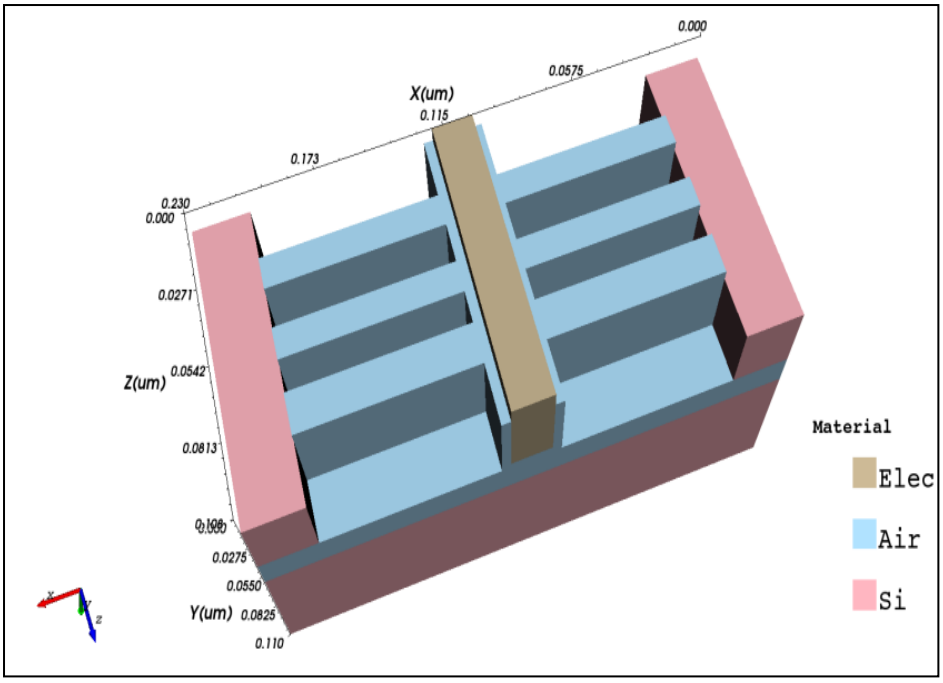


Fig 6.10 3 fin structured triple gate 18nm FinFET as biosensor

Figure 6.11 shows the interactions between the drain parameters of the biomolecules for both charged and neutral analytes in a specific region and demonstrates that the I_{OFF} abruptly decreases from 10^{-14}A/µm to 10^{-18}A/µm when neutral biomolecules with dielectric constants of 1 to K >1 are subsequently immobilized, while the I_{ON} experiences only minor changes of the order of 10^{-7} A.

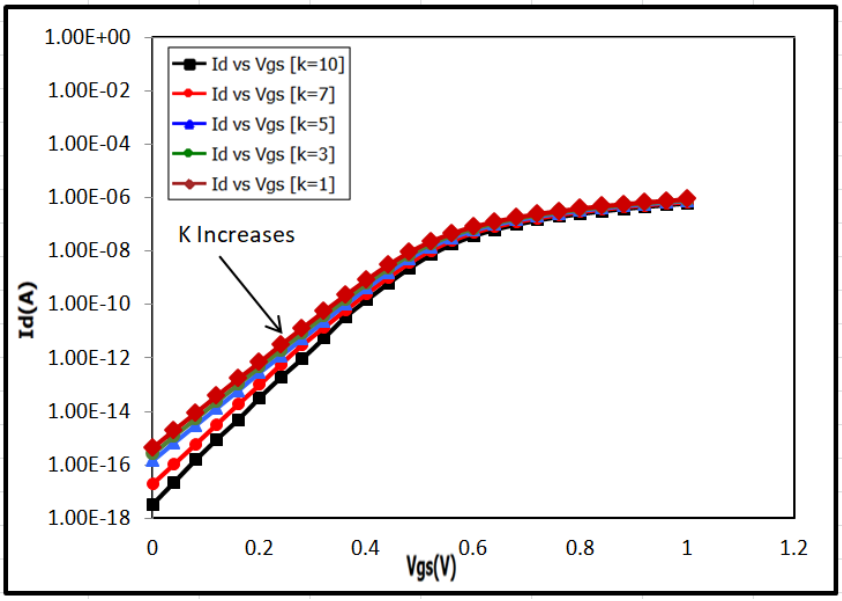


Fig 6.11 I_d-V_{gs} characteristics with various biomolecules of 18nm triple gate FinFET-based biosensor with air cavity for different neural biomolecules

For a dielectric constant of 10, the ON current is measured at V_{gs}=0 Volts at V_{ds}=1 Volts, and the IOFF is observed at V_{gs}=1 Volts. Cavities are separated by 5nm. Effective gate control on the channel lowers the IOFF because the channel's carriers are severely depleted.

Table 6.6 Application of different neutral bio molecules on 3 fin triple gate 18 nm finfet with respect to di-electric constant

Materials used		K=1	K=3	K=5	K=7	K=10
Performance Characteristics of 18nm FinFET	Threshold Voltage	0.36V	0.4V	0.42V	0.44V	0.48V
	Sub threshold Slope	69.4 mV/ dec	58.5 mV/ dec	57.4 mV/ dec	50.6 mV/ dec	48.2 mV/ dec
	I_{ON}/I_{OFF} ratio	$4.17*10^{7}$	$1.09*10^{9}$	$3.32*10^{9}$	$1.03*10^{10}$	$9.16*10^{10}$

Figure 6.12 also displays the I_d-V_{gs} parameters of the suggested biosensors with neutral and charged analytes in the cavity area. Positive charges range from $1*10^{12}$ C/cm^2 to $2*10^{12}$ C/cm^2. The amount of IOFF is observed to increase as the quantity of positively charged molecules increases if the cavity area of the proposed n-type biosensor is disabled due to a thinner gate regulator over the channel and a thinner gate charged region in the middle. Thus it is clearly showing that the IOFF is increased for molecules with negative charges between - $2*10^{12}$ C/cm^2 and -10^{12} C/cm^2 at a constant K of 10.

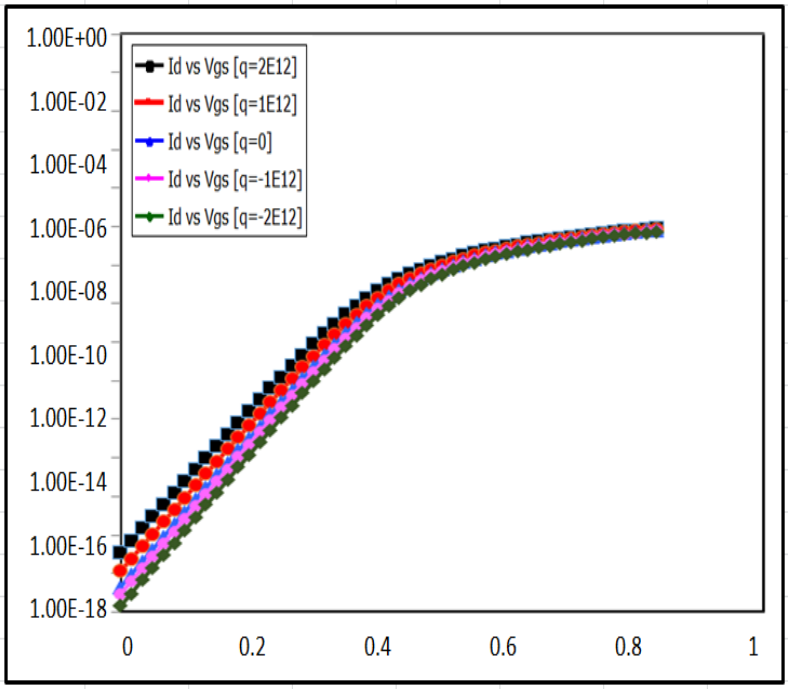


Fig 6.12: I_d-V_{gs} characteristics with various biomolecules of 18nmtriple gate FinFET-air cavity-based biosensors for charged and neutral biomolecules

Table 6.7 Application of different bio molecules on 3 fin triple gate 18nm finfet with respect to positive and negative charges

Materials used		q=2E12	q=1E12	q=0	q= -1E12	q=-2E12
Performance Characteristics of 18nm FinFET	Threshold Voltage	0.34V	0.36V	0.40V	0.44V	0.44V
	Sub threshold Slope	69.4 mV/ dec	62.5 mV/ dec	55.2 mV/ dec	50.6 mV/ dec	48.8 mV/ dec
	I_{ON}/I_{OFF} ratio	$7.67*10^8$	$2.48*10^8$	$5.65*10^9$	$9.63*10^9$	$4.18*10^{10}$

Figure 6.15 shows how the I_{ON}/I_{IOFF} ratio is affected by different cavity lengths—5 nm, 7 nm, and 10 nm—with various dielectric constants, depending on the biomolecule introduced. For 18nm triple gate FinFETs, it is discovered that the I_{ON}/I_{IOFF} ratio is rising as the cavity length shrinks from 10nm to 5nm. The biomolecule Keratin, with a dielectric constant of K = 10, exhibits extremely low I_{IOFF} for a 5 nm cavity length in comparison to other biomolecules. Therefore, it is abundantly clear that the I_{ON}/I_{IOFF} ratio is higher for shorter cavity length for all the different biomolecules introduced. The increase in I_{ON}/I_{IOFF} ratio with shorter cavity length is due to charge analytes being closer to the channel's middle, and thus the capability barrier being most affected by high capacitive impact.

6.3.6 Electrostatic behavior of 18nm Triple gate FinFET as Biosensor:

The electric field strength variation through the channel's middle is depicted in the figure below in a straight line. This states that the rolled gate 3D Fin Field Effect Transistor's average electric field is stronger for the cylindrical shape.

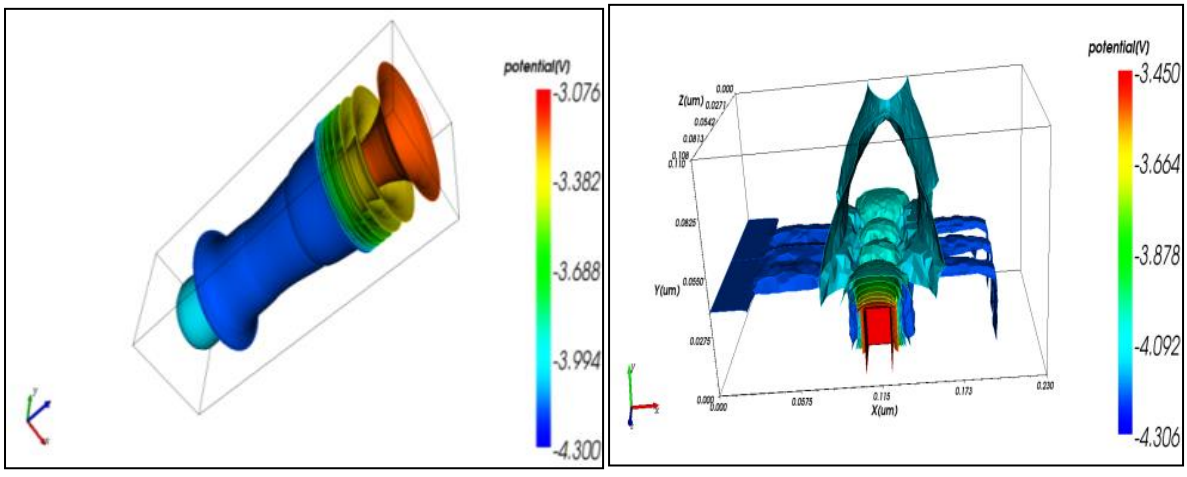


Fig 6.13 3D view of potential for Nano wire and triple gate FinFET

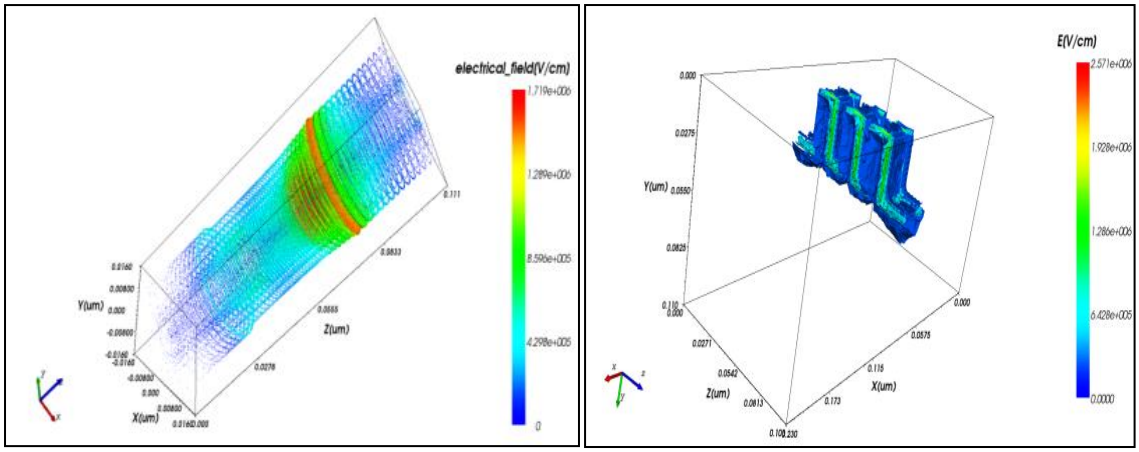


Fig 6.14 3d view of electric field(v/cm) for cylindrical shaped gate nano wire and 18nm triple gate FinFET

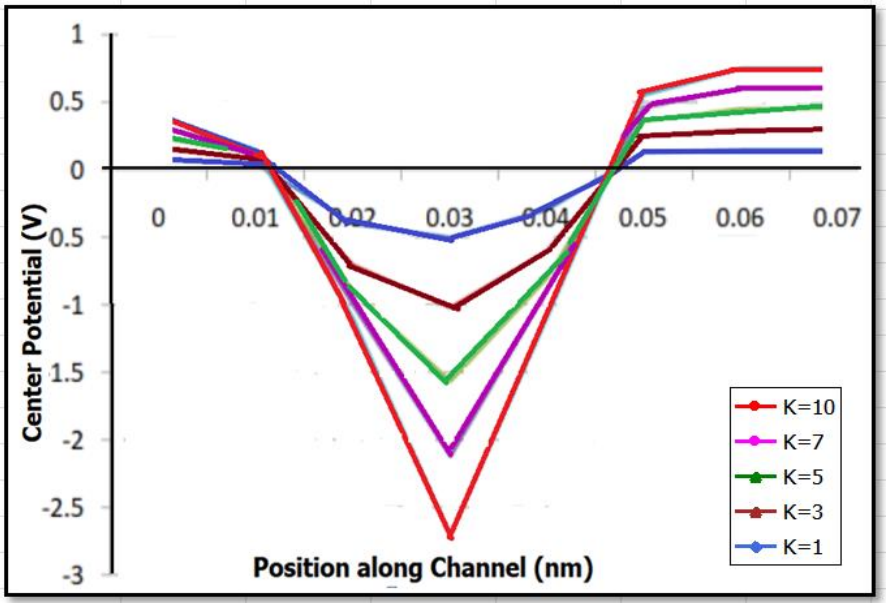


Fig. 6.15 Central Potential varying along with the channel for Neutral bio-molecules

This section investigates the difference in the proposed biosensor's middle capability in the channel as K changes for neutral and charged bio-molecules. Figure 6.16 depicts the middle capability of the channel if the cavity is free from the biomolecules, indicating that any of the molecular elements are stable in the cavity area. In that case, the middle capability of the channel along with the source and drain increases by 0.5 and 1.5 Volts, respectively.

When the capability of the centre is examined to interact locally on enhancing dielectric constant (K), it meets a minimum of -0.53 Volts. This is done to increase gate capacitance by increasing K in the cavity area, thereby increasing the vertical electric region.

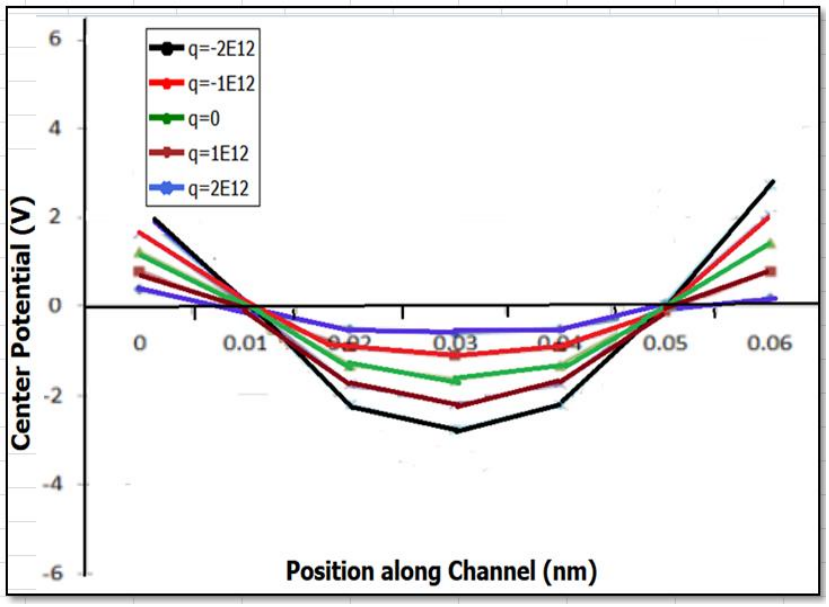


Fig. 6.16 Central Potential varying along with channel for charged bio-molecules

This denotes an increase in coupling between the gate and the channel, which has shown in a Figure 6.16 presents the central potential including the location of channel for positively and negatively charged bio-molecules. If the cavity is completed by charge analytes, it is noticed that centre capability reduces for the negatively charged analytes. The centre potential is accurately -0.82 Volts for q=0 C/ cm^2 and −3.36 Volts for q= -2 × 10^{12} C/cm^2. The cause is beyond enhancement in flat band voltage from q_{Nf}/C_{eff}, which reduces the centre potential. This implies further exhaustion in the channel space, leading to higher regulator of gate. For positively charged bio-molecules, the centre potential is high at -4.2 V, because of better performance among the charges in the cavity and the channel. A high centre capability indicates an exhaustion of charge in channel and hence represents the gate regulator that lowers the V_{th}.

Threshold voltage and I_{ON}/I_{OFF} Ratio at different cavity lengths of 18nm Triple Gate FinFET

The below mentioned Table 6.8 briefs the performance of 18nm triple gate FinFET that acts as biosensor with high performance for low power applications for different bio molecules with different cavity lengths with the performance parameters such as threshold voltage and I_{ON}/I_{OFF} ratio. It is observed that the Bio molecule Keratin with di-electric constant K is equal to 10 with cavity length of 5nm is showing remarkable performance with high I_{ON}/I_{OFF} ratio of 9.16*10^{10} with appreciable threshold voltage. Another observation from the above graph that for K = 10, the V_{th} is also high for less cavity distance, which causes the execution aspects to develop. All four areas of the nano gap cavities have I_{OFF} outputs and bio-molecule ordering.

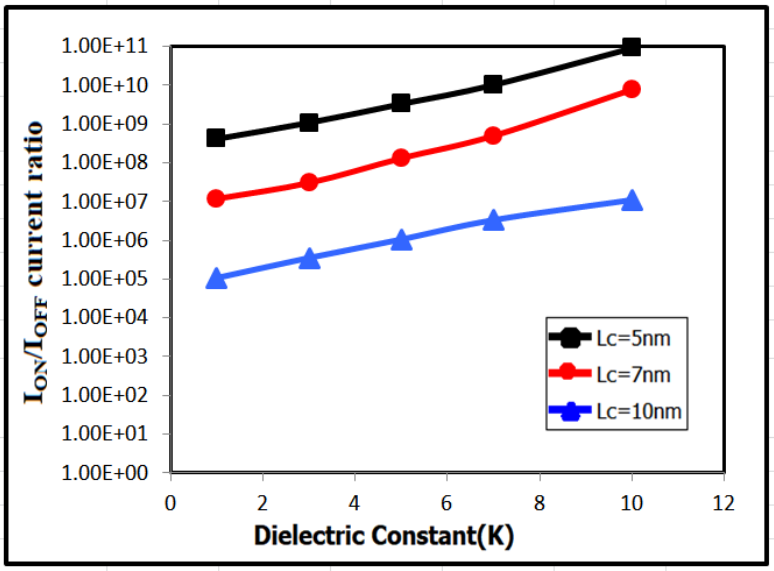


Fig 6.17.I_{ON}/I_{IOFF} ratio vs. Dielectric Constant (K) for different cavity lengths

Table 6.8: Threshold voltage and I_{ON}/I_{OFF} Ratio at various cavity lengths of 18nm Triple Gate FinFET

Cavity Length (L_{cav}) (nm)	Biomolecule Dielectric Constant (K)	Threshold Voltage V_{th} (V)	I_{ON}/I_{OFF} Ratio
5	1	0.52	4.17E+08
	3	0.52	1.09E+09
	5	0.53	3.32E+09
	7	0.55	1.03E+10
	10	0.54	9.16E+10
7	1	0.44	1.19E+07
	3	0.44	3.06E+07
	5	0.46	1.32E+08
	7	0.48	5.03E+08
	10	0.46	7.86E+09
10	1	0.32	1.08E+05
	3	0.32	3.56E+05
	5	0.34	1.07E+06
	7	0.34	3.38E+06
	10	0.36	1.12E+07

Comparison of performance characteristics of Nano wire for cylindrical gate, 3 fin 18nm triple gate FinFET and Bulk CMOS device:

Table 6.9 gives the comparison of performance characteristics of Nano wire for cylindrical gate, 3 fin 18nm triple gate FinFET and Bulk CMOS device interms of electrical charateristics such as threshold voltage, sub threshols slope and I_{ON}/I_{OFF} ratio. From the table, it is clearly showing that I_{ON}/I_{OFF} ratio is greater for 3 fin 18nm triple gate FinFET wth appresiable threshold voltage and subthreshold slope when compared to other two devices. Hence the short channel effects are largely suppressed in the 3 fin 18nm triple gate FinFET device that giving rise to high performance at low power.

Table 6.9 Comparison of performance characteristics of Nano wire for cylindrical gate, 3 fin 18nm triple gate FinFET and Bulk CMOS device

Device Type		18nm Nano wire for cylindrical gate	18nm 3 fin triple gate FinFET	Bulk CMOS (REF)
Performance Characteristics at K=10 (KERATIN BIO MOLECULE)	Threshold Voltage	0.44V	0.48V	0.36V
	Sub threshold Slope	50.2 mV/decade	48.2 mV/decade	76 mV/decade
	I_{ON}/I_{OFF} ratio	$7.86* 10^{9}$	$9.16*10^{10}$	$1.32*10^{7}$

6.4 Chapter Conclusion:

A triple gate 18nm FinFET was used in this work for bio sensing techniques. Various model aspects were changed using expanded simulations to achieve better implementation aspects of the suggested triple gate FinFET. The ultra-thin fin on the triple gate FinFET at low power results in suppression of short channel effects and leakage current and operates at high sensitivity for bio-sensing techniques . In terms of I_{ON} (10-7 A/µm), I_{OFF} (10^{-18} A/µm), and I_{ON}/I_{OFF} ratio, the suggested device performed better compared with the other technologies. The V_{th} deflection was observed to be V_{th}=0.54 V and V_{th}=0.36 V for dielectric constants of 10 and 1 respectively. For various di electric constants and positively and negatively charged molecules, the center potential was investigated, yielding a minimum value of -0.82V and a maximum value of -3.2V. This work also looks at the performance of the triple gate FinFET device with different cavity lengths such as 5nm, 7nm, and 10nm. The observation shows that as cavity length decreases, I_{ON}/I_{OFF} ratio increases. Thus the 18nm triple gate FinFET is designed by various neutral and charged bio molecules with appreciable I_{ON}/I_{OFF} ratios.

CHAPTER 7: CONCLUSION AND FUTURE SCOPE

7.1 Conclusion: This thesis presents the culmination of research conducted on three distinct technologies: 10nm, 18nm, and 22nm FinFET technologies. The primary objective is to mitigate short channel effects even at reduced channel lengths, ensuring high performance and yielding a significant ION/IOFF ratio and threshold voltage. A 10nm FinFET and a 22nm triple gate FinFET were meticulously designed, simulated, and analyzed for both AC and DC performance characteristics, including threshold voltage, subthreshold slope, Drain Induced Barrier Lowering (DIBL), ION/IOFF ratio, capacitances, and transconductance, utilizing the Cogenda Visual TCAD simulation tool. Device performance optimization was achieved by scrutinizing drain current characteristics under various conditions such as different channel lengths, SiO2 and HfO2 oxides, diverse doping levels, temperatures, and various metal contacts for source, drain, and gate in the proposed 10nm Triple gate FinFET. The proposed device demonstrated a notable enhancement in the ION/IIOFF ratio, reaching up to 108. Electrostatic behavior, encompassing electrical characteristics, surface potential, and electron and hole density, was comprehensively evaluated based on the device architecture. Additionally, a triple gate 18nm FinFET was designed and implemented for bio-sensing applications. Various bio-molecules, including Biotin, Zein, and Keratin, were introduced into the air cavity for bio-sensing operations.

This device has provided a better I_{ON} of order ~ 10^{-8} A/µm, I_{OFF} of order ~ 10^{-18} A/µm and I_{ON}/I_{IOFF} ratio of 10^{1o}.The deflection in V_{th} was noticed to be ΔV_{th}=0.54 V and ΔV_{th}=0.36 Volts of value for dielectric constant = 10 and 1 respectively. The central potential has been analyzed for different Di electric constants and for positive and negatively charged molecules that reached to a minimum value of -0.82V and Maximum value of -3.2V. Also in this work, the performance of the triple gate FinFET device is analyzed with different cavity lengths such as 5nm, 7nm and 10nm. The observation shows that the I_{OFF} becomes small when cavity length decreases. Thus a high sensitive 18nm triple gate FinFET is designed with highly threshold voltage and I_{ON}/I_{IOFF} ratio with different dielectric constants of different neutral and charged molecules. Finally, the proposed device shows appreciable performance in giving rise to higher I_{ON}/I_{IOFF} ratio. The I_{ON}/I_{OFF} ratio value comes around 9.16×10^{10} which is considerably high, when compared to the most of the existing architectures.

7.2 Future Scope:

The current research has been conducted by studying the n-type proposed FinFET Biosensor structure. The research can be carried forward with the study of its counterpart, p-type FinFET Biosensor structure. This would pave the way for designing a complementary FinFET device. Further, a compact model could be developed for the device using Cogenda Visual TCAD tool which can be then exported to circuit simulation software like Cadence Virtuoso for performing circuit-level analysis of the device. In terms of the biomedical applications, this P type FinFET biosensor is also an interesting topic of research, where the properties of the device can be utilized to improve the sensitivity of the biosensors in use to compare with N type as well. From the comprehensive study, it is stated that a promising area for future generations of investigators may be the identification of biomolecules with changes in their dielectric constant as well as the application of a disease.

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PAPER PUBLICATION DETAILS

Sno.	Title of paper with author names	Name of journal / conference	Published date	Issn no/vol no/ Issue no	Indexing in Scopus/ Web of Science/ UGC-CARE list (*please mention*)
1	K Bindu Madhavi and Suman Lata Tripathi "Strategic review of different materials for FinFET Structure Optimization" 2020 *IOP Conf. Ser.: Mater. Sci. Eng.* 988 012054	International Conference on Recent Developments in Material Scienceand Applications (ICRDMSA 2020)-IOP Science conference Proceedings	Nov,2020	ISSN:1757-8981 Vol 988	Scopus Conference Paper
2	Bindu Madhavi, Suman Lata Tripathi, Bhagwan Shree Ram "Chapter 17: FinFET Technology for Low-Power Applications" Wiley	Design and Development of Efficient Energy Systems, Wiley	15/04/2021	ISBN: 978-1-119-76178-5	Scopus Chapter
3	K Bindu Madhavi, Suman Lata Tripathi "Robustness Evaluation of sub- 22nm FinFETs Electrical characteristics Affected by Physical Variability" Materials TodayProceedings, 49, Part 5, 2245-2252.	Global Conference onRecent Advances in Sustainable Materials 2021-Elsevier Materials TodayProceedings	Oct,2021	ISSN 2214-7853 Vol-49	Scopus-Conference Paper
4	K Bindu Madhavi, Suman Lata Tripathi "Electrical Characterization of highly stable 10nm triple-gate FinFET for different contacts and oxide region materials" *Silicon* 14, 12281–12291 (2022)	Silicon, Springer	14/05/2022	ISSN 1876-9918	**SCI / Scopus Article**
5	Kalasapati Bindu Madhavi, Suman Lata Tripathi, Sobhit Saxena, Deepika Ghai, and Balwinder Raj "Design and Analysis of 18 nm Multichannel FinFET as Biosensor for Detection of Biological Species" Silicon, 15, 6313–6322 (2023)	Silicon, Springer	May,2023	ISSN 1876-9918	**SCI/SCOPUS Article**

6	Kalasapati Bindu Madhavi, Suman Lata Tripathi "Design and optimization of low power high performance triple gate FinFET for sub 22NM technology" L-126699/2023	Copyright published	June-2023	L-126699/2023	**Copyright**
7	Design and optimization of low-power, high-performance Triple gate FinFET at the 18nm Technology Node for Biomedical applications.	Patent, In submission process	-	-	Patent