DESIGN AND ANALYSIS OF AN OPTIMIZED ASYMMETRIC MULTILEVEL INVERTER FOR GRID CONNECTED PV SYSTEM

Thesis Submitted For the Award of the Degree of

DOCTOR OF PHILOSOPHY

in

Electrical Engineering

By

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DECLARATION

I declare that the thesis entitled "**DESIGN AND ANALYSIS OF AN OPTIMIZED ASYMMETRIC MULTILEVEL INVERTER FOR GRID CONNECTED PV SYSTEM**" has been prepared by me under the supervision of **Dr. Aman Ganesh,** Professor, School of Electronics and Electrical Engineering, Lovely Professional University, Punjab, India, and co-supervision of **Dr. Neerudi Bhoopal,** Professor & Dean Administration, Department of Electrical and Electronics Engineering, B V Raju Institute of Technology, UGC-Autonomous, Narsapur, Telangana, India. No part of this thesis has formed the basis for the award of any degree or fellowship previously.

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ABSTRACT

Due to the increase in energy demand and growing awareness of the environmental impact, renewable energy harnessing has attracted increased interest. The solar photovoltaic system (SPV) is the most enabling technology for power generation among various available renewable energy sources. The inverter in a grid-connected solar photovoltaic (GCSPV) system is a significant component to convert PV power into AC power since it costs 59% of the total cost. Generally, two and three-level inverters are used in the GCSPV system to reduce the cost of the inverter. However, these inverters suffer from a lack of galvanic isolation between the grid and the PV source and provide constant dv/dt output, which requires a bulky filter to convert the constant dv/dt to a nearly sinusoidal output. As a result, multilevel power converter technology has emerged as a potential solution for medium and high-power applications.

Traditional multilevel inverters (MLIs) such as neutral point clamped (NPC), flying capacitor (FC), and cascaded H-bridge inverter (CHB), are not commercially significant for solar photovoltaic (SPV) systems, where the potential for conversion of energy is already limited (performance in commercial applications is generally less than 20%). Such multilevel inverters are more costly as they require more semiconductor switches, capacitors, dc sources, and clamping diodes. Due to its modular design and simple operation, the CHB-MLI has gained more importance in grid interconnecting applications. However, it necessitates many power electronic switches and separate dc sources in its design, which leads to a significant problem in the control circuit and switching modulation. The researchers have developed various solutions to address the CHB-MLI control complexities. The number of switches and isolated dc sources often increases with the output voltage levels, making CHB-MLI even more complicated. Furthermore, when employing the CHB-MLI for PV applications, it is challenging to handle asymmetric PV sources produced by varying temperature and irradiance.

This research aims to develop an optimized asymmetric multilevel inverter for interconnecting the PV sources under the different operating conditions of the grid. The performance of the inverter majorly depends on design topology, switching modulation techniques, and control methodology. The first part of the thesis focuses on the inverter topology. This dissertation presents the design and analysis of a single-phase asymmetric

inverter for a grid-connected solar photovoltaic (SPV) system with reduced components. The proposed inverter topology comprises two circuits, namely the primary circuit and the auxiliary circuit. The primary circuit is connected to the asymmetric PV sources and can generate several levels. The auxiliary circuit is an H-bridge circuit that reverses the polarity of output voltage. The proposed MLI utilizes seven power switches, three diodes, and three dc sources for 15-level output. The required number of switches, diodes, and input dc sources of the proposed inverter is compared with existing 15-level topologies. The proposed inverter utilizes a minimum number of switches to generate a more significant number of output voltage levels. It is also free from clamping capacitors, where voltage balancing is a major issue and utilizes very few switching diodes. Hence, the effect of reverse recovery times of the diode on inverter performance is minimal. The metrics considered for the proposed inverter's performance assessment are reduced switches, power losses, THD, and grid integration.

The second part of the thesis focuses on improving the designed inverter performance by switching modulation. This includes both high-frequency (carrier-based) modulation and low-frequency modulations. It is intended to reduce the power losses by reducing the switching losses and conduction losses to improve the efficiency of the inverter. This study explores selective harmonic elimination pulse width modulation (SHEPWM) as low-frequency switching modulation to lower the system power losses while minimizing the selected lower order harmonics at the inverter's output.

The inverter is simulated using the PLECS thermal model for analyzing the power losses in the proposed 15-level inverter using low switching frequency modulation (SHEPWM) and high switching frequency modulation (phase disposition pulse width modulation - PDPWM). The power losses obtained from the PLECS thermal model with SHEPWM are compared with the PDPWM. The inverter's efficiency is determined in both cases. It is observed that the efficiency of the inverter with SHEPWM (97.99%) is greater than PDPWM (97.38%) switching. Further, the power losses and inverter efficiency are validated with precise models simulated on Simulink using SHEPWM control.

To solve the nonlinear transcendental equations established by SHEPWM, optimization techniques such as Genetic Algorithm (GA), Particle Swarm Optimization (PSO), Whale Optimization Algorithm (WOA), and Harris Hawk Optimization algorithm

(HHO) were used to the 15-level asymmetric inverter for reducing the THD of output voltage and current as per IEEE519 standard. To improve the algorithm's performance (speed of convergence) and the quality and accuracy of the solution, the hybrid algorithms combine the algorithms above with appropriate ones. The Enhanced Whale Optimization algorithm (EWOA), hybrid Asynchronous Particle Swarm Optimization with Newton Raphson algorithm (APSO-NR), hybrid Particle Swarm Optimization with Genetic Algorithm (PSO-GA), and hybrid Harris Hawk with Differential Evolution (HH-DE) algorithms were applied to the 15-level asymmetric multilevel inverter to improve the performance of the designed inverter. The results of these algorithms are compared in terms of convergence rate, THD of output voltage, and currents. The THD of output voltage using PSO-GA is 5.34%, HH-DE is 5.33%, and the THD of output current using PSO-GA is 2.66%, HH-DE is 2.78%. These results show that the hybrid PSO-GA and HH-DE algorithms give better results than other algorithms implemented without a filter.

The third part of the thesis deals with the use of the proposed asymmetric 15-level inverter for grid integrating the solar photovoltaic system. For this, a grid-connected SPV system is implemented with the proposed asymmetric 15-level inverter. A closed-loop grid-connected controller has been developed with three individual voltage controllers, one overall voltage controller, and a current controller using a PI controller. The gain parameters of the PI controller are adjusted to ensure a steady current and voltage on the grid under variable temperature and irradiance conditions. An LCL filter is employed between the proposed inverter output and the grid to reduce the ripples and improve the waveform quality. The THD & efficiencies are determined to verify the grid-connected solar photovoltaic (GCSPV) system's performance under various irradiance and temperature conditions using PSO-PI, HHO-PI, and hybrid PSO_GA-PI controllers. The obtained results show that the hybrid PSO_GA-PI given the minimum THD value of 1.26% at higher efficiency of 95.82% compared to other control algorithms. Finally, the leakage current on the GCSPV system is measured to evaluate the proposed inverter's performance.

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Date: 19/03/2022 **Devineni Gireesh Kumar**

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LIST OF SYMBOLS & ABBREVIATIONS

SPV	-	Solar photovoltaic system
GCSPV	-	Grid-connected photovoltaic system
P&O	-	Perturb and observe
MPPT	-	Maximum power point tracking
MLI	-	Multilevel inverter
SHEPWM	-	Selective harmonic elimination pulse width modulation
PDPWM	-	Phase disposition pulse width modulation
SVPWM	-	Space vector pulse width modulation
MV	-	Medium voltage
HV	-	High voltage
THD	-	Total harmonic distortion
V_{dc}	-	DC input voltage
FSFC	-	Fundamental switching frequency control
α	-	Switching angle
V_{1max}	-	Peak fundamental voltage
V_1	-	Actual fundamental voltage
k	-	Degree of freedom
N	-	No of output voltage levels
N_{DC}	-	Number of DC sources
N_S	-	Number of switches
N_D	-	Number of diodes
N_C	-	Number of capacitors
M	-	Modulation index
OF	-	Objective function
$P_{Conduction}$	-	Conduction losses
$\lvert I_C \rvert$	-	Conduction Current
V_{on}	-	ON State voltage of the IGBT
$E_{on\_SW\_loss}$	-	ON state energy loss of IGBT
$E_{off\_SW\_loss}$	-	OFF state energy loss of IGBT
V_{CE}	-	Collector emitter voltage of IGBT

T_{on}	-	ON time of IGBT
T_{off}	-	OFF time of IGBT
E_{SW_loss}	-	Total switching losses of IGBT
T	-	Operating time of IGBT Switch
f_{SW}	-	Switching frequency
v_D	-	Diode voltage
GA	-	Genetic algorithm
PSO	-	Particle swarm optimization
WOA	-	Whale optimization algorithm
HHA	-	Harris hawk algorithm
EWOA	-	Enhanced whale optimization algorithm
APSO-NR	-	Asynchronous Particle Swarm Optimization with Newton Raphson Algorithm
PSO-GA	-	Particle Swarm Optimization with Genetic Algorithm
HH-DE	-	Harris Hawk with Differential Evolution Algorithms
V_{grid}	-	Grid voltage
V_{PV}	-	PV cell voltage
I_{PV}	-	PV cell current
P_{PV}	-	PV cell power
V_{Boost}	-	The output voltage of the dc-dc boost converter
I_{Boost}	-	The output current of the dc-dc boost converter
K_{Vp}	-	The proportional gain value of the voltage controller
K_{Vi}	-	The integral gain value of the voltage controller
K_{Cp}	-	The proportional gain value of the current controller
K_{Ci}	-	The integral gain value of the current controller
PI	-	Proportional plus integral

CHAPTER-1

INTRODUCTION

1.1 INTRODUCTION

The advancement in day-to-day technology and cost-effectiveness are the two significant factors that use solar energy to meet increased energy demands. From 2007 to 2022, there was an 85% reduction in the cost of solar panels, which steers to decrease the cost of generation from solar PV panels. The power generation cost dropped to 83.5%, from INR 24.82 to INR 4.12 per kWh during 2010–2022 [1]. The cost of solar power production in India is expected to fall to about INR 1.9 per unit by 2030, according to TERI-CPI research. Thus, the multi-megawatt rating PV energy has become a reality. The standard solar power plants mainly consist of PV modules, which are physically exposed to the environment to convert solar radiation into DC power. With the frequency of the solar radiation and operating temperature, the peak power produced by the PV panel varies. A PV array's maximum power can be extracted using MPPT control algorithms. In MPPT, many algorithms were used to maximize the PV system's power output power.

Power modulator (Power electronic converter that converts dc to dc and dc to ac) is one of the significant components of the solar PV system. Power electronics is about converting power from one form to another form, while power conversion takes place in the field of electricity. The power conversion from the existing state to the required should happen with minimal power losses, minor deviation in quality of power, low cost, reduced number of switching devices and electronic components. Also, there should be minimal mathematical overheads.

Today India is looking towards renewable energy sources for its power demands. The Atmospheric conditions of India can harness enormous solar energy. Annually about 5000 trillion kWh power is incident in the land areas of India. Almost every component receives 4-7 kWh per sq.m per day. Due to this, conversions from solar radiation to heat and from solar radiation to electricity are successfully utilized. Photovoltaic generations are available in both grid-connected mode and islanded mode.

It is generously available and meets energy demands such as power, heating, cooling, etc., in urban and rural areas. Photovoltaic generation is the most secure power and green energy generation of all Renewable resources [2].

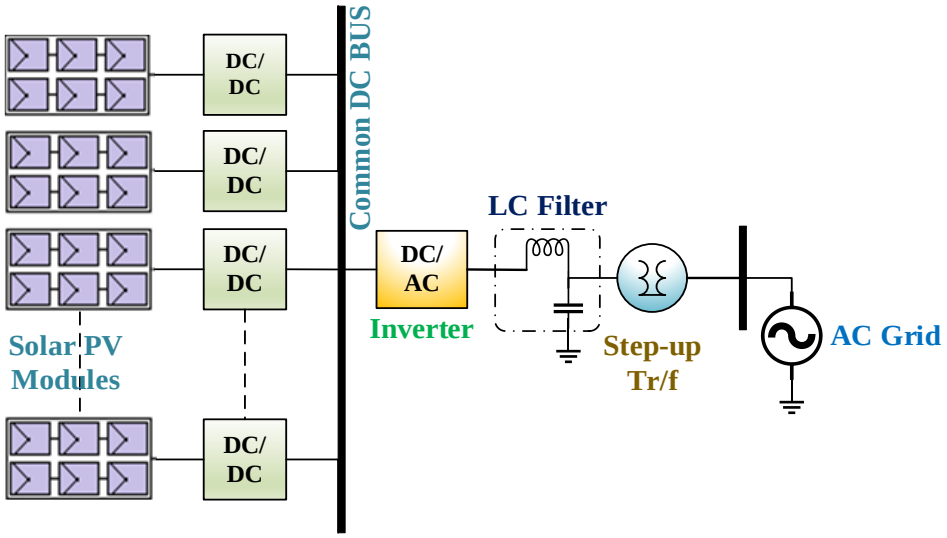


Figure 1.1 Common grid-connected solar PV system

Solar energy can fulfill the entire country's needs if harnessed effectively. There are still numerous places in India that are not electrified. Photovoltaic generating systems are an excellent alternative for electrifying these formerly unconnected locations. Photovoltaic generation uses series & parallel-connected PV modules, power electronic converters, energy storage devices (battery), step-up transformers and filters, etc. Figure 1.1 shows the standard grid-connected PV system setup with a common dc bus. The inverter is a significant component of the grid-connected PV system since it costs 59% of the total cost. The researcher developed many inverter topologies to test the GCSPV system's applicability, efficiency, and lifetime.

There are four different types of inverters utilized for grid-connected photovoltaic systems. The four different configurations of PV inverters are listed as follows:

1. AC- module inverter
2. String inverter
3. Multi string inverter
4. Centralized inverter

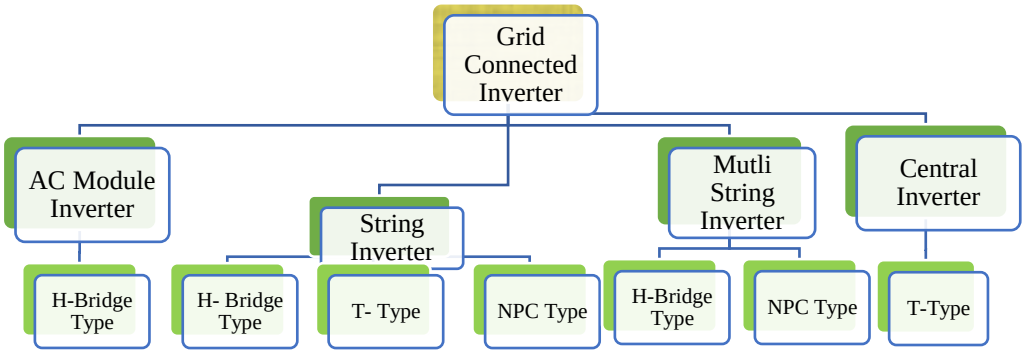


Figure 1.2 Different configurations of grid-connected PV inverters

Figure 1.2 shows different PV inverters available in the market, such as AC-module inverter, string inverter, multi-string inverter, and centralized inverter. NPC, T-type, and H-bridge are the most common designs for high-power and residential applications in the KW to MW range.

From the above configurations, AC-module inverter is used for the small-scale applications, i.e. < 350 W range, string, and multi-string inverters are used for medium-scale applications, i.e. > 10 KW and < 500 KW respectively, centralized inverter are used for the large-scale applications, i.e. > 850 KW range. The unit cost for string inverters is as high as it is only suitable for low-power applications. The efficiency of the central inverter is more elevated, i.e. about 98.6%. Still, there are several disadvantages. It needs blocking diodes and gives poor MPPT performance, i.e. only a single MPPT is used for the entire system, and the centralized inverters are not flexible. Whereas in the case of the multi-string inverter, separate MPPT systems are available for each string. Related research is also carried out in [3]-[5].

To get a near sinusoidal staircase waveform, the multilevel inverter employs several power electronic switches that are connected to several small dc voltage sources. The multilevel inverter's most pleasant trademarks are Common mode voltage, Input current, Switching frequency, Reduced harmonic distortion etc.

Specific applications of multilevel inverters are Variable frequency AC motor drives, Active power filters, Electric vehicle motor drives, DC source utilization, Power factor correction equipment, Renewable energy conversion system, Consecutive frequency link systems, Integration of non-conventional energy resources.

A staircase type approximated near sinusoidal waveform of multilevel inverter output is shown in figure 1.3.

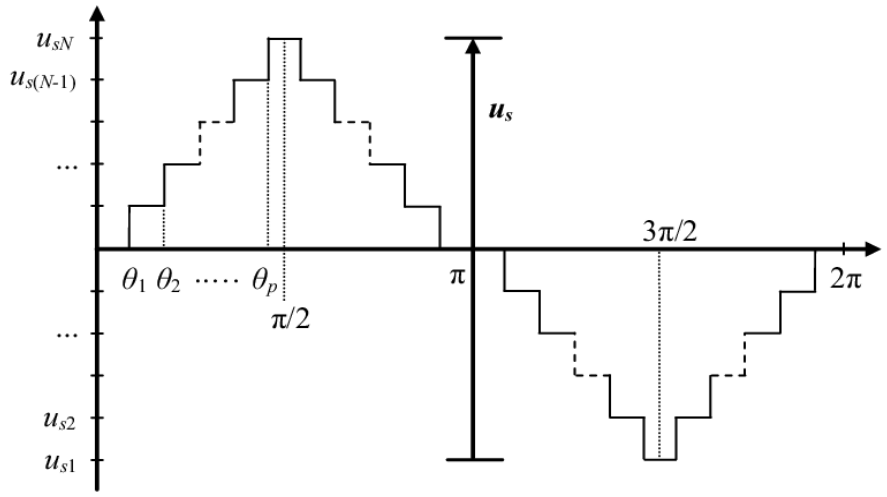


Figure 1.3 Near sinusoidal staircase waveform of multilevel inverter

Many industrial applications nowadays need significant power. Nonetheless, most of the industrial equipment runs on medium or low energy. While certain industrial loads may gain from high-power sources, others may suffer. For medium and high-voltage applications, the multilevel inverter has been used since 1975.

Multilevel inverters can be conveniently applied to solar PV systems due to their ability to produce variable voltage from a constant dc source and remove harmonics in the conversion process when incorporating PV power into the grid. The appreciable features of multilevel converters are as follows:

i. *Stairway waveforms quality:* multilevel inverters may alleviate electromagnetic compatibility (EMC) issues by having extremely low distortion and lowering dv/dt.
ii. *Switching Frequency:* one of a multilevel inverter's key advantages is running at both a high and low switching frequency.
iii. *More sinusoidal output waveform:* by raising the levels of the multilevel inverter, the voltage output becomes more sinusoidal, and the harmonic content is decreased.
iv. *Source current*: Multilevel converters will draw the low distortion current.

There are currently several multilevel inverters being developed. The

following improvements have been observed for multilevel inverters and are presently being used by the industries. The classification of these MLIs is given in figure 1.4.

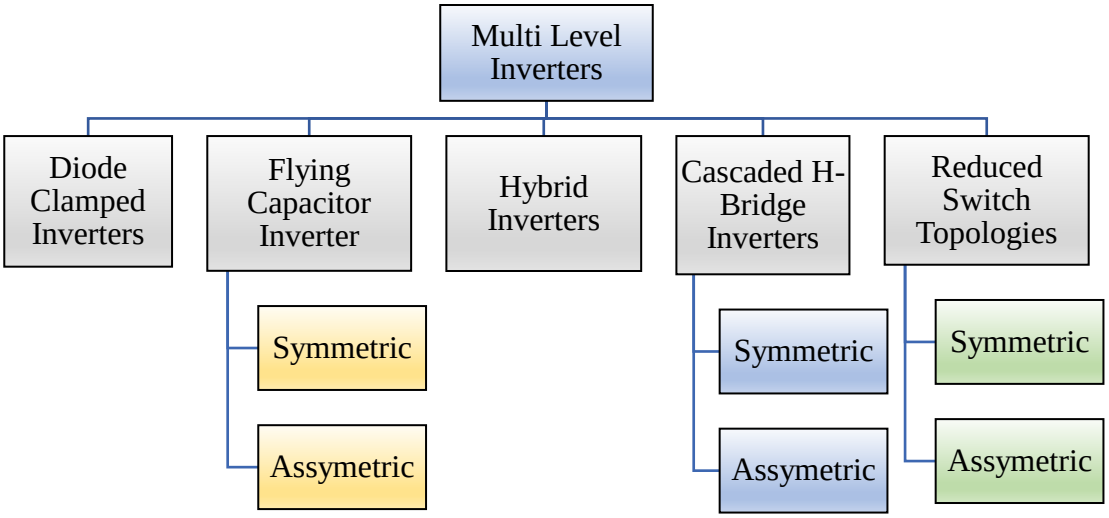


Figure 1.4 Classification of multilevel inverters presently used in the industries

1.2 INVERTER CHALLENGES

Solar PV systems can be stacked or integrated into the grid using inverters. A variety of inverters are developed and designed for solar PV systems. Currently, 2- level and 3-level inverters transformerless inverters are being used in solar PV plants due to their low cost, simple, compact design, and control. Among these, the transformerless inverter is highly efficient and can operate with an efficiency of around 99% [6]. Although these inverters are highly efficient, the major drawback is that there is no isolation between the solar PV system and the grid. With the lack of galvanic isolation, transformerless inverters damage the solar PV plant during the short circuit faults on the grid. Even though these low-level inverters are cost-effective, the problem with these inverters is that they have constant dv/dt. But all the load equipment is designed to operate with variable dv/dt with the instantaneous change in voltage magnitude. The constant dv/dt in 2-level and 3-level inverters decreases the load equipment life and gives the deviated characteristics compared to their actual operating characteristics. Hence it is essential to use high-level inverters that provide the variable dv/dt output voltage in the near-sinusoid for safe loading equipment operation. Many researchers have carried out the study to obtain multilevel output and have proposed advanced developments. Three MLIs are used in practice: diode clamped, flying capacitor, and

H-bridge inverters. When the number of levels is high, such multilevel inverters are more expensive since they require more semiconductor switches, capacitors, DC sources, and clamping diodes. Also, the control circuit becomes complicated using more switching devices, which increases the harmonics and further increases switching losses. Modern MLI topologies are not commercially feasible for solar photovoltaic (SPV) systems with limited energy conversion potential (performance in commercial applications is less than 20%).

To reduce the volume, cost, and losses in the multilevel inverter and to meet the load requirements, multilevel inverters with reduced power switches and fewer circuit elements are required to build. On the other hand, the symmetrical MLI can increase the voltage levels of the inverter while operating at a low switching frequency, making it a potential PV inverter with greater efficacy. With a reduced number of switches, the inverter operates relatively at a low switching frequency, which improves the inverter's performance and reduces the filter requirements for stand-alone or grid-connected PV applications.

The present research focused on identifying and developing an asymmetric multilevel inverter with reduced switches to optimize the power and control circuits. The proposed multilevel inverter configuration is quite simple and easy to extend for higher levels, as well as its gating circuits are simplified due to the optimized number of switches. The primary factor influencing the inverter's performance is the harmonics of the multilevel output. Although in the proposed topology of the inverter, the number of switches is reduced for the operation with different switching angles, which often causes harmonics in the output. The goal here is to optimize the switching angles to minimize the lower-order harmonics of the proposed inverter.

Several optimization algorithms were reported to evaluate the optimal switching angles for the inverters, thereby reducing the harmonics content in the inverter output. However, these algorithms are designed to operate at higher switching frequencies, unsuitable for effectively eliminating the lower-order harmonics. The study carried out by various researchers mainly develops symmetrically reduced switch inverters with optimization methods, which are not relevant for solar PV applications since the solar PV system's output is variable with the variation of solar irradiance and temperature.

The inverters must accept variable input from solar PV to produce a constant output voltage suitable for stand-alone or grid operation.

The above motivation leads this research to implement an asymmetric multilevel inverter with optimal switches and dc sources. The proposed topology is implemented for a 15-level inverter with seven power switches, three diodes, and three dc sources as shown in figure 1.5.

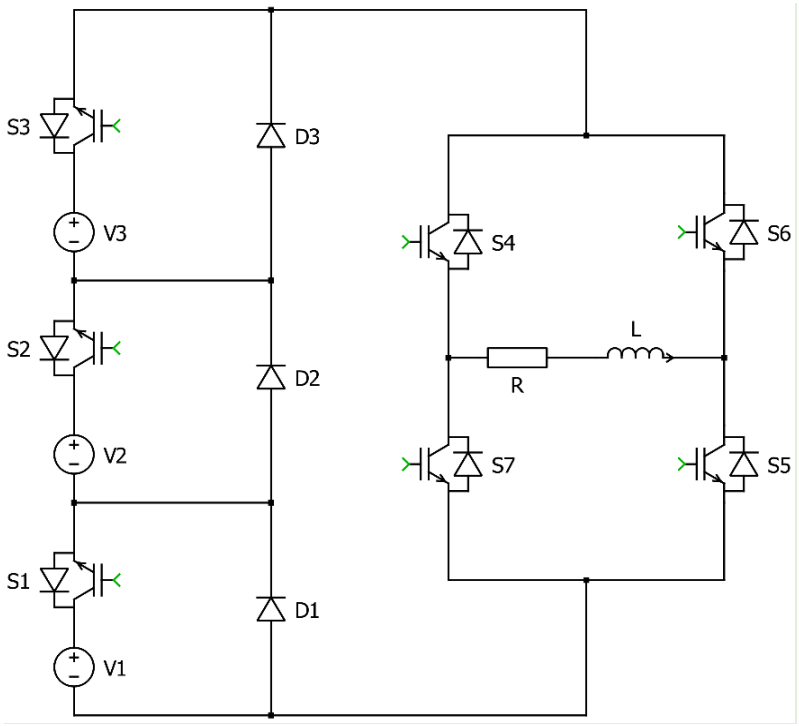


Figure 1.5 An asymmetric inverter with a reduced number of switches

The proposed topology consists of two parts namely, the level generation part and the polarity generation part. The level generation part consists of three switches, three dc sources, and three switched diodes. By cascading the basic units, the number of output levels was increased. The polarity generation part is an H-bridge inverter consisting of four switches and a load circuit, which is responsible to reverse the polarity of the output waveform for every half cycle. Three input sources were chosen based on the binary approach as the ratio of 1:2:4 for asymmetric sources. The detailed methods of choice input sources and the structure of the 15-level asymmetric inverter are presented in chapter-3.

1.3 RESEARCH OBJECTIVES & METHODOLOGY

The objectives of the research are summarized as follows

1. To select and develop the asymmetric multilevel PV inverters with reduced switch count for the limited number of commutations by considering nonlinear loads.
2. To reduce the switching losses by the low switching frequency control.
3. To implement different hybrid soft computing algorithms for optimizing the switching angles of the proposed asymmetric multilevel inverter to reduce total harmonic distortion.
4. To simulate and test the performance of the proposed inverter on a grid-connected PV system.

The proposed research is aimed to minimize the THD in reduced switch multilevel PV inverters using different soft computing techniques. To accomplish this, an asymmetric grid-connected PV inverter is considered for commercial loads. The research is carried out in two phases. The first phase is focused on selecting and developing an asymmetric multilevel inverter with reduced switching losses using the low frequency switching modulation technique. The following methodology is adopted in this phase.

(i) Developing an efficient asymmetrical multilevel inverter with reduced switch count for the minimum number of commutations which includes.
   a) Investigation of the current topologies of multilevel PV inverters to explore the limitations of the traditional multilevel inverters.
   b) Study of the various factors affecting the performance of grid-connected inverters.
   c) Study of various factors affecting the power quality of the inverter and explore the remedial measures.

(ii) Formulation of low/variable switching frequency control to eliminate the power losses in the proposed inverter.

The second phase is committed to optimizing the proposed inverter's switching angles, which involves the following steps;

(i) Study and implementation of selected traditional optimization algorithms in solving various types of problems related to power electronic converters to explore their limitations.
(ii) Implementation of various soft computing algorithms, including hybrid algorithms, to reduce the proposed inverter's lower order harmonics.
(iii) Analyzing and validating the results obtained from the applied algorithms on a grid-connected PV system.

1.4 ORGANIZATION

Chapter-1 gives an overview of grid-connected inverters and their challenges.

Chapter-2 presents the comprehensive literature review of grid-connected multilevel inverters and a review of various optimization techniques and their application to multilevel inverters. Based upon the conducted review, the research gaps are also presented in the last section of the chapter.

Chapter-3 presents the design and development of a 15-level asymmetric inverter and its modes of operation. The chapter further presents the use of a low switching frequency control method for mitigating the switching losses. The proposed inverter performance is then compared to seven-level and eleven-level inverters.

Chapter-4 analyzes the power losses in the proposed 15-level inverter with high-frequency switching (PDPWM) and low-frequency switching (SHEPWM) control using PLECS thermal model. These power losses are validated using curve fitting based on precise models on Simulink, and the inverter's efficiency is computed.

Chapter-5 presents the comparative analysis of various traditional and hybrid optimization techniques as applied to the designed inverter for reducing the generated harmonics by optimizing the switching angles.

Chapter-6 discusses the implementation of the proposed inverter to a grid-connected solar PV system. The chapter evaluates the performance of the proposed inverter under different operating conditions.

Chapter-7 presents the conclusive summary of the entire research and recommendations for future work.

CHAPTER-2

STATE OF THE ART OF THE GRID-CONNECTED MULTILEVEL INVERTER

2.1 INTRODUCTION

Multilevel inverters are applied to solar PV systems due to their inherent ability to convert input dc voltage to output ac voltage. Many MLI topologies and control methodologies have been proposed in the literature to get the optimum output from the inverter, which injects the least harmonics into the system. This chapter presents an exhaustive literature review on multilevel inverters for grid-connected applications and their control methodologies. The first section presents the review on multilevel grid-connected PV inverters considering different configurations, topologies and switching methodologies, followed by the research gaps and scope of research in the second section.

2.2 REVIEW OF MULTILEVEL GRID-CONNECTED PV INVERTERS

While designing the medium-voltage converters for multiple applications such as motor drives, solid-state transformers, and solar photovoltaic presents some common problems such as difficulties with large-scale photovoltaic systems, complicate the converter and control circuit. Multilevel inverter theory was first introduced in 1971 as a substitute for medium-power applications for a series of connected power electronic switching devices [6]. During the 1971-1981 era, the MLIs such as neutral point clamped (NPC), a flying capacitor (FC), and cascaded H-bridge (CHB), were suggested [7-8].

Because of its basic circuit design, the idea of a three-level NPC converter has become more popular and are still commercially available. However, the rise in levels of neutral point clamped topology considerably increases the number of clamping diodes. [9], [10]. The inverse retrieval times of the clamping diode render this topology feasible to develop an inverter with more levels for medium power applications [11]. Hence, the neutral point clamped topology and the flying capacitor topologies are too

inadequate for MV and HV applications because they use many condensers requiring prior charging and balancing the capacitors [9], [11]. Furthermore, a large dc-link capacitor needs for single-cell topology limits its application to medium and high voltages, particularly solar PV applications, where different PV panels are connected in series [12-13]. This vast number of series-connected PV panels will decrease the overall system efficiency due to common MPPT and series resistance [14].

Modular structures have been developed by cascading the full-bridge inverters, named multi-cell multilevel CHB converter topology, which provides MPPT operation at the module level and is scalable to various voltage levels. Also, clamping diodes and capacitors are not used by CHB topologies [11]. The CHB is getting rid of the more series PV modules; however, continuous module parameters and the partial shading will cause mismatch problems [15-18]. These mismatch problems create imbalance and result in low quality of power to the grid [19]. While using CHB converters for PV applications, this module mismatch is another challenge compared to converters in solid-state transformers [20-23] and solid-state motor drives [24-25].

Multilevel Inverter (MLI) in solar photovoltaic (PV) systems is increasingly used for standalone or grid-connected applications [26-28]. Traditional two and three-level inverters are widely used for standalone and GCSPV systems [26]-27]. These are, however, affected by high THD and high dv/dt stress on the switches of the inverter. Furthermore, the switching frequency of pulse width modulation is increased; hence the THD and power losses are often high.

For grid-connected PV systems, there are several MLIs, such as the neutral point clamped MLI [28], flying capacitor-based MLI [29], cascaded H-bridge MLI [30-32], and hybrid topologies [33-36]. Symmetric cascaded MLIs become more prominent due to their modular design, increased rating capability, and near sinusoidal voltage levels. On the other hand, traditional inverters have significant power losses because they require many power switches and often operate at a high switching frequency. Asymmetrically configured cascaded MLIs can increase to more voltage levels with less number of comonents [37-38]. Nevertheless, the numbers of switches are still high in the traditional cascaded inverter and increase with the inverter levels.

Many MLIs with a limited number of components have continuously been used in numerous power electronics applications [39-51], [61-63], [78], [82-83], [88], [102], [106-110]. Many MLIs have two parts: the level generating part and the polarity generating part [43-51], [106-110]. Some of these topologies are ideal for the symmetrical configurations [44-46], [49], [50]. In [48], [82-83], an asymmetric inverter with packed U-cells is proposed that may not function under symmetrical source conditions.

In certain inverter topologies, the level generation portion is composed of numerous bidirectional switches connected back to back [44-46], [49], [51]. A cascaded switched diode structure with controlled switches and multiple power diodes is proposed for the MLI to enhance the voltage level (symmetrical and asymmetrical arrangement) [41]. Although the MLIs have more voltage blocking capacity in the polarity generating part than the level generating part.

However, an inverter with asymmetric sources will not be able to create all of the voltage levels. For higher voltages, the circuit with bi-directional switches increases inverter costs. The MLI with a low number of switches may significantly improve the efficiency and harmonics of PV systems interconnected to the grid.

Several researchers recently proposed the number of reduced switch MLIs for GCSPV systems [45], [52-54]. In [45], a 7-level inverter with a minimum number of components and a dc input with a capacitor divided into three equal parts is proposed. Nevertheless, there are no specifics about the voltage balance of the capacitor. A simplified cascaded MLI with reduced witches is suggested for the GCSPV system [53] discussed the voltage balance of dc ties between several dc links. On the other hand, the inverters mentioned above are built only for symmetrical PV voltages and require extra switches. Some of the researchers reported the asymmetric MLI for the PV application; however, the performance of the inverter is the central issue.

Multilevel inverter design has got plenty of literature, among the existing investigations, some of the research investigations for four arm current source inverter [55], quasi-z-source inverter [56], single phase direct grid integrated transformer less converter [57], single-stage direct grid-connected inverter [58], transformerless grid-connected PV inverter [59], modified z-source inverter [60], transformerless cascaded h-4 inverter [61], three phase cascaded h-5 inverter [62], common mode h-5 topology

[63], enhanced h5-d topology [64], two-half-bridge h4 topology [65], common mode grounding topology [66], conventional two-level inverter [67], common mode grounding topology [68], multi cell voltage-source inverter (VSI) [69], multilevel diode clamped inverters [70], h-bridge topology with bipolar switch [71], diode-clamped topology [72], grid-connected PV inverter [73], neutral point clamped inverter [74], two level 3-phase VSI [75], two-stage transformerless dual-buck PV grid-connected inverters [76], single source and double source mli [77], reduced switch asymmetric multilevel inverter [78], three-level NPC inverter [79], multi-phase neutral point clamped 3-level inverter [80], cascaded h-bridge multilevel inverter [81], seven-level packed u-cell inverter [82], seven-level packed u- cell inverter [83], cascaded h-bridge multilevel inverter [84], four-leg voltage-source multilevel inverter [85], single-phase asymmetrical four-level diode-clamped inverter [86], multi-paralleled three-level t-type inverters [87], asymmetrical reduced switched multilevel inverter [88], parallel operated multilevel inverters [89], single-phase hybrid multilevel inverter [90], multilevel voltage source inverter [91], single-phase π-type 5-level inverter [92], 9-level cascaded inverters [93], symmetric and asymmetric MLIs [94], cascaded 11-level inverter [95], voltage source inverters [96], cascaded h-bridge diode clamped inverter [97], 7-level switched capacitor mli topology [98], zero current switching dc-dc boost converter based mli [99], bidirectional switch based reduced switch MLIs [100], 5-level diode clamped multilevel inverter [101], reduced switch count multilevel inverter [102], multi-topology mode inverter [103], hybrid 7-level cascaded multilevel inverter [104], 5-level h-bridge dual buck inverter topology [105], multilevel converter topology with reduced components [106], optimized three-phase multilevel inverter topology [107], hybrid cascaded multilevel inverter (HCMLI) [108], five-level inverter using PODPWM technique [109], symmetrical & asymmetrical MLIs with minimal switches [110]. The detailed summary, problems addressed and solution methods suggested in the literature is listed in table 2.1.

Table 2.1 Review of grid-connected PV inverters

Authors	Type of Inverter	Problems addressing	Journal/ Conference	Year of Publication	Reference
Sandeep *et al.*	4-Arm CSI	• Improve the performance of CSI due to reduced DC-link capacitance. • Reduce the leakage current injected into the grid, thereby limiting the need for an isolation transformer.	IEEE Transactions on industrial electronics	2014	[55]
Mohammad *et al.*	Quasi-Z-source inverter (qZSI)	• Reduction in common mode current. • Eliminate the conduction of the H-bridge body diode, which has lower reverse recovery characteristics. • Eliminating the use of a dc-dc converter.	IEEE Journal of emerging and selected topics in power electronics	2019	[56]

Subhendu *et al.*	Single-phase direct grid integrated transformer less converter	• Tracking MPP under varying atmosphere conditions. • Reducing the number of series linked PV modules within the sub-array	IEEE Transactions on industrial electronics	2018	[57]
Sachin *et al.*	Single-stage direct grid-connected inverter	• Reduction in total harmonic distortion as per grid IEEE-519 standard. • PV array efficiency, cost, size-related issues.	IEEE Transactions on power electronics	2017	[58]
Lloyd *et al.*	Transformerless grid-connected PV inverter	• Eliminate the ground leakage currents and improve the reliability. • Bypass the PV array film capacitance. • Improve efficiency using SiC transistors in the design.	IEEE Transactions on power electronics	2014	[59]
Siddhartha *et al.*	Modified Z-source Inverter	• High voltage boost in a single stage.	IEEE Transactions on industrial electronics	2018	[60]

		• Elimination of multiple stages in the DC-AC conversion process. • MZSI to provide galvanic isolation.			
Xiaoqiang *et al.*	Transformerless cascaded H-4 Inverter	• Common mode current model. • H4 inverter has good reliability, but it cannot eliminate the leakage current.	IEEE Transactions on industrial electronics	2017	[61]
W. Li *et al.*	Three phase cascaded H-5 Inverter	• Mitigation of leakage current.	IEEE Transactions on industrial electronics	2015	[62]
Hong Li *et al.*	Common mode H-5 Topology	• Common mode leakage current. • Electromagnetic interference and insecurity.	IEEE Transactions on power electronics	2019	[63]
Abhijit *et al.*	Enhanced H5-D topology	• Reducing the CM current by adding a clamping diode to the topology of H5. • CM current is brought to one-third of CM current in H5-D topology.	IEEE Transactions on industrial electronics	2017	[64]

Y. Gu *et al.*	Two-half-bridge H4 topology	• To bypass the stray capacitance of the PV array. • Eliminate the leakage current. • Structure and control circuits are more complicated.	IEEE Transactions on power electronics	2013	[65]
N.Vazquez *et al.*	Common mode grounding topology	• Common mode grounding practices of PV array. • The output voltage is distorted in the negative half cycle.	IEEE Transactions on industrial electronics	2015	[66]
J.F. Ardashir *et al.*	Conventional two-level inverter	• Economical operation of the inverter. • Harmonic content is very high.	IEEE Transactions on industrial electronics	2017	[67]
Zhiling *et al.*	Common mode grounding topology	• Improve the efficiency of the dc bus. • It requires the two-stage energy transfer, which increases the losses.	IEEE Access	2019	[68]
Thierry *et al.*	Multi-cell voltage-source Inverter (VSI)	• Harmonic mitigation.	IEEE Transactions on industrial electronics	2002	[69]

		• Equality of open-loop nominal voltage.			
GuiJia *et al.*	MLDCL inverters	• Reduce clamping diodes, capacitors, gate drive circuits. • Reduce the size and volume of the topology.	IEEE transactions on industry application	2005	[70]
Gerardo *et al.*	H-bridge topology with bipolar switch	• Reduce the power circuit complexity • Create a smooth output profile with high modulating frequencies.	IEEE Transactions on power electronics	2006	[71]
A.Nami *et al*.	Diode-Clamped Topology	• Compare between unequal symmetrical and asymmetrical configurations. • Analysis of harmonic content.	IEEE Transactions on power electronics	2008	[72]
Yongheng *et al.*	Grid-connected PV inverter	• Improve thermal performance. • Increased utilization factor of the power converter.	IEEE Transactions on power electronics	2014	[74]

		• Select the tradeoff factors to power limit for constant power generation.			
Remya *et al.*	Neutral Point Clamped (NPC) inverter	• Voltage balance to balance the capacitor voltages of NPC • To achieve high voltage gain, a P.I. controller is used. • Inductor current ripple averaging technique is used for controller design.	IET Power electronics	2014	[75]
Yong *et al.*	Two Level 3-Phase VSI	• Improvement in computational efficiency. • Reduction in the number of sectors in vector control from 6 to1. • An Improved FCS-MPC control algorithm is proposed for fast computation.	IEEE Access	2017	[76]

Li Zhang *et al.*	Two-Stage Transformer less Dual-Buck PV Grid-Connected Inverters	• Elimination of common-mode leakage current by direct neutral of grid to the PV negative terminal. • Bypass the stray capacitance of the PV Panel. • Lower voltage drops and smaller dv/dt to improve the efficiency and reliability of the inverter.	Chinese Journal of electrical engineering	2018	[77]
Nagaraj *et al.*	Single Source and Double Source MLI	• Lower the common-mode voltage and dv/dt stress on power devices. • Minimize the switching losses using low-frequency switching. • Reduce the switching losses and improve efficiency with minimum switch count.	Journal of engineering	2017	[78]

Muralidhar *et al.*	Reduced Switch Asymmetric Multilevel Inverter	• Partial shading pattern identification using ANN • Cost-effective MPPT controller for maximum utilization PV power. • Reduced harmonic distortion with high-level reduced switch inverter for economic considerations.	IEEE Access	2019	[79]
Ning Li *et al.*	Three-level NPC inverter	• Neural point potential fluctuations. • Reduction in power losses in the inverter to enhance efficiency.	The Journal of engineering	2019	[80]
Weidong *et al.*	Multi-Phase Neutral Point Clamped 3-Level inverter	• Balance of neutral point voltages under steady and dynamic conditions. • Avoid the non-ideal factors.	IEEE Access	2019	[81]

		• The disadvantage of proposed PWM: Increased switching losses limited to applicability in practice.			
Manyuan *et al.*	CHB MLI	• Carrier reconstruction for cascaded H-bridge inverter. • Improvement in harmonics of output line voltage.	IEEE Access	2019	[82]
Atif Iqbal *et al.*	Seven-Level (P.U.C.) Packed U-cell Inverter	• Elimination of 3rd order harmonics in reduced switch P.U.C. converter using GA-based SHE algorithm. • An optimum solution for low THD	IEEE Access	2019	[83]
Seyed *et al.*	Seven-level packed U-cell inverter	• Mitigate the line current total harmonic distortion (THD) and capacitor voltage error. • Multi-objective predictive control (MO-PC) of the seven-	IET Power electronics	2019	[84]

		level U-cell (PUC7) grid-connected Inverter. • The MO-FCS predictive control technique 'Max-Min process' is applied.			
P.N.V.S. Ayyappa *et al.*	Cascaded H-bridge Multilevel Inverter	• Break-even with step strategy and selective harmonic elimination. • Reduction of THD in comic CHB inverter.	I.C.E.C.A Conference	2017	[85]
Hazrul Mohamed Basri and Saad Mekhilef	Four-leg voltage-source Multilevel inverter	• Predict future behaviour of the output current with FCS-PCC, finite control set–current predictive control. • To control load current of 4-leg multilevel VSI • Select the switching states to minimize the cost function.	IET Electric power applications	2017	[86]

Arash *et al.*	Single-Phase Asymmetrical Four-Level Diode-Clamped Inverter	• Capacitor voltage balancing and voltage quality enhancement of diode clamped inverter through single inductor dc-dc converter.	IEEE Transactions on power electronics	2010	[87]
Alian *et al.*	Multi-Paralleled Three-Level T-Type Inverters	• Elimination of ZCS spikes due to symmetrical 3-level SVM. • Suppress the circulation of zero-sequence current in multi-parallel T-type inverters	IEEE Conference	2017	[88]
Madan *et al.*	Asymmetrical reduced switched multilevel inverter	• Performance analysis of reduced switch asymmetric MLI GCSPV system considering the power losses at various temperatures and irradiations.	IET Renewable power generation	2018	[89]
Qijun *et al.*	Parallel Operated Multilevel Inverters	• Circulating current suppression in parallel operated inverters to meet the high-power demands.	IEEE Transactions on power electronics	2019	[90]

		• Effective phase synchronization.			
Shivam *et al.*	Single-phase hybrid multilevel inverter	• Reduction in cost and installation area • Self-balancing of capacitor voltages. • Multi-carrier pulse-width modulation strategy for pulse generation.	IET Power electronics	2018	[91]
Mehrdad *et al.*	Multilevel Voltage Source Inverter	• Mitigation of common-mode voltage • Presented Novel PWM control method to reduce the common-mode voltage to zero. • But the proposed method increases the THD by 3% at the fundamental current harmonic.	IET Power electronics	2019	[92]

Yanshen *et al.*	Single-phase π-type 5-level inverter	• Better distribution of losses, voltage, and volume reduction of the inductor output filter. • Reduction of THD and improvement in inverter efficiency.	IEEE Transactions on industrial electronics	2016	[93]
Hr.Aghay *et al.*	9-Level Cascaded Inverters.	• Variable frequency multi-carrier PWM Techniques. • Reduction in THD, EMI, and switching losses.	C.E.A.T. Conference	2016	[94]
Kanike *et al.*	Symmetric and Asymmetric M.L.I.s	• Simplified pulse generation using logic gates. • Reduced switch multilevel inverter design.	IEEE Access	2019	[95]
Huibo *et al.*	Cascaded 11-level inverter	• Optimal solutions for the SHE problem. • Shuffled frog leaping algorithm for THD optimization.	IET Power electronics	2014	[96]

Wenchao *et al.*	Voltage source Inverters	• Supply-demand balance of active power. • Microgrid integration with multiple inverters based on intermittent DGs.	IEEE Transactions on smart grid	2016	[97]
Alireza *et al.*	Cascaded H-Bridge Diode Clamped Inverter	• Reduce the THD of voltage and current waveform. • Balancing dc-link capacitor voltages.	IEEE Transactions on power electronics	2011	[98]
S.Raghu Raman *et al.*	7-Level S.C.M.L.I. topology	• Capacitor voltage balancing. • Selective harmonic elimination.	IEEE Transactions on power electronics	2018	[99]
Naresh *et al.*	ZCS DC-DC boost converter based MLI	• Reduce transformer saturation-related issues. • Optimize the structure and conduction losses.	IEEE Transactions on industrial applications	2018	[100]
Hosein *et al.*	Bidirectional Switch based reduced switch MLIs	• Reduction in Total harmonic distortion. • Switching, conduction losses, and total blocking voltage.	IET Power electronics	2017	[101]

Shelas *et al.*	5- Level Diode clamped multilevel inverter	• Voltage balancing effects in diode clamped inverter. • High voltage gain. • Reduce the conduction losses (Low rating MOSFETs are used)	IEEE Transactions on power electronics	2018	[102]
Hari Priya *et al.*	Reduced switch count multilevel Inverter (RSC-MLI	• Harmonic performance of traditional multilevel inverters. • Switching losses and efficiency.	IET Power electronics	2017	[103]
Fengjiang *et al.*	Multi-topology mode inverter	• Assessment payback period R.E.S. • Comprehensive performance improvement.	IEEE Transactions on power electronics	2017	[104]
Manyuan *et al.*	Hybrid 7-Level cascaded multilevel inverter	• Power balance issues. • Performance issues of the inverter. • Modified hybrid PWM strategy is implemented.	IET Power electronics	2018	[105]

Li Zhang *et al.*	5-Level H-Bridge Dual Buck Inverter Topology	• Reverse recovery issues of inverter diodes. • Reliability issues of existing five-level DBFBI topologies	IEEE Transactions on power electronics	2017	[73]
Javad *et al.*	Reduced switch MLI	• Reduce the size, cost, and losses of the inverter. • Balancing circuit's dc-link voltage. • Full bridge converters operate at reduced voltage.	IEEE Transactions on industrial electronics	2012	[106]
Arpan *et al.*	Optimized Three-phase Multilevel Inverter Topology	• Decrease the need for additional components. • Eliminate the possibility of inter-phase asymmetry. • Compact the size of the inverter.	IEEE Transactions on power electronics	2014	[107]
Sze *et al.*	Hybrid Cascaded Multilevel Inverter (HCMLI)	• Decrease switch count is exceptionally compact.	IEEE Transactions on power electronics	2016	[108]

		• Reduction in the number of conductive switches for all voltage levels and needs less isolation for gate drives.			
P.Vishnuvardhan *et al.*	Five Level Inverter using POD PWM Technique	• Generate five-level performance with few switches. • Low switching frequency operation leads to minor switching losses.	International Journal of professional engineering studies	2017	[109]
Marif *et al.*	Symmetrical & Asymmetrical MLI with Reduced Number of Switches	• Utilize lower switch count to produce 13 output levels using only three dc sources. • Fundamental frequency switching method to generate gate pulses.	IEEE Transactions industrial electronics	2018	[110]
Vanaja *et al.*	Asymmetric inverter for grid-connected PV system	• 27 Level Modular Multi-Level Inverter was developed. • The asymmetric structure utilized 14-switches, 3-sources.	International Transactions on Electrical Energy Systems	2020	[174]

2.3 REVIEW OF SWITCHING AND OPTIMIZATION ALGORITHMS

The optimization target could be simply to reduce production costs and optimize production efficiency. A suitable approach is an optimization algorithm. Optimization has become independent of computer-assisted development practices with the introduction of computers. There are different types of algorithms for optimization that are commonly used are include, PSO algorithm (or) Ant colony algorithm (or) Bird's flock algorithm [111], [133], combined PSO and P&O algorithms [112], PSO-based MPPT [113], PSO (global optimization) and MADSA (local optimization) [114], MSHE based on PSO [115], PSO based modified SHE PWM [116], Binary PSO [117], Genetic algorithm [118], Immune genetic algorithm (IGA) [119], BSA algorithm [120], Hybrid GA and PSO [121], SVPWM based optimization [122], Hybrid APSO-NR algorithm [123], Hybrid interior-point algorithm [124], Whale optimization algorithm [125], Modified particle swarm optimization (MPSO) [126], Predictive control algorithm [127], Pareto frontier and multi-objective optimization [128], Modified species based particle swarm optimization [129], Fuzzy SVPWM [130], PSO based memetic algorithm [131], Real-time algorithm [132], Bee optimization algorithm [134], Ant colony optimization [135]-[136], GA, BEE, PSO, BSA, and DSA algorithms [137], Harris Hawk Optimization [180], Harrish Hawk Differential Evaluation Algorithm [181], Improved Dingo Optimization Algorithm [182]. The detailed literature of optimization algorithms for symmetric and asymmetric multilevel inverters is described in table 2.2

Table 2.2 Review of optimization algorithms & switching algorithms

Authors	Type of Optimization Algorithm	Problems addressing	Journal/ Conference	Year of Publication	Reference
Mehrdad, *et al.*	PSO Algorithm (or) Ant Colony Algorithm (or) Bird's flock Algorithm	• Voltage magnitude optimization and increased number of switching angles optimization to minimize the THD of seven-level inverters. • PSO associated with local minima problems for less initial populations. • Avoid local minima problems by generating a vast number of initial populations.	IET Journals	2017	[111]
Chakkarapani *et al.*	Combined PSO and P&O Algorithms	• Partial shading conditions lead to trap into Local MPP and fail to track Global MPP • To overcome this PSO is proposed. • However, this causes excessive oscillations before converging GMPP. • Hence to track GMPP accurately under variable irradiance and partial shading	IEEE Transactions on power electronics	2016	[112]

		conditions, P&O and PSO are combined to provide a novel control strategy.			
H.Renaudineau, *et al.*	PSO-based MPPT	• Improvement of the MPPT under partial shading conditions. • Reduction of oscillation in steady-state. • It is developed in PV-oriented MPPT problems. • PSO-based MPPT is also applied for parallel structures. • But these are not applied on any series connected DMPPT.	IEEE Transactions on power electronics	2015	[113]
Kumle *et al.*	A hybrid algorithm PSO & MADS algorithms	• Local optimization was achieved after getting the optimal global position using PSO to achieve precision in harmonic elimination.	IET Power electronics	2015	[114]
Etesami *et al.*	MSHE based on PSO	• Eliminated the dominant lower order harmonics in the inverter output. • PSO with MSHEPWM provides the THD satisfcatory as per IEEE-519 standard.	IET Power electronics	2017	[115]

Kaibalya *et al.*	PSO based modified SHEPWM	• Eliminate the 3rd and 5th harmonics of seven-level inverters.	IET Power Electronics	2018	[116]
Wu.Haitao *et al.*	Binary PSO	• The BPSO (Binary Particle Swarm Optimization Algorithm) is characterized by its speed, precision, and efficiency, making it well suited for online implementation.	Asia-Pacific power and energy engineering conference	2010	[117]
Burak *et al.*	Genetic Algorithm	• Control of multilevel inverters by Genetic Algorithm. • The convergence speed of GA is too slow, hence only applied for online implementations.	IEEE Power electronics letters	2005	[118]
Yuan.J *et al.*	Immune Genetic Algorithm (I.G.A.)	• IGA is an advanced genetic algorithm, and it is still slow to converge.	IEEE Conference	2006	[119]
Civicioglu *et al.*	Binary Search Algorithm	• BSA is a global search algorithm focused on evolutionary computation. • A social group of living organisms hunting regions at random intervals is prompted by	Applications of mathematical computation journal	2013	[120]

		nature, for instance, to overcome food shortage. • It has a simple structure and the ability to solve the higher-order problem of nonlinear, non-differentiable optimization.			
Bharath *et al.*	Hybrid GA and PSO	• GA and PSO algorithms are separately tested to estimate THD • Combining these two, a hybrid approach with GA+PSO algorithm is considered. • This hybrid approach gives superior THD values.	IET Science, measurement and technology	2014	[121]
Oier *et al.*	SVPWM based optimization	• Variable switching frequency-based switching to reduce the switching losses to improve the THD	IEEE Transactions on power electronics	2018	[122]
Mudasir *et al.*	Hybrid asynchronous PSO-Newton-Raphson (APSO-NR) algorithm	• Eliminate 5^{th} and 7^{th} harmonics in7- level CHB MLI • The algorithm is suitable for both symmetric and asymmetric configurations.	IET Power electronics	2018	[123]

		• The algorithm provides optimal switching angles in fewer iterations than GA, PSO, and Bee algorithms.			
Amin *et al.*	Hybrid interior-point algorithm.	• SHE is confined to low bandwidth applications and becomes increasingly complex as the level count rises. • The switching angles are determined via a restricted minimization problem using harmonic optimization.	IEEE Transactions on power delivery	2012	[124]
Pratik *et al.*	Whale optimization algorithm	• Effective optimization strategies are used to improve inverter performance, convergence rate, and computational overhead.	IET Power electronics	2019	[125]
Abhinandan *et al.*	Modified Particle Swarm Optimization (MPSO)	• SHEPWM switching uses a modified PSO algorithm. • Removing lower-order odd harmonics from the HCMLI output voltage (5th, 7th, 11th, and 13th). • MPSO outperforms GA and PSO.	IEEE Transactions on industrial informatics	2019	[126]

Marcelo *et al.*	Predictive Control Algorithm	• Exceptional performance in terms of dynamic characteristics • For a high number of switching states, reduce the complexity of computations and the range of possible combinations.	IEEE Transactions on industrial electronics	2008	[127]
Mehran *et al.*	Pareto frontier and Multi-Objective Optimization	• Component-level multi-objective optimization. • Performance limits of a Module Integrated Inverter are examined.	IEEE Transactions on power electronics	2014	[128]
Mehrdad *et al.*	Modified Species Based Particle Swarm Optimization	• Enhanced the algorithm's resilience to find the global optimum. • Effective minimization of a large number of specific harmonics.	IEEE Transactions on power electronics	2009	[129]
Neeraj *et al.*	Fuzzy SVPWM	• Obtain high tracking efficiency as well as optimal MPP under adverse operating states. • Over-current protection, Switching losses, current harmonic content. • Compensation of current error and effective utilization of dc-link power.	IET Electric power applications	2018	[130]

Alireza *et al.*	PSO based Memetic Algorithm	• High conversion efficiency and low switching losses. • Harmonic optimization problem.	IET Power electronics	2015	[131]
Yu Liu *et al.*	Real-Time Algorithm	• Mitigate the harmonics • Switching angle optimization under variable voltages. • High-speed convergence.	IEEE Transactions on industrial electronics	2009	[132]
Taghizadeh *et al.*	PSO optimization algorithm	• Selective harmonic elimination in CHB for unequal voltages. • Optimization of switching angles.	IEEE Transactions on industrial electronics	2010	[133]
Ayoub *et al.*	Bee optimization algorithm	• Selective harmonic elimination in CHB • Optimization of switching angles for SHEPWM	IEEE Transactions on power electronics	2012	[134]
Sarika *et al.*	Ant Colony Optimization	• Eliminate 5^{th} and 7^{th} order harmonics in CHBM.L.I. • Reduce THD to lower value as per IEEE519 standards.	International Conference	2016	[135]
Mahmoud *et al*.	Ant Colony Optimization	• Testing of the ACO algorithm to eliminate the harmonics.	25th Iranian conference on	2017	[136]

		• Find the optimum switching angles of 7-Level CHBMLI.	electrical engineering		
Sourabh *et al.*	GA, BEE., PSO, BSA, and DSA algorithms	• Compare different algorithms to optimize the switching angles of CHBMLI • Findings demonstrated ACO has the best efficacy for convergence.	IET Power electronics	2017	[137]
S. Birogul, *et al.*	Hybrid Harris Hawk –Differential Evaluation Algorithm.	• Analyzed the optimal power flow in a grid-connected PV system • The hybrid HH-DE algorithm gives superior performance compared to other algorithms.	IEEE Access	2019	[181]
Dishore *et al.*	Harris Hawk Algorithm	• Switching angle optimization with novel HHO algorithm for 31 level inverter. • Findings are validated with a 1kW grid-connected PV system.	International Transactions on Electrical Energy Systems	2021	[180]
Juan H. Almazan-Covarrubias *et al.*	Improved Dingo Optimization Algorithm	• The modification is conducted to the survival criteria by including a local search to provide a better balance when replacing vectors (dingoes) with a low survival rate.	Applied Sciences	2022	[182]

2.4 SUMMARY OF LITERATURE

From the conducted literature review, it can be concluded that the grid-connected PV inverters have issues such as electromagnetic interference, high harmonic content, high dv/dt, increased switching losses, galvanic isolation, leakage current, high filter requirements, and voltage imbalance on variable voltage inputs which are needed to be addressed. But from the literature, it is clear that the single topology cannot address all these problems. Also, when developing the inverters, it becomes necessary to consider that the topology is more economical with fewer circuit components and reduced circuit complexity. The key highlight features concluded from the literature are:

- *NPC ML Inverter:* The rise in the number of levels considerably increases the number of clamping diodes; inverse retrieval times of the clamping diode render this topology not feasible to develop a medium voltage converter with more levels.
- *Flying Capacitor ML Inverter:* Inadequate for MV and HV applications because it uses many capacitors requiring circuits for prior charging and balancing, furthermore a large dc-link capacitor needed for single-cell topology limits its application to medium and high voltages, particularly to solar PV applications, where different PV panels are to be connected in series. These huge number of series-connected PV panels will decrease the overall system efficiency due to common MPPT and series resistance.
- *CHB ML Inverter:* The CHB is getting rid of more PV modules; however, the continuous variation of the module parameters and the partial shading causes mismatch problems. These mismatch problems create imbalance and result in a low power quality of the grid.
- *LDML Inverter:* Additional components are only for higher-level operation in the primary circuit, the components required for the proposed MLI is, therefore, less than the traditional working topologies at a higher level, but the voltage blocking capacity of the polarity generator part is more than the level generation part.
- *Modified LDML Inverter:* Utilize less switch count in its topology, but it cannot

work under conditions of asymmetric source as the sources are transversal with balanced capacitors.

- 4-arm c*urrent source inverter (CSI):* Modified CSI nullifies the leakage current of the ground without using an isolation transformer that increases overall efficiency and reduces system cost compared to the conventional CSI-based solar grid.
- *Z-Source transformerless inverter:* A common-mode current is a major issue in transformerless topologies due to the lack of galvanic insulation.
- *H4 Topology:* The H4 cascaded bridge has good reliability, but the leakage current cannot be reduced.
- *Conventional two-level inverters:* This topology gives the economic operation of the inverter, but the harmonic content is very high.
- *Common mode grounding topology:* Improve the efficiency of dc bus but require a two-stage energy transfer that increases losses.
- *Multi-Phase NPC-based 3-Level Inverter:* Effective voltage balance is achieved in NPC, but increased switching losses are limited in practice to applicability.
- *Bidirectional Switch H-Bridge MLIs:* Voltage blocking ability is more but switching burden is more due to multiple switching in each half output voltage cycle, which increases switching losses.

Optimization is the most efficient resource used for achieving the optimal maximum or minimum as a mathematical function. Nowadays, the solution is obtained with different optimization algorithms in every engineering & non-engineering research problem and has become one of the massive areas of application. Hence a lot of research continues to find new algorithms and hybrid algorithms to minimize the current system's limitations and achieve better and more reliable performance. From the conducted literature survey, the following points are concluded.

- *Particle Swarm Optimization Algorithm:* PSO associates with local minima problems for fewer initial populations, avoiding local minima problems a vast number of initial populations is needed to generate.
- *Binary PSO:* The BPSO (Binary Particle Swarm Optimization Algorithm) is characterized by its speed, precision, and efficiency, making it well suited for

online implementation.

- *Genetic Algorithm:* The convergence speed of GA is too slow, hence only applied for online implementations.
- *Bat Algorithm:* Solutions to have a close probability of achieving global minimum runs for 1, 2, 5, and 10 times, and this probability is greater than the same runs for GA.
- *Immune Genetic Algorithm (IGA):* IGA is an advanced genetic algorithm that is still slow to converge; problems are associated with global minima.
- *Hybrid GA and PSO:* This hybrid approach gives superior convergence.
- *Hybrid APSO-NR algorithm:* In comparison to GA, PSO, and BEE algorithms, this technique gives optimal switching angles in a less number of iterations.
- *Binary Search Algorithm:* BSA is a global search algorithm focused on evolutionary computation, the ability to solve the higher-order problem of nonlinear, non-differentiable optimization.
- *Whale optimization algorithm:* Much determined compared to other algorithms, but sometimes it does not work better.
- *Predictive Control Algorithm:* Has good dynamic behavior, which reduces the number of potential combinations and the complexity of computations for a high number of switching states.
- *Real-Time Algorithm:* Switching angle optimization under variable voltages, high-speed convergence.
- *Bat Algorithm:* Easy to implement and requires fewer execution efforts and search for better solutions at a high convergence rate, and due to local optima, this algorithm confronts improper convergence.
- *Harris Hawk Optimization:* Flexible structure, high performance, high speed of convergence due to dynamic behaviors hawks of and high-quality result.
- *Hybrid Harris Hawk Differential Evaluation Optimization:* The balance between the exploratory tendency and the exploitative tendency of the algorithm is well consistent.
- *Improved Dingo Optimization Algorithm:* Benchmarked with some unimodal functions to illustrate its better exploitation capabilities.

All these optimization algorithms are discussed for optimizing the switching angles of the multilevel inverter. The process is described in the flow chart shown in figure 2.1.

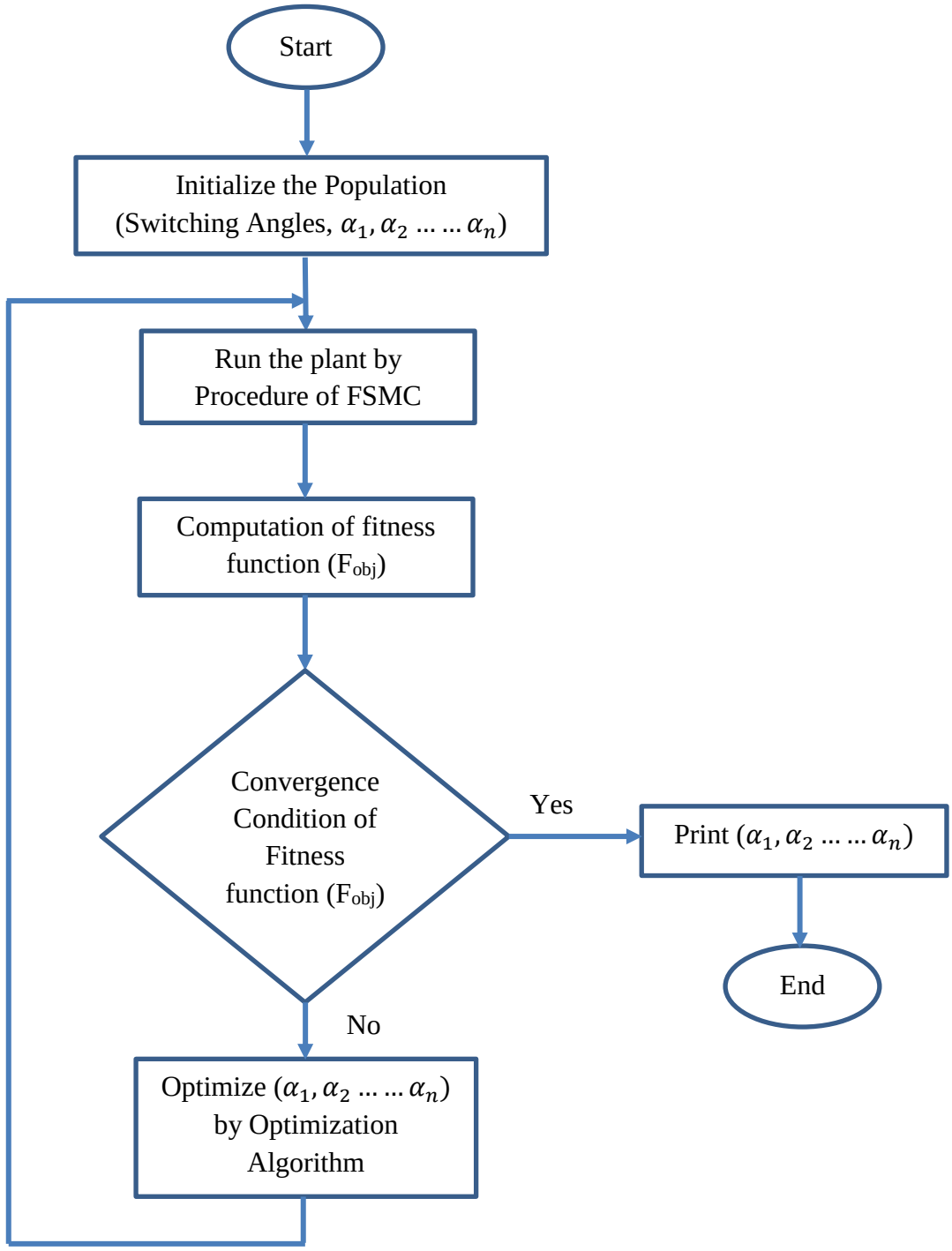


Figure 2.1 Process of finding optimal switching angles of the inverter using optimation algorithms

The flow diagram in figure 2.1 represents the process of finding the optimal switching angle of the multilevel inverter using nature-inspired optimization algorithms.

From the above literature, it is observed that the investigation and technological developments of MLIs are essential to improve the power quality of the PV system. The nonlinear properties of the three-level inverters limit their use in PV applications since they do not meet the grid codes. It also requires the use of an LC filter for improving the quality of waveforms per the grid.

These problems associated with the three-level inverter are addressed by designing modular multilevel inverters (MMI) with reduced components. These inverters are applicable to medium and high-power applications even though the switching control method is a significant concern for pulse generation for MMIs. The use of high-frequency switching control still creates voltage stress on the power switches, which further affects the power quality of the output of the inverter. However, switch reduction, harmonic reduction, and grid integration are three concerns observed in traditional multilevel inverters and their modulation schemes.

With the increase in levels, the power switches also increase in conventional multilevel inverters, which increases the components of the gate driver and control circuit. Hence the complexity of triggering power switches increases, which affects the inverter's reliability.

The switching control method employed for the multilevel inverter is another critical concern for enhancing the power quality at the output. Usually, the high frequency switching modulation techniques causes more power losses and thereby reduce the inverter efficiency. The total harmonic distortion is reduced at the inverter output by implementing high switching frequency control, but the switching losses get increased during the switching transitions.

2.5 CHAPTER SUMMARY

A comprehensive review of significant development, topology, control techniques, and applications of multi-level inverters has been carried out in this chapter. The review reveals that:

Multilevel inverters are employed in the grid-connected PV system, but the increased number of components makes it both complex and costly. Symmetric MLIs with reduced switches are not suited for PV applications and have mismatch problems.

The new asymmetric MLI topologies are unsuitable for producing all possible voltage levels from the asymmetric dc sources, moreover, the presence of many capacitors and diodes in the circuit leads to voltage imbalance and increased inverse recovery times of the diode.

The PWM switching approach is critical to MLI performance, but the high-frequency switching modulation causes more switching losses and THD. The optimization algorithms have their own advantages and limitations in convergence rate, applicability, dynamic behavior, local and global minima, etc. Very limited literature is available to use optimization techniques to control the MLI on the most recent reduced switch topologies. Moreover as per the "No free lunch theorem of optimization," no single optimization algorithm will give a solution to all types of problems.

CHAPTER-3

DESIGN OF 15-LEVEL ASYMMETRIC MULTILEVEL INVERTER & SWITCHING CONTROL

3.1 INTRODUCTION

In new industrial and academic research paradigms, multilevel inverters have evolved dramatically because of their ability to produce high-quality output at reduced costs. Philosophers have worked on lowering inverter costs by utilizing fewer components. The main aim of a multilevel topology of the inverter is to incorporate the harmonic profile into the IEEE-519 standard, which eliminates the need for heavy filters [138]. Multiple targets such as minimum THD, low dv/dt stress, and lower common-mode voltages are available to guarantee the use of electric motors. Electromagnetic interference (EMI) problems are less frequent on the multilevel inverters than conventional 2-level and 3-level inverters [139]. In general, researchers aimed at increasing the basic units in series or cascading of the basic unit to get more output voltage levels to improve the inverter's efficiency at lower THD. The inverter perceives its usefulness in PV-fed UPS, propulsion systems, integration of green energy sources, airplanes, battery-powered vehicles, etc. A simple control strategy is necessary to reduce the complexity of multilevel inverters. Therefore, the investigators focused on efficient topology architecture and modulation [140].

This chapter presented an asymmetric MLI structure with minimum switch count by avoiding the use of bidirectional switches, clamping diodes, and capacitors in its design. In addition, the proposed converter does not affect diode reverse recovery times, capacitor voltage balancing and uses a simple gate control circuit due to the absence of bidirectional switches [141-144]. The proposed inverter uses low switching frequency control to reduce lower order harmonics [145]. The Newton Raphson approach finds a viable solution to the non-linear SHEPWM equations for obtaining the inverter's optimum switching angles. The proposed inverter is operated for different possible levels (seven-level, eleven-level, fifteen-level), and the corresponding THDs are analyzed.

3.2 DESIGN OF PROPOSED ASYMMETRIC 15-LEVEL INVERTER

This research presented a simple design topology of a 15-level asymmetric inverter suitable to variable dc sources such as SPV systems. The basic cell configuration of the suggested model is given in figure 3.1. It has a single voltage source in series with a power switch connected across the bypass diode. During the switch 'S' is turned ON, the source voltage 'V' appears at the load, then $V_{dc\text{-}out}$ becomes source voltage 'V', and while the switch 'S' is turned OFF, then the source voltage is isolated from the load; hence $V_{dc\text{-}out}$ equals to '0'.

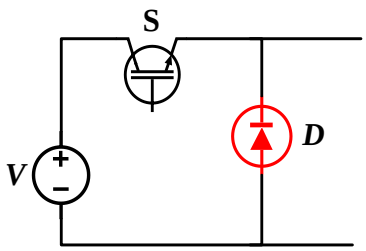


Figure 3.1 Basic cell structure

Basic cell structures are cascaded, as shown in figure 3.2 for 'n' cell structure of the suggested configuration of the inverter, known as the primary circuit.

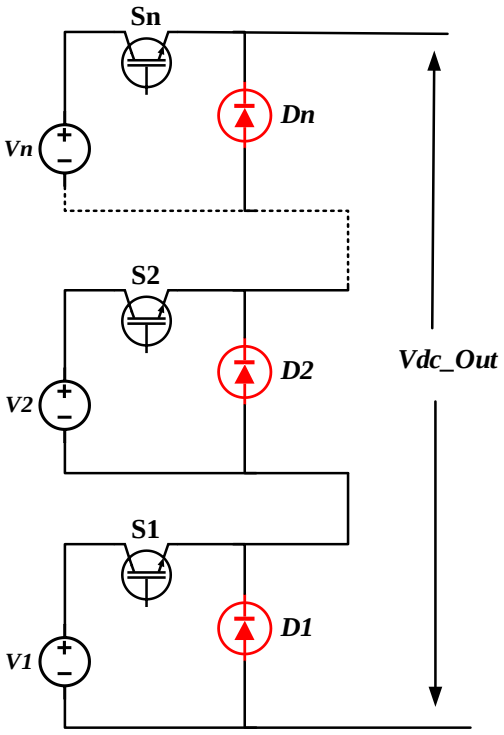


Figure 3.2 'n' cell cascaded primary circuit

However, this 'n' cell configuration can generate a multilevel output only with a positive polarity. The inverter's bidirectional output can be achieved by connecting an H-bridge auxiliary circuit to the primary circuit's output, as illustrated in figure 3.3. Therefore, the complete cycle of the output's +ve and -ve polarity is achieved by combining the primary and auxiliary circuits. This structure synthesizes 15-output voltage levels with 7-positive, 7-negative, and zero levels.

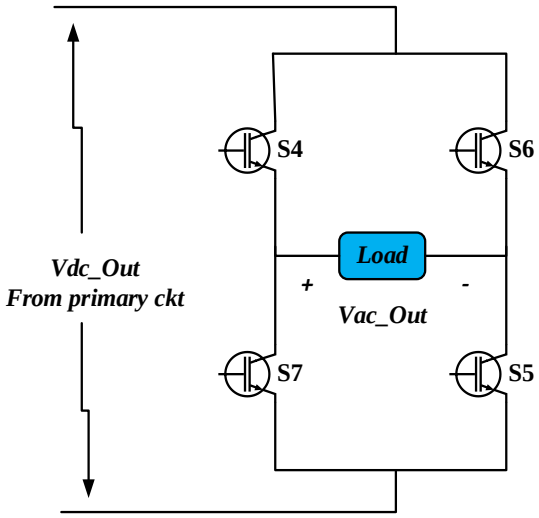


Figure 3.3 Auxiliary circuit

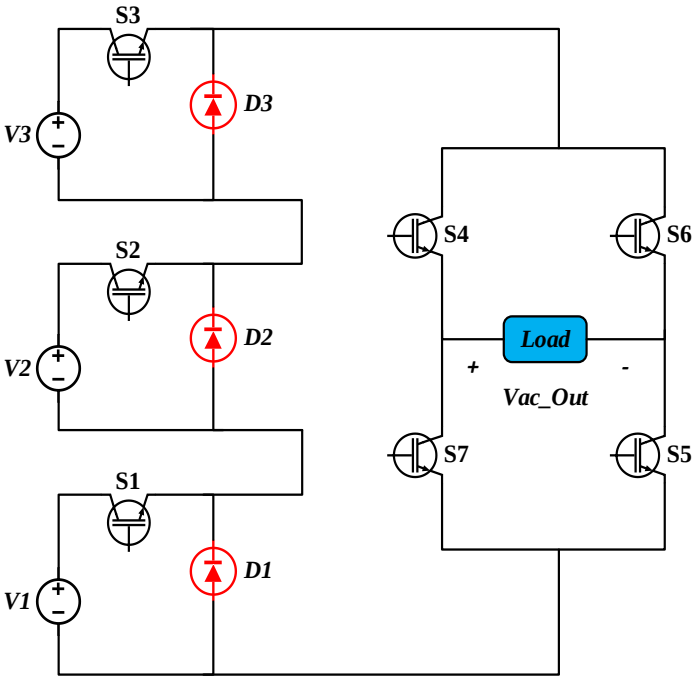


Figure 3.4 Proposed 15-level asymmetric inverter

Figure 3.4 depicts the suggested 15-level multilevel inverter structure. In its design, the primary circuit is cascaded with three basic cell structures and interconnected across the auxiliary circuit, which uses three dc sources, seven controlled switches (IGBTs), and 3-diodes. The proposed topology and switching path choices are appropriately configured so that IGBTs or diodes can never dead short circuit with the dc sources. The rating of numerous dc sources depends on the magnitude of output levels. The dc source reduced voltage rating specifies V_{dc} step voltage at the output. Different potential dc voltage sources combinations are presented in table 3.1.

Table 3.1 Choice of dc sources for suggested topology

Method of Selection	**Choice of DC Sources**	**No of Steps**	**No of Levels**	**Max. O/p Voltage**
Equal Magnitude	$V_1=V_2=V_3=V_{dc}$	4	7	$3V_{dc}$
Unequal Magnitude	$V_1= V_{dc}$ $V_2=V_3=2V_{dc}$	6	11	$5V_{dc}$
Binary Approach	$V_1= V_{dc}$ $V_2= 2V_{dc}$ $V_3= 4V_{dc}$	8	15	$7V_{dc}$

The binary approach is considered for this study among the above three choices of dc source selection. Since multilevel inverters work with high efficiency at low switching and conduction losses, output voltage levels significantly increase with the few dc sources and power switches. Therefore, the choice of voltages for 15-level output is as follows,

$$V_1= V_{dc}, \quad V_2= 2V_{dc}, \quad V_3= 4V_{dc}$$

This approach also offers asymmetrical operation to multilevel inverter ideal for variable PV voltages due to variable solar irradiance. The switching sequence for different output step voltages varies from +7 Vdc to -7 Vdc, including the '0' voltage level.

The switches S_4 and S_5 in the auxiliary circuit continuously conduct 7-levels of +ve half cycle of output voltage and switches S6 & S7 conduct for 7-levels of a -ve half cycle of output. The '0' output level is obtained by either short circuit of load with switches S_4 & S_6 is ON, or S_5 & S_7 is ON. Thus, the fifteen-level output voltage is obtained from the proposed converter by operating the primary and axillary circuits according to the switching conditions described in table 3.2.

Table 3.2 Asymmetric switching sequences and output voltage levels of proposed 15-level inverter

ON Switches	**Power flow path**	**Output voltage level**
S_1, S_2, S_3, S_4 & S_5	$V_1^+ \rightarrow S_1 \rightarrow V_2 \rightarrow S_2 \rightarrow V_3 \rightarrow S_3 \rightarrow S_4 \rightarrow$ Load $\rightarrow S_5 \rightarrow V_1^-$	$+7V_{dc}$
S_2, S_3, S_4 & S_5	$V_2^+ \rightarrow S_2 \rightarrow V_3 \rightarrow S_3 \rightarrow S_4 \rightarrow$ Load $\rightarrow S_5 \rightarrow D_1 \rightarrow V_2^-$	$+6V_{dc}$
S_1, S_3, S_4 & S_5	$V_1^+ \rightarrow S_1 \rightarrow D_2 \rightarrow V_3 \rightarrow S_3 \rightarrow S_4 \rightarrow$ Load $\rightarrow S_5 \rightarrow V_1^-$	$+5V_{dc}$
S_3, S_4 & S_5	$V_3^+ \rightarrow S_3 \rightarrow S_4 \rightarrow$ Load $\rightarrow S_5 \rightarrow D_1 \rightarrow D_2 \rightarrow V_3^-$	$+4V_{dc}$
S_1, S_2, S_4 & S_5	$V_1^+ \rightarrow S_1 \rightarrow V_2 \rightarrow S_2 \rightarrow D_3 \rightarrow S_4 \rightarrow$Load $\rightarrow S_5 \rightarrow V_1^-$	$+3V_{dc}$
S_2, S_4 & S_5	$V_2^+ \rightarrow S_2 \rightarrow D_3 \rightarrow S_4 \rightarrow$ Load $\rightarrow S_5 \rightarrow D_1 \rightarrow V_2^-$	$+2V_{dc}$
S_1, S_4 & S_5	$V_1^+ \rightarrow S_1 \rightarrow D_2 \rightarrow D_3 \rightarrow S_4 \rightarrow$ Load $\rightarrow S_5 \rightarrow V_1^-$	$+V_{dc}$
S_4 & S_6 (or) S_5 & S_7	$S_4 \rightarrow$ Load $\rightarrow S_6 \rightarrow S_4$ (or) $S_5 \rightarrow$ Load $\rightarrow S_7 \rightarrow S_5$	0
S_1, S_6 & S_7	$V_1^+ \rightarrow S_1 \rightarrow D_2 \rightarrow D_3 \rightarrow S_6 \rightarrow$ Load $\rightarrow S_7 \rightarrow V_1^-$	$-V_{dc}$
S_2, S_6 & S_7	$V_2^+ \rightarrow S_2 \rightarrow D_3 \rightarrow S_6 \rightarrow$ Load $\rightarrow S_7 \rightarrow D_1 \rightarrow V_2^-$	$-2V_{dc}$
S_1, S_2, S_6 & S_7	$V_1^+ \rightarrow S_1 \rightarrow V_2 \rightarrow S_2 \rightarrow D_3 \rightarrow S_6 \rightarrow$Load $\rightarrow S_7 \rightarrow V_1^-$	$-3V_{dc}$
S_3, S_6 & S_7	$V_3^+ \rightarrow S_3 \rightarrow S_6 \rightarrow$ Load $\rightarrow S_7 \rightarrow D_1 \rightarrow D_2 \rightarrow V_3^-$	$-4V_{dc}$
S_1, S_3, S_6 & S_7	$V_1^+ \rightarrow S_1 \rightarrow D_2 \rightarrow V_3 \rightarrow S_3 \rightarrow S_6 \rightarrow$ Load $\rightarrow S_7 \rightarrow V_1^-$	$-5V_{dc}$
S_2, S_3, S_6 & S_7	$V_2^+ \rightarrow S_2 \rightarrow V_3 \rightarrow S_3 \rightarrow S_6 \rightarrow$ Load $\rightarrow S_7 \rightarrow D_1 \rightarrow V_2^-$	$-6V_{dc}$
S_1, S_2, S_3, S_6 & S_7	$V_1^+ \rightarrow S_1 \rightarrow V_2 \rightarrow S_2 \rightarrow V_3 \rightarrow S_3 \rightarrow S_6 \rightarrow$ Load $\rightarrow S_7 \rightarrow V_1^-$	$-7V_{dc}$

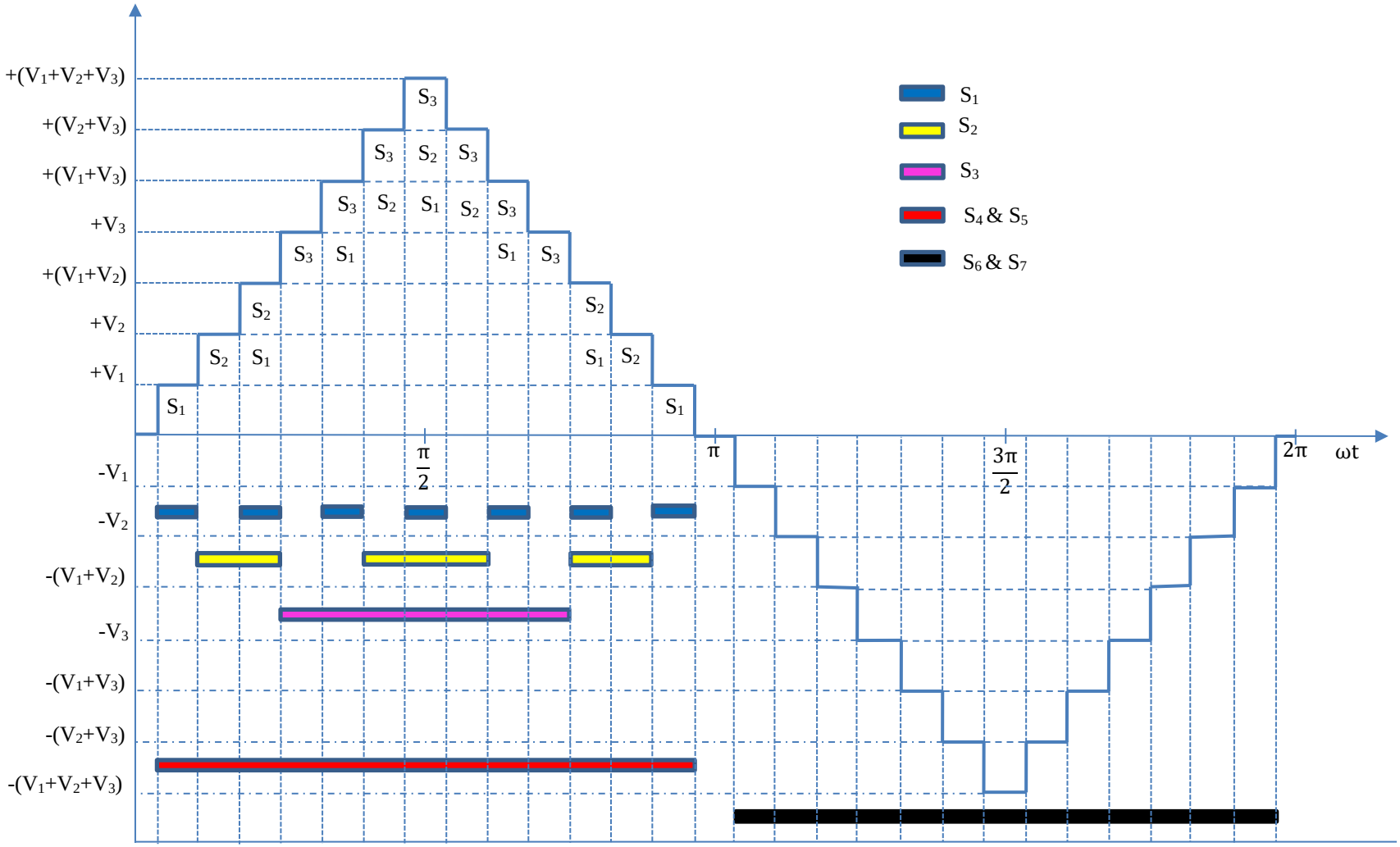
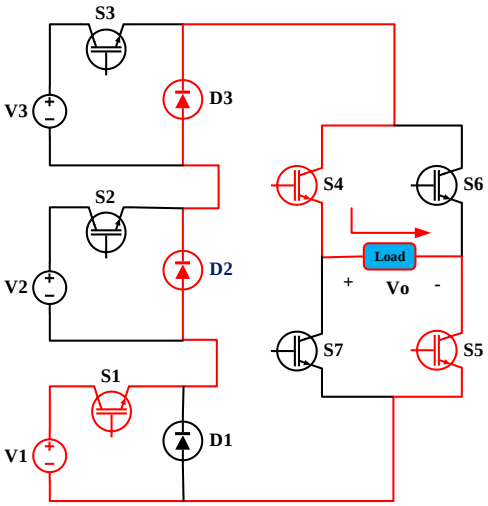
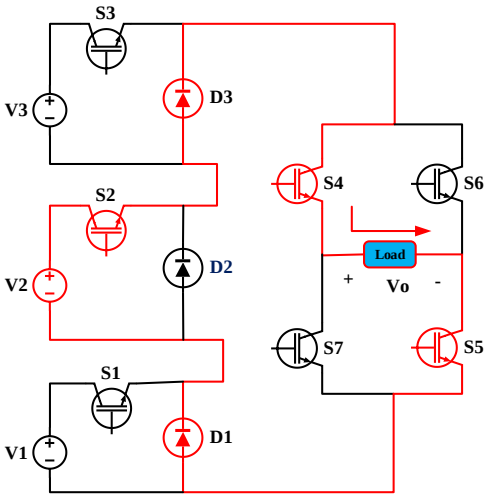


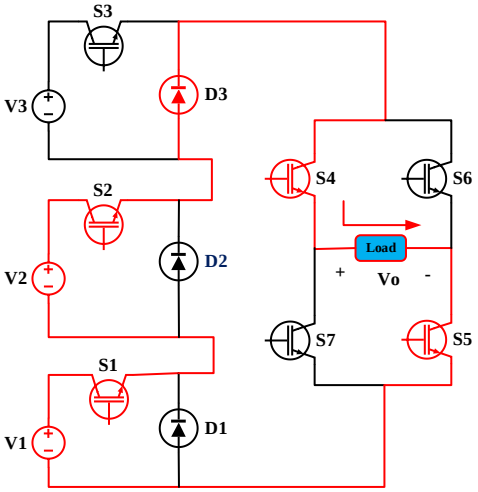
Figure 3.5 The approximated waveform of the proposed 15-level inverter and its switching pattern.



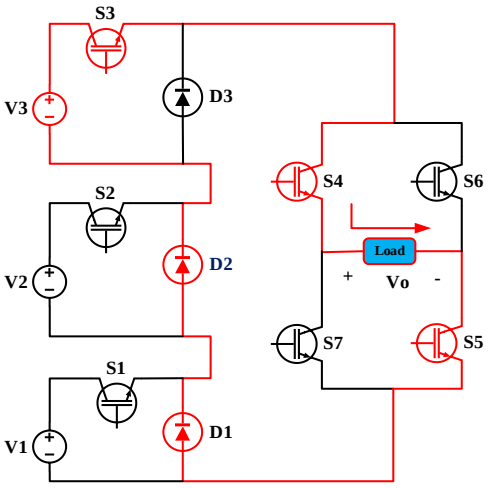
(a) Mode-1 ($V_0 = V_1$)



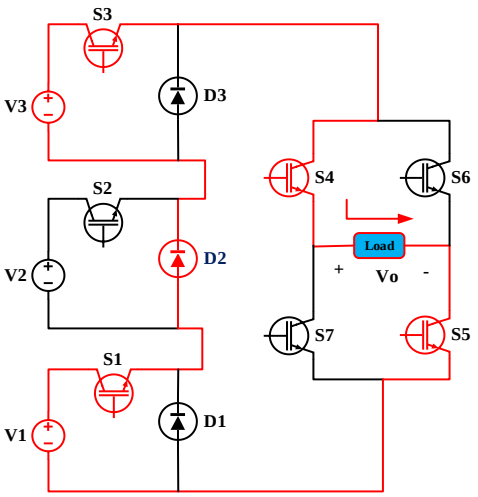
(b) Mode-2 ($V_0 = V_2$)



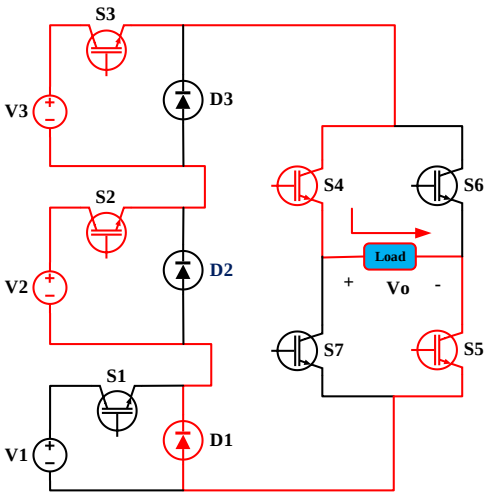
(c) Mode-3 ($V_0 = V_1 + V_2$)



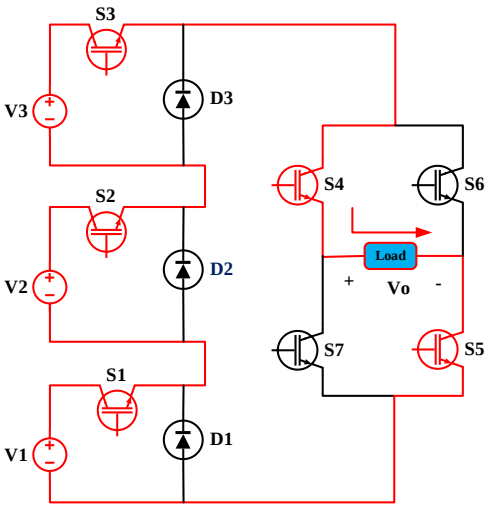
(d) Mode-4 ($V_0 = V_3$)



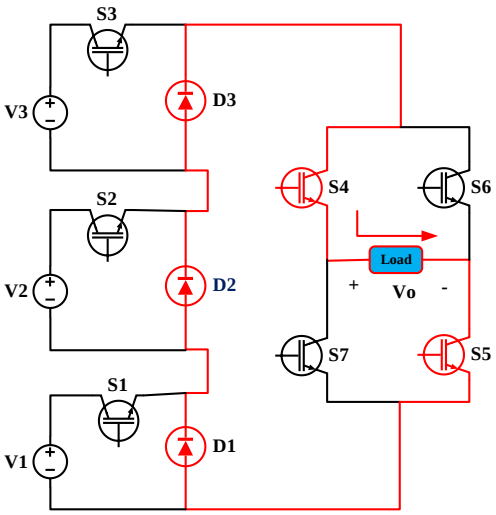
(e) Mode-5 ($V_0 = V_1 + V_3$)



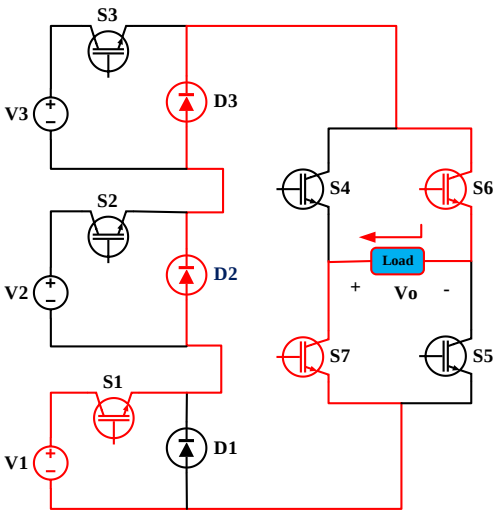
(f) Mode-6 ($V_0 = V_2 + V_3$)



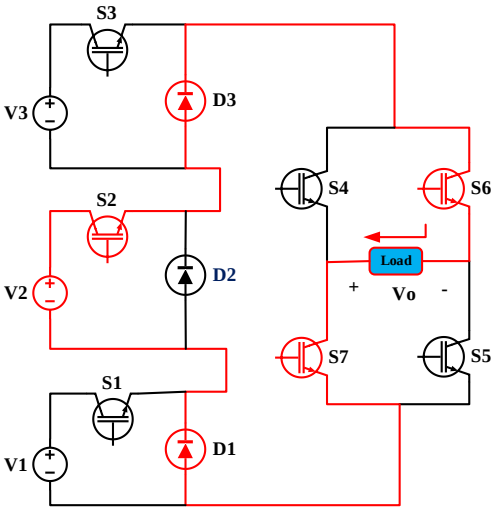
(g) Mode-7 ($V_0 = V_1 + V_2 + V_3$)



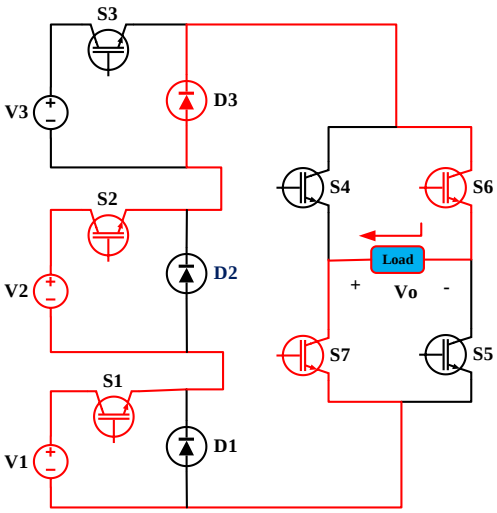
(h) Mode-8 ($V_0 = 0V$)



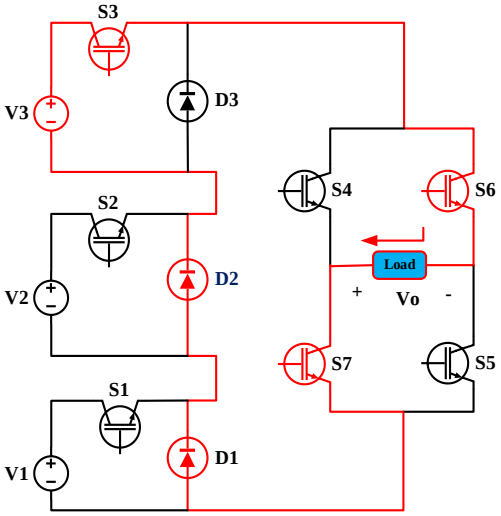
(i) Mode-9 ($V_0 = -V_1$)



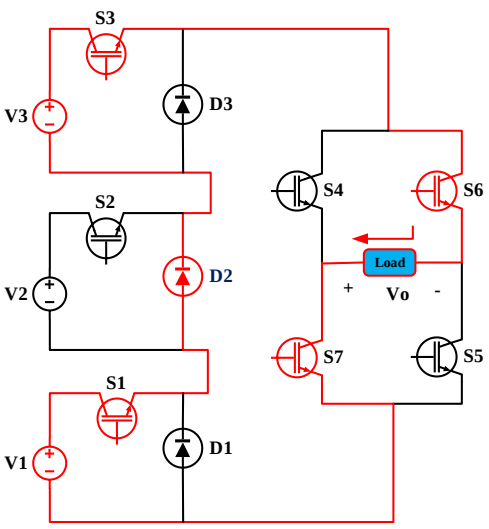
(j) Mode-10 ($V_0 = -V_2$)



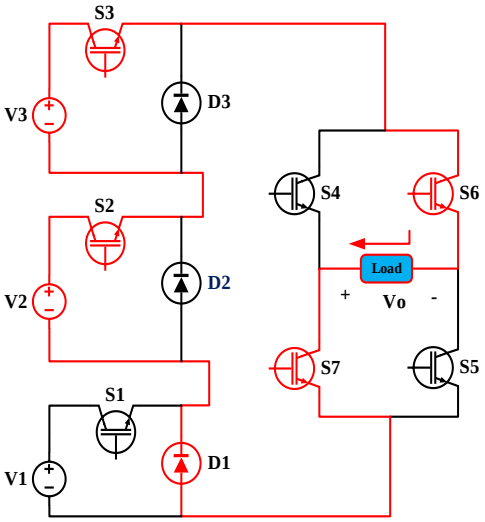
(k) Mode-11 ($V_0 = -(V_1 + V_2)$)



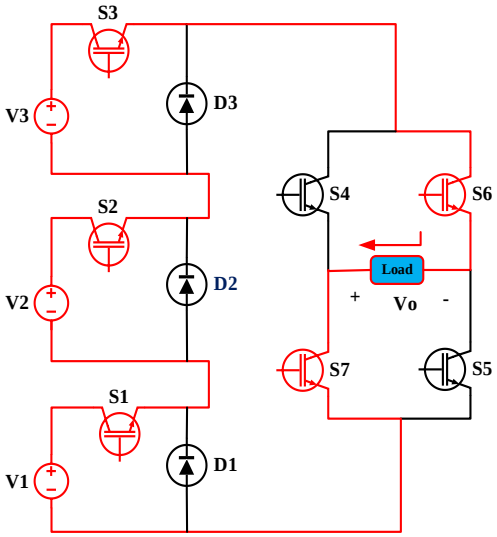
(l) Mode-12 ($V_0 = -V_3$)



(m) Mode-13 ($V_0 = -(V_1 + V_3)$)



(n) Mode-14 ($V_0 = -(V_2 + V_3)$)



(o) Mode-15 ($V_0 = -(V_1 + V2 + V3)$)

Figure 3.6 Modes of operation of proposed 15-level inverter. (a) $V_0 = V_1$, (b) $V_0 = V_2$, (c) $V_0 = V_1 + V_2$, (d) $V_0 = V_3$, (e) $V_0 = V_1 + V_3$, (f) $V_0 = V_2 + V_3$, (g) $V_0 = V_1 + V_2 + V_3$, (h) $V_0 = 0V$, (i) $V_0 = -V_1$, (j) $V_0 = -V_2$, (k) $V_0 = -(V_1 + V_2)$, (l) $V_0 = -V_3$, (m) $V_0 = -(V_1 + V_3)$, (n) $V_0 = -(V_2 + V_3)$), (o) $V_0 = -(V_1 + V2 + V3)$

The ON-OFF switching states of all seven switches are represented in figure 3.5, and different modes of operation of the proposed 15-level inverter are shown in figure 3.6.

3.3 COMPARISON WITH OTHER TOPOLOGIES

A reduced switch multilevel inverter's primary goal is to increase the number of levels using a few electronic components. Consequently, several contrasts were established between the suggested topology and other cascaded inverters of a similar kind, including switch count, the number of diodes, and dc sources.

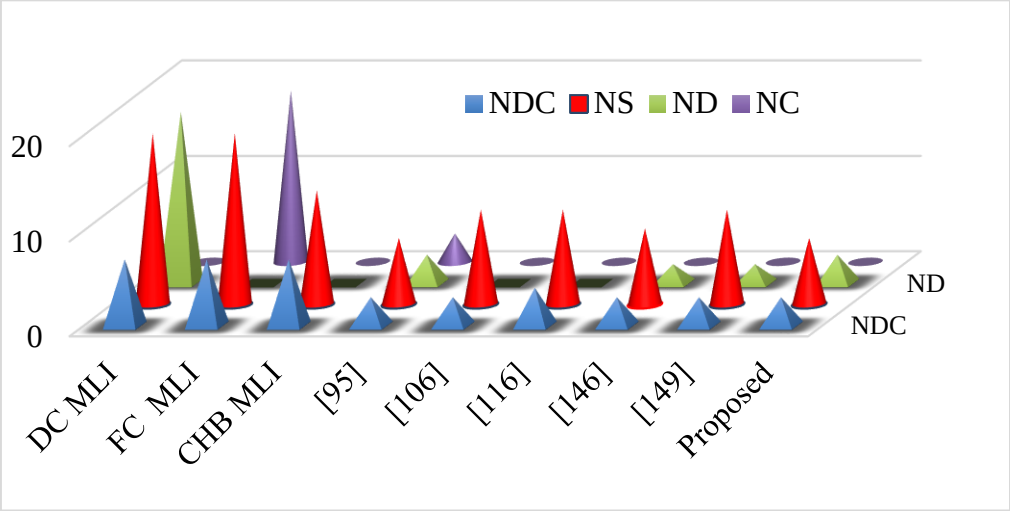


Figure 3.7 Comparison between the existing 15-level asymmetric topologies and proposed 15-level inverter

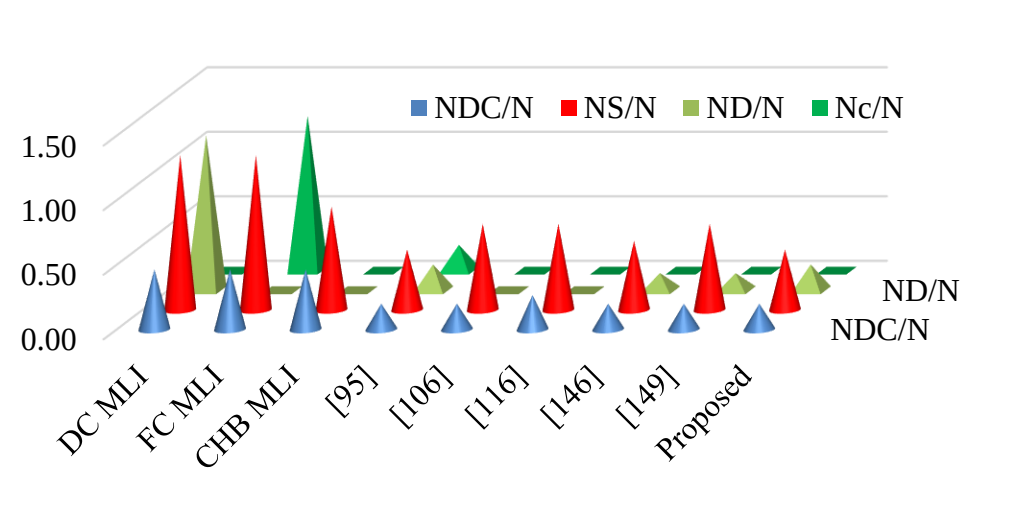
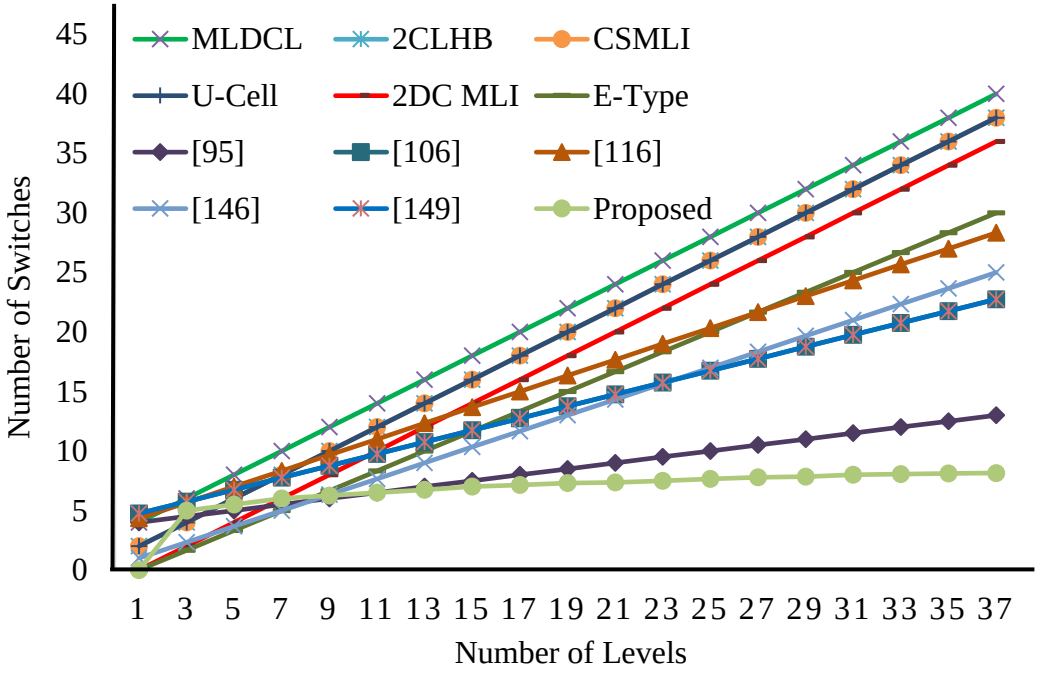


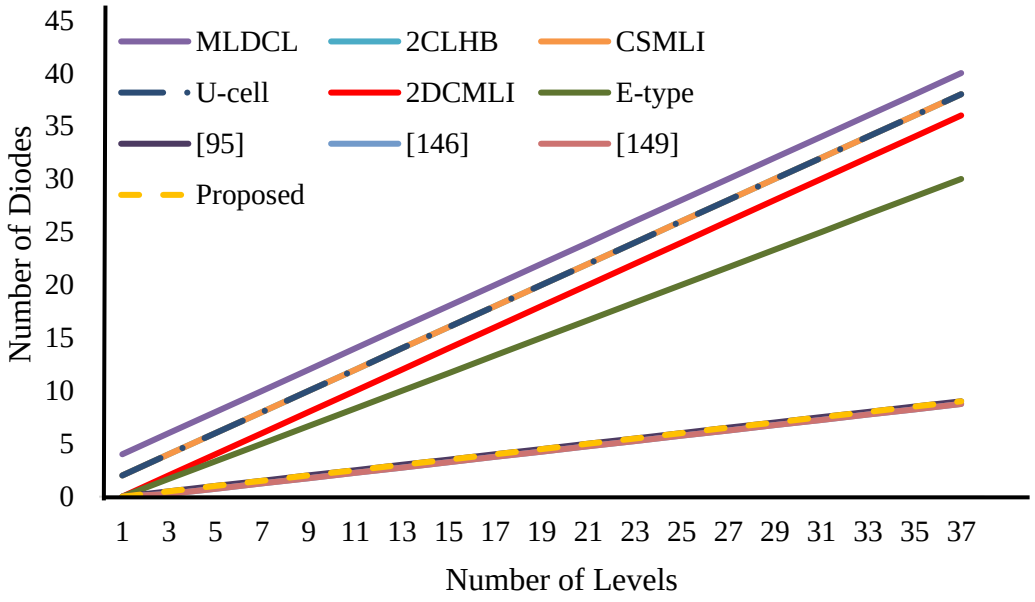
Figure 3.8 DC sources, switches, diodes & capacitor ratio comparison for other 15-level inverters with proposed 15-level inverter

The comparison between the number of dc sources, switches, diodes, and capacitors required for various topologies cited in this thesis with the proposed topology

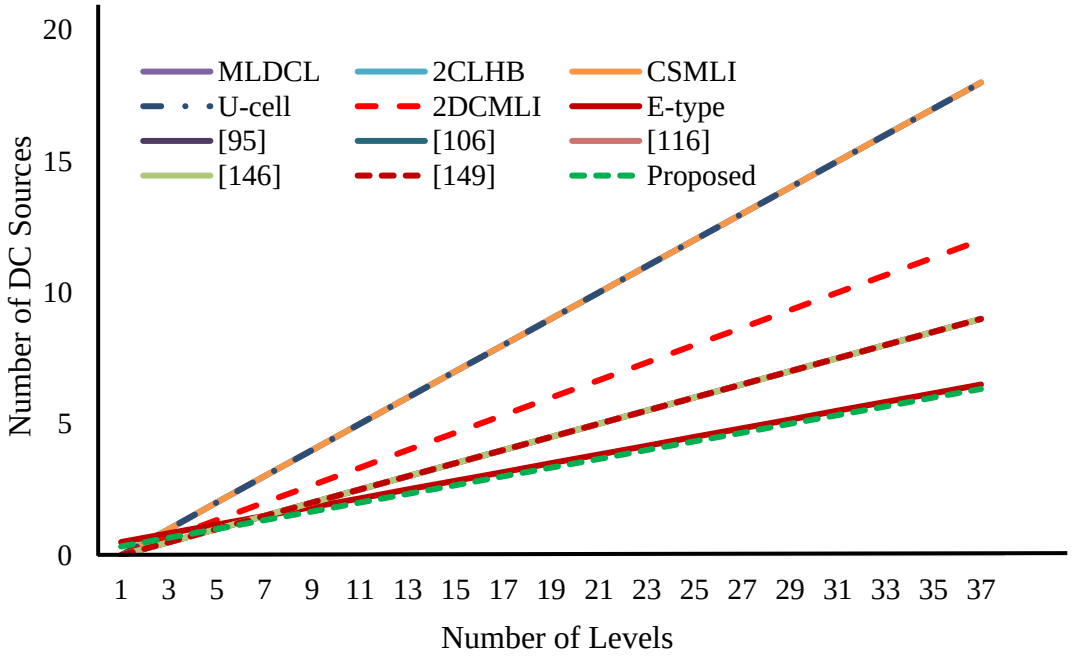
is shown in figure 3.7. This distinction demonstrates that the suggested topology uses fewer devices in its design. Different components required are presented in figure 3.8, and figure 3.9 shows the comparison between the power switches, diodes, and dc sources necessary for the proposed inverter with other topologies.



(a) Required number of switches Vs number of levels



(b) Required number of diodes Vs number of levels



(c) Required number of dc sources Vs number of levels

Figure 3.9 Comparison between the design components of various MLIs

3.4 FUNDAMENTAL SWITCHING FREQUENCY CONTROL (SHEPWM)

Fundamental switching frequency control is one of the best PWM control methods for multilevel converters. FSFC control can be achieved based on selective harmonic elimination (SHEPWM) pulse width modulation [146-148]. Generally, the waveform of multilevel inverter output is expressed using Fourier series expansion. The generalized expression is given in equation (3.1).

$$V(\omega t) = \sum_{n=1}^{\infty} V_n \sin(n\omega t) \tag{3.1}$$

Here, V_n= n^{th} harmonic voltage magnitude. Due to the odd symmetry of the quarter-wave, the even-order harmonics become zero. Therefore the expression for V_n becomes,

$$V_n = \begin{cases} \dfrac{4V_{dc}}{n\pi} \sum_{i=1}^{k} \cos(n\alpha_i); \; for \;\; odd \;\; values \;\; of \;\; 'n' \\ 0; \;\; for \;\; even \;\; values \;\; of \;\; 'n' \end{cases} \tag{3.2}$$

Where, α_i is the switching angles of i[th] harmonic and is between 0˚-90˚ (i.e. $0<\alpha_i<\frac{\pi}{2}$).

SHEPWM aims to suppress lower-order harmonics, whereas harmonic filters remove the remaining harmonics. This research developed a 15-level asymmetric inverter with a fundamental switching frequency control scheme to conceal the 5[th], 7[th], 11[th], 13[th], 17[th], 19[th] harmonic voltages. The application of 15-level output will reduce the size of the harmonic filters as the prominent harmonics from the 5[th] to 19[th] harmonics are controlled. By expanding equation (3.2) for odd values of 'n', equation (3.3) can be obtained

$$\left.\begin{aligned}
\frac{4V_{dc}}{\pi}\left[\cos\alpha_1+\cos\alpha_2+\cdots\ldots+\cos\alpha_7\right] &= V_1\\
\frac{4V_{dc}}{5\pi}\left[\cos5\alpha_1+\cos5\alpha_2+\cdots\ldots+\cos5\alpha_7\right] &= V_5\\
\frac{4V_{dc}}{7\pi}\left[\cos7\alpha_1+\cos7\alpha_2+\cdots\ldots+\cos7\alpha_7\right] &= V_7\\
\frac{4V_{dc}}{11\pi}\left[\cos11\alpha_1+\cos11\alpha_2+\cdots\ldots+\cos11\alpha_7\right] &= V_{11}\\
\frac{4V_{dc}}{13\pi}\left[\cos13\alpha_1+\cos13\alpha_2+\cdots\ldots+\cos13\alpha_7\right] &= V_{13}\\
\frac{4V_{dc}}{17\pi}\left[\cos17\alpha_1+\cos17\alpha_2+\cdots\ldots+\cos17\alpha_7\right] &= V_{17}\\
\frac{4V_{dc}}{19\pi}\left[\cos19\alpha_1+\cos19\alpha_2+\cdots\ldots+\cos19\alpha_7\right] &= V_{19}
\end{aligned}\right\} \quad (3.3)$$

Where, $V_5, V_7, V_{11}, V_{13}, V_{17}, V_{19}$ are the harmonic voltages of 5[th], 7[th], 11[th], 13[th], 17[th], 19[th] harmonics, respectively, which are required to suppress to reduce the THD of output voltage. Therefore, these are equated to zero, and the resulting equation can be represented in equation (3.5). The fundamental voltage component in equation (3.3) is equated to modulation index corresponding PWM scheme, which can be written as:

$$M=\frac{V_1}{V_{1\max}} \quad (3.4)$$

Where,

V_{1max} = Peak fundamental voltage.

$$V_{1\max}=\frac{4kV_{dc}}{\pi}$$

V_1 = Actual fundamental voltage.

k = Degree of freedom = $(N-1)/2$.

N = No of output voltage levels.

By combining (3.3) and (3.4) the above conditions can be written as follows.

$$\left.\begin{aligned}
&\frac{4V_{dc}}{\pi}(\cos\alpha_1+\cos\alpha_2+\cos\alpha_3+\cos\alpha_4+\cos\alpha_5+\cos\alpha_6+\cos\alpha_7)=M\\
&\frac{4V_{dc}}{5\pi}(\cos 5\alpha_1+\cos 5\alpha_2+\cos 5\alpha_3+\cos 5\alpha_4+\cos 5\alpha_5+\cos 5\alpha_6+\cos 5\alpha_7)=0\\
&\frac{4V_{dc}}{7\pi}(\cos 7\alpha_1+\cos 7\alpha_2+\cos 7\alpha_3+\cos 7\alpha_4+\cos 7\alpha_5+\cos 7\alpha_6+\cos 7\alpha_7)=0\\
&\frac{4V_{dc}}{11\pi}(\cos 11\alpha_1+\cos 11\alpha_2+\cos 11\alpha_3+\cos 11\alpha_4+\cos 11\alpha_5+\cos 11\alpha_6+\cos 11\alpha_7)=0\\
&\frac{4V_{dc}}{13\pi}(\cos 13\alpha_1+\cos 13\alpha_2+\cos 13\alpha_3+\cos 13\alpha_4+\cos 13\alpha_5+\cos 13\alpha_6+\cos 13\alpha_7)=0\\
&\frac{4V_{dc}}{17\pi}(\cos 17\alpha_1+\cos 17\alpha_2+\cos 17\alpha_3+\cos 17\alpha_4+\cos 17\alpha_5+\cos 17\alpha_6+\cos 17\alpha_7)=0\\
&\frac{4V_{dc}}{19\pi}(\cos 19\alpha_1+\cos 19\alpha_2+\cos 19\alpha_3+\cos 19\alpha_4+\cos 19\alpha_5+\cos 19\alpha_6+\cos 19\alpha_7)=0
\end{aligned}\right\} \quad (3.5)$$

The switching angles must not violate the constraints,

$$\alpha_1<\alpha_2<\alpha_3<\alpha_4<\alpha_5<\alpha_6<\alpha_7<\frac{\pi}{2} \quad (3.6)$$

The set of non-linear equations in (3.5) can be solved using constraint (3.6) to obtain the switching angles required for the fifteen-level inverter. These equations can be solved using a fundamental switching frequency control method and optimization methods to optimize the inverter's switching angles. Any optimization strategy requires developing an objective function related to the variables to be evaluated [149]. The primary objectives are,

a. To obtain the value of the base voltage equivalent to any preset or expected value.
b. To suppress or reduce a few harmonics of lower order.

The inverter's switching angles influence the output harmonic voltages. The generalized harmonic voltage objective function (OF) consists of the following form to achieve the above objectives:

$$OF = \min_{\alpha_k} \left\{ \left(100 \times \left(\frac{V_1^* - V_1}{V_1^*} \right)^4 \right) + \sum_{k=2}^{N} \frac{1}{h_k} \left(50 \times \frac{V_{h_k}}{V_1} \right)^2 \right\} \quad (3.7)$$

To minimize the 5th, 7th, 11th, 13th, 17th, 19th harmonics, the above objective function can be taken as:

$$OF = 100 \times \left(\frac{V_1^* - V_1}{V_1^*} \right)^4 + \left(\frac{50}{V_1} \right)^2 \times \left(\frac{V_5^2}{5} + \frac{V_7^2}{7} + \frac{V_{11}^2}{11} + \frac{V_{13}^2}{13} + \frac{V_{17}^2}{17} + \frac{V_{19}^2}{19} \right) \quad (3.8)$$

Where,

V_{1d} = Desired fundamental voltage

V_1 = Actual fundamental voltage

V_5 = Harmonic voltage of 5th Harmonic

V_7 = Harmonic voltage of 7th harmonic

V_{11} = Harmonic voltage of 11th harmonic

V_{13} = Harmonic voltage of 13th harmonic

V_{17} = Harmonic voltage of 17th harmonic

V_{19} = Harmonic voltage of 19th harmonic

The objective of this research is to minimize the above objective function to reduce the THD. The transcendental equations (3.5), satisfying the constraint function (3.6) with objective function (3.8), can be solved by using the N-R method for minimum THD and optimal switching angles of the proposed multilevel inverter. The comparison between different switching control methods with the proposed SHEPWM control is given in the table.3.3 [150].

Table 3.3 Comparison between switching control methods with SHEPWM

Method of switching	**SVPM**	**SVPWM**	**SHEPWM**
Utilization of dc sources	0~0.866	0~1	0~1.12
Frequency of switching	Medium	High	Low
Complexity	Low	High	High
Implementation	Online	Online	Offline

3.5 COMPUTATION OF SWITCHING ANGLES USING NEWTON RAPHSON METHOD

The seven switching angles for seven switches in the inverter are first computed by numerical successive approximation technique known as Newton Raphson (N-R) approach [151]. The computation of switching angles involves equations (3.5) with equation (3.6). The N-R approach for solving non-linear equations is given in detail below.

Step 1: For the calculation of switching angles, a matrix is formulated with seven (1-7) switching angles in equation (3.9)

$$\alpha^i = [\alpha^1, \alpha^2, \alpha^3, \alpha^4, \alpha^5, \alpha^6, \alpha^7]^T \tag{3.9}$$

Step 2: The non-linear system matrix is formulated in equation (3.10), and the transpose matrix of its partial derivation concerning switching angles is given in equation (3.11)

$$F^i = \begin{bmatrix} \cos(\alpha_1^i) + \cos(\alpha_2^i) + \cos(\alpha_3^i) + \cos(\alpha_4^i) + \cos(\alpha_5^i) + \cos(\alpha_6^i) + \cos(\alpha_7^i) \\ \cos(5\alpha_1^i) + \cos(5\alpha_2^i) + \cos(5\alpha_3^i) + \cos(5\alpha_4^i) + \cos(5\alpha_5^i) + \cos(5\alpha_6^i) + \cos(5\alpha_7^i) \\ \cos(7\alpha_1^i) + \cos(7\alpha_2^i) + \cos(7\alpha_3^i) + \cos(7\alpha_4^i) + \cos(7\alpha_5^i) + \cos(7\alpha_6^i) + \cos(7\alpha_7^i) \\ \cos(11\alpha_1^i) + \cos(11\alpha_2^i) + \cos(11\alpha_3^i) + \cos(11\alpha_4^i) + \cos(11\alpha_5^i) + \cos(11\alpha_6^i) + \cos(11\alpha_7^i) \\ \cos(13\alpha_1^i) + \cos(13\alpha_2^i) + \cos(13\alpha_3^i) + \cos(13\alpha_4^i) + \cos(13\alpha_5^i) + \cos(13\alpha_6^i) + \cos(13\alpha_7^i) \\ \cos(17\alpha_1^i) + \cos(17\alpha_2^i) + \cos(17\alpha_3^i) + \cos(17\alpha_4^i) + \cos(17\alpha_5^i) + \cos(17\alpha_6^i) + \cos(17\alpha_7^i) \\ \cos(19\alpha_1^i) + \cos(19\alpha_2^i) + \cos(19\alpha_3^i) + \cos(19\alpha_4^i) + \cos(19\alpha_5^i) + \cos(19\alpha_6^i) + \cos(19\alpha_7^i) \end{bmatrix} \tag{3.10}$$

$$\left[\frac{\partial F^i}{\partial \alpha}\right]^T = \begin{bmatrix} -sin(\alpha_1^i) - sin(5\alpha_1^i) - sin(7\alpha_1^i) - sin(11\alpha_1^i) - sin(13\alpha_1^i) - sin(17\alpha_1^i) - sin(19\alpha_1^i) \\ -sin(\alpha_2^i) - sin(5\alpha_2^i) - sin(7\alpha_2^i) - sin(11\alpha_2^i) - sin(13\alpha_2^i) - sin(17\alpha_2^i) - sin(19\alpha_2^i) \\ -sin(\alpha_3^i) - sin(5\alpha_3^i) - sin(7\alpha_3^i) - sin(11\alpha_3^i) - sin(13\alpha_3^i) - sin(17\alpha_3^i) - sin(19\alpha_3^i) \\ -sin(\alpha_4^i) - sin(5\alpha_4^i) - sin(7\alpha_4^i) - sin(11\alpha_4^i) - sin(13\alpha_4^i) - sin(17\alpha_4^i) - sin(19\alpha_4^i) \\ -sin(\alpha_5^i) - sin(5\alpha_5^i) - sin(7\alpha_5^i) - sin(11\alpha_5^i) - sin(13\alpha_5^i) - sin(17\alpha_5^i) - sin(19\alpha_5^i) \\ -sin(\alpha_6^i) - sin(5\alpha_6^i) - sin(7\alpha_6^i) - sin(11\alpha_6^i) - sin(13\alpha_6^i) - sin(17\alpha_6^i) - sin(19\alpha_6^i) \\ -sin(\alpha_7^i) - sin(5\alpha_7^i) - sin(7\alpha_7^i) - sin(11\alpha_7^i) - sin(13\alpha_7^i) - sin(17\alpha_7^i) - sin(19\alpha_7^i) \end{bmatrix} \tag{3.11}$$

Step 3: Formulation of harmonic magnitude matrix and represented in equation (3.12)

$$T = \left[\frac{\pi M_i}{4}, 0, 0, 0, 0, 0, 0\right]^T \tag{3.12}$$

Equations (3.5) and (3.12) are modified and rewritten as equation (3.13)

$$F(\alpha) = T \tag{3.13}$$

The matrices (3.9) to (3.13) are simulated in MATLAB software for the programmed N-R method, implemented in the following steps.

Step 1: Predict the initial switching angles using equal area criterion with the equation (3.14)

$$\alpha^0 = [\alpha_1^0, \alpha_2^0, \alpha_3^0, \alpha_4^0, \alpha_5^0, \alpha_6^0, \alpha_7^0] \tag{3.14}$$

Step 2: This step involves the design equations of the N-R approach from equations (3.15) to (3.18)

$$F(\alpha^0) = F^0 \tag{3.15}$$

The equation (3.13) is linearized to get the α^0

$$F^0 + \left[\frac{\partial F}{\partial \alpha}\right]^0 d\alpha^0 = T \tag{3.16}$$

And,

$$d\alpha^0 = [d\alpha_1^0, d\alpha_2^0, d\alpha_3^0, d\alpha_4^0, d\alpha_5^0, d\alpha_6^0, d\alpha_7^0] \tag{3.17}$$

Equation (3.17) can be solved using the inverse of the equation represented in equation (3.18).

$$d\alpha^0 = INV\left[\frac{\partial F}{\partial \alpha}\right]^0 (T - F^0) \tag{3.18}$$

Step 3: Update the initial values using the equation (3.19)

$$\alpha^{i+1} = \alpha^i + d\alpha^i \tag{3.19}$$

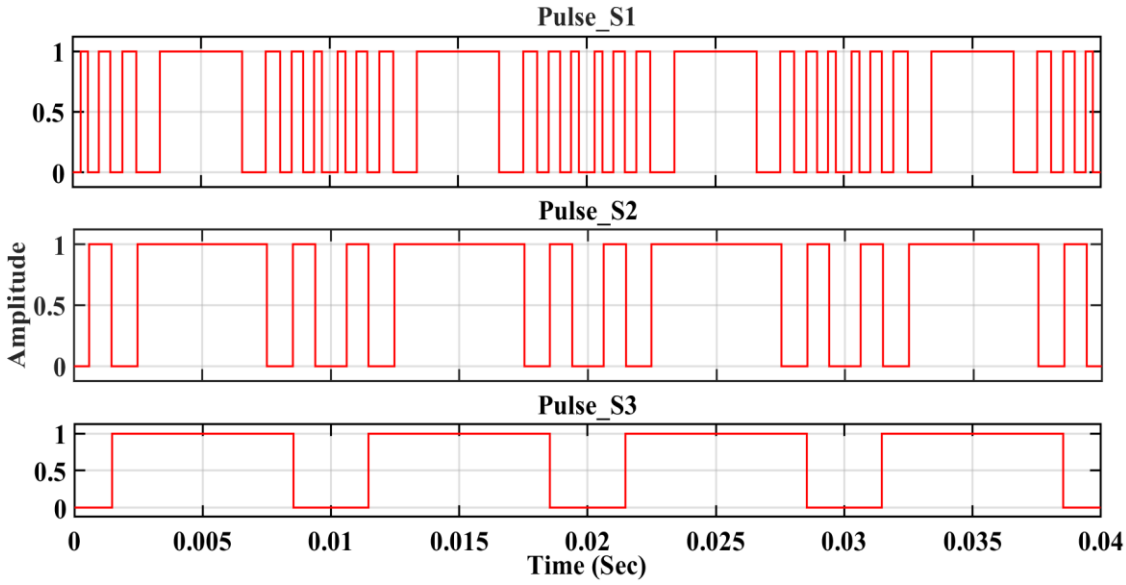
Step 2 & 3 are repeated till the $d\alpha^i$ is satisfied for the degree of accuracy and to satisfy the constraint $\alpha_1 < \alpha_2 < \alpha_3 < \alpha_4 < \alpha_5 < \alpha_6 < \alpha_7 < \frac{\pi}{2}$. Thus the switching angles α_1 to α_7 be evaluated using the Newton Raphson approach, and the same is stored in the look-up tables for different modulation indexes. During the real-time operation of the inverter, these switching angles are accessed from memory look-up tables.

3.6 RESULTS & DISCUSSIONS

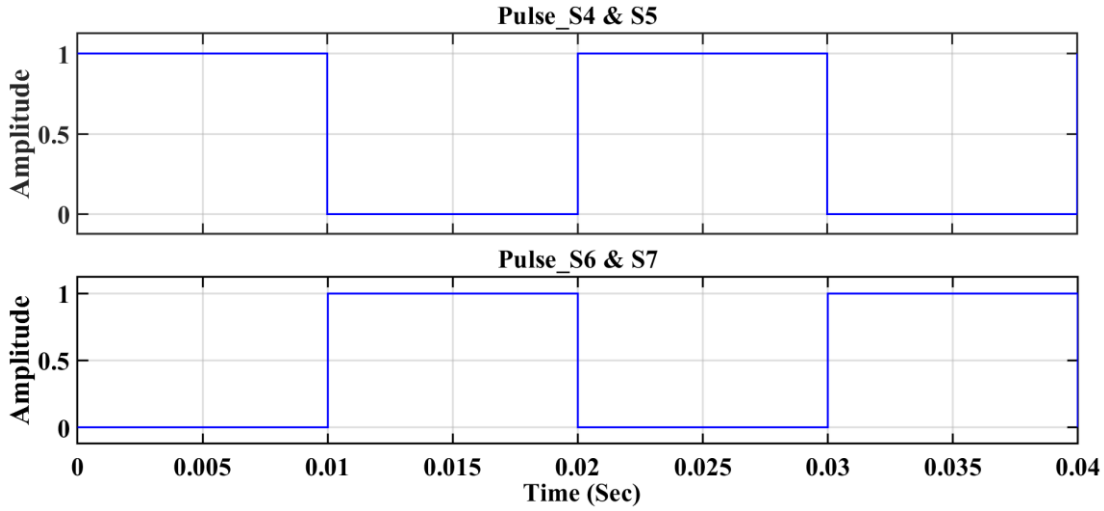
The proposed asymmetric inverter is implemented on MATLAB Simulink using seven IGBT switches, three switched diodes and three dc sources. To generate the switching pulses, a selective harmonic elimination pulse width modulation has been used. The switching frequency of is 5kHz, the maximum harmonic frequency is 1 kHz, and the Nyquist frequency for THD is 5 kHz. The inverter's load is modeled as a non-resistive load with R = 26.83 Ω and L = 9.9 mH. The proposed inverter operated at three different levels using dc sources described below.

Case (i): Equal magnitude of dc sources

The suggested inverter depicted in figure 3.4 produces a seven-level output voltage when the input dc sources are all equal in magnitude as 1:1:1 ratio. Here the magnitude of dc sources are taken as V_1 = 37V, V_2 = 37V and V_3 = 37V to get a peak voltage of 111V. The switching pulses of the seven-level operation of the suggested inverter are illustrated in figure 3.10. Figure 3.11 presents the 7-level voltage waveform of the suggested inverter with the equal magnitude of dc sources, and figure 3.12 shows the corresponding THD of the 7-level output as 15.36%.



(a)



(b)

Figure 3.10 Switching pulses of proposed inverter for seven-level operation

(a) Primary circuit (b) Auxiliary circuit

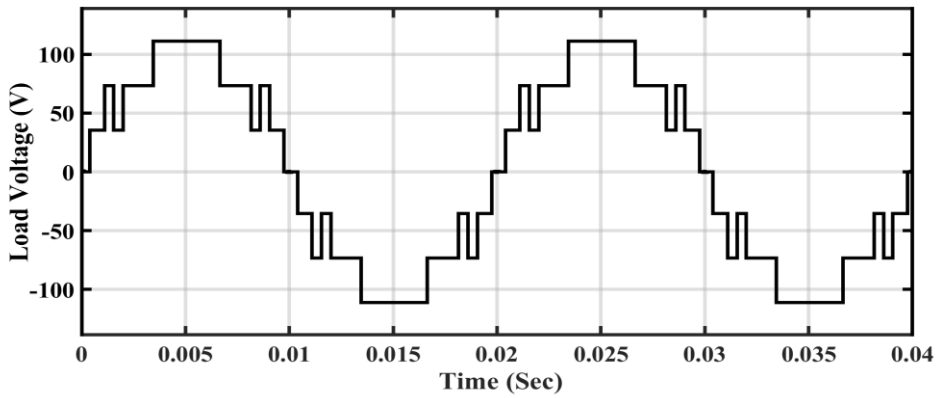


Figure 3.11 Seven level output voltage of the proposed inverter

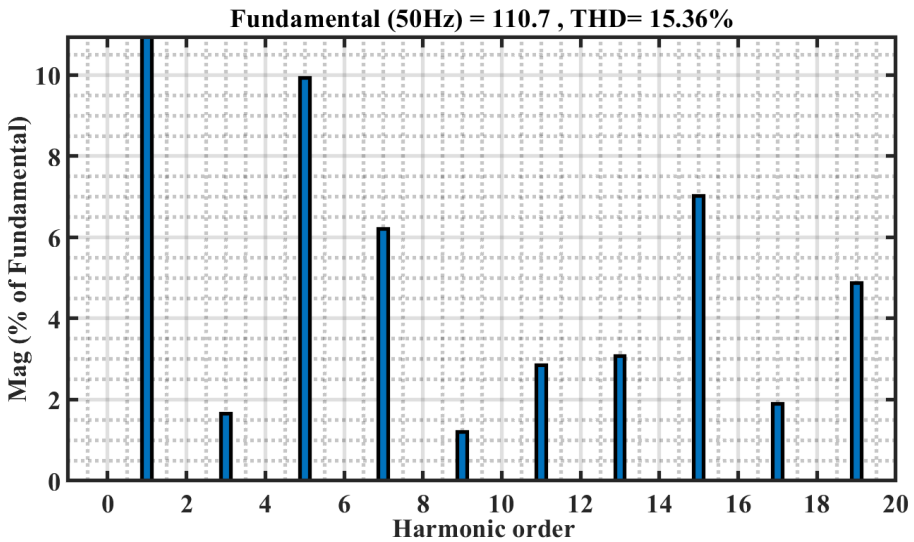
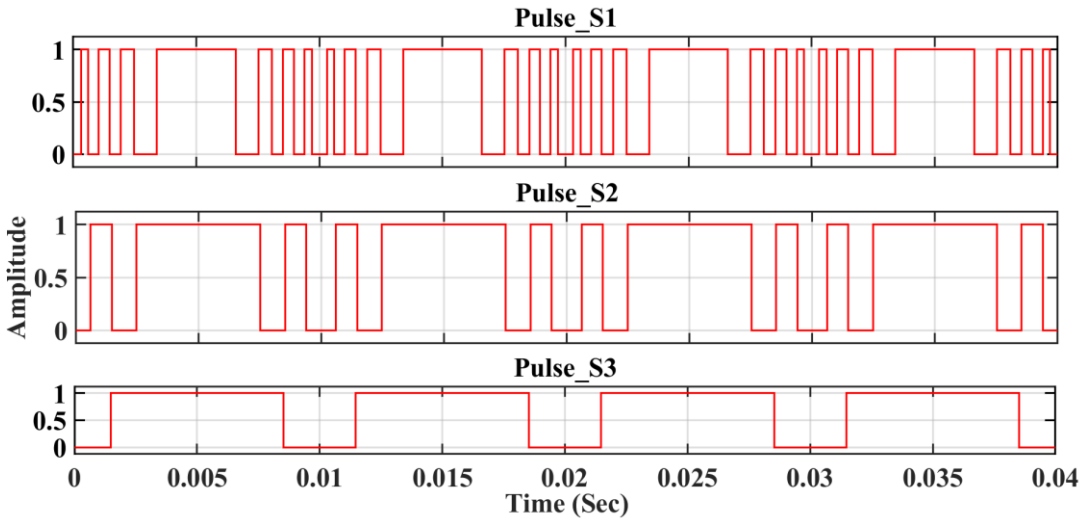


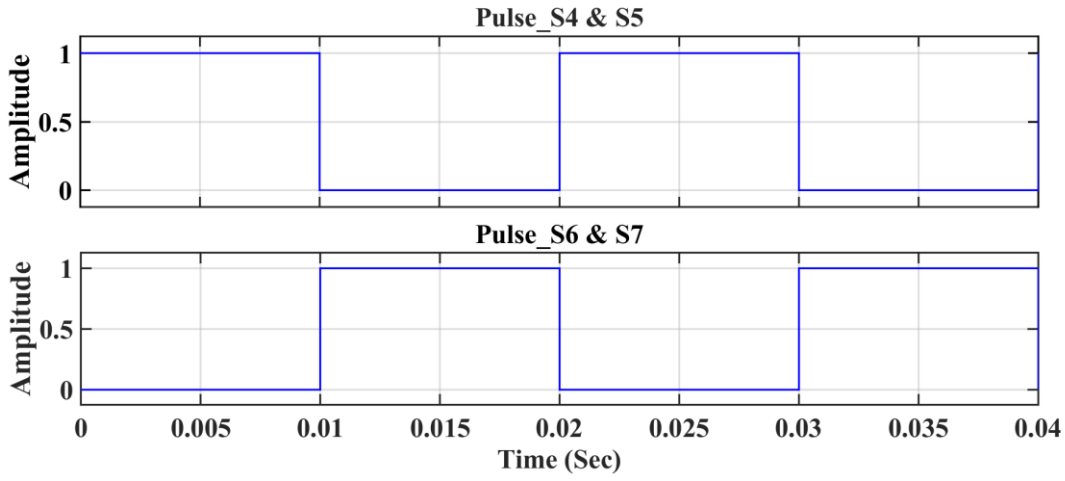
Figure 3.12 THD of proposed inverter for seven-level operation

Case (ii): Unequal magnitude of dc sources

The suggested inverter depicted in figure 3.4 produces an eleven-level output voltage when the input dc sources are in the ratio of 1:2:2. Here the magnitude of dc sources are taken as V_1 = 37V, V_2 = 74V and V_3 = 74V to get a peak voltage of 185V. The switching pulses of eleven level operation of the suggested inverter are illustrated in figure 3.13. Figure 3.14 presents the 11-level output voltage waveform of the proposed inverter with an unequal magnitude of dc sources. Figure 3.15 shows the corresponding THD of the 11-level output as 11.17%.



(a)



(b)

Figure 3.13 Switching pulses of proposed inverter for eleven level operation (a) Primary circuits (b) Auxiliary circuit

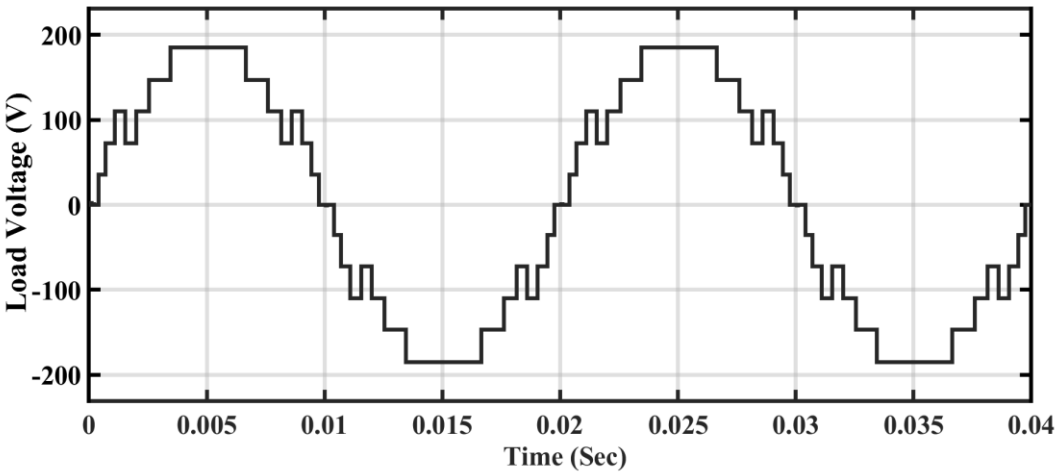


Figure 3.14 Eleven level output voltage of the proposed inverter

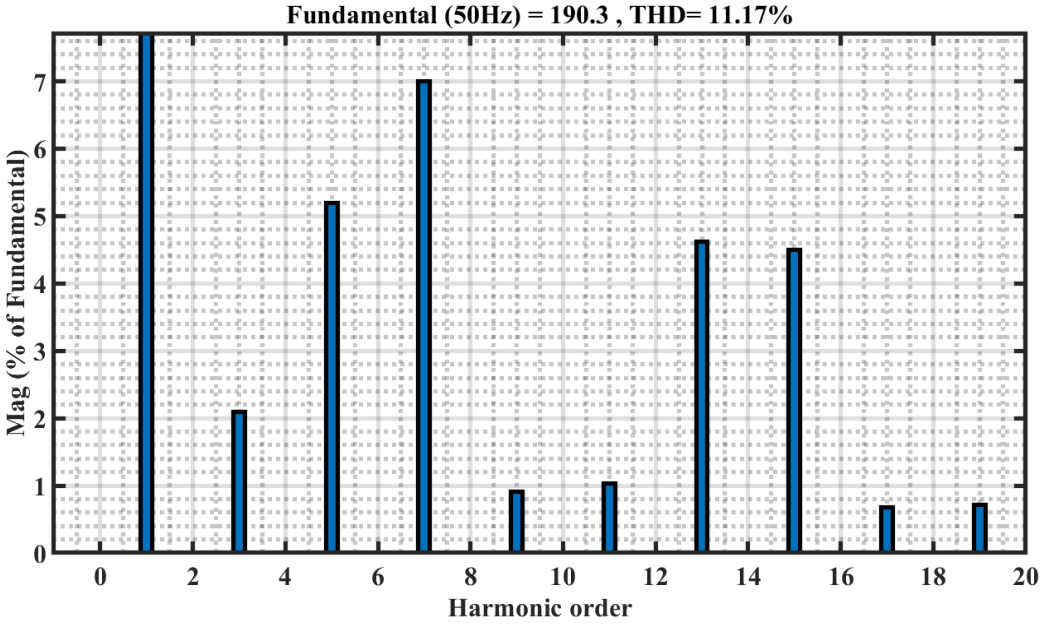
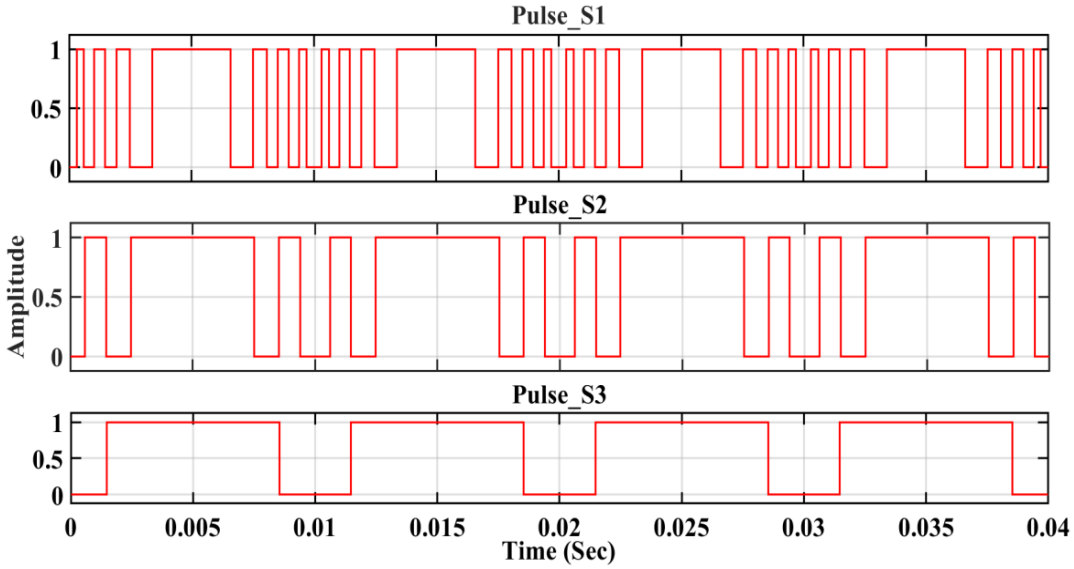


Figure 3.15 THD of proposed inverter for eleven level operation

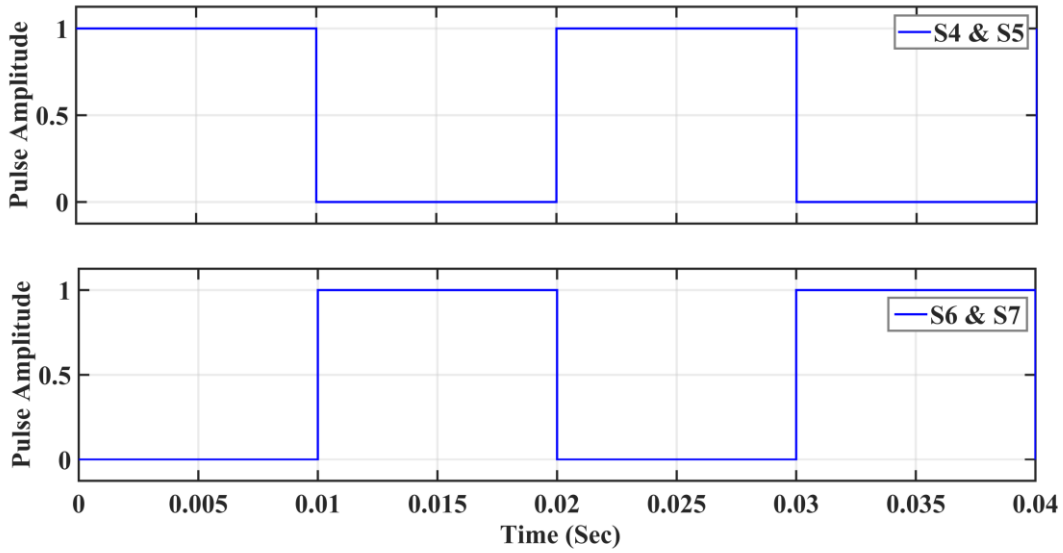
Case (iii): Binary approach of DC sources

The output voltage of the proposed inverter depicted in figure 3.4 is a fifteen-level voltage since the input dc sources are diverse in magnitude with the ratio of 1:2:4. Here the magnitude of dc sources are taken as V_1 = 37V, V_2 = 74V, and V_3 = 148V to get a peak voltage of 259V. The switching pulses corresponding to the generated switching angles are shown in figure 3.16 (a) for the primary circuit and figure 3.16 (b) for an auxiliary circuit. Figure 3.17 illustrates the 15-level voltage waveform of the suggested inverter with the binary approach of dc sources (1:2:4 ratio). Figure 3.18

shows the load current waveform for 15-level operation 3.19 shows the corresponding THD of the 15-level output as 7.3%. Figure 3.18 confirms that the output current waveform approximately resembles the sinusoidal waveform without using any filter at the output of the inverter. Also, it is in phase with the load voltage so that the power factor is maintained approximately unity.



(a)



(b)

Figure 3.16 Switching pulses of proposed inverter for 15-level operation

(a) Primary circuits (b) Auxiliary circuit

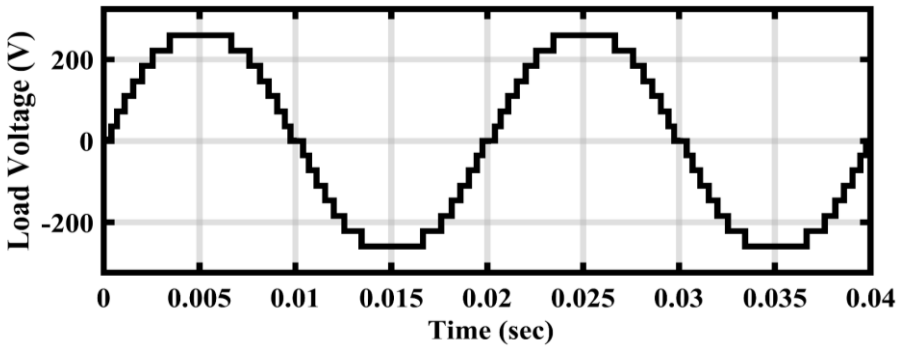


Figure 3.17 Output voltage waveform of the 15-level asymmetric inverter

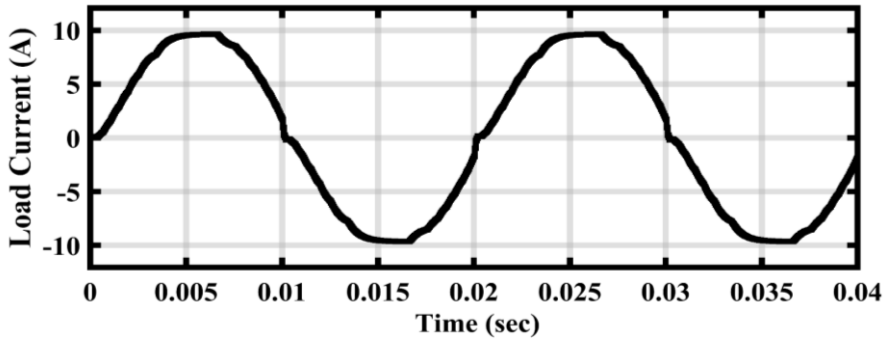


Figure 3.18 Output current waveform of the 15-level asymmetric inverter

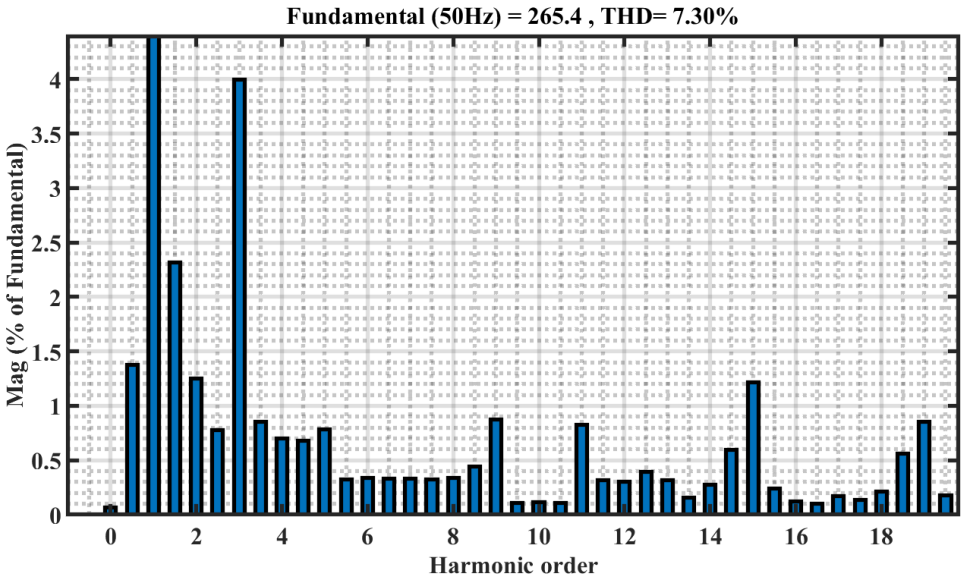


Figure 3.19 THD of the output voltage of proposed inverter for 15-level operation

The peak value of output voltage is 259V, and the peak value of current is 9.65A for the figures shown in 3.17 and 3.18, respectively. The peak output voltage and current are divided by $\sqrt{2}$ to produce the RMS values. So the output voltage is 183.16V, and the output current is 6.83A.

Therefore the output power of the 15-level inverter is determined by taking the product of RMS values of output voltage and current.

$P_0 = V_{RMS} * I_{RMS}$

$= 183.16 * 6.83$

$= 1250$ W

Thus the output of the proposed 15-level inverter is computed as 1250W. The inverter's efficiency can be determined after estimating the power losses of the IGBT switches, which is discussed in chapter-4.

3.7 CHAPTER SUMMARY

An asymmetric 15-level inverter with 7-switches, 3-diodes had been developed in this chapter to optimize the size of the design topology. The lower order dominant harmonics in the inverter output had been minimized using a low-frequency switching modulation (SHEPWM). The transcendental equations generated in SHEPWM had been solved using the NR method to obtain the switching angles. The THD of the inverter output had been analyzed for 7-level, 11-level, and 15-level operations using equal magnitude, un-equal magnitude, and binary approaches of dc sources respectively. The fifteen-level operation had given a minimum of 7.3%, compared to other levels of operation, as shown in table 3.4.

Table 3.4 THD comparisons of proposed inverter with existing topologies NR Method

Author	**Inverter**	**No of Sources**	**No of Switches**	**No of Levels**	**Max. O/p Voltage**	**%THD**
Jagdish Kumar (2008)	Symmetric CHB	5	20	11	$5V_{dc}$	7.9%
Aman Parkash (2014)	Symmetric H-Bridge	3	12	7	$3V_{dc}$	11.68%
Faouzi ARMI (2016)	Symmetric CHB inverter	4	16	9	$4V_{dc}$	19.3%

	Symmetric CHB inverter	3	12	7	$3V_{dc}$	25.91%
	Asymmetric CHB inverter	3	12	9	$4V_{dc}$	10.2%
Wahidah Abd Halim (2017)	Symmetric CHB inverter	3	12	7	$3V_{dc}$	11.9%
	Asymmetric CHB inverter	4	16	9	$4V_{dc}$	8.4%
Proposed	Asymmetric modular Multilevel inverter	3	7	7	$3V_{dc}$	15.36%
		3	7	11	$5V_{dc}$	11.17%
		3	7	15	$7V_{dc}$	7.30%

CHAPTER-4

POWER LOSS ANALYSIS USING PLECS THERMAL MODEL & SIMULINK PRECISE MODELS

4.1 INTRODUCTION

Power losses are the most critical metrics in power converters and significantly impact economic and technological assessments due to their sufficient approximation. The contribution presented in this chapter aims to prove that the power losses (switching & conduction losses) are low at fundamental frequency switching modulation in contrast with high switching frequency modulation. Two switching modulation techniques, such as phase disposition (PD-multi carrier-based pulse width modulation at high switching frequency) and selective harmonic elimination pulse width modulation (SHEPWM-fundamental switching frequency), are considered for the power loss analysis in a 15-level reduced switch asymmetric inverter. This work proposed a simplified model for calculating power losses in multilevel inverters using MATLAB Simulink. Further, the thermal model of the proposed inverter is implemented on PLECS for analyzing the power losses. The comparative analysis of switching and conduction losses of the proposed inverter with the PLECS thermal model and MATLAB precise models is an integral part of this work.

4.2 SWITCHING CONTROL METHODOLOGY

Various control approaches have been used to regulate multilevel inverter output voltage waveform. These control approaches are classified by switching frequency, such as low-frequency and high-frequency switching. High-frequency switching modulations like sine pulse width modulation (SPWM), multi-carrier modulation schemes like phase disposition pulse width modulation (PDPWM), phase opposition & disposition pulse width modulation (PODPWM), alternate phase opposition & disposition pulse width modulation (APODPWM), and others, [156] in which the active switch can trigger several times in a cycle. SVPWM [157] and SHEPWM [158] are low frequency switching modulation methods where the active power switch is operated only once or twice in each cycle.

In this study, both high & low frequency switching methods are implemented on the proposed 15-level inverter. For better results, the phase disposition PWM (PDPWM) from high-frequency switching and selective harmonic elimination (SHEPWM) methods was offered to control the inverter. Due to its low switching frequency, SHEPWM has fewer switching losses and EMI. The dominant low order harmonics were also reduced, reducing the desired filter size at the inverter output. The power losses are calculated for comparative analysis in both the switching methods and corresponding efficiencies were determined.

4.2.1 Phase disposition pulse width modulation (PDPWM)

Phase disposition pulse width modulation is a high-frequency switching modulation. Figure 4.1 shows the PDPWM switching pulse generating technique with all carrier signals are in phase and level-shifted. A unipolar PDPWM switching method is implemented for the suggested fifteen level inverter. This modulation technique utilizes a single-phase reference or modulating signal is 'V', and fourteen carrier signals are C1 to C14. All the carrier signals are selected to have a higher frequency than the reference signal and are arranged in phase to each other. The control signal to be provided to the corresponding phase leg switches is produced by comparing these fourteen carrier signals with the corresponding modulating signal.

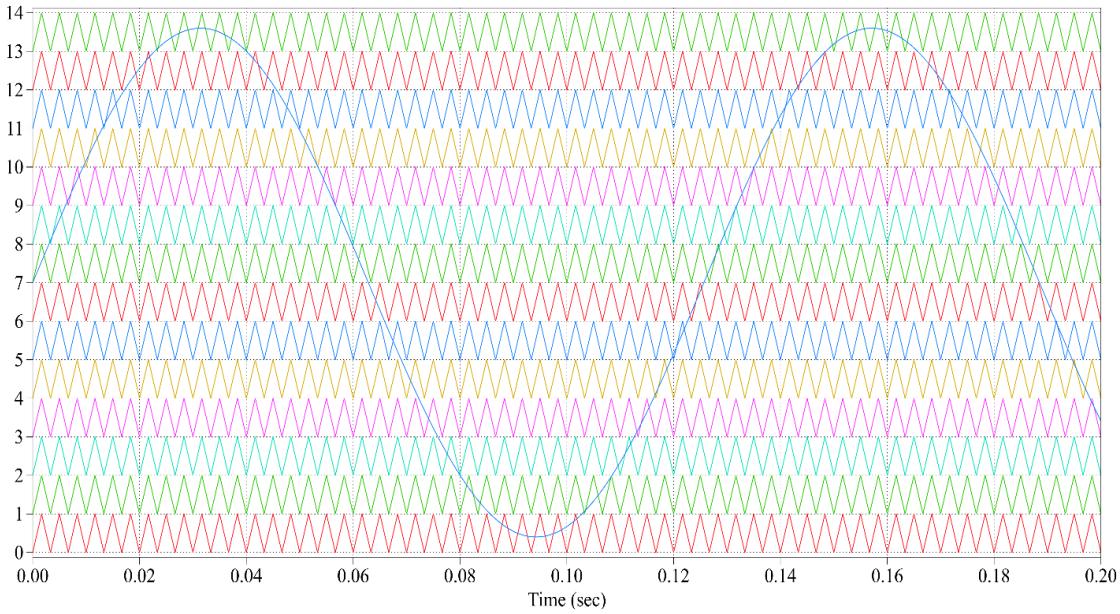


Figure 4.1 Phase disposition pulse width modulation

4.2.2 Selective harmonic elimination pulse width modulation (SHEPWM)

To get the desired multilevel output voltage, SHE uses predefined switching angles and eliminates dominant lower order harmonics that reduce the total harmonic distortion (THD). The triggering angles of the suggested 15-level inverter must be predetermined off-line, and hence it is known as the open-loop method. Figure 4.2 presents the approximated 15-level quarter-wave voltage waveform of the proposed inverter. Seven triggering angles α_1 to α_7 need to be predetermined in this scenario for the quarter-wave generation of 15-level output.

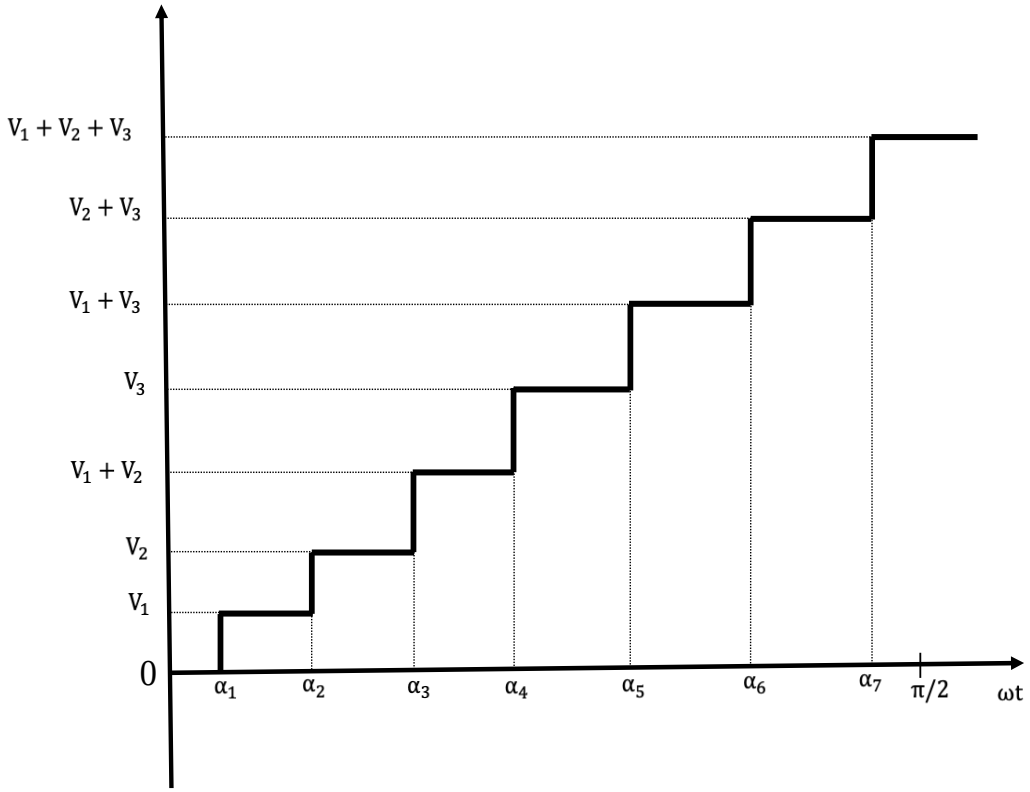


Figure 4.2 Quarter wave approximation of 15-level output of multilevel inverter

The Fourier expansion of the stepped voltage waveform yields periodic sine and cosine signals and a constant. The signal is made up of both odd and even harmonics. The quarter-wave symmetry cancels the even harmonics and dc components. Therefore, the output voltage waveform of the multilevel inverter consists of odd harmonics only. Also, the triplen harmonics becomes zero for balanced three-phase systems. Hence the Fourier representation of the proposed 15-level inverter output is approximated for SHEPWM control, considering the odd-order harmonics by neglecting even order and triplen harmonics.

4.3 POWER LOSS MODELS FOR THE PROPOSED INVERTER

While using power semiconductor devices in the design of power converters, there are primarily 4-types of power losses that will occur in the devices during the operation. These types include (1) Switching losses (2) Conduction losses (3) Gate driver losses. (4) OFF state losses. Gate driver and OFF state losses are negligible and ignored. The inverter's switching and conduction losses are therefore estimated.

4.3.1 Power losses in IGBT

The power losses in ideal switches are negligible, while the practical switch's static (conducting) and dynamic (switching) losses have been recorded over the switching cycle shown in figure 4.3. During the ON and OFF operation of the switch, there would be a switching time of several microseconds, and the device absorbs some power when the voltage and currents are non-zero. There is an inevitable on-state voltage drop on the device (several volts for IGBT) while the switch is in conduction, which results in conduction losses.

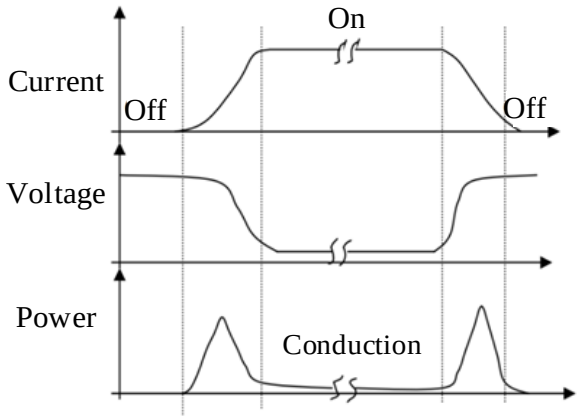


Figure 4.3 Switching cycle representation of IGBT over a cycle

Power loss in the IGBT limits its use. It thus becomes a significant problem that cannot be ignored while designing a power converter because it influences the inverter's efficiency. Power losses act as a heat source inside the semiconductor switch, and this heat will raise the junction temperature and increase the temperature inside the device. This is considered a self-heating effect which is more significant when the device is tightly packed.

To prevent destruction and severe damage to the system, the T_j junction temperature must be retained to the healthy T_{jmax} operating value typically defined by the manufacturer. A better configuration is provided if the temperature gradient can be correctly predicted within the device under actual operating conditions. Thermal analysis is critical in designing power converters for optimal stability, performance, and system design optimization.

4.3.2 Datasheet specifications and thermal characteristics of IGBT

The IGBTs in the proposed 15-level inverter are chosen from Infineon manufacturer. The device model and specifications are given in table 4.1.

Table 4.1 Datasheet specifications of IGBT

IGBT Model	**IGA30N60H3**
Make	**Infineon**
Collector- emitter voltage VCEO max	**600V**
Continuous collector current at 25^0 C	**18A**
Continuous collector current **Ic Max**	**11A**
Pd - Power dissipation	**43W**
Device temperature	**25^0 to 175^0 C**
Gate-emitter leakage current	**100nA**
Maximum blocking voltage	**400V**
Device ON state current	**120A at 175^0 C**

The IGBT device should also be provided with pre-calculated conduction energy losses, turn-on losses, and turn-off losses at two different temperatures of 25^0 and 175^0 for base values of on-state voltage V_{on} and conduction i_{on} current as shown in figure 4.4, figure 4.5, and figure 4.6.

4.3.3 Thermal simulation: Accounting for switching and conduction losses

The thermal operation of electronic power switches is an important aspect, which becomes more critical for designing a simplified system with greater power density. PLECS is a simulation software where thermal analysis of semiconductor devices can be carried out will little effort. PLECS requires an early thermal system integration with the electrical design and provides an appropriate cooling method for each specific use. Furthermore, calculations of switching and conduction loss are quickly carried out. During loss simulations, the speed of simulation is not adversely affected as ideal switching is preserved.

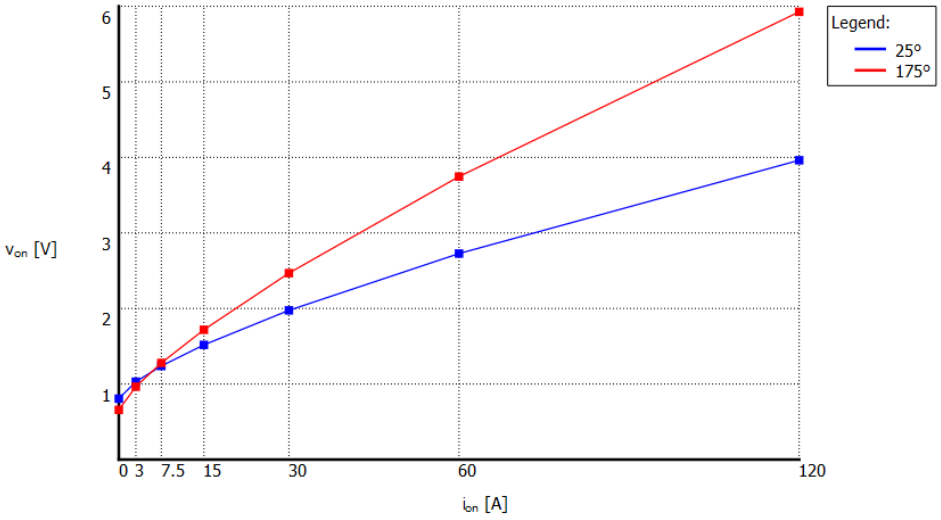


Figure 4.4 Conduction losses of IGBT

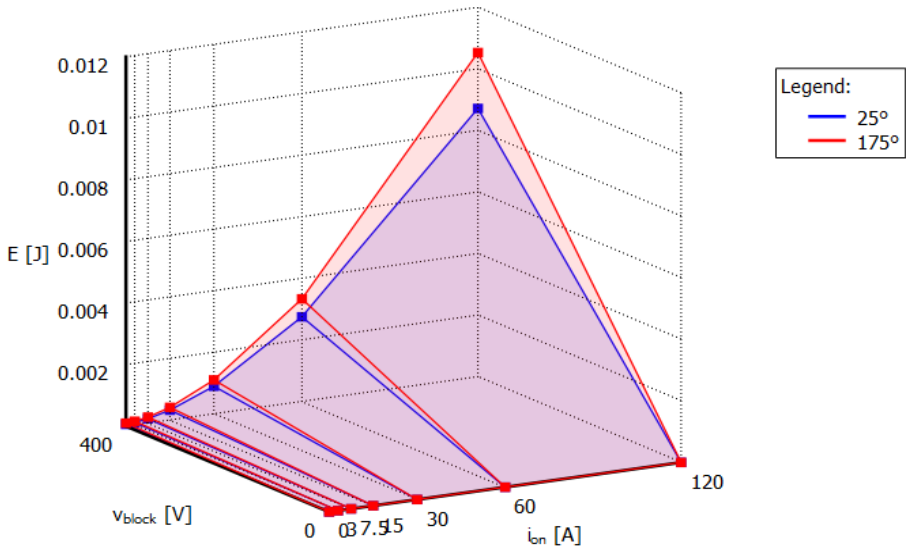


Figure 4.5 Turn_ON losses of IGBT

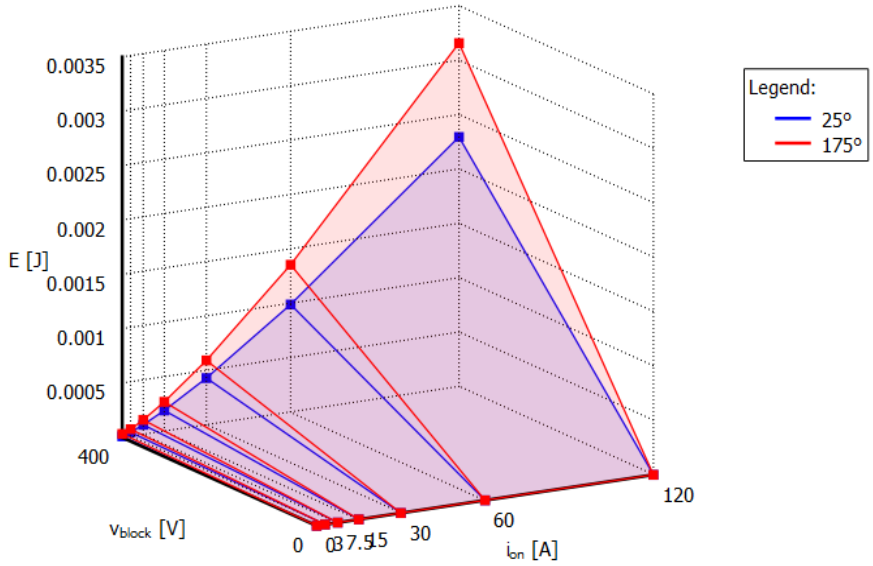


Figure 4.6 Turn_OFF losses of IGBT

PLECS records semiconductor material operating conditions (forward current, voltage blocking, and junction temperature) before and after any switching operation rather than evaluating semiconductor switching losses from current and voltage transients. The resulting dissipated energy is then read from a 3D look-up table using these parameters. The dissipated power is determined from the current and temperature of the device during the operation. This synthesis of optimal switching models and accurate loss data presents an inexpensive and precise alternative to detailed device simulation. PLECS integrated visual editor is used to access the appropriate datasets.

4.4 ELECTRO-THERMAL MODELING OF IGBT USING PLECS

PLECS is a software tool that has been developed by Plexim to perform the system-level simulation of electric circuits, remarkably intended for power electronics but can be used for all power systems. Apart from the electrical system, PLECS includes modelling controls and various physical domains such as thermal, magnetic, and mechanical systems.

For IGBT, PLECS uses only one of its dc characteristics, the high-valve output of a control signal linearly interpolated according to the user points. With the dynamic properties of this IGBT, it is essential, especially to accurately model the dependencies of the total energy from switching E_{ts} on several variables, such as T_j, the current collector I_C, R_G, or overvoltage switching. These relationships can be used in PLECS,

and they are often interpolated linearly, as with the dc characteristics. The system also relies on the value entered by the user for switching energy losses. The energy values of the ON and OFF losses are entered independently, both for the IGBT and the reverse diode.

The thermal model of IGBT is shown in figure 4.7, which is modelled for one of the IGBT switches of an auxiliary circuit of the suggested 15-level inverter. The impedance of the thermal model is designed from the foster circuit model for junction temperature to case temperature.

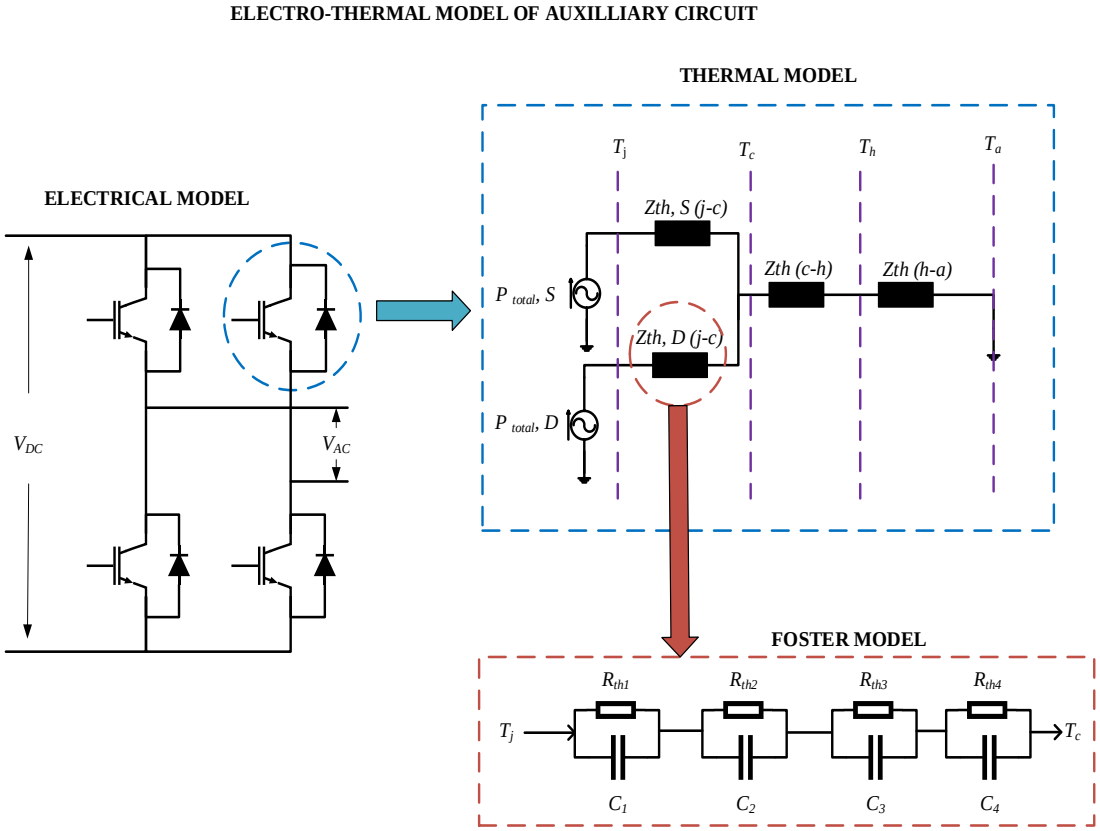


Figure 4.7 Foster electro-thermal model of IGBT

Considering junction temperature as 150^0 C and thermal impedance of 1.25Ω, the foster thermal model is designed on PLECS for the 15-level inverter. The 7- IGBT switches are modelled thermally using a heat sink in PLECS simulation for power loss analysis. The conduction losses and switching losses are measured using this analysis for both PDPWM (high-frequency switching) and SHEPWM switching (low-frequency switching).

4.4.1 Concept of the heat sink

The heatsink absorbs the switching and conduction losses of all devices in its boundary. A heat sink simultaneously describes an isothermal atmosphere and distributes its temperature to the surrounding components. The semiconductors mounted on the heat sink will have the same case temperature. The switching energy losses are modelled as direct type pulses on PLECS, having zero width and infinite height. Thus, either the thermal capacitance of the heat sink needs to be specified, or a thermal chain with a capacitance should be used to avoid the infinite thermal resistance to switching energy losses. The electric equivalent model of the thermal circuit for power loss analysis is shown in figure 4.8.

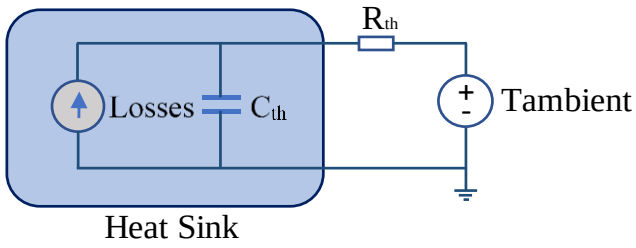


Figure 4.8 Electrical equivalent of thermal circuit

4.4.2 Calculation of total cycle-average losses

The total power dissipation of each semiconductor is also a factor of interest. The average losses for a device can be determined by adding the losses in the next switching period to the average power cycle. The average cycle method of loss calculation is shown in figure 4.9, which gives the summation of the switching and conduction losses of the device. The C-Script PLECS block is used to perform integrated loop summing on energy loss operations [159].

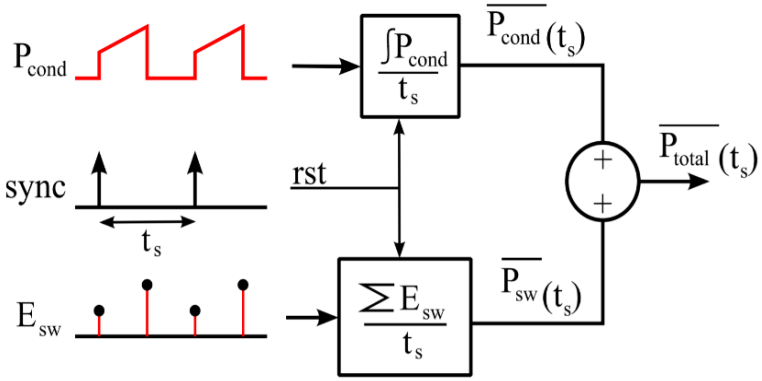


Figure 4.9 Calculation of total cycle average losses

4.5 SIMULINK PRECISE CURVE FITTING MODELS FOR POWER LOSS CALCULATION

Calculating power losses for multilevel inverters is more difficult than for two-level inverters. Multilevel inverters need different approaches for calculating losses than two-level inverters [160-161]. The fundamental cause is that each switch has a different current in multilevel inverters, resulting in variable loss behaviour. However, each device's switching frequency is not the same at higher levels, bringing more difficulty in calculating losses. A simplified model for estimating power losses of 15-level MLI is proposed in this study. A model is suggested that uses the approach employed in [162-164] with slight modifications. The maximum working temperature is set to be 150^0. The model is being evaluated online using the tool MATLAB Simulink. This study considered the combined load of R = 26.83Ω and L = 9.9mH. The effect is a transition from pure resistive to pure inductive load contrasted with the load's situation. The aim is to analyze the behaviour of inverter losses under various load conditions.

4.5.1 Conduction loss calculation model

In power semiconductor devices, the conduction losses occur during the ON state of the device with conduction current. In the proposed inverter, the conduction losses will increase proportionally with the number of levels. The precise conduction loss calculation model is presented in figure 4.10.

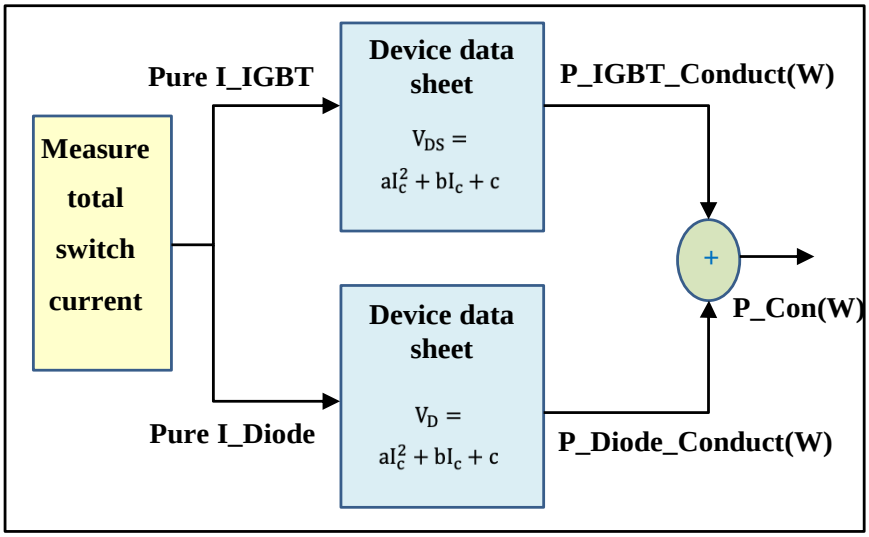


Figure 4.10 Conduction loss calculation process using curve fitting Simulink model

The conduction losses in any ON state device can be computed using saturated voltage and conduction current during the ON state [161]. It is therefore represented with the following expression.

$$P_{Conduction} = |I_C| V_{on}$$

The current value should always be positive; hence the absolute value is considered. On-state voltage is often approximated by adding a V_o voltage (threshold voltage) and a R_{on} resistor (current dependence) in series with the ideal device.

The method's significant flaws,

i. The circuit is partially rebuilt by adding components in series with the ideal devices.
ii. This model is unreliable since it does not utilize real device datasheet curves.

The proposed model will compute the conduction losses with a more straightforward and efficient method. The device's threshold voltage is represented with second-order expression in terms of conduction current. The quadratic equation is constructed from the datasheet's actual curves using curve fitting. Both the switch and the diode have quadratic equations in the control scheme. The Simulink model measures the pure switch and diode currents independently. The positive component of the on-state device current is pure switch current, while the negative is pure diode current. Conduction losses of the IGBT switch and the diodes are achieved by adding these two blocks, as shown in figure 4.10.

4.5.2 Switching loss calculation model

During the switching on and off of the power semiconductor, the power loss may be characterized as the power dissipation that occurs. Switching losses are caused by both the switch and the parallel diode being used. As a result, switching losses are directly proportional to the frequency of switching, and as a result, they contribute considerably to the total inverter loss, particularly when using sine pulse width modulation (SPWM). The power switch is responsible for both the turn-on loss (E_{on}) and the turn-off loss (E_{off}). Compared to this, only the turn-off (E_{rec}) loss is considered in the antiparallel diode since the turn-on loss is often overlooked due to the quick behaviour of the diode when the bias is applied in the forward direction. Compared to

conventional diodes, turn-on losses are less than 1% relative to turn-off losses. In reality, five important parameters influence switching loss behaviour: switching current, blocking voltage, junction temperature, gate resistance, and coil inductance. Power loss is a severe problem of multilevel inverters, leading to significant cost increases and lower performance in PV applications.

The results of this study revealed that losses might be evaluated online using the energy curves of switches provided in the device's datasheet. The energy factor (K) of a curve is calculated by dividing the current into two halves. After that, the energy factor curves are computed using second-order polynomials, and the curve fitting technique is used. The energy loss is calculated by multiplying the energy factor equation by the switching current, and the power loss is calculated by multiplying the energy loss by the switching frequency. A block diagram of an IGBT device is shown in Figure 4.11, along with the blocks that are utilized to quantify switching loss.

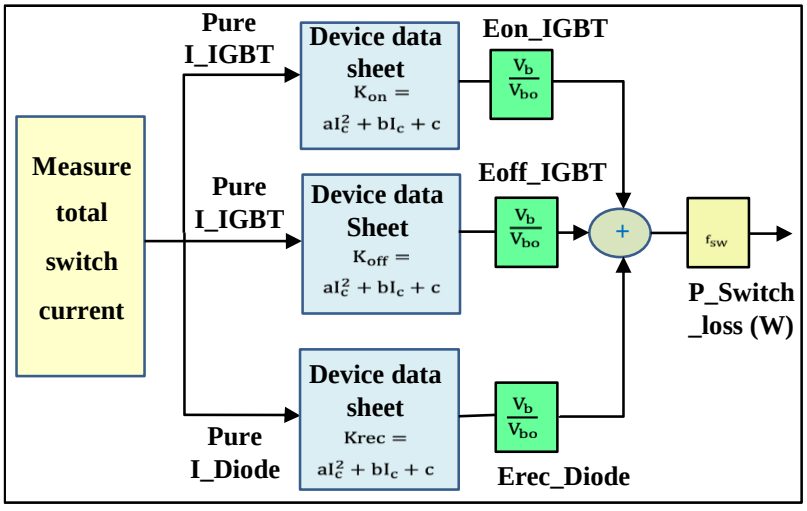


Figure 4.11 Switching loss calculation process using curve fitting Simulink model

In general, the switching losses are calculated during the ON and OFF times of the device operation.

Energy loss during IGBT on time is

$$E_{on\_SW\_loss} = V_{CE} * I_C * \frac{T_{on}}{2}$$

Energy loss during IGBT off time is

$$E_{off\_SW\_loss} = V_{CE} * I_C * \frac{T_{off}}{2}$$

The total energy loss during switching operation

$$E_{SW\_loss} = E_{on\_SW\_loss} + E_{off\_SW\_loss}$$

The power loss in the operation switch $= (E_{SW\_loss})/T$

Total switching losses $= (E_{SW\_loss}) * f_{SW}$

Where,

f_{SW} is switching frequency

E_{SW_loss} is total energy loss during switching operation.

4.5.3 Total power loss calculation model

The total power losses are calculated by combining the conduction loss and switching loss calculation models using the selective harmonic pulse width modulation (SHEPWM) for the proposed 15-level inverter, as shown in figure 4.12.

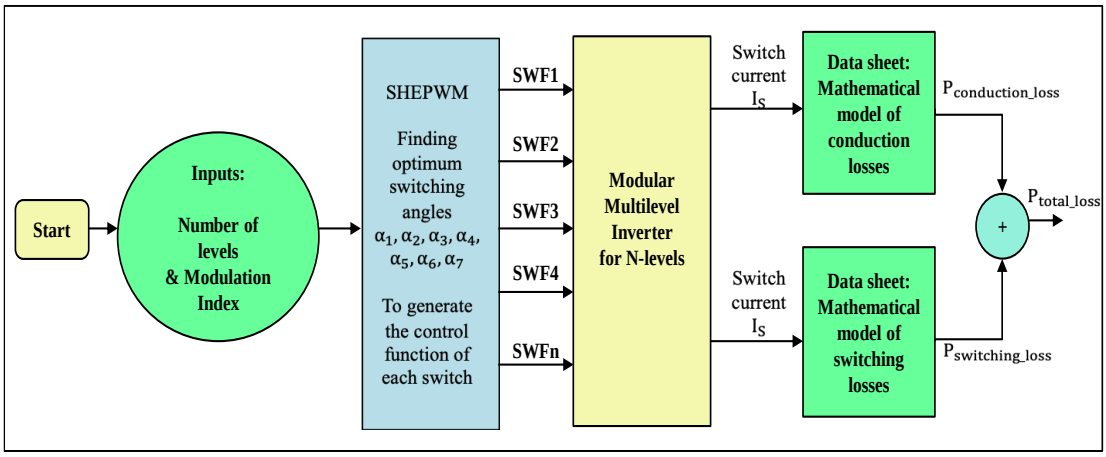


Figure 4.12 Total power loss calculations with SHEPWM switching using curve fitting Simulink model

IGBT curve fitting equations from the datasheet

$$v_{CE} = -2 * 10^{-7} I_c^2 + 0.0018 I_c + 0.9661$$

$$v_D = -1 * 10^{-7} I_D^2 + 0.0012 I_D + 0.7796$$

$$K_{IGBT-on} = 8 * 10^{-7} I_c^2 - 0.0023 I_c + 4.016$$

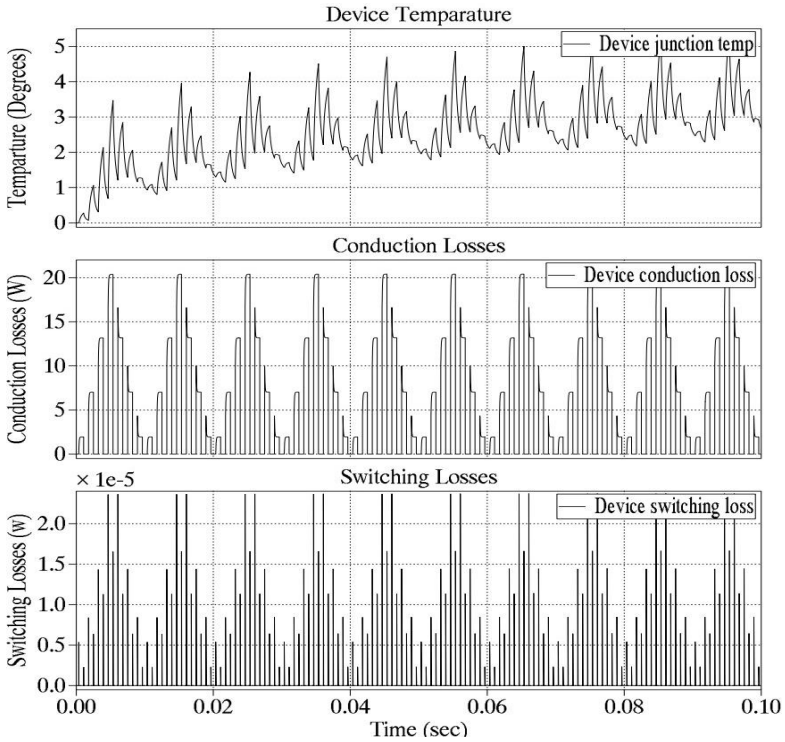
$$K_{IGBT-off} = 3 * 10^{-7} I_c^2 - 0.0011 I_c + 3.1584$$

$$K_{Diode-rec} = 7 * 10^{-7} I_D^2 - 0.0039 I_D + 6.6546$$

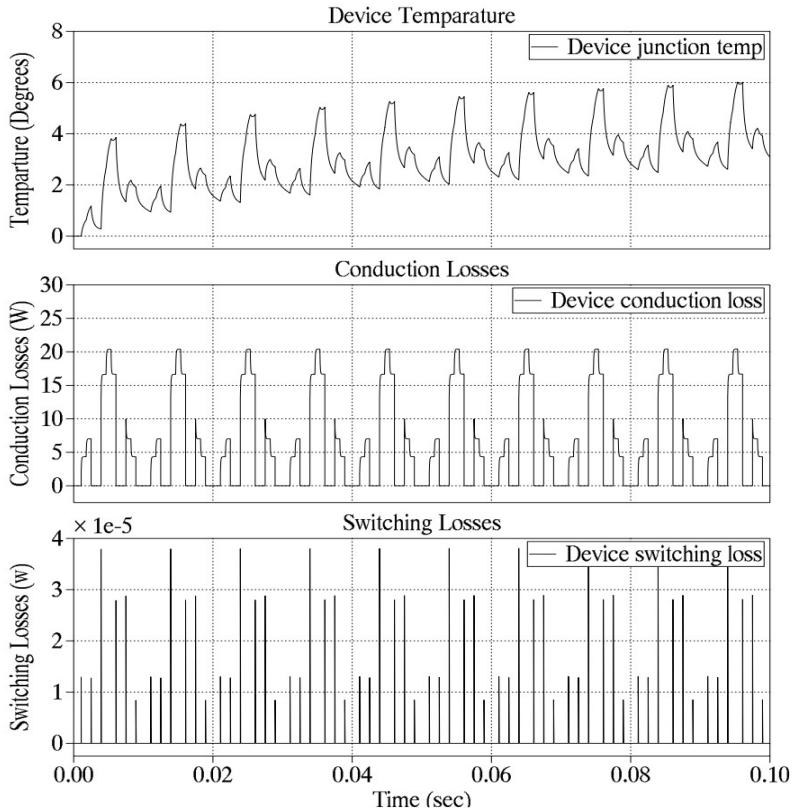
4.6 RESULTS & DISCUSSIONS

4.6.1 Power loss analysis using PLECS thermal models

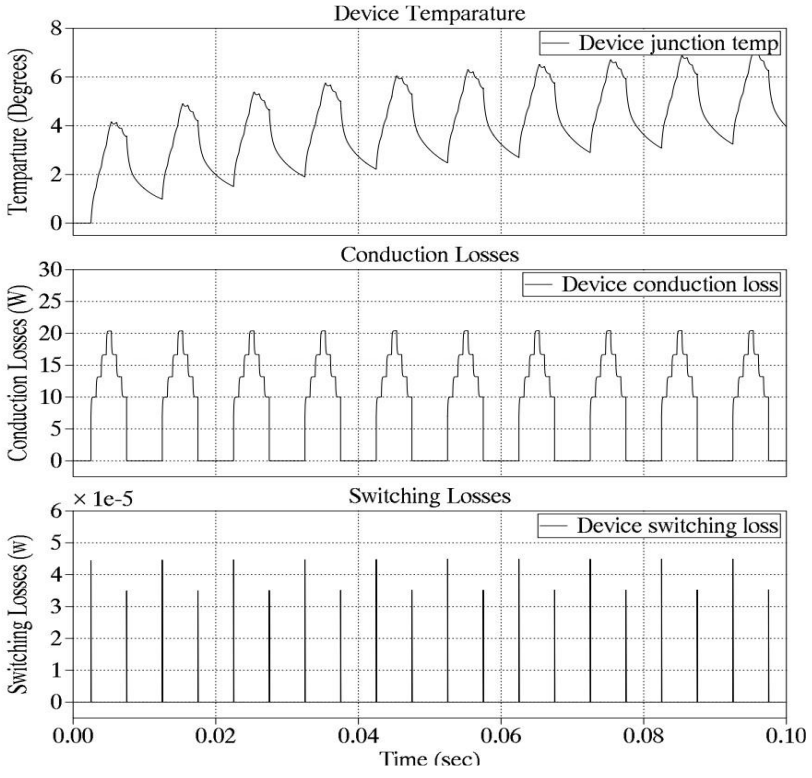
Power losses are analyzed in the proposed 15-level inverter presented in figure 3.4 for determining its efficiency. The 15-level inverter consists of seven IGBT switches, three in a primary circuit called high-frequency switches and the other four in auxiliary circuit known as low-frequency switches. These IGBT switches are modelled on a heat sink using PLECS to foster thermal equivalent circuits. The switching and conduction losses for PDPWM and SHEPWM were plotted using PLECS simulation. The device junction temperature, conduction losses, and switching losses are plotted in figure 4.13 for phase disposition pulse width modulation (PDPWM) switching control. The IGBT switches' S1', 'S2', and 'S3' are high-frequency switches in the operation of the proposed inverter; hence these switches undergo ON and OFF several times resulting in more switching losses. Similarly, the switches' S4', 'S5', 'S6' and 'S7' are the low-frequency switches, which undergoes only one time for ON and OFF per cycle resulting in fewer power losses.



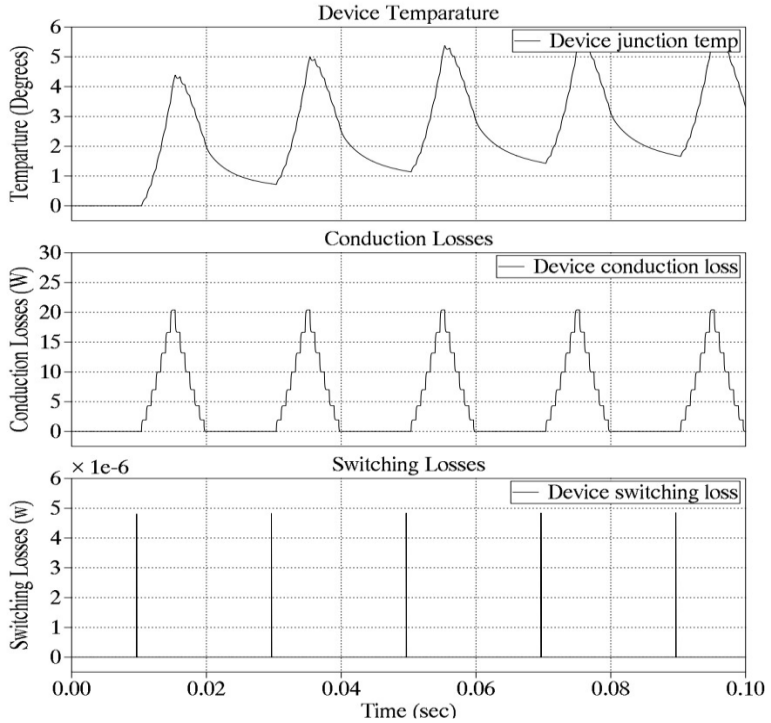
(a)


Device Temparature
Device junction temp
Temparture (Degrees)
Conduction Losses
Device conduction loss
Conduction Losses (W)
Switching Losses
× 1e-5
Device switching loss
Switching Losses (w)
Time (sec)

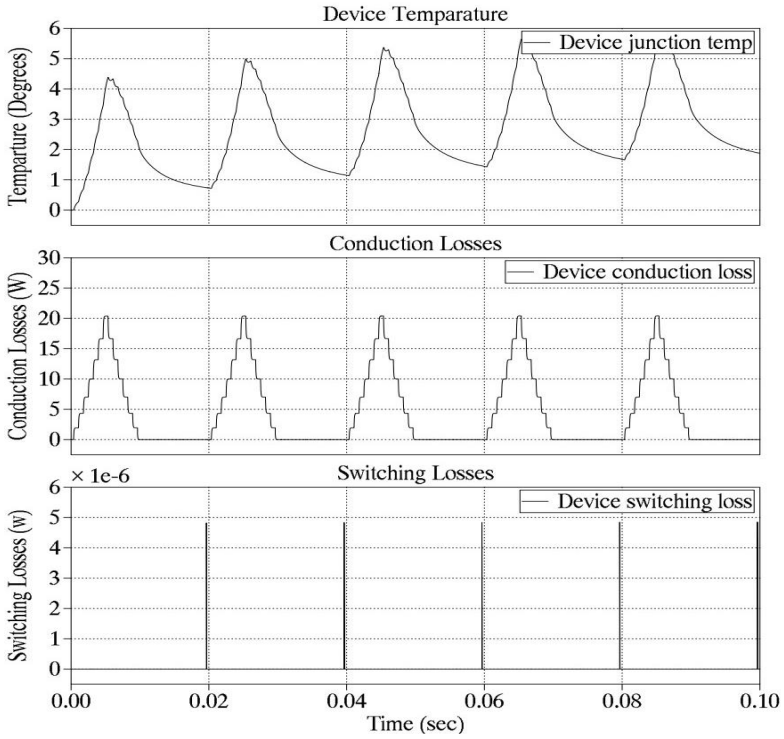
(b)


Device Temparature
Device junction temp
Temparture (Degrees)
Conduction Losses
Device conduction loss
Conduction Losses (W)
Switching Losses
× 1e-5
Device switching loss
Switching Losses (w)
Time (sec)

(c)

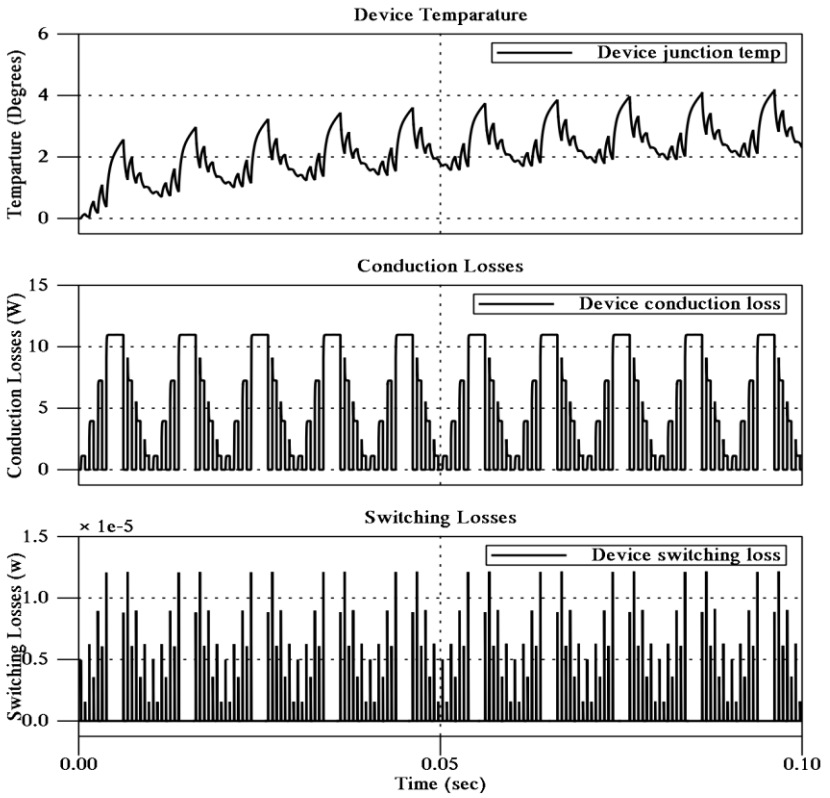


(d)

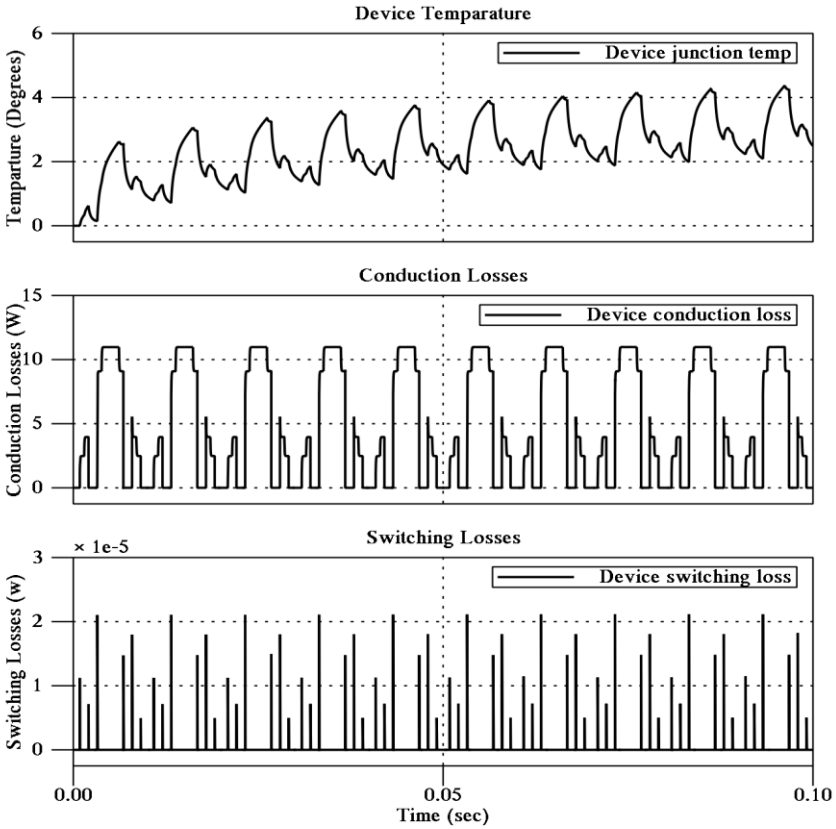


(e)

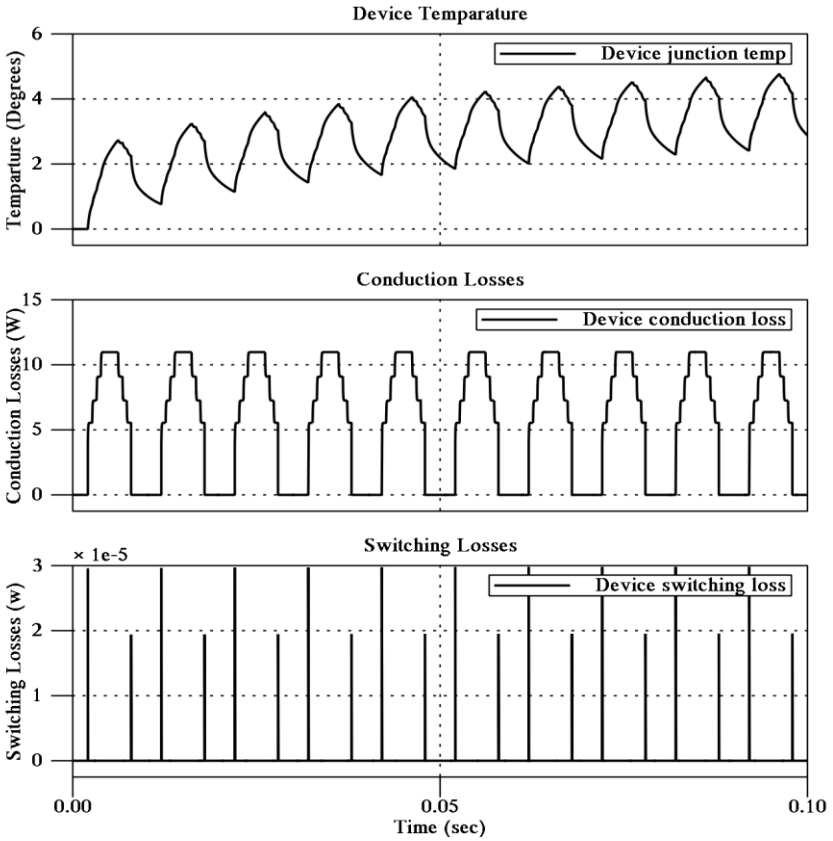
Figure 4.13 Device temperature, conduction losses & switching losses with high frequency (PDPWM) switching (a) Switch 'S1' (b) Switch 'S2' (c) Switch 'S3' (d) Switches' S4 & S5' (e) Switches' S6 & S7' using PLECS.


Device Temparature
Device junction temp
Temparture (Degrees)
6
4
2
0
Conduction Losses
Device conduction loss
Conduction Losses (W)
15
10
5
0
Switching Losses
× 1e-5
Device switching loss
Switching Losses (w)
1.5
1.0
0.5
0.0
0.00
0.05
0.10
Time (sec)

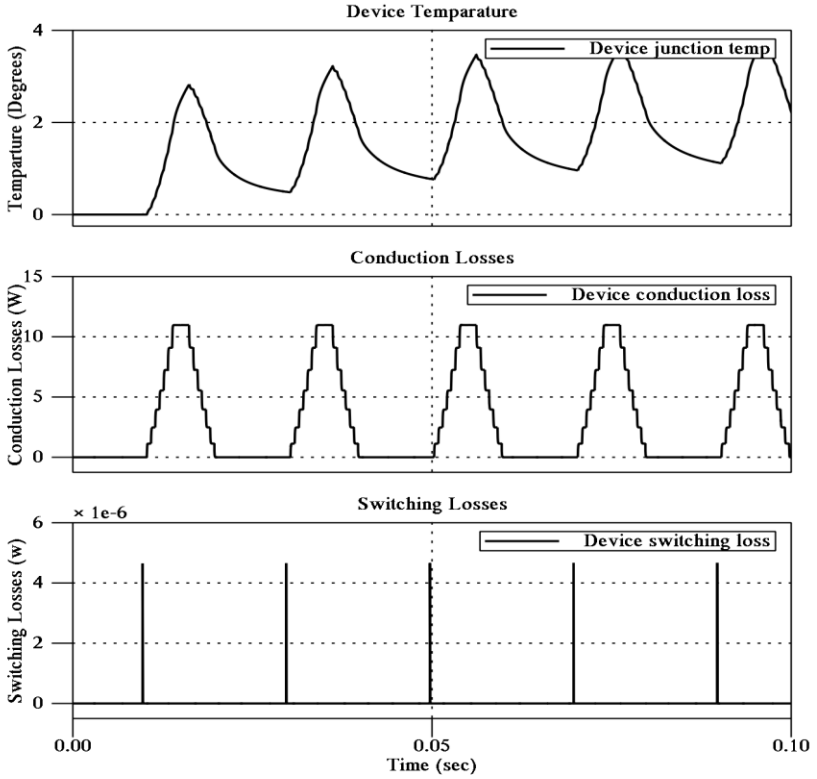
(a)


Device Temparature
Device junction temp
Temparture (Degrees)
6
4
2
0
Conduction Losses
Device conduction loss
Conduction Losses (W)
15
10
5
0
Switching Losses
× 1e-5
Device switching loss
Switching Losses (w)
3
2
1
0
0.00
0.05
0.10
Time (sec)

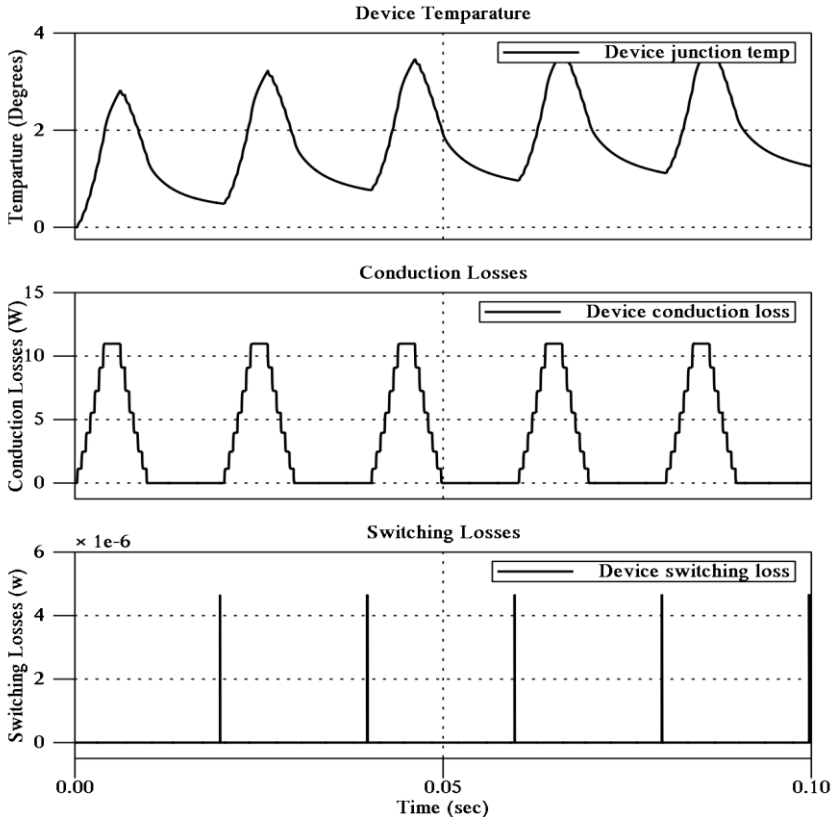
(b)


Device Temparature
Temparture (Degrees)
Device junction temp
Conduction Losses
Conduction Losses (W)
Device conduction loss
Switching Losses
× 1e-5
Switching Losses (w)
Device switching loss
0.00
0.05
0.10
Time (sec)

(c)


Device Temparature
Temparture (Degrees)
Device junction temp
Conduction Losses
Conduction Losses (W)
Device conduction loss
Switching Losses
× 1e-6
Switching Losses (w)
Device switching loss
0.00
0.05
0.10
Time (sec)

(d)



(e)

Figure 4.14 Device temperature, conduction losses & switching losses with low frequency (SHEPWM) switching. (a) Switch 'S1' (b) Switch 'S2' (c) Switch 'S3' (d) Switches' S4 & S5' (e) Switches' S6 & S7' using PLECS

The device junction temperature, conduction losses, and switching losses are plotted in figure 4.14 using low-frequency switching (SHEPWM) control. The IGBT switches' S1', 'S2', and 'S3' are high-frequency switches in the operation of the proposed inverter; hence these switches undergo ON and OFF several times resulting in more switching losses. Similarly, the switches' S4', 'S5', 'S6' and 'S7' are the low-frequency switches, which undergoes only one time for ON and OFF per cycle resulting in fewer power losses.

Further, from figures 4.13 and figure 4.14, it is observed that the magnitude of switching losses and conduction losses more using high-frequency switching (PDPWM)) compared to low-frequency switching (SHEPWM). The switching losses and conduction losses calculated from PDPWM and SHEPWM using PLECS simulation are tabulated in table 4.2 for each IGBT switch of the 15-level inverter.

Table 4.2 Power loss analysis using PLECS thermal model with PDPWM & SHEPWM switching control

Switches	High-Frequency Switching (PDPWM)			Low-Frequency Switching (SHEPWM)		
	Conduction Losses (W)	Switching Losses (W)	Total Losses (W)	Conduction Losses (W)	Switching Losses (W)	Total Losses (W)
S1	4.6019	0.0155	4.6174	4.0303	0.0091	4.0394
S2	5.4398	0.0129	5.4527	4.4049	0.0077	4.4126
S3	7.135	0.008	7.143	5.1532	0.0049	5.1581
S4	4.5187	0.002	4.5207	3.0227	0.0002	3.0229
S5	4.5187	0.002	4.5207	3.0227	0.0002	3.0229
S6	4.5187	0.002	4.5207	3.0227	0.0002	3.0229
S7	4.5187	0.002	4.5207	3.0227	0.0002	3.0229

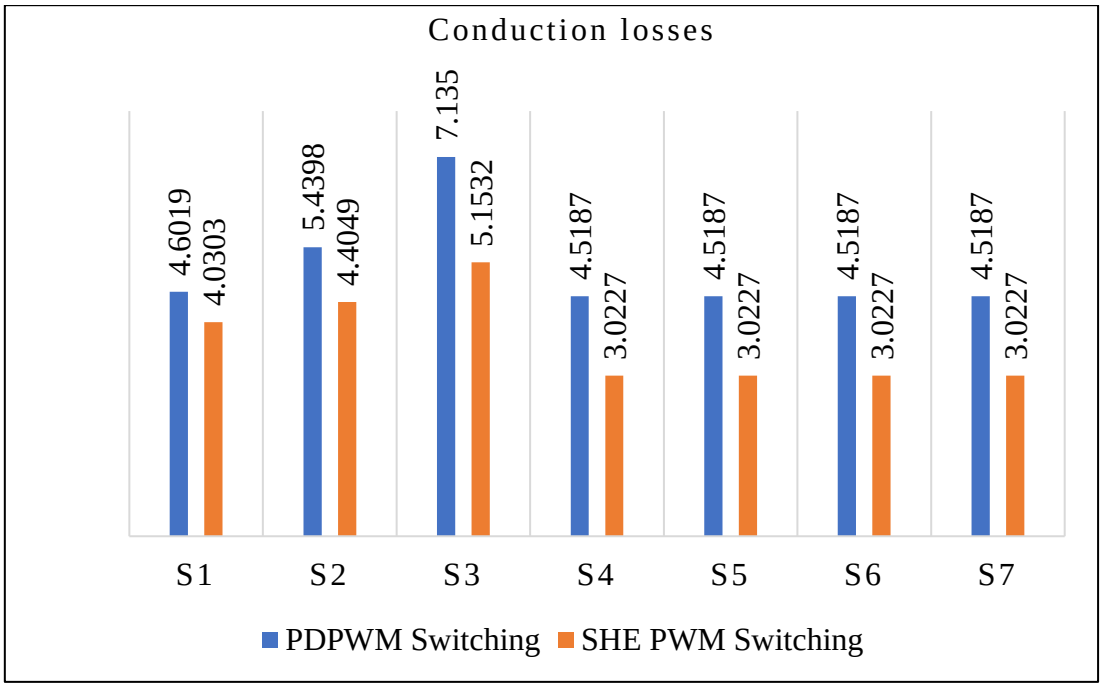


Figure 4.15 Conduction losses comparison using PLECS thermal model with PDPWM & SHEPWM switching

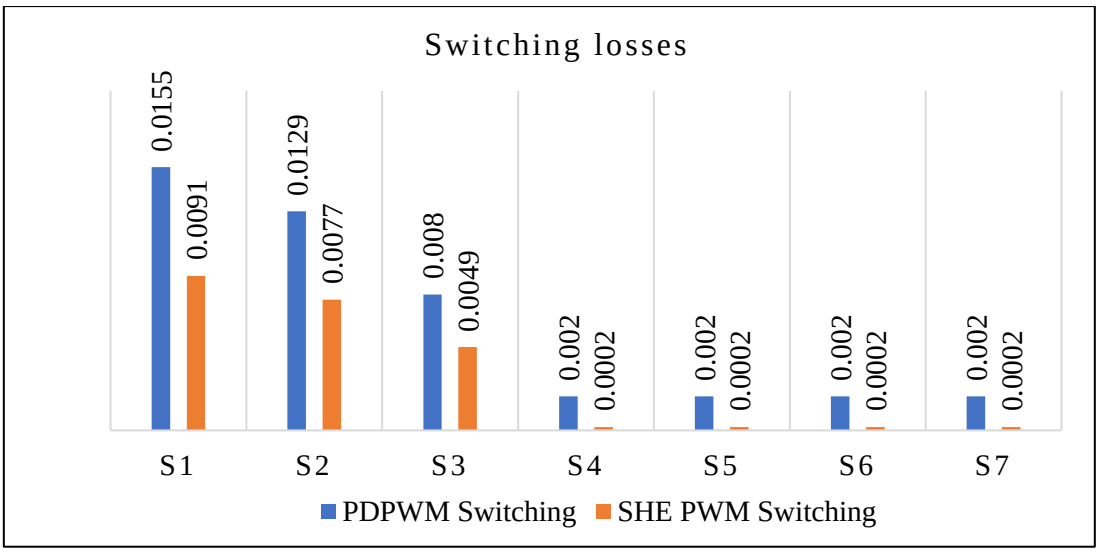
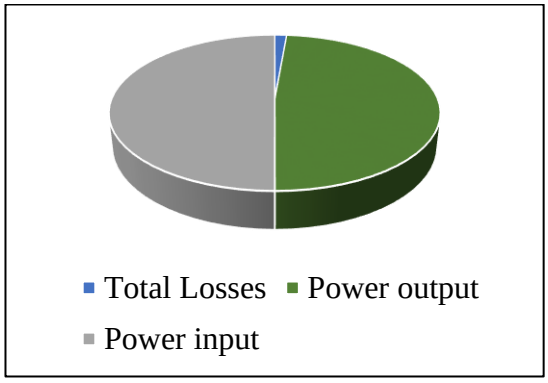
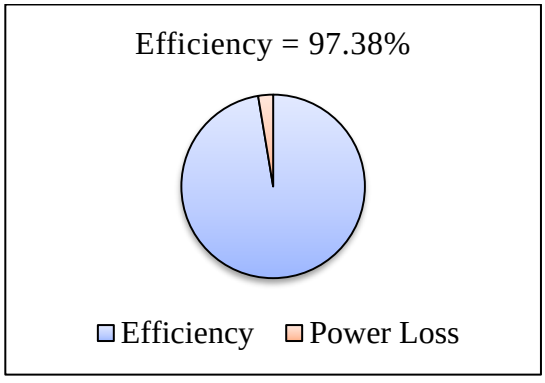


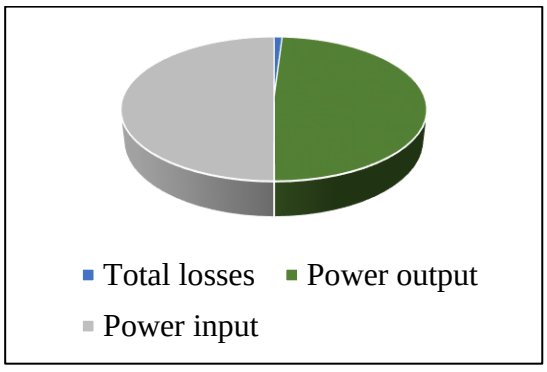
Figure 4.16 Switching losses comparison using PLECS thermal model with PDPWM & SHEPWM switching



(a)



(b)



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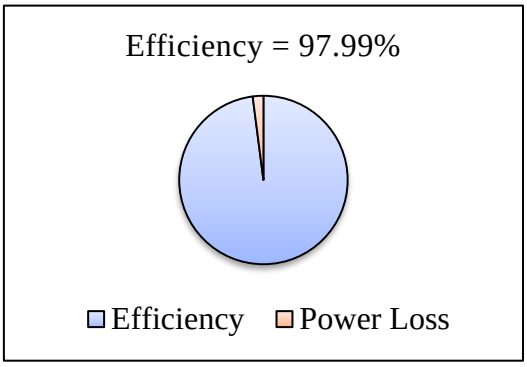


(d)

Figure 4.17 Power delivered and efficiency of the inverter using PLECS thermal model (a) Power delivered by PDPWM switching (b) Efficiency with PDPWM switching (c) Power delivered by SHEPWM switching (d) Efficiency with SHEPWM switching

The comparative analysis of conduction losses with PDPWM and SHEPWM switching control methods are given in figure 4.15. Here SHEPWM switching gives fewer conduction losses than the PDPWM. Also, the switching loss comparison analysis is shown in figure 4.16 and observed that the switching losses are comparatively low in the SHEPWM switching method than PDPWM switching control.

The proposed inverter output power is 1250W at a peak voltage of 259V and a peak current of 9.65A. The total power loss measured from the PDPWM switching method is 35.3W. The overall power losses and power output of the proposed inverter equal 1285.3W, which equals the power input of the inverter. Hence the efficiency of the 15-level inverter with PDPWM switching is determined as follows;

$$\eta_{\text{PDPWM Switching}} = \frac{\text{Output power}}{\text{Output power + Total losses}} \times 100$$

$$\eta_{\text{PDPWM Switching}} = \frac{1250}{1250 + 35.3} \times 100$$

$$\eta_{\text{PDPWM Switching}} = 97.38\%$$

Which gives the efficiency 97.38% as shown in figures (4.17a and 4.17c). The total power loss measured by SHEPWM switching control is about 25.7W. The power input using this control method is 1275.7W. Therefore the efficiency of the 15-level inverter with SHEPWM switching control is determined as;

$$\eta_{\text{SHEPWM Switching}} = \frac{\text{Output power}}{\text{Output power + Total losses}} \times 100$$

$$\eta_{\text{SHEPWM Switching}} = \frac{1250}{1250 + 25.7} \times 100$$

$$\eta_{\text{SHEPWM Switching}} = 97.99\%$$

Which gives the efficiency of 97.99%, as shown in figures (4.17b and 4.17d). With the efficiencies obtained from these two control methods, it is observed that the SHEPWM switching control offers high efficiency with low power losses than the PDPWM switching control of the 15-level inverter. Therefore the proposed 15-level asymmetric inverter is suggested to control with low switching frequency control called

selective harmonic elimination pulse width modulation (SHEPWM) for lesser switching losses and high performance.

4.6.2 Power loss analysis using precise Simulink models

The precise models presented in figures 4.10, 4.11, and 4.12 are implemented on the Simulink platform using curve fitting methods from the IGBT device datasheet. The SHEPWM (low-frequency switching) control method is used for determining the power losses using precise models. Table 4.3 depicts the power losses for all seven switches in the 15-level inverter.

Table 4.3 Power loss analysis using precise Simulink models with SHEPWM control

Switches	Conduction Losses (W)	Switching Losses (W)	Total Losses (W)
S1	4.1024	0.00878	4.1112
S2	4.4312	0.00764	4.4388
S3	5.2341	0.00531	5.2394
S4	3.0622	0.00031	3.0625
S5	3.0622	0.00031	3.0625
S6	3.0622	0.00031	3.0625
S7	3.0622	0.00031	3.0625

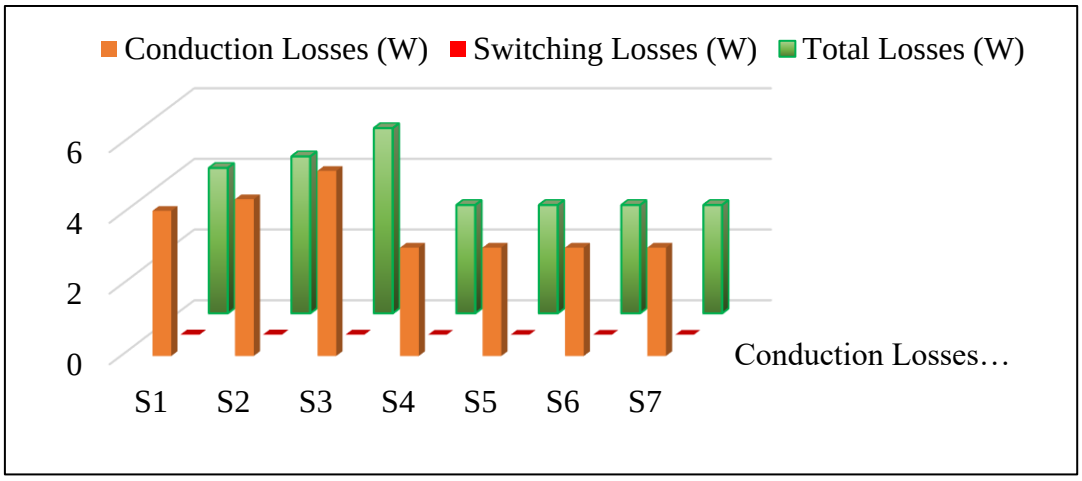
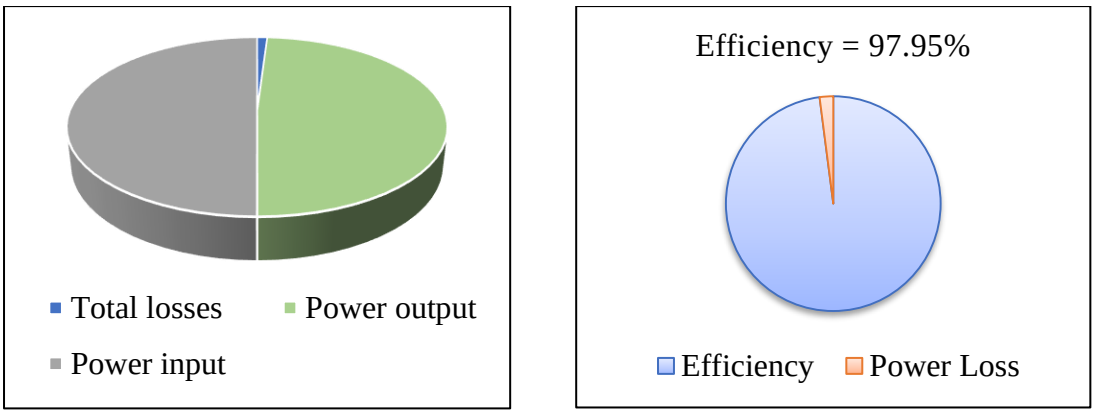


Figure 4.18 Power loss analysis using precise Simulink models with SHEPWM switching



(a) (b)

Figure 4.19 Power delivered and efficiency of the inverter using precise Simulink models (a) Power delivered by SHEPWM switching (b) Efficiency by SHEPWM switching.

The switching losses, conduction losses, and total power losses obtained from Simulink models are compared in figure 4.18. The total power losses are calculated in this analysis are 26.13W, the power delivered to the load is 1250W, and the power input is 1276.13W, which are represented in figures (4.19a and 4.19b). The efficiency of the 15-level inverter for SHEPWM switching control using precise curve fitting Simulink models is calculated as follows;

$$\eta_{\text{SHEPWM Switching}} = \frac{\text{Output power}}{\text{Output power} + \text{Total losses}} \times 100$$

$$\eta_{\text{SHEPWM Switching}} = \frac{1250}{1250 + 26.13} \times 100$$

$$\eta_{\text{SHEPWM Switching}} = 97.95\%$$

The efficiency of the 15-level inverter obtained by PLECS thermal modelling with SHEPWM switching control is 97.99%. The efficiency obtained from precise curve fitting Simulink models is 97.95%, which are approximately the same. Therefore these comparative results validate the power losses and efficiency of the proposed inverter.

The Simulink model presented in figure 4.12 has been run for different modulation indexes, and corresponding power losses are tabulated in table 4.4. The variation of power losses with modulation index is plotted in figure 4.20.

Table 4.4 Power losses with the variation of modulation index by SHEPWM control

Modulation Index	Conduction Losses (W)	Switching Losses (W)	Total Losses (W)
0.4	22.062	0.025	22.08
0.5	22.423	0.025	22.44
0.6	23.382	0.024	23.40
0.7	24.561	0.024	24.58
0.8	25.257	0.023	25.28
0.9	26.106	0.023	26.13
1.0	26.984	0.022	27.00
1.1	27.125	0.021	27.14
1.2	27.459	0.022	27.48

Figure 4.20 Power losses Vs modulation index using precise Simulink models

4.7 CHAPTER SUMMARY

Transient losses in semiconductor devices had a significant impact on the performance of the power converter circuit in which they had used. A 15-level asymmetric inverter had been designed and implemented with fewer switches suitable for PV applications. The asymmetric inverter's performance was evaluated relying on conduction and switching losses. The power losses had been determined in a 15-level asymmetric inverter using thermal modelling in PLECS and precise curve fitting

models in Simulink. The switching and conduction losses had been evaluated separately, considering junction temperature as 150^0 C and thermal impedance of 1.25Ω. The foster thermal model was designed on PLECS for a 15-level inverter, and corresponding plots were plotted for high-frequency switching (PDPWM) and low-frequency switching (SHEPWM). The efficiency of the inverter at 0.9 modulation index was proved 97.38% with PDPWM and 97.99% using SHEPWM.

Further, the precise Simulink curve fitting models had been designed on Simulink and as per the device datasheet, the model used actual voltage and energy curves. The overall inverter losses were found to constitute around 1.044% of the total power delivered by the inverter at low frequency switching control with an inverter efficiency of 97.95%. It had been concluded that the efficiency of the proposed inverter was approximately the same as 97.99% using PLECS modelling and 97.95% using curve fitting models on Simulink at low switching frequency control method.

CHAPTER-5

THD ANALYSIS OF 15-LEVEL INVERTER USING TRADITIONAL & HYBRID SOFT COMPUTING ALGORITHMS

5.1 INTRODUCTION

Elimination of harmonics in multilevel inverters is a complex task involving transcendental equations with numerous local minima. The nonlinear equations are derived from the programmed PWM method, which identifies the low-order harmonics that must be removed. The critical limitation of programmed PWM, also known as selective harmonic elimination PWM, is to solve the equations that result in better harmonic reduction [165]. The harmonic elimination in any inverter depends on the switching angles and frequency of switching. In this study, the switching angles of the proposed multilevel inverter are optimized using nature-inspired optimization algorithms.

Optimization has been the most inspiring technique for many design applications, showing significant progress in computing systems. The optimization schemes can allow organizations to define optimal requirements and optimize operations and high production efficiency. The method of formulating the objective function that a minimum problem occurs in chosen optimization strategies. Metaheuristic algorithms have mainly been employed in recent years to solve many of the nonlinear equations of all conventional optimization methodologies to give efficient solutions for real-time applications.

Certain optimization algorithms such as genetic algorithm (GA), particle swarm optimization (PSO), whale optimization algorithm (WOA) & Harris hawk algorithm (HHO) were applied for the 15-level asymmetric inverter for solving the nonlinear transcendental equations formulated by the SHEPWM problem are described in this chapter to reduce the THD of output voltage and current. Also, to improve the algorithm's performance, quality, and accuracy of the solutions, the hybridization of traditional algorithms was developed by combining the above algorithms with suitable ones to improve the mutation rate. The algorithms such as enhanced whale optimization

algorithm (EWOA), hybrid asynchronous particle swarm optimization with newton Raphson algorithm (APSO-NR), hybrid particle swarm optimization with genetic algorithm (PSO-GA), and hybrid Harris hawk with differential evolution (HH-DE) algorithms were applied to the 15-level asymmetric multilevel inverter for analyzing THD of output. The results of these algorithms are compared in terms of the number of iterations (convergence speed), THD of output voltage, and currents.

5.2 TOTAL HARMONIC DISTORTION

A periodic non-sinusoidal waveform is created by combining a succession of sine waves at different frequencies. The fundamental frequency of a waveform is often referred to as the first harmonic of that waveform. Harmonics are frequency components that are multiples of the fundamental frequency in alternating current and voltage waveforms. Example: If the fundamental frequency is 50Hz, the harmonic frequencies are 100Hz, 150Hz, and so on. Non-sinusoidal waveforms comprise the fundamental frequency of the sine wave and its harmonics, while a pure sine wave has just the fundamental frequency of the sine wave and does not contain any supplementary harmonics.

The fundamental frequency is 50Hz and additional odd harmonics such as 150Hz, 250Hz, 350Hz, etc. PWM adds high-frequency sine wave harmonics to the waveform, which must be eliminated before the grid receives a pure sine wave voltage. THD of high-quality grid-tied inverters is less than 5%. A waveform's THD is calculated by dividing the power of each harmonic by the power of the fundamental.

Total Harmonic Distortion (THD) measures how near the waveform is generated to the shape of the fundamental waveform. The THD of a waveform can be measured using equation (5.1).

$$THD = \frac{1}{V_1}\sqrt{\sum_{n=2,3\ldots}^{\infty} V_n^2} \tag{5.1}$$

Where,

V_1 = Fundamental Voltage,

V_n = voltage of the n^{th} wave

5.3 CONTROL METHODOLOGY

Figure 5.1 illustrates the control methodology for the proposed inverter. Here, the inverter is controlled by optimal switching angles. The optimal switching angles of the MLI are obtained by synthesizing the inverter's output into Fourier series representation, as shown in equation (3.2). This equation further expanded in terms of the switching angles of the inverter as given in equation (3.3). Additionally, the nonlinear transcendental equations were formulated by considering the harmonics to be minimized, as shown in equation (3.5).

Using Simulink's solver, an optimization approach is used to find the best possible switching angles based on the objective function given in equation (3.8). The fundamental output voltage equation is assigned with modulation index, which is obtained from the dc-link control. The solutions of the nonlinear equations are stored in lookup tables. Then the switching angles decoder decodes the firing angles of the corresponding switch and produces the pulse related to the corresponding switching angle.

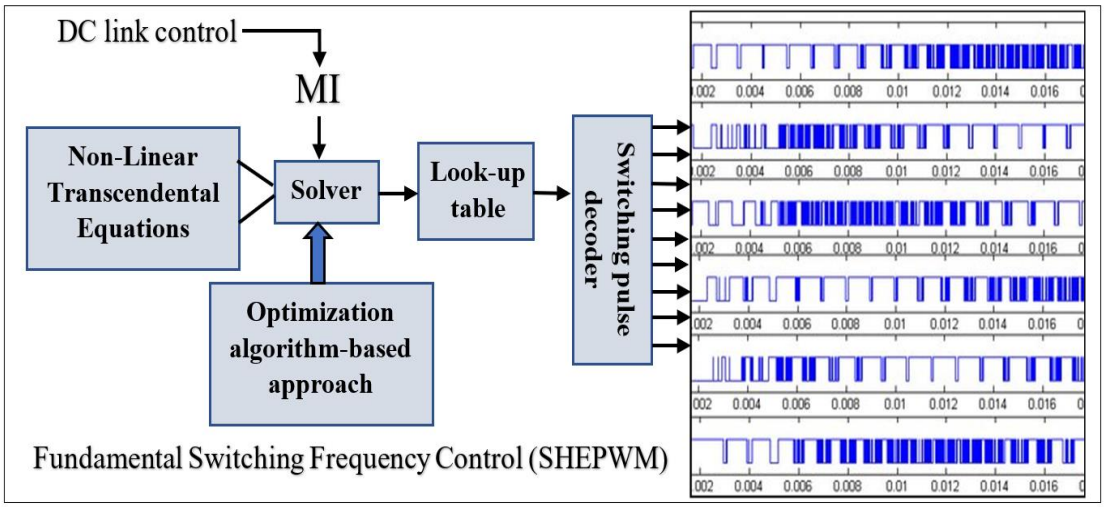


Figure 5.1 Control methodology of proposed MLI

Thus, the switching pulses for the multilevel inverter are produced using the selective harmonic elimination method using nature-inspired optimization algorithms for minimizing the THD of the inverter. Various optimization algorithms to obtain the solution of transcendental equations formulated by SHEPWM control are described in the following.

5.4 TRADITIONAL SOFT COMPUTING ALGORITHMS TO OPTIMIZE SWITCHING ANGLES OF THE 15-LEVEL INVERTER

This research presents a variety of contemporary optimization techniques inspired by real-life in nature. Optimization reveals substantial developments in computing systems and has become the most promising strategy for several design applications. These optimization schemes will be of excellent help to organizations to identify optimum criteria and improve the process and high product quality. Over the years, most combinatorics problems have been solved using metaheuristic algorithms to have optimal solutions for real-time applications. Some of those essential and feasible optimization schemes and the related algorithms and approaches are used in this work for THD optimization in the 15-level asymmetric inverter.

5.4.1 Switching angle optimization of 15-level inverter using genetic algorithm

Genetic algorithms (GA) are computerized search methods that are based on natural selection and genetics. These algorithms are beneficial for large search areas. They are navigated relatively quickly to search for suitable combinations of solution sets that could require a very long period for other techniques. Genetic algorithms are based on the population size of pre-selected candidates. The implementation of genetic algorithms takes place following phases [166].

1. ***Initialization:*** The initial population set of any candidate solutions has been created by random means of the following equation (5.2) across the whole search space, close to the center of every switching boundary. For each solution set, the number of populations is 20.

$$\alpha_{ij}^{IP} = \alpha_{ij} + \left| \alpha_{ij}^{L} \pm rand_j \left\{ \frac{\left(\alpha_{ij}^{U} - \alpha_{ij}^{L}\right)}{2} \right\} \right| \tag{5.2}$$

   Where, α_{ij}^{IP} represents initial population matrix, α_{ij}^{L} initial guess of solutions from $\alpha_1 to\ \alpha_7$

2. ***Evaluation:*** The objective values of the candidate solutions will be determined using the pre-formulated objective function shown in equation (3.8) when the population set for each switching angle is initialized, or the offspring populations are established.

3. ***Selection:*** Several higher objective values have been chosen to produce offspring, thus applying the most suitable survival strategy for the candidates' solutions. This is done by calculating the cumulative probability using the objective value of each population with the random number (0,1) provided by the selection of the roulettes.
4. ***Crossover or Recombination:*** Combining two or more parental solutions blends to generate multiple (e.g., offspring) solutions. Each solution is converted into 11-bit binary, parental pairs have been randomly picked for crossover solutions; a random number 'r' is generated for each pair in the random variant of (0,1) so that "r" is equal to a predetermined crossover probability (here, 0.6), intending to decide whether it should be perforated. A random number of (0,1) were produced to choose a convergence point when it was found. A single point crossover has been used here.
5. ***Mutation:*** By recombining two or more parental chromosomes, local yet random mutations alter a solution to boost the solution. Here too, for and descendant, a random number 'r' between (0,1) is generated in which the 'r' contrasts with the predetermined mutation probability (here 0.1). A random number was generated between (0,1) when the mutation was deemed appropriate to select the point of mutation, and this specific bit was complemented.
6. ***Replacement:*** Selecting, recombining, and mutating the parental population of the first generation was used to replace the parents of the second generation.
7. ***Termination:*** The termination criteria are set for 200 iterations. Until a given termination condition was met, steps 2-6 were repeated.

The proposed 15-level inverter's switching angles are updated using this technique for each iteration. The switching angles for modulation index for 0.5 to 1 were determined using a genetic algorithm and tabulated in table 5.1. The corresponding THD of output voltage for all of these modulation indexes is also calculated and found to be the minimum (6.25%) at 0.9 modulation index. The genetic algorithm takes 103 iterations to converge the solution of transcendental equations. The convergence characteristics with the number of iterations Vs objective function values (THD) are shown in figure 5.2.

Table 5.1 Switching angles and THD of output voltage with the variation of modulation index using genetic algorithm

S. No	M_i	α_1	α_2	α_3	α_4	α_5	α_6	α_7	%THD
1	0.5	6.32^0	13.71^0	23.56^0	36.3^0	49.42^0	58.8^0	67.3^0	**10.42**
2	0.55	6.54^0	12.51^0	23.58^0	35.78^0	46.32^0	57.1^0	66.8^0	**9.85**
3	0.6	6.31^0	12.16^0	23.31^0	37.4^0	45.76^0	55.7^0	65.8^0	**9.37**
4	0.65	5.82^0	12.11^0	22.56^0	36.57^0	45.91^0	54.32^0	65.57^0	**8.28**
5	0.7	5.78^0	12.16^0	22.35^0	37.61^0	46.24^0	55.12^0	65.36^0	**7.27**
6	0.75	5.82^0	12.12^0	22.93^0	37.34^0	46.46^0	55.78^0	64.21^0	**6.8**
7	0.8	5.78^0	11.91^0	22.48^0	36.67^0	45.38^0	55.67^0	63.7^0	**6.67**
8	0.85	5.91^0	11.22^0	20.53^0	31.26^0	40.36^0	51.78^0	62.32^0	**6.45**
9	**0.9**	$\mathbf{5.61^0}$	$\mathbf{10.93^0}$	$\mathbf{18.62^0}$	$\mathbf{26.54^0}$	$\mathbf{34.82^0}$	$\mathbf{44.62^0}$	$\mathbf{61.21^0}$	**6.25**
10	0.95	5.92^0	11.05^0	19.21^0	26.23^0	34.39^0	46.48^0	62.92^0	**6.31**
11	1	5.06^0	12.32^0	22.3^0	36.5^0	44.27^0	55.8^0	65.23^0	**6.39**

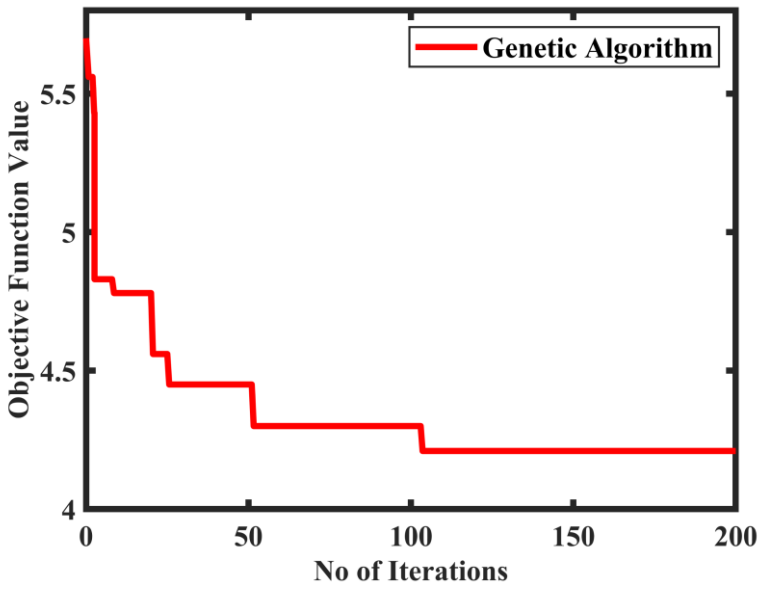


Figure 5.2 Convergence characteristics using genetic algorithm

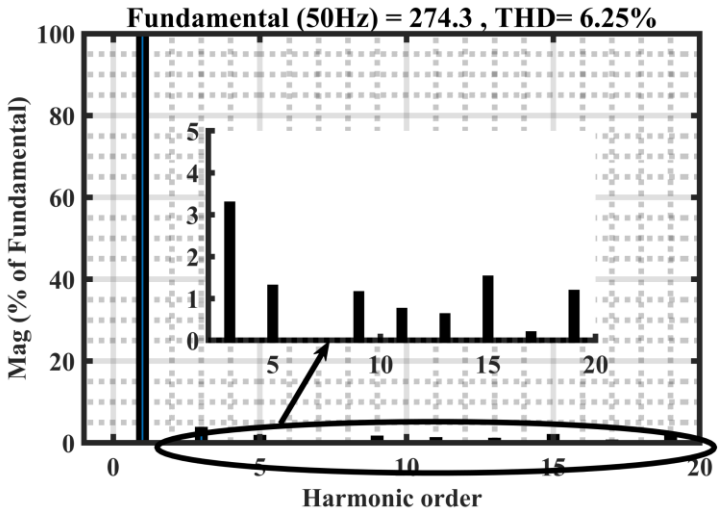


Figure 5.3 Voltage harmonic distortion using genetic algorithm

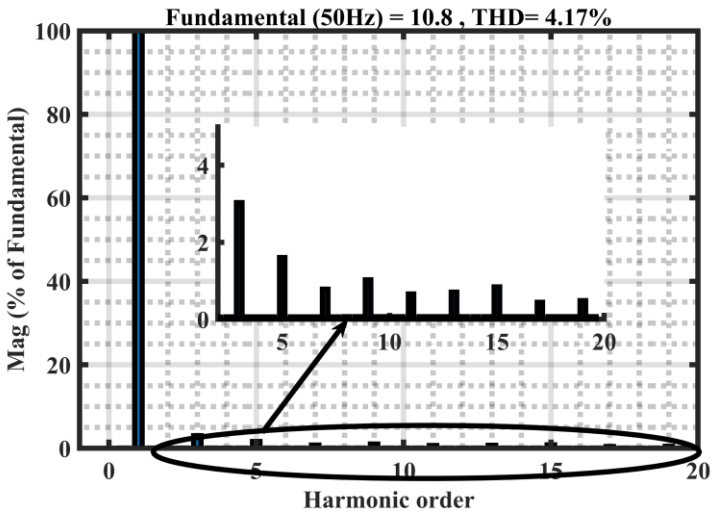


Figure 5.4 Current harmonic distortion using genetic algorithm

The total harmonic distortion (THD) of the output voltage and current of the 15-level inverter are determined by optimizing the switching angles using a genetic algorithm at a modulation index of 0.9. The total harmonic distortion of the output voltage is 6.25% at 243.7V, as seen in figure 5.3, and the total harmonic distortion of the output current is 4.17% at 10.8A, as illustrated in figure 5.4.

5.4.2 Switching angle optimization of 15-level inverter using PSO algorithm

PSO is defining swarms' sociological behavior. Each particle's PSO vectors are 1 x N and the vector of each particle. The best individual location in an identified particle is the local best, and the best position in the whole swarm is the global best. PSO is ideally suited to solving complex problems due to its low computation effort

and quick computer coding. Initial values such as other traditional iterative methods are not required for PSO. In the following steps, the PSO mechanism is articulated:

Step 1: Initialize the parameters of particle vectors X_i, V_i, P_{best}, G_{best}, and inertia weight of the particle C_0. Choose the number of generations as 200, size of the population as 50 and every particle is randomly initialized as switching angles between 0^0 and 90^0.

Step 2: Test the conditions for and $(C_1 + C_2)/2 < C_0 < 1$. The system would then be guaranteed to converge to a stable equilibrium if the two criteria were met. If false, go to Step 1.

Step 3: The new position and velocity vectors of particles were determined using (5.3)

$$v_l^i(t+1) = w(t).v_l^i(t) + C_{ind}.rand1,(p_l^i - x_l^i(t) + C_{soc}.rand2.(G^i - x_l^i(t)) \quad (5.3)$$

Then the new position is defined as,

$$x_l^i(t+1) = x_l^i(t) + v_l^i(t+1) \quad (5.4)$$

Step 4: Evaluate the objective function of the particles using equation (5.5) to find the switching angles (1 to 7), such that the harmonics of the 5^{th}, 7^{th}, 11^{th}, 13^{th}, 17^{th} and 19^{th} harmonics are eliminated at the inverter output.

$$OF = \min_{\alpha_k}\left\{\left(100 \times \frac{V_1^* - V_2}{V_1^*}\right)^4 + \sum_{k=2}^{N}\frac{1}{h_k}\left(50 \times \frac{V_{h_k}}{V_1}\right)^2\right\} \quad (5.5)$$

Step 5: Check for the constraint of the objective function as

$$\alpha_1 < \alpha_2 < \alpha_3 < \alpha_4 < \alpha_5 < \alpha_6 < \alpha_7 < \frac{\pi}{2} \quad (5.6)$$

Step 6: Check for $P(X_i) < P(P_i)$, if not then i = i + 1 go to step3.

Step 7: Update the particle's best local position if the best local position is better than before. Thus replaces the local best position.

Step 8: Pg = min (P neighbor).

Step 9: Termination criteria for a maximum of 200 iterations and terminate the process if the optimal switching angles are achieved.

The switching angles for each modulation index are computed offline and stored in lookup tables. The switching angles for modulation index for 0.5 to 1 were determined using the PSO algorithm and tabulated in table 5.2. The corresponding THD

of output voltage for all of these modulation indexes is calculated and found to be the minimum (5.74%) at 0.9 modulation index.

Table 5.2 Switching angles and THD of output voltage with the variation of modulation index using PSO

S. No	M_i	α_1	α_2	α_3	α_4	α_5	α_6	α_7	%THD
1	0.5	5.48^0	12.78^0	21.86^0	35.4^0	47.42^0	56.8^0	64.3^0	**9.42**
2	0.55	5.34^0	11.56^0	23.61^0	36.3^0	45.32^0	56.1^0	62.8^0	**7.85**
3	0.6	5.21^0	10.76^0	22.36^0	37.4^0	45.76^0	54.7^0	63.8^0	**7.37**
4	0.65	4.88^0	11.21^0	21.56^0	36.56^0	44.91^0	55.32^0	64.5^0	**7.28**
5	0.7	4.59^0	11.56^0	22.35^0	37.61^0	43.24^0	56.12^0	65.32^0	**7.27**
6	0.75	4.36^0	12.32^0	22.93^0	36.34^0	41.46^0	56.78^0	64.21^0	**6.8**
7	0.8	4.19^0	11.98^0	20.68^0	35.67^0	42.38^0	54.67^0	65.7^0	**6.5**
8	0.85	4.03^0	12.2^0	21.56^0	31.26^0	42.36^0	53.67^0	64.32^0	**6.19**
9	**0.9**	$\mathbf{3.9^0}$	$\mathbf{12.1^0}$	$\mathbf{20.9^0}$	$\mathbf{29.9^0}$	$\mathbf{38.1^0}$	$\mathbf{48.7^0}$	$\mathbf{61.1^0}$	**5.74**
10	0.95	4.23^0	12.18^0	19.16^0	28.91^0	41.2^0	51.72^0	62.3^0	**6.17**
11	1	4.41^0	12.32^0	22.2^0	31.52^0	42.7^0	52.8^0	63.23^0	**6.30**

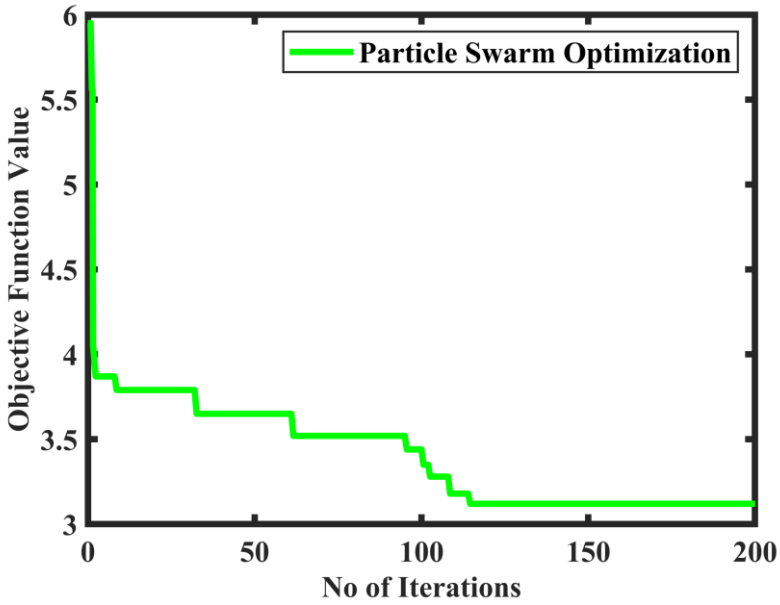


Figure 5.5 Convergence characteristics using PSO algorithm

The PSO takes 114 iterations to converge the solution of transcendental equations. The convergence characteristics with the number of iterations Vs objective function values (THD) are shown in figure 5.5.

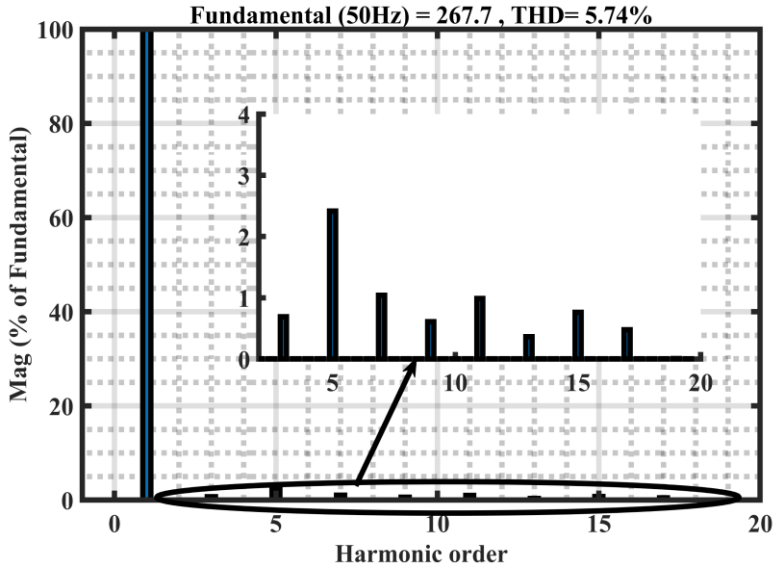


Figure 5.6 Voltage harmonic distortion using PSO algorithm

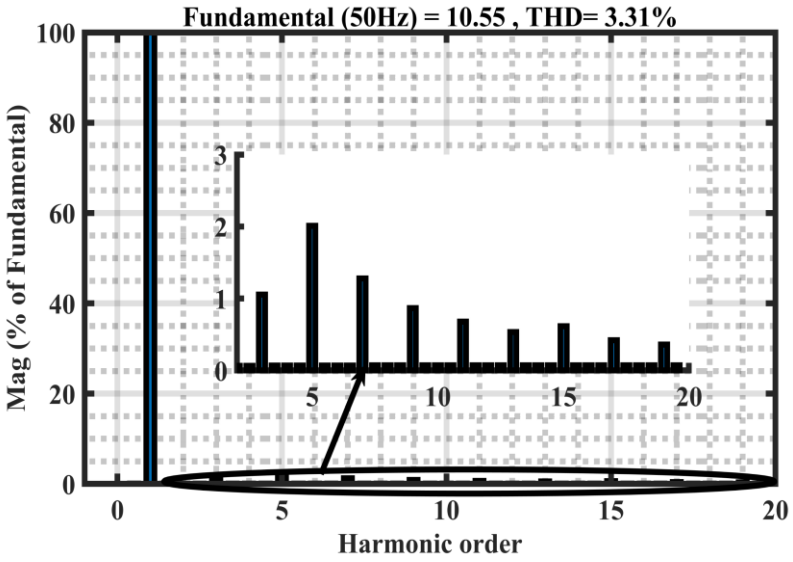


Figure 5.7 Current harmonic distortion using PSO algorithm

The total harmonic distortion (THD) of the 15-level inverter output is measured using switching angles calculated by the PSO method at a modulation index of 0.9. The output voltage's total harmonic distortion (THD) is 5.74% at 267.7V, as shown in figure 5.6, and the total harmonic distortion (THD) of the output current is 3.31% at 10.55A, as shown in figure 5.7.

5.4.3 Switching angle optimization of 15-level inverter using WOA algorithm

The whale optimization algorithm is a population-oriented algorithm that was developed in 2016 by Mirjalili & Lewis. This algorithm simulates humpback whales' social behavior. WOA, like other population-based algorithms, uses a random solution and three rules to update and develop candidate solutions in each stage that encircle the prey, spiral update position, and search for target [125].

a) Exploitation Phase: Bubble net attacking

The algorithm comprises two steps; the first step concerns the exploitation phase with encircling pray and the spiral position updating. The second step is the exploration phase called searching pray. There are two approaches for modeling the behavior of humpback whales in the Bubble Sea, which is called mathematical exploitation.

(1) Encircling Prey: After discovering the position of the prey, they surround them. Therefore, the WOA algorithm implies that the current leading candidate solution is the optimal target, assuming that the appropriate solution is not in the search area. The other search agents then seek to switch their location to the better search agents. The following equations describe this behavior

$$\vec{X}(t+1) = \vec{X}^{*}(t) - \vec{A}.\vec{D} \tag{5.7}$$

$$\vec{D} = \left|\vec{C}.\vec{X}^{*}(t) - \vec{X}(t)\right| \tag{5.8}$$

Where $\overrightarrow{X^{*}}(t)$ is the previous best location for the whale in iteration t. is $\overrightarrow{X}(t+1)$ is the current location of the whale, $\vec{D}$ is a vector distance between pray and whale, and || indicates absolute value. The coefficients C and A are calculated as follows:

$$\vec{A} = 2.\vec{a}.\vec{r} + \vec{a} \tag{5.9}$$

$$\vec{C} = 2.\vec{r} \tag{5.10}$$

The value is decreased to apply shrinking in equation (5.9); therefore, the range of oscillation of $\vec{A}$ is also decremented by $\vec{a}$. The $\vec{A}$ value could be lie in $(-a, a)$ interval, where iterations reduce weight from 2 to 0. By choosing random values of $\vec{A}$ between (−1, 1), any search agent may decide the new position somewhere between the agent's original location and the existing best agent location.

(2) Spiral position Updating: The interval between the whale and the prey is estimated at (X, Y), and the prey is positioned at (X*, Y*). In this case, a spiral approximation between the whale's location and the prey is generated to track the humpback whales' loop movement as follows:

$$\vec{X}(t+1) = e^{bk}.\cos(2\pi k).\vec{D}^{*} - \vec{X}^{*}(t) \tag{5.11}$$

$$\vec{D}^{*} = \left|\vec{X}^{*}(t) - \vec{X}(t)\right| \tag{5.12}$$

Where b is the logarithmic spiral's scalar quantity and k is a random number in the range [-1, 1]. This behabehaviorluences the role of whales in the WOA while optimizing. The shrinking circular pattern and the spiral pattern have a 50% chance of being chosen, and the following are the elements of each:

$$\vec{X}(t+1) = \begin{cases} \vec{X}^{*}(t) - \vec{A}.\vec{B}, p < 0.5 \\ e^{bk}.\cos(2\pi k).\vec{D}^{*} - \vec{X}^{*}(t), p > 0.5 \end{cases} \tag{5.13}$$

Where p is an arbitrary number in the range (0, 1).

b) Exploration Phase: Searching Pray

In the exploration phase of the search process for the prey, a particular method based on the vector $\vec{A}$ variances may be used. The whales deliberately search at random to find their food based on the location of one another. As a result, WOA forces the search agents to move away from the local whale by using the vector $\vec{A}$ with random values greater or smaller than 1. The search agent's position is randomly selected instead of the best search agent being reorganized during the discovery period.

$$\vec{X}(t+1) = \vec{X}_{rand} - \vec{A}.\vec{B} \tag{5.14}$$

$$\vec{D} = \left|\vec{C}.\vec{X}_{rand} - \vec{X}\right| \tag{5.15}$$

While implementing the WOA to SHEPWM for the proposed 15-level inverter, the number of iterations is considered 200, and the population size is 100. The search agent dimension is regarded as seven (for the switching angles α_1, α_2 ……. and α_7). The initialization matrix is created with seven columns and seven rows. The population

is initialized randomly between [0^0 and 90^0]. The fitness value of each whale or search agent during the i^{th} iteration can e represented as,

$$G_{best}^{i} = \left[best_{1,}^{i}\ best_{2,}^{i} \ldots\ldots, best_{d}^{i}\right] \tag{5.16}$$

$$\alpha_{k}^{i} = \left[\alpha_{k,1}^{i},\ \alpha_{k,2}^{i}, \ldots\ldots \alpha_{k,d}^{i}\right] \tag{5.17}$$

Where, k = 1, 2, ……, n

n = number of populations

d = number of decision variables

α = Switching angle

B will be utilized to choose the best search agent. Every iteration, all search agents move to either the best fitness obtained so far or a random search agent. To switch between exploration and exploitation, modify b from 2 to 0.

The value of p in each iteration determines whether a circular or spiral bubble-net trajectory is chosen. The locations of all search agents will be updated based on which search agent has the best fitness value. The process is performed as many times as necessary until the stated maximum number of iterations is met. The algorithm will terminate after it has discovered the global best solutions for all modulation indexes.

The switching angles for modulation index for 0.5 to 1 were determined using the WOA algorithm and tabulated in table 5.3. The corresponding THD of output voltage for all of these modulation indexes is calculated and found to be the minimum (5.73%) at 0.9 modulation index. The WOA takes 109 iterations to converge the solution of transcendental equations. The convergence characteristics with the number of iterations Vs objective function values (THD) are presented in figure 5.8.

The total harmonic distortion (THD) of the output voltage and current of the 15-level inverter is measured using switching angles determined by the whale optimization method at a modulation index of 0.9. According to figure 5.9, the total harmonic distortion (THD) of the output voltage is 5.73% at 265.7V, and the total harmonic distortion (THD) of output current is 3.98% at 10.48A, according to figure 5.10.

Table 5.3 Switching angles with the variation of modulation index using a whale optimization algorithm

S. No	M_i	α_1	α_2	α_3	α_4	α_5	α_6	α_7	%THD
1	0.5	6.82^0	13.62^0	24.53^0	37.25^0	46.1^0	56.82^0	67.46^0	**8.61**
2	0.55	6.46^0	13.21^0	24.11^0	36.81^0	45.51^0	56.12^0	66.89^0	**7.65**
3	0.6	6.12^0	12.49^0	23.72^0	36.25^0	45.03^0	54.59^0	66.48^0	**7.25**
4	0.65	5.89^0	12.81^0	23.36^0	36.49^0	44.35^0	55.34^0	65.38^0	**6.98**
5	0.7	5.63^0	12.53^0	22.95^0	36.21^0	43.18^0	54.67^0	64.85^0	**6.77**
6	0.75	5.32^0	11.99^0	22.58^0	34.28^0	42.58^0	53.48^0	65.78^0	**6.48**
7	0.8	4.95^0	12.47^0	21.82^0	32.75^0	42.22^0	52.94^0	65.65^0	**6.24**
8	0.85	4.45^0	12.13^0	21.39^0	30.82^0	41.46^0	51.16^0	64.45^0	**5.91**
9	**0.9**	$\mathbf{4.32^0}$	$\mathbf{11.89^0}$	$\mathbf{20.61^0}$	$\mathbf{28.64^0}$	$\mathbf{40.62^0}$	$\mathbf{48.51^0}$	$\mathbf{63.63^0}$	**5.73**
10	0.95	4.13^0	11.52^0	20.27^0	27.91^0	40.22^0	49.72^0	63.13^0	**5.86**
11	1	4.32^0	11.96^0	21.52^0	29.16^0	41.15^0	51.38^0	63.41^0	**5.98**

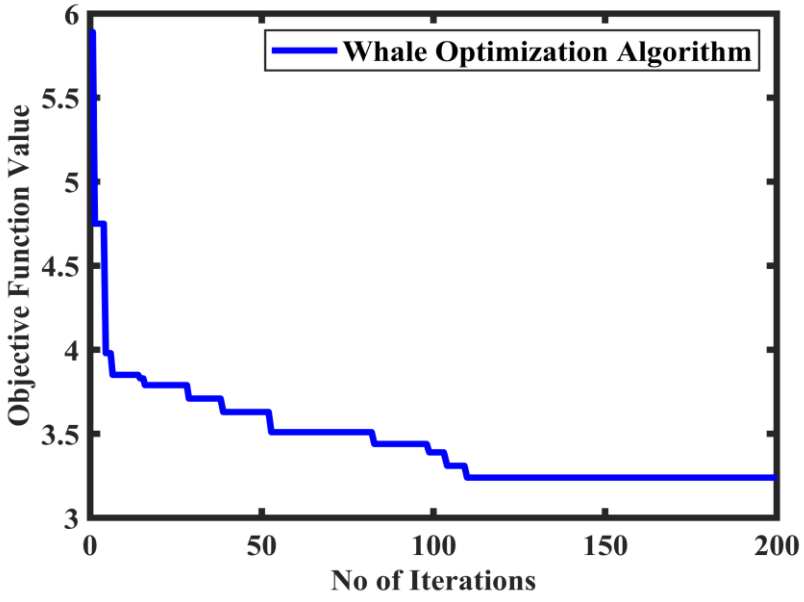


Figure 5.8 Convergence characteristics using the whale optimization algorithm

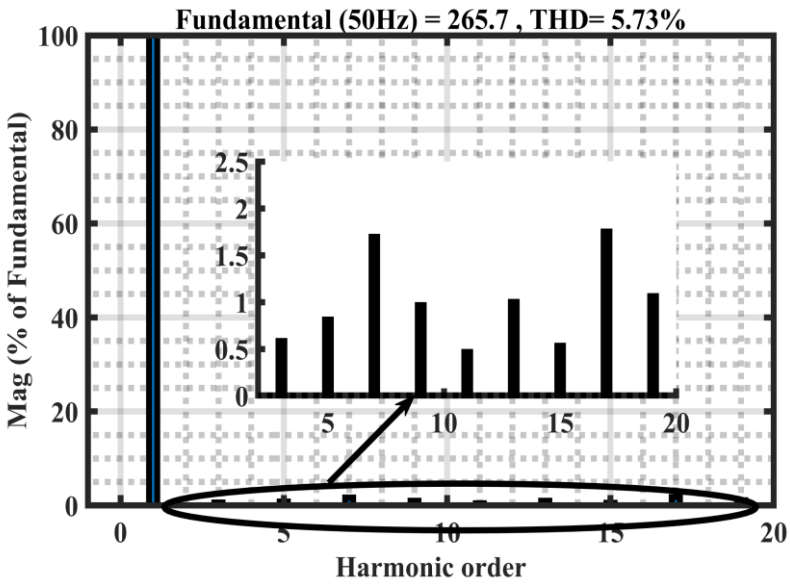


Figure 5.9 Voltage harmonic distortion using the whale optimization algorithm

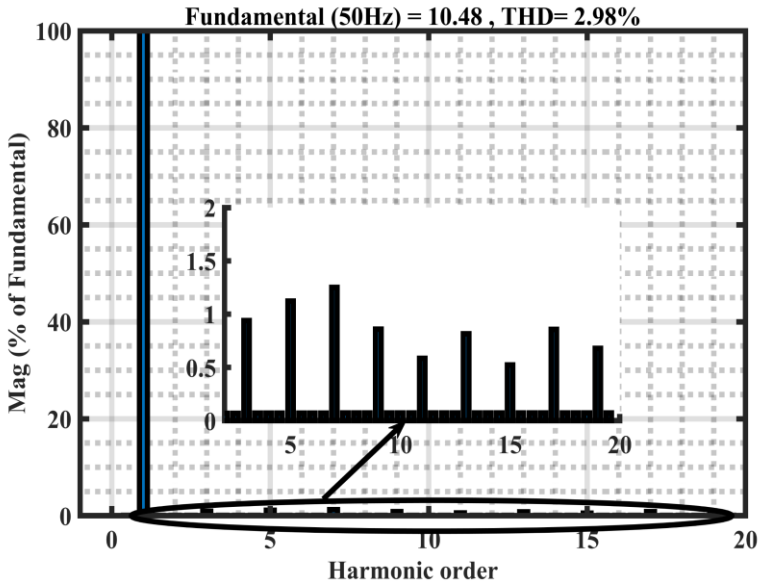


Figure 5.10 Current harmonic distortion using the whale optimization algorithm

5.4.4 Switching angle optimization of 15-level inverter using HHO algorithm

An optimization model influenced by nature is the Harris Hawk Optimizer. The wild Harris' hawks' coordinated behavior and pursuing manner inspired HHO called surprise pounce. Several hawks cooperate to swoop on prey from various angles. Harris hawks can reveal various chase patterns depending on the situation's complexity and

the prey's escaping patterns. For optimum MLI switching angles using SHEPWM, Harris hawk's knowledge while hunting pray is mathematically formulated [180].

The Harris hawk has a distinctive community that aims to track, encircle, smoot, and capture the likely prey within a group. This species is among the most knowledgeable and distinguished birds of predatory nature. In the first population, seven killing tactics or surprise pounces are assumed to be a group of hawks who wish to achieve the aim (optimization problem solution). Suppose the animal does not catch because of the complication of appearance and the escaping actions of the prey. In that case, swaps are pursued to reach the other hawks after capturing the escaping prey. The most significant advantage is that the birds follow their goal by puzzling and completing their escape. HHO gives Harris Hawks the solution, and the targeted pray is the best solution.

Step1-Exploration Phase: Harris hawks stick up arbitrarily, sit in certain areas, follow and track the prey. The leader hawks are focused on the location of the communities and their prey. This is defined as a mathematical equation for distance (q) switch between hawks and prey, as follows:

$$X(t+1)=\begin{cases} X_{rand}(t)-r_1X_{rand}(t)-2r_2X(t), & q\geq 0.5 \\ X_r(t)-X_m(t)-r_3(L_B+r_4(U_B-L_B)), & q<0.5 \end{cases} \tag{5.18}$$

Where, $r_1,\ r_2,\ r_3, r_4\ and\ q$ are the random values in the range between 0 and 1. $X(t+1)$ is the position update vector of the Hawk for the $(i+1)^{th}$ iteration, $X_r(t)$ is the position of the pray and $X(t)$ is the position vector of the Hawk at the i^{th} iteration. U_B & L_B are the Upper & Lower bounds, respectively and $X_{rand}(t)$, $X_m(t)$ are the random populations.

Each Hawk has an average position as:

$$X_{i+1}(t)=\frac{1}{N}\sum_{i=1}^{N}X_i(t) \tag{5.19}$$

Where,

$X_i(t)$ = Hawks current position.

$X_{i+1}(t)$ = Updating position vector.

N = Number of Hawks.

Step2 - The hawks are attempting to identify and reach the prey during the exploration phase. As a result, the energy (E) of the prey is significantly modified and provided by

$$\text{Escaping Energy, } E = 2E_0\left(1-\frac{t}{T}\right) \tag{5.20}$$

Where T is the maximum iteration number, t is the current iteration, and the initial energy (E_0) varies at random from (-1 to 1) during each iteration. $E \geq 1$ Indicates that the prey is tired and that hawks are looking for prey in a new location. $E < 1$ also indicates that the prey is tired and that its attack is intensified by fast striking.

Step3 - Exploitation phase: The switching tactics will begin to focus on the prey at this stage. The prey still tends to escape from the hawks, and it is seen that the potential to escape the prey is 'r'. If r<0.5 the prey can escape safely; if r≥0.5 it would be unable to escape. Even so, the hawks target the prey and win or lose in a soft or hard siege. The hard siege takes place as the prey escapes if (r≥0.5) and $|E|< 0.5$. If (r≥0.5) and $|E|\geq 0.5$ then there will be a soft siege. 'r' is a chance for the prey to escape here. It can be modeled in the following mathematical form in steps 4 to 7.

Step4 - Soft siege: The prey here (switching angle for proposed problem) has potential and is trying to escape by sprouting and is smoothly modeled around the hawks.

$$X(t+1) = \Delta X(t) - E\left|JX_\alpha(t) - X(t)\right| \tag{5.21}$$

$$\Delta X(t) = X_\alpha(t) - X(t) \tag{5.22}$$

$J = 2(1-r_5)$ is the prey jumps at random

$\Delta X(t)$ is the difference in the position of the vector in successive iterations to r_5, which is a random number inside the (0,1) range.

Step5 - Hard siege: The prey in this situation is completely tired and barely surrounded by the hawks and surprise. The locations will be updated by (5.22)

$$X(t+1) = X_\alpha(t) - E\left|\Delta X(t)\right| \tag{5.23}$$

Step6 - Soft siege with continued rapid dives: The prey still has the energy and is attempting to get away from it, which can be summarized as total and r<0.5, with a soft siege needed to begin until the hawks begin to pounce. This move is more intelligent than in the past. The Levy flight (LF) concept has been applied to progressive rapid

dives of hawks for the soft siege, and the next move is calculated by the hawks using the following equation:

$$Y = X_{\alpha}(t) - E\left|JX_{\alpha}(t) - X(t)\right| \tag{5.24}$$

Although they have attempted several times, the hawks compare each movement with the previous dive to determine whether it was successful. If diving is unsuccessful, the animal is treated irregularly, briefly, and rapidly. We presume that the hawks dive in the following rules based on LF patterns:

$$Z = Y + S \times LF(D) \tag{5.25}$$

Where D is the dimension of the problem, S is the random vector 1 to D, and LF is the levy flight function to follow:

$$LF(x) = 0.01 \times \frac{\mu \times \sigma}{|v|^{1/\beta}} \tag{5.26}$$

$$\sigma = \left(\frac{\tau(1+\beta) \times \sin\left(\frac{\pi\beta}{2}\right)}{\tau\left(\frac{1+\beta}{2}\right) \times \beta \times 2^{\left(\frac{\beta-1}{2}\right)}} \right)^{\frac{1}{\beta}} \tag{5.27}$$

Where u and v are unintended values (0, 1) and β are expected to be 1.5. Therefore, in the soft siege phase, the last upgrade rule of the hawk position is:

$$X(t+1) = \begin{cases} Y, F(Y) < F(X(t)) \\ Z, F(Z) < F(X(t)) \end{cases} \tag{5.28}$$

Where Y and Z are calculated using (5.24) and (5.25).

Step7 - In this case, a hard siege of relentless quick dives: and r<0.5 are lost and exhausted. The hawks then use a hard siege, in which they keep their distance from the prey to kill it. The updating rule in this case is:

$$Y = X_{\alpha}(t) - E\left|JX_{\alpha}(t) - X_{m}(t)\right| \tag{5.29}$$

$$Z = Y + S \times LF(D) \tag{5.30}$$

For the latest iteration, Y and Z at (5.29) and (5.30) are the next positions before the prey is killed, i.e. the optimal solution is achieved.

The SHEPWM transcendental equations are solved using the harris hawk optimization method to get the switching angles of the proposed 15-level inverter. The switching angles for various modulation indexes are computed and stored in lookup tables, satisfying all load conditions. For a given modulation index or varying load conditions, these angles are retrieved from memory in real-time. The switching angles for modulation index for 0.5 to 1 were determined using the harris hawk algorithm and tabulated in table 5.4.

Table 5.4 Switching angles with the variation of modulation index using harris hawk optimization algorithm

S. No	**M_i**	**α_1**	**α_2**	**α_3**	**α_4**	**α_5**	**α_6**	**α_7**	**%THD**
1	0.5	7.59^0	14.25^0	25.61^0	38.65^0	47.29^0	58.23^0	67.38^0	**7.76**
2	0.55	6.92^0	13.35^0	24.55^0	37.71^0	46.23^0	57.65^0	66.71^0	**7.45**
3	0.6	6.45^0	13.86^0	23.49^0	36.92^0	45.64^0	56.38^0	66.23^0	**7.03**
4	0.65	5.92^0	13.54^0	22.75^0	35.87^0	44.56^0	55.82^0	65.55^0	**6.76**
5	0.7	5.65^0	12.65^0	21.86^0	34.06^0	43.28^0	54.87^0	65.73^0	**6.59**
6	0.75	5.19^0	12.23^0	21.35^0	32.84^0	42.45^0	53.68^0	65.37^0	**6.13**
7	0.8	4.58^0	11.85^0	20.95^0	31.54^0	41.22^0	52.58^0	64.41^0	**5.84**
8	0.85	4.23^0	11.59^0	20.52^0	29.67^0	40.12^0	51.65^0	63.16^0	**5.63**
9	**0.9**	**3.91^0**	**11.43^0**	**19.55^0**	**28.91^0**	**39.22^0**	**50.51^0**	**62.63^0**	**5.51**
10	0.95	3.87^0	11.37^0	19.32^0	27.42^0	38.69^0	49.46^0	63.13^0	**5.65**
11	1	4.52^0	12.16^0	20.16^0	28.53^0	39.85^0	50.16^0	63.41^0	**5.73**

The corresponding THD of output voltage for all of these modulation indexes is calculated and found to be the minimum (5.51%) at 0.9 modulation index. The HHO Algorithm takes 75 iterations to converge the solution of transcendental equations. The convergence characteristics with the number of iterations Vs objective function values (THD) are shown in figure 5.11.

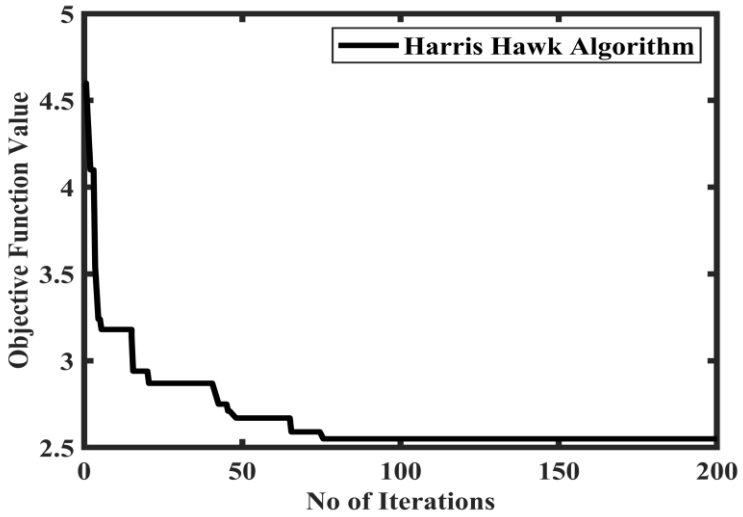


Figure 5.11 Convergence characteristics using harris hawk algorithm

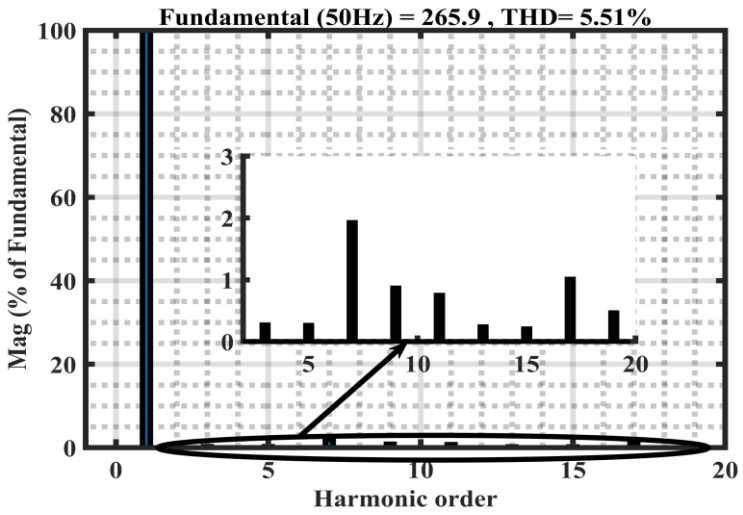


Figure 5.12 Voltage harmonic distortion using harris hawk algorithm

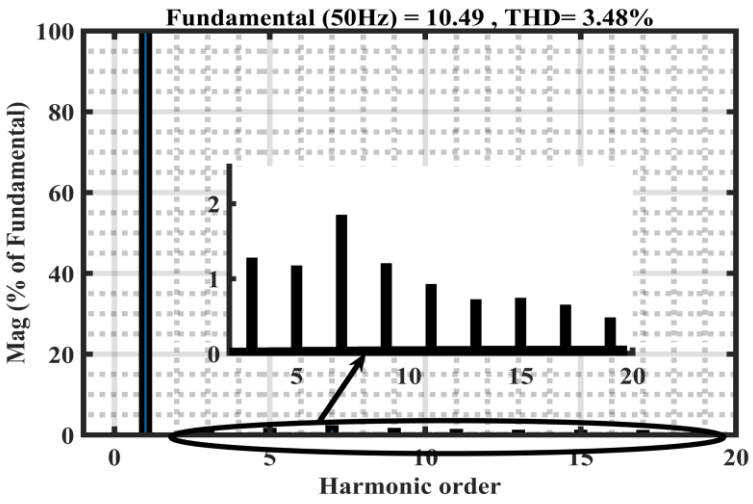


Figure 5.13 Current harmonic distortion using harris hawk algorithm

The THD of output voltage and output current of the 15-level inverter is measured with switching angles computed by the HHO algorithm at 0.9 modulation index. The THD of o/p Voltage is 5.51% at 265.9V, shown in figure 5.12 and the THD of output current is 3.48% at 10.49A, as shown in figure 5.13.

5.5 HYBRID SOFT COMPUTING ALGORITHMS TO OPTIMIZE SWITCHING ANGLES OF THE 15-LEVEL INVERTER

Wolpert and Macready's "No Free Lunch Theorem," says that no single method can address all problems optimally. As a result, research into hybrid optimization algorithms has accelerated in recent years. "Hybridization" is a method of combining the capabilities of two robust theories so that the best characteristics of each are embraced. For addressing complicated optimization problems, a hybrid method is typically considered an efficient strategy (requiring fewer evaluations) that is also more successful (finding high-quality solutions). This research assessed the following hybrid optimization algorithms to solve the nonlinear transcendental equations.

5.5.1 Switching angle optimization of 15-level inverter using EWOA algorithm

The Levy flight method and the ranking-based mutation operator are used toresolvinge the premature convergence in the whale optimization technique. A more refined approach to whale optimization may be able to strike a balance between exploration and exploitation to get the optimal global solution.

a. Levy flight strategy

In addition to extending the algorithm's search space, the Levy flight method helps to avoid premature convergence while improving global searchability. There in the whale optimization method, the Levy flying technique increases accuracy. Here's how it's calculated:

$$X(t+1) = X(t) + \mu\, sign\left[rand - \frac{1}{2}\right] \oplus Levy \qquad (5.31)$$

Where X is the position of Levy flight at time t, μ is the random number which is uniformly distributed, $sign\left[rand - \frac{1}{2}\right]$ consists of three values -1, 0, 1 and $\oplus$ is multiplication for each entry.

When the step length of the Levy flight is compared to time t, the Levy

distribution is observed to be true. Concerning Levy's flight strategy's probability density function, the following position is computed.

$$Levy\ \mu = t^{-\lambda}, \quad 1 < \lambda < 3 \tag{5.32}$$

Here λ is the power coefficient. As part of the Levy flight strategy, the Mantegna algorithm calculates the generated random step length. Here's how to figure out the position.

$$s = \frac{\mu}{|v|^{1/\beta}} \qquad \mu = N\left(0, \sigma_\mu^2\right) \qquad v = N(0, \sigma_v^2) \tag{5.33}$$

Where 's' is the step length which is a random value, β = 1.5, 'μ' and 'v' have normal distributions, σ_μ and σ_v are computed in the following manner:

$$\sigma_\mu = \left[\frac{\Gamma\,(1+\beta)\,.\sin(\frac{\pi\beta}{2})}{\beta.\ \Gamma[(1+\beta)/2]\,.2^{(\beta-1)/2}}\right]^{1/\beta} \qquad \sigma_v = 1 \tag{5.34}$$

Here Γ is the standard gamma function.

b. Ranking-based mutation operator

The objective value of each search agent is used to arrange the optimally selected search agents into a group. Each wave's objective value determines the population's ranking in ascending order (i.e., from most fit to least fit). The following formula is used to rank search agents:

$$R_i = N_p - i, \quad i = 1, 2 \ldots \ldots N_p \tag{5.35}$$

N_p is the population size. The better the search agent, the higher the ranking will be on the search. It's possible to sort search agents and determine their selection probability. Here's how to figure out P_i for the i_{th} wave.

$$P_i = \frac{R_i}{N_p}, \quad i = 1, 2 \ldots \ldots N_p \tag{5.36}$$

'DE/rand/1' is a mutation operator with a ranking-based mutation. Individuals with a higher ranking are more likely to be picked as the mutation operator's base vector or terminal vector. On the other hand, the mutation operator conveys favorable information to future generations. The ranking-based mutation operator ignores the

initial vector selection probability. This reduction may occur quickly if two of the differential vector's search steps are taken from the top-ranking vectors. As a result, the optimal global solution may be found quickly and efficiently using the enhanced whale optimization method.

Table 5.5 Switching angles with the variation of modulation index using the enhanced whale optimization algorithm

S. No	**M_i**	**α_1**	**α_2**	**α_3**	**α_4**	**α_5**	**α_6**	**α_7**	**%THD**
1	0.5	7.84^0	14.62^0	25.32^0	36.03^0	46.12^0	56.64^0	66.48^0	**8.25**
2	0.55	7.12^0	14.25^0	24.21^0	34.56^0	45.57^0	56.12^0	66.32^0	**7.84**
3	0.6	6.64^0	13.69^0	23.62^0	33.86^0	44.17^0	55.55^0	65.68^0	**7.69**
4	0.65	6.23^0	13.35^0	22.54^0	32.56^0	43.74^0	54.35^0	65.38^0	**7.31**
5	0.7	5.58^0	12.76^0	21.96^0	31.23^0	42.35^0	53.75^0	65.12^0	**6.78**
6	0.75	5.25^0	12.42^0	21.55^0	30.76^0	41.21^0	52.53^0	64.37^0	**6.52**
7	0.8	4.78^0	11.93^0	20.67^0	29.35^0	40.35^0	52.67^0	64.89^0	**5.98**
8	0.85	4.36^0	11.68^0	20.39^0	28.23^0	39.73^0	52.04^0	64.32^0	**5.76**
9	**0.9**	**4.2^0**	**11.92^0**	**19.94^0**	**28.73^0**	**39.43^0**	**51.71^0**	**63.44^0**	**5.61**
10	0.95	3.95^0	11.54^0	19.42^0	28.26^0	39.56^0	50.81^0	63.26^0	**5.69**
11	1	4.63^0	12.22^0	20.14^0	29.45^0	40.13^0	50.93^0	63.75^0	**5.81**

EWOA evaluates the SHE equations for set criteria to find the optimal switching angles of the inverter. The switching angles for modulation index for 0.5 to 1 were determined using the EWOA algorithm and tabulated in table 5.5. The EWO algorithm takes 84 iterations to converge the solution of transcendental equations. The convergence characteristics with the number of iterations Vs objective function values (THD) are shown in figure 5.14.

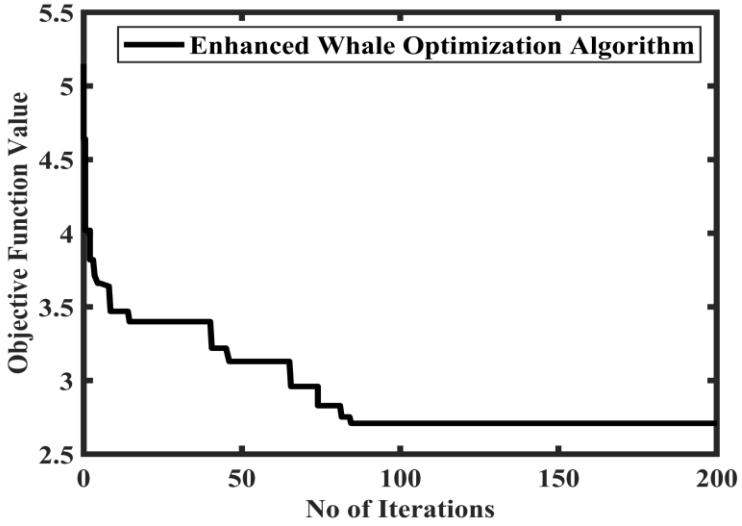


Figure 5.14 Convergence characteristics using EWO algorithm

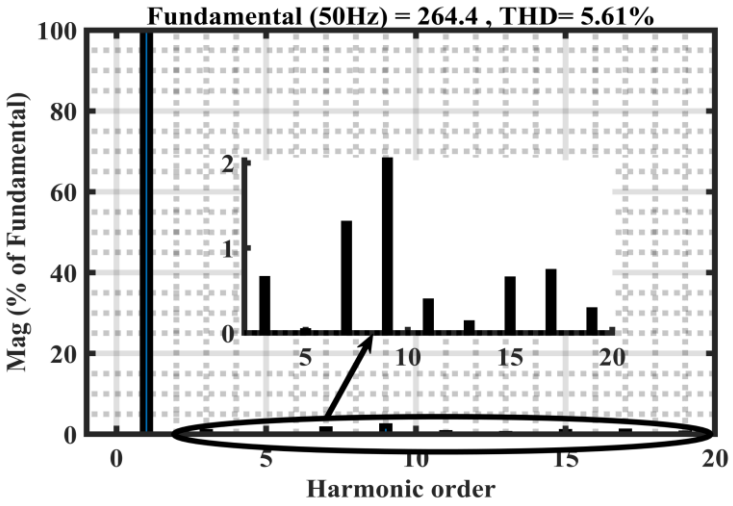


Figure 5.15 Voltage harmonic distortion using EWO algorithm

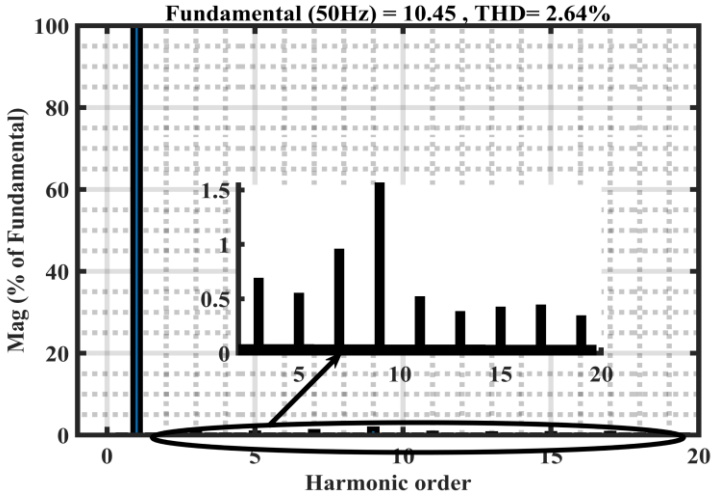


Figure 5.16 Current harmonic distortion using EWO algorithm

The total harmonic distortion (THD) of the output voltage and current of the 15-level inverter is measured using switching angles estimated by the EWO method at a modulation index of 0.9. Figure 5.15 shows that the THD of the output voltage is 5.61% at 264.4V, while the THD of output current is 2.64% at 10.45A, as shown in figure 5.16.

5.5.2 Switching angle optimization of 15-level inverter using hybrid APSO-NR algorithm

An APSO-NR optimization-based selective harmonic elimination method is used for the proposed multilevel inverter to eliminate the dominant harmonics. This approach is used for any level with equal and unequal dc inputs. To avoid local minima and broaden the search area, the particles in APSO are stacked in a ring topology. It was shown that using the NR method in conjunction with asynchronous particle updates improved convergence. Global search approach APSO and fine-tuning the best solutions using NR were utilized. The velocity and position of the particles are updated using (5.3) and (5.4), respectively.

In the suggested technique, the PSO algorithm has been applied to every particle, and then each particle instantly shares its updated objective with its nearest neighbors once the velocity and position are altered in the same iteration. The next particle determines its new location using the updated position of an adjacent particle in the same iteration, allowing for a high convergence rate. This procedure is continued until the ring's particles have been updated. In an asynchronous update, each particle in the next iteration evaluates the updated position of its neighbors, resulting in a slow convergence rate and the need for more iterations to reach global minima. NR is applied to the best particles in every iteration for local optima to generate more optimum and precise firing angles. This technique produces accurate solutions and allows for more optimal and exact firing angles. The Jacobian matrix for NR is computed using (5.37) and $d\alpha^m$ is computed using (5.38).

$$\left[\frac{df}{d\alpha}\right]^m = \begin{bmatrix} \frac{df_1}{d\alpha_1} & \frac{df_1}{d\alpha_2} & \cdots & \frac{df_1}{d\alpha_n} \\ \frac{df_2}{d\alpha_1} & \frac{df_2}{d\alpha_2} & \cdots & \frac{df_2}{d\alpha_n} \\ \frac{df_n}{d\alpha_1} & \frac{df_n}{d\alpha_2} & \cdots & \frac{df_n}{d\alpha_n} \end{bmatrix} \tag{5.37}$$

$$d\alpha^m = INV\left[\frac{df}{d\alpha}\right]^m [T' - f(\alpha^m)] \tag{5.38}$$

Where T is the target vector and

$f(\alpha^m)$ is the function of the nonlinear equations.

$$\left[\frac{df}{d\alpha}\right]^m = \begin{bmatrix} \frac{df_1}{d\alpha_1} & \frac{df_1}{d\alpha_2} & \frac{df_1}{d\alpha_3} & \frac{df_1}{d\alpha_4} & \frac{df_1}{d\alpha_5} & \frac{df_1}{d\alpha_6} & \frac{df_1}{d\alpha_7} \\ \frac{df_2}{d\alpha_1} & \frac{df_2}{d\alpha_2} & \frac{df_2}{d\alpha_2} & \frac{df_2}{d\alpha_2} & \frac{df_2}{d\alpha_2} & \frac{df_2}{d\alpha_2} & \frac{df_2}{d\alpha_2} \\ \frac{df_3}{d\alpha_1} & \frac{df_3}{d\alpha_2} & \frac{df_3}{d\alpha_3} & \frac{df_3}{d\alpha_4} & \frac{df_3}{d\alpha_5} & \frac{df_3}{d\alpha_6} & \frac{df_3}{d\alpha_7} \\ \frac{df_4}{d\alpha_1} & \frac{df_4}{d\alpha_2} & \frac{df_4}{d\alpha_3} & \frac{df_4}{d\alpha_4} & \frac{df_4}{d\alpha_5} & \frac{df_4}{d\alpha_6} & \frac{df_4}{d\alpha_7} \\ \frac{df_5}{d\alpha_1} & \frac{df_5}{d\alpha_2} & \frac{df_5}{d\alpha_3} & \frac{df_5}{d\alpha_4} & \frac{df_5}{d\alpha_5} & \frac{df_5}{d\alpha_6} & \frac{df_5}{d\alpha_7} \\ \frac{df_6}{d\alpha_1} & \frac{df_6}{d\alpha_2} & \frac{df_6}{d\alpha_3} & \frac{df_6}{d\alpha_4} & \frac{df_6}{d\alpha_5} & \frac{df_6}{d\alpha_6} & \frac{df_6}{d\alpha_7} \\ \frac{df_7}{d\alpha_1} & \frac{df_7}{d\alpha_2} & \frac{df_7}{d\alpha_3} & \frac{df_7}{d\alpha_4} & \frac{df_7}{d\alpha_5} & \frac{df_7}{d\alpha_6} & \frac{df_7}{d\alpha_7} \end{bmatrix} \tag{5.39}$$

While the determinant of the matrix approaches' 0' or the switching angles remains the same, the traditional method of inverting the Jacobian matrix might result in numerical errors. To get around this, the LU decomposition technique is used to construct the inverse of the Jacobian matrix. In this section, a fifteen-level inverse Jacobian matrix is derived, and the Jacobian matrix is provided in equation (5.39).

After determining the angles from $d\alpha^m$ using equation (5.38), the updated switching angles can be determined using equation (5.40).

$$\alpha^{m+1} = \alpha^m + d\alpha^m \tag{5.40}$$

NR is used to find the local minima close to the best particles for each best-selected individual. A previous best solution is used if a local minimum is found after applying NR around the chosen particle; otherwise, the technique keeps the original best values. When the angle difference is less than ε or counter IterN reaches IterNmax, the refining step ends. The revised solutions will be included in the population in the subsequent group. When the counter IterP reaches IterPmax, the program ends. A particle with the lowest objective value will be recorded as an optimum solution. All load circumstances are taken into consideration while computing and storing the firing

angles for each modulation index in memory as a lookup table in offline mode. Based on the modulation index or changing load parameters, these angles are fetched from memory in real-time.

Table 5.6 Switching angles with the variation of modulation index using hybrid APSO-NR algorithm

S. No	M_i	α_1	α_2	α_3	α_4	α_5	α_6	α_7	%THD
1	0.5	6.92^0	15.65^0	25.45^0	34.22^0	42.36^0	55.36^0	66.72^0	**7.65**
2	0.55	6.64^0	15.53^0	24.36^0	33.49^0	41.62^0	54.25^0	66.47^0	**7.35**
3	0.6	6.02^0	14.69^0	23.74^0	32.58^0	40.23^0	53.54^0	65.68^0	**6.87**
4	0.65	5.56^0	13.85^0	22.36^0	31.36^0	39.46^0	52.45^0	65.13^0	**6.35**
5	0.7	4.75^0	13.45^0	21.12^0	30.62^0	38.55^0	51.36^0	64.68^0	**6.02**
6	0.75	4.25^0	12.65^0	21.65^0	29.45^0	37.21^0	50.65^0	64.27^0	**5.78**
7	0.8	3.76^0	12.93^0	20.55^0	28.35^0	36.32^0	49.38^0	63.56^0	**5.63**
8	0.85	3.45^0	12.54^0	20.32^0	27.68^0	35.73^0	48.04^0	63.25^0	**5.45**
9	**0.9**	$\mathbf{3.71^0}$	$\mathbf{12.31^0}$	$\mathbf{20.40^0}$	$\mathbf{27.23^0}$	$\mathbf{35.63^0}$	$\mathbf{47.75^0}$	$\mathbf{62.34^0}$	**5.41**
10	0.95	3.62^0	11.75^0	19.35^0	26.69^0	35.56^0	48.21^0	62.26^0	**5.48**
11	1	3.95^0	12.36^0	20.36^0	27.43^0	36.51^0	49.06^0	63.03^0	**5.76**

The switching angles for modulation index for 0.5 to 1 were determined using a hybrid APSO-NR algorithm and tabulated in table 5.6. The corresponding THD of output voltage for all of these modulation indexes is also calculated and found to be the minimum (5.41%) at 0.9 modulation index. The hybrid APSO-NR Algorithm takes 65 iterations to converge the solution of transcendental equations. The convergence characteristics with the number of iterations Vs objective function values (THD) are shown in figure 5.17.

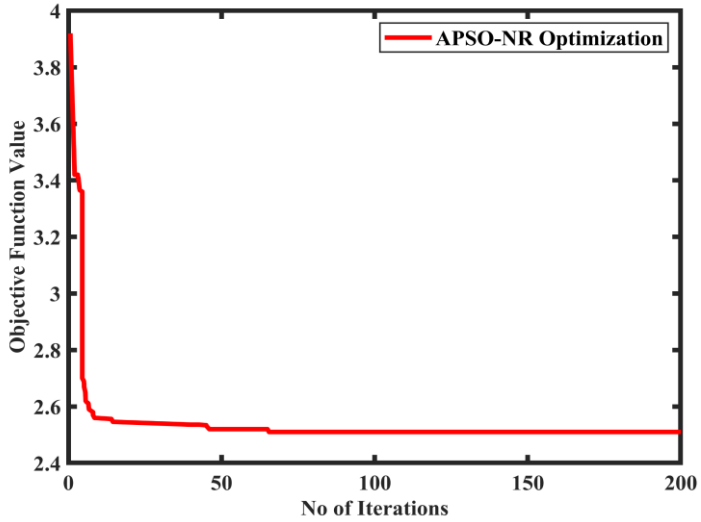


Figure 5.17 Convergence characteristics using APSO-NR algorithm

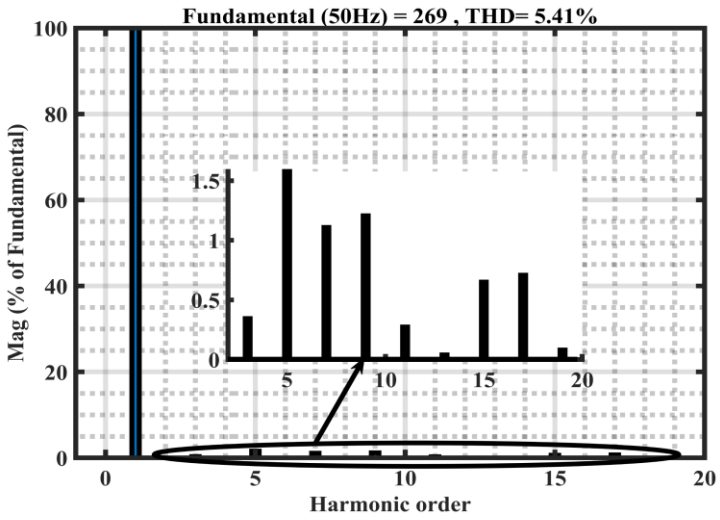


Figure 5.18 Voltage harmonic distortion using APSO-NR algorithm

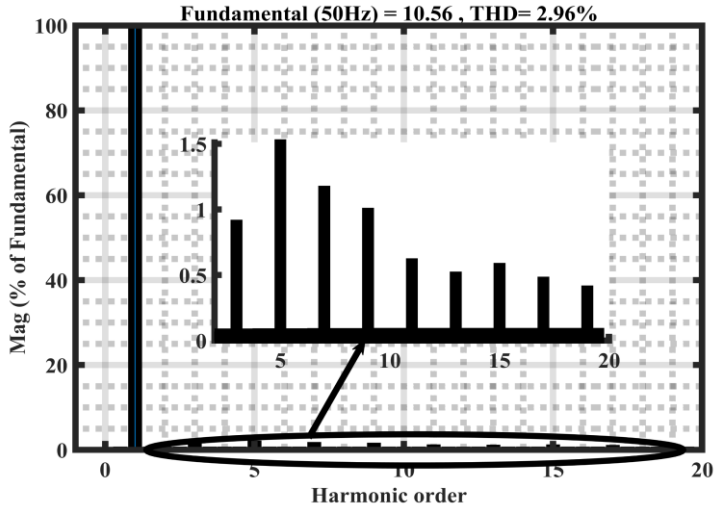


Figure 5.19 Current harmonic distortion using APSO-NR algorithm

Switching angles calculated by the hybrid APSO-NR method at 0.9 modulation index are used to assess the THD of the 15-level inverter's output voltage and current. The o/p THD Figure 5.18 shows the voltage at 54.1% and the THD of the output current at 10.56 A at 2.96%, respectively.

5.5.3 Switching angle optimization of 15-level inverter using hybrid PSO-GA algorithm

A hybrid approach is proposed, which combines a genetic algorithm (GA) with PSO. This hybrid algorithm combines GA and PSO principles and produces individuals through the GA crossover and mutations and PSO processes in the new generation. It can solve the local minima of the PSO and have greater search accuracy.

The Algorithm of GA-PSO with combined accuracy is given below:

Step-1: Initialization of variables for GA

Step-2: Initialization of variables for PSO

Step-3: Determine the best GA solution coefficient for each PSO condition.

Step-4: Impose GA's optimal location condition and perform GA mutations and crossover.

Step-5: When the best candidate in GA or PSO has satisfied the termination criteria, choose the best solution and cease.

Step-6: The reproduction process is halted if the PSO's condition is satisfied (target value or iteration number). If this is not the case, we'll go on to step 3.

Step-7: If generations could be exactly separated by iterative items N, then use a hybrid approach. Pick P individuals at random from each subsystem based on their objective.

To get the switching angles of the proposed 15-level inverter, the SHEPWM transcendental equations are solved using a hybrid PSO-GA optimization approach, which is a combination of PSO and GA. It is necessary to compute and store the switching angles for each modulation index in a lookup table that covers all possible load circumstances in offline mode. These angles are retrieved from memory in real-time in response to changes in the modulation index or the load parameter values being used. The switching angles for modulation index for 0.5 to 1 were determined using hybrid PSO-GA and tabulated in table 5.7.

Table 5.7 Switching angles with the variation of modulation index using PSO-GA algorithm

S. No	M_i	α_1	α_2	α_3	α_4	α_5	α_6	α_7	%THD
1	0.5	5.12^0	13.61^0	22.62^0	34.42^0	46.32^0	57.82^0	65.46^0	**8.86**
2	0.55	5.22^0	12.36^0	23.91^0	35.34^0	45.92^0	56.87^0	63.82^0	**8.32**
3	0.6	5.13^0	11.76^0	23.36^0	37.54^0	44.98^0	55.77^0	62.87^0	**7.69**
4	0.65	4.96^0	11.43^0	21.89^0	36.87^0	44.32^0	54.37^0	63.75^0	**7.42**
5	0.7	4.76^0	11.34^0	21.35^0	35.61^0	44.24^0	53.42^0	62.33^0	**7.13**
6	0.75	4.43^0	12.04^0	21.67^0	36.46^0	42.26^0	54.75^0	63.43^0	**6.65**
7	0.8	4.51^0	12.35^0	21.32^0	35.12^0	43.43^0	55.71^0	64.71^0	**6.23**
8	0.85	4.21^0	12.37^0	21.47^0	34.27^0	44.32^0	53.84^0	63.67^0	**5.71**
9	**0.9**	$\mathbf{4.01^0}$	$\mathbf{12.11^0}$	$\mathbf{20.32^0}$	$\mathbf{29.06^0}$	$\mathbf{38.62^0}$	$\mathbf{49.74^0}$	$\mathbf{64.32^0}$	**5.34**
10	0.95	4.29^0	12.78^0	22.36^0	34.81^0	45.78^0	53.68^0	64.39^0	**5.92**
11	1	4.59^0	12.43^0	22.54^0	33.45^0	44.57^0	54.43^0	64.89^0	**6.24**

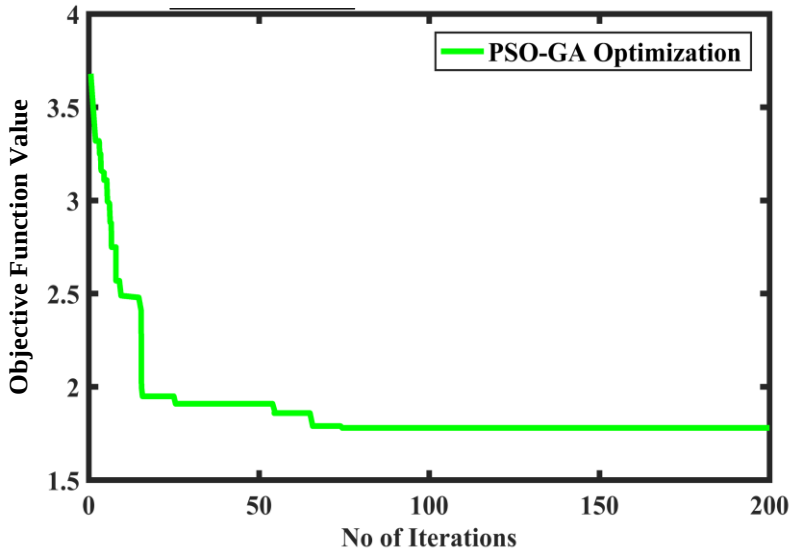


Figure 5.20 Convergence characteristics using PSO-GA algorithm

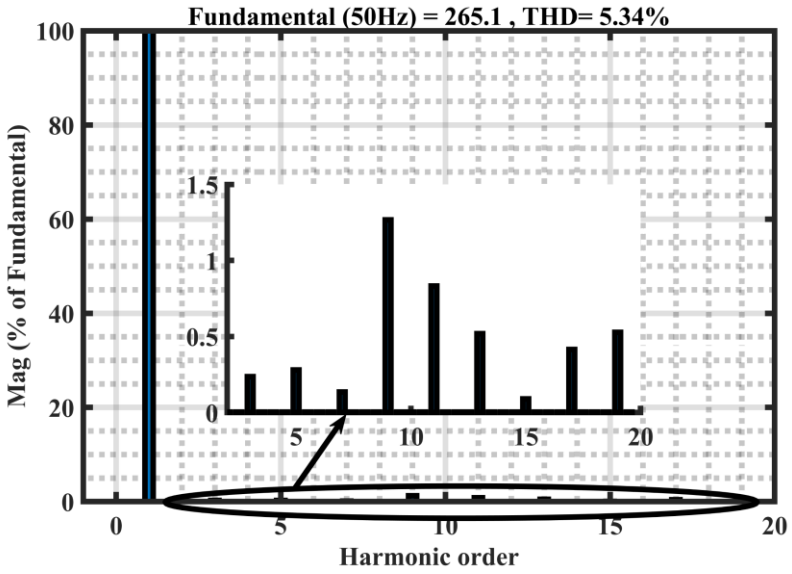


Figure 5.21 Voltage harmonic distortion using PSO-GA algorithm

The Hybrid PSO-GA Algorithm takes 74 iterations to converge the solution of transcendental equations. The corresponding THD of output voltage for all of these modulation indexes is calculated and found to be the minimum (5.34%) at 0.9 modulation index. The convergence characteristics with the number of iterations Vs objective function values (THD) are presented in figure 5.20.

The THD of output voltage and output current of the 15-level inverter is measured with switching angles computed by Hybrid PSO-GA at 0.9 modulation index. The THD of o/p Voltage is 5.34% at 265.1V, as shown in figure 5.21, and the THD of output current is 2.66% at 10.45A, as shown in figure 5.22.

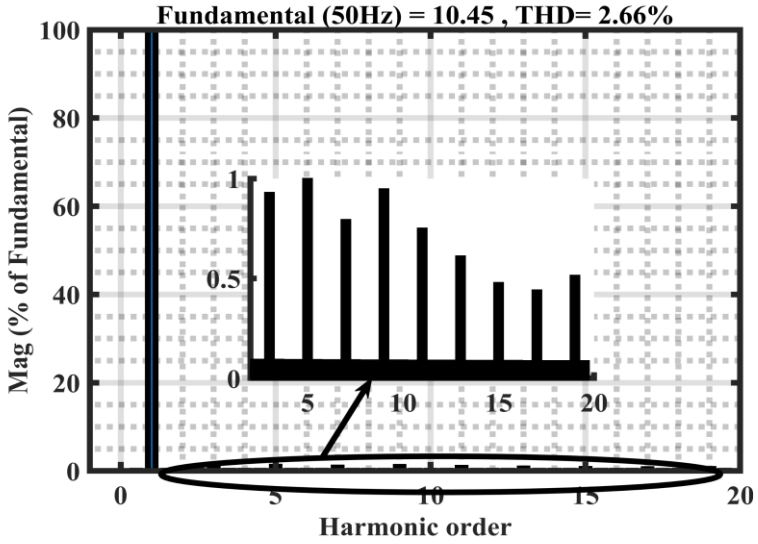


Figure 5.22 Current harmonic distortion using PSO-GA algorithm

5.5.4 Switching angle optimization of 15-level inverter using hybrid HH-DE algorithm

Using its keen vision, a Harris' Hawk searches for and locates its prey (rabbits, etc.) in a hunting environment, as indicated in the study's solution point. It's important to remember that this isn't always true. So the Harris' Hawk will spend many minutes or even hours observing, tracking, and following its prey before deciding on whether or not to pursue it. In this procedure's Exploration Phase, DE mutation operators are used. Starting from a random position, each Hawk waits for prey depending on the following two circumstances. In the situation $q < 0.5$, the Hawk perches according to its prey (rabbit) position, and in the scenario $q \geq 0.5$, the Hawk perches according to the position of other Hawks in the hunting area. The five mutation operators of DE are used to calculate X (t + 1), HH-DE structure when $q \geq 0.5$. As a result, HH-DE maintains a population space shared by both HHO and DE to maximize efficiency. There is a benefit to using differential evolution (DE) optimization for local search in that it increases the population's variety during the process of local search.

In the exploration phase for $|E| \geq 1$ and $q \geq 0.5$, there are five possible mutation operators of DE when calculating X (t + 1). The selective harmonic elimination problem is evaluated using five mutation operators independently in this study. By then, it will only be necessary to arbitrarily apply one of these mutation operators of DE to calculate X (t + 1).

The hybrid HH-DE algorithm is used to update the switching angles of the proposed 15-level inverter for each iteration. The Hybrid HH-DE Algorithm takes 40 iterations to converge the solution of transcendental equations. The convergence characteristics with the number of iterations Vs objective function values (THD) are shown in figure 5.23. The switching angles computed for various modulation index is presented in table 5.8.

The total harmonic distortion (THD) of the output voltage and output current of the 15-level inverter is measured using switching angles estimated by the hybrid HH-DE method at 0.9 modulation index. The THD of the output voltage is 5.33% at 267.6V, as shown in figure 5.24, and the THD of output current is 2.78% at 10.52A, as shown in figure 5.25.

Table 5.8 Switching angles with the variation of modulation index using HH-DE algorithm

S. No	M_i	α_1	α_2	α_3	α_4	α_5	α_6	α_7	%THD
1	0.5	6.11^0	14.51^0	23.56^0	35.91^0	45.36^0	56.32^0	65.86^0	**7.42**
2	0.55	5.45^0	14.36^0	23.45^0	35.68^0	44.25^0	55.57^0	65.62^0	**7.16**
3	0.6	5.13^0	13.76^0	23.34^0	34.46^0	43.65^0	54.35^0	65.17^0	**6.89**
4	0.65	5.37^0	13.25^0	22.68^0	32.35^0	42.35^0	53.48^0	64.75^0	**6.61**
5	0.7	5.37^0	13.21^0	22.35^0	32.61^0	41.34^0	52.35^0	64.67^0	**6.34**
6	0.75	5.43^0	12.67^0	21.89^0	32.75^0	40.22^0	51.65^0	64.23^0	**5.92**
7	0.8	4.75^0	12.42^0	21.56^0	31.25^0	39.43^0	50.71^0	63.79^0	**5.68**
8	0.85	4.35^0	12.65^0	21.12^0	30.32^0	38.32^0	49.84^0	63.45^0	**5.43**
9	**0.9**	$\mathbf{3.91^0}$	$\mathbf{12.22^0}$	$\mathbf{20.60^0}$	$\mathbf{29.40^0}$	$\mathbf{37.05^0}$	$\mathbf{48.70^0}$	$\mathbf{63.10^0}$	**5.33**
10	0.95	4.12^0	12.15^0	21.16^0	30.81^0	37.78^0	47.68^0	62.39^0	**5.43**
11	1	4.32^0	12.35^0	21.44^0	31.45^0	38.57^0	48.43^0	62.76^0	**5.49**

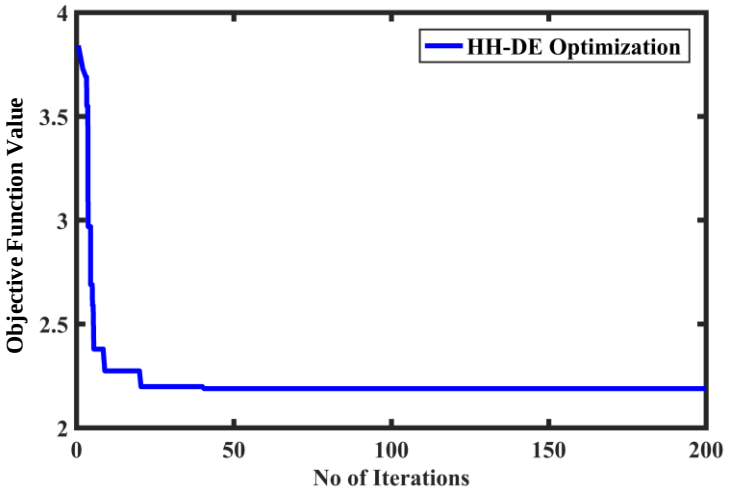


Figure 5.23 Convergence characteristics using HH-DE algorithm

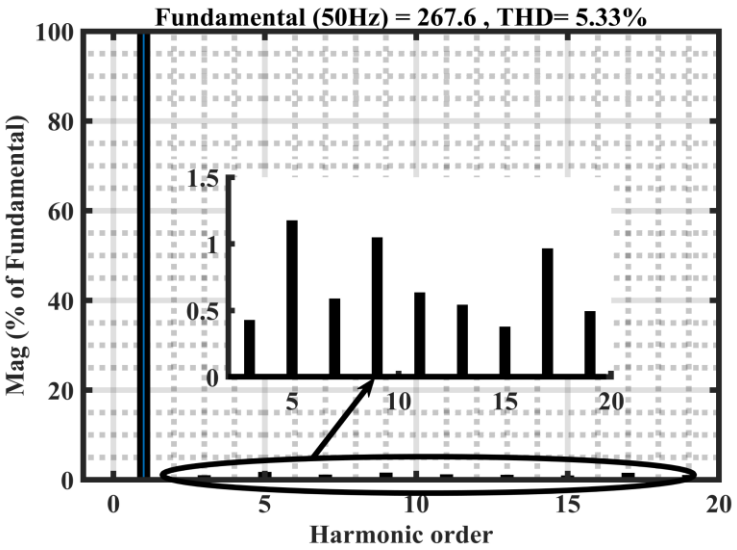


Figure 5.24 Voltage harmonic distortion using HH-DE algorithm

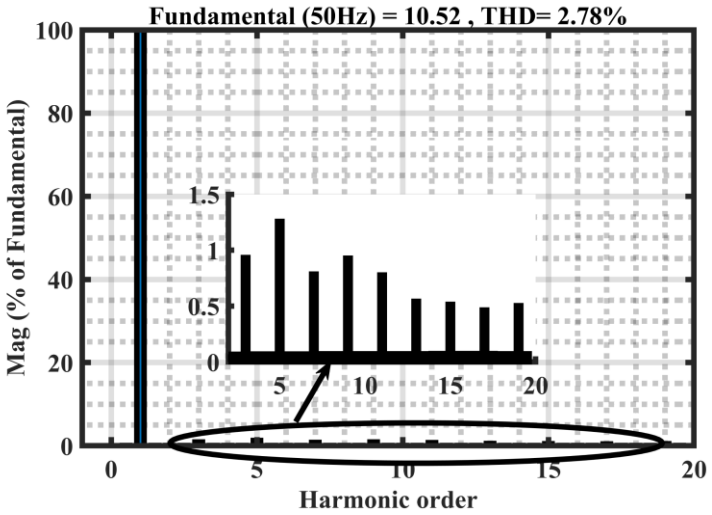


Figure 5.25 Current harmonic distortion using HH-DE algorithm

5.6 COMPARATIVE ANALYSIS OF THD USING SOFT COMPUTING ALGORITHMS

The optimal switching angles derived from different optimization algorithms at 0.9 modulation index (convergence region) and the corresponding THDs of output voltage and currents are tabulated in table 5.9. From table 5.10, it is confirmed that the hybrid PSO-GA & hybrid HH-DE algorithms are responsible for giving the best solution (%THD) at the minimum number of iterations (75-iterations & 40-iterations, respectively) compared to other algorithms. Also, the THD analysis was considered at both Nyquist frequencies (generally 5 kHz) and at Harmonic frequency (considered for 1 kHz for eliminating up to 19th harmonic). The measured THDs are 5.34% using PSO-

GA optimization and 5.33% using HH-DE optimization, approximately the same at Nyquist frequency. The THDs measured are 1.78% using PSO-GA optimization and 2.18% using HH-DE optimization at the harmonic frequency.

Table 5.9 Optimal switching angles and corresponding THD resulted from different optimization algorithms for 15-level multilevel inverter at 0.9 modulation index

Algorithm	α_1	α_2	α_3	α_4	α_5	α_6	α_7	THD_V	THD_i
GA	5.6^0	10.9^0	18.6^0	26.5^0	34.8^0	44.6^0	61.2^0	6.25%	4.17%
PSO	3.9^0	12.1^0	20.9^0	29.9^0	38.1^0	48.7^0	61.1^0	5.74%	3.31%
WOA	4.3^0	11.89^0	20.6^0	28.6^0	40.6^0	48.5^0	63.6^0	5.73%	2.98%
HHA	3.9^0	11.4^0	19.5^0	28.9^0	39.2^0	50.5^0	62.6^0	5.51%	3.48%
EWOA	4.2^0	11.9^0	19.9^0	28.7^0	39.4^0	51.7^0	63.4^0	5.61%	2.64%
APSO-NR	3.7^0	12.3^0	20.4^0	27.2^0	35.6^0	47.7^0	62.3^0	5.41%	2.96%
PSO-GA	4^0	12^0	20.3^0	29^0	38.6^0	49.7^0	64.3^0	5.34%	2.66%
HH-DE	3.9^0	12.2^0	20.6^0	29.4^0	37^0	48.7^0	63.1^0	5.33%	2.78%

Table 5.10 Performance analysis of proposed inverter with different optimization algorithms

Algorithm	No of Iterations	% (THD)v	% (THD)i	% (THD)v	% (THD)i	V_{PEAK} (V)	V_{RMS} (V)	I_{PEAK} (A)	I_{RMS} (A)
		At Nyquist Frequency		At max Frequency (1kHz)					
GA	103	6.25	4.17	4.21	3.95	259.0	194.8	9.65	7.18
PSO	114	5.74	3.31	3.12	3.02	259.0	189.4	9.65	7.08
WOA	109	5.73	2.98	3.24	2.68	259.0	188.0	9.65	6.96
HHA	75	5.51	3.48	2.55	3.16	259.0	189.0	9.65	6.96
EWOA	84	5.61	2.64	2.71	2.23	259.0	187.0	9.65	6.93
APSO-NR	65	5.41	2.96	2.51	2.62	259.0	190.3	9.65	7.01
PSO-GA	74	5.34	2.66	1.78	2.25	259.0	187.6	9.65	6.94
HH-DE	40	5.33	2.78	2.19	2.39	259.0	189.4	9.65	6.98

Therefore this analysis concludes that the performance of these two algorithms are the same at Nyquist frequency, and PSO-GA optimization performance is better than HH-DE optimization at harmonic frequency, as it gives less harmonic distortion of 1.78%. Similarly, the current harmonic distortion is presented in table 5.10, where EWOA optimization gives low current harmonic distortion over other optimizations, as 2.5% at Nyquist frequency and 2.11% at Harmonic frequency at 65 iterations.

Table 5.11 Magnitudes of harmonic voltages

Algorithm	H3	H5	H7	H9	H11	H13	H15	H17	H19
GA	3.25	1.26	0.00	1.11	0.71	0.58	1.48	0.15	1.14
PSO	0.69	2.42	1.04	0.61	0.99	0.37	0.76	0.48	0.01
WOA	0.58	0.81	1.70	0.97	0.47	1.00	0.53	1.75	1.06
HHA	0.27	0.26	1.93	0.86	0.75	0.24	0.21	1.01	0.47
EWOA	0.64	0.02	1.29	2.03	0.38	0.12	0.63	0.72	0.27
APSO-NR	0.34	1.58	1.11	1.21	0.27	0.04	0.65	0.71	0.08
PSO-GA	0.24	0.28	0.14	1.27	0.83	0.52	0.09	0.42	0.53
HH-DE	0.41	0.57	0.57	1.03	0.61	0.52	0.36	0.94	0.48

The comparison of the magnitude of different harmonic voltages from 3^{rd} harmonic to 19^{th} harmonics is presented in table 5.11 and figure 5.26. Lower dominant harmonics such as 3^{rd}, $5^{th,}$ and 7^{th} harmonics are optimized to very low values about 0.24, 0.28, and 0.14, respectively, using a hybrid PSO-GA algorithm compared to other algorithms. Hence, the hybrid PSO-GA optimizer gives superior performance compared to other optimizers proposed in this research, while analyzing voltage harmonics in the 15-level inverter for the feasible solution since it gives the THD of 5.34% at Nyquist 1.78% at the harmonic frequency. Later the HH-DE optimizer gives the 3^{rd}, $5^{th,}$ and 7^{th} harmonic voltages less than 1%., i.e., 0.41%, 0.57% and 0.57% respectively. Also, the EWOA optimizer reduces the 5^{th} harmonic to 0.02%, which is almost negligible.

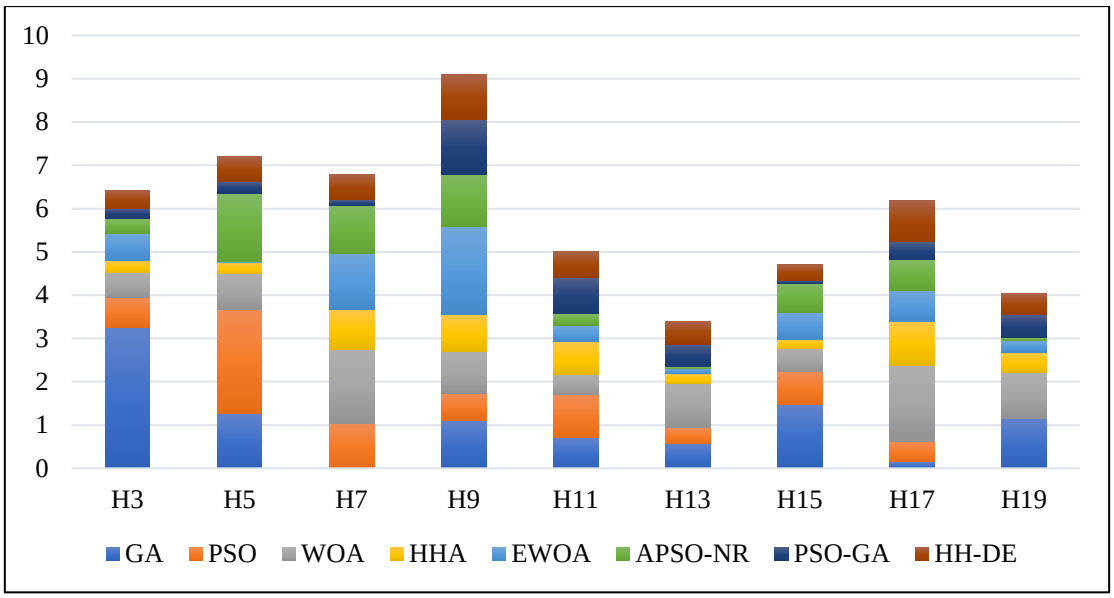


Figure 5.26 Comparison of voltage harmonics with different optimizations

Table 5.12 Magnitudes of harmonic currents

Algorithm	H3	H5	H7	H9	H11	H13	H15	H17	H19
GA	3.03	1.6	0.78	1.03	0.66	0.71	0.84	0.44	0.49
PSO	1.05	2.01	1.28	0.87	0.68	0.53	0.61	0.42	0.36
WOA	0.94	1.12	1.25	0.86	0.58	0.82	0.52	0.86	0.68
HHA	1.25	1.14	1.82	1.17	0.89	0.69	0.71	0.62	0.45
EWOA	0.67	0.53	0.94	1.55	0.5	0.37	0.41	0.42	0.33
APSO-NR	0.9	1.51	1.16	0.99	0.6	0.5	0.57	0.46	0.4
PSO-GA	0.92	0.99	0.78	0.94	0.74	0.6	0.47	0.43	0.5
HH-DE	0.93	1.26	0.79	0.93	0.78	0.54	0.51	0.47	0.5

The magnitude of current harmonics from 3rd harmonic to 19th harmonics are presented in table 5.12 and figure 5.27. Lower dominant harmonics such as 3rd, 5^{th,} and 7th harmonics are optimized to very low values about 0.67, 0.53, and 0.94, respectively, using an enhanced whale optimization algorithm compared to other algorithms. Hence, the Enhanced whale optimizer is the better choice for the proposed multilevel inverter for a feasible solution while considering the current harmonics are the parameters in

the analysis since it gives the THD of 2.5% at Nyquist frequency and 2.11% at the harmonic frequency.

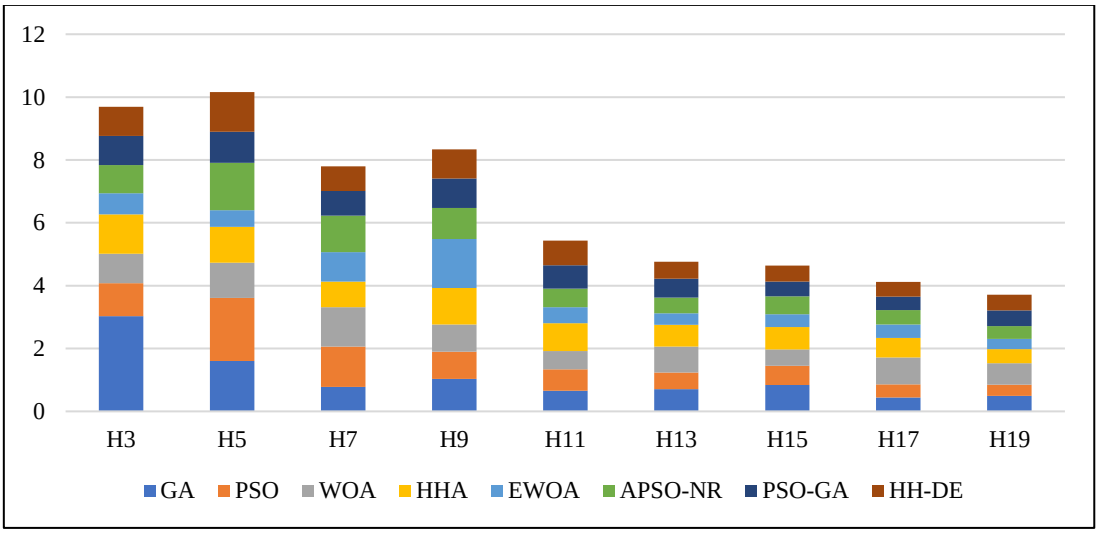


Figure 5.27 Comparison of current harmonics with different optimizations

5.7 CHAPTER SUMMARY

This chapter demonstrated the application of traditional and hybrid optimization algorithms on the proposed asymmetric multilevel inverter most suited for solar PV applications. A selective harmonic elimination-based pulse width modulation (SHEPWM) had been implemented using four traditional algorithms: GA, PSO, WOA, and HHO. Further, the hybridization of these algorithms, such as EWOA, APSO-NR, PSO-GA, and HH-DE, were implemented for SHEPWM. The optimization algorithms optimized the switching angles of the proposed topology to optimize the THD of output voltage and current. The THD obtained from these algorithms was comparatively low as per IEEE-519 standard without employing any filter at the output of the inverter. The proposed inverter performed satisfactorily with a low THD of 5.34% at Nyquist frequency and 1.78% at the harmonic frequency with hybrid PSO-GA optimization compared to other optimizations. Also, the current THD obtained 2.5% at Nyquist frequency and 2.11% at the harmonic frequency with EWOA optimization. As per the IEEE-519 standard, the converter with THD below 5% is recommended for power system applications. As a result, according to IEEE-519 standards, the performance of the proposed inverter was satisfactory without using any filter in terms of voltage and current THD.

CHAPTER-6

GRID INTEGRATION OF ASYMMETRIC 15-LEVEL INVERTER

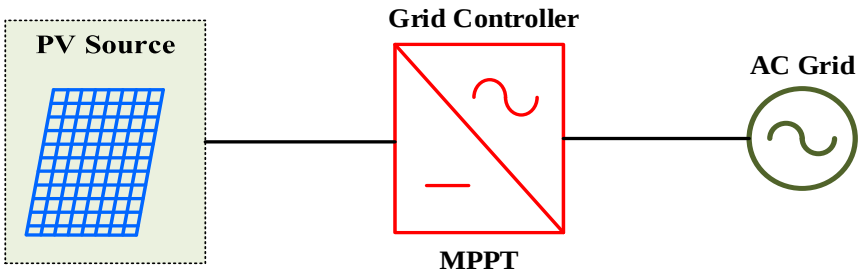
6.1 INTRODUCTION

Solar photovoltaic (SPV)-based standalone inverters have been more popular in low and medium power applications over the past several years. Photovoltaic systems have become more important in our everyday lives in the twenty-first century. Due to temperature or irradiation changes, the output voltage of a PV system produces large ripples and is often variable power output. This chapter describes the integration of an asymmetric 15-level inverter with a grid-connected solar PV system. A grid-connected SPV system is modelled and simulated using an asymmetric 15-level inverter. The 15-level inverter's dc sources are replaced with PV sources. The results are analyzed with different operating temperatures and solar irradiance conditions. The GCSPV system is controlled by a closed-loop control system using PSO, HHO, hybrid PSO-GA based PI controllers. The grid voltage, grid current, active, reactive power and THD of grid currents are measured. Finally, the performance of the 15-level asymmetric inverter is analyzed by comparing the THD of the grid current.

6.2 METHODS OF GRID INTEGRATION OF PV SYSTEMS

The inverter system is a primary component in the grid-connected PV system. The inverters are employed in the GCSPV system for power conversion, control and synchronization. Further, the synchronization of PV power to the grid and its control under a steady state is a significant concern. Hence, the inverter's output is required to maintain near sinusoidal for proper synchronization to the grid. In addition to that, the input supplied to the grid should have lower THD for the faster dynamic response. To extract maximum power from the PV system and pump sinusoidal current into the grid in GCSPV systems, an interconnection between the PV system and the grid is necessary. To achieve this, three different grid integration methods are majorly is being in use [167]. The figure shown in 6.1 represents these three types of configurations.

The inverter acts as a power conditioning unit in single-stage grid integration and has a controlled power flow between the SPV system and the grid. In this, the conversion efficiency is low since it depends on temperature, irradiation and isolation.



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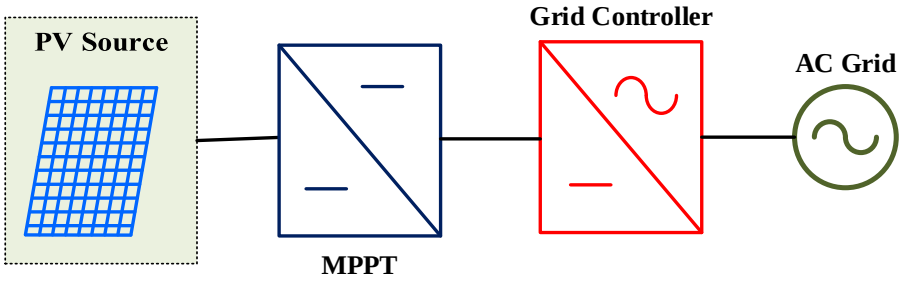

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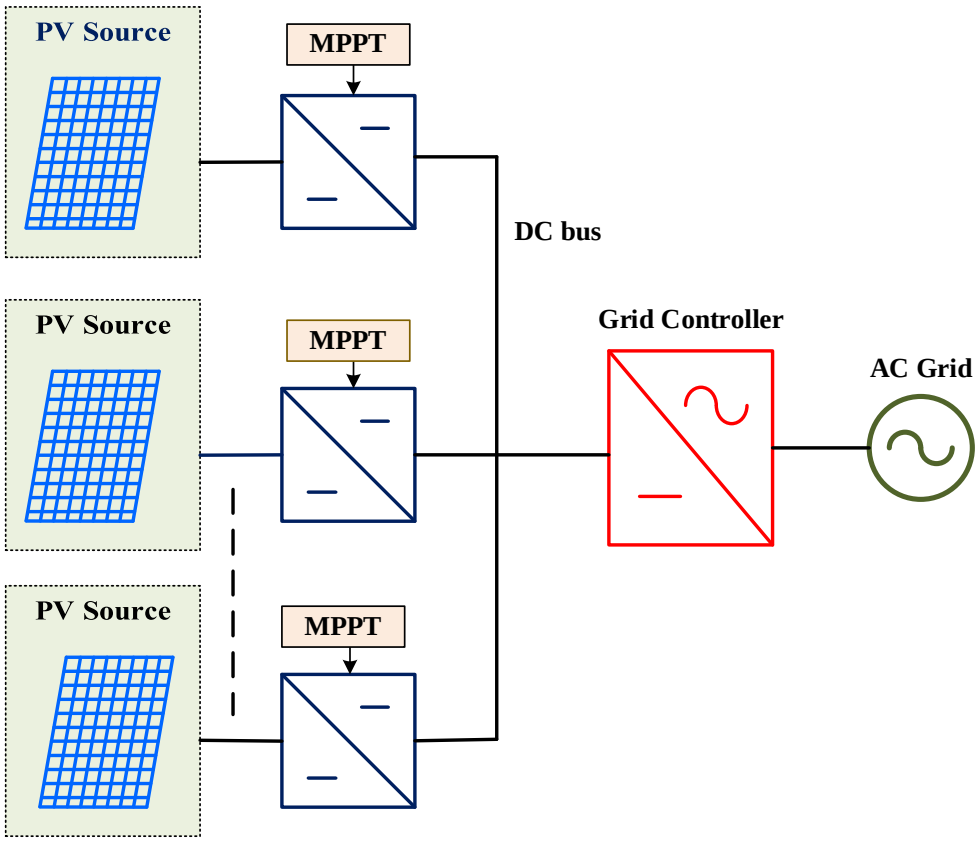


(c)

Figure 6.1 Types of grid integration of SPV systems

(a) Single-stage (b) Two-stage (c) Multistage with dc bus

The two-stage arrangement includes dc-dc (boost converter) and dc-ac converters (inverter). A dc-link capacitor connects the boost converter and inverter. The dc-link capacitor can be flexibly designed for the required voltages. The two-stage grid-connected SPV system is usually employed for domestic applications like DGs.

The multi-stage configuration is employed explicitly for high power applications. It consists of a dc-dc converter, dc-ac inverter and a dc bus. The power extracted from the PV sources are fed onto the dc bus, and the input power to the inverter is from this dc bus.

6.3 POWER FLOW IN A SINGLE-PHASE GRID-CONNECTED SPV SYSTEM

Single-phase SPV systems are generally implemented for low power applications of the range of a few kilowatts with maximum power point tracking at unity power factor [168]. The SPV system pumps the power into the grid when the output power exceeds the load demand. Power produced by the grid-connected SPV system or the grid's demand determines the active power flow in the SPV system. Figure 6.2 shows the power flow diagram between the SPV system and grid when the unity power factor is required at the grid side for low and medium power applications.

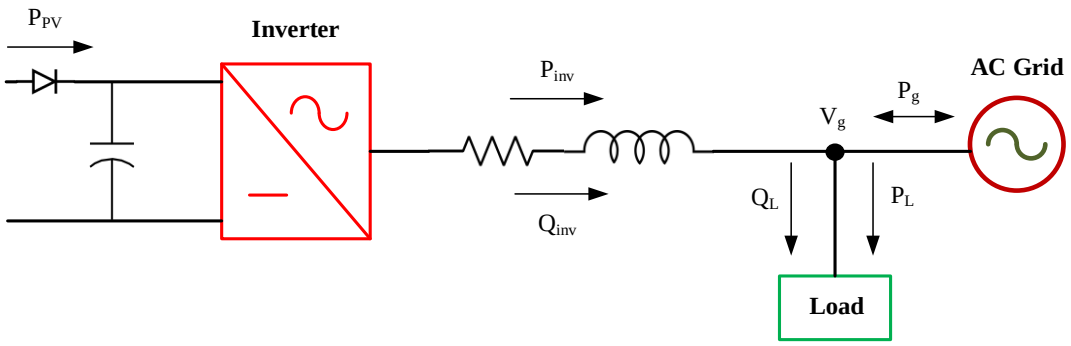


Figure 6.2 Power flow diagram for single-phase grid-connected SPV system

In figure 6.2, the P_{PV} is the active power generated from the PV sources, P_{inv} is the active power output of the inverter, Q_{inv} is the reactive power output of the inverter, V_g is the grid voltage, P_g is the active power of the grid, P_L is the active power supplied to the load, and Q_L is the reactive power supplied to the load. Considering the d-q reference frame, a single-phase grid-connected inverter's total active and reactive power can be written in equations (6.1) and (6.2).

$$P_g = \frac{1}{2}\left(V_{gd}I_d + V_{gq}I_q\right) \quad (6.1)$$

$$Q_g = \frac{1}{2}\left(V_{gd}I_q - V_{gq}I_d\right) \quad (6.2)$$

Where, V_{gd} & V_{gq} are the direct axis and quadrature axis voltages of the grid, respectively and I_d & I_q are the direct axis and quadrature axis currents of the inverter, respectively. The quadrature axis voltage of the grid becomes zero due to the zero averaged sinusoid of the grid voltage waveform with less harmonic content. Therefore, the equations (6.1) and (6.2) can be rewritten as follows;

$$P_g = \frac{1}{2}\left(V_{gd}I_d\right) \quad (6.3)$$

$$Q_g = \frac{1}{2}\left(V_{gd}I_q\right) \quad (6.4)$$

Assuming the inverter is lossless (ideal case), neglecting the power losses on the filter inductance and losses on the dc-dc converter, the steady-state power produced by the PV sources is equal to the active power of the grid. Therefore the equation (6.3) can be rewritten as follows;

$$P_{PV} = \frac{1}{2}\left(V_{gd}I_d\right) \quad (6.5)$$

$$V_{PV} * I_{PV} = \frac{1}{2}\left(V_{gd}I_d\right) \quad (6.6)$$

But, practically, the relation in equation (6.5) is not possible since the power switches used in the power converters include some losses during their operation. Therefore, the active power of the grid is always less than the PV power.

6.4 PROPOSED TWO-STAGE GRID-CONNECTED SPV SYSTEM

The proposed grid-connected solar photovoltaic system is shown schematically in figure 6.3. This strategy incorporates photovoltaic (PV) energy into the single-phase grid. The design model constitutes a photovoltaic source, a boost converter, and an asymmetric inverter. The PV cells are usually made with semiconductor materials and can produce voltages between 0.5 to 0.8 volts, which is very low for real-time applications. Thus, many PV cells (36 to 72) are connected in series to form a PV module to increase the voltage rating. Further, these PV modules are arranged in series

and in parallel to create a PV panel. PV modules connected in series enhance the voltage rating, while those connected in parallel increase the current rating.

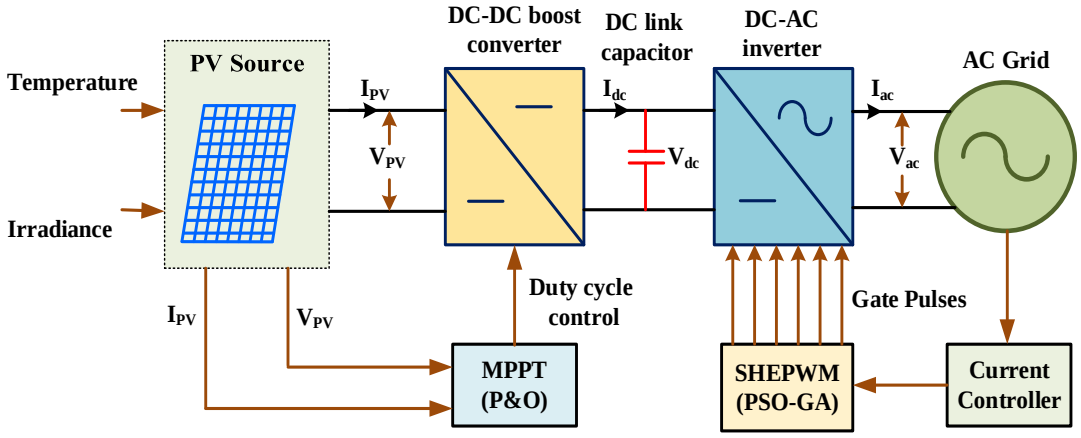


Figure 6.3 Proposed two-stage grid-connected SPV system

The boost converter is powered by the PV panel. With the P&O MPPT algorithm, the boost converter extracts the maximum power from the PV panel and feeds it to the inverter input through a dc-link capacitor. The dc-link capacitor stabilizes the dc-link voltage of the grid-connected system, which increases the injected voltage into the grid. A point of common coupling connects the inverter to the grid, which is required for its operation. The grid is interfaced with the proposed 15-level inverter, which can supply maximum power throughout the day. This can be achieved by optimal converter, inverter and control circuit to enhance the overall system efficiency.

6.5 IMPLEMENTATION OF PROPOSED GRID-CONNECTED SPV SYSTEM

Systemic block diagram of grid-connected photovoltaic (PV) power plant in figure 6.4. PV panels (or arrays), power converters, and the ac grid are the three essential components of the SPV system. Because PV arrays produce dc power, power electronic equipment must convert dc power into ac power. The grid-connected SPV system makes use of three PV sources to power the three inputs of the proposed 15-level inverter, which is linked to the power grid. A total of three distinct boost converters, each controlled by the P&O MPPT algorithm, are used to fulfil the input voltage requirements of a 15-level inverter. The dc power produced by three PV sources is supplied into three different boost converters. The inverter converts direct solar power into ac power and is crucial to operating an SPV system, although it is housed in

sophisticated circuitry [169]. The most important characteristics of an inverter are the capacity to function over a broad range of currents and voltages, output frequency, voltage control, and the ability to produce alternating current with high power quality. The key innovation is the grid integration of a reduced switch 15-level inverter with solar photovoltaic systems [170]. The inverter is controlled by the SHEPWM using a hybrid PSO-GA optimization algorithm considering the grid voltage and grid currents are the reference parameters. Standalone power generating systems have been built in several locations worldwide without any grid connection. The grid-connected system is thus a practical compromise for high power requirements and the erratic quality of renewable energy [171].

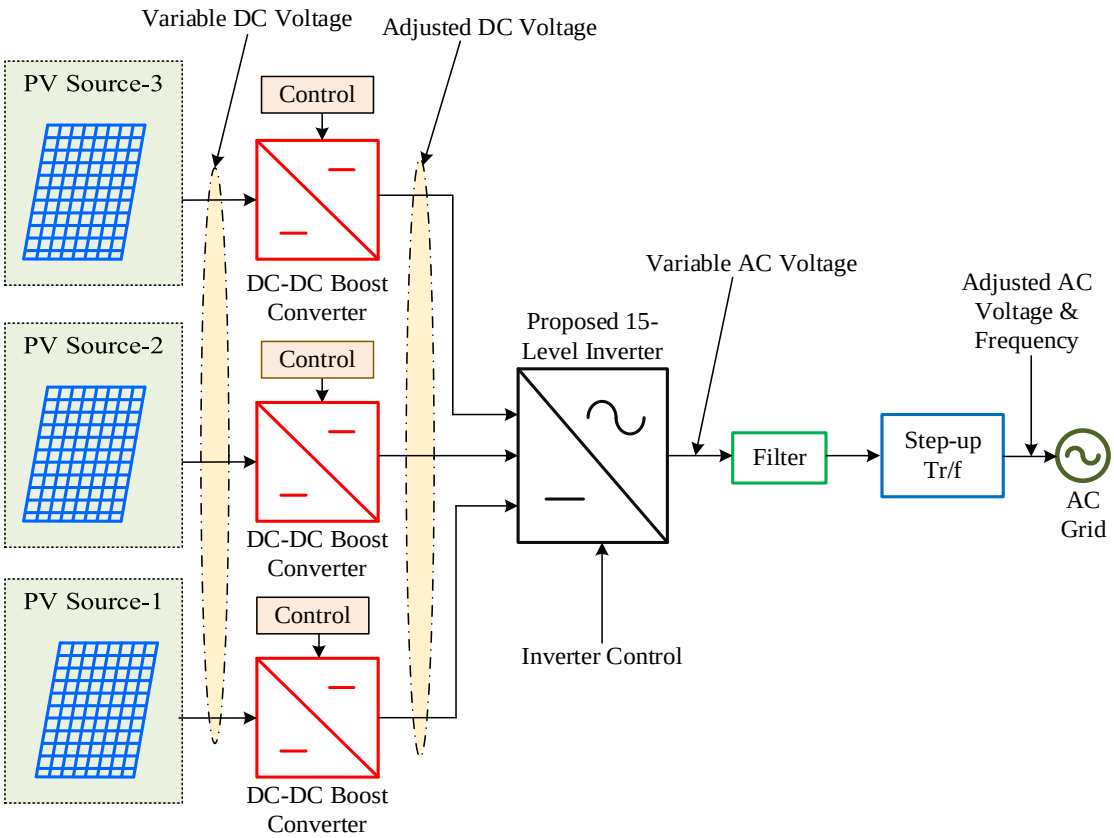


Figure 6.4 Schematic diagram of proposed grid-connected SPV system

The passive LCL filter then incorporates the suggested topology with the grid-connected system to further minimize the THD and improve waveform quality as per the grid requirements. The PV sources considered standard and practical test conditions with variable irradiance and temperature settings for the performance assessment of the proposed inverter under varying climate conditions.

6.6 MODELLING OF SPV SOURCES

A PV module is a power generation unit of the SPV system. The power output of the PV modules mainly depends on the temperature and irradiation and has non-linear I-V and P-V characteristics. Therefore, it is required to construct a PV module to determine the precise design, function, and reasons for PV output deterioration. There are two major PV system design categories: single diode type and two diode type. Single diode type design is quite simple, but it does not consider the recombination of losses (constant ideality factor '1') in the depletion layer. The two diode type is efficient and frequently used to match an actual curve, with the second diode's denominator of the exponential term's argument comprising an ideality factor of '2'. Even though single diode modelling is more common in PV modelling, it has several disadvantages.

i. Temperature variations have a significant impact on photovoltaic performance. It prevents diffusion loss in the depletion region of PV cells.
ii. The precision of the measurement was determined at low irradiance, in fact, at an open circuit (Voc).

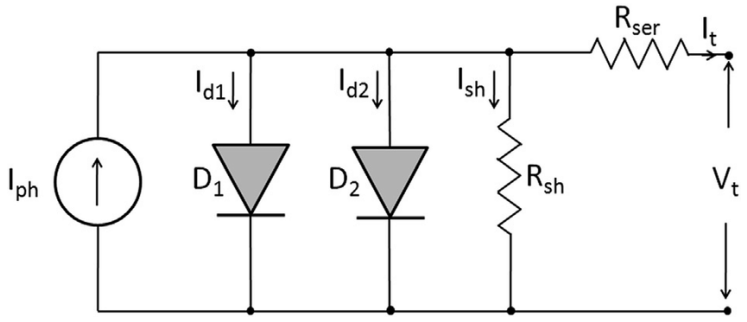


Figure 6.5 A two-diode model of photovoltaic cell

The two-diode model is recommended to improve PV technique precision, improve curve fitting, and remove the annoyance of the single-diode model. The circuit of the two-diode photovoltaic cell model is illustrated in figure 6.5. It consists of a current source (I_{PV}) and two diodes. But in practice, there are two additional resistances, one in series (R_{ser}) other in parallel (R_{sh}). The series resistance represents the ohmic loss because a solar cell is not a perfect conductor. Any slight change in R_{ser} has a significant impact on the output of the PV cell. The design equations of PV cell is represented as follows;

$$I = I_{Ph} - \mu_1 - \mu_2 - (V_S + 1 * R_{ser})/R_{sh} \quad (6.7)$$

Where,

$$\mu_1 = I_{d1} * \left(e^{\frac{V_S+1*R_{ser}}{\varepsilon_1 * V_t}} - 1 \right) \quad (6.8)$$

$$\mu_2 = I_{d2} * \left(e^{\frac{V_S+1*R_{ser}}{\varepsilon_2 * V_t}} - 1 \right) \quad (6.9)$$

Here,

μ_1= Current flowing through the diode D_1

μ_2= Current flowing through the diode D_2

I_{d1}= Saturation current of diode D_1

I_{d2}= Saturation current of diode D_2

ε_1= Emission coefficient of diode D_1

ε_2= Emission coefficient of diode D_2

V_s = PV cell voltage

V_t=Terminal voltage of PV cell

I_{ph}= Current produced in a photovoltaic cell.

Therefore the current produced by the PV cell is represented in equation (6.10).

$$I_{ph} = I_\sigma * (I_{so}/I_{\sigma 0}) \quad (6.10)$$

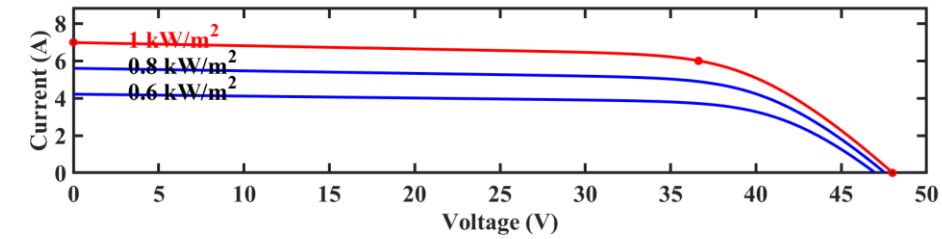
Where,

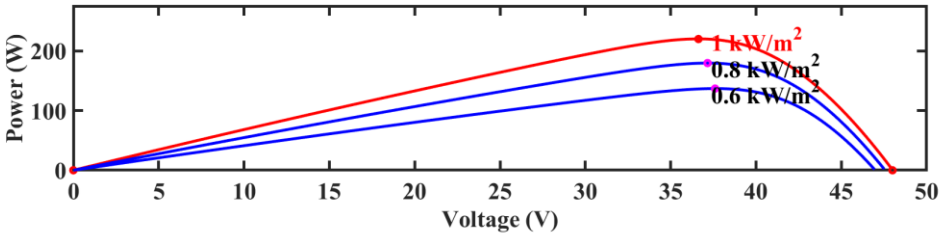
I_{so} = Solar current

I_σ & $I_{\sigma 0}$ = Irradiance currents

A solar panel consists of 24 PV cells. The open-circuit voltage of each PV cell is 0.5V. At standard test conditions (1000 W/m^2 and 25°C), these solar PV cells are connected in series to generate 12V. The choice PV sources for the proposed grid-connected system are P_{V1} = 48V, P_{V2} = 96V, and P_{V3} = 192V to get a peak value of 336V. Therefore, four 12V modules are connected in series to generate a voltage of 48V at the solar PV system's output.

Similarly, the 96V output can be obtained by series connection eight 12V modules, and series connection sixteen 12V modules get 192V output. The characteristics I-V and P-V of the PV_1, PV_2 & PV_3 are presented in figure 6.6 at a constant temperature of 25^0 C for variable irradiance.





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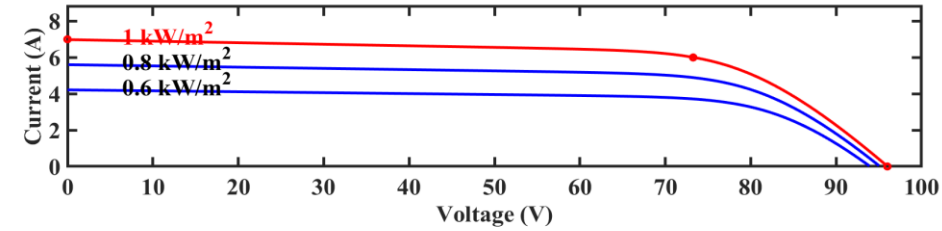

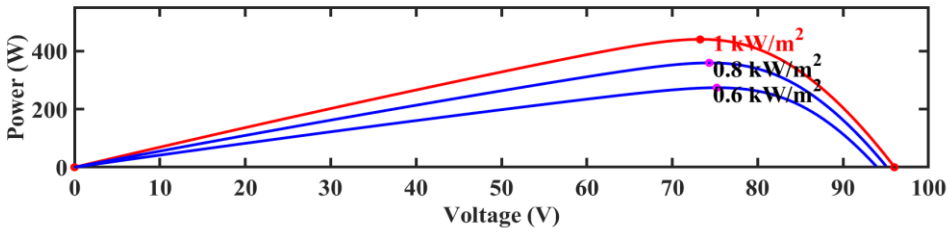

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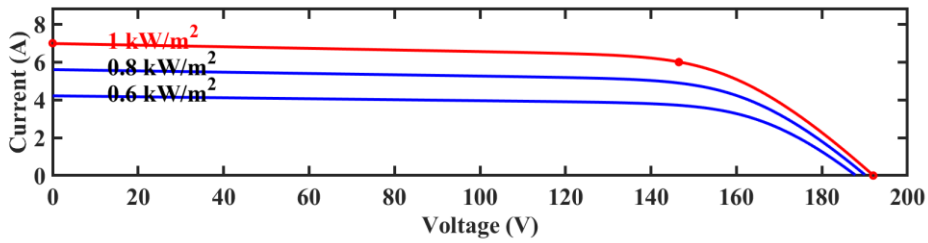
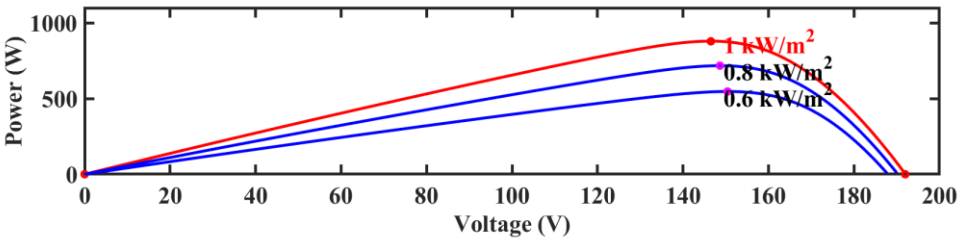
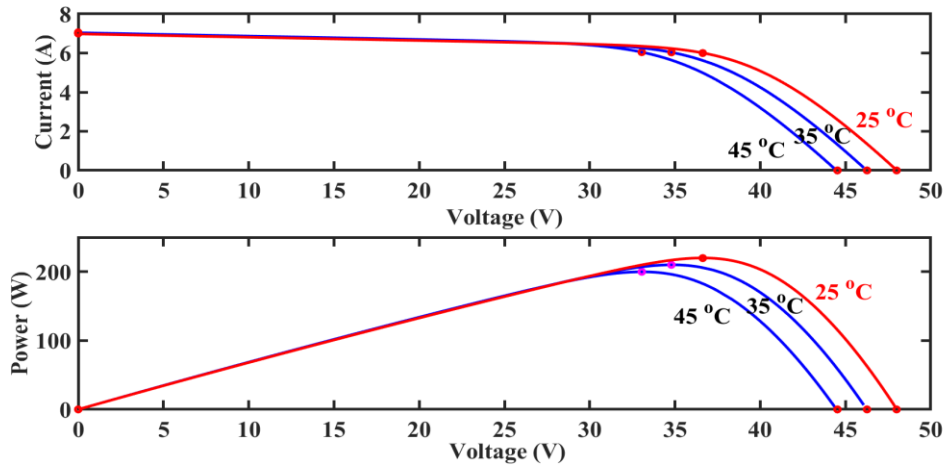




(c)

Figure 6.6 I-V & P-V curves at a constant temperature of 25^0 C with variable irradiance (a) PV source-1, (b) PV source-2 (c) PV source-3

The characteristics I-V and P-V of photovoltaic cell is illustrated in figure 6.7 at constant (1000 W/m^2) irradiance with varying temperature.



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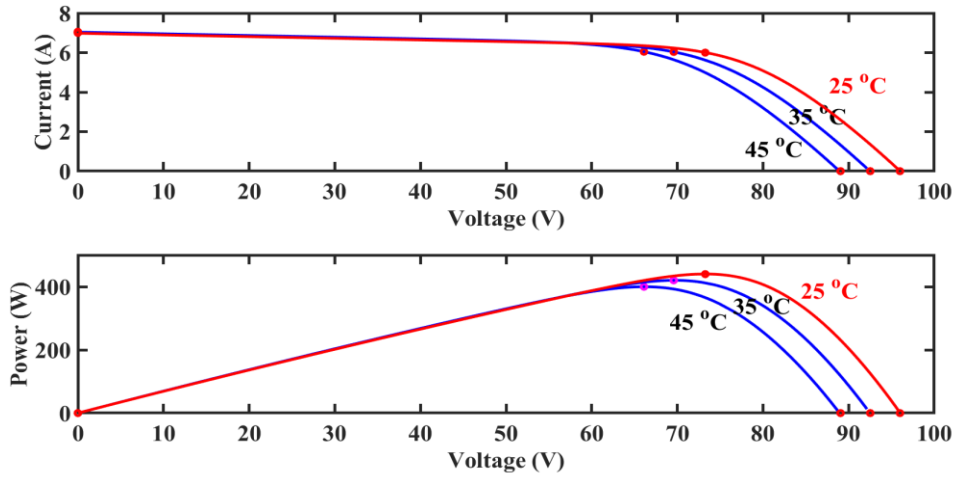

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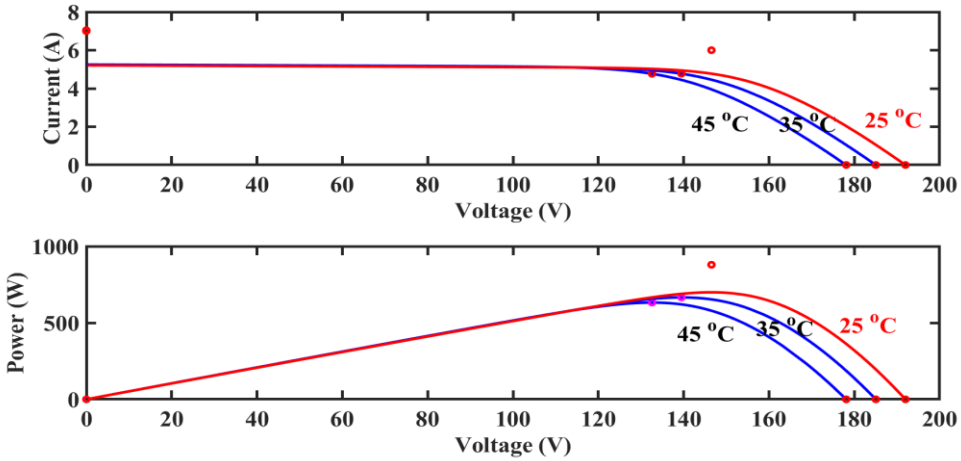

(c)

Figure 6.7 I-V & P-V curves at constant irradiation (1000 W/m^2) with variable temperature (a) PV source-1, (b) PV source-2 (c) PV source-3

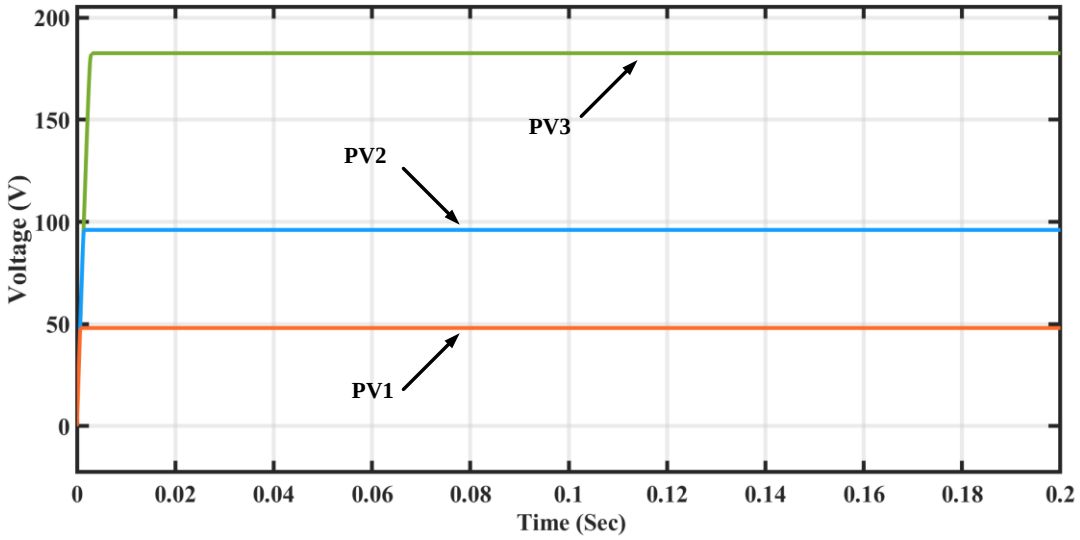

Figure 6.8 Asymmetric PV sources for the input of proposed 15-level inverter

The three input sources required for the 15-level inverter is illustrated in figure 6.8. These sources are dissimilar and asymmetric in nature with P_{V1} = 48V, P_{V2} = 96V, and P_{V3} = 192V.

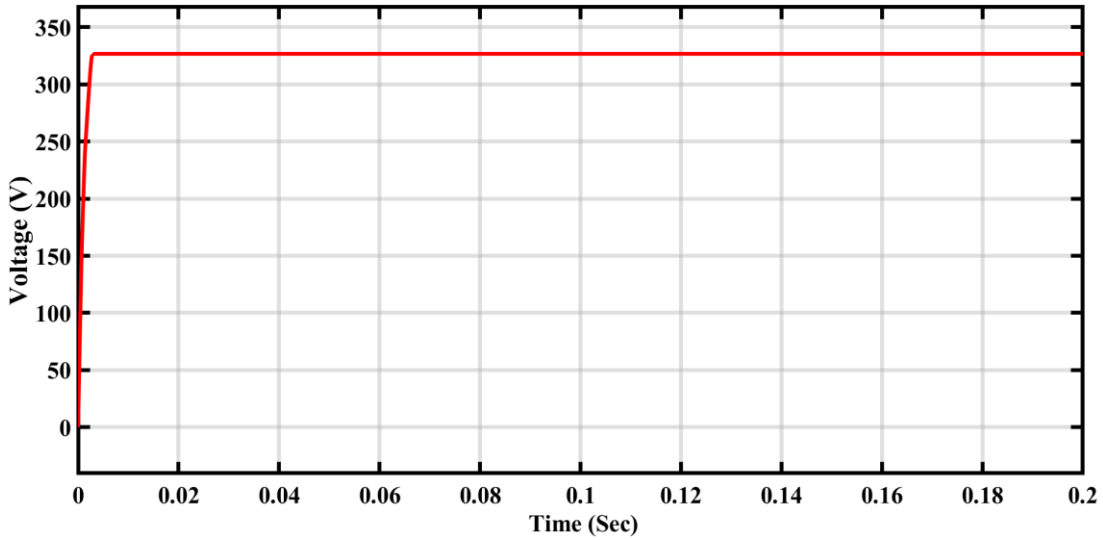

Figure 6.9 Total dc-link voltage of the three PV sources

The total value of the dc-link voltages combing the three PV sources is illustrated in figure 6.9. The simulated results give a peak value of 336V.

6.7 DESIGN OF DC-DC BOOST CONVERTER

The dc-dc conversion is critical in photovoltaic systems since the voltage generated by the PV panels does not meet the load requirements. The boost converter gives maximum power to the proposed 15-level inverter throughout this operation. The

typical design model of the dc-dc boost converter is illustrated in figure 6.10. The boost converter is used to step up the voltage of the PV system. It includes the diode, IGBT switch, inductor, capacitor. The purpose of the capacitor is to remove voltage disturbances in the output.

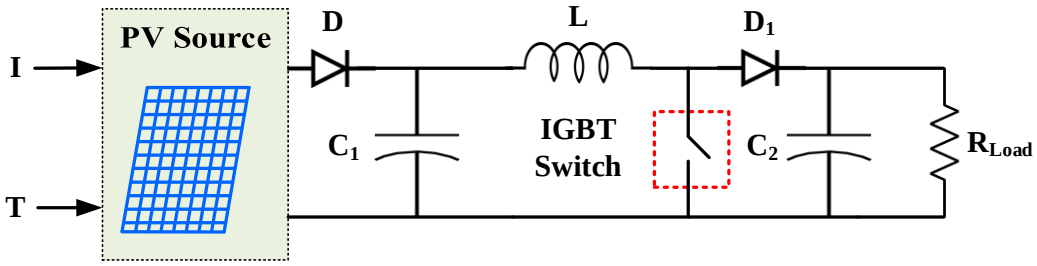

Figure 6.10 PV connected dc-dc boost converter

The inductor and capacitor are two critical components of a dc-dc converter that must be modelled to obtain the required output voltage. The inductor and capacitor are designed using fundamental mathematics.

$$L = \frac{V_{in} * (V_{out} - V_{in})}{\Delta I_L * f_s * V_{out}} \tag{6.11}$$

$$C = \frac{I_{out} * \delta}{f_s * \Delta V_C} \tag{6.12}$$

Where,

ΔI_L = Inductor ripple current

ΔV_C = Capacitor ripple voltage

δ = Duty cycle = $\frac{V_0 - V_s}{V_0}$

f_s = Switching frequency of the converter

The values of inductor ripple current and capacitor ripple voltages are calculated using equations (6.13) & (6.14), respectively.

$$\Delta I_L = (2\% \; to \; 4\%) * I_{out(max)} * \frac{V_{out}}{V_{in}} \tag{6.13}$$

$$\Delta V_C = (2\% \; to \; 4\%) * V_{out(max)} * \frac{I_{out}}{I_{in}} \tag{6.14}$$

Where, V_{out} is the maximum output voltage, V_{in} is the input voltage of the PV module, I_{in} is the input current of the PV module, $I_{out(max)}$ is the maximum output current of the PV module.

There are three separate boost converters used for the three independent PV sources to boost the PV voltage as per the requirement of inverter input. These boost converters are employed with individual P&O MPPT controllers for the control of the duty cycle.

6.8 DESIGN OF LCL FILTER

In most cases, the filter is connected to both the inverter and the grid. The filter performs three essential functions: it reduces high-frequency noise, shields the transient, and converts the voltage to a current source. The L-type, LC-type, and LCL-type filters are the three primary filters used in grid-connected networks. The LCL filter is used to link the inverter with the grid in this application. Because the inverter is concentrated on the switching devices and the switches require gating signals in the form of pulses, the output current may contain significant harmonic distortions that seek to deteriorate power quality. The criteria for calculating the model parameters are listed below.

The inductor at the inverter side is modelled with the equation (6.15).

$$L_i = \frac{V_{dc\ link}}{8\ f_s\ \Delta I_L} \tag{6.15}$$

Where,

ΔI_L = inductor ripple current

f_s = Switching frequency = 1000 Hz

$V_{dc\ link}$ = DC link voltage = 336V

Also, the inductor ripple current is evaluated using equation (6.16)

$$\Delta I_L = 0.1 * \frac{\sqrt{2}\ P}{V_{ph\ (grid)}} \tag{6.16}$$

Where,

P = Active power of the grid = 1250W

$V_{ph\ (grid)}$ = Phase voltage of the grid = 240V

Substituting these value in equation (6.15),

L_i = 57.03 mH

The grid side inductor can be calculated using equation (6.17)

$$L_g = 0.6 * L_i \quad (6.17)$$

= 34.22 mH

The capacitance value is determined, considering 5% of the base capacitance using the relation given in equation (6.18).

$$C_f = 0.05 * C_b \quad (6.18)$$

Where,

$$C_b = \frac{P}{\omega_{grid} * V_{grid}^2}$$

ω_{grid} = Angular frequency = 2πf = 314.2 rad/sec.

V_{grid} = Phase voltage of the grid = 240V

Therefore using the above values, the filter capacitance is,

C_f = 3.45 μF

6.9 CONTROL METHODOLOGY OF PROPOSED GRID-CONNECTED PV SYSTEM

Asymmetric PV sources feed the input dc supply of the proposed inverter. The current into the grid is injected by using an adaptive PI controller. The current injected must have a sinusoidal waveform and be in phase with the grid voltage in order to preserve the unity power factor [172-173]. For the PV array to provide a sinusoidal grid current, the dc voltages produced by the array must be maintained constant at all times.

There are two different control strategies used for voltage control for injecting the current into the grid. One can regulate the entire dc voltage output of the proposed inverter, while the other can control the dc voltage output of the PV array's respective

dc sources. Because asymmetrical PV inputs are connected to the inverter through dc links, individual dc-dc boost converters with MPPT controllers are constructed for each PV source in the proposed configuration. Under various operating situations, these independent MPPT controllers keep the dc-link voltages in the 1: 2: 4 ratio. To produce the reference PV voltages such as V_{dc1}^{*}, V_{dc2}^{*} and V_{dc3}^{*} a P&O based MPPT algorithm is used.

Figure 6.11 illustrates the suggested grid-connected inverter's control approach. The grid-connected controller regulates the three independent dc sources and maintains the appropriate voltage ratios between them (1 : 2 : 4).

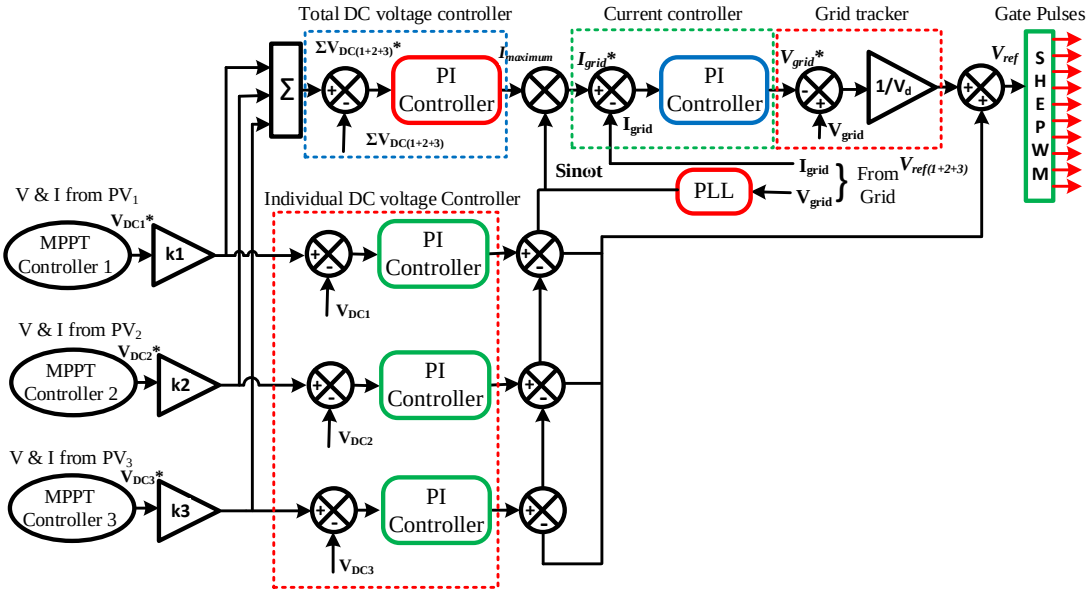

Figure 6.11 Grid-connected controller for proposed 15-level inverter [174].

6.9.1 Total dc voltage control

The closed-loop voltage controller seen in figure 6.11 is used to maintain a minimum dc-link voltage comparable to the appropriate reference voltage for the given irradiation level. To control the total dc voltage, the reference voltage (V_{dc1}^{*}+ V_{dc2}^{*} + V_{dc3}^{*}) is compared with the actual voltage (V_{dc1} + V_{dc2} + V_{dc3}), and the corresponding error is processed through the PI controller. The PI controller consists of two gains like Kp_{v1}, Kp_{i1} which are tuned by a hybrid PSO-GA optimization control to get the maximum value of reference current of the grid (I_{max}). A PLL generates the sinusoidal reference current (I_{g}^{*}) of the grid for the grid-connected system.

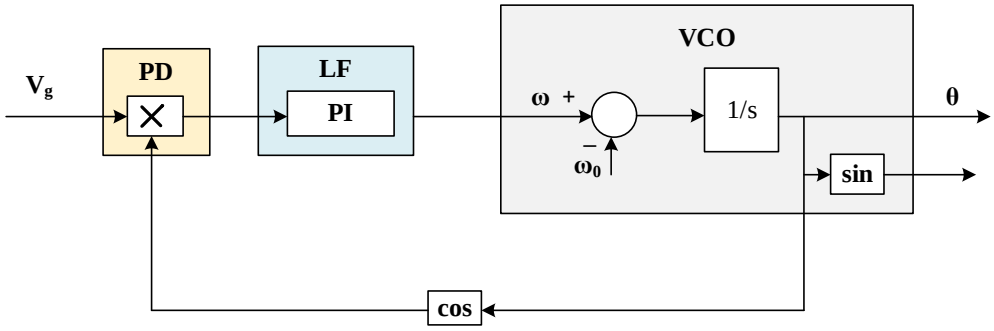

Figure 6.12 A typical model of single-phase PLL

The PLL is usually employed for grid integration. The typical model of PLL is illustrated in figure 6.12. The components of the PLL are a voltage-controlled oscillator, a low pass filter controlled by a PI controller and a phase detector. The phase detector block is responsible for detecting the phase difference between the input and feedback signals. The input of the phase detector block is provided by equation (6.19).

$$V_G(t) = \sqrt{2}\, V_{grid\ (rms)} * \sin(\omega_g t + \varphi) \tag{6.19}$$

The output obtained from the phase detector block is represented in equation (6.20).

$$V_{PD}(t) = \sqrt{2}\, V_{grid(rms)} \sin(\theta_g) \cos(\hat{\theta}) \tag{6.20}$$

The equation (6.20) further represented as,

$$V_{PD}(t) = \frac{\sqrt{2}}{2} V_{grid(rms)} \left(\sin \begin{bmatrix} (\omega_g - \hat{\omega})t + \\ (\varphi_g - \hat{\varphi}) \end{bmatrix} + \sin \begin{bmatrix} (\omega_g + \hat{\omega})t + \\ (\varphi_g + \hat{\varphi}) \end{bmatrix} \right) \tag{6.21}$$

There are two components in equation (6.21) (high frequency and low frequency). When the phase detector's output is transmitted through the PI-based LF block, the low pass filter removes the high-frequency component, and the frequency component is retrieved at the LF block's output.

$$V_{LF}(t) = \frac{\sqrt{2}}{2} V_{grid(rms)} \left(\sin \left[(\omega_g - \hat{\omega})t + (\varphi_g - \hat{\varphi}) \right] \right) \tag{6.22}$$

The PI controller will provide appropriate frequency. As $\omega_g = \widehat{\omega_g}$ and $\varphi_g = \hat{\varphi}$, the output signal from the LF block indicated in equation (6.22) tends to zero under the steady condition. By using the grid voltage as an input, the output phase signal is locked.

6.9.2 Grid voltage and grid current control

The reference current needed by the grid is generated using a PLL (phased lock loop). The measured value (I_{grid}) is compared to the reference grid current I_{grid*}, and the error acquired is sent into the PI current controller. The grid current is maximized by changing the PI controller's gains (Kp, Ki). The current controller provides a reference signal V_{k*} during stable operating conditions, and the reference inverter voltage is obtained by subtracting the grid voltage signal from the reference inverter voltage. As a result, the inverter reference voltage changes in line with the grid voltage. When the grid voltage drops, the difference $V_{grid} - V_{k*}$ drops as well, and the reference voltage of the inverter drops as well. This is known as a grid tracker. The grid tracker's output can be scaled to create a part of the proposed inverter's reference voltage.

6.9.3 Individual dc voltage control

For a 15-level asymmetric inverter, three unequal dc sources V_{dc1}, V_{dc2}, $V_{dc3,}$ are used under various atmospheric conditions. In addition to the total dc voltage control, there exist two other voltage controllers, which are required to maintain the V_{dc2}, V_{dc3} voltages at their reference voltages V_{dc2}^{*} and V_{dc3}^{*}. For the inverter's reference signal, the sine component of grid frequency (obtained by PLL) is combined with outputs from the total and individual voltage controllers.

6.9.4 SHEPWM control for proposed grid-connected PV system

A harmonic-free output waveform is generated using the selective harmonic elimination method, which determines the triggering angles for inverter switches to conduct. [175]. Lower order harmonics are reduced by using the SHEPWM method, resulting in a smaller filter size for the system. This method uses quarter-wave symmetry to cut down on computations. Hence the switching angles are computed between 0^0 and 90^0 ($0^0 \leq \alpha \leq 90^0$). The even-order harmonics in the Fourier expansion are zero due to the odd symmetry of the quarter-wave.

The output of the proposed inverter is synthesized as follows.

$$V_0 = a_0 + \sum_{n=1}^{\infty} A_n \cos(n\omega t) + \sum_{n=1}^{\infty} B_n \sin(n\omega t) \quad (6.23)$$

The even harmonics become zero in the output of the inverter because the analysis is considered the quarter-wave symmetry. Therefore, the equation (6.23) can be written as,

$$V_0 = \sum_{n=1}^{\infty} B_n \, sin(n\omega t) \tag{6.24}$$

Where,

$$B_n = \frac{1}{\pi} \int_0^{2\pi} V_{PV} \, sin(n\omega t) \, d\omega t \tag{6.25}$$

Generally, the output of the multilevel inverter is the staircase in nature; hence the equation (6.25) can be represented as,

$$B_n = \frac{2}{\pi} \int_0^{\pi} V_{PV} \, sin(n\omega t) \, d\omega t \tag{6.26}$$

On integrating the equation (6.26), the resultant B_n can be written as

$$B_n = \frac{4V_{PV}}{k\pi} \sum_i^z cos(k\alpha_i) \tag{6.27}$$

Here, k represents the order of the harmonic, z represents the number of switching angles for the quarter-wave, α_i Represents the ith switching angle, and V_{PV} represents the dc voltages fed from the SPV system. The number of firing angles required for an N-level output is represented in equation (6.28).

$$Z = \frac{N-1}{2} \tag{6.28}$$

Where N represents the number of output voltage levels. According to equation (6.28), 15 voltage levels needed seven switching angles, and 7-1 = 6 is the harmonic order k. Six non-linear equations (excluding fundamental) must be solved to generate the proposed 15-level inverter's seven switching angles. The switching angles must fulfil the below constrain for the quarter-wave approximation.

$$\alpha_1 < \alpha_2 < \alpha_3 < \alpha_4 < \alpha_5 < \alpha_6 < \alpha_7 < \frac{\pi}{2} \tag{6.29}$$

The fundamental voltage component always is to be equated to modulation index (M_i) of corresponding PWM technique, which can be written as:

$$M_i = \frac{V}{V_{PV}} \tag{6.30}$$

Where V is the magnitude of the fundamental component, V_{PV} represents the DC voltages fed from the SPV system. Therefore the non-linear equations generated from equation (6.27) is solved using a hybrid PSO-GA algorithm, and the corresponding switching angles are stored in lookup tables for various modulation index. These switching angles are retrieved from the lookup tables for a given modulation index set by the dc-link voltage. Further, these switching angles trigger the seven switches in the proposed inverter to produce the corresponding voltage and currents.

6.10 RESULTS & DISCUSSIONS

The simulation results of a single-phase SPV fed asymmetric inverter-based GCSPV system employing PSO-PI, HHO-PI and hybrid PSO_GA-PI controllers are discussed in this section. The suggested control approach to increase the power quality and inject sinusoidal current into the grid is developed in MATLAB. The grid-connected PV system is introduced, and the system's power quality is investigated in the proposed control approach. The adaptive control of the proposed method feeds sinusoidal current into the grid for various grid circumstances. On the grid side, the feasibility of the proposed system is evaluated based on variable temperature and irradiations and the corresponding performance for different solution strategies. The parameters and their specifications of the SPV fed grid-connected system is illustrated in table 6.1.

Table 6.1 Specifications of the PV fed grid-connected system

Parameter	Specifications
RMS voltage of the grid	240V (rms)
DC link voltage	336V
Switching frequency	1000Hz
Supply frequency	50Hz
Filter inductance (inverter side)	57.03mH
Filter inductance (grid side)	34.22mH
Filter capacitance	3.45μF
Grid resistance	0.05Ω

6.10.1 Simulation of dc sources under variable atmospheric conditions for GCSPV system

For a 1.25kW single-phase SPV system, a 15-Level asymmetric inverter is modelled and simulated in Simulink. The input voltages are taken as 48V, 96V, and 192V to obtain the peak voltage of 336V. i.e., the total dc-link voltage is 48V+ 96V + 192V = 336V. The voltage sources V_1, V_2, and V_3 in figure 3.4 are replaced by PV sources as PV_1, PV_2, and PV_3. This inverter is simulated by connecting a single-phase grid as the load on the system. The inverter dc input voltages greater than $\sqrt{2}V_{grid}$, should be satisfied for grid-connected SPV systems. The peak voltage of the proposed system is 336V, which is more than the grid voltage. The proposed grid-connected SPV system is evaluated under various irradiance and temperature circumstances, with the appropriate PV current, voltage, and power values determined. Also, the Boost voltage (DC bus voltage) and boost current are measured. It is desired to maintain the dc inputs of the inverter at constant PV_1 = 48V, PV_2 = 96V, and PV_3 = 192V. The boost converter duty cycle is tuned to adjust these voltages from the variable PV sources. Three different cases of uneven irradiation and temperatures are considered for the PV system for analyzing the performance of the 15-level inverter.

Case (i) Irradiance of 1000 W/m^2 at a temperature of 25^0 C

In case (i), the PV sources operated at standard test conditions with the irradiance of 1000 W/m^2 and temperature of 25^{0}C.

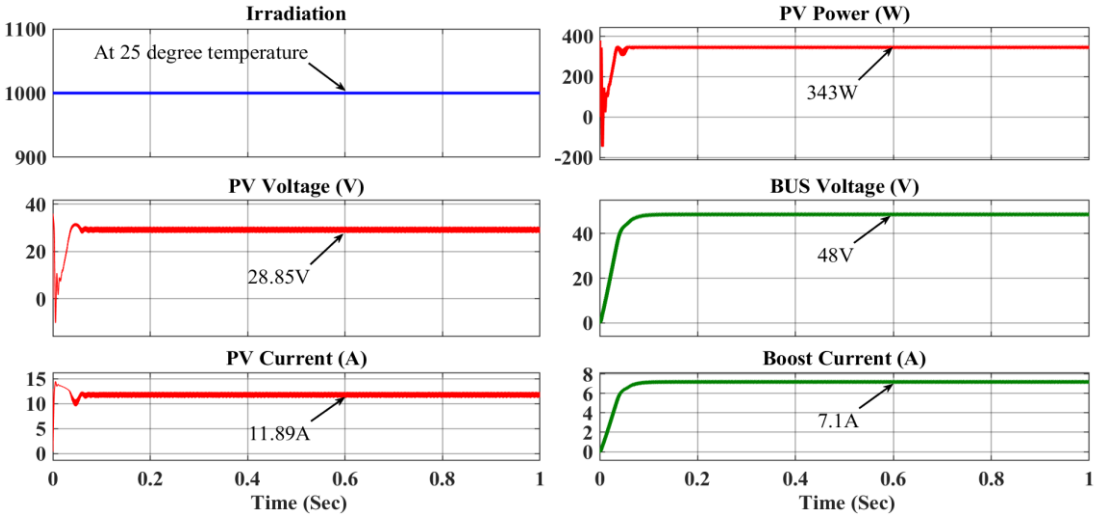

Figure 6.13 PV measurements, boost voltage & current at an irradiance of 1000 W/m^2 and temperature of 25^0 C for PV_1

At this test condition, PV_1 produces a power of 343W with a voltage of 28.85V and a current of 11.89A. This voltage level is not sufficient for the proposed inverter. PV_1 voltage is increased to 48V with the help of a boost converter, and the corresponding output current is 7.1A, as shown in figure 6.13.

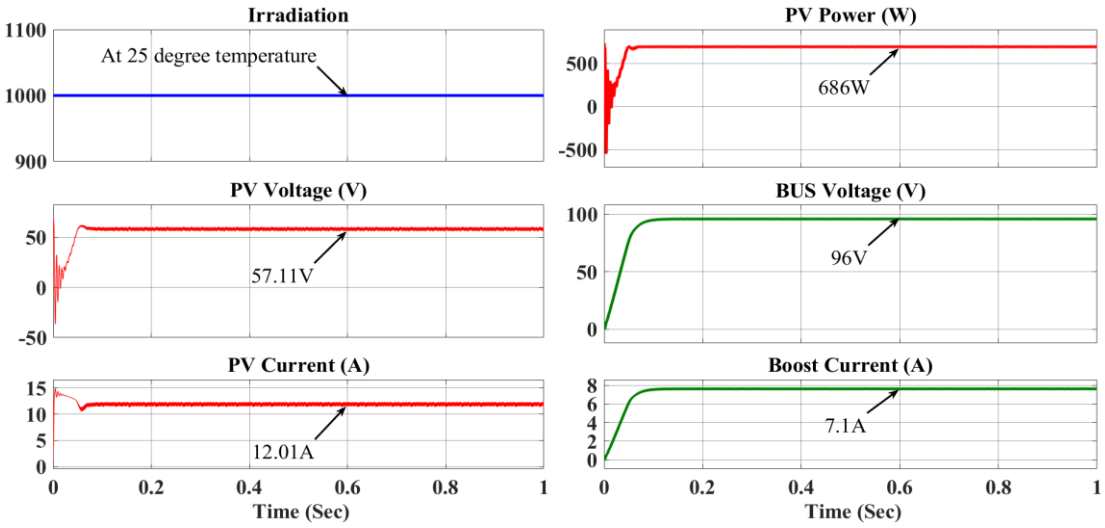

Figure 6.14 PV measurements, boost voltage & current at an irradiance of 1000 W/m^2 and temperature of 25^0 C for PV_2

PV_2 produces a power of 686W with a voltage of 57.11V at 12.01A of current. But the inverter input-2 is required 96V. Hence, the PV_2 voltage increased to 96V from 57.11V using a boost converter to get a current of 7.1A, as shown in figure 6.14.

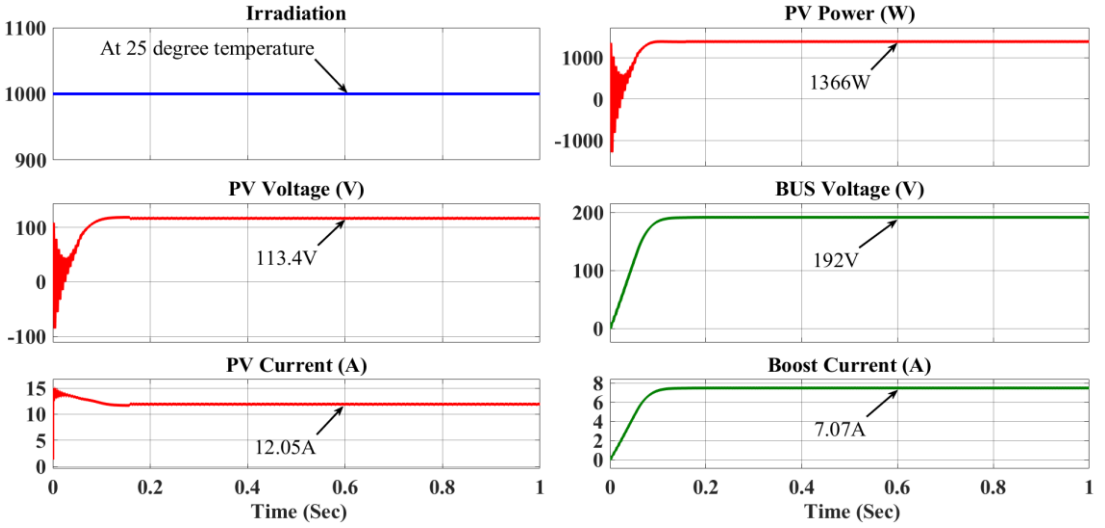

Figure 6.15 PV measurements, boost voltage & current at an irradiance of 1000 W/m^2 and temperature of 25^0 C for PV_3

Similarly, PV_3 produces a power of 1366W with a voltage of 113.4V at 12.05A of current. But the inverter input-3 is required 192V. Hence, the PV_3 voltage increased to 192V from 113.4V using a boost converter to get an output current of 7.07A, as shown in figure 6.15.

Case (ii) Irradiance of 800 W/m^2 at a temperature of 25^0 C

In case (ii), the PV sources operated at practical test conditions with the irradiance of 800 W/m^2 and temperature of 25^{0}C. At this test condition, PV_1 produces a power of 276W with a voltage of 28.86V and a current of 9.565A. This voltage level is not sufficient for input-1 of the proposed inverter. PV_1 voltage is increased from 28.86V to 48V with the help of a boost converter, and the corresponding output current is 5.72A, as shown in figure 6.16.

PV_2 produces a power of 552W with a voltage of 57.24V at 9.65A of current. But the inverter input-2 is required 96V. Hence, the PV_2 voltage increased to 96V from 57.24V using a boost converter to get an output current of 5.72A, shown in figure 6.17.

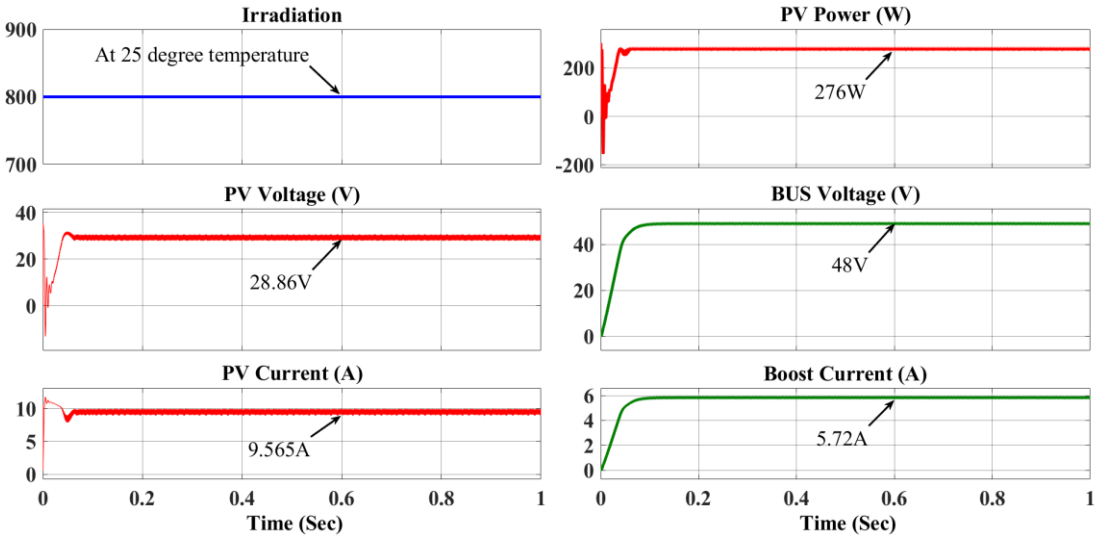

Figure 6.16 PV measurements, boost voltage & current at an irradiance of 800 W/m^2 and temperature of 25^0 C for PV_1

Similarly, PV_3 produces a power of 1022W with a voltage of 99.94V at 10.23A of current. But the inverter input-3 is required 192V. Hence, the PV_3 voltage increased to 192V from 99.94V using a boost converter which gives an output current of 5.3A, as shown in figure 6.18.

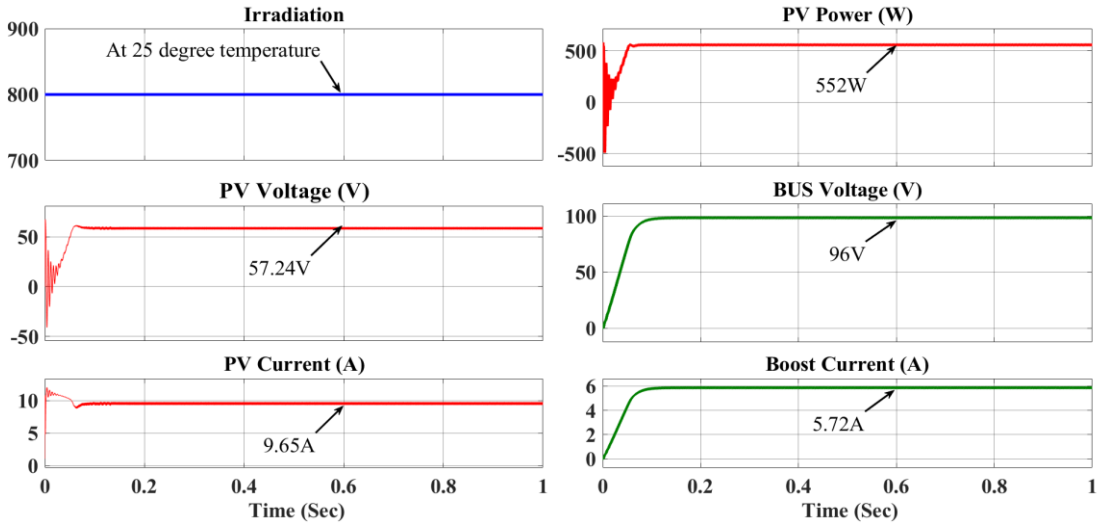

Figure 6.17 PV measurements, boost voltage & current at an irradiance of 800 W/m^2 and temperature of 25^0 C for PV_2

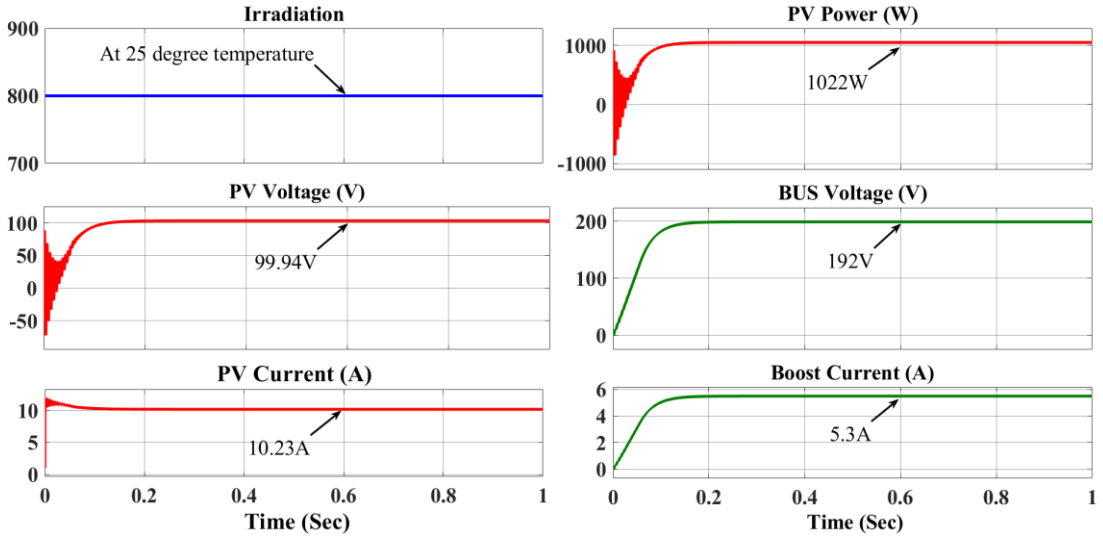

Figure 6.18 PV measurements, boost voltage & current at an irradiance of 800 W/m^2 and temperature of 25^0 C for PV_3

Case (iii) Irradiance of 600 W/m^2 at a temperature of 35^0 C

In case (iii), the PV sources operated at practical test conditions with the irradiance of 600 W/m^2 and temperature of 35^{0}C. At this test condition, PV_1 produces a power of 200W with a voltage of 27.42V and a current of 7.316A. This voltage level is not sufficient for input-1 of the proposed inverter. PV_1 voltage is increased from 27.42 V to 48V with the help of a boost converter, and the corresponding output current is 4.13A, as shown in figure 6.19.

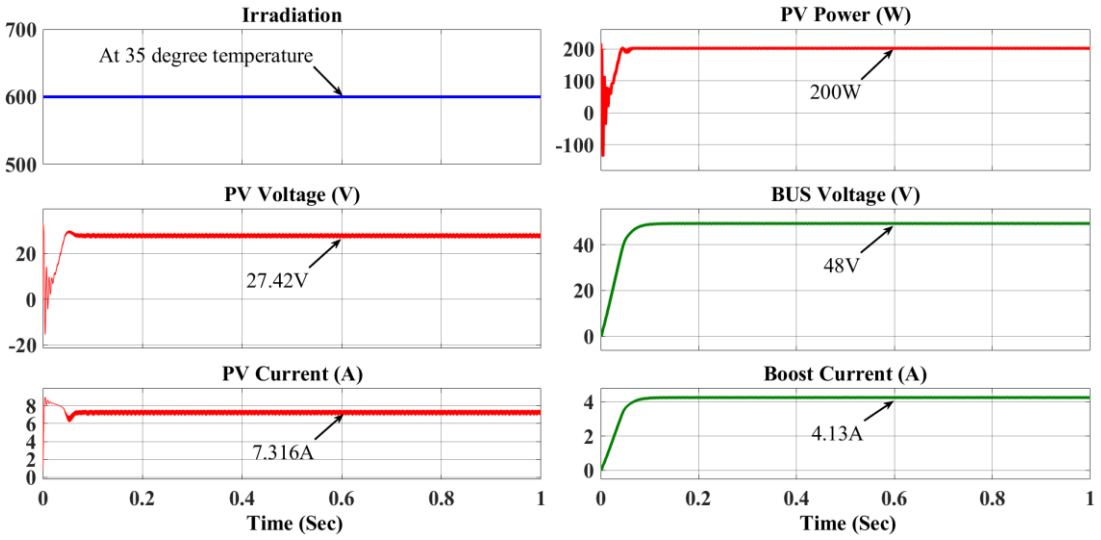

Figure 6.19 PV measurements, boost voltage & current at an irradiance of 600 W/m^2 and temperature of 35^0 C for PV_1

PV_2 produces a power of 400.7W with a voltage of 54.6V at 7.34A of current. But the inverter input-2 is required 96V. Hence, the PV_2 voltage increased to 96V from 54.6V using a boost converter, giving an output current of 4.14A, as shown in figure 6.20.

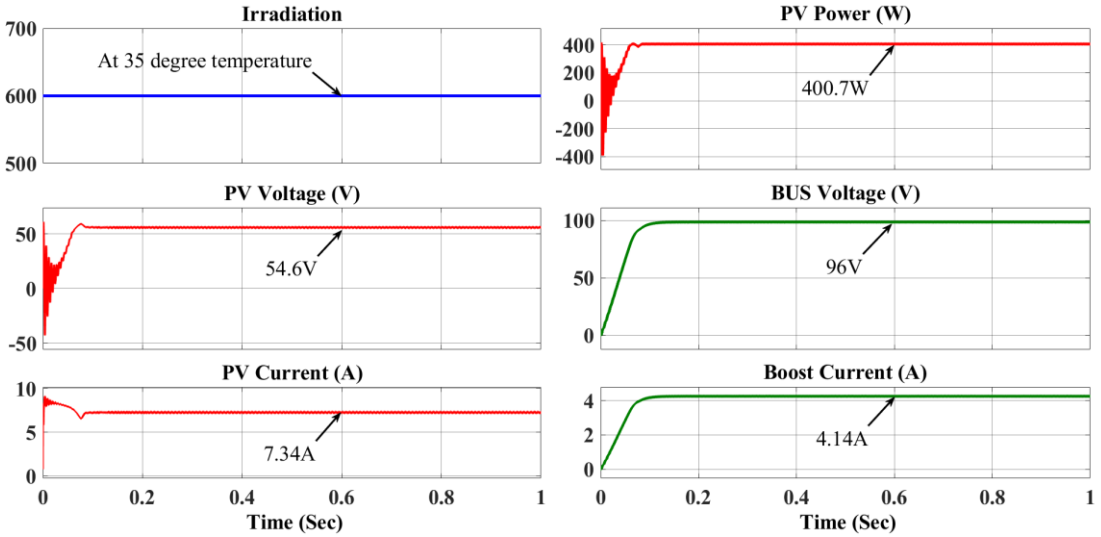

Figure 6.20 PV measurements, boost voltage & current at an irradiance of 600 W/m^2 and temperature of 35^0 C for PV_2

Similarly, PV_3 produces a power of 621.5W with a voltage of 78.08V at 7.96A of current. But the inverter input-3 is required 192V. Hence, the PV_3 voltage increased to 192V from 78.08V using a boost converter, giving an output current of 3.22A, as shown in figure 6.21. From the discussions of case (i), case (ii) & case (iii), it is

confirmed that the reduction irradiation and increase the temperature will result in a reduction in the output power of the PV panel. So, it is necessary to operate the PV panels at maximum irradiance and minimum temperature to get maximum power point.

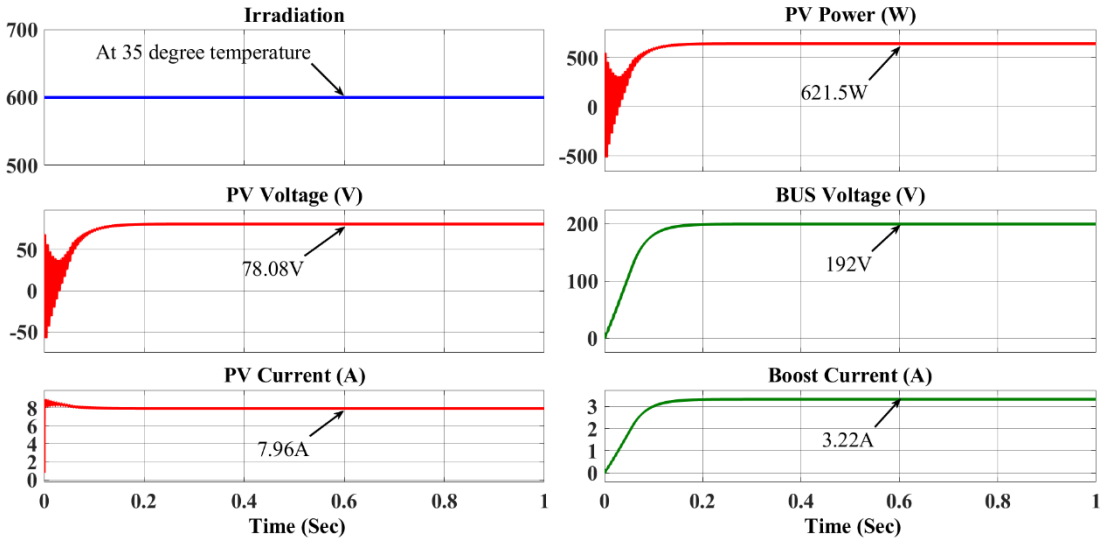

Figure 6.21 PV measurements, boost voltage & current at an irradiance of 600 W/m^2 and temperature of 35^0 C for PV_3

Although, for analyzing the performance of the proposed inverter on practical operating test conditions of the PV system, an irradiance of 600 W/m^2 and a temperature of 35^{0}C is considered. The control of grid parameters under these test conditions is described in the following sections.

6.10.2 Implementation of PSO-PI controller for GCSPV system

The PSO variables necessary to adjust the gains of PI controllers of the entire voltage control block and the current control block are shown in table 6.2. The integral time absolute error is chosen as the cost function, and the PSO algorithm gives the gains of the two PI controllers while minimizing the fitness function. After 114 iterations, the best gain parameters for voltage gains of PI (K_{Vp}, K_{Vi}) and current gains of PI (K_{Cp}, K_{Ci}) controllers are achieved. The PSO tuned PI gains of the voltage and current controllers are given as K_{Vp} = 0.51, K_{Vi} = 0.209, K_{Cp} = 0.87, K_{ci} = 0.341, respectively. Figure 6.22 illustrates the grid voltage and grid current waveforms for the unity power factor employing PSO-PI control, with a peak voltage of 336.8V and a peak current of 6.89A, which are in phase with the grid voltage. The FFT analysis of grid current waveform, representing the total harmonic distortion (3.96%), is shown in figure 6.23 using the PSO-PI controller.

Table 6.2 Parameters & specifications of PSO

Parameters	Values
Population size	50
Cognitive constant, C1	0.5
Social constant, C2	1.25
Inertia Weight, W	1
Maximum velocity	10
Number of iterations	200

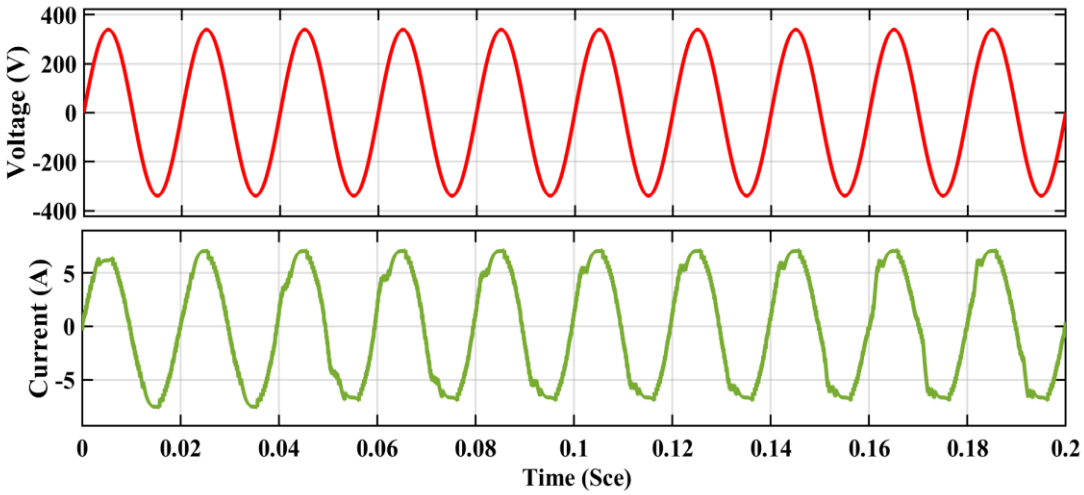

Figure 6.22 Grid voltage and grid current waveforms with PSO-PI controller

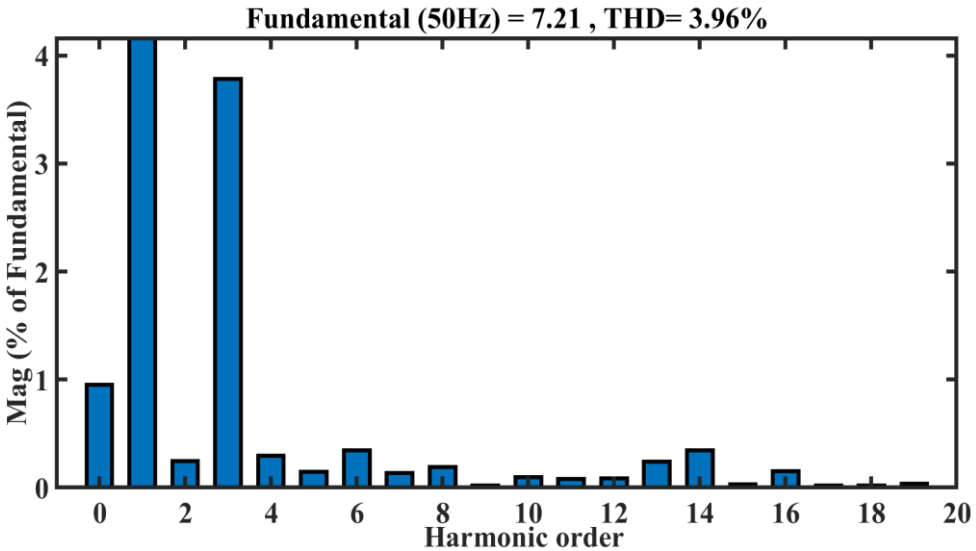

Figure 6.23 THD analysis of grid current waveform with PSO-PI controller

6.10.3 Implementation of HHO-PI controller for GCSPV system

The HHO method uses the integral time absolute error as the fitness function to determine the parameters of the PI controller in the proposed control system's total voltage controller block and current controller block. Equation (6.31) and equation (6.32) represents integral time absolute errors used as the fitness functions of HHO for tuning the gain values of total voltage control and current control blocks, respectively. The parameters and specifications involved in tuning the PI controller using the HHO algorithm are represented in table 6.3.

$$ITAE = \int t * |e(t)|\, dt = \int_0^t \left|V_{DCref} - V_{DCact}(t)\right| * t\, .dt \tag{6.31}$$

$$ITAE = \int t * |e(t)|\, dt = \int_0^t \left|I_{GRIDref} - I_{GRIDact}(t)\right| * t\, .dt \tag{6.32}$$

Table 6.3 Specifications and parameters of HHO

Parameters	Values
Number of Hawks 'N'	30
Random generations r1, r2, r3, r4	In the range of [0,1]
Number of search agents	7
Initial energy (E_0)	[-1,1], [-1.0] loosing energy, [0,1] raising energy
Convergence probability 'r'	0.5
Number of iterations	200

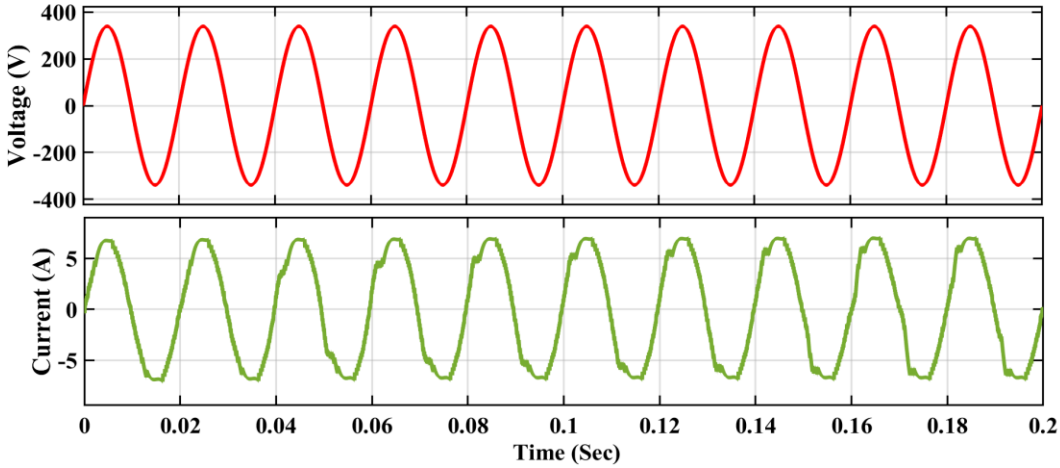

Figure 6.24 Grid voltage and grid current waveforms with HHO-PI controller

HHO uses 75 iterations to get the most acceptable voltage and current control gains of the PI controller. The optimum values of gain parameters are K_{Vp} = 0.81, K_{Vi} = 0.11, K_{Cp} = 0.91, Kc_i = 0.089 using HHO-PI controller for GCSPV system.

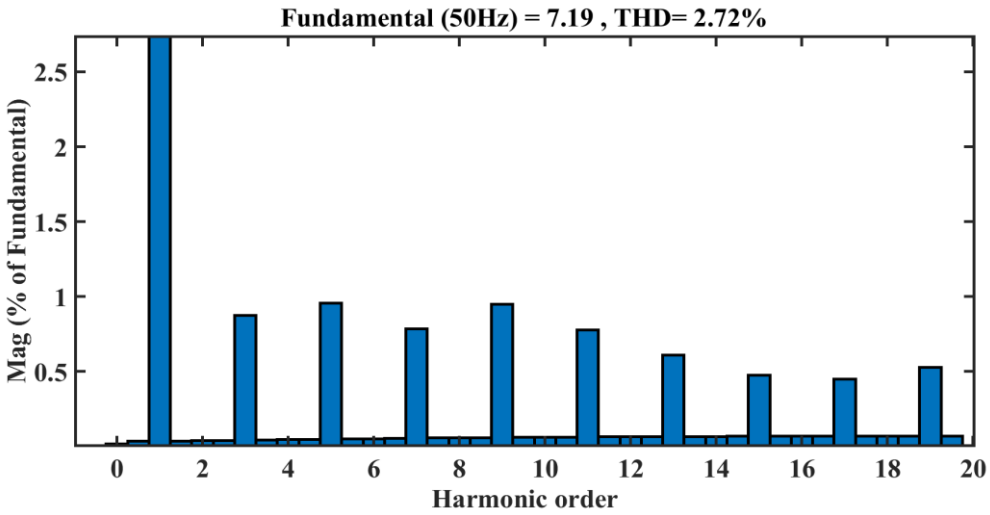

Figure 6.25 THD analysis of grid current waveform with HHO-PI controller

Figure 6.24 shows the grid voltage waveform and grid current waveform with a peak voltage of 336.7V & peak current of 6.91A, which are in phase for the unity power factor using HHO-PI control. The FFT analysis of grid current waveform, representing the total harmonic distortion (2.72%), is shown in figure 6.25 using the HHO-PI controller.

6.10.4 Implementation of a hybrid PSO_GA-PI controller for GCSPV system

Particle swarm optimization (PSO) improves the vector in this approach, while the genetic algorithm (GA) is used to update the decision vectors using genetic operators. The balance between exploration and exploitation abilities has been further enhanced by introducing genetic operators, such as crossover and mutation, into the PSO algorithm. The fitness function is chosen to be the integral time absolute error. The PSO algorithm is used to calculate the gains of the two PI controllers while minimizing the fitness function. Here the equation (6.31) is the fitness function for the voltage controller of PI, and equation (6.32) is the fitness function of the current controller of PI. The optimum values of gain parameters are K_{Vp} = 0.96, K_{Vi} = 0.089, K_{Cp} = 0.94, Kc_i = 0.096 using PSO_GA -PI controller for GCSPV system. The specifications and parameters used in hybrid PSO_GA based PI tuning is presented in table 6.4.

Table 6.4 Specifications and parameters of hybrid PSO-GA

Parameters	Values
Population size from	50
Crossover fraction	0.8 as default
Number of iterations	200
Mutation rate	0.006
Cognitive constant, C1	0.5
Social constant, C2	1.25
Inertia Weight, W	1

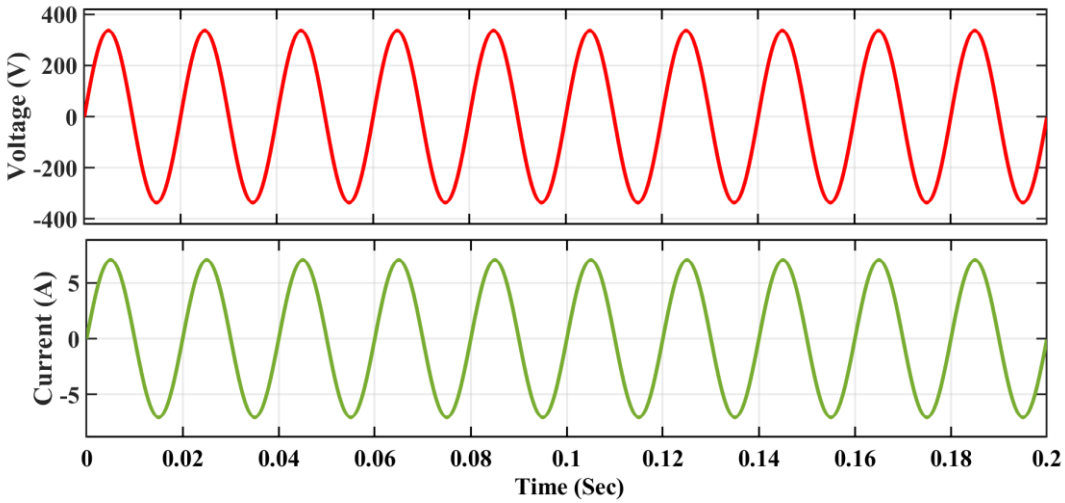

Figure 6.26 Grid voltage and grid current waveforms with PSO_GA-PI controller

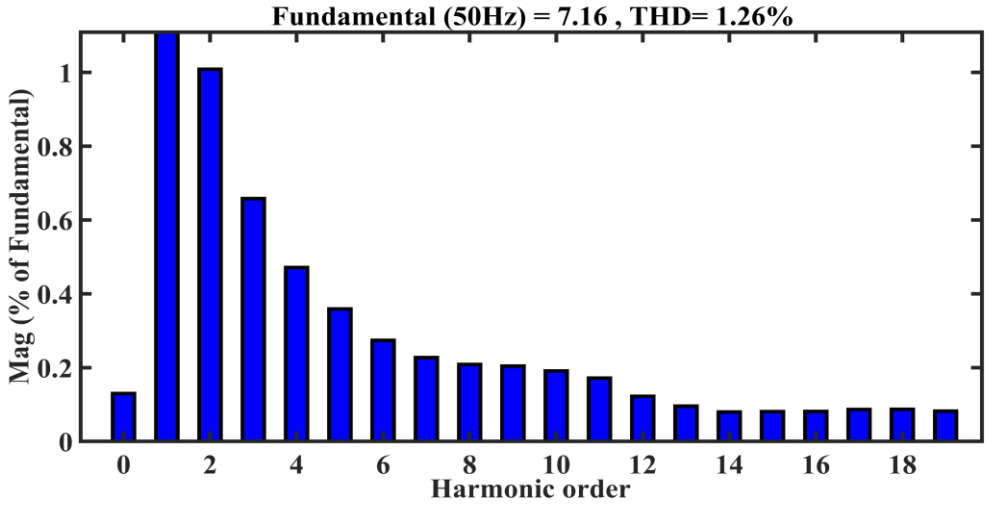

Figure 6.27 THD analysis of grid current waveform with PSO_GA-PI controller

Figure 6.26 shows the grid voltage waveform and grid current waveform with a peak voltage of 336.7V & peak current of 6.96A, which are in phase for the unity power factor using PSO_GA-PI control. The FFT analysis of grid current waveform, representing the total harmonic distortion (1.26%), is shown in figure 6.27 using the PSO_GA-PI controller.

The inverter provides active power to the grid during grid steady-state operation. To preserve the unity power factor, the proposed inverter injects current into the grid in phase with the grid voltage. Active and reactive power of the grid under steady-state is measured, and the corresponding waveforms of the system are presented in figure 6.28. The active and reactive powers measured are 1171.7W and 26.09 VAr, respectively.

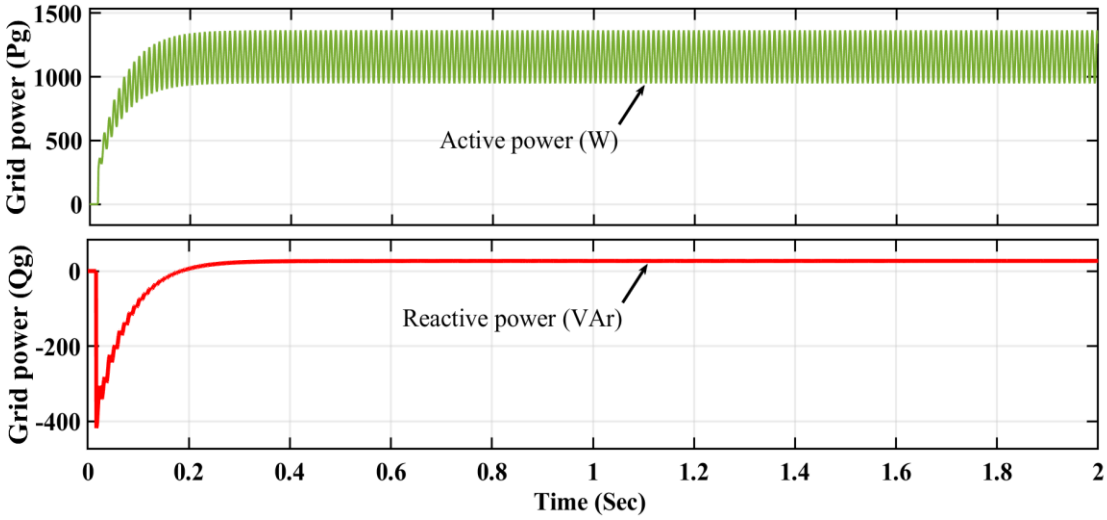

Figure 6.28 Active and reactive power delivered to the grid

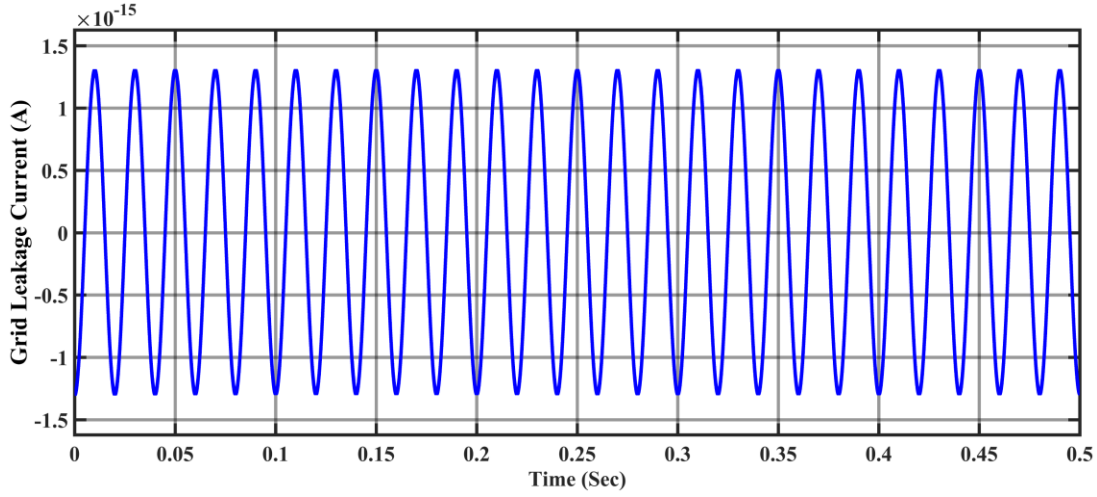

Figure 6.29 Leakage current in the grid-connected PV system

Figure 6.29 depicts the leakage current measured in the grid, which is in the order of 1.25 x 10^{-15}A (very low). The leakage current in the grid is very low and insignificant. Thus this research concludes that the grid's performance is good with the suggested inverter and control method. The leakage current is affected by the driver circuit's design, grid voltage, and frequency of pulse width modulation, grid impedance, and filter interference. A comparison of various gain parameters and corresponding THDs of different grid-connected controllers with the proposed controller is presented in table 6.5.

Table 6.5 Comparison of gain parameters and THDs of proposed GCSPV system

Controller	Gain Parameters				%THD
	Voltage Controller		Current Controller		
	K_{Vp}	K_{Vi}	K_{Cp}	K_{Ci}	
PSO-PI	0.51	0.209	0.87	0.341	3.96%
HHO-PI	0.81	0.11	0.91	0.089	2.72%
PSO_GA-PI	0.96	0.089	0.94	0.096	1.26%

The performance of grid-connected PV systems with different grid controllers is described in terms of efficiency, as shown in table 6.6. According to equation (6.6), The grid power is, $\frac{1}{2}\ V_g * I_g$. Where, V_g is the peak value of grid voltage, and I_g is the peak value of grid current. The dc power of the PV system can be obtained using equation (6.33).

$$P_{DC} = (V_{pv1} * I_{pv1}) + (V_{pv2} * I_{pv2}) + (V_{pv3} * I_{pv3}) \quad (6.33)$$

P_{DC} = (27.42*7.31) + (54.6*7.34) + (78.08*7.96) = 1222.72W

Table 6.6 Efficiency of the proposed GCSPV system with different controllers

Controller	Power from PV system (W)	Grid voltage V_g (V)	Grid current I_g (A)	Grid Power $\frac{1}{2}\ V_g * I_g$ (W)	% Efficiency
PSO-PI	P_{DC} = 1222.72	336.8	6.89	1160.28	94.89 %
HHO-PI		336.7	6.91	1163.33	95.14 %
PSO_GA-PI		336.7	6.96	1171.72	95.82 %

Also, the comparative analysis of different controllers with other topologies presented in the literature is presented in table 6.7. This comparative analysis shows that the proposed PSO_GA-based PI controller performs well with a low THD of 1.26% at 95.82% efficiency.

Table 6.7 Comparative analysis with other techniques proposed in the literature

Authors	Controller	Level of the inverter	% THD	% Efficiency
Bihari and Sadhu [176]	EANFIS	27	0.78%	-
	PI	27	18.19%	-
	PID	27	16.11%	-
Makhamreh et al [177]	MPC	7	3.45%	-
Satti and Hasan [178]	DMPC	7	2.7%	95.3%
Lakshmi and Hemamalini [179]	PI	3	3.32%	-
	FO-PI	3	2.62%	-
Dishore Shanmugam Vanaja et al [180]	HHO-PI	31	1.49%	94%
Proposed	PSO-PI	15	3.96%	94.89 %
	HHO-PI	15	2.72%	95.14 %
	PSO_GA-PI	15	1.26%	95.82 %

6.11 CHAPTER SUMMARY

The proposed 15-level asymmetric inverter on grid integration of an SPV system was explored in this chapter. A 1.25kW grid-connected SPV system had been modelled on the Simulink platform. The proposed grid-connected SPV system had been tested with various solar irradiance and temperature settings. For the suggested system to inject sinusoidal current into the grid, two voltage controllers were considered. The entire dc voltage of the proposed inverter was controlled by one controller, while the dc voltage of the corresponding dc sources provided by the PV array was controlled by the other. A PI controller was used to control the grid voltage and current under changing irradiance and variable temperature circumstances, which adjusted the needed gain to maintain constant grid voltage in all weather conditions. The THDs obtained

from PSO-PI, HHO-PI, and PSO_GA-PI controllers were 3.96%, 2.72% and 1.26% respectively. These comparisons concluded that the hybrid PSO_GA based PI controller gave a good response with less THD of 1.26% than other controllers. Also, the GCSPV system with the proposed inverter worked flawlessly, with an efficiency of 95.82% using a hybrid PSO_GA based PI controller.

CHAPTER-7

CONCLUSION & FUTURE SCOPE

7.1 CONCLUSION

This research proposed an optimized single-phase, 15-level asymmetric inverter for grid-connected PV systems. The inverter consists of two circuits, namely the primary circuit and the auxiliary circuit. The number of levels can be extended by adding the power switches in the primary circuit. The suggested topology was free of clamping capacitors and used a minimum number of switching diodes. The proposed inverter utilized 7-IGBTs, 3-diodes, and 3-power sources to reduce the design and control circuit complexity. The designed topology was compared and validated with existing literature for the number of switching devices, diodes, and DC sources required. Also, the topology gave its operation for a minimum number of commutations to reduce the power losses in the inverter. The THD and power losses are the two key metrics used to gauge the performance of the proposed asymmetric inverter.

The proposed inverter was operated in three different levels of operations such as 7-level, 11-level and 15-level with a suitable choice of dc sources like equal magnitude, unequal magnitude and binary approach respectively. A selective harmonic pulse width modulation (SHEPWM) had been employed to reduce the THD and power losses. The NR approach was used to solve the non-linear equations of SHEPWM. The THDs obtained are 15.36%, 11.17% and 7.3% for 7-level, 11-level and 15-level operations respectively using the NR approach. The results have concluded that the THD reduces as the number of levels in the inverter's output increases. However, the THD with this method is greater than 5%, which was not under the acceptable limits as per IEEE-519 standards.

The transient losses in the power switch substantially influence the performance of the power converter circuit in which they were employed. It was also crucial to thoroughly analyze power losses in multilevel inverters. The most prevalent losses in multilevel inverters were conduction and switching losses. Thermal modelling in PLECS, simple and precise curve fitting models in Simulink were used to analyze the power losses of a 15-level asymmetric inverter. The switching and conduction losses

are evaluated separately, considering junction temperature as 150^0 C and thermal impedance of 1.25 Ω. The foster thermal model was designed on PLECS for a 15-level inverter high-frequency switching (PDPWM) and low-frequency switching (SHEPWM). The inverter was simulated on PLECS with a 0.9 modulation index, and the efficiency with PDPWM was 97.38% and 97.99% using SHEPWM.

Furthermore, the precise Simulink curve fitting models were designed using SHEPWM. The model utilized exact voltage and energy curves as per the device datasheet. The inverter losses were found to be 1.044% of the total power delivered using SHEPWM control with an inverter efficiency of 97.96%. It was concluded that the efficiency of the proposed inverter is approximately the same as 97.99% using PLECS modeling and 97.96% using curve fitting models at the low switching frequency control method without employing the filter.

The total harmonic distortion (THD) of the inverter's output was reduced by optimizing the switching angles. SHEPWM is a selective harmonic elimination-based pulse width modulation (SHEPWM) developed using four traditional optimization algorithms: GA, PSO, WOA, and HHO, which give comparatively higher THD. Therefore, hybrid algorithms, such as EWOA, APSO-NR, PSO-GA, and HH-DE, were developed to solve the SHE equations. The THD produced from these approaches was relatively low compared to the IEEE-519 standards without filtering at the inverter's output. Compared to other optimizations, the THD of the proposed inverter is 5.34% at Nyquist frequency (5 kHz) and 1.78% at the harmonic frequency (1 kHz) with hybrid PSO-GA optimization. In addition, with EWOA optimization, the current THD is 2.5% at Nyquist frequency and 2.11% at the harmonic frequency. The obtained THD levels were within the permissible limits as governed by the IEEE-519 standards.

A 15-level asymmetric inverter was further implemented on a grid-connected solar photovoltaic system to test its performance under practical test conditions. Different solar irradiance and temperature conditions were used to evaluate the proposed grid-connected SPV system. A test case with an irradiance of 600 W/m^2 and a temperature of 35^0C was considered for the SPV system. A PI controller regulates the grid voltage and current under changing irradiance and variable temperature conditions, adjusting the required gain to maintain constant grid voltage in all-weather situations.

The gain values of PI controllers were optimized by using PSO, HHO and hybrid PSO-GA algorithms. The THDs were evaluated for grid current waveform, which is 3.96%, 2.72%, and 1.26% for PSO-PI, HHO-PI and hybrid PSO_GA-PI respectively. Also, the efficiencies were determined as 94.89% using PSO-PI controller, 95.14% using HHO-PI controller and 95.82%with PSO_GA-PI controller. The proposed GCSPV system performs admirably with a lower THD of 1.26% and higher efficiency of 95.82% with a hybrid PSO_GA-PI controller.

7.2 FUTURE SCOPE

In this work, the performance of the inverter was assessed under different input variations of PV sources to estimate the power losses and the efficiency and specified loads. To extend the research work presented in this thesis, future work can be considered in the following possibilities:

- The investigations can be extended to operate the inverter considering an array of renewable energy resources such as fuel cells, PV cells, wind energy, etc.
- By extending the concepts and procedures deduced in the thesis, the fault-tolerant capability of the MLI can be carried out.
- The performance assessment can be carried out by injecting reactive power into the grid. This further improves the efficiency of the inverter, but investigations are required into the lifetime of the inverter since the inverter's performance will degrade with the injection of reactive power.
- The real-time analysis can be carried out to validate the analytical results of the proposed work.
- The investigations can be extended to optimize dc-link voltage of designed multilevel inverter with input energy storage system under varying operating conditions.
- The proposed multilevel inverter topology can be applied for various stand-alone medium and high-voltage applications such as induction motor drive, FACTS devices, and HVDC applications.
- The suggested method can be extended to the three-phase systems.

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APPENDICES

A.1 PARAMETERS OF OPTIMIZATION ALGORITHMS

A.1.1 Parameters & specifications of genetic algorithm

Parameters	Values
Initialization of population	$\alpha_1 < \alpha_2 < \alpha_3 < \alpha_4 < \alpha_5 < \alpha_6 < \alpha_7 < \frac{\pi}{2}$
Population size	20
Generations	100
Creation function	Constraint dependent
Selection function	Roulette
Crossover function	Constraint dependent
Crossover fraction	0.6 as default
Number of iterations	200
Mutation rate	0.1
Generation gap	0.9
Modulation index	$0 < M \leq 1$

A.1.2 Parameters & specifications of PSO algorithm

Parameters	Values
Initialization of particles	$\alpha_1 < \alpha_2 < \alpha_3 < \alpha_4 < \alpha_5 < \alpha_6 < \alpha_7 < \frac{\pi}{2}$
Population size	50
Cognitive constant, C1	0.5
Social constant, C2	1.25
Inertia Weight, W	1
Maximum velocity	10
Number of iterations	200
Modulation index	$0 < M \leq 1$

A.1.3 Parameters & specifications of the whale optimization algorithm

Parameters	Values
Population size	20
Control coefficient a0	Linearly decreased from 2 to 0
Probability coefficient (p)	0.5
Convergence factor (a)	[0, 2]
Number of iterations	200
Mutation rate	0.0021
Dimensions	7
Lower boundary	$[0^0, 0^0, 0^0, 0^0, 0^0, 0^0, 0^0]$
Upper boundary	$[90^0, 90^0, 90^0, 90^0, 90^0, 90^0, 90^0]$
Modulation index	$0 < M \leq 1$

A.1.4 Parameters & specifications of harris hawk optimization algorithm

Parameters	Values
Number of Hawks ‘N’	30
Random generations r1, r2, r3, r4	In the range of [0,1]
Number of search agents	7
Initial energy (E_0)	[-1,1], [-1.0] loosing energy, [0,1] raising energy
Convergence probability ‘r’	0.5
Number of iterations	200
Lower boundary	$[0^0, 0^0, 0^0, 0^0, 0^0, 0^0, 0^0]$
Upper boundary	$[90^0, 90^0, 90^0, 90^0, 90^0, 90^0, 90^0]$
Modulation index	$0 < M \leq 1$

A.1.5 Parameters & specifications of the enhanced whale optimization algorithm

Parameters	Values
Population size	20
Control coefficient a0	Linearly decreased from 2 to 0
Probability coefficient (p)	0.5
Convergence factor (a)	[0, 2]
Number of iterations	200
Mutation rate	0.0039
Dimensions	7
Lower boundary	$[0^0, 0^0, 0^0, 0^0, 0^0, 0^0, 0^0]$
Upper boundary	$[90^0, 90^0, 90^0, 90^0, 90^0, 90^0, 90^0]$
Modulation index	$0 < M \leq 1$

A.1.6 Parameters & specifications of hybrid PSO-GA algorithm

Parameters	Values
Generations	100
Population size from	50
Initialization of population	$\alpha_1 < \alpha_2 < \alpha_3 < \alpha_4 < \alpha_5 < \alpha_6 < \alpha_7 < \frac{\pi}{2}$
Crossover fraction	0.8 as default
Number of iterations	200
Mutation rate	0.006
Cognitive constant, C1	0.5
Social constant, C2	1.25
Inertia Weight, W	1
Modulation index	$0 < M \leq 1$

A.1.7 Parameters & specifications of hybrid HH-DE algorithm

Parameters	Values
Number of Hawks 'N'	30
Random generations r1, r2, r3, r4	In the range of [0,1]
Initial energy (E_0)	[-1,1], [-1.0] loosing energy, [0,1] raising energy
Convergence probability 'r'	0.5
Number of iterations	200
Scaling factor	0.6
Crossover probability	0.5
Modulation index	$0 < M \leq 1$

A.1.8 Parameters & specifications of hybrid APSO-NR algorithm

Parameters	Values
Acceleration constant	2.0
Swarm size	100
Initialization of population	$\alpha_1 < \alpha_2 < \alpha_3 < \alpha_4 < \alpha_5 < \alpha_6 < \alpha_7 < \frac{\pi}{2}$
Maximum inertia	0.9
Minimum inertia	0.4
Number of iterations	200
Modulation index	$0 < M \leq 1$

A.2 SPECIFICATIONS AND PARAMETERS OF PV MODULE

Parameters		Specifications
Type of Module		User-defined
No of Parallel Strings		2
No of Series Strings	For PV source-1	1
	For PV source-2	2
	For PV source-3	4
No of Cells per Module		60
Maximum Power (W)		174W
Open Circuit Voltage V_{oc} (V)		36V
Short Circuit Current I_{sc} (A)		7A
Voltage at MPP V_{mp} (V)		29V
Current at MPP I_{mp} (A)		6A
Temperature Coefficient of V_{oc} (%/deg.C)		-0.36099^0C
Temperature Coefficient of I_{sc} (%/deg.C)		0.102^0C
Light Generated Current I_L (A)		7.0699A
Diode Saturation Current I_0 (A)		2.5449e-10A
Diode Ideal Factor		1.954
Shunt Resistance (Ω)		41.057Ω
Series Resistance (Ω)		0.41Ω

A.3 RELATIONSHIP BETWEEN DC INPUT POWER AND AC OUTPUT POWER IN PROPOSED INVERTER

In reality, while converting DC power to AC power, 50% of conventional losses are considered. The output power of the solar PV system is 1.5 times that of the inverter. The DC inputs are implemented using the inverter's output voltage. The relation between AC power from the inverter and dc power from the PV arrays is described by equation (A.1)

$$P_{AC} = \eta\, P_{DC} \quad \text{(A.1)}$$

Where η represents the conversion efficiency.

The equation (A.1) can be written in terms of PV parameters as follows;

$$P_{AC} = I_{rr} * A_m * \eta_m * \eta_i * \rho_{loss} \quad \text{(A.2)}$$

Where, I_{rr} is the irradiance of the PV panel (kWh/m^2), A_m is the area of the PV panel (m^2), $\eta_m$is the module efficiency = $\left(\frac{output\ of\ the\ PV\ module}{1000 * A_m}\right) * 100$, η_i is the inverter efficiency = $\left(\frac{P_{inv\ out}}{P_{inv\ out} + \rho_{loss}}\right)$, ρ_{loss} is the inverter power loss = $P_{cond} + P_{sw}$.

In the recommended grid-connected network, the dc power produced by a solar system should be kept constant, whilst the power transferred to the grid via the inverter changes over time. As a result, there is an imbalance between the dc input power and the ac output power. Capacitors are used in parallel with the solar network to correct this imbalance.

For the proposed 15-level inverter, the dc input power is represented with the equation (A.3),

$$P_{DC} = (V_{pv1} * I_{pv1}) + (V_{pv2} * I_{pv2}) + (V_{pv3} * I_{pv3}) \quad \text{(A.3)}$$

The power injected to the grid is,

$$P_{AC} = V_{AC} * I_{AC} = \frac{1}{2} VI\,(\cos\varphi) - \frac{1}{2} VI\cos(2\omega t + \varphi) \quad \text{(A.4)}$$

Taking the phase shift is equal to zero in equation (A.4),

$$P_{AC} = \frac{1}{2} VI - \frac{1}{2} VI\cos(2\omega t) \quad \text{(A.5)}$$

The first term in equation (A.5) represents the actual power output, and the second term represents the pulsating power, and its frequency is double the grid frequency. Assuming the inverter is lossless, the PV power is equal to the actual grid power, i.e., $P_{DC} = \frac{1}{2} VI$, therefore the equation (A.5) can be written as,

$$P_{AC} = P_{DC} - P_{DC}\cos(2\omega t) \quad \text{(A.6)}$$

Implementing decoupling capacitance reduces the distortions inherent in the pulsating power. An equation can be used to compute decoupling capacitance (A.7).

$$C_D = \frac{P_{DC}}{2\pi * f_{grid} * V_{DC} * \emptyset} \quad (A.7)$$

Where f_{grid} means the grid frequency of 50Hz, V_{DC} denotes the voltage across the decoupled capacitance, equal to the total PV voltage from individual panels of 336V, and denotes the voltage ripple across decoupled capacitance, which is very low and may be ignored.

A.4 COMPONENTS COMPARISON OF VARIOUS ASYMMETRIC MLIS WITH PROPOSED MLI FOR N-LEVELS

Type of Inverter	No of Switches	No of Diodes	No of DC sources	TSV (xVdc)
NPC	2(N-1)	N+1	(N-1)/2	2(N-1)
FC	2(N-1)	2(N-1)	N-1	2(N-1)
CHB	2(N-1)	2(N-1)	(N-1)/2	2(N-1)
MLDCL	N+3	N+3	(N-1)/2	3(N-1)
2CLHB	N+1	N+1	(N-1)/2	2(N-1)
CSMLI	N+1	N+1	(N-1)/2	2(N-1)
U-Cell	N+1	N+1	(N-1)/2	2(N-1)
2DCMLI	N-1	N-3	(N-1)/3	(N-1)/3
E-Type	5(N-1)/6	5(N-1)/6	(N-1)/6	10(N-1)6
[95]	(N-1)/4+4	(N-1)/4	(N-1)/4	(N-1)/2
[106]	(2N+1)/4+4	0	(N+1)/4	(2N+1)/2
[116]	(2N-1)/3+4	0	(N-1)/4	(N-1)/2
[146]	(N+1)/6	(N-2)/4	(N-1)/4	(N-2)/2
[149]	(2N-1)/4+4	(N-2)/4	(N-1)/3	(N-1)/2
Proposed	(N-1)/4+4	(N-1)/6	(N-1)/4	(N-1)/4

A.5 RATING AND SPECIFICATIONS OF PROPOSED INVERTER

Quantity	Rating/Specifications
Maximum AC power output at UPF	2500 W
AC voltage (nominal)	240 (RMS)
AC Voltage Range	228V – 252V
AC output frequency (nominal)	50 Hz
AC frequency range	49.4 Hz – 60.5 Hz
Maximum continuous output current	10.5A
Current THD	< 4%
Voltage THD	< 6%
Power factor	> 0.95
DC input voltage range	190V – 600V (V_{dc})
Maximum DC current	17.5A
Peak power tracking voltage range	190V – 550V (V_{dc})
Peak inverter efficiency	98%

LIST OF PUBLICATIONS

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1. **Devineni Gireesh Kumar**, Aman Ganesh (2019). Technological developments in direct grid-connected power converters for solar PV power plants. International journal of engineering and advanced technology. Vol. 9, No. 1, pp: 6604-6615, 10.35940/ijeat.A1857.109119 (Scopus Indexed).
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1. **Devineni Gireesh Kumar**, Aman Ganesh, and DSNMRAO (2021). Design and analysis of a novel cascaded 15-level asymmetric inverter using PSO and whale algorithms. International conference on sustainable energy and future electric transportation (SEFET), Hyderabad, India, 2021, pp. 1-6, doi:10.1109/SeFet48154.2021.9375752. (Scopus & Web of Science Indexed).
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BOOK CHAPTERS

1. **Gireesh Kumar Devineni**, Aman Ganesh, Neerudi Bhoopal & DSNMRAO (2021). THD optimization with low switching frequency control for 15-level reduced switch asymmetric multilevel inverter. Lecture notes in electrical engineering (Book Chapter). Vol. 795, chapter-9, pp.81-91. 10.1007/978-981-16-4943-1_9. (Springer – Scopus Indexed).