DESIGN OF HYBRID NEGATIVE CAPACITANCE FIELD EFFECT TRANSISTOR (HYB-NCFET) FOR LOW POWER VLSI CIRCUITS

Thesis Submitted for the Award of the Degree of

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Electronics and Communication Engineering

Submitted by

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DECLARATION

I hereby declare that the work being presented in this thesis report entitled **"DESIGN OF HYBRID NEGATIVE CAPACITANCE FIELD EFFECT TRANSISTOR (HYB-NCFET) FOR LOW POWER VLSI CIRCUITS"**, is an authentic record of my own work carried out in fulfilment of requirements for the award of degree of Doctor of Philosophy in Electronics and Communication Engineering at Lovely Professional University, Phagwara under the supervision of **Dr. Sanjeet K. Sinha**, Associate Professor, School of Electronics and Electrical Engineering and Co-supervision of **Dr. Sweta Chander**, Assistant Professor, School of Electronics and Electrical Engineering. The matter presented in this thesis has not been submitted elsewhere in part or fully to any other University or Institute for the award of any degree.

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This is to certify that Amandeep Singh (Registration Number: 41800068) has completed objective formulation of his thesis titled, "**DESIGN OF HYBRID NEGATIVE CAPACITANCE FIELD EFFECT TRANSISTOR (HYB-NCFET) FOR LOW POWER VLSI CIRCUITS**" for the award of degree of Doctor of Philosophy in Electronics & Communication Engineering at Lovely Professional University, Phagwara under my guidance and supervision. The matter presented in this thesis has not been submitted elsewhere in part or fully to any other University or Institute for the award of any degree.

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LIST OF SYMBOLS

C_d	Depletion capacitance
V_{TH}	Threshold voltage
C_{in}	Intrinsic capacitance
C_{ox}	Oxide capacitance
C_{eq}	Equivalent capacitance
C_S	Channel to Source Capacitance
E_{DE}	Depolarization field
C_{MOS}	Semiconductor Capacitance
C_{FE}	Ferroelectric Capacitance
fs(E)	Fermi-Dirac distribution function
v(E)	Velocity of carriers
D(E)	Density of state
EFs	Fermi energy level at source
T	Temperature
k	Boltzmann constant
T_{FE}	Fe material thickness
L_{CH}	Channel length
ρ	Internal resistivity
I_{ON}	On current
I_{OFF}	Off/Leakage current
I_{ON}/I_{OFF}	Current Ratio
V_{ds}	Drain to Source Voltage
V_{DD}	Drain Voltage
α, β, and γ	Landau constants
P	Electric polarization
E_x	Transverse field
E_y	Longitudinal Field
V_{PT}	Punch through voltage
FL	Ferroelectric layer
DL	Gate dielectric layer
e	Electronic charge
Q_g	Gate charge
Q_d	Drain charge
Q_b	Base charge
Q_s	Source charge
Q_{acc}	Accumulation charge
Q_{inv}	Inversion charge
Q_{dep}	Depletion charge
Q_{dep0}	Depletion charge at zero drain bias
V_{FB}	Flat band voltage
h	Reduced planck's constant
q	Coulomb's charge
W_{active}	Width of channel

L_{active}	Length of channel
A_{bulk}	Effective Area
m_r	Average effective mass
m_c	Effective mass of electrons in conduction band
m_v	Effective mass of electrons in valence band
V_{FE}	Voltage across ferroelectric material
G	Gibb's energy
$E_{barrier}$	Potential across barrier
V_{ox}	Voltage across oxide layer
A_v	Voltage amplification
P_r	Remnant polarization
E_c	Coercive field
V_{gtfet}	Gate voltage of conventional TFET
V_{eff}	Effective voltage across the heterojunction
N_A	Source doping
N_I	Channel doping
N_D	Drain doping
T_{OX}	Oxide Thickness
L_{SOV}	Source gate overlap length
L_{GUL}	Gate drain underlap length
g_m	Transconductance
g_d	Output Transconductance
g_{m2}, g_{m3}	Higher order transconductances
T	Temperature
N_t	Interface trap density
C_{gd}	Gate-drain capacitance
C_{gs}	Gate-source capacitance
f_T	Cut-off frequency
τ	Transit time
V_{in}	Input Voltage
V_{out}	Output Voltage
S_{ID}	Drain current noise spectral density
S_{vg}	Voltage noise spectral density
λ	Tunneling parameter
f	Frequency
V_{G1S}	Voltage across gate 1
V_{G2S}	Voltage across gate 2

LIST OF ABBREVIATIONS

CMOS	Complementary Metal Oxide Semiconductor Field Effect Transistor
VLSI	Very Large Scale Integration
FET	Field Effect Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
TFET	Tunnel Field Effect Transistor
SS	Subthreshold Swing
FinFET	Fin Field Effect Transistor
DIBL	Drain induced barrier lowering
BTBT	Band to Band Tunnelling
NCTFET	Negative Capacitance Field Effect Transistor
LK Equation/Model	Landau-Khalatnikov Equation/Model
PZT	Lead Zirconate Titanate
P(VDF-TrFe)	Poly(Vinylidene Fluoride-trifluoroethylene
SBT	Strontium Bismuth Tantalate
$BaTiO_3$	Barium Titanate
HZO/ HfO_2	Hafnium Oxide
SiO_2	Silicon Dioxide
CNTFET	Carbon Nanotube Field Effect Transistor
TTL	Transistor Transistor Logic
LTFET	Lateral Tunnel Field Effect Transistor
VTFET	Vertical Tunnel Field Effect Transistor
EOT	Effective oxide thickness
UTBB	Ultra-thin body and ultra-thin insulator
SG-FET	Suspended gate FET
Fe-FET	Ferroelectric FET
ADC	Analog to digital converter
PLLs	Phase locked loops
VTC	Voltage to time converter
IF	Interfacial
BOX	Buried Oxide
InAs	Indium arsenide
GaSb	Gallium antimonite
InGaAs	Indium gallium arsenide
GaAsSb	Gallium arsenide antimonite
Zr-doped HfO_2	Zirconium doped Hafnium Oxide
GAA-TFET	Gate All Round Tunnel Field Effect Transistor
S_{ID}/I_D^2	Normalized power spectrum density
LTFET	L-shaped tunnel field effect transistor
QCE	Quantum confinement effect
GDU-LTFET	Gate drain underlap LTFET
SM	Sense Margin
RT	Retention time
VB	Valence Band
CB	Conduction Band
DRAM	Dynamic random access memory
SRAM	Static random access memory
m-factor	Body factor
n-factor	Transport factor

NEGF	Non-energy green function
sde	Sentaurus Structure Editor
sdevice	Sentaurus Device
MATLAB	MATrix LABoratory
HD2, HD3	Linearity Parameters
IIP3	Third order intercept point
GBP	Gain bandwidth product
TFP	Transconductance frequency product
TGF	Transconductance generation efficiency
GFP	Gain frequency product
GTFP	Gain transconductance frequency product
VTC	Voltage transfer characteristics

ABSTRACT

Complementary Metal Oxide Semiconductor Field Effect Transistor (CMOS) is a major switching element in most of the Very Large Scale Integration (VLSI) circuits but with the rapid scaling of CMOS in nanometer regime, the performance and power dissipation of CMOS is limited by short channel effects like drain induced barrier lowering (DIBL) and higher subthreshold swing (SS), which in turns increases the leakage current. This miniaturization of CMOS is due to scaling of device parameters as per Dennard's rule of scaling. Due to intervention of short channel effects, the transition of CMOS from OFF state to ON state becomes difficult while lowering supply voltages. The main reason behind the same is physical limitations of Metal Oxide Semiconductor Field Effect Transistor (MOSFET). In Metal Oxide Semiconductor Field Effect Transistor the current flows by thermal injection of electrons. To overcome the limitations of conventional MOSFET, Researchers are now looking for the possibility to replace the conventional MOSFET with an alternative device with better electronic and mechanical properties, compact size and lesser power consumption. Moving from bigger transistors to the smaller ones, so as to reduce the short channel effects, various device architectures have evolved with ultra-thin body and capability to operate below 60 mV/decade (fundamental limit).

With various engineered device structures, the current CMOS technology has achieved a sub threshold slope of less than 60 mV/decade but the supply voltage has not been achieved below 1 V. Tunnel Field Effect Transistor (TFET) is a promising alternative to conventional MOSFET due to its capability to achieve steeper subthreshold swing and reduce the supply voltage below 0.5 V. The current transport mechanism in TFET is Band to Band Tunnelling (BTBT) instead of thermal injection/point tunnelling. Thus TFETs can replace conventional MOSFETs in low power applications. The shortcomings of putting TFETs into practical applications is lesser I_{ON} current and ambipolar behaviour. These things degrades the performance of TFET but can be controlled by choosing the materials wisely and doing certain structural modifications of the device. Double gated TFET structures with high-k dielectric, addition of pocket layers at source, making heterojunction at source channel junction, changing doping concentration of source material are some alterations done in conventional TFETs to enhance ON current and reduce the ambipolar behaviour by many folds. Heterojunction device structures have also been presented in literature that subsequently improvises the ON current of the device as effective band gap reduces which in turns increases the band to band tunnelling. Different materials

reported in the past are InGaAs, InP, GaAsSb, InAs etc. Device structures implemented using these materials have been successful in replacing conventional MOSFETs in many low power applications. The other limitation of TFET Structure is the ambipolar current. As in TFET, drain and source are oppositely doped so if a positive gate to source V_{GS} is applied, tunnelling will occur at the gate-source junction. But if negative voltage is applied, then tunnelling will occur at drain junction as well. Thus the leakage current will increase, which in turns is the main reason of ambipolar behaviour. To overcome this shortcoming, various device structures have been tried up, such as gate-drain overlap, low-drain doping etc and these have been successful in reducing the ambipolarity in TFETs while compromising on ON current of the device. The strongest candidate that has emerged as best solution to the stated problems is negative capacitance field effect transistor (NCFET). With the intervention of a ferroelectric layer at gate stack of TFET, ON current is enhanced along with making subthreshold swing (SS) super steep. Thus, Negative Capacitance Tunnel Field Effect Transistor (NCTFET) has a great potential in overcoming the limitations of TFETs and replacing them in low power VLSI applications. It has been seen that various device structures like T-Shaped, U-Shaped, F-Shaped TFETs have been reported in literature. Based on the new age device structures and phenomenon adopted, a raised source gate overlapped NCTFET device have been structured and reported in this work. In proposed device, Ge material is used as source material to form a heterojunction at source-channel junction and a 3nm thick $BaTiO_3$ Fe material layer is stacked over HfO_2 layer to form a gate stack of NCTFET. The proposed device is capable of achieving 53.7 mV/decade subthreshold swing and I_{ON}/I_{OFF} current ratio of $7.14x10^{+9}$. Moreover, in comparison to the conventional device, DIBL calculated for conventional NCTFET is 61.2 mV/V and for proposed NCTFET is 31.92 mV/V. So DIBL improvement of 47.8% has been achieved. The proposed device is then analysed and compared with conventional device in terms of AC performance, DC performance and Linearity. Noise analysis has clearly depicted that the proposed device structure has lesser effect of noise as compared to other devices. Nonetheless, S_{ID} is inversely proportional the frequency, reduced values of noise is observed at high frequency than at low frequency. The device is further optimized and put to use in circuit applications by making an inverter and 1-T dynamic random access memory. The devices so formed are then compared with conventional devices in terms of power consumed. It has been observed from the result that the proposed NCTFET inverter can be put to use in practical applications to replace conventional MOSFET.

CHAPTER 1: INTRODUCTION

With the advancement in technology and new insights of MOSFET fabrications, power consumption in VLSI circuits has been optimized to a greater extent. However, with the increase in density and compactness of transistors, subthreshold swing (SS) becomes higher than (60mV/dec) and leakage current also increases for a constant I_{ON}. MOS transistor have been scaled to nanometer feature size so as to make it compact and power efficient. According to Moore's law, silicon-based technology has grown so much and has facilitated the fabrication of power efficient yet faster devices. But, nowadays MOSFET is approaching towards the lower limit in context to feature size [1]. Shrinking the length of MOSFETs gate in nanometer regime, introduces several critical issues and reliability problems such as reduced channel control, introduction of short channel effects, more leakage current and more-power consumption etc. The most common trend for lowering power consumed by VLSI circuits is to alter the supply voltage. But after the specific value, the threshold voltage of MOSFET hinders the further lowering of supply voltage [2]. The threshold voltage of MOSFET used in designing of circuit is the lower limit, voltage supplied must at least be equal to or greater than the threshold.

While reducing feature size of transistors, various unwanted problems have introduced, these are referred as short channel effects like higher subthreshold (SS), reduced I_{ON}/I_{OFF}, drain induced barrier lowering, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Carrier Injection are some of the short channel effects that increases the leakage current and makes SS higher. The researchers are working towards finding an alternative device in nanometer regime to replace the conventional MOSFET without compromising on performance. With day by day scaling of MOSFET, traditional semiconductor devices have led researchers to look into other alternative devices like Carbon Nanotube Field Effect Transistor (CNTFETs), Carbon Nano Wire Field Effect Transistor (CNWFET), Tunnel Field Effect Transistor (TFET), etc. [3]. Tunnel Field Effect Transistor (TFET) is an emerging alternative to the conventional MOSFET because of its capability to deliver stepper subthreshold swing and reduce the supply voltage below 0.5 V. The mechanism used to move charge carrier in TFET is Band to Band Tunnelling (BTBT) instead of thermal injection/point tunnelling. Thus, TFET device can be a good replacement over conventional MOSFET for low power applications [4].

1.1. CMOS Scaling

For denser and faster integration of VLSI chips, the CMOS scaling has been in trend for the past decades. If we compare the present age transistors with the ones that were manufactured 20 years ago, present age transistors are twenty times faster and have area lesser than 1%. Over the last two decades, the speed of system and number of transistors per chip have improved exponentially. With the continues shifting of technologies towards nanometer regime, the feature size is decreasing, the speed is improving and the power consumed for one transition event is decreasing.

During early 1970s, Mead and Dennard have figured out that there exists a need for scaling basic MOS transistor to smaller physical dimensions. They developed a theory named "Photocopy reduction" to reduce the channel length in CMOS technology. The originally formulated scaling theory was Constant Field Scaling, i.e. with the shrinking of dimensions, the field range in MOSFET remains the same over the different generations. In 1980s, with the development of 5V power supply (being compatible with TTL logic), the previously used field scaling has been changed to constant voltage scaling. In this scaling, the field was not remaining same, but inside the generation it increases with very new generation till early 1990s. Moore's law states that the number of transistors in a chip doubles every two years. This was named after Gordon Moore, co-founder of Fairchild Semiconductors and Intel.

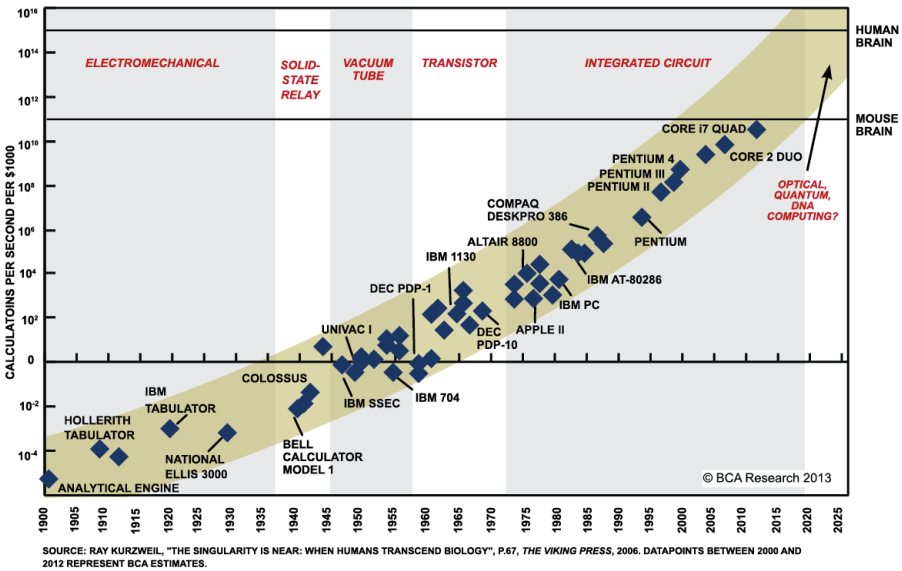


Figure 1.1: Moore's Law [5]

1.2. Short Channel Effects in MOSFETS

To achieve a better performance in processors and memory units, scaling of transistors is must but with the reduction of channel length, this performance and power consumption is limited by certain short channel effects like drain induced barrier lowering (DIBL) and higher subthreshold swing (SS), which in turns increases the leakage current [6]. As the channel length is lowered for a given doping concentration, the depletion width of drain and source junctions becomes comparable to channel length. Thus, the potential distribution becomes dependent on both transverse and longitudinal fields. E_x (transverse field) is controlled by back-surface bias and gate voltage and E_y (Longitudinal Field) is controlled by drain bias. Hence, the potential distribution becomes 2-D and results in the degradation of threshold behaviour. Following are the various short channel effects in MOSFETs:

1.2.1. Mobility Degradation

This effect is seen due to limited mobility of charges carriers (electrons and holes) in MOSFET and is dependent on following two effects:

1.2.1.1. Lateral Field Effect

As the lateral field is increased in case of short channels, the field applied directly controls the channel mobility and with increase in field the velocity saturation occurs. This results in current saturation.

1.2.1.2. Vertical Field Effect

On shrinking the channel, the vertical field also increases, hence there occurs the scattering off carriers near the surface which in turns reduces the surface mobility.

1.2.2. Drain Induced Barrier Lowering (DIBL)

With continuous scaling, source and drain are been fabricated closer, the depletion region intrudes into the channel even without biasing. This effect is called charge sharing, as source and drain controls the channel charge instead of gate. With the expansion of drain depletion region by increasing biasing, it interacts with the source channel junction and in turns reduces the potential barrier which is named as Drain Induced Barrier Lowering (DIBL) [7]. Thus, the electrons are easily injected into the channel and there exists no control of V_{gs} over I_D.

1.2.3. Drain Punch Through

A similar effect like DIBL is seen when the drain voltage is increased to a certain level, such that the depletion region of drain extends to the source and current flows independently from gate voltage. This condition is called as Drain punch through condition and is defined by punch through voltage (V_{PT}):

$$V_{PT} = qN_aL^2/2E_s \quad (1.1)$$

Where L is channel length, with the decrease in L, the punch through voltage rapidly decreases.

1.2.4 Boltzmann's Tyranny

For faster switching devices, a stepper transition is required to turn the device from OFF state to ON state rapidly. An ideal MOSFET switch should be capable to transit between these two states smoothly and abruptly. The rate at which current changes with applied voltage is dependent upon thermal current transport across the source-channel barrier. Subthreshold swing is the parameter associated with the degree of abruptness of transition from OFF to ON state and vice versa.

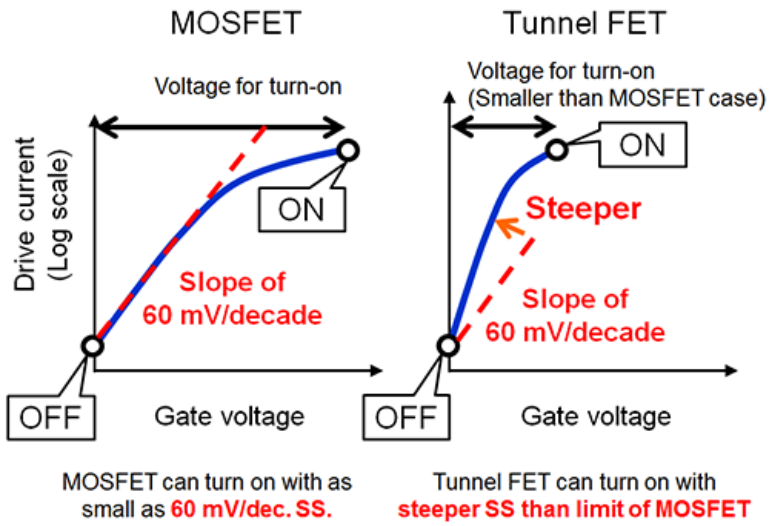


Figure 1.2: Subthreshold swing in case of MOSFET and TFET [8]

There exists a limitation on subthreshold swing to be lower than 60 mV/decade as a result of Boltzmann's distribution of electrons, which in turns is responsible for high power consumption of MOSFETs. The new age device structures work on altering the device to break the theoretical limit of "Boltzmann Tyranny".

1.3. New age FET Devices

As discussed in previous sections, with the continuous scaling of VLSI devices, there arises various short channel effects in conventional MOSFET. In practical circuit applications, certain limitations also exist in terms of thermal injection mechanism of current transport in MOSFET, inability of sharp doping profile etc. Hence, these shortcomings make conventional MOSFETs unsuitable for use in nanometer regime at 10 nm or lower. Thus, researchers are now looking for various alternate FET structure to replace the conventional MOSFET and release novel ideas that overcome the listed limitations and obtain an improvised device performance. TFET is a strong contender in this race which provides higher I_{ON}/I_{OFF} ratio with steeper sub-threshold swing [9]. Moreover, due to band to band tunneling mechanism, it capable of a) cutting high fermi energy tail, b) lower I_{OFF}, c) dependence of I_{ON} on tunneling width and area. These benefits of using TFET helps in lowering subthreshold swing which further downscales the threshold voltage. Hence TFET is a strong candidate for replacing the conventional MOSFETs in low power applications.

1.4. Concept of Negative Capacitance in FETs

Negative capacitance (NC) FETs fabricated using Hafnium-based ferroelectric material stacked with a conventional MOSFET overcomes the physical limitation and possesses a steeper sub-V_{TH} swing (SS) lesser than the physical limitation (60 mV/decade). First reported in 2007 by Giovanni, Negative capacitance associated with Fe layer is the main factor of low SS swing in Fe-FET transistors. Moreover, it provides high I_{ON}/I_{OFF} and ample voltage amplification; with particular selection of ferroelectric material to form gate stack [10]. By incorporating a thin layer of ferroelectric material with High-k dielectric for making gate stack (Inspite of gate of a standard MOSFET), it is feasible to overcome the physical subthreshold limit (i.e. 60mV/decade) at room temperature.

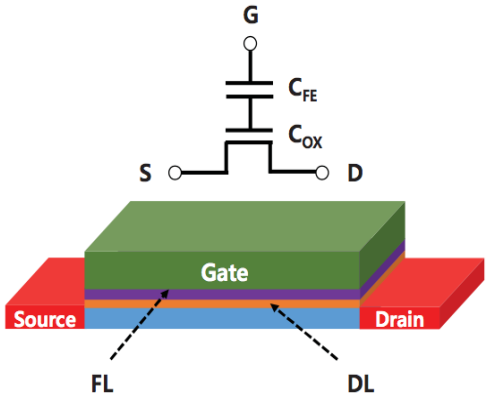


Figure 1.3: Device Structure of Negative Capacitance FET (NCFET)

In above figure, Ferroelectric material is adopted as the Ferroelectric layer FL which brings Negative capacitance effect on gate dielectric layer (DL). Negative Capacitance devices can become one of the most promising alternatives with steep SS slope and can be utilized in low-power applications [11].

Negative capacitance field effect transistor (NCFET) is a promising alternative to baseline Metal oxide field effect transistor. In NCFET, a Fe layer is merged with the gate stack on top of gate oxide, thus making total capacitance makes a series combination of C_{OX} and C_{FE}. This ferroelectric layer added to the conventional MOSFET's gate oxide provides voltage amplification that results in a stepper subthreshold swing compared to the baseline MOSFET. Different ferroelectric materials give different device characteristics and subthreshold slope values at room temperature, thus the overall analysis at device level requires proper investigation and study [12].

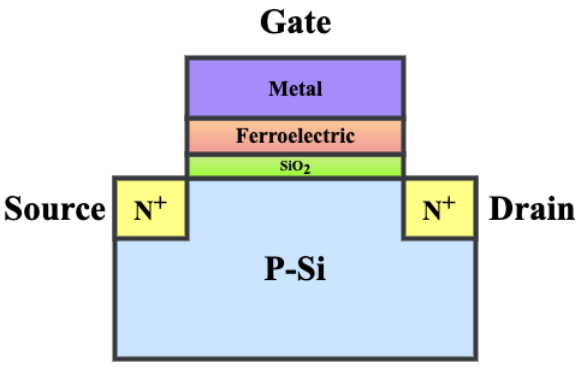


Figure 1.4: Schematic Diagram of Negative Capacitance Field Effect Transistor (NCFET)

Voltage-charge characteristics for Ferroelectric materials can be defined by Landau-Khalatnikov (LK) equation, that states:

$$V_{FE} = T_{FE}\,(\rho^{\frac{dP}{dt}} + 2\alpha P + 4\beta P^3 + 6\gamma P^5)\ (1) \qquad (1.2)$$

Where T_{FE} is ferroelectric thickness, ρ is internal resistivity, P is electric polarization, {α,β,γ} are landau expansion coefficients.

Since, negative capacitance becomes a part of the insulating layer capacitance hence it is added in series to the gate capacitance. Therefore, by this the overall capacitance of series combination is increased which in turns makes the sub threshold swing steeper and its value is reduced below the minimum limit of 60 mV/decade [13].

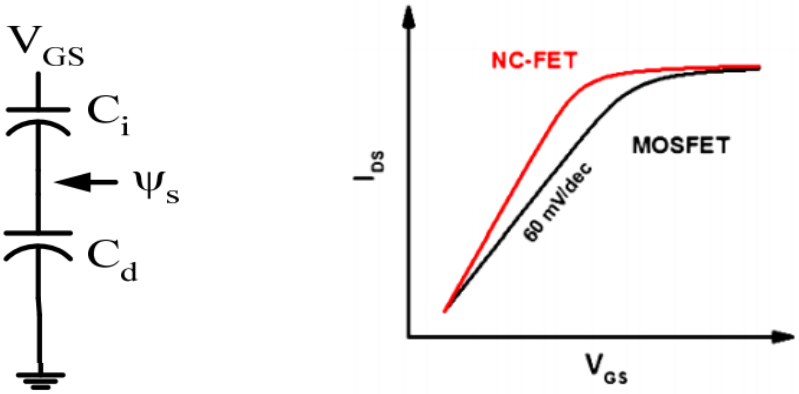


Figure 1.5: a) Capacitance Model [26] b) Comparison of SS for NCFET and Conventional MOSFET

The I_{ON} of the device so formed can reach as high as supply voltage that may be reduced considerably and the transport dynamics are not altered for the transistor. So, the negative capacitance FET acts as a low voltage device without compromising on the switching capability.

The above diagram shows the series combination of two capacitors, one is C_d (i.e. positive) and another is C_i (i.e. negative). Both are connected in series and the equivalent capacitance of the combination can be given as:

$$C_{eq} = \frac{|Ci|Cd}{|Ci|-Cd} \qquad (1.3)$$

Since, the positive capacitance depends on the applied voltage, so it should have no charge when the voltage applied is zero. This condition also confirms the ferroelectric material should also be biased at Q=0, at zero bias voltage, i.e. with negative capacitance [14].

It can be seen that for $C_i > C_d$, which is usually the case, the equivalent capacitance will be greater that both capacitances, C_i and C_d. But we know that in series combination of capacitors,

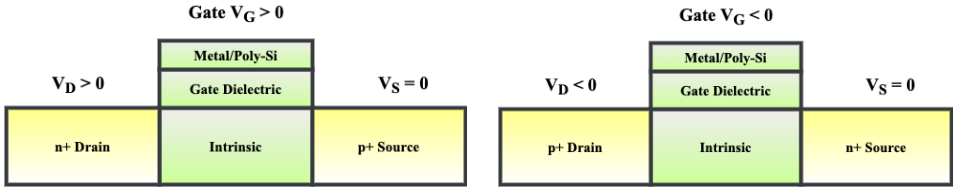
the equivalent capacitance is always smaller that the smallest capacitance. With overall capacitance to be greater that the individual capacitors, there is a possibility of storing more charge with the same gate voltage or alternatively we can say that the supply voltage can be reduced to obtain similar quantity of charge in the channel. So, this is the unique property of NCFET in comparison to normal capacitances that can be utilized in low power applications [NITJ]. The working of NCFET mainly depends on the phenomenon of "Capacitance matching". In terms of capacitance, SS can also be written as:

$$SS = 60 \times [1+\frac{CMOS}{CFE}] \quad (1.4)$$

Where series combination of oxide capacitance (C_{OX}) and channel to source capacitance (C_S) forms C_{MOS} and C_{FE} is the capacitance of ferroelectric material. There are two main requirements of capacitance matching to pull down SS below 60 mV/dec. First one is that C_{FE} should be negative and Second one is C_{FE} should be greater or equal than C_{MOS} [15].

1.5 Tunnel Field Effect Transistor

Tunnel field-effect transistor (TFET) is promising solution for replacing MOSFET as a switch for future logic implementations. However, due to lack of tools available for device fabrication and design constraints of moderate tunnel junction, TFET are face challenges in making the subthreshold slope (SS) steeper, which is directly associated with the power consumption, and channel control. In tunnel FETs, BTBT of carriers acts as a major carrier injection phenomenon across reverse biased PN junction. There are certain drawbacks like low I_{ON} and higher SS, which hinders the replacement of conventional MOSFET with tunnel FET in low power circuits. To overcome these drawbacks, Tunnel FET is engineered in various topologies depending upon gate electric field (V_{gs}) and tunneling junction field. Having capability to operate at Subthreshold swing lesser than 60 mV/dec and offering high I_{ON}/I_{OFF} at decreased supply voltages, TFET can be put to practical power applications.



(a) (b)

Figure 1.6: Biasing conditions of (a) n-TFET (b) p-TFET

Figure 1.6 shows the biasing conditions of n-TFET and p-TFET. It can be seen that for n-TFET the positive gate voltage is required to turn on the device. With the use of heterojunction, I_{OFF} is very low compared to MOSFET, thus it further reduces the static and dynamic power dissipation. The only problem that persists with TFET is its lesser I_{ON} current and ambipolar behavior that can be controlled by choosing the materials wisely and doing some structural modification of the device [15-16]. Further, by intervention of a ferroelectric material at gate stack of TFET, I_{ON} current is enhanced along with making Subthreshold swing (SS) super steep. So, with ferroelectric material being added to the gate stack of TFET, faster switching with enhanced I_{ON} current is achieved. Thus, Negative Capacitance TFET (NCTFET) has a great potential for low power applications in VLSI domain.

1.6 Subthreshold Swing in TFETs

Subthreshold swing is an important parameter associated with TFETs that makes it different from the conventional MOSFETs. It is calculated as inverse of subthreshold slope. In transfer characteristics of the device, subthreshold slope is found as the straight-line approximation of the subthreshold current, and is expressed as decades/mV.

In conventional MOSFET, with application of gate voltage, the charge carriers transport from source to drain region due to thermal injection. Charge carriers having energies greater than Φmax will be responsible of current near the subthreshold zone. Below expression gives the relationship between drain current and Electron Energy (E), Fermi-Dirac distribution function fs(E), velocity of carriers v(E), density of state D(E).

$$I_d \propto \int dE.D(E).v(E).f_S(E) \tag{1.5}$$

A Boltzmann approximation can be used to derive the source Fermi–Dirac distribution function fs(E) in the exponential tail region:

$$f_s(E) \approx \exp\left(-\frac{E - E_F^s}{kT}\right) \tag{1.6}$$

In the above equation, EFs represents Fermi energy level at the source, T denotes the temperature and k represents the Boltzmann constant. The product of $D(E) \times v(E)$ can be considered as the constant for simplicity purpose, assuming just one spatial direction of transport [17]. Likewise, it can be assumed for a MOSFET that whenever the gate to source voltage changes, there would be shift in the conduction band. Thus, it can be written:

$$\frac{\partial I_d}{\partial V_{GS}} = |e| \frac{dI_d}{dE} \tag{1.7}$$

where *e* represents the electronic charge. Using Equation (1.6) and Equation (1.7), in an ideal MOSFET, the subthreshold swing can be calculated as:

$$SS = \left(\frac{\partial \log(I_d)}{\partial V_{GS}}\right)^{-1} = \ln(10)\left(\frac{1}{I_d}\frac{\partial I_d}{\partial V_{GS}}\right)^{-1} \approx \ln(10)\frac{kT}{e} \tag{1.8}$$

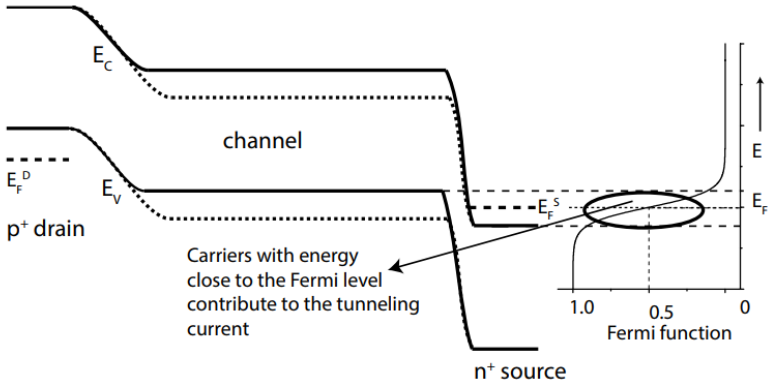


Figure 1.7: Band diagram at subthreshold region of p-type TFET at two different gate voltages [30].

The energy band diagram in subthreshold region of a p-TFET, at two separate gate voltages is shown in Figure 1.7. The holes would tunnel into the channel, whenever a negative gate voltage is given, as at source, the channel is drawn above conduction band. If the valence band is lower than the conduction band, no tunnelling occurs. The channel prevents carriers from tunneling with energy in the Fermi–Dirac distribution's high-energy tail [18]. The Fermi–Dirac distribution's low-energy tail is cut off at the source contact by the semiconductor bandgap. When the channel's valence band gets aligned with source's conduction band, BTBT is activated, causing the state to switch from OFF condition to ON state abruptly.

1.7 Ambipolar Current in TFETs

The undesired tunneling at drain-current junction is the main cause of ambipolarity in TFET device when the applied voltage at gate is reversed. Ambipolar behavior of TFET is a grave concern as this unwanted leakage limits it to be used for practical circuit and devices. Device improvisations have been reported in literature to suppress this ambipolarity in TFET structure. Some of methods suggested in the literature [17], [19] are:

1. Material used in channel and drain region can be altered to control the tunneling of charge carriers from the VB of channel to CB of drain, on application of negative gate bias. This method significantly suppressed the ambipolarity. The only challenge in this modification is that there occur lattice mismatch issues while using different materials and the cost of device also shifts to a higher end while using material other than silicon.

2. Doping profile also plays an important role in controlling the tunneling and using gaussian drain doping profile helps in reducing ambipolar behavior of the device. The only challenge in this method is the complexity involved in the fabrication. So, this solution can be used in case of dopingless devices.

3. Work function of gate and dielectric can also be helpful in reduction of ambipolar behavior of the device.

So, to use the TFETs in practical circuits, ambipolar conduction needs to be suppressed in a significant manner.

The devices discussed in this chapter play a very vital role to overcome the problems associated with MOSFET in nanometer regime, with arising short channel effects (due to scaling). Moreover, with the adoption of new age phenomenon i.e. negative capacitance field effect the device performance can be further improvised in terms of steeper subthreshold swing and better current ratio.

CHAPTER 2: LITERATURE REVIEW AND PROBLEM FORMULATION

2.1 Introduction

With the advancement and rapid scaling of largescale integrated circuits, the power consumption of the fabricated chips is increasing gradually. The scaling limitations (intervention of short channel effects) of current MOSFET technology is forcing researchers to look for different alternative options to replace conventional MOSFET. Tunnel Field Effect Transistors (TFETs) has emerged as strong candidate in replacing MOSFET as they are successful in achieving a stepper sub threshold swing at room temperature due to Band to Band Tunneling (BTBT) mechanism [20]. There exists various structures and improvising techniques in making TFETs a strong contender to replace conventional MOSFETs in low power applications. Next section discusses the various device structures and techniques reported in literature for boosting I_{ON} current and making sub-threshold swing steeper.

2.2 Improvisations Reported in Literature for Tunnel Field Effect Transistors

TFETs have been successful in attaining low I_{OFF} current and steeper sub-threshold slope due to BTBT mechanism, but there exist certain drawbacks of TFETs. Firstly, TFETs yields low I_{ON} current that needs to be boosted. The I_{ON} can be increased with structural modification by altering the positioning of gate stack by overlapping it towards source side. This can be overcome by including a layer of ferroelectric high-k material in gate stack of TFET. By the intervention of Negative capacitance in series with gate stack will improvise the performance and makes the power dissipation lower [21]. The negative capacitance is implemented practically by the series combination of a ferroelectric capacitor (being operated in NC Region) with a positive capacitance to stabilize the Negative capacitance. By including a negative capacitor in the gate stack, the total capacitance of series combination becomes larger than the conventional value i.e. lesser value of supply voltage is required to obtain same I_{ON} current [22]. Thus, the unique property of ferroelectric materials is used to lower the voltage amplification factor so that SS can be pulled down below 60 mV/dec. Secondly, the ambipolar behaviour, band to band tunneling at channel and drain junction, makes the off-state leakage current higher

due to existence of unwanted electric field at channel drain junction [23]. Few common solutions adopted by the researchers for improving the device performance of TFETs are using thinner body, strong doping profile, high source doping, high-k gate dielectric, thin dielectric etc.

2.3 Literature Survey

Various device structures and improvisations have been reported in literature to overcome the drawbacks of conventional TFET listed in previous section.

Giovanni et al. has demonstrated the integration of a thin ferroelectric layer in the gate stack of a conventional MOSFET for the very first time. The results show that the device formed has overcome the fundamental limit of Subthreshold swing and achieved 13 mV/decade SS in Fe-FETs with 40 nm P(VDF-TrFe)/SiO_2 gate stack. Negative capacitance of ferroelectric layer acts as voltage amplifier and helps in achieving better results in terms of current ratio and SS at lesser supply voltage [24].

S. Salahuddin et al. has introduced the concept of negative capacitance onto the conventional MOSFET devices for the very first time and has reported the ability of this phenomenon in breaking the subthreshold swing's fundamental limit of 60mV/decade at 300K temp. The replacement of standard insulator layer with ferroelectric material has affected the power consumption and current conversion of the device [25]. The gate stack so formed can be viewed as step-up transformer which amplifies the gate voltage which in turns is responsible for making the value of SS swing lower than 60mV/decade and provides low voltage/low power operation.

J. David et al. presented a comprehensive physics model for surface potential and drain current. The model reported in this work helps in figuring out the ability of negative capacitance field effect transistors for low power applications. Moreover, this work provides an insight to experimentally validate the operation of NC region in newly reported NCTFET structures [26].

A. I. Khan et al. worked on defining a design methodology of ferroelectric negative capacitance FETs (NCFETs) based on capacitance matching. Antiferroelectric model presented in this work can significantly reduce the subthreshold swing below the fundamental limit of 60mV/decade, plus it also boosts the on-current with trade off of nominal hysteresis. The effect of Fe thickness, Effective Oxide Thickness (EOT), Source/drain Overlap etc is also studied and analysed. It has been seen that there are visible differences in device characteristics with the intervention of negative capacitance [27].

C.W. Yeung et al. has presented an Ultra-thin Non-hysteresis Negative Capacitance Field Effect Transistor (NCFET) implemented on ultra-thin body and ultra-thin insulator (UTBB) platform. The authors have demonstrated the relationship between negative and positive capacitance and it has been concluded that to break the fundamental limit on subthreshold slope, the negative capacitance should be lesser than the gate oxide capacitance and should be greater than the total MOSFET capacitance within the operating voltage [28].

A. Jain et al. explained the constraints and hysteresis free operation associated with negative capacitance field effect transistors. The authors have also provided the general algorithm for calculation of subthreshold swing and compared the results to figure out the improvisations as applied to suspended gate-FET (SG-FET) and ferroelectric FET (Fe-FET) with constant channel capacitance. The observations made in this work has highlighted the need of optimizing C_{eq} to improvise the subthreshold swing further. The values of Subthreshold swing obtained are validated with detailed numerical modelling/simulations [29].

C. Lin et al. has analysed the effect of changing ferroelectric material's thickness, polarization and coercivity on performance of negative capacitance FETs. Based on the study been done, a device structure of NCFET has been proposed in which upon ~±3% variation in ferroelectric properties will not affect the device performance much, no emergence of hysteresis and a very reasonable variation in I_{ON} current (i.e. ≤5%) [30].

S. Alghamdi et al. has reported for the very first time, low frequency noise in MoS_2 NCFETs. The author has taken Hafnium Oxide (HZO) ferroelectric and has analysed the device performance (in terms of low frequency noise) by varying interfacial oxides and different thickness of interfacial oxide [31]. It has been seen that the low frequency noise decreases with

the increase in HZO thickness in subthreshold regime of NCFETs. This observation reveals that negative capacitance phenomenon not only alters the I_{ON} and I_{OFF} states but also supresses the noise of the device.

J. Zhuo et al. has experimentally validated that the depolarization field (E_{DE}) in the ferroelectric layer of NCFET leads to voltage gains. Subthreshold swing and I_{ON} current are obtained for both NCFET with and without floating gate corresponding to the calculated voltage gains [32]. This gain is also measured experimentally depending upon the depolarization theory and voltage distribution across the gate stack. It has been concluded that E_{DE} in Fe layer produces the negative capacitance effect and voltage gains.

Y. Liang et al. has presented the use of negative capacitance FETs to analog circuits. It has already been seen in the literature that NCFETs have great potential for replacing conventional devices in low-power digital logic circuits and memories. The author has proposed new insights and characteristics of NCFET in analog circuit design space, specially phase-locked loops (PLLs) and analog to digital converters (ADCs). So, a digital clock-based comparator and a capacitor-based voltage to time converter (VTC) are demonstrated by the author, which are basic circuit elements of ADCs and PLLs [33].

Hung-Han Lin et al. has analysed the device design and analog performance of GaAsSb/InGaAs Negative capacitance Vertical Tunnel Field Effect Transistor. It has been seen that the proposed design has maximized the vertical tunneling over the corner tunneling due to amplified vertical electric field [34]. Optimized device has achieved larger I_{ON} (405 μ A/am), lesser I_{OFF} (10pA/ μ m) and steeper subthreshold swing of 14mV/decade over 4 decades of current at V_{DD} = 0.5 V.

R. Mann et al. has presented a new design approach of ferroelectric FETs based on theory of negative capacitance. The device structure been shown in this work helps in reducing the subthreshold swing and enhancing the current ratio. Comparison of various parameters such as TGF, g_d, C_{gg}, A_v and short channel effects such as SS, V_{TH}, DIBL have shown that proposed device structure can be used in energy efficient circuits as I_{OFF} is decreased by one order of

magnitude and SS in linear and saturation region is reduced by 7.09 % and 16.86 % respectively [35].

S. Chaudhary et al. has compared the simulation results of Bulk MOSFET and NCFET. The results have shown a considerable reduction in SS swing value, ensuring the use of negative capacitance phenomenon in low power applications. Further, effect of various parameters (such as effective oxide thickness, doping concentrations, drain voltage, thickness of ferroelectric material) on the device performance are also discussed in this work. With ferroelectric thickness of 60 nm, an average SS of 53 mV/decade and a hysteresis free operation is obtained at V_{DS}=0.4V [36].

S. Somu et al. have presented a circuit model for Landau-Khalatnikov ferroelectric model. It has been seen that the size and shape of hysteresis loops are depending on the frequency and amplitude of the applied electric field. The work reported has compared the experimental data with the simulated results and a method has been outlined to extract the coercive field by employing a driving voltage with both ac and dc components [37]. The coercive field can be calculated with a great accuracy if the relative dielectric constant at zero applied field and remnant polarization are known.

Y. Lin et al. has demonstrated the 2-D negative capacitance FET and effect of gate stack composition and thickness on the device performance. Few important findings have been reported in this work (which includes gate controllability, Impact of gate dielectric and thickness on threshold voltage). It has been seen that the threshold voltage shifts positively with the increase in Fe material thickness and negatively with the increase in dielectric thickness [38]. Moreover, the use of interfacial metal layer is also explored by comparing the performance of 2-D NCFET devices with and without IF layer.

B. Lu et al. has reported a new approach where the combination of line-tunneling mechanism and heterojunction are considered together. This approach has significantly improved the I_{ON} current and reduced the sub-threshold swing when applied to tunnel field effect transistors. The major issue reported in this approach is the isolation between source and drain in case of InAs/GaSb line-tunneling field effect transistor. For this cantilever or airbridge structure is proposed and in case of InAs/GaSb LTFETs (with buried drain technique) current ratio > 10^7

and SS < 60 mV/decade has been obtained for five decades of current. The buried drain technique not only keeps the device planar but also makes the fabrication simpler which is great importance for low power applications [39].

Tzu-Yu Yu et al. has investigated the performance of GaAsSb/InGaAs based negative capacitance vertical tunneling FET for maximizing the vertical tunneling over the corner tunneling. A novel device structure has been proposed in this work, where vertical tunneling has been enhanced and I_{OFF} of 10 pA/μ m and I_{ON} of 405 μ A/μ m has been reported with 14 mV/decade sub-Vt swing over four decades of current at V_{DD} = 0.5V. Moreover, the I_{ON} improvement of optimized NCV-TFET device over baseline TFET becomes of great importance as V_{DD} scales from 0.5 V to 0.1 V. So, the device reported in the work has a great potential for ultralow power applications [40].

H. W. Kim et al. has proposed a negative capacitance tunnel FET with tunneling current in normal direction to the gate. The characteristics obtained are calibrated with the model parameters using TCAD simulations. By optimally selecting the doping concentration of overlap region the current has been increased to 3.5 times and average subthreshold slope of 43.9 mV/decade has been obtained [41]. Further to enhance the subthreshold swing (SS) and to control ambipolar current, device is optimized by changing the channel length and source overlap length.

R. Narang et al. presented the impact of Gate Drain Underlap on ambipolar behaviour of TFET. Although in this work the theoretical approach is used to see the impact of ambipolar behaviour on TFET circuits, however the in-depth analysis of the circuit level is not been carried out in this work [42].

S. Guha et al. has shown the improvements done in speed and power consumption in sub-0.4 V_{DD} digital circuits by intervention of negative capacitance TFETs. A steeper SS of 27 mV/decade and current ratio of 10^{16} is achieved and device so formed is tested in Inverter, Ring oscillator, Multiplexer and Full Adder Circuits [43].

N. K. Kranthi and M. Shrivastava [44] have researched about the grounded gate configuration of TFET for analysing the electrostatic discharge behaviour, and the result of the device showed that the interaction between band to band tunneling, avalanche multiplication, and thermal carrier generation leads to voltage snapback and failure.

L. Ding et al. [45-46] showed the electrical stress impacts of buried oxide (BOX) layer in TFETs and it can't be overlooked altogether in ionizing dose radiation tests as they can overpower the radiation-induced degradation, that presents more serious degradation than TFETs [16].

V. Pi-Ho Hu et. al. presented a negative capacitance vertical tunnel field effect transistor with GaAsSb/InGaAs. The vertical tunneling is enhanced as compared to corner tunneling in the device proposed. Subthreshold swing of 14 mV/decade over 4 dec of drain current is obtained with small Ioff and large I_{ON}. NCVTFET is further optimized and at V_{DD}=1V, device has achieved a current ratio of 6E+5 [47].

H.W. Kim et. al. has investigated electrical characteristics of new NCTFET structure where tunneling current is kept in normal direction to the gate. The new device so performed has p+ doping in channel overlap region which plays a vital role in suppressing the corner BTBT which degrades the on/off transition. Subthreshold swing of 43.9 mV/dec has been achieved with I_{ON} current being enhanced by 3.5 times [48].

D. Kwon et. al. has reported a negative capacitance FET having 1.8 nm thick HfO_2 gate oxide layer fabricated on an FDSOI wafer. In this work, author has shown the hysteresis free operation of NCTFET. At a channel length of 30 nm (Constant I_{ON}), 10 X reduction in I_{OFF} current an SS steeper than 20 mV/dec is seen. At a constant value of I_{ON}, larger than 10X reduction is seen in I_{OFF} current and subthreshold slope has been made more than 20mV/decade steeper, by the intervention of Zr-doped HfO_2 layer as compared to a baseline NCFET using HfO_2 gate oxide. On the other hand, at constant I_{OFF}, the device provides a larger I_{ON} current at constant V_{DD}[49].

C. Su et. al has analysed that there exists a trade-off between making the subthreshold swing steeper and attaining a higher Ion/Ioff over large range of drain current based on the domain

switching dynamics model of Ferroelectric (Fe). The SS can be made steeper only for a limited range of drain current. The results indicate that the drain current range can be enlarged only within the limited range of sweeping rate and Fe switching time [50].

S. T. Bu et al. has presented an analytical model for the fluctuation of electrostatic potential in TFET, induced by charged trap in gate oxide region. The impact of frequency and bias voltage on normalized power spectrum density (S_{ID}/I_D^2) is discussed in this work and it has been seen that there exists a different noise spectrum in reported TFET structure than conventional MOSFET. The results depict that the noise from the channel is due to mobility fluctuations rather than carrier number fluctuations [51].

A. Pahariya et al. discussed about surface potential model for MFIS negative capacitance field effect transistor and results obtained have shown that there exists an excellent match between device parameters received from presented modelling and TCAD simulations. It has also been concluded in this work that capacitance matching and gate control has a direct relationship with thickness of Fe material and the ratio of coercive field to remnant polarization [52].

V. P. Hu et al. investigated various Fe materials for negative capacitance vertical-tunnel FET to improvise the vertical tunneling over the corner tunneling which in turns improve the overall performance of the device so reported. With optimization of device formed, super steep subthreshold swing of 14 mV/dec has been obtained with I_{ON} = 405 μA/μm and smaller I_{OFF} = 10 pA/μm [53].

F. Najam et al. has discussed the impact of quantum confinement on BTBT tunneling and has employed overlapping phenomenon to improvise the device performance. An L-Shaped tunnel field effect transistor (LTFET) is considered with thin overlapped channel and geometrical quantum confinement effect (QCE). The effect of QCE on conduction and valence band is analysed and discussed in this work [54].

A. Pal et al. has reported a drain current model and the proposed model in this study has calculated the surface potential under two modes: accumulation and depletion mode. Another important aspect reported deals with the approximation of I_D when V_{DS} is not applied. Negative conductance region is also reported for the first time in this work [55].

C. Jiang et al. has investigated the performance of Gate All Round Tunnel Field Effect Transistor (GAA-TFET) with negative capacitance phenomenon and has shown super steep subthreshold swing and larger I_{ON} without any hysteresis. An electrostatic analytical model has been simulated and there exists a good matching with the numerical simulations. Moreover, the effect of thickness and gate controllability is also addressed in this work [56].

M. Kao. et al. demonstrated the modelling of polarization gradient effect using compact model for negative capacitance phenomenon. Author has worked for reducing I_{OFF}, reducing the drain-induced barrier lowering (DIBL) by using a higher value for coefficient of polarization gradient effect [6]. The work reported in literature has shown that the negative capacitance has a great potential in replacing conventional MOSFETs due to switching of polarization in Fe material. Performance of device so formed is dependent on switching characteristics [57].

X. Huang et al. has presented a dynamic current model for double-gate negative capacitance FET. A dynamic model is formulated analytically with time-dependent charge densities at source and drain side [58]. When compared with the TCAD simulated data, the model presented in this work has accurately reproduced the static negative capacitance effect which is helpful in enhancing the driving current and dynamic NC effect.

S. Poorvasha et al. has experimentally validated the results of double gate tunnel FETs by using an analytical model of quantum mechanical tunneling. Double gate tunnel field effect transistor structure has been proposed in this work and drive current Ion has shown a considerable improvement. The physics and device performance of the structure is analysed using different materials (such as Si, SiGe, InAs etc). Moreover, the concept of gate-drain overlap has also shown improvements as compared to device without overlap [59].

H. Lee et al. proposed a semi-analytical model for negative capacitance FET with $BaTiO_3$ Fe material. L-K equation is numerically solved with Poisson's equation to get the surface potential in the channel. With the help of surface potential calculated by above method, ID is obtained by solving current continuity equation. The model used in this study is validated by matching the results of TCAD simulations and MATLAB calculations and it has shown a good agreement between the two. Moreover, the impact of Fe material thickness and channel doping concentration on the device performance is also explained [60].

H. Mulaosmanovic et al. explained the use of Negative capacitance field effect transistor for making large memory window devices. It has been seen that HfO_2 based Fe-FET can be utilized to make a non-volatile memory but the Memory window of this device is small which is the main hindrance in using these devices for practical circuits and memory elements. A novel device with 28 nm high-k metal gate and 90 nm channel length is reported in this work and with this device a memory window of about 3V is achieved [61]. Moreover, the device formed has good retention at high temperature making it suitable for future memory circuits.

F. Meng et al. has proposed a L-Shaped tunnel field effect transistor (LTFET) with gate-drain underlapping and has significantly reduced the ambipolar behaviour and resulted in improvisation of inverter circuit. It has been seen that with the gate-drain underlapping, the energy band of junction has changed so, GDU-LTFET has lowered the BTBT tunneling rate that in turns has reduced the static power consumption of the TFET circuit. The simulation results reported in this work have shown a clear picture that with gate-drain underlapping the voltage gain, noise margin and static power have reduced in inverter circuit as compared to baseline LTFET structure [62].

N. Kamal et al. has designed a L-Shaped 1-T DRAM with SiGe region for holding. The sense margin and retention time are improved with the use of SiGe material has simulation results shows that LTFET DRAM reported in this work has SM of 6.2 μ A/μ m with retention time of 1.7 Seconds at 50nm gate length and 27 C temperature. The device performance also has a dependence on temperature. In comparison to the earlier results, the same device provided a SM of 5.1 μ A/μ m and RT of 290 ms when operated at Temperature of 85 C. LTFET devices exhibits a better gate length scalability as compared with TFET based 1T DRAMs [63].

V. Chauhan et al. have presented recent advances in negative capacitance FinFETs as applied to low power applications. The review done by the author emphasizes that how negative capacitance can withstand with the aggressive scaling of transistors and moreover supports the persistence of Moore's law and addresses the ultimate limitation of Boltzmann Tyranny. The author has focussed on explaining the theoretical background of negative capacitance effect and FinFET devices, along with this, the recent advancements in this field are also highlighted [64]. The upcoming need is to use a blend of NCFinFETs and CMOS technologies to get a better correlation between device and circuit.

Looking onto the issues addressed in the literature, a device incorporating the benefits of overlapping and underlapping the gate stack over the channel is proposed. Various device architectures (like T-Shaped, L-Shaped, U-Shaped) have been reported and simulated in the literature [65-67]. Considering the possible improvisations, the negative capacitance phenomenon with tunnel field effect transistors has been used and experimental validation of the simulation results have been carried out. Having a gate stack comprising of Fe layer and Gate Oxide layer has made I_{ON} current higher, which is major limitation of conventional TFET. Moreover, with Ge source, a heterojunction has been made at source channel junction which provides a narrow tunneling, improvising the current as well as I_{ON}/I_{OFF} ratio.

2.4 Problem Statement and Research Gap

Looking into the solutions reported in the literature certain device modifications are required in conventional TFET structure so as to obtain a more optimal device performance. Few of the motivations behind selecting this research area are listed below:

1. TFETs are considered as strong contenders to replace the conventional MOSFETs in the future technologies, still various device structures have low drive currents. The techniques used to enhance the I_{ON} current, effects the I_{ON} current as well. So overall I_{ON}/I_{OFF} ratio turns out to stay lower. So, in this work, prime focus is on selecting appropriate materials for source, channel and drain such that the higher tunneling should occur which in turns yield higher I_{ON} current at source channel junction and prevents tunneling at drain-channel junction such that there is minimum leakage current.

2. Negative capacitance phenomenon is implemented for TFET structure to overcome various shortcoming and to achieve a steeper sub-threshold swing. Negative capacitance being a novel technique provides promising results in terms of current ratio, reduction of short channel effects and reduction of power consumption. In this work, after extensive review and simulations, the selection of ferroelectric material, thickness of ferroelectric material and their effect on device performance are discussed. It has been concluded (with supporting plots) that selecting HfO_2 as gate oxide and $BaTiO_3$ as

ferroelectric material has provided best results. Moreover, its length and thickness are also optimized to achieve higher I_{ON}/I_{OFF} ratio and sub-threshold swing lesser than 60mV/decade.

3. Doping profile of source and drain regions plays a vital role in achieving better characteristics of TFET structures. While reviewing the literature, it has been found that the doping of source and drain regions should be of opposite dopants. Like in case of n-type TFET, the drain region should be n-type doped whereas source region should be p-type doped. As a consequence of this, if we apply a negative gate voltage to TFET, there occurs a current transport due to BTBT tunneling at drain channel junction.

4. The new age TFET structures (L-Shaped, T-Shaped, U-Shaped) reported in literature have been successful in improvising the device performance in terms of current ratio, SS swing and power consumption. So, in this work, the concept of source region raising along with gate overlapping over source region has been used. Moreover, the gate stack positioning has also been optimized to achieve better tunneling at source-channel junction and least at drain-channel junction.

Heterojunction (Ge-Source) negative capacitance tunnel field effect transistor has been presented in this work. The phenomenon of gate stack overlapping and underlapping is also used to improvise the results along with raising the source to a certain height for getting stronger and more concentrated electric field.

2.5 Objectives of proposed work

1. Simulation of Negative capacitance FET and comparison with existing technologies;
2. Mathematical modelling of Negative capacitance device;
3. Design of Heterojunction NCTFET with ferroelectric and High-k dielectric gate stack as channel.
4. Application of designed NCFET for power optimization in VLSI circuit.

2.6 Research Methodology

Keeping in view the shortcomings of conventional MOSFET devices, the technologies presented in the literature are reviewed extensively and new phenomenon (like negative

capacitance) has been studied and explained. A novel device has been made by applying negative capacitance to TFET device. The following flowchart explains the process followed in carrying out research.

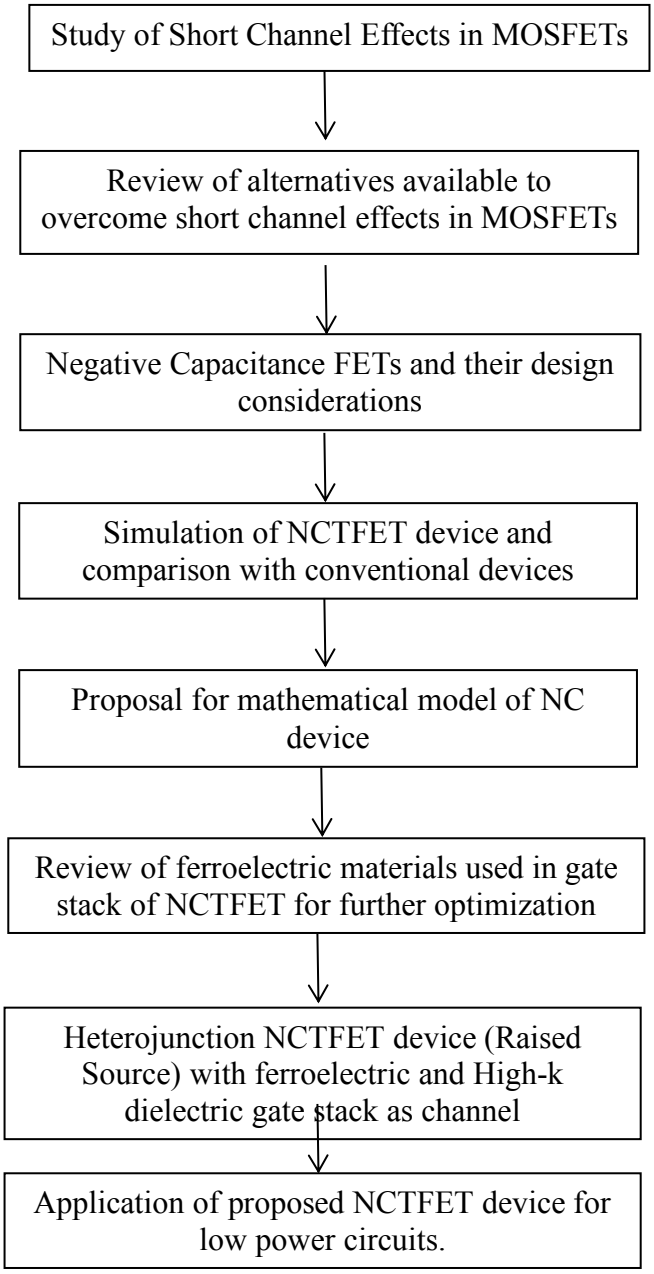


Figure 2.1 Research Methodology

Based on the study of short channel effects, their impact on device performance and major challenges in scaling the MOSFETs, the main focus has been made on controlling the limitations and improvisation of device performance. Objective wise research methodology formed have been discussed as follows:

Objective 1: Simulation of Negative capacitance FET and comparison with existing technologies

As stated negative capacitance FETs are emerging as an intelligent alternative addressing the promising solutions to the problems of existing technologies. In our first objective we have started up with the simulation-based study of conventional devices, their limitations and have done improvisations in the existing technologies by applying phenomenon of Negative Capacitance to get improvised results.

For achieving this objective, extensive literature review has been done for figuring out the concept of negative capacitance and its application to low power VLSI circuits. It has been seen that various device structures like T-Shaped, U-Shaped, F-Shaped TFETs have been reported in literature. Moreover, the choice of Ferroelectric material (such as PZT, P(VDF-TrFe), $BaTiO_3$, SBT) used in making NCTFET also plays a significant role in device performance. The device proposed in this study is capable to achieving a steeper subthreshold swing (SS) and higher I_{ON}/I_{OFF} ratio.

Objective 2: Mathematical modelling of Negative capacitance device

The aim of this objective is to carry out mathematical modelling of the proposed device so as to have clear picture of the result obtained by TCAD simulations. For achieving this objective, mathematical modelling is carried out in MATLAB software and NCTFET is implemented to obtain the transfer characteristics, I_{ON}, I_{OFF} currents and Subthreshold Swing (SS). The voltage-charge characteristics of Ferroelectric materials can be defined by Landau-Khalatnikov (LK) equation, that states:

$$V_{FE} = T_{FE}\left(2\alpha Q_t + 4\beta Q_t^3 + 6\gamma Q_t^5\right). \tag{2.1}$$

Here T_{FE} is the thickness, and α, β, and γ are the Landau constants of the ferroelectric material. Different materials have different landau coefficients and the thickness of ferroelectric material plays an important role in device performance. It has been seen that best results are obtained with $BaTiO_3$ material at thickness of 3 nm.

Objective 3: Design of Heterojunction NCTFET with ferroelectric and High-k dielectric gate stack as channel

With all the literature review and simulation study done so far, it has been seen that device engineering along with wise choice of materials is required to design an improvised Negative Capacitance TFET. So to achieve this objective, a raised source gate overlapped NCTFET device have been structured and reported in this work. In proposed device, Ge material is used as source material to form a heterojunction at source-channel junction and a 3nm thick $BaTiO_3$ Fe material layer is stacked over HfO_2 layer to form a gate stack of NCTFET. Due to high doping concentration of source and drain regions, Band-gap narrowing model and Fermi Dirac statistics model have been activated for the optimized device. The dynamic non-local BTBT model has been included at the tunnelling junction of proposed device due to tunnelling probability of the carriers. The effect of traps have been investigated by including the Gaussian trap model.

It has been seen that the proposed device is capable of achieving 53.7 mV/decade subthreshold swing and I_{ON}/I_{OFF} current ratio of $7.14x10^{+9}$. Although heterojunction structures provide a better ON current but the tunnelling leakage is also more in such devices due to smaller bandgap at short channel lengths. Moreover, to reduce the ambipolar current the doping concentration of source terminal is kept higher as compared to drain. The device formed has shown a decline of 6.3 mV/dec in subthreshold swing as compared to the fundamental limit of 60mV/dec and enhances the I_{ON}/I_{OFF} ratio to 250 times in magnitude. DIBL calculated for conventional NCTFET is 61.2 mV/V and for proposed NCTFET is 31.92 mV/V. So DIBL improvement of 47.8% has been achieved.

Objective 4: Application of designed NCFET for power optimization in VLSI circuit

To analyse the use of proposed NCTFET device for low power applications, an inverter and dynamic random-access memory has been designed and compared with conventional devices in terms of power consumed. It has been observed from the result that the proposed NCTFET inverter can be put to use in practical applications to replace conventional MOSFET.

CHAPTER 3: MODELLING OF PROPOSED NCTFET DEVICE

3.1 Introduction

The major hindrance in reduction of supply voltage is the barrier in lowering the subthreshold slope (SS) below the Boltzmann tyranny limit of 60 mV/decade. To overcome this issue, negative capacitance has emerged as a promising concept taking into view the internal voltage amplification and improved subthreshold swing. To use negative capacitance phenomenon in practical circuit designs, an efficient physics-based model is required. The work reported in literature has shown that the negative capacitance has a great potential in replacing conventional MOSFETs due to switching of polarization in Fe material. Performance of device so formed is dependent on switching characteristics [68].

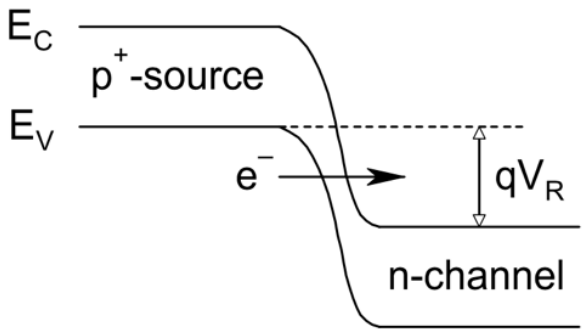


Figure 3.1: Band Diagram of Heterojunction

The energy band diagram of the heterojunction so formed in proposed device is shown in Figure 3.1 during its ON state, where V_R denotes the range of potential for electron tunnelling to take place from the source valence band to the channel conduction band. This has been seen that the behavior of ferroelectric material is best explained by Landau-Khalatnikov equation, popularly known as L-K Model [9]. It relates the voltage across ferroelectric material with the time dependent ferroelectric polarization and thickness of ferroelectric layer. In this section, an accurate and computationally efficient analytical model for NCTFET is presented. The model discussed is based on capacitance matching and Landau-Khalatnikov equations implemented on conventional TFET. The current-voltage model is developed by calculating the capacitance and voltage across ferroelectric layer. The ψ_s calculated is used subsequently to obtain the charge and capacitance behavior. The results show that there is a good match between modelling results and obtained from Synopsys TCAD simulations. The calculations include various device parameters such as charges, V_{FE}, drain current, subthreshold slope (SS). The

impact of Fe material thickness can be seen in I_D-V_{GS} characteristics of proposed device.

3.2 Model Description

The proposed device has a ferroelectric layer stacked on HfO_2 oxide layer and structure is improvised for getting better I_{ON}/I_{OFF} ratio with steeper subthreshold swing [69]. The device so formed can be viewed as a capacitive voltage divider.

3.2.1 Capacitance Charge Model

For modelling NCTFET, 1-D Landau-Ginzburg equation is considered with an assumption that P is equal to Q_g. The gate charge Q_g is comprising of following:

$$Q_g = (Q_{inv} + Q_{dep} + Q_{acc}) \tag{3.1}$$

Where Q_{inv} is channel inversion charge, Q_{acc} is accumulation charge and Q_{dep} is substrate depletion charge.

$$Q_b = (Q_{acc} + Q_{dep}) \tag{3.2}$$

$$Q_{inv} = (Q_s + Q_d) \tag{3.3}$$

Qd, Qg, Qb, Qs, and are charges for drain, gate, base and source respectively. Further, the depletion charge can be divided into two major parts: Qdep0 at zero source-drain bias and additional non-uniform depletion charge when drain bias is applied (δQdep) [70]. Taking all these in consideration Qg becomes:

$$Q_g = -(Q_{inv} + Q_{acc} + Q_{dep0} + \delta Q_{dep}) \tag{3.4}$$

The total charge is calculated by integrating the charge along channel.

Due to presence of non-uniform depletion charge, the threshold voltage along the channel is given by:

$$V_{th}(y) = V_{th}(0) + (A_{bulk} - 1)V_y \tag{3.5}$$

$$Q_c = W_{active} \int_0^{L_{active}} q_c \, dy = - W_{active} C_{ox} \int_0^{L_{active}} (V_{gt} - A_{bulk} V_y) dy \tag{3.6}$$

$$Q_g = W_{active} \int_0^{L_{active}} q_g \, dy = W_{active} C_{ox} \int_0^{L_{active}} (V_{gt} + V_{th} - V_{FB} - \phi_s - V_y) dy \tag{3.7}$$

$$Q_b = W_{active} \int_0^{L_{active}} q_b \, dy = - W_{active} C_{ox} \int_0^{L_{active}} (V_{gt} + V_{th} - V_{FB} - \phi_s + (A_{bulk} - 1) V_y) dy \tag{3.8}$$

Substituting the following:

$$dy = \frac{dV_y}{\varepsilon_y} \; I_{ds} = \frac{W_{active} \mu_{eff} C_{ox}}{L_{active}} \left(V_{gt} - \frac{A_{bulk}}{2} V_{ds} \right) = W_{active} \mu_{eff} C_{ox} \left(V_{gt} - A_{bulk} V_y \right) E_y \tag{3.9}$$

Charge equations become:

$$Q_c = -W_{active} L_{active} C_{ox} \left(V_{gt} - \frac{A_{bulk}}{2} V_{ds} + \frac{A_{bulk}^{\,2} V_{ds}^{\,2}}{12 \left(V_{gt} - \frac{A_{bulk}}{2} V_{ds} \right)} \right) \tag{3.10}$$

$$Q_g = -Q_{sub0} + W_{active} L_{active} C_{ox} \left(V_{gt} - \frac{V_{ds}}{2} + \frac{A_{bulk} V_{ds}^{\,2}}{12 \left(V_{gt} - \frac{A_{bulk}}{2} V_{ds} \right)} \right) \tag{3.11}$$

$$Q_b = -(Q_g + Q_c) = Q_{sub} + Q_{sub0} + Q_{acc} \tag{3.12}$$

To ensure the charge conservation, all the capacitances are derived from the charges. Considering all the four terminals, there exists in total 16 components and for each component:

$$C_{ij} = \frac{\delta Q_i}{\delta V_j} \; \sum_i Cij = \sum_j Cij = 0 \tag{3.13}$$

Where i and j denotes the transistor terminals.

3.2.2 Band to Band Tunneling Model

By integrating the tunnel current density along the device width (W) and thickness, the total current can be derived. As the current remains consistent along the width (W) so below expression provides the tunneling current per unit width:

$$I_D = A\int\left(V_R.E.\exp(-B/E_{barrier})[1-\exp(-qV_R/E)]\right).dy \tag{3.14}$$

In above equation, A = q2mv2/(8πh3(mvml)1/2), B/Ebarrier = 2Eg/(3E) and E = qhEbarrier/(8mrEg)1/2 (q is coulomb charge, h is reduced planck's constant), m_r is average effective mass, expressed as:

$$m_r = (1/m_c + 1/m_v)^{-1} \tag{3.15}$$

m_c denotes the effective mass of electrons in conduction band and m_v denotes the effective mass of electrons in valence band. In this work, the entire channel thickness is used to obtain the electric field at the surface [71]. The BTBT current is the function of $E_{barrier}$ and V_R both.

3.2.3 Ferroelectric Material Model

Landau-Khalatnikov Equation (LK-Model) is a compact model of ferroelectric materials which captures the negative capacitance phenomenon accurately and defines a relationship between electric field (E) and Polarization (P) of material used:

$$\delta\frac{dP}{dt} = -\frac{\delta G}{\delta P} \tag{3.16}$$

$$G = \alpha P^2 + \beta P^4 + \gamma P^6 - EP \tag{3.17}$$

In above expressions, E is Electric Field along Fe material, P is ferroelectric polarization and G is Gibb's energy. α, β, γ are Landau coefficients associated with Ferroelectric materials and values of these coefficients for commonly used Ferroelectric materials are shown in Table 3-1.

Table 3-1: Landau Coefficients for Various Ferroelectric Materials

Landau Coeff. / Material	α (cm/F)	β (cm5/F/Coul2)	γ (cm9/F/Coul4)
PZT	-2.25e9	1.3e18	9.8333e25
BaTiO3	-5e8	-2.225e18	7.5e27
P(VDF-TrFE)	-1.8e11	5.8e22	0

The parameter δ is the polarization damping factor, which in turns depend on the amplitude of voltage applied. From above equations electric field can be written as:

$$E = \frac{V_{fe}}{T_{fe}} = 2\alpha P + 4\beta P^3 + 6\gamma P^5 + \delta \frac{dP}{dt} \tag{3.18}$$

V_{FE} is Voltage across ferroelectric material and T_{FE} is thickness of ferroelectric layer.

Figure 3.2 shows the transfer characteristics obtained for different Fe materials and it can be seen that $BaTiO_3$ is providing the most steeper transfer characteristics among all three materials.

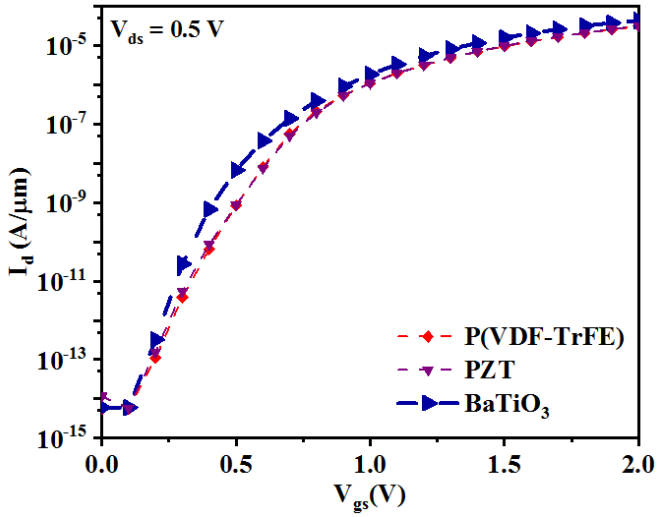


Figure 3.2: $I_D V_{GS}$ characteristics of proposed NCTFET with different Fe materials.

By applying the boundary conditions at M-F (Metal-Ferro) interface, the expression for

polarization can be obtained in terms of gate charge density, Q and V_{fe} as:

$$P = Q - \varepsilon_0 \frac{V_{fe}}{T_{fe}} \tag{3.19}$$

The above equation is used to obtain device characteristics and other parameters associated [72].

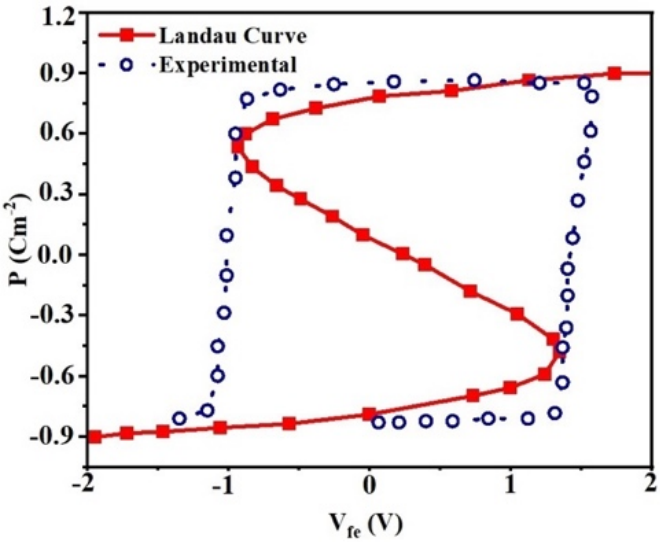


Figure 3.3: P-V_{FE} curve of proposed NCTFET with $BaTiO_3$ Fe Material

The experimental P-V_{FE} curve as shown in Figure 3.3 has been shifted along the V_{FE} axis. By this it has been made symmetrical so that it fits the landau equation.

3.3 Device Calibration

To verify the accuracy of simulation, the TCAD Simulation data of the optimized device is calibrated against the reference experimental data [73] at drain voltage 0.5 V as shown in Figure 3.4. The Kane's model for non-local electric field is used for calculation of BTBT direct generation rate (G), and is given by equation 4.20 below:

$$G = AE^2 \exp\left(\frac{-B}{E}\right) \tag{3.20}$$

The prefactor A and exponential factor B are set to $8.1*10^{18}$ $cm^{-1}s^{-1}V^{-2}$ and $2.95*10^7$ V/cm in the Synopsys TCAD simulation model [74]. On the other hand, A and B are adjusted to $9.16*10^{18}$ $cm^{-1}s^{-1}V^{-2}$ and $3.1*10^7$ V/cm in the analytical model. Due to high doping concentration in source and drain regions, Band-gap narrowing model and Fermi Dirac statistics model have been used. As depicted in the Figure 3.4 there exists a good matching of

both the data, which certify the validity of the selected models. The source and drain material are Ge, and the channel material is Si.

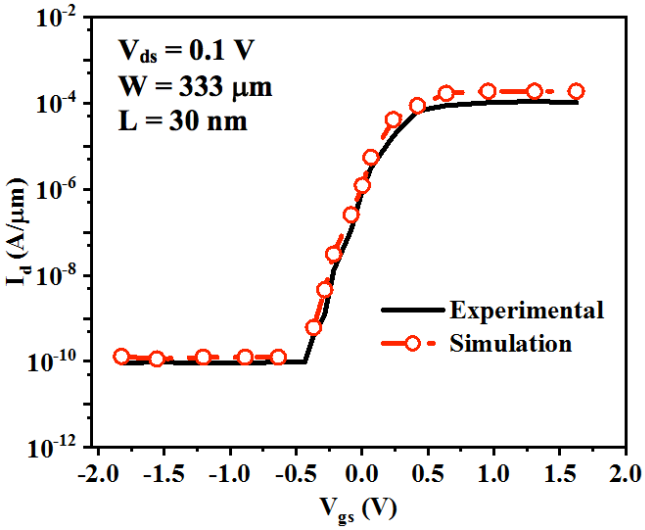


Figure 3.4: Calibration of TCAD set up of optimized device with experimental data of reported paper [72]

3.4 Device Characteristics

To calibrate the simulations experimentally, Landau coefficients are extracted by fitting the LK equation against the data sampled from P-V_{fe} hysteresis curve as shown in Figure 3.3.

The overall gate potential can be summed up as:

$$V_g = V_{FB} + V_{fe} + V_{ox} + \psi_s \tag{3.21}$$

In the above equation, V_{FB} denotes the flat band voltage and $V_{ox} = Q/C_{ox}$ is the voltage across oxide layer and C_{ox} denotes oxide capacitance, V_{fe} is voltage across ferroelectric layer and ψ_s is surface potential.

3.4.1 Voltage amplification (Av) due to negative capacitance is obtained as:

$$A_v = \frac{\delta V_{int}}{\delta V_g} = \left(\frac{|C_{fe}|}{|C_{fe}| - C_{int}} \right) \tag{3.22}$$

In practical applications, with the use of high k dielectric layer and thin gate oxide layer, increases the C_{int}, which is helpful in enhancing the gate controllability.

$$C_{fe} = \frac{\delta Q}{\delta V_{fe}} = \left(\frac{1}{t_{fe}\left(2\alpha + 12\beta Q^2 + 30\gamma Q^4\right)} \right) \tag{3.23}$$

If $\gamma = 0$, $\alpha = -\frac{3\sqrt{3}Ec}{Pr}$, $\beta = \frac{3\sqrt{3}Ec}{Pr}$, where P_r = Remnant Polarization and E_c = Coercive Field. Substituting these C_{fe} can be written as:

$$C_{fe} = \left(\frac{1}{t_{fe}\left(2\alpha + 12\beta Q^2\right)} \right) \tag{3.24}$$

The reduced value of C_{fe} will result in good capacitance matching, hence higher gain and improved current ratio [75].

3.4.2 Transfer Characteristics and Sub-threshold swing:

The overall voltage across gate stack of NCTFET can be obtained as:

$$V_{gnc} = V_{gtfet} + V_{fe} \tag{3.25}$$

Where V_{gtfet} is gate voltage of conventional TFET and V_{fe} is Voltage across ferroelectric layer. These expressions when implemented in MATLAB gives the I_D-V_{gs} characteristics of the device and is matched against the simulation results obtained from Synopsys TCAD as depicted in figure:

$$SS = \frac{\delta V_{gnc}}{\delta(\log_{10} I_d)} \tag{3.26}$$

$$SS = \ln 10 \left[\frac{1}{V_{eff}} \frac{dV_{eff}}{dV_{gnc}} + \frac{E + \delta}{E^2} \frac{dE}{dV_{gnc}} \right]^{-1} \tag{3.27}$$

In the above equation, δ is a constant, E is the electric field at the tunnel junction and V_{eff} denotes the total voltage across the heterojunction [76].

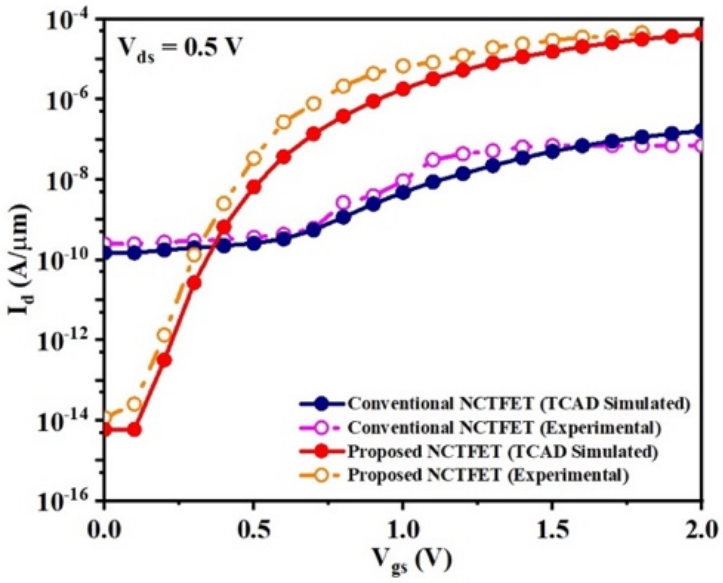


Figure 3.5: Experimental validation of transfer characteristics of proposed NCTFET against Conventional NCTFET

So as to make SS slope steeper, dV_{eff}/dV_{gs} should be improved, which is due by concept of overlapping and underlapping so that gate controllability is enhanced. In addition, ferroelectric layer introduced has a direct effect on improvising the gate controllability and improving the total gate capacitance. It has been seen that there is a good matching between Synopsys TCAD simulated model and MATLAB simulated model [70], [77]. The operation of NCTFET with varying thickness and Fe materials has been demonstrated and analysis has depicted that the thickness of gate oxide and ferroelectric material plays an important role in achieving steeper subthreshold slope and higher I_{ON}. In addition, body factor (m-factor) and transport factor (n-factor) associated with the device were improvised in proposed NCTFET and with Fe material engineering, the electrical performance is boosted up in case of proposed NCTFET device. The device parameters examined in this work shows the first-order continuity making the proposed device suitable for circuit simulations.

CHAPTER 4: ELECTRICAL CHARACTERISTICS OF PROPOSED NCTFET DEVICE

4.1 Introduction

The current CMOS technology has a substhreshold swing (~ 60 mv/Dec) but the supply voltage has not been achieved below 1V. Tunnel Field Effect Transistor (TFET) is an emerging alternative to the conventional MOSFET because of its capability to deliver stepper subthreshold swing and reduce the supply voltage to value lesser than 0.5 V. The mechanism used to move charge carrier in TFET is Band to Band Tunnelling (BTBT) instead of thermal injection/point tunnelling. Thus, TFET device can be a good replacement over conventional MOSFET for low power applications [78-80]. Having capability to operate at Subthreshold swing lesser than 60 mV/decade and offering high I_{ON}/I_{OFF} at decreased supply voltages, TFET can be put to practical power applications. Also, with the use of heterojunction, I_{OFF} is very low compared to MOSFET, thus it further reduces the static and dynamic power dissipation.

The only problem that persists with TFET is its lesser I_{ON} current and ambipolar behaviour that can be controlled by choosing the materials wisely and doing some structural modification of the device [80]. Further, by intervention of a ferroelectric material at gate stack of TFET, I_{ON} current is enhanced along with making Subthreshold swing (SS) super steep. So, with ferroelectric material being added to the gate stack of TFET, faster switching with enhanced I_{ON} current is achieved. Thus, Negative Capacitance TFET (NCTFET) has a great potential for low power applications in VLSI domain [82].

By including a thin ferroelectric layer into a gate stack of a baseline MOS transistor, it is possible to reduce the subthreshold swing below 60mV/decade limit at room temperature. Further to improve SS and control ambipolar current device is optimized by altering channel length and source overlap length. With the intervention of negative capacitance following enhancements have been made that includes: less fabrication intricacy, less area, minimal cost, reduction of stray charges (due to core part of the nanotube), and less noise without compromising the I_{ON} of the device. In this section, negative capacitance phenomenon will be applied to heterojunction tunnel field effect transistor to get super steep subthreshold swing and higher I_{ON}/I_{OFF} ratio [83].

4.2 Effect of Source Overlapping/Underlapping on Device Performance

NCTFETs and TFETs are simulated with TCAD tool utilizing the BTBT model and Landau ferroelectric equation. Figure 4.1 shows the schematics of proposed NCTFET. The TFET structure is indistinguishable from NCTFET, just a ferroelectric (FE) layer is added to the gate stack of TFET. In this work, the nominal device parameters for NCTFET and TFET are recorded in Table 4-1. The source material Si and Ge are used and compared, and the drain and channel material is Si. For the ferroelectric material, landau coefficients are:

α = -1.299e^{11} cm/F, β = 6.4952e^{20} cm^5/FC^2, and γ = 5e^{30} cm^9/FC^4.

V_{DS} is kept constant at 0.5 V.

TABLE 4-1: Device Parameters

Quantities	**Symbol**	**Values**
Source Doping	N_A	1e19 cm^{-3}
Channel Doping	N_I	1e16 cm^{-3}
Drain Doping	N_D	1e19 cm^{-3}
Oxide Thickness	T_{ox}	5 nm
Ferroelectric Thickness	T_{FE}	3 nm
Channel Length	L_{CH}	30 nm

To minimize the ambipolar conduction and enhance the performance, TFET is designed in two different configurations with Si and Ge Source:

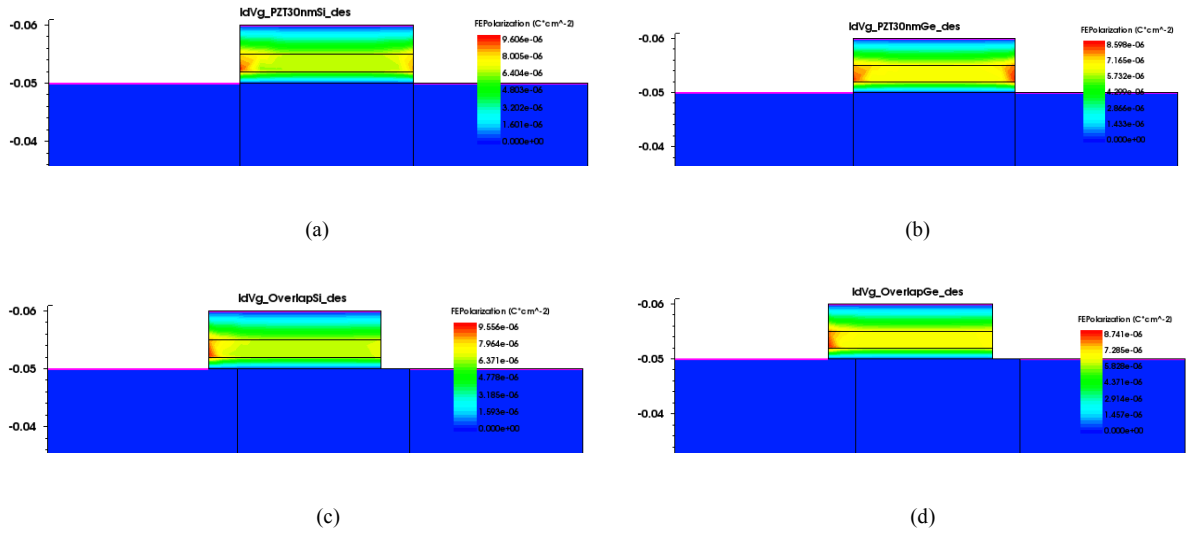


Figure 4.1: Fe Polarization in case of (a) & (b) for conventional NCTFET with Si and Ge Source (c) & (d) for Proposed NCTFET

Table 4-2: Design wise changes in Proposed Device in comparison with Conventional TFET

Particular	**TFET**	**NCTFET**
Ferroelectric Layer	No Fe layer	Fe layer of 3 nm Thickness
Source Gate Overlap Length (LSOV)	No Overlapping	5nm
Gate Drain Underlap Length (LGUL)	No Underlapping	5nm

It can be concluded from figure 4.1 that the device performance is enhanced in overlapped configuration of NCTFET. Fe Polarization can be seen on only source side which enhances the I_{ON} and reduces the leakage current [84].

4.2.1 Band to Band Generation in Overlapped and Underlapped Structures:

Figure 4.2 shows the Band to Band Tunnelling effect in case of conventional NCTFET and Proposed Heterojunction NCTFET.

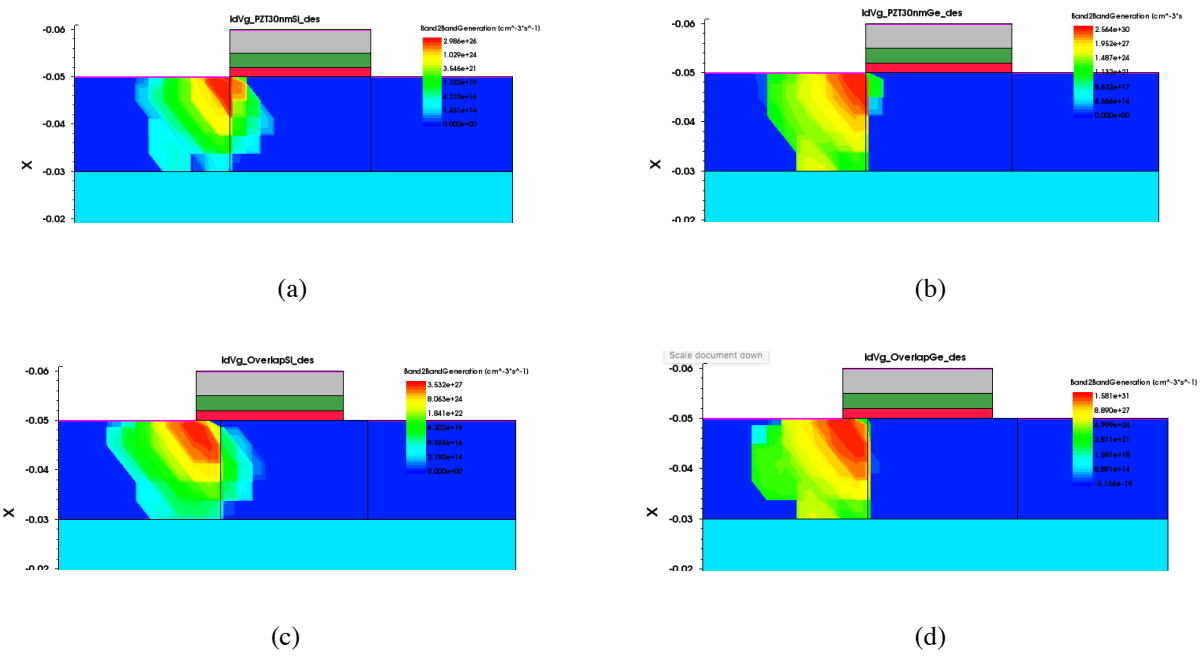


Figure 4.2: Band to Band Generation (a) Si Source and (b) Ge Source in Conventional NCTFET; (c) Si Source and (d) Ge Source in Proposed NCTFET

Figure 4.2 clearly depicts that band to band tunnelling effect in case of proposed NCTFET with heterojunction (Ge Source) is better. It can be seen in figure 4.2 (d), that the leakage in channel area is negligible and strong band to band tunnelling in source area results in higher concentration and I_{ON} current.

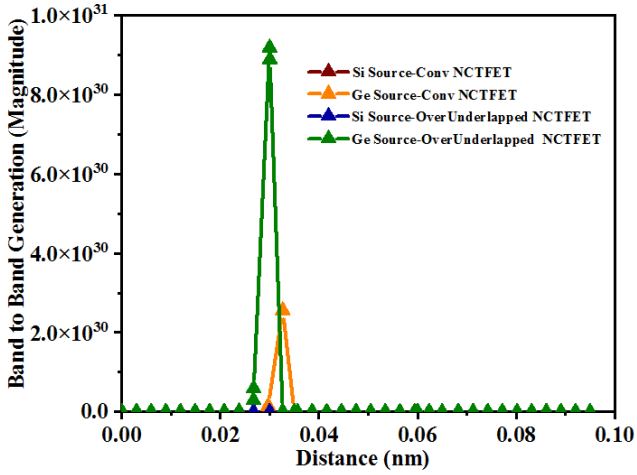


Figure 4.3: Band to Band Tunnelling Concentration

4.2.2 Comparison of Energy Band Diagram with Different Source Materials

The energy band diagram of NCTFETs during its ON state is shown in Figure 4.4. A significant factor which decides the I_{ON} of the device is dependent on the material property at the tunnelling junction (source side). Henceforth Silicon (Si) and Germanium (Ge) source materials have been used to make a heterojunction, by utilizing narrow band gap material in the tunnelling region and boarder gap material in the rest of the device [85].

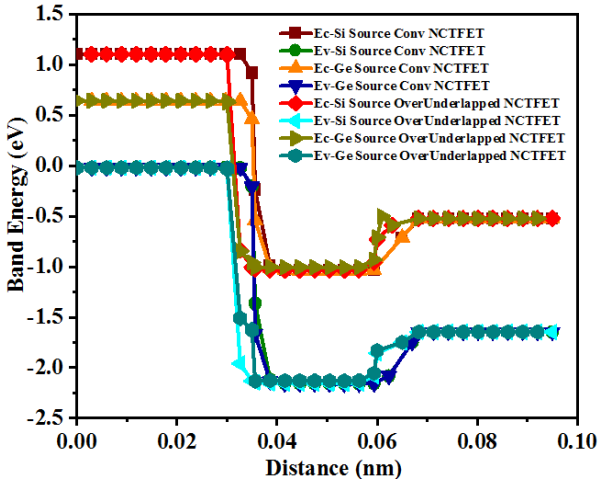


Figure 4.4 Energy Band Diagram for Conventional NCFET and Proposed NCTFET with different sources (Si and Ge)

From Figure 4.4, it may be very well seen that tunnelling width of NCTFET towards source-gate overlap is narrower in contrast to other devices, which at last enhances the tunnelling

probability and upgrades I_{ON}. Moreover, due to increased tunnelling rate of charge carrier at the source-channel junction, super steeper subthreshold swing has been achieved [86].

4.2.3 Electric Field of Different Source Materials

Figure 4.5 shows the absolute electric field generated along the channel for NCTFET with and without gate-source overlap.

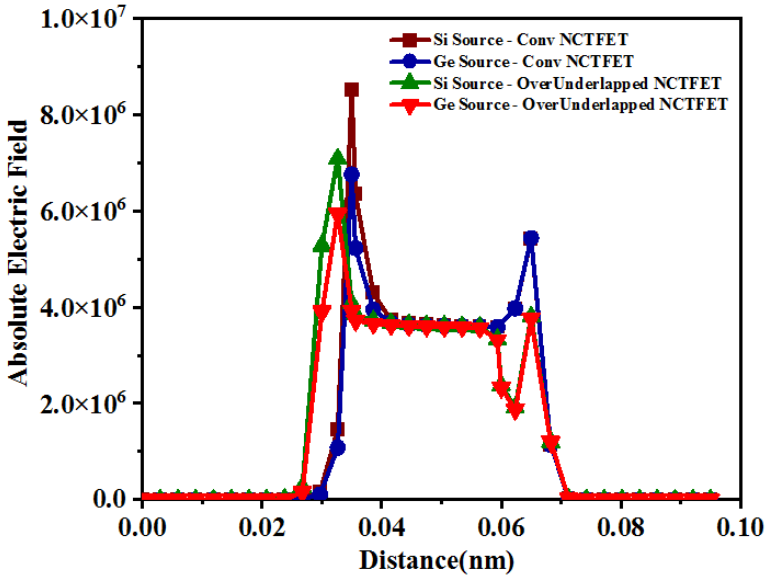
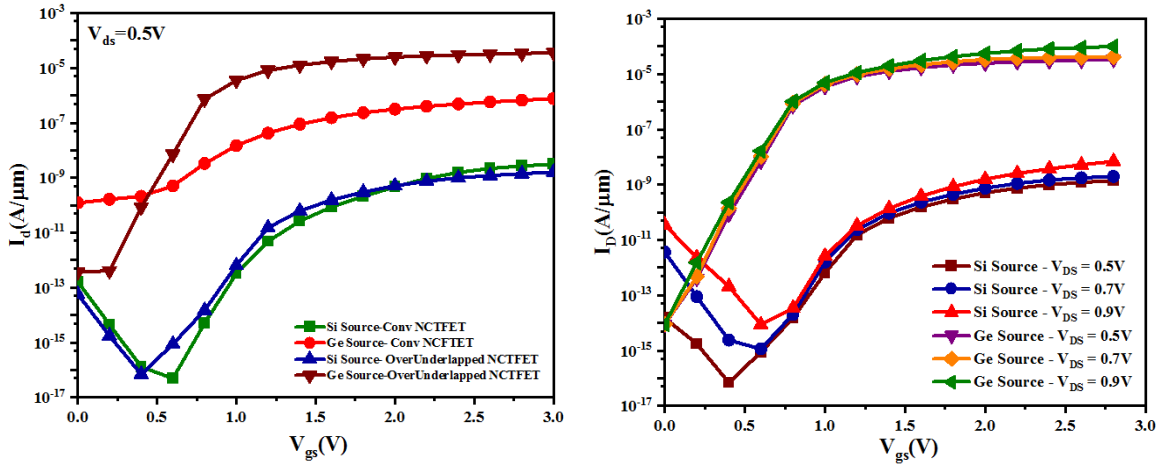


Figure 4.5: Absolute Electric Field for Conventional NCFET and Proposed NCTFET with different sources (Si and Ge)

The electric field created towards the source end is extremely strong for the device with gate source overlap when compared with the device without overlap. This effect is because of injection of charge carrier from the source is at a higher speed which in turns is liable for not degrading the device's overall performance.

4.2.4 Impact of Overlapping/Underlapping with different source materials on I_D/V_{GS}

Conventional NCTFET and Proposed NCTFET have been operated at a constant V_{DS}=0.5V and results are obtained as shown in Figure 4.6. It can be observed from the graph that a steeper response has been obtained in case of heterojunction over-underlapped NCTFET.



(a) (b)

Figure 4.6: (a) I_D-V_{GS} characteristics of Conventional NCTFET and Proposed NCTFET with Si and Ge Source (b) I_D-V_{GS} characteristics of Proposed NCTFET at different values of V_{DS}

Similarly, the proposed NCTFET has been operated at different V_{DS} values as 0.5V, 0.7V and 0.9V as seen in Figure 4.6 (b). The results are better for Ge Source NCTFET with V_{DS} in range of 0.5-0.9V. It is important to optimally select the overlapping of the ferroelectric material with source/channel side so the enhancement of the voltage should be possible appropriately with least hysteresis. In outline, it can be seen that to get low V_{TH} and steeper subthreshold swing without compromising the performance of the device, use of the right ferroelectric material and optimize the device structure to obtain maximum I_{ON}/I_{OFF} ratio and steeper subthreshold swing is very important [87].

4.2.5 Impact of Overlapping/Underlapping with different source materials on I_D/V_D

It can be seen in Figure 4.7 that output characteristics are better for Ge Source Heterojunction NCTFET. So, this configuration can be used to get a higher I_{ON} and stepper substhreshold swing.

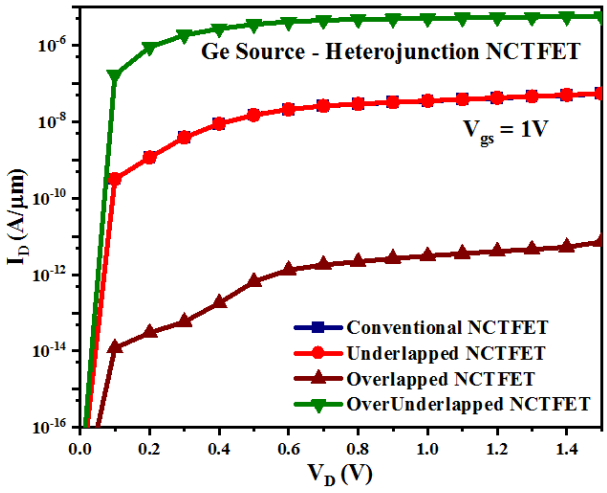


Figure 4.7: I_DV_D Characteristics in case of Conventional, Underlapped, Overlapped and Proposed NCTFET

4.3 Device architectures and their simulation setup

A novel structure of raised source NCTFETs is simulated (with gate stack overlapping the source) using Synopsys TCAD tool [74] utilizing the BTBT model and Landau ferroelectric equation. Device simulations have been performed in TCAD tool to predict the device behaviour and performance with better understanding of the physical mechanism of the device [88]. Due to high doping concentration of source and drain regions, Band-gap narrowing model and Fermi Dirac statistics model have been activated for the optimized device. The dynamic non-local BTBT model has been included at the tunnelling junction of proposed device due to tunnelling probability of the carriers. Landau-Khalatnikov (L-K) model is used to reflect the polarization of the FE material and Poisson equations are self-consistently calculated [89]. Figure 4.8 (a) and (b) shows the schematics of conventional TFET and Negative Capacitance (NC) TFET respectively.

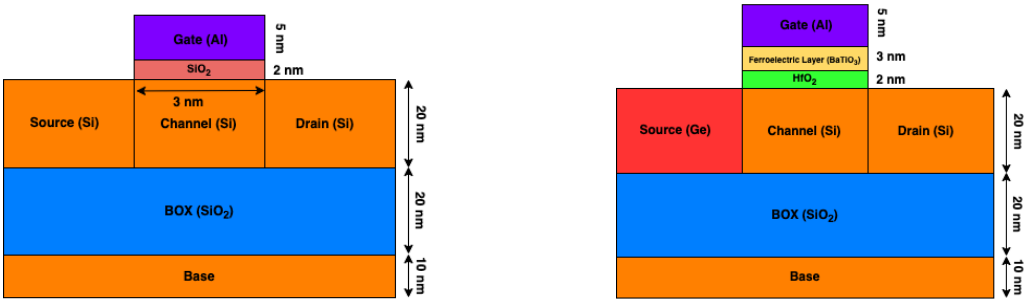


Figure 4.8: Schematic of (a) Conventional TFET and (b) Negative Capacitance TFET

Recently several structures have been engineered for TFET exhibiting line tunneling having overlapped gate/source/channel structure so that band to band tunneling becomes better and

I_{ON}/I_{OFF} is improved [90-91]. Figure 4.9 depicts a structure in which gate stack of NCTFET is shifted by 5 nm towards the source side.

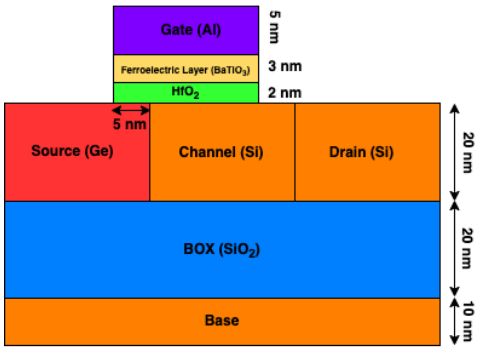
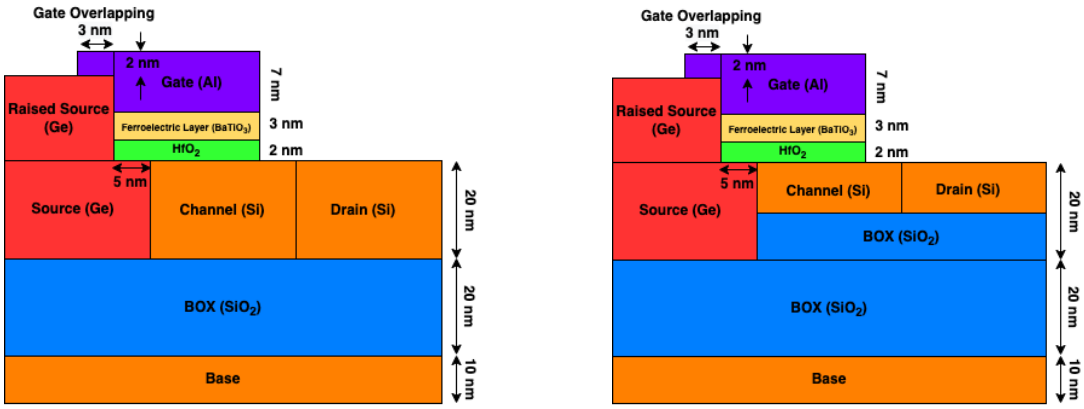


Figure 4.9: Schematic of Overlapped/Underlapped NCTFET

So, there exists an overlapped area of 5 nm source side and an underlapped area towards the drain side. But still if we analyse the electric field generation in this structure there exists an unwanted electric field at channel drain junction that need to be suppressed. With Raised Source NCTFET, certain short comings of TFET have been overcome but still there exists an unwanted electric field at gate/source junction which needs to be improvised. To overcome this, SiO_2 box is added to channel and drain size in order to suppress the field. Thus, the gate stack and source are raised and suppressing is done with the help of SiO_2 box as shown in Figure 4.10 (b).



(a) (b)

Figure 4.10: Schematic of (a) Raised Source NCTFET (b) Raised Source Suppressed Channel NCTFET.

The optimized NCTFET structure is identical to NCTFET, just a ferroelectric (FE) layer is added to the gate stack of TFET and gate stack is shifted towards source by 5nm. Table 4-3 summarizes the structural modifications done in conventional TFET to make Proposed NCTFET structure.

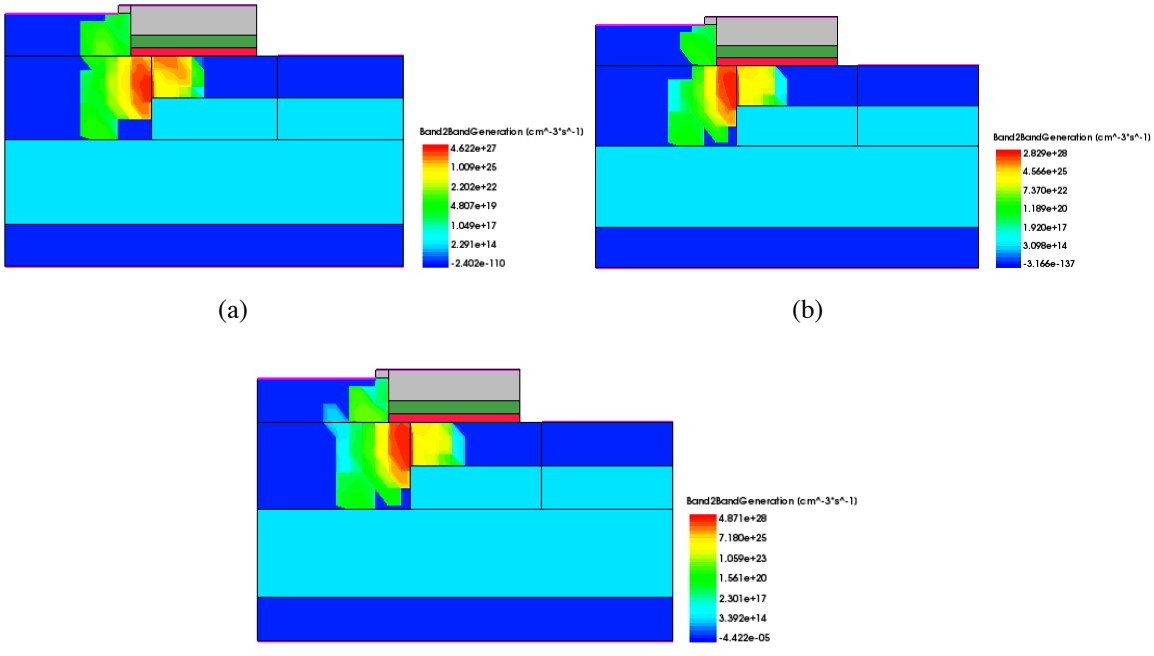
Table 4-3: Design changes done in Conventional TFET to Proposed NCTFET

Device	Structural Changes
Conventional TFET	Conventional TFET with 30 nm channel length and 7 nm Gate Stack
Conventional NCTFET	NCTFET formed by adding 3 nm Fe material in Gate Stack of Conventional TFET
Shifted NCTFET	Gate stack of NCTFET shifted by 5nm towards the source side
Raised Source Shifted NCTFET	Ge Source raised by 10 nm and Gate Overlapped by 3 nm to improvise the performance of device by enhancing the electric field generation and BTBT tunnelling
Proposed NCTFET	Channel and Drain region suppressed by adding SiO_2 Box of 50% thickness

4.3.1 Effect of Fe Material on performance of NCTFET

Different Fe materials provide different device performances. PZT (Lead Zirconate Titanate), $BaTiO_3$ (Barium Titanate) and P(VDF-TrFE) (Poly(Vinylidene Fluoride-trifluoroethylene)) have been used and analysed.

Following diagrams shows the electron band to band generation in case of PZT, P(VDF-TrFE) and $BaTiO_3$ materials as depicted in the Figure 4.11 (a), the band to band generation is highest in case of $BaTiO_3$ material (as in Fig 4.11 (c))



(a) (b)

(c)

Figure 4.11: Electron Band to Band Generation with (a) BaTiO3 (b) P(VDF-TrFE) (c) PZT Fe Materials

Further the transfer characteristics, output characteristics, energy band diagram and electrostatic potential generation are plotted in Figure 4.12 with $BaTiO_3$, P(VDF-TrFE) and

PZT material(s). It can be seen that in all the plots, $BaTiO_3$ is coming out to be the best choice with better characteristics and higher Electrostatic Potential.

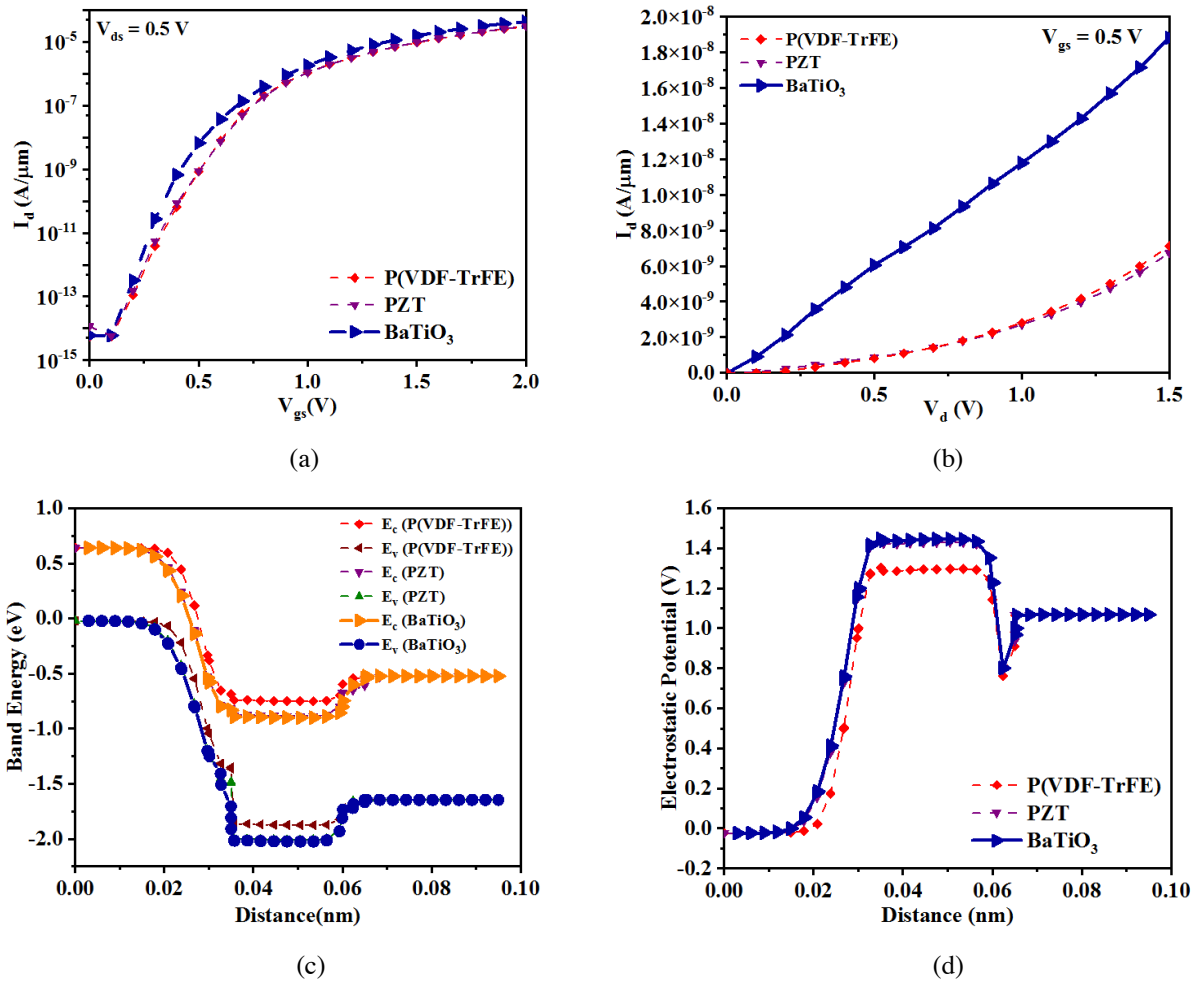


Figure 4.12 (a) I_DV_{GS} characteristics (b) I_DV_D characteristics (c) Energy Band Diagram (d) Electrostatic Potential of optimized NCTFET with different Fe materials.

4.3.2 Effect of Fe Thickness on performance of NCTFET

To minimize the ambipolar conduction and enhance the performance, NCTFET is equipped with Fe material, it can be clearly seen in Figure 4.13 that stronger electron band to band generation is obtained in case of optimized NCTFET with T_{FE} = 3 nm.

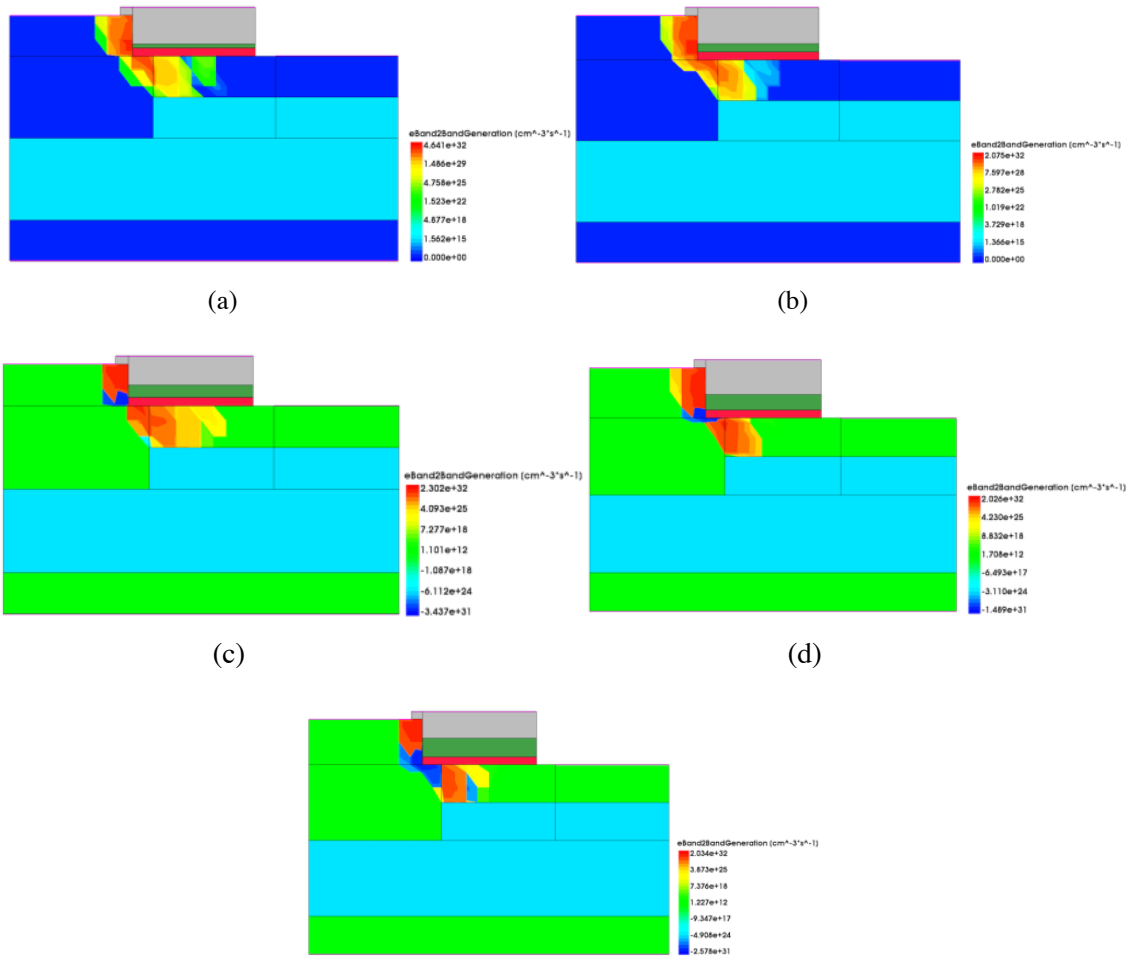


Figure 4.13 Electron Band to Band Generation in case of Fe Thickness (a) 1nm (b) 2 nm (c) 3 nm (d) 4 nm (e) 5nm

It is very important to choose the thickness of Fe material as the negative capacitance being generated makes the substhreshold slope steeper at the cost of I_{ON} current.

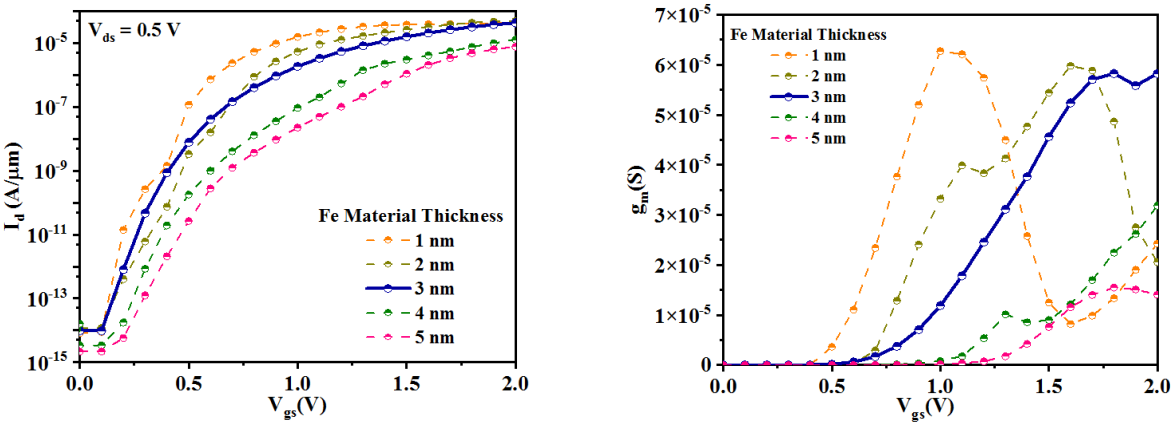


Figure 4.14 (a) $I_D V_{GS}$ characteristics (b) g_m plot for Optimized NCTFET with different Fe material thickness.

The transfer characteristics of optimized NCTFET are shown in Fig 4.14 (a) and g_m plot at different Fe thickness is plotted in Fig 4.14 (b). As depicted in the Fig 4.14 (a) the transfer characteristics obtained in case of T_{FE} = 3 nm for optimized NCTFET are having steepest SS and larger I_{ON} current. Moreover, g_m obtained in 3 nm thickness is not dropping throughout the entire voltage range of gate voltage.

From above figure, it may be very well seen that tunnelling width of NCTFET towards source-gate overlap is decreased at T_{FE} = 3 nm, which at last enhances the tunnelling probability and upgrades I_{ON} [92]. Moreover, due to increased tunnelling rate of charge carrier at the source-channel junction, super steeper subthreshold swing has been achieved. The other performance parameters obtained at various Fe thickness are tabulated in Table 4-4:

Table 4-4: Device Parameters at Different Fe Thickness

Parameter	**1 nm**	**2 nm**	**3 nm**	**4 nm**	**5 nm**
$\mathbf{V_{T\ (Transconductance)}}$	0.74	1.04	1.22	1.54	1.50
$\mathbf{V_{T\ (Common\ Current)}}$	0.48	0.66	0.65	1.01	1.19
Transconductance (g_m)	6.27	5.97	5.82	3.18	1.54
I_{ON}/I_{OFF} Ratio	2.9E+9	4.3E+9	**7.1E+9**	1.7E+9	1.7E+9
Subthreshold Swing (SS)	58	78	**53.7**	63	79

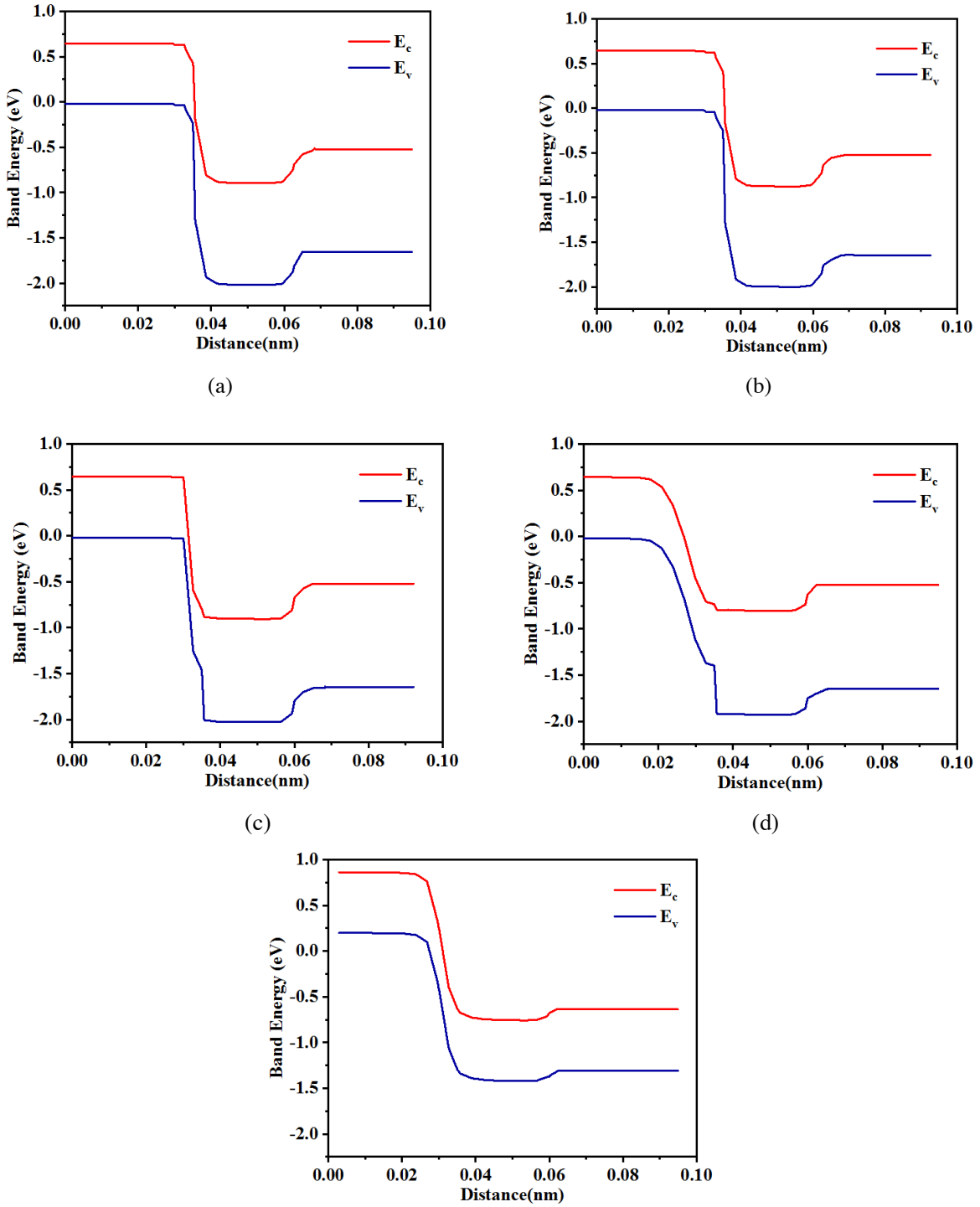
The electric field created towards the source is extremely strong for the structure with gate source overlap when compared to the structure without any overlapping [93-94]. This effect is due to speedy injection of charge carrier from the source which in turns is liable for not degrading the device's overall performance. It can be interpreted from experimental results that a stepper SS of NCTFET can be obtained when I_D is small. To achieve average SS < 60 mV/decade, we need to closely investigate that how NC effect will decrease the supply voltage V_{DD} at larger drain current I_D.

4.4 Comparison of device characteristics of various NCTFET structures

This section compares the energy band diagram, electric field generation, surface potential and Band to Band generation in various NCTFET devices. This in turns provides a clear insight into betterment of proposed NCTFET device over all other structures.

4.4.1 Energy Band Diagram of NCTFET Devices

Fig 4.15 (a) to (e) shows the energy band diagrams of Conventional TFET, Conventional NCTFET, Over-underlapped NCTFET, Raised source NCTFET and Proposed NCTFET respectively.



(a) (b)

(c) (d)

(e)

Figure 4.15: Energy Band Diagram in case of a) Conventional TFET, (b) Conventional NCTFET, (c) Over-underlapped NCTFET, (d) Raised source NCTFET and (e) Proposed NCTFET

It can be observed that better tunneling is obtained in case of proposed NCTFET as depicted by Fig 4.15 (e)

4.4.2 Electrical Field of NCTFET Devices

Fig 4.16 (a) to (e) shows the electric field generation in case of Conventional TFET, Conventional NCTFET, Over-underlapped NCTFET, Raised source NCTFET and Proposed NCTFET respectively. It can be observed from Figure 4.16 (e) that stronger electric field is obtained in case of proposed NCTFET.

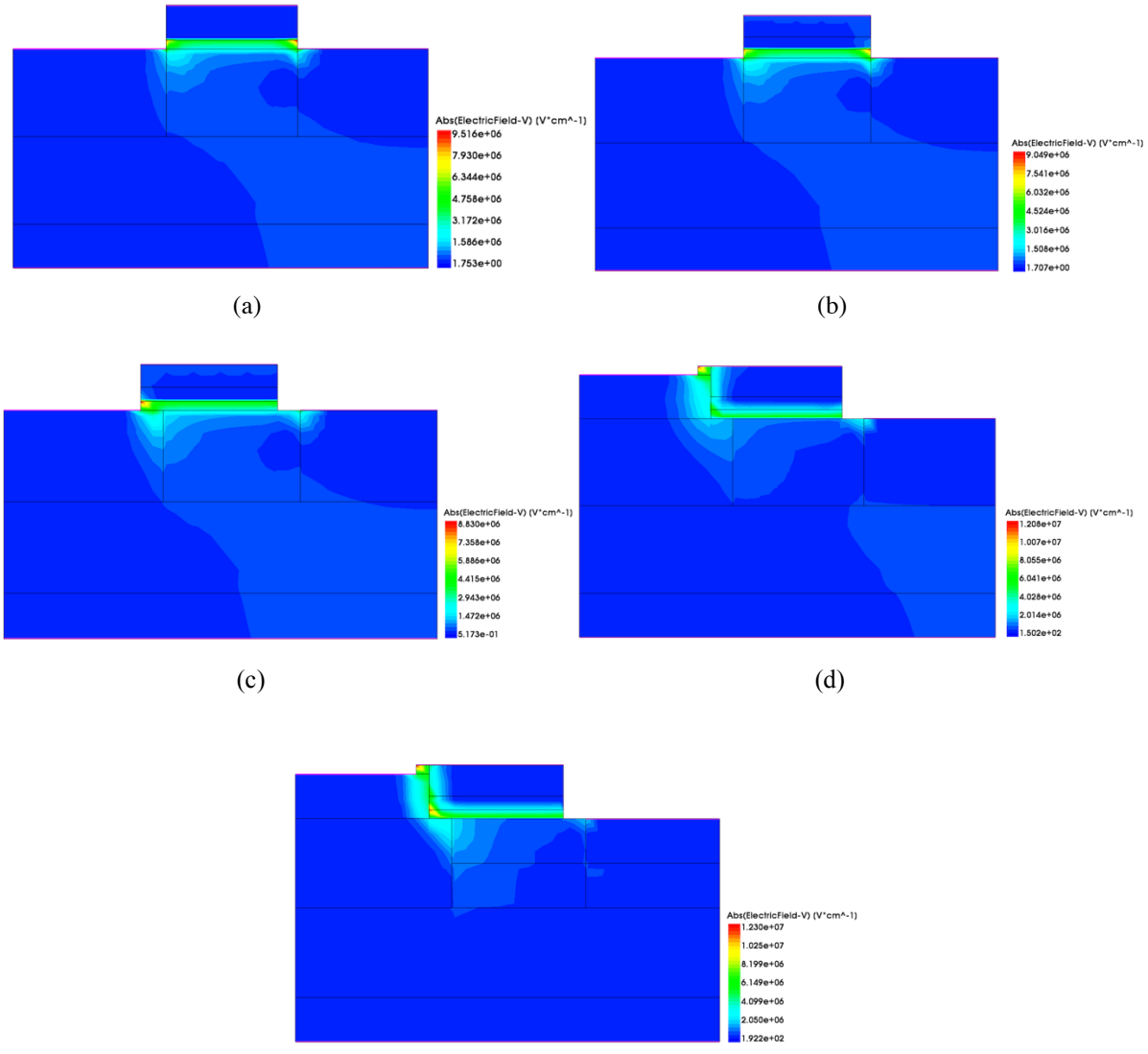


Figure 4.16: Electric Field Generation in a) Conventional TFET, (b) Conventional NCTFET, (c) Over-underlapped NCTFET, (d) Raised source NCTFET and (e) Proposed NCTFET

4.4.3 Electric Potential of NCTFET Devices

Fig 4.17 (a) to (e) shows the surface potentials of Conventional TFET, Conventional NCTFET, Over-underlapped NCTFET, Raised source NCTFET and Proposed NCTFET respectively. It can be observed from Figure 4.17 (e) that strong surface potential is generated in case of proposed NCTFET.

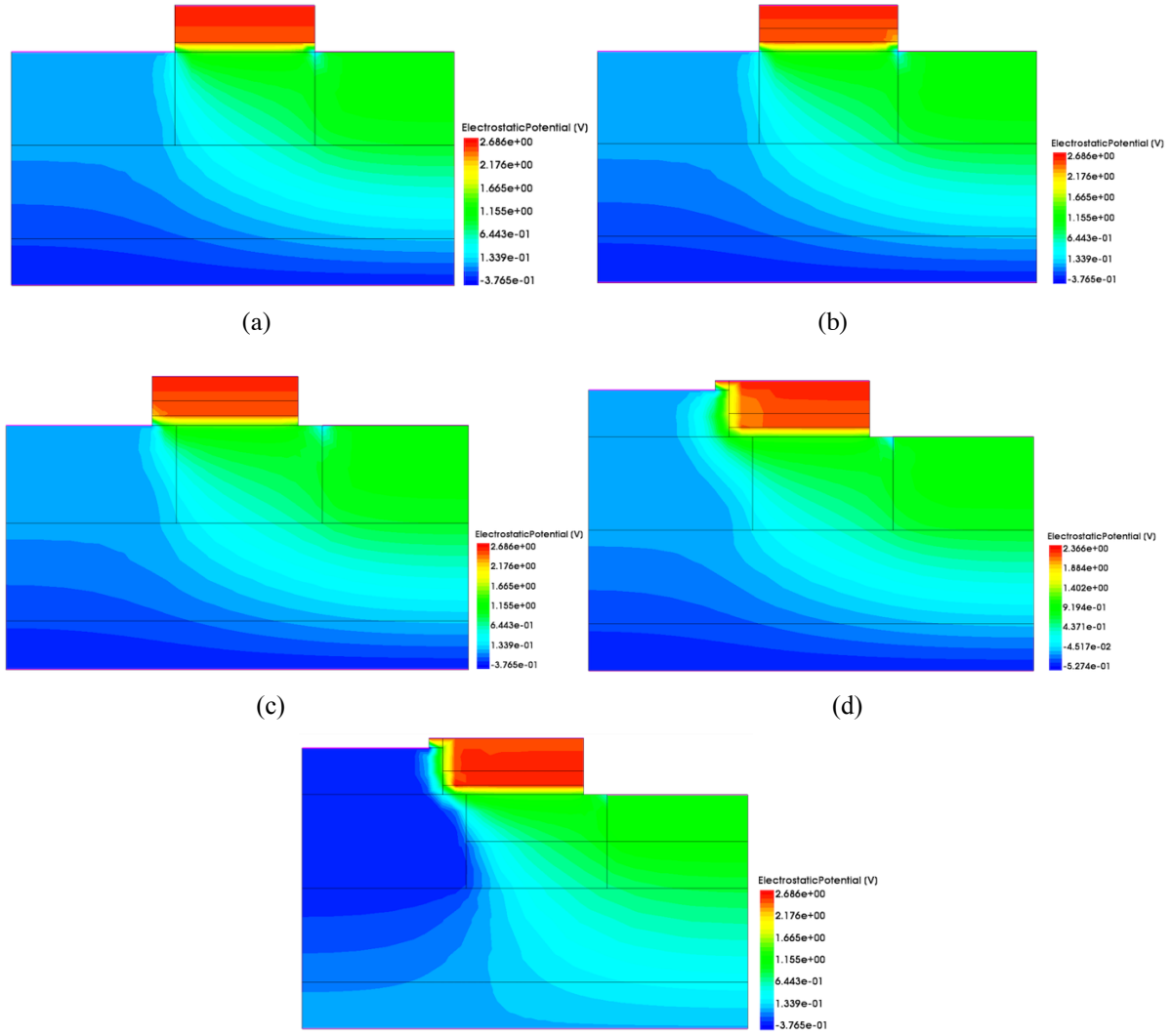


Figure 4.17: Surface Potential in a) Conventional TFET, (b) Conventional NCTFET, (c) Over-underlapped NCTFET, (d) Raised source NCTFET and (e) Proposed NCTFET

4.4.4 eBand to Band Generation of NCTFET Devices

Figure 4.18 (a) to (e) shows the e-band to band generations in case of Conv. TFET, Conv. NCTFET, Over-underlapped NCTFET, Raised source NCTFET and Proposed NCTFET respectively. It can be seen that narrower tunneling is obtained in case of proposed NCTFET as depicted by Figure 4.18 (e)

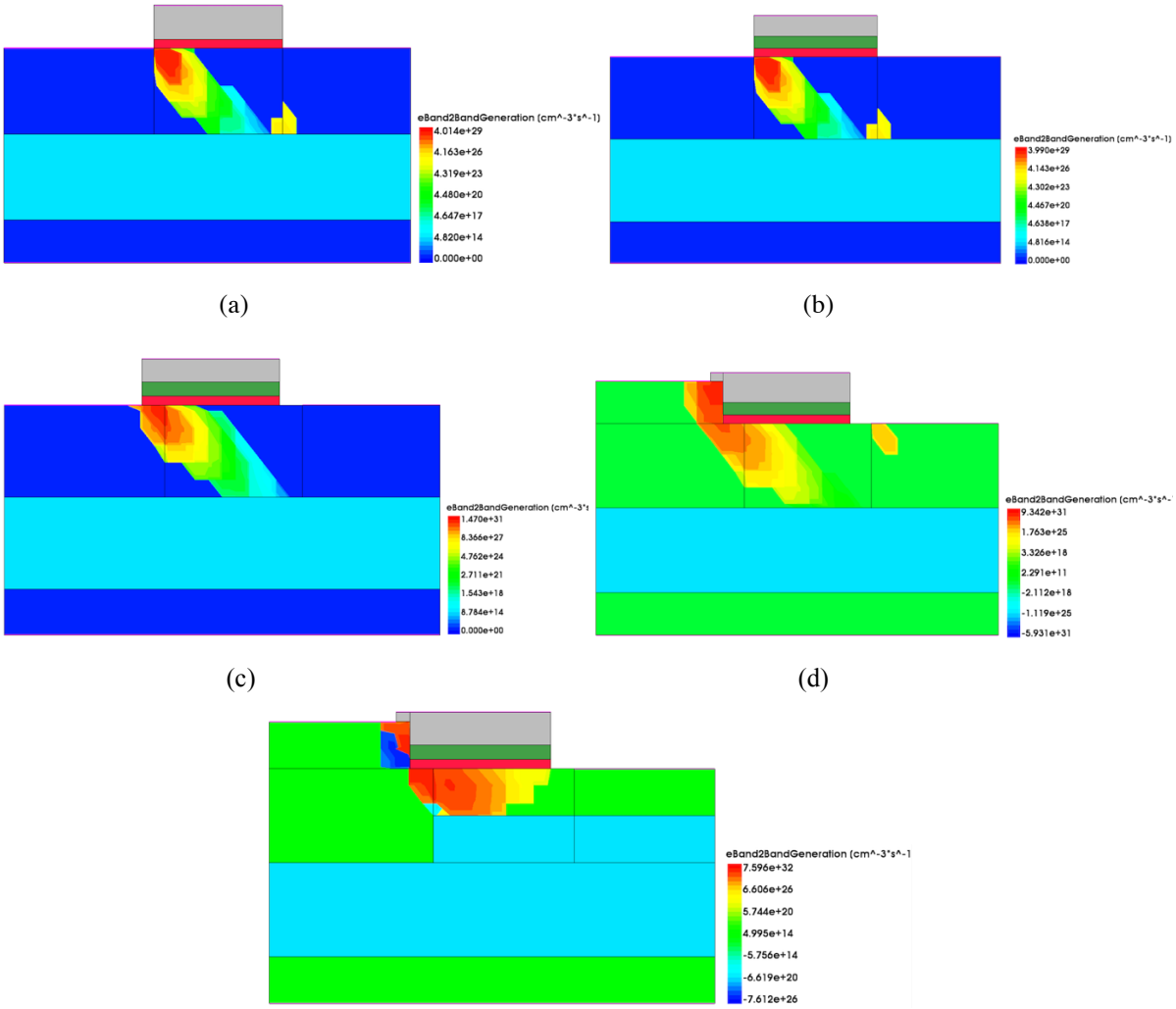


Figure 4.18: e-Band to Band Generation in a) Conventional TFET, (b) Conventional NCTFET, (c) Over-underlapped NCTFET, (d) Raised source NCTFET and (e) Proposed NCTFET

4.4.5 Transfer Characteristics of NCTFET Devices

Figure 4.19 shows the I_dV_{gs} characteristics of all NCTFET devices. V_{ds} is fixed at 0.5 V. In the proposed NCTFET device, the gate is overlapped to raised source by 3 nm that facilitates higher electric field generation and enhanced gate control which in turns improve the on-state current. Moreover, with the intervention of ferroelectric layer in the gate stack of TFET the subthreshold swing has been pulled down below 60 mV/decade [94]. In proposed NCTFET device both leakage current and on-current are low. The device shows ambipolarity as well. As depicted in the above graph, for proposed NCTFET structure the leakage current is minimum (~1E-14) and on current is highest (~1E-4), in comparison to the conventional TFET structure there is 99.9% decrease in I_{OFF} current and huge rise in I_{ON} current.

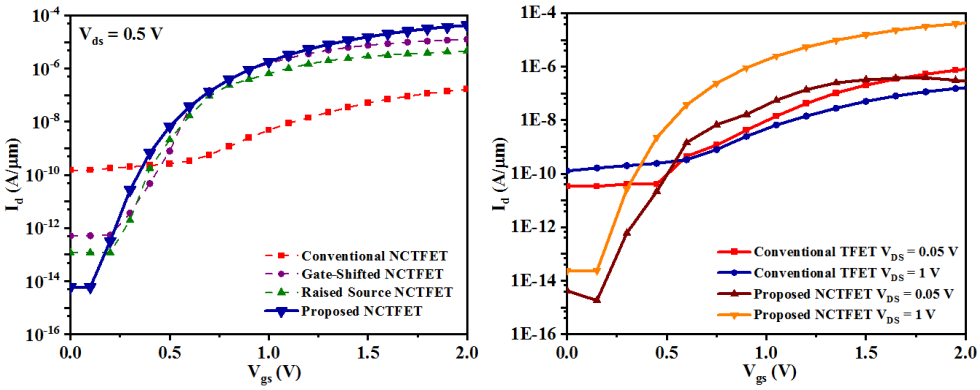


Figure 4.19: (a) Transfer characteristics of NCTFET devices (b) Plot for calculating DIBL

I_{ON}/I_{OFF} ratio for conventional TFET is $1.31x10^{+7}$ and for proposed NCTFET is $3.26x10^{+9}$. DIBL calculated for conventional NCTFET is 61.2 mV/V and for proposed NCTFET is 31.92 mV/V. So DIBL improvement of 52.2% has been achieved. Moreover, a stepper SS of 53.7 mV/decade has been obtained which is 69.8% steeper than the slope of conventional TFET.

4.4.6 Output Characteristics of NCTFET Devices

Figure 4.20 shows the output characteristics obtained for all NCTFET devices at V_{gs} = 1.0 V. From the results it can be observed that current saturation is not achieved at lower voltage as V_{ds} has more impact on charge carriers [96]. At higher V_{ds}, the effect of BTBT increases and drain current increases. As the maximum tunneling rate is achieved, the drain current saturates. As shown in Figure 4.20, highest on-state current is achieved in case of proposed NCTFET device [97].

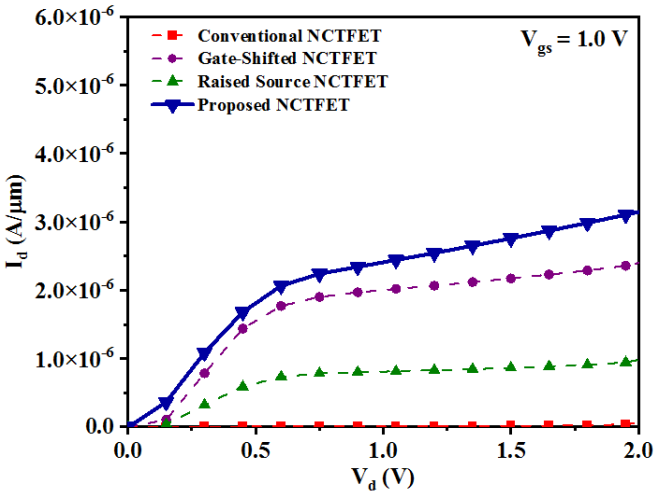


Figure 4.20: Output Characteristics of simulated devices

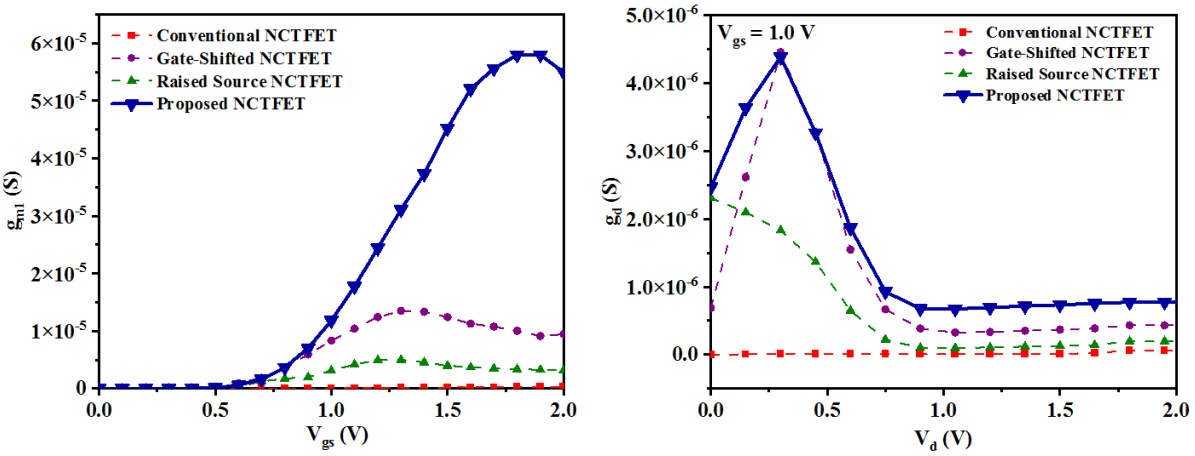
4.4.7 AC Analysis of NCTFET Devices

Radio Frequency plays a vital role in choosing the proposed device to be used in analog circuits. Transconductance (g_m) defines the amplification capability of device and is defines as the change in drain current with change in V_{gs} and can be expressed by equation 4.1:

$$g_m = \frac{\partial I_d}{\partial V_{gs}} \tag{4.1}$$

The g_m plots obtained for all device structures are shown in Fig 4.21 (a). As depicted in the plots among all the devices reported, proposed device structure has the maximum g_m values. With higher g_m value, proposed device can perform at higher switching speed due to faster conversion of volatge into current [98]. g_d is the reciprocal of output resistance and can be expressed by equation 4.2. The g_d plots for all the four structures are plotted in Figure 4.21 (b) and it is seen that maximum g_d is obtained in case of proposed NCTFET device.

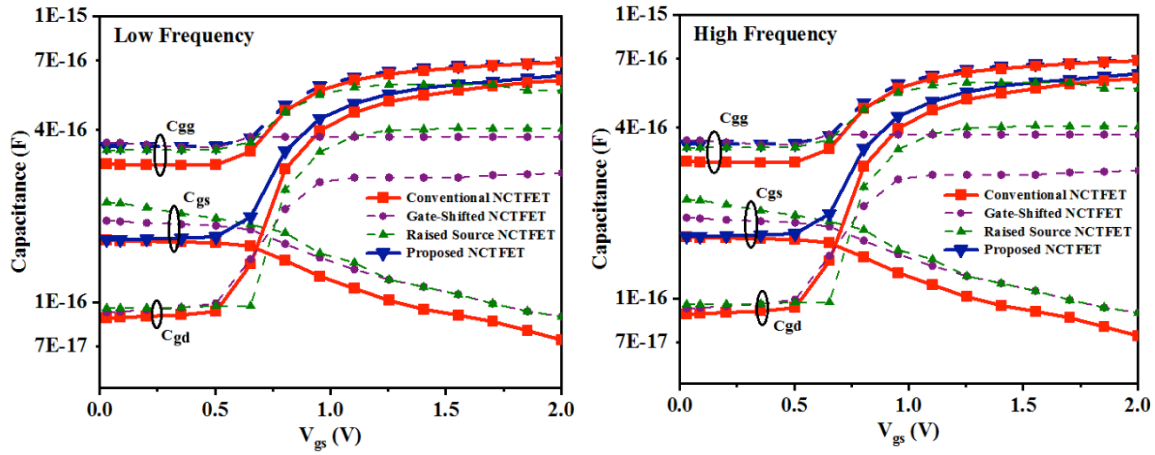
$$g_d = \frac{\partial I_d}{\partial V_{ds}} \tag{4.2}$$



(a) (b)

Figure 4.21: (a) Obtained Transconductance (g_m) (b) Output conductance (g_d) of simulated structures.

Capacitances of a device plays very crucial role in determining its AC performance. Figure 4.22 shows the variation in gate-drain capacitance (C_{gd}) and gate-source capacitance (C_{gs}) with V_{gs} for low frequency and high frequency. It is very clear from the plots that with increase in V_{gs}, C_{gd} increases rapidly but C_{gs} changes slightly. The sudden rise in C_{gd} is due to the accumulation of electrons at the gate-channel interface [99]. Plots received at low and high frequency have almost same values.



(a) (b)

Figure 4.22: Obtained Capacitance at (a) Low frequency (b) High frequency.

The intrinsic voltage gain (A_v) can be written as:

$$A_v = \frac{g_{m1}}{g_d} \tag{4.3}$$

A_v obtained for all the four structures implemented in this work are plotted in Figure 4.23 (a). As per the results obtained, it can be seen that at lower values of gate voltage the gain achieved is less for proposed NCTFET device and then there is an abrupt increase in value for higher gate voltages [25]. For devices other than proposed NCTFET, the value of gain is lesser. Cut-off frequency (f_T), Transit time (τ) and gain bandwidth product (GBP) are other prominent parameters for RF analysis. In HF circuits, higher value of f_T and GBP are required and the expressions for cut-off frequency, transit time (τ) and GBP are written as:

$$f_T = \frac{g_{m1}}{2\pi(C_{gd} + C_{gs})} \tag{4.4}$$

$$GBP = \frac{g_{m1}}{2\pi C_{gd}} \tag{4.5}$$

$$\tau = \frac{1}{2\pi f_T} \tag{4.6}$$

As per equation 4.4, f_T is directly varying with the increase/decrease in gm1 and is inversely proportional to total gate capacitance. While GBP is calculated at a fixed gain and is expressed as equation 4.5. The plot of f_T and GBP are shown in Figure 4.23 (b) and (c). The abrupt increase in gm1 increases the f_T and attains maximum value around 0.5 V. After that the steep fall in gm1 reduces the f_T. GBP of the proposed device has attained a maximum value at V_{gs} = 0.4 V and GBP decreases with the reduction in gm1 value [100]. Another important factor of

RF analysis is the time taken by charge carriers to travel from source to drain and is denoted by transit time. The results obtained for transit time are plotted in Figure 4.23 (d).

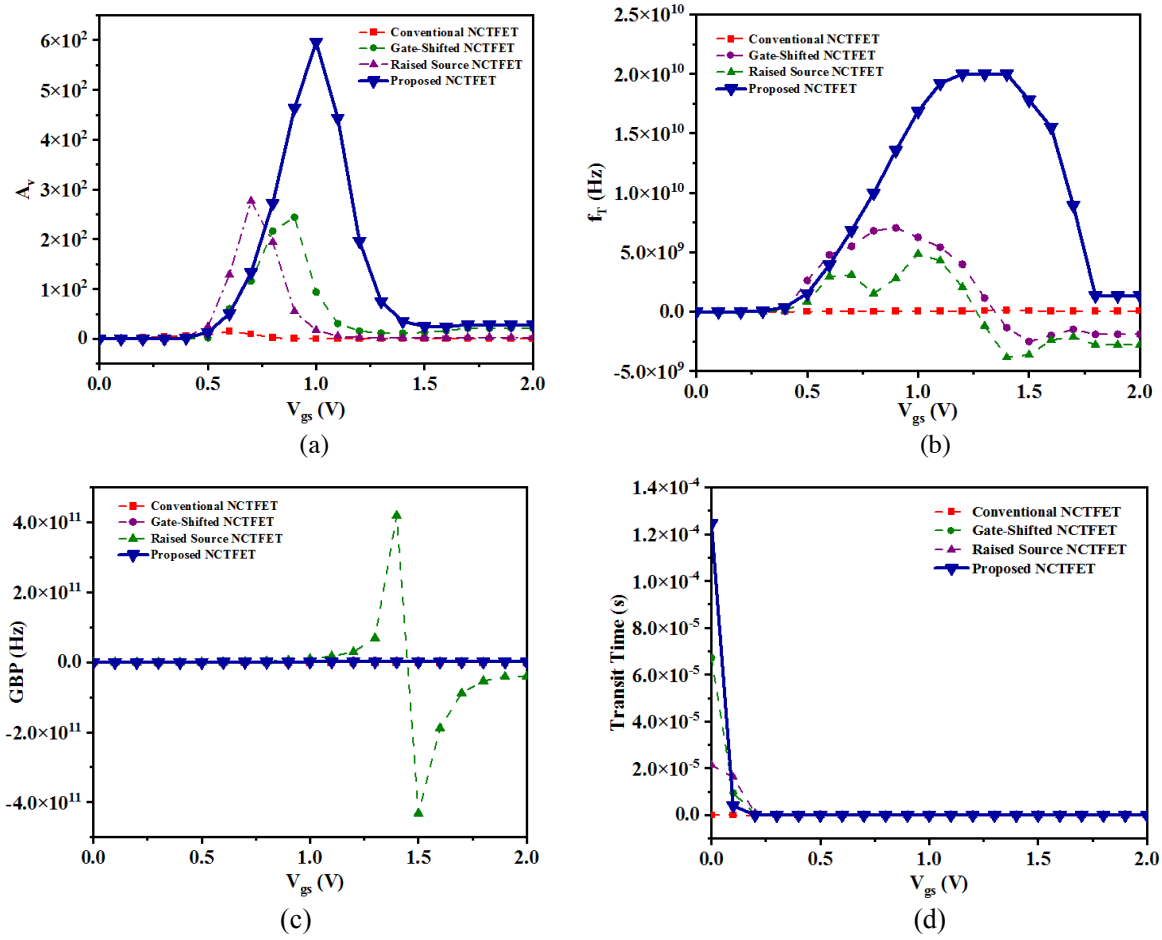


Figure 4.23: A_v, f_T, GBP and Transit Time plot for NCTFET Devices

4.4.8 Linearity and Distortion analysis of NCTFET devices

Linearity parameters (HD2, HD3, higher order transconductance (g_{m2}, g_{m3}) and third order intercept point (IIP3) are analysed in this work. The factors discussed in this section defines the performance of device with respect to linearity and distortions.

The transconductance and its coefficients can be written as:

$$g_{mn} = \frac{1}{n!}\frac{\partial^n I_{ds}}{\partial V_{gs}^n} \tag{4.7}$$

where n = 1, 2, 3

Figure 4.24 shows the plots for g_{m2} and g_{m3}. It has been seen in these plots that the proposed device has reached maximum values of g_{m2} and g_{m3}.

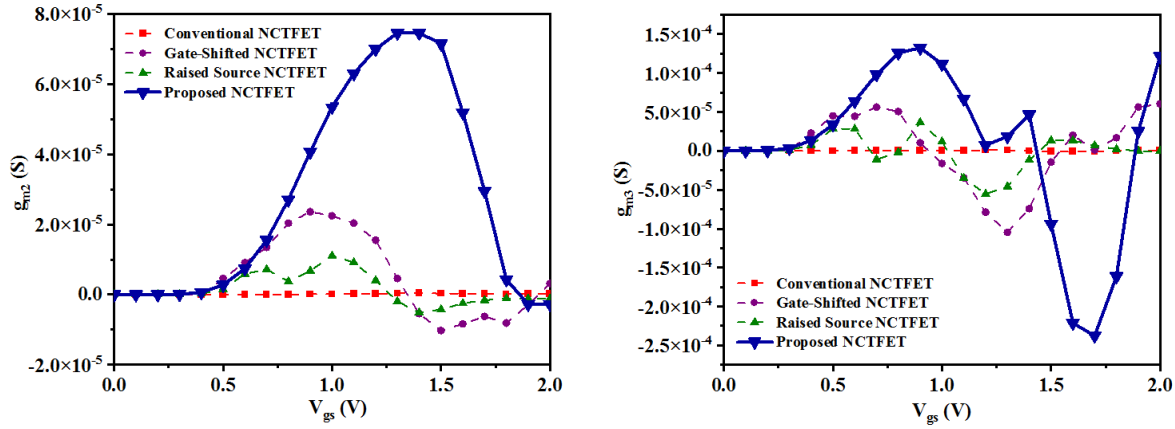


Figure 4.24: g_{m2} and g_{m3} plots for NCTFET devices

Next important factor associated is transconductance frequency product (TFP). It is an efficiency factor which defines a trade-off between power and bandwidth. Transconductance generation efficiency (TGF) depicts that how efficiently current is being converted to transconductance. TGF and TFP can be expressed as equation 4.8 and equation 4.9 respectively.

$$TGF = \frac{g_{m1}}{I_d} \tag{4.8}$$

$$TFP = \frac{g_{m1} f_T}{I_d} \tag{4.9}$$

The values obtained for TFP and TGF for all the devices considered in this work are plotted in Figure 4.25 (a) and (b). It has been seen that for N=1, 2, 3, TGF has attained maximum value for small V_{gs} and then decreases as SS slope deteriorates with the increase in V_{gs}. Although having higher values of TGF ensures that the amplification per unit drain current is better but it has some linearity issues [101-103].

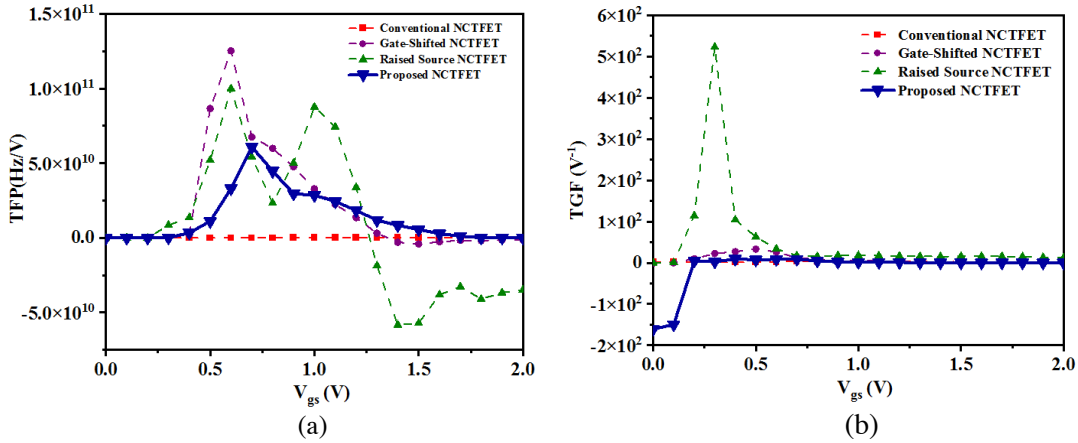


Figure 4.25 TFP and TGF plots for NCTFET devices

As shown in Fig 4.25 (b), for proposed device the TGF values remains almost same which in turns ensures the better linearity of the device.

Similar parameters are associated with the gain as well expressed in equation 4.10 and 4.11. Gain frequency product (GFP) and Gain transconductance frequency product (GTFP) have prime important in defining the performance index of the device in terms of linearity and distortions.

$$GFP = \frac{g_{m1}}{g_d} \times f_T \tag{4.10}$$

$$GFTP = \frac{g_{m1}}{g_d} \times \frac{g_{m1}}{I_d} \times f_T \tag{4.11}$$

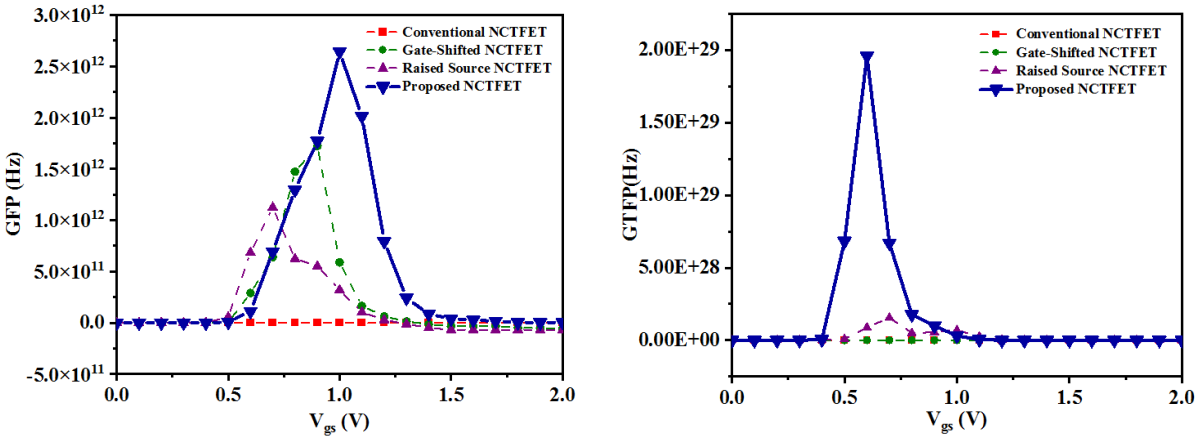


Figure 4.26 (a) GFP and (b) GTFP plots for NCTFET devices

As depicted in the graphs, with the increase in gain and f_T, the GFP and GFTP values increases in case of proposed NCTFET device [104]. Linearity parameters (HD2, HD3) and third order intercept point (IIP3) are associated with defining the linearity and distortions of the system. These are expressed as:

$$HD2 = \frac{1}{2} \times Vi \times \frac{g_{m2}}{2g_{m1}} dBm \tag{4.12}$$

$$HD3 = \frac{1}{4} \times V_i^2 \times \frac{g_{m3}}{6g_{m1}} dBm \tag{4.13}$$

Here V_i is the amplitude of input signal.

$$IIP3 = \frac{2}{3} \times \frac{g_{m1}}{g_{m3} \times R_s} dBm \tag{4.14}$$

IIP3 defines the extrapolated input power at which the first and third harmonic are equal. This unique parameter can serve as the factor to compare various circuits in terms of linearity.

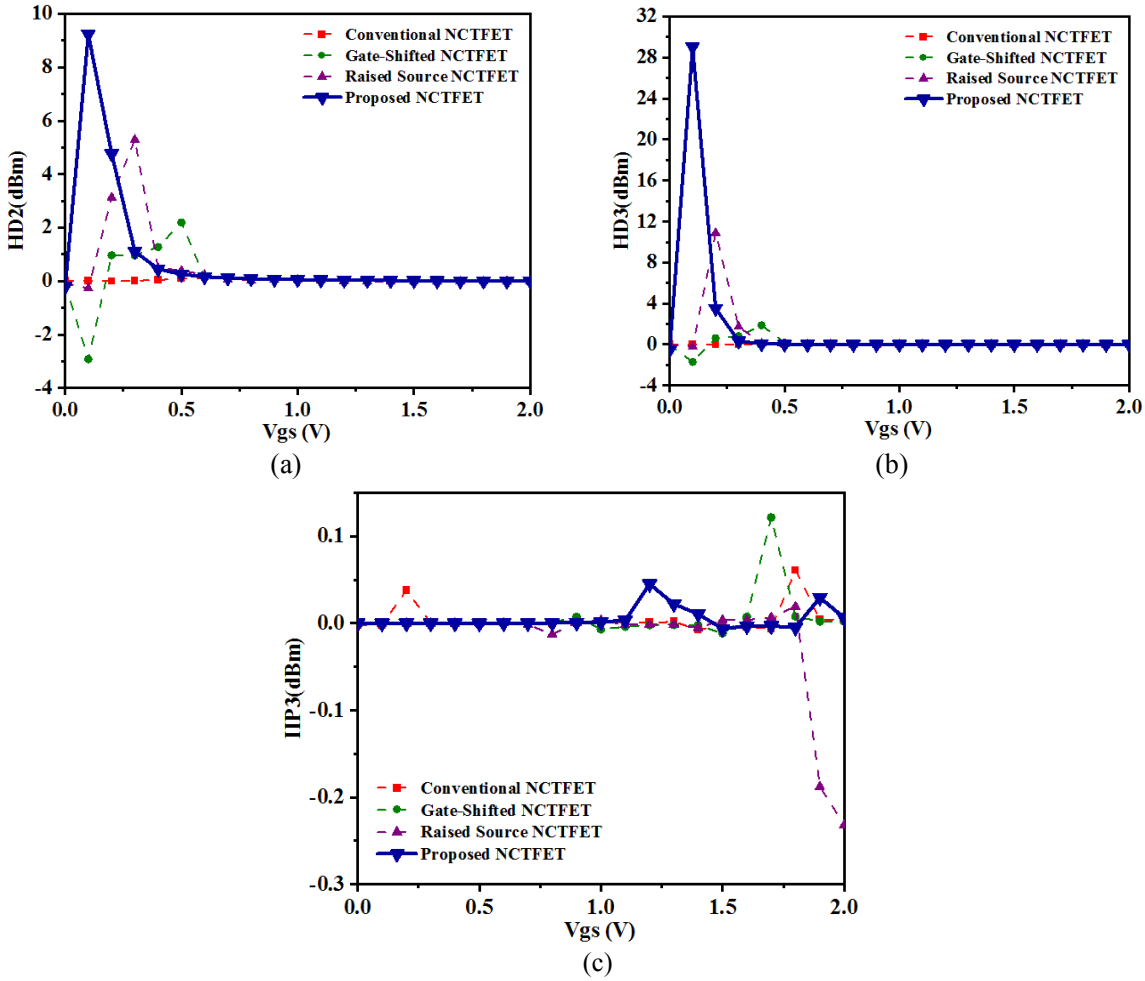


Figure 4.27: (a) HD2, (b) HD3 and (c) IIP3 plots for NCTFET Devices

The linearity factors are being plotted in Figure 4.27 The plots depict that Harmonic distortions (HD2 and HD3) have higher values when device is turned ON i.e. at low V_{gs}. But with the increase in V_{gs}, the distortions decrease [105].

4.4.9 Electrical Noise Analysis of NCTFET Devices

The impact of noise on the performance of device is discussed in this section taking different values of V_{gs} and frequency. The prominent parameters associated with this study are drain current noise spectral density (S_{ID}) and voltage noise spectral density (S_{vg}). These can be expressed as:

$$S_{ID} = \frac{q^2 kT\lambda N_t}{C_{ox}{}^2 WL_{eff} f^{\gamma}} \frac{I_d{}^2}{(V_{gs} - V_t)^2} \qquad S_{VG} = \frac{q^2 kT\lambda N_t}{C_{ox}{}^2 WL_{eff} f^{\gamma}} \tag{4.15}$$

where, q is charge, Vt denotes the threshold voltage, T is temperature, W is the width of the device, V_{gs} denotes the gate-to source voltage, N_t is the interface trap density, k is Boltzmann constant, L is effective channel length, C_{ox} is the oxide capacitance per unit of area, λ is a tunneling parameter, f is the frequency [107].

Figure 4.28 shows S_{ID} vs. V_{gs} of various TFET structures at low frequency and high frequency. As heterojunction TFET structure exhibits high current noise spectral density than homojunction so least effect of noise is seen in proposed NCTFET structure [108].

Due to fluctuations of charge carries in the channel, there exists an electrical noise. In TFETs, these carriers are determined by BTBT generation rate. At lesser values of V_{gs}, small fluctuation of charge carriers occurs but as the V_{gs} is increased BTBT generation rate increases thus fluctuation of charge carriers increases. S_{ID} at high V_{gs} increases compared to low V_{gs}. Nonetheless, S_{ID} is inversly proportional the frequency, reduced values of noise is observed at high frequency than at low frequency [109].

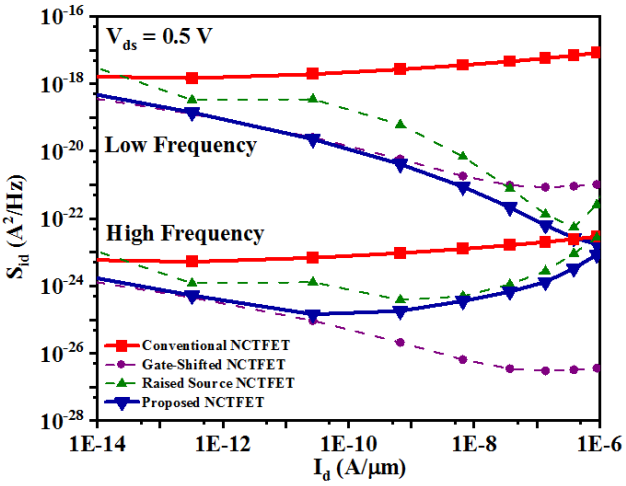


Figure 4.28: S_{ID} vs. I_d at Low frequency and High frequency.

For all four NCTFET devices, the analysed voltage noise spectral density (S_{vg}) is shown in Figure 4.29. It has been observed that among all the four devices, the least effect of noise is seen in gate-shifted NCTFET while proposed device shows maximum effect of noise. Due to inverse dependence of noise on frequency, with increase in frequency, the effect of noise is more at high frequency as compared to low frequency [110].

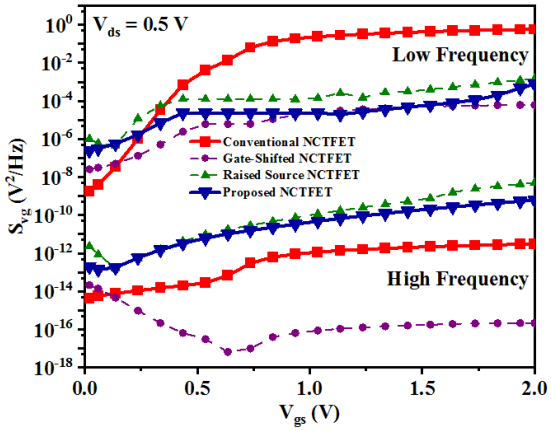


Figure 4.29: S_{vg} vs. V_{gs} at Low and High frequency

Table 4-5 shows the change in drain current noise spectral density (S_{ID}) at various frequencies for all NCTFET devices.

Table 4-5: S_{ID} vs Frequency

Frequency (Hz)	S_{ID} (A^2/Hz)			
	Conv. NCTFET	Overlapped NCTFET	Raised Source NCTFET	Proposed NCTFET
10	2.98E-17	3.56E-21	2.70E-20	4.79E-23
10^2	2.97E-17	3.54E-21	2.69E-20	4.77E-23
10^3	2.33E-17	2.78E-21	2.11E-20	3.75E-23
10^4	1.58E-17	1.88E-21	1.43E-20	2.53E-23
10^5	1.46E-17	1.74E-21	1.32E-20	2.36E-23
10^6	1.04E-17	1.25E-21	9.50E-21	2.53E-23
10^7	3.60E-19	4.30E-23	4.29E-22	2.98E-23
10^8	3.69E-21	4.40E-25	1.09E-22	2.99E-23
10^9	3.69E-23	4.44E-27	1.06E-22	2.99E-23

V_{ds} is kept at 0.5 V and V_{gs} is kept at 1.0 V

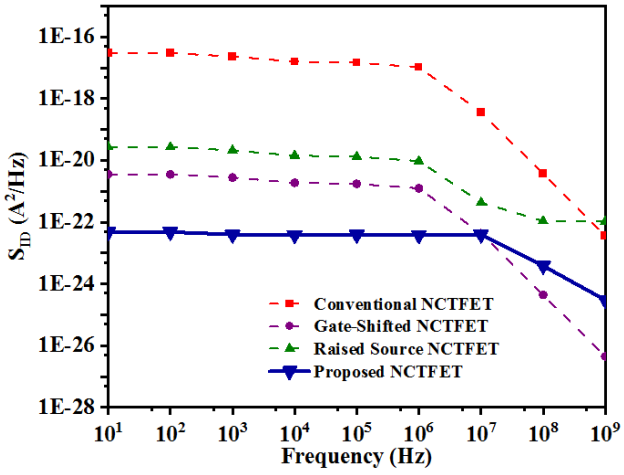


Figure 4.30: S_{ID} vs. Freq plots for NCTFET Devices

The effect of traps on noise current spectral density (S_{ID}) and noise voltage spectral density (S_{vg}) is plotted in figure 4.31. It can be clearly observed from the trapping and de-trapping of thermally generated carriers is high. With the increase in V_{gs} voltage, BTBT also increases which in turns has a direct impact on trapping and de-trapping.

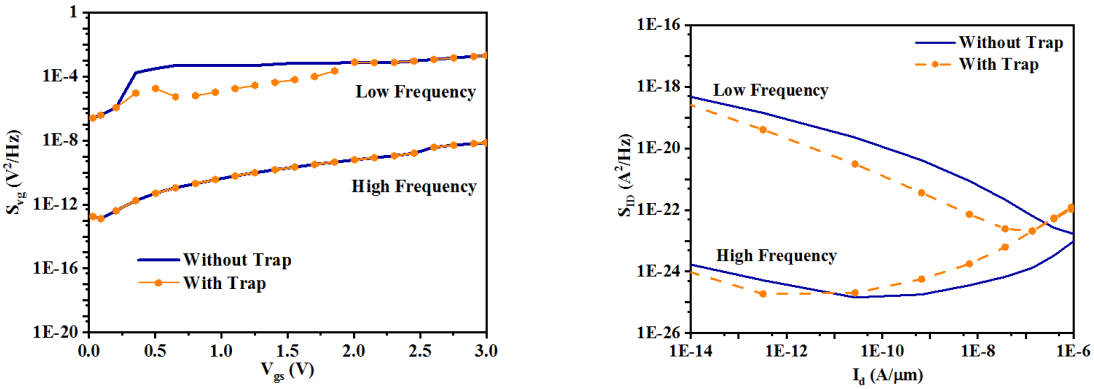


Fig. 4.31. (a) Plot of S_{vg} v/s V_{gs} (b) Polt of S_{ID} v/s I_d at low and high frequency

Based on the results obtained, is can be clearly seen in plot that the drain current noise spectral density is minimum for the proposed NCTFET device structure and decreases with the increase in frequency [111].

After comparison of TCAD simulation for conventional, overlapped, raised source NCTFET structure using Si and Ge as source material, it has been found that raised source structure of NCTFET provides good performance and values of I_{ON}, I_{OFF} and Subthreshold slope (SS) obtained are $4.295*10^{-5}$ A/μm, $6.01*10^{-15}$ A/μm, 53.75 mV/decade respectively. DIBL calculated for conventional NCTFET is 61.2 mV/V and for proposed NCTFET is 31.92 mV/V. So DIBL improvement of 52.2% has been achieved. Moreover, the effect is noise is lesser in heterojunction NCTFET than homojunction NCTFET. The reported devices are analysed in terms of DC analysis, AC analysis, Noise and Linearity analysis. Overall an improvised performance has been achieved in raised source heterojunction NCTFET and the optimised device can be used in wide range of low power applications. In summary, this work discusses the AC and Linearity parameters for the proposed device and has shown its clear comparison with the conventional NCTFET.

CHAPTER 5: IMPLEMENTATION AND ANALYSIS OF LOW POWER INVERTER AND 1T DRAM MEMORY USING PROPOSED NCTFET DEVICE

TFETs are emerging as a strong replacement device for MOSFETs in power efficient circuits due to their ability to give subthreshold swing lesser than 60 mV/decade and superior switching characteristics at ultra-low V_{DD}. This chapter explains the use of proposed device in making inverter and DRAM memory element.

5.1 Implementation of Inverter using proposed NCTFET device

The proposed device in this work is used to make inverter and its characteristics are plotted and analysed. TFETs ability to provide SS lesser than 60 mV/decade gives an advantage to use this in inverter circuits and the I_D-V_{DS} characteristics at smaller values of V_{out} is crucial. So smaller inverse subthreshold swing facilitates rapid change of I_D with respect to V_{in} is required and this in turns provide a large voltage gain and sufficient noise margins in the inverter transfer characteristics.

Figure 5.1 shows the schematic of n-type NCTFET device using Ge source to form a heterojunction at source channel junction. To maintain low leakage current, channel and drain are made up of larger bandgap Si material. So, with the change of smaller bandgap material to higher bandgap material better tunneling takes place which provides higher increment in I_D current [112].

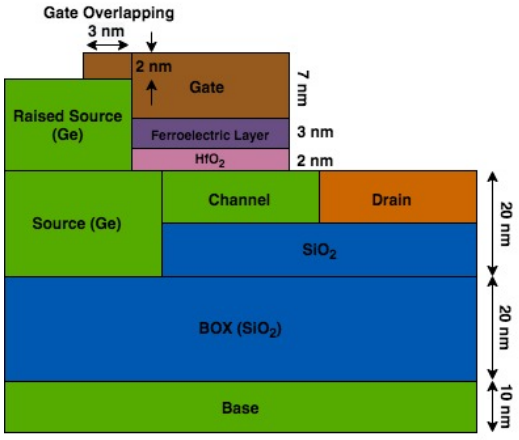


Figure 5.1 Schematic of Proposed NCTFET Device

The proposed NCTFET is implemented as a complementary TFET as shown in Figure 5.2. The transfer characteristics of N-NCTFET and P-NCTFET are plotted in Figure 5.3 showing the variation in drain current I_D as a function of V_{gs} voltage. A mixed mode C-TFET inverter is simulated in Synopsys TCAD.

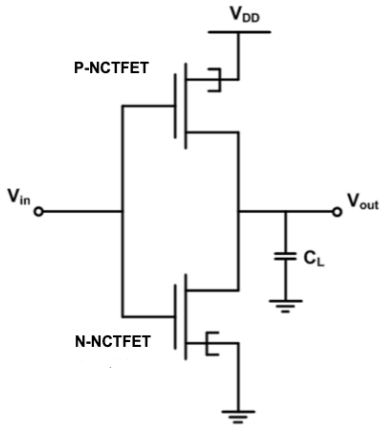


Figure 5.2: Schematic of NCTFET Inverter

As per the circuit shown in Figure 5.2, N-NCTFET and P-NCTFET are used to make an inverter and the performance of inverter made is analysed at various values of V_{DD} as shown in Figure 5.4 and 5.5 [113-114].

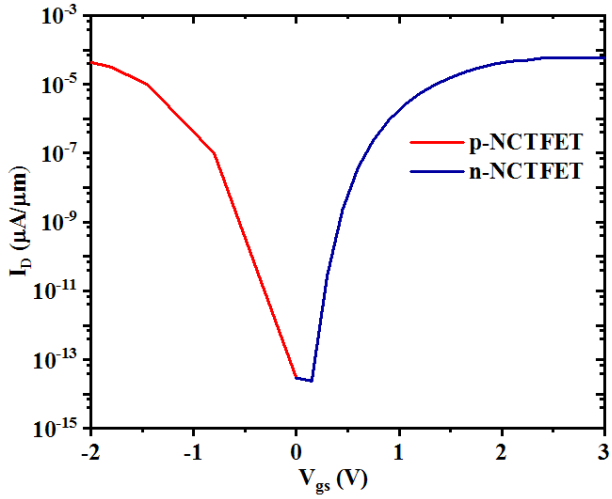


Figure 5.3: Transfer characteristics of N-NCTFET and P-NCTFET devices

5.1.1 Inverter Characteristics

In addition to the transfer characteristics of inverter with n-type and p-type NCTFET characteristics, V_{out} v/s V_{in} plot is equally important to see the voltage transfer characteristics (VTC) of NCTFET inverter. A sharp transition is seen at V_{DD} as low as 0.5 V as seen in Figure 5.4 (a) in case of conventional NCTFET.

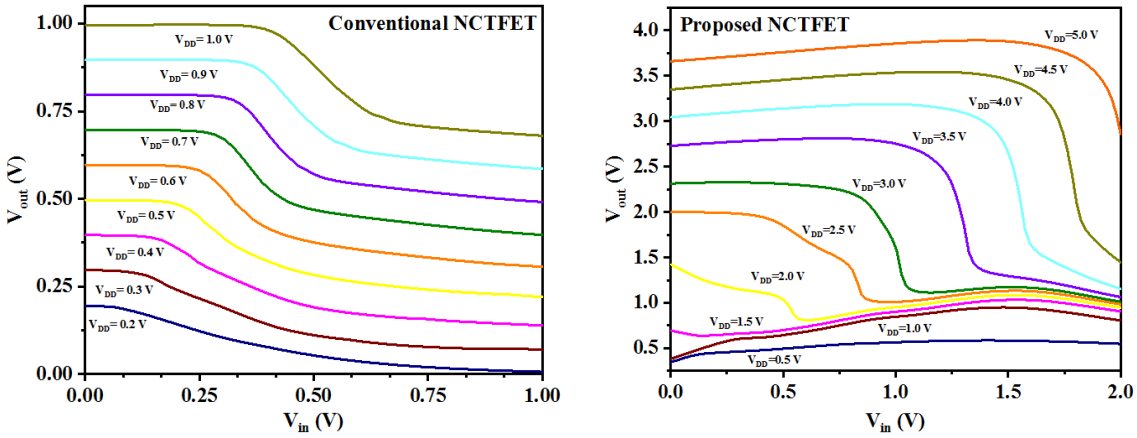


Figure 5.4: Voltage transfer characteristics of NCTFET Inverter

Another important plot is Figure 5.5 in which the voltage gain is plotted against the input voltage to the inverter.

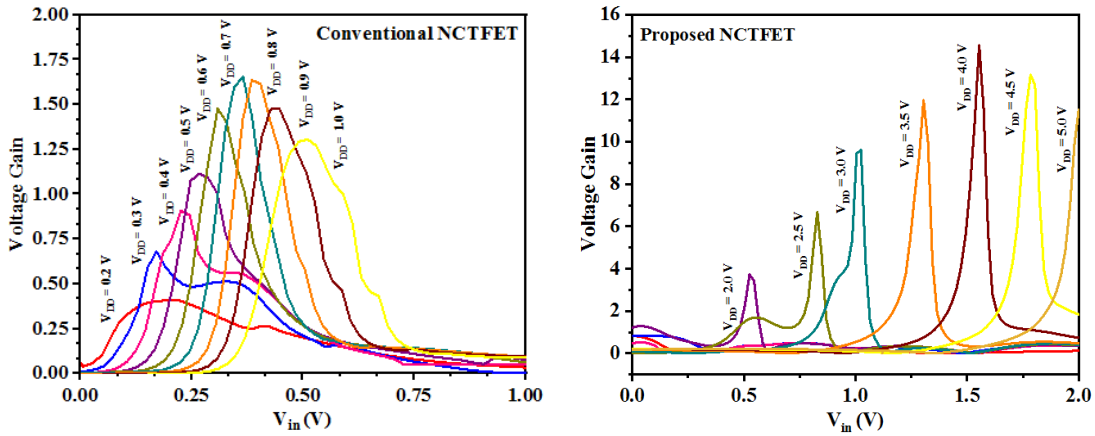


Figure 5.5: Plot of Voltage gain v/s V_{in} at different values of V_{DD}

The voltage gains $\Delta Vout/\Delta Vin$ is obtained at different values of V_{DD}. In conventional NCTFET, highest gain of 1.65 is obtained at $V_{DD} = 0.7$ V. The highest value of gain in proposed NCTFET (i.e. 14.13) is obtained at $V_{DD} = 4.0$ V and even keeping $V_{DD} = 0$ V, gain of 1.64 is obtained. The output voltage (V_{out}) shows degradation due to ambipolar behaviour of Complementary TFET when $V_{out} < V_{DD}$ at lower values of V_{in} and $V_{out} > 0$V at higher values of V_{in} [115-116]. So, with 5 magnitude change in V_{DD} voltage, we are able to achieve tremendous increase in gain (8.5 times) of inverter circuit with proposed NCTFET device.

5.2 Implementation of 1T-DRAM using proposed NCTFET device

With the continuous scaling of integrated circuits, dynamic RAM memory industry has also achieved success in packing more and more bits per unit area in a silicon die. The scaling of capacitance is difficult as compared to conventional transistors so the optimal design of 1T/1C DRAM memory cell has attracted attention due to ability of achieving higher memory cell

density and to solve the problems associated with scaling of physical capacitor [117-118]. There are several improvisations and experiments associated with solving this problem in literature. Tunnel field effect transistors have been reported in literature to be an efficient alternative for making capacitor-less DRAM units with reduced leakage current and improved switching energy. Based on band to band tunneling generation, the extra hole charges are generated into the body which is effective in maintaining the 1-state current level in DRAM cell. The device proposed in this work has been utilized to make a 1T DRAM cell and is capable of operating at a much lower input voltage as compared to conventional devices offering higher data rate and memory density.

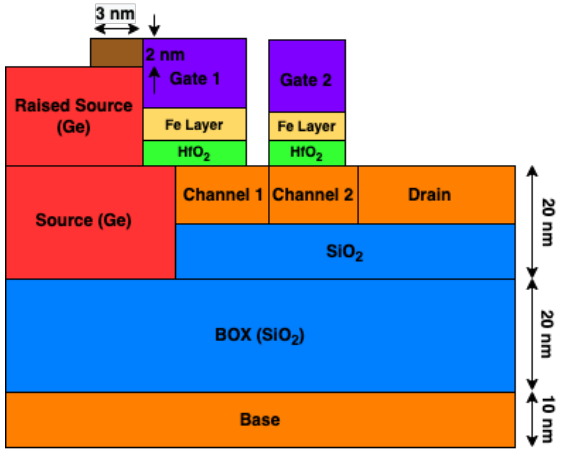


Figure 5.6 Schematic of 1-T DRAM using NCTFET

Figure 5.6 shows the schematic of 1-T DRAM cell capable of creating a potential well which is used to store the extra holes generated from the source to channel junction when the back-gate voltage is accumulated. Various new device architectures, materials and integration techniques have been reported in literature [119-121]. Two separate gates have been used in structure where a Ge storage area is made under GATE 2 and different channel doping is used in the region for holding the charge carriers. The working of DRAM cell depends on the BTBT mechanism and for effective tunneling, L-Shaped GATE1 is used which has a larger cross-sectional area for band to band tunneling. The hole concentration in storage region represents the write '1' and '0' operations. Table 5-1 shows the parameters of proposed memory cell. GATE1 is incorporated to do read operations whereas GATE 2 is employed for write and hold operation. The optimised length used for GATE1 and GATE2 is specified in Table 5-1.

Table 5-1: Device Dimensions and Simulation Parameters

Parameter	1T NCTFET DRAM
Silicon Thickness	10 nm
Gate Oxide Thickness	2 nm
Fe Material Thickness	3 nm
Channel 1 Doping (cm-3)	1×10^{16}
Channel 2 Doping (cm-3)	1×10^{18}
S/D Doping	1×10^{20}
Gate Work function	4.45
Gate 1 Length	14 nm
Gate 2 Length	12 nm
Source Height	10 nm

5.2.1 Write '1' operation

In this operation, negative bias is applied across V_{G2S}= -0.75V and 0V is applied at V_{G1S}. With this applied biasing, with the reduction in the barrier width electrons tunnels from VB of channel region to CB of drain region [122]. The energy band diagram is shown in Figure 5.7. As the barrier width reduces, tunneling occurs from channel to drain region this the hole concentration increases in the storage region (seen in Figure 5.7)

5.2.2 Write '0' operation

In this operation, positive bias of 0.75V is applied across V_{G2S} which helps in evacuating the holes from storage region to drain region. The number of holes in storage region thus reduces as compared to write '1' operation.

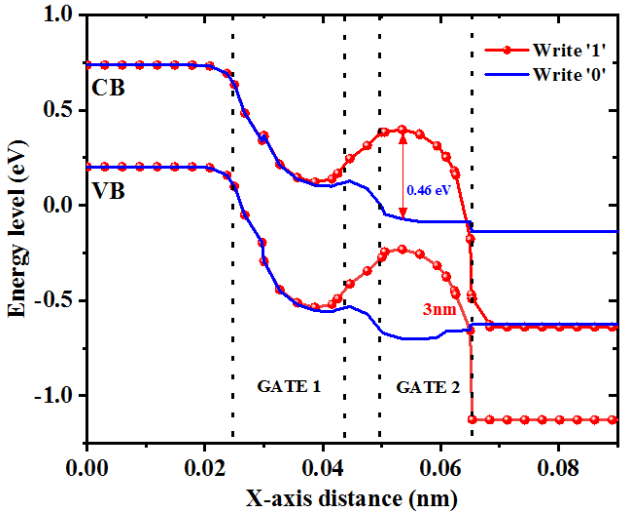


Figure 5.7: Energy band diagram during Write '1' and '0' operation

5.2.3 Hold operation

A negative bias of -0.25V is applied across V_{G2S}, for hold 1 operation, so as to keep the holes intact in storage region. As seen in Figure 5.8 during hold 0 operation 0.22eV potential barrier has been maintained beneath G2 as compared to hold 1 operation.

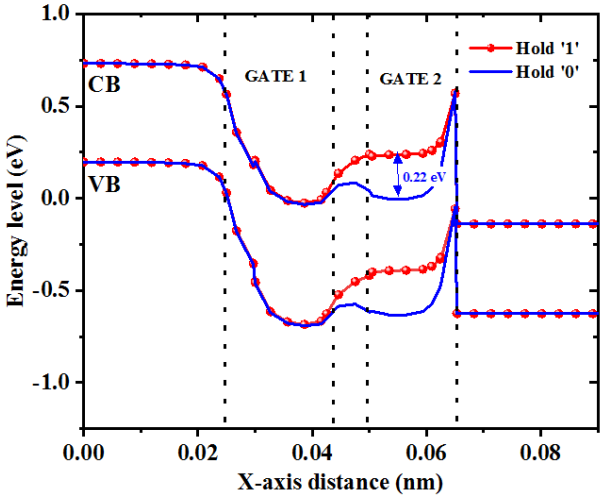


Figure 5.8: Energy band diagram during Hold '1' and '0' operation

5.2.4 Read operation

The read operation is dependent on G1 and drain voltage so a positive voltage of 0.5V is applied across drain and V_{G1S} is kept at 0.75V. With the application of positive bias at G1, the tunneling barrier width near the source-channel junction reduces and electrons from valence band of source tunnels to conduction band of channel. Moreover, the electrons drift from the channel to drain region due to positive potential applied at drain terminal. From Figure 5.9, it can be observed that potential barrier during read '0' operation is underneath of G2 by approximately 0.43eVs as compared to read '1' operation. The following biasing conditions are used to carry various memory operations.

Table 5-2: Biasing Conditions of 1T DRAM

Operations	**V_{DS} (V)**	**V_{G1S} (V)**	**V_{G2S} (V)**
Write '1'	**0.5**	**0.0**	**-0.75**
Write '0'	**0.0**	**0.0**	**0.75**
Hold	**0.0**	**0.25**	**-0.25**
Read	**0.5**	**0.75**	**0.0**

Depending upon the value to be written the data line is pulled up or pulled down thus the read operation has to be followed by a write-back so that the data to be read must not return a vague or corrupted bit.

For data = 1, the data line is to pre-charged to $V_{DD}/2$. If the stored data is '1', due to charge sharing, the voltage of data line rises slowly. The small change in voltage of data line is detected by sense amplifier and returns '1' as stored value. Same is followed for read '0' operation. The charge/discharge takes longer time as data line is having large capacitance, so sense amplifiers is required to efficiently detect the logic '1' or logic '0' values.

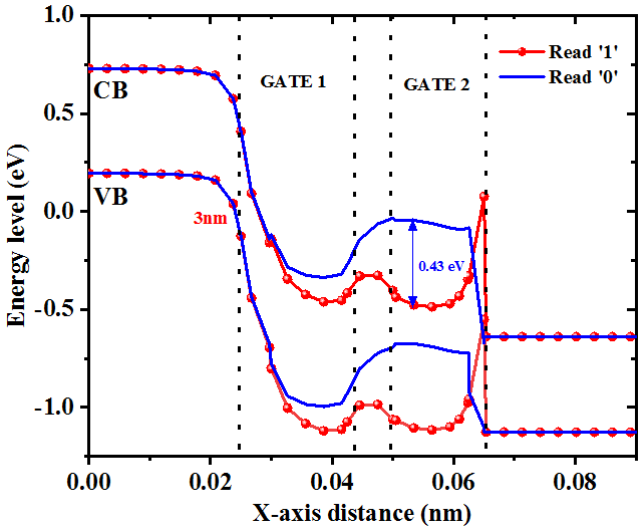


Figure 5.9: Energy band diagram during Read '1' and '0' operation

As seen in Table 5-2, the operating voltage is much lesser than the conventional TFET structures. 1T DRAM cell made from proposed NCTFET has the capability to perform fairly good in low power circuit applications without compromising on the device performance and storage capabilities [123].

The analysis and graphs depict that the operating voltage of circuit elements made using proposed NCTFET is lesser. Thus, the proposed NCTFET inverter and 1T DRAM have a potential to replace conventional TFET in low power circuit applications [124].

CHAPTER 6: CONCLUSION AND FUTURE SCOPE OF THE WORK

6.1 Conclusion

With the advancement and rapid scaling of large-scale integrated circuits, the power consumption of the fabricated chips is increasing gradually. The scaling limitations (intervention of short channel effects) of current MOSFET technology is forcing researchers to look for different alternative options to replace conventional MOSFET. With the miniaturization of chip size in today's VLSI circuits, V_{TH} is scaled proportionately with decreasing transistor size but scaling of supply voltage (V_{DD}) is the biggest challenge associated in this. TFET is a strong candidate in replacement of Conventional MOSFET due to its band to band tunneling mechanism. The improvisations in this field are limited to scaling the size of transistor but also focuses on different device structures and their optimization. In order to relevant to scaled nodes, the conventional TFET is tried for various gate stack positions and thickness of ferroelectric material to provide steeper subthreshold swing, improved I_{ON}/I_{OFF} ratio for the same V_{DD}.

- Current ratio (I_{ON}/I_{OFF}) and subthreshold swing plays a vital role in the making tunnel FET better from the conventional MOSFET. So, in this work, Electrical characteristics of proposed device are plotted and analyzed to obtain a better current ratio and a steeper subthreshold swing.
- The major problem associated with TFET device is its ambipolar behavior. To suppress the leakage current I_{OFF} changes are being made in the device structure keeping in view the improvisations reported in the literature. So, the proposed device (with SiO_2 box and Heterojunction) is capable of attaining an improved I_{ON}/I_{OFF} ratio.
- The operation of NCTFET with varying thickness and Fe materials has been carried out. The analysis has depicted that thickness of gate oxide and ferroelectric material plays an important role in achieving steeper subthreshold slope and higher I_{ON}. In addition, body factor (m-factor) and transport factor (n-factor) associated with the device were improvised in proposed NCTFET and with Fe material engineering, the electrical performance is boosted up in case of proposed NCTFET device.
- An analytical model for heterojunction NCTFET is presented. Solving the capacitance equations and Landau-Khalatnikov Equations for ferroelectric materials, it has been seen

that there is a good matching between Synopsys TCAD simulated model and MATLAB simulated model. Moreover, with the experimental data support, the simulated results have been properly validated for practical applications. The device parameters examined in this work shows the first-order continuity making the proposed device suitable for circuit simulations.

- Shifted Gate Stack Negative Capacitance Tunnel Field Effect Transistor has been proposed in this work. Source Material (Si/Ge) Comparison, AC Analysis, Electrical Noise Analysis have been performed for conventional and proposed NCTFET with different gate materials. Due to the intervention of Fe layer in gate stack, improvised results have been obtained and gate stack shifting has further enhanced the I_{ON}/I_{OFF} ratio and made the SS more stepper.
- The proposed device is then put to circuit level, making a complementary TFET device and 1T DRAM. The device has shown good results and is capable of lowering the overall power consumption of the circuit.

6.1.1 Following contributions are being made:

- The NCTFET device is optimized in this work by doing certain structural modifications and analyzed in the TCAD Sentaurus Device software. In comparison with the already proposed NCTFETs, the optimized NCTFET device structure, in this work, diminishes the band to band tunnelling corner which induces poor on/off transition and in this manner an abrupt switching slope is obtained. By intervention of a ferroelectric material at gate stack of TFET, the I_{ON} current and be improved along with making Subthreshold swing (SS) super steep. Moreover, out of underlapped and overlapped device configurations, the optimized device is a blend of underlapping and overlapping with source-gate overlap length of 5nm. The structure of optimized device is planar and much simpler as compared to other reported works on engineered NCTFETs indicating its compatibility with existing CMOS platform and easier fabrication process.
- To optimize the device further the structural modification is done by raising the source region and suppressing the channel drain junction by SiO_2 box with 50% thickness. Different Ferroelectric materials have been tried and it has found that min average SS of 53.7 mV/dec and I_{ON}/I_{OFF} ratio of $7.14x10^{+9}$ has been achieved in case of $BaTiO_3$.

- Based on domain switching dynamics of Fe material, the subthreshold swing and its corresponding drain current range are physically analyzed. The device formed has shown a decline of 6.3 mV/dec in subthreshold swing as compared to the fundamental limit of 60mV/dec and enhances the I_{ON}/I_{OFF} ratio to 250 times in magnitude. DIBL calculated for conventional NCTFET is 61.2 mV/V and for proposed NCTFET is 31.92 mV/V. So DIBL improvement of 52.2% has been achieved.
- Noise analysis has clearly depicted that the proposed device structure has lesser effect of noise as compared to other devices. Nonetheless, S_{ID} is inversely proportional the frequency, reduced values of noise is observed at high frequency than at low frequency. The use of negative capacitance phenomenon in FETs enables the possibility of having a sub-subthreshold swing lower than 60 mV/decade without comprising on current ratio and to exhibit lower current leakage.

Thus, the proposed optimized device exhibits a steeper sub threshold swing of 53.7 mV/decade and higher I_{ON}/I_{OFF} ratio of $7.14x10^{+9}$ over a large range of current.

6.2 Future Scope of the Work

The n-type NCTFET been designed is capable to achieving a good current ratio and steeper subthreshold swing. Further improvisations can be done in device characteristics with the use of various Fe materials to enhance the negative capacitance effect in the device. The proposed device has been simulated using Kane's band to band tunneling model but in future, we can try quantum simulation models like atomistic simulations, non-energy green function (NEGF) etc. In terms of applications, the proposed device has a great potential to be used in making DRAM and SRAM memory elements. The Fe layer used acts as a rechargeable energy storage region which capable of storing, releasing and retrieving the energy. This helps in achieving a better charge density with lesser external voltage. Work can be done in maximizing the retention time and memory window of such device structures. Digital circuit designing is an area that can be probed by NCTFETs due to their lower SS. Thus, the upcoming trend is to use both NCTFET and CMOS to set a correlation between the device and circuit technology.

References

[1] N. Pandey and Y. Chauhan, "Analytical Modeling of Short-Channel Effects in MFIS Negative Capacitance FET including Quantum Confinement Effects", *IEEE Transactions on Electron Devices*, Vol. 67, Issue No. 11, pp. 4757-4764, Nov 2020.

[2] A. Singh and S. K. Sinha, "Reduction of short channel effects in Metal Oxide Semiconductor Field Effect Transistors: A Literature Review", *Think India Journal*, Vol. 22, Issue No. 37, Dec 2019.

[3] G. Pahwa, T. Dutta, A. Agarwal, S. Khandelwal, S. Salahuddin, C. Hu and Y. S. Chauhan, "Analysis and Compact Modeling of Negative Capacitance Transistor with High On-Current and Negative Output Differential Resistance – Part I: Model Description", *IEEE Transactions on Electron Devices*, Vol. 63, Issue No. 12, pp. 4981-4985, Dec 2016.

[4] S. K. Sinha, K. Kumar and S. Chaudhury, "Si/Ge/GaAs as channel material in Nanowire -FET structures for future semiconductor devices", 11th *IEEE International Conference on Electron Devices and Solid State Circuits,* Nanyang Executive Centre, pp. 527-530, 2015.

[5] (2018) The Moore's Law Or Why Your Computer Is Slow, Available: https://www.sergilehkyi.com/the-moores-law-or-why-my-computer-is-slow/

[6] C.-Y. Chang, K. Endo, K. Kato, C. Yokoyama, M. Takenaka and S. Takagi, "Impact of La_2O_3/InGaAs MOS interface on InGaAs MOSFET performance and its application to InGaAs negative capacitance FET", *IEEE International Electron Devices Meeting (IEDM)*, pp. 1-4, Dec 2016, DOI: 10.1109/IEDM.2016.7838404

[7] S. Huang, S. Lin and P. Su, "Investigation of Inversion Charge Characteristics and Inversion Charge Loss for InGaAs Negative-Capacitance Double-Gate FinFETs Considering Quantum Capacitance", *Journal of Electron Devices Society*, Vol. 8, pp. 105-109, Jan 2020.

[8] (2015) Demonstration of enhanced performance and long-term reliability of tunnel transistors operating under ultra-low voltage, Available: Demonstration of enhanced performance and long-term reliability of tunnel transistors operating under ultra-low voltage (phys.org)

[9] I. A. Pindoo, S. K.Sinha and S. Chander, "Improvement of Electrical Characteristics of SiGe Source Based Tunnel FET Device", *Springer, Silicon*, Vol. 13, Issue No. 9, pp. 3209-3215 Aug 2020.

[10] A. Singh, S. K. Sinha, "Performance analysis of device characteristics in Negative Capacitance Field Effect Transistor", *2nd IEEE International Conference on Electronics and Sustainable Communication Systems at Hindusthan Institute of Technology*, Coimbatore, India, 4-6 August 2021.

[11] J. P. Duarte, S. Khandelwal, A. I. Khan, A. Sachid, Y. Lin, H. Chang, S. Salahuddin and C. Hu, "Compact Models of Negative-Capacitance FinFETs: Lumped and Distributed charge models", *IEEE International Electron Devices Meeting (IEDM)*, Feb 2017.

[12] A. Singh and S. K. Sinha, "Comparative analysis of various ferroelectric materials used in Negative Capacitance Field Effect Transistor (NCFET)", *International Conference on Recent Development on Materials, Reliability, Safety and Environmental Issues (IMRSE),* June 2021.

[13] A.D. Gaidhane, G. Pahwa, A. Verma and Y. S. Chauhan, "Compact Modeling of Drain Current, Charges and Capacitances in Long-Channel Gate-All-Aorund Negative Capacitance MFIS Transistor", *IEEE Transactions on Electron Devices,* Vol. 65, Issue No. 5, pp. 2024-2032, May 2018.

[14] A. C. Seabaugh and Q. Zhang, "Low-voltage tunnel transistors for beyond CMOS logic," *Proceedings IEEE*, Vol. 98, Issue no. 12, pp. 2095–2110, Dec. 2010.

[15] S. Chander, S. Baishya, S.K. Sinha, S. Kumar, P.K. Singh, K. Baral, M.R. Tripathy and S. Jit, "Two-dimentional analytical modeling for electrical characteristics of Ge/Si SOI-tunnel FinFETs", *Elsevier, Superlattices & Microstructures*, Vol. 131, pp. 30-39, 2019.

[16] A. Pahariya and A. K. Dutta, "A new surface potential-based analytical model for MFIS NCFETs", *IEEE Transactions on Electron Devices,* Vol. 69, Issue No. 2, pp. 870-877, Feb 2022.

[17] T. Yuan; et al., "An Analytic Model for Heterojunction Tunnel FETs with Exponential Barrier", *IEEE Transactions on Electron Devices*, Vol. 62, Issue No. 5, pp. 1399-1402, May 2015.

[18] R. Narang, M. Saxena, R.S. Gupta and M. Gupta, "Assessment of ambipolar behaviour of a tunnel FET and influence of structural modifications", *Journal of Semiconductor Technology and Science*, Issue No. 12, pp. 482-491, 2012.

[19] N. Paras, and S. S. Chauhan, "Temperature sensitivity analysis of vertical tunneling based dual metal gate TFET on analog/RF FOMs", *Applied Physics A,* Vol. 125, pp. 316, 2019.

[20] S. Kumar and D. S. Yadav, "Temperature analysis on electrostatics performance parameters of dual metal gate step channel TFET", *Applied Physics A*, Vol. 127, Issue No. 5, pp. 1-11, 2021.

[21] S. K. Sinha and S. Chander, "Investigation of DC Performance of Ge-Source Pocket Silicon-on-Insulator Tunnel Field Effect Transistor in Nano Regime", *Inderscience, International Journal of Nanoparticles*, Volume 13, Issue No. 1, pp. 13-20, May 2021.

[22] A. M. Ionescu and H. Riel, "Tunnel Field-Effect Transistors as Energy Efficient Electronic Switches," *Nature*, Vol. 497, pp. 329- 337, 2011.

[23] L. Liu, D. Mohata, and S. Datta, "Scaling length theory of double-gate interband tunnel field-effect transistors," *IEEE Transactions on Electron Devices*, Vol. 59, Issue no. 4, pp. 902–908, Apr 2012.

[24] A. Giovanni., B. Didier and I. Adrian Mihai, "Demonstration of Subthrehold Swing Smaller Than 60mV/decade in Fe-FET with P(VDF-TrFE)/SiO2 Gate Stack", *IEEE International Electron Devices Meetings*, pp. 1-4, Dec 2008 DOI: 10.1109/IEDM.2008.4796642

[25] S. Salahuddin and S. Datta, "Use of Negative Capacitance to provide Voltage Amplification for Low Power Nanoscale Devices," *Nano Letters*, Vol. 8, Issue No. 2, pp. 405–410, 2008.

[26] J. David, M. Enrique, and G. Andrés, "Analytic Model for the Surface Potential and Drain Current in Negative Capacitance Field-Effect Transistors", *IEEE Transactions on Electron Devices*, Vol. 57, Issue. 10, pp. 2405-2409, Oct 2010.

[27] A. I. Khan, C. W. Yeung, C. Hu, and S. Salahuddin, "Ferroelectric negative capacitance MOSFET: Capacitance tuning & antiferroelectric operation," in *Proceedings IEEE International Electron Devices Meeting*, pp. 11.3.1–11.3.4, 2011.

[28] C.W. Yeung, A. I. Khan, S. Salahuddin and C. Hu, "Device design considerations for ultra-thin body non-hysteretic negative capacitance FETs", *IEEE Third Berkeley Symposium on Energy Efficient Electronic Systems (E3S)*, Oct 2013.

[29] A. Jain, M. A. Alam, "Stability Constraints Define the Minimum Subthreshold Swing of a Negative Capacitance Field-Effect Transistor", *IEEE Transaction on Electron Devices*, pp. 2235-2242, Vol. 61, Issue No. 7, July 2014.

[30] C. Lin, A. I. Khan, S. Salahuddin, C. Hu, "Effects of the Variation of Ferroelectric Properties on Negative Capacitance FET Characteristics", *IEEE Transaction on Electron Devices*, pp. 2197-2199, Vol. 63, Issue No. 5, May 2016.

[31] S. Alghamdi, M. Si, L. Yang, P. D. Ye., "Low Frequency Noise in MoS2 Negative Capacitance Field-effect Transistor", *IEEE International Reliability Physics Symposium (IRPS)*, March 2018.

[32] J. Zhuo, G. Han, N. Xu, J Li, Y. Peng, Y. Liu, j. Zhang, Q. Sun, D. W. hang and Y. Hao, "Experimental Validation of Depolarization Field Produced Voltage Gains in Negative Capacitance Field-Effect Transistors", *IEEE Transactions on Electron Devices*, Vol. 66, Issue No. 10, pp. 4419-4424, Oct 2019.

[33] Y. Liang, Z. Zhu, X. Li, S. K. Gupta, S. Datta and V. Narayanan, "Utilization of Negative-Capacitance FETs to Boost Analog Circuit Performances", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 27, Issue No. 12, pp. 1-6, Sep 2019.

[34] Hung-Han Lin, Vita Pi-Ho Hu, "Device Designs and Analog Performance Analysis for Negative-Capacitance Vertical- Tunnel FET", *IEEE International Symposium on Quality Electronic Design (ISQED)*, pp. 241-245, Mar 2019. DOI:10.1109/ISQED.2019.8697625

[35] R. Mann, R. Chaujar, "A Comparative Investigation on Characteristics of Conventional MOSFET and Ferroelectric Thin Film Modified FET", *Devices for Integrated Circuit*, pp. 53-56, May 2021. DOI: 10.1109/DevIC50843.2021.9455861

[36] S. Chaudhary, C. Sahu and Menka, "Simulation study based performance projection of Negative capacitance FET", *IEEE India Council International Conference (INDICON),* Dec 2020. 10.1109/INDICON49873.2020.9342497

[37] S. Somu, Y. Srivastava, "Equivalent circuit and simulations for the Landau-Khalatnikov model of ferroelectric hysteresis", *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency control*, Vol. 50, Issue No. 8, pp. 950-957, Aug 2003.

[38] Y. Lin, F. McGuire, S. Noyce, N. Williams, Z. Chaeng, J. Andrews and A. D. Franklin, "Effects of Gate Stack Composition and Thickness in 2-D Negative Capacitance FETs", *Journal of Electron Device Society,* Vol. 7, pp. 645-649, June 2019.

[39] B. Lu, Y. Cui, A. Guo, D. Wang, Z. Lv, "Characteristics of InAs/GaSb Line-Tunneling FETs With Buried Drain Technique", *IEEE Transactions on Electron Devices*, Vol. 68, Issue No. 4, pp 1537-1541, Apr 2021.

[40] T. Yu, L. Peng, C. Lin and Y. Hsin, "GaAsSb/InGaAs tunnel field effect transistor with a pocket layer", *Microelectronics Reliability*, Vol. 83, pp. 235-237, March 2018.

[41] H. W. Kim and D. Kwon, "Gate-Normal Negative Capacitance Tunnel Field-Effect Transistor (TFET) With Channel Doping Engineering", *IEEE Transactions on Nanotechnology*, Vol. 20, pp. 278-281, 2021.

[42] S. Shreya, N. Kumar, S. Anand and I. Amin, "Performance Analysis of a Charge Plasma Junctionless Nanotube Tunnel FET Including the Negative Capacitance Effect", *Journal of Electronic Materials*, Jan, 2020. DOI: /10.1007/s11664-020-07969-3

[43] S. Guha, P. Pachal, "Heterojunction Negative-Capacitance Tunnel-FET as a Promising Candidate for Sub-0.4V V_{DD} Digital Logic Circuits", *IEEE Transcations on Nanotechnology*, Vol. 20, pp. 576-583, July 2021.

[44] N. K. Kranthi, and M. Shrivastava, "ESD Behavior of Tunnel FET Devices," *IEEE Transactions on Electron Devices*, Vol. 64, Issue No. 1, pp. 28-36, Jan, 2017.

[45] L. Ding, E. Gnani, S. Gerardim, M. Bagatin, F. Driussi, P. Palestri, L. Selmi, C. L. Royer, and A. Paccagnella, "Investigation of Hot Carrier Stress and Constant Voltage Stress in High-ϰ Si-Based TFETs," *IEEE Transactions on Device and Materials Reliablity*, Vol. 15, Issue No.2, pp. 236-241, June 2015.

[46] L. Ding, E. Gnani, S. Gerardin, M. Bagatin, F. Driussi, P. Palestri, L. Selmi, C. L. Royer, and A. Paccagnella, "Total Ionizing Dose Effects in Si-Based Tunnel FETs," *IEEE Transactions on Nuclear Science*, Vol. 61, Issue No. 6, pp. 2874-2880.

[47] V. Pi-Ho Hu, H. Lin, Y. Lin and C. Hu "Optimization of Negative Capacitance Vertical-Tunnel FET (NCVT-FET)", *IEEE Transactions on Electron Devices*, Vol. 67, Issue No. 6, pp. 2593-2599, 2020.

[48] H. W. Kim and D. Kwon, "Gate-Normal Negative Capacitance Tunnel Field-Effect Transistor (TFET) With Channel Doping Engineering", *IEEE Transactions on Nanotechnology*, Vol. 20, pp. 278-281, 2021.

[49] D. Kwon, S. Cheema, N. Shanker, K. Chatterjee, Y. Liao, A.V. Tan, C. Hu and S. Salahuddin, "Negative Capacitance FET with 1.8-nm-Thick Zr-Depoed HfO_2 oxide", *IEEE Electron Device Letters*, Vol. 40, Issue No. 6, pp. 993-996, 2019.

[50] C. Su, Q. Huang, M. Yang, L. Chen, Z. Liang and R. Huang, "Origin of Steep Subthreshold Swing Within the Low Drain Current Range in Negative Capacitance Field Effect Transistor", *China Semiconductor Technology International Conference (CSTIC)*, Dec 2020. DOI: 10.1109/CSTIC49141.2020.9282519

[51] S. T. Bu, D. M. Huang, G. F. Jiao, H. Y. Yu and M. F. Li, "Low frequency noise in tunneling field effect transistors", *Solid-State Electronics,* Vol. 137, pp. 95-101, 2017.

[52] A. Pahariya and A. K. Dutta, "A new surface potential-based analytical model for MFIS NCTFETs", *IEEE Transactions on Electron Devices*, Vol. 69, Issue No. 2, pp. 870-877, Feb 2022.

[53] V. P. Hu, H. Lin, Y. Lin and C. Hu, "Optimization of Negative-Capacitance Vertical-Tunnel FET (NCVT-FET)", *IEEE Transactions on Electron Devices*, Vol. 67, Issue No. 6, June 2020.

[54] F. Najam and Y. S. Yu, "Impact of Quantum Confinement on Band-to-Band Tunneling of Line-Tunneling Type L-Shaped Tunnl Field-Effect Transistor", *IEEE Transactions on Electron Devices,* Vol. 66, Issue No. 4, pp. 2010-2016, Apr 2019.

[55] A. Pal and A. K. Dutta, "Analytical Drain Current Modeling of Double-Gate Tunnel Field Effect Transistor", *IEEE Transactions on Electron Devices,* Vol. 63, Issue No. 8, pp. 3213-3221, Aug 2016.

[56] C. Jiang, R. Liang and J. Xu, "Investigation of Negative Capacitance Gate-all-around Tunnel FETs Combining Numerical Simulation and Analytical Modeling", *IEEE Transactions on Nanotechnology*, Vol. 16, Issue No. 1, pp. 58-67, Jan 2017.

[57] M. Kao, G. Pahwa, A. Dasgupta, S. Salahuddin and C. Hu, "Analysis and Modelling of Polarization Gradient Effect on Negative Capacitance FET", *IEEE Transactions on Electron Devices*, Vol. 67, Issue No. 10, pp. 4521-4525, Oct 2020.

[58] X. Huang, L. Li, Y. Jiao, X. Lin, Q. Huang, L. Zhang and R. Huang, "A dynamic current model for MFIS Negative Capacitance Transistors", *IEEE Transactions on Electron Devices*, Vol. 68, Issue No. 7, pp. 3665-3671, July 2021.

[59] S. Poorvasha and B. Lakshmi, "Investigation and statistical modeling of InAs-based double gate tunnel FETs for RF performance enhancement", *Journal of Semiconductors*, Vol. 39. Issue No. 5, May 2018.

[60] H. Lee, J. D. Park, and C. Shin, "Study of random variation in germanium-source vertical tunnel FET," *IEEE Transactions on Electron Devices*, Vol. 63, Issue No. 5, pp. 1827-1834, May. 2016.

[61] H. Mulaosmanovic, E. T. Breyer, T. Mikolajick and S. Slesazick, "Ferroelectric FETs with 20-nm-Thick HfO2 Layer for Large Memory Window and High Performance", *IEEE Transactions on Electron Devices*, Vol. 66, Issue No. 9, Sep 2019.

[62] F. Meng, H. Lu, Y. Zhang, Y. Zhang, B. Lu, Z. Lv and Y. Zhao, "The Application of Gate-Drain underlap Architecture in TFET-based Inverters", *IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT),* Dec 2018. DOI: 10.1109/ICSICT.2018.8564852

[63] N. Kamal, A. K. Kamal and J. Singh, "L-Shaped Tunnel Field-Effect Transistor-Based 1T DRAM With Improved Read Current Ratio, Retention Time, and Sense Margin", *IEEE Transactions on Electron Devices,* Vol. 68. Issue No. 6, June 2021.

[64] V. Chauhan and D. P. Samajdar, "Recent Advances in Negative Capacitance FinFETs for Low Power Applications: A Review", *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, Vol. 68, Issue No. 10, pp. 3056-3068, Oct 2021.

[65] P. Bal , M.W. Akram, P. Mondal and B. Ghosh, "Performance estimation of sub-30 nm junctionless tunnel FET (JLTFET)", *Journal of Computational Electronics*, Vol. 12, pp. 782-789, June 2013.

[66] S. W. Kim, J. H. Kim ,T. K. Liu, W. Y. Choi and B-G "Demonstration of L shaped Tunnel Field Effect Transisitor" *IEEE Transactions on Electron Devices*, Vol. 63, Issue No. 4, April 2016.

[67] W. Wang, P.F. Wang, C.M. Zhang, X. Lin, X.Y. Liu, Q.Q. Sun, P. Zhou, and D. W. Zhang, "Design of U-shape channel tunnel FETs with SiGe source regions", *IEEE Transactions on Electron Devices*, Vol. 61, Issue No. 1, pp. 193-197, Jan 2014.

[68] D. J. Frank, Y. Taur, and H.-S. P. Wong, "Generalized scale length for two-dimensional effects in MOSFETs," *IEEE Electron Device Letters*, Vol. 19, Issue No. 10, pp. 385–387, Oct 1998.

[69] I. A. Pindoo, S. K.Sinha and S. Chander, "Performance Analysis of Heterojunction Tunnel FET Device with Variable Temperature", *Springer, Applied Physics A,* Vol. 127, Issue No. 10, pp. 1-10, 2021.

[70] S. Chander, S. K.Sinha, R. Chaudhury and A. Singh , "Ge-Source Based L-shaped Tunnel Field Effect Transistor for Low Power Switching Application", *Springer, Silicon*, October 29, 2021, DOI: 10.1007/s12633-021-01475-9.

[71] M. A. Wahab, M. A. Alam, "MATLAB: Negative Capacitance (NC) FET Model," *Nano Hub*, Dec 2015.

[72] A. Saeidi, F. Jazaeri, F. Bellando, I. Stolichnov, G. V. Luong, Q. Zhao, S. Mantl, C. C. Enz and A. M. Ionescu, "Negative Capacitance as Performance Booster for Tunnel FETs and MOSFETs: an experimental study", *Journal of Electron Device Letters*, Vol. 38, Issue No. 10, pp. 1485-1488, Oct 2017.

[73] Sentaurus Device User Guide, Synopsys Inc.,Version D-2021.0.

[74] A. Pal, A. B. Sachid, H. Gossner and V. R. Rao, "Insights into the Design and Optimization of Tunnel-FET Devices and circuits," *IEEE Transactions on Electron Devices*, Vol. 58, Issue No. 4, pp. 1045-1053 Apr 2011.

[75] W. M. Reddick and G. A. J. Amaratunga, "Silicon surface tunnel transistor", *Applied Physics Letters*, Vol. 67, Issue No. 4, pp. 494-497, 1995.

[76] J. Koga and A. Toriumi, "Negative differential conductance in three-terminal silicon tunneling device", *Applied Physics Letters*, Vol. 69, Issue No. 10, pp. 1435-1437, 1996.

[77] A. Singh, S. K. Sinha & S. Chander, "Effect of Negative Capacitance on Heterojunction Tunnel Field Effect Transistor", *IEEE International Conference on Electronics, Communication and Aerospace Technology (ICECA 2021)* , Coimbatore, India, pp. 347-350, 2-4 December 2021.

[78] B. Bhushan, K. Nayak and V. Ramgopal Rao, "DC Compact Model for SOI tunnel field effect", *IEEE Transactions on Electron Devices*, Vol. 59, Issue No. 10, Oct 2012.

[79] C.W. Yeung; et al., "Low Power Negative Capacitance FETs for Future Quantum-Well Body Technology", *International Symposium on VLSI Technology, Systems and Application (VLSI-TSA)*, Apr. 2013.

[80] S. Chander, S. K. Sinha, S. Kumar, P. Singh, K.Baral, K.Singh and S. Jit, "Temperature Analysis of Ge/si Hetrojunction SOI-Tunnel FET", *Elsevier, Superlattices & Microstructures,* Vol. 110, pp. 162-170, 2017.

[81] M. Halid, T. B. Evelyn, M. Thomas, S. Stefan, "Ferroelectric FETs with 20-nm Thick HfO_2 Layer for Large Memory Window and High Performance", *IEEE Transactions on Electron Devices*, Vol. 66, Issue. 7, pp. 3828-3833, Sep. 2019.

[82] L. Livio, L. D. Michielis and A. M. Ionescu, "Complementary Germanium Electron–Hole Bilayer Tunnel FET for Sub-0.5-V Operation", *IEEE Electron Device Letters*, Vol. 33, Issue No. 2, pp. 167-169, Feb. 2012.

[83] L. Shen-Yang; et al., "Experimental Demonstration of Stacked Gate-All-Around Poly Si Nanowires Negative Capacitance FETs with Internal Gate Featuring Seed Layer and Free of Post- Metal Annealing Process", *IEEE Electron Device Letters*, Vol. 40, Issue No. 11, pp. 1708-1711, Sep. 2019.

[84] S. Chander, S. K. Sinha and R Chaudhary, "Comprehensive review on electrical noise analysis of TFET structures", *Elsevier, Superlattices & Microstructures,* December 2021, DOI: 10.1016/j.spmi.2021.107101.

[85] H. Amrouch, M. Rapp and S. Salamin, "Impact of Negative Capacitance Field-Effect Transistor (NCFET) on Many-Core Systems", *A Journey of Embedded and Cyber-Physical Systems, Springer*, pp. 107-123, July 2020.

[86] Q. Xie, J. Xu, and Y. Taur, "Review and critique of analytic models of MOSFET short-channel effects in subthreshold", *IEEE Transactions on Electron Devices*, Vol. 59, Issue No. 6, pp. 1569 - 1579, Jun 2012.

[87] S.-H. Oh, D. Monroe, and J. M. Hergenrother, "Analytic description of short-channel effects in fully-depleted double-gate and cylindrical, surrounding-gate MOSFETs", *IEEE Electron Device Letters*, Vol. 21, Issue No. 9, pp. 445–447, Sep 2000.

[88] A. Biswas and A. M. Ionescu, "1T capacitor-less DRAM cell based on asymmetric tunnel FET design", *IEEE Journal of Electron Devices Society,* Vol. 3, Issue No. 3, pp. 217–222, May 2015.

[89] N. Rodriguez, S. Cristoloveanu, and F. Gamiz, "Novel capacitorless 1T-DRAM cell for 22-nm node compatible with bulk and SOI sub- strates," *IEEE Transactions on Electron Devices*, Vol. 58, Issue No. 8, pp. 2371–2377, Aug 2011.

[90] S. K. Sinha, P. Singh and S. Chaudhury, "Effect of temperature and chiral vector on emerging CNTFET device", *IEEE International Conference on Computing for Sustainable Global Development (INDIACom),* pp. 432-435, 2014. DOI: 10.1016/j.mssp.2014.12.013

[91] S. Gupta, M. Steiner, A. Aziz, V. Narayanan, S. Datta, and S.K. Gupta,"Device-circuit analysis of ferroelectric FETs for low-power logic," *IEEE Transactions on Electron Devices,* Vol. 64. Issue No. 8, pp. 3452-3458, 2017.

[92] S. Y. Wu, "Theory of generation-recombination noise in MOS transistors", *Solid State Electron*, Vol. 11, pp. 25-32, 1968.

[93] K. K. Bhuwalka, J. Schulze and I. Eisele, "Scaling the vertical tunnel FET with tunnel bandgap modulation and gate work function engineering", *IEEE Transactions on Electron Devices,* Vol. 52, pp. 909-917, 2005.

[94] W. Hansch, P. Borthen, J. Schulze, C. Fink, T. Sulima and I. Eisele, "Performance improvement in vertical surface tunneling transistors by a boron surface phase", *Japanese Journal of Applied Physics*, Vol. 40, Issue No. 5A, pp. 3131-3136, 2001.

[95] S. K. Sinha and S. Chaudhury, "Impact of Temperature Variation on CNTFET Device Characteristics", *IEEE International Conference on Control, Automation, Robotics & Embedded Systems,* pp. 1-5, 2013. DOI: 10.1109/CARE.2013.6733774

[96] S. Danial, S. Majid, J. Farzan, "Ultrathin Junction-less Nanowire FET Model, Including 2-D Quantum Confinements", *IEEE Transactions on Electron Devices*, Vol. 66, Issue No. 9, pp. 4101-4106, Sep. 2019.

[97] W. Cao, C. J. Yao, G. F. Jiao, D. Huang, H. Y. Yu, and M. Li, "Improvement in Reliability of Tunneling Field- Effect Transistor With p-n-i-n Structure", *IEEE Transactions on Electron Devices*,Vol. 58 Issue No. 7, July 2011.

[98] W. Y. Choi, B. G. Park, J. D. Lee and T. K. Liu., "Tunneling field effect transistors (TFETs) with subthreshold swing (SS) less than 60 mV/dec", *IEEE Electron Device Letters,* Vol. 28, pp. 743– 745, 2007.

[99] S. K. Sinha and S Chaudhury, "Oxide thickness effect on Quantum Capacitance in single gate MOSFET and CNTFET devices", *Annual IEEE India Conference*, pp. 042-046, 2012. DOI: 10.1109/INDCON.2012.6420586

[100] J. Zhou, G. Han, N. Xu, J. Li, Y. Peng, Y. Liu, J. Zhang, Q. Sun, D. W. Zhang and Y. Hao, "Experimental Validation of Depolarization Field Produced Voltage Gains in Negative Capacitance Field-Effect Transistors", *IEEE Transactions on Electron Devices*, Vol. 66, Issue. 10, pp. 4419-4424, Oct. 2019.

[101] S. Chen, S. Wang, H. Liu, W. Li, Q. Wang and X. Wang, "Symmetric U-shaped gate tunnel field-effect transistor," *IEEE Transaction on Electron Devices*, Vol. 64, Issue No. 3, pp. 1343-1349, Mar 2017.

[102] F. I. Sakib, Md. A. Hasan and M. Hossain, "Negative Capacitance Gate-All-Around Tunnel FETs for Highly Sensitive Label-Free biosensors", *IEEE Transactions on Electron Devices*, Vol. 69, Issue No. 1, pp. 311-317, Jan 2022.

[103] J. Wan, C. L. Royer, A. Zaslavsky and S. Cristoloveanu, "Low-Frequency noise behavior of tunneling field effect transistors", *Applied Physics Letters*, Vol. 97, Issue No. 24, pp. 243-253, 2010.

[104] S. Chander, R. Chaudhary and S. K. Sinha, "Impact of Low Frequency Noise Source over Tunnel Field Effect Transistor in Nano Regime", *IEEE International Conference on Recent Trends on Electronics, Information , Communication & Technology*, pp. 770-773, 2021. DOI: 10.1109/RTEICT52294.2021.9573734

[105] M. J. Kirton and M. J. Uren, "Noise in solid-state microstructures: A new perspective on individual defects, interface states and low-frequency (1/*f*) noise", *Advances in Physics*, Vol. 38, Issue No. 4, pp. 367-468, Nov 1989.

[106] R. Bijesh, D. K. Mohata, H. Liu and S. Datta, "Flicker noise characterization and analytical modeling of homo and hetero-junction III–V tunnel FET", *Proc. 70th Annu. DRC*, pp. 203-204, Jun 2012. DOI: 10.1109/DRC.2012.6257032

[107] R. Pandey, "Electrical noise in heterojunction interband tunnel FETs", *IEEE Transactions on Electron Devices*, Vol. 61, Feb 2014.

[108] B. Das and B. Bhowmick, "Noise Behavior of Ferroelectric Tunnel FET", *Microelectronics Journal*, Vol. 96, 2020.

[109] Q. Yang, L. Wang, Z. Qi and Z. Ma, "Analysis of Gate-Source Voltage Spike Generated by Miller Capacitance and Common Source Inductance", *2021 IEEE 12thEnergy Conversion Congress & Exposition - Asia (ECCE-Asia)*, July 2021. DOI: 10.1109/ECCE-Asia49820.2021.9479360

[110] C. Wu, R. Huang, Q. Huang, J. Wang, and Y. Wang, "Design guideline for complementary heterostructure tunnel FETs with steep slope and improved output behavior", *IEEE Electron Device Letters,* Vol. 37, Issue No. 1, pp. 20–23, Jan 2016.

[111] P. G. D. Agopian, D. V. M. Martino, S. D. Santos, F. S. Neves, J. A. Martino, R. Rooyackers, A. Vandooren, E. Simoen, A. V. Theon and C. Claeys, "Influence of the source composition on the analog performance parameters of vertical nanowire-TFETs", *IEEE Transactions on Electron Devices*, Vol. 62, Issue No. 1, pp. 16-22, Jan 2015.

[112] E. Gnani, M. Visciarelli, A. Gnudi, S. Reggiani and G. Baccarani, "TFET Inverter Static and Transient Performances in Presence of Traps and Localized Strain", *Solid State Electronics*, Vol. 159, pp. 38-42, Sep 2019.

[113] V. D. Wangkherirakpan, B. Bhowmick and P. D. Pukhrambam, "Investigation of N+ pocket-doped junctionless vertical TFET and its digital inverter application in the presence of true noises", *Applied Physics A*, Vol. 126, Issue No. 798, 2020.

[114] J. Madan, R. Chaujar, "Numerical simulation of N+ source pocket PI-GAA-tunnel FET: impact of interface trap charges and temperature", *IEEE Transactions on Electron Devices,* Vol. 64, Issue No. 4, pp. 1482–1488, 2017.

[115] R. Goswami, B. Bhowmick, S. Baishya, "Effect of scaling on noise in circular gate TFET and its application as a digital inverter", *Microelectron Journal*, Vol. 53, pp. 16–24, 2016.

[116] L. Knoll, Q. Zhao, A. Nichau, S. Trellenkamp, S. Richter, A. Schafer, D. Esseni, L. Selmi, K. K. Bourdelle and S. Mantl, "Inverters With Strained Si Nanowire

Complementary Tunnel Field-Effect Transistors", *IEEE Electron Device Letters*, Vol. 34, Issue No. 6, June 2013.

[117] T. Tanaka, E. Yoshida, and T. Miyashita, "Scalability study on a capaci- torless 1T-DRAM: From single-gate PD-SOI to double-gate FinDRAM", *IEEE International Electron Devices Meeting (IEDM)*, pp. 919–922, Dec. 2004. DOI: 10.1109/IEDM.2004.1419332

[118] C. Hu, T.-J. King, and C. Hu, "A capacitorless double-gate DRAM cell," *IEEE Electron Device Letters,* Vol. 23, Issue No. 6, pp. 345–347, June 2002.

[119] Guoliang Tian, Gaobo Xu, Huaxiang Yin, Lianlian Li, Gangping Yan, Yanna Luo and Xiaoting Sun, "Negative Capacitance Double-Gate Vertical Tunnel FET with Improved Subthreshold Characteristics," *2022 China Semiconductor Technology International Conference (CSTIC)*, 2022, pp. 1-3, doi: 10.1109/CSTIC55103.2022.9856792.

[120] A. Biswas and A. M. Ionescu, "1T capacitor-less DRAM cell based on asymmetric tunnel FET design," *IEEE Journal of Electron Devices Society*, Vol. 3, Issue No. 3, pp. 217–222, May 2015.

[121] D.-O. Kim, D.-I. Moon, and Y.-K. Choi, "Optimization of bias schemes for long-term endurable 1T-DRAM through the use of the biristor mode operation," *IEEE Electron Device Letters,* Vol. 35, Issue no. 2, pp. 220–222, Feb. 2014.

[122] N. Navlakha, J. Lin and A. Kranti, "Improved Retention Time in Twin Gate 1T DRAM with Tunneling Based Read Mechanism", *IEEE Electron Device Letters*, Vol. 37, Issue No. 9, Sep 2016.

[123] R. Goel, A. Sharma and Y. S. Chahuan, "Analysis and Modeling of Current Mismatch in Negative Capacitance Field-Effect Transistor," *IEEE Transactions on Electron Devices*, Vol. 69, Issue No. 9, pp. 5337-5344, Sept. 2022, DOI: 10.1109/TED.2022.3192216.

[124] Yang Zhao, Zhongxin Liang, Qianqian Huangm , Cheng Chen, Mengxuan Yang, Zixuan Sun, Kunkun Zhu, Huimin Wang, Shuhan Liu, Tianyi Liu, Yue Peng, Genquan Han and Ru Huang, "A Novel Anti-Ferroelectric Negative Capacitance Tunneling FET with Mitigated Subthreshold Swing Degradation Issue," *2022 China Semiconductor Technology International Conference (CSTIC)*, 2022, pp. 1-3, DOI: 10.1109/CSTIC55103.2022.9856738.

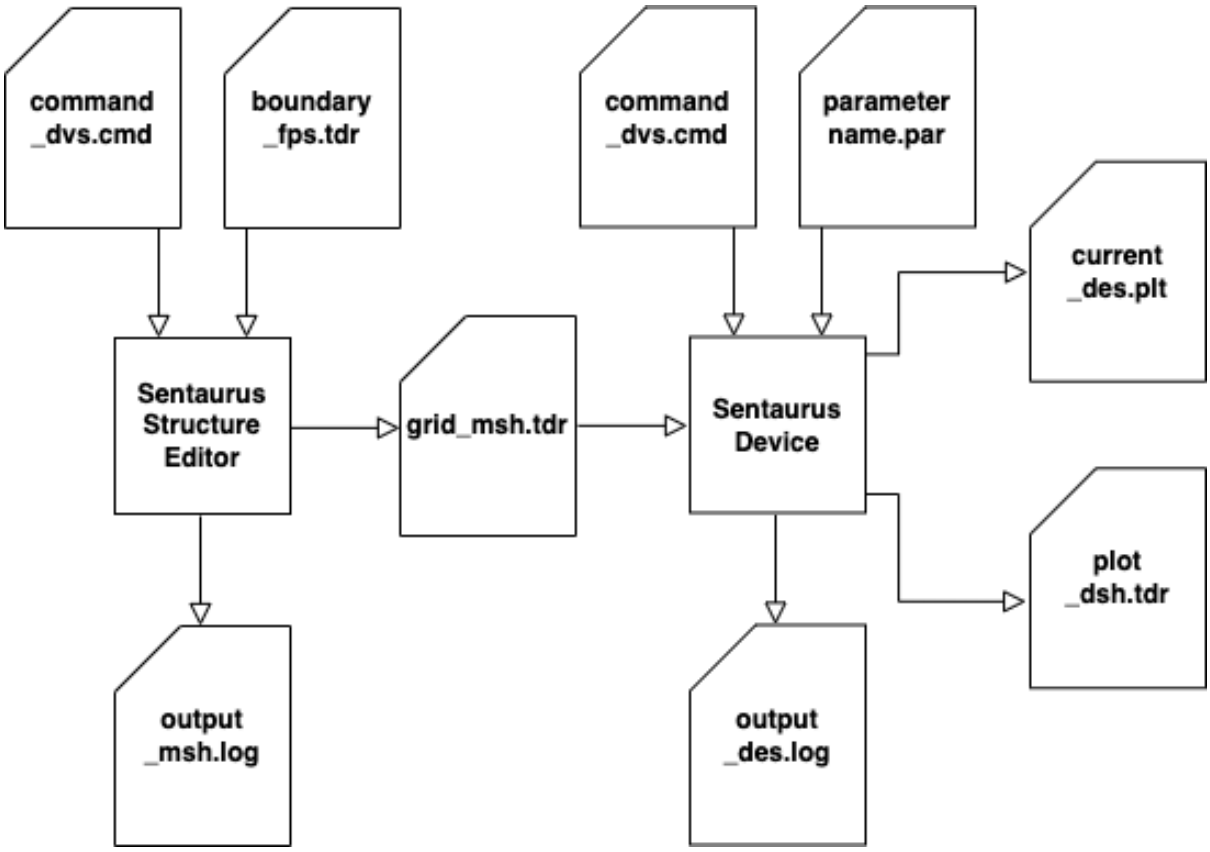
APPENDIX

A1: Synopsys TCAD Simulation Basics

Sentaurus Structure Editor (sde) is a 2D and 3D device structure editor. The distinct operational modes share a common data representation. Geometric operations can be mixed freely, adding more flexibility to the generation of 3D structures.

In addition, Sentaurus Structure Editor offers state-of-the-art visualization. Structures are displayed as they are created and powerful view filters make it possible to select a subset of regions and to make regions transparent.

Sentaurus Device (sdevice) is an advanced multidimensional device simulator capable of simulating electrical, thermal, and optical characteristics of silicon-based and compound semiconductor devices. Sentaurus Device is a new-generation device simulator for designing and optimizing current and future semiconductor devices.



A2: Few data points of the proposed device:

TABLE A2.1: log I_D v/s V_{GS} transfer characteristics of the TFET devices

Gate Voltage (Volts)	Drain Current (A/μm)				
	Conv. TFET	Conv. NCTFET	Overlapped NCTFET	Raised Source NCTFET	Proposed NCTFET
0	1.67E-10	1.28E-10	3.72E-13	3.42E-13	1.48E-14
0.1	1.99E-10	1.51E-10	4.09E-13	1.71E-13	6.01E-15
0.2	2.35E-10	1.78E-10	8.52E-11	1.19E-13	3.23E-13
0.3	2.85E-10	2.00E-10	7.12E-09	1.98E-12	2.72E-11
0.4	4.48E-10	2.27E-10	7.27E-07	1.76E-10	6.69E-10
0.5	1.32E-09	2.63E-10	3.49E-06	2.13E-09	6.66E-09
0.6	4.74E-09	3.35E-10	8.14E-06	1.67E-08	3.74E-08
0.7	1.35E-08	5.61E-10	1.25E-05	9.23E-08	1.38E-07
0.8	3.44E-08	1.17E-09	1.71E-05	2.41E-07	3.90E-07
0.9	7.04E-08	2.48E-09	2.13E-05	3.95E-07	9.07E-07
1	1.17E-07	4.87E-09	2.47E-05	6.54E-07	1.83E-06
1.1	1.72E-07	8.83E-09	2.74E-05	1.02E-06	3.29E-06
1.2	2.35E-07	1.42E-08	2.95E-05	1.49E-06	5.38E-06
1.3	3.07E-07	2.26E-08	3.16E-05	1.98E-06	8.17E-06
1.4	3.87E-07	3.49E-08	3.37E-05	2.46E-06	1.15E-05
1.5	4.76E-07	5.10E-08	3.57E-05	2.87E-06	1.56E-05
1.6	5.71E-07	7.02E-08	3.78E-05	3.25E-06	2.06E-05
1.7	6.70E-07	9.17E-08	3.97E-05	3.61E-06	2.59E-05
1.8	7.73E-07	1.15E-07	4.15E-05	3.94E-06	3.16E-05
1.9	8.78E-07	1.40E-07	4.32E-05	4.28E-06	3.74E-05
2	9.87E-07	1.66E-07	4.52E-05	4.58E-06	4.27E-05

TABLE A2.2: log I_D v/s V_{GS} transfer characteristics for Si/Ge Source at different VDS values

Gate Voltage (Volts)	**Drain Current (A/μm)**					
	Si Source			**Ge Source**		
	V_{DS} = 0.5V	**V_{DS} = 0.7V**	**V_{DS} = 0.9V**	**V_{DS} = 0.5V**	**V_{DS} = 0.7V**	**V_{DS} = 0.9V**
0	1.63E-13	1.22E-10	5.73E-14	3.72E-13	5.73E-14	3.72E-13
0	1.63E-13	1.22E-10	5.73E-14	3.72E-13	5.73E-14	3.72E-13
0.2	4.54E-15	1.64E-10	1.76E-15	4.09E-13	1.76E-15	4.09E-13
0.4	1.30E-16	2.12E-10	6.89E-17	8.52E-11	6.89E-17	8.52E-11
0.6	4.94E-17	5.07E-10	8.80E-16	7.12E-09	8.80E-16	7.12E-09
0.8	5.06E-15	3.30E-09	1.51E-14	7.27E-07	1.51E-14	7.27E-07
1	3.19E-13	1.49E-08	6.42E-13	3.49E-06	6.42E-13	3.49E-06
1.2	4.85E-12	4.23E-08	1.51E-11	8.14E-06	1.51E-11	8.14E-06
1.4	2.64E-11	8.90E-08	6.20E-11	1.25E-05	6.20E-11	1.25E-05
1.6	8.60E-11	1.53E-07	1.55E-10	1.71E-05	1.55E-10	1.71E-05
1.8	2.12E-10	2.33E-07	3.00E-10	2.13E-05	3.00E-10	2.13E-05
2	4.62E-10	3.16E-07	5.09E-10	2.47E-05	5.09E-10	2.47E-05
2.2	9.45E-10	3.99E-07	7.54E-10	2.74E-05	7.54E-10	2.74E-05
2.4	1.56E-09	4.83E-07	9.90E-10	2.95E-05	9.90E-10	2.95E-05
2.6	2.18E-09	5.72E-07	1.20E-09	3.16E-05	1.20E-09	3.16E-05
2.8	2.69E-09	6.67E-07	1.41E-09	3.37E-05	1.41E-09	3.37E-05
3	3.15E-09	7.67E-07	1.61E-09	3.57E-05	1.61E-09	3.57E-05

TABLE A2.3: Variation of Performance with different Fe Materials

Gate Voltage (Volts)	**Drain Current (A/μm)**		
	PZT	**$BaTiO_3$**	**P(VDF-TrFE)**
0	5.53E-15	6.01E-15	1.16E-14
0.1	5.53E-15	6.01E-15	5.85E-15
0.2	1.11E-13	3.23E-13	1.57E-13
0.3	3.86E-12	2.72E-11	5.51E-12
0.4	6.50E-11	6.69E-10	8.58E-11
0.5	8.37E-10	6.66E-09	8.65E-10
0.6	8.02E-09	3.74E-08	7.46E-09
0.7	5.54E-08	1.38E-07	5.03E-08
0.8	2.12E-07	3.90E-07	1.95E-07
0.9	5.40E-07	9.07E-07	5.23E-07
1	1.10E-06	1.83E-06	1.09E-06
1.1	1.96E-06	3.29E-06	1.96E-06
1.2	3.18E-06	5.38E-06	3.19E-06
1.3	4.80E-06	8.17E-06	4.85E-06
1.4	6.92E-06	1.15E-05	7.01E-06
1.5	9.56E-06	1.56E-05	9.72E-06
1.6	1.27E-05	2.06E-05	1.29E-05
1.7	1.63E-05	2.59E-05	1.66E-05
1.8	2.05E-05	3.16E-05	2.09E-05
1.9	2.54E-05	3.74E-05	2.59E-05
2	3.09E-05	4.27E-05	3.17E-05

TABLE A2.4: Variation of Performance with different thicknesses of Fe Material

Gate Voltage (Volts)	**Drain Current (A/μm)**				
	T_{FE} = 1nm	**T_{FE} = 2nm**	**T_{FE} = 3nm**	**T_{FE} = 4nm**	**T_{FE} = 5nm**
0	8.19E-15	1.20E-14	4.87E-15	3.40E-15	2.17E-15
0.1	8.83E-15	1.20E-14	9.65E-15	3.40E-15	2.17E-15
0.2	1.39E-11	4.02E-13	8.00E-13	1.77E-14	5.73E-15
0.3	2.64E-10	6.06E-12	4.70E-11	8.47E-13	1.25E-13
0.4	1.44E-09	7.43E-11	8.68E-10	1.94E-11	2.09E-12
0.5	1.17E-07	3.33E-09	7.78E-09	1.79E-10	2.67E-11
0.6	7.35E-07	1.60E-08	4.12E-08	9.99E-10	2.77E-10
0.7	2.36E-06	1.45E-07	1.47E-07	4.06E-09	1.24E-09
0.8	5.33E-06	8.83E-07	4.05E-07	1.31E-08	3.66E-09
0.9	9.70E-06	2.66E-06	9.29E-07	3.57E-08	9.48E-09
1	1.56E-05	5.38E-06	1.86E-06	9.35E-08	2.25E-08
1.1	2.17E-05	9.15E-06	3.33E-06	2.00E-07	4.92E-08
1.2	2.76E-05	1.29E-05	5.43E-06	5.43E-07	1.01E-07
1.3	3.29E-05	1.66E-05	8.22E-06	1.42E-06	2.13E-07
1.4	3.63E-05	2.11E-05	1.16E-05	2.25E-06	5.16E-07
1.5	3.79E-05	2.61E-05	1.57E-05	3.03E-06	1.09E-06
1.6	3.88E-05	3.21E-05	2.07E-05	4.08E-06	2.07E-06
1.7	3.95E-05	3.78E-05	2.61E-05	5.50E-06	3.34E-06
1.8	4.07E-05	4.38E-05	3.20E-05	7.56E-06	4.78E-06
1.9	4.22E-05	4.72E-05	3.76E-05	9.97E-06	6.39E-06
2	4.46E-05	4.92E-05	4.31E-05	1.28E-05	7.67E-06

TABLE A2.5: Variation of SID with Frequency (ranging from 1MHz-1GHz)

Frequency (Hz)	**S_{ID} (A^2/Hz)**			
	Conv. NCTFET	**Overlapped NCTFET**	**Raised Source NCTFET**	**Proposed NCTFET**
10	2.98E-17	3.56E-21	2.70E-20	4.79E-23
10^2	2.97E-17	3.54E-21	2.69E-20	4.77E-23
10^3	2.33E-17	2.78E-21	2.11E-20	3.75E-23
10^4	1.58E-17	1.88E-21	1.43E-20	2.53E-23
10^5	1.46E-17	1.74E-21	1.32E-20	2.36E-23
10^6	1.04E-17	1.25E-21	9.50E-21	2.53E-23
10^7	3.60E-19	4.30E-23	4.29E-22	2.98E-23
10^8	3.69E-21	4.40E-25	1.09E-22	2.99E-23
10^9	3.69E-23	4.44E-27	1.06E-22	2.99E-23

V_{ds} is kept at 0.5 V and V_{gs} is kept at 1.0 V

LIST OF PUBLICATIONS

International Journals:

1. Singh, A., Sinha, S.K. & Chander, S. "Impact of Fe Material Thickness on Performance of Raised Source Overlapped Negative Capacitance Tunnel Field Effect Transistor (NCTFET)", *Springer, Silicon,* January 2022. **(SCI, IF 2.67)**

   DOI: https://doi.org/10.1007/s12633-022-01696-6

2. Singh, A., Sinha, S.K. & Chander, S., "Effect of shifted gate stack engineering over negative capacitance tunnel field effect transistor (NCTFET)", Engineering Research Express, IOP Science, Vol. 4, Issue No. 3, Sep 2022. **(Scopus Indexed)**

   DOI: https://doi.org/10.1088/2631-8695/ac8fce

3. **Accepted:** Singh, A., Sinha, S.K. & Chander, S., "Simulation Analysis of Noise Components in NCTFET with Ferroelectric Layer in Gate Stack, *Integrated Ferroelectrics, Taylor & Francis,* Oct 2022. **(SCI, IF 0.836)**

International Conferences:

1. Singh, A., Sinha, S.K. & Chander, S., "Analytical Model of Heterojunction Tunnel Field Effect Transistor incorporating the negative capacitance phenomenon", ***IEEE*** *International Conference on Electronics and Renewable Systems (ICEARS 2022),* Tuticorin, Tamil Nadu, India, **16-18 March 2022**. **(Scopus Indexed)** DOI:10.1109/ICEARS53579.2022.9751842

2. Singh, A., Sinha, S.K. & Chander, S., "Effect of Negative Capacitance on Heterojunction Tunnel Field Effect Transistor", ***IEEE*** *International Conference on Electronics, Communication and Aerospace Technology (ICECA)* , Coimbatore, India, pp. 347-350, **2-4 December 2021. (Scopus Indexed)** DOI: 10.1109/ICECA52323.2021.9676074

3. Singh, A. & Sinha, S.K., "Performance Analysis of Device Characteristics in Negative Capacitance Field Effect Transistor (NCFET)", ***IEEE*** *International Conference on Electronics and Sustainable Communication Systems (ICESC),* Coimbatore, India, pp. 297-303, **4-6 August 2021. (Scopus Indexed)** DOI: 10.1109/ICESC51422.2021.9532660

4. Singh, A. & Sinha, S.K., "Comparative analysis of various ferroelectric materials used in Negative Capacitance Field Effect Transistor (NCFET)", *International Conference on Recent Development on Materials, Reliability, Safety and Environmental Issues (IMRSE– 2021),* **NIT Jalandhar**, India, **25-27 June 2021.**

Book Chapter:

1. **Accepted:** Singh, A., Sinha, S.K. & Chander, S., "Device Structure Modifications in Conventional Tunnel Field Effect Transistor (TFET) for low power applications", *Nanoelectronics Devices: Design, Materials, and Applications, Bentham Science Books,* Sep 2022. **(Scopus Indexed)**

UGC Care Listed Paper:

1. Singh, A. & Sinha, S.K., "Reduction of short channel effects in Metal Oxide Semiconductor Field Effect Transistors: A Literature Review", *Think India,* Volume 22, Issue No. 37, pp 170-176, December 2019.