

**DESIGN AND IMPLEMENTATION OF EZ-PASS ROUTER  
FOR ENERGY AND PERFORMANCE EFFICIENT  
NETWORK ON CHIPS**

Thesis Submitted For the Award of the Degree of

**DOCTOR OF PHILOSOPHY**

in

**Electronics and Communication Engineering**

By

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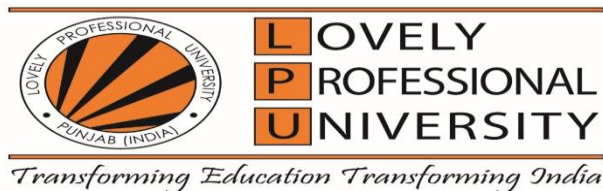
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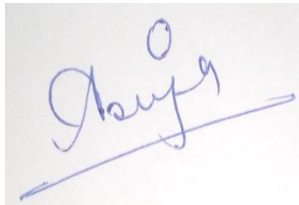
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## **DECLARATION**

I hereby declare that the thesis entitled “**Design and Implementation of EZ-Pass Router For Energy and Performance Efficient Network on Chips**” has been prepared and submitted by me under the guidance of Supervisor **Dr. Sanjeet K. Sinha**, Associate Professor, School of Electronics & Electrical Engineering, Lovely Professional University, Phagwara, Punjab and Co-Supervisor **Dr. Govind Singh Patel**, Professor, Department of Electronics & Telecommunication Engineering, SITCOE, Ichalkaranji, Maharashtra as per the requirement for the award of the degree of **Doctor of Philosophy (Ph.D.) in Electronics & Communication Engineering** is entirely my original work and ideas, references are duly acknowledged. It does not contain any work that has been submitted for the award of any other degree or diploma from any University.



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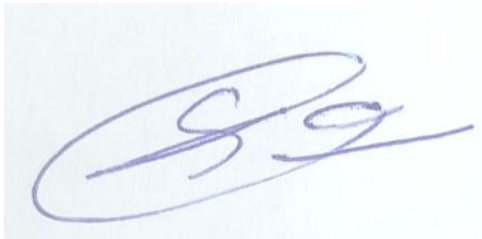
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## CERTIFICATE

This is to certify that **Mr. Ashish Ashok Mulajkar** has completed his Doctor of Philosophy (Ph.D.) in Electronics & Communication Engineering thesis entitled **“Design and Implementation of EZ-Pass Router For Energy and Performance Efficient Network on Chips”** is a bonafide work carried out by him under my supervision and guidance. To the best of my knowledge, the present work is the result of his original investigation and study. No part of the thesis has ever been submitted to any other University or Institute for the award of any degree or diploma.



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## **ABSTRACT**

Network-on-chips is developed as the typical transmission framework to connect Processing Elements and memories on the chip. The NoC acts in areas of enhanced security of networks and also helps to resolve queries in the networking domain. NoC delivers lower scalability, lesser latency and power between PEs associated with chip. Nowadays static power is considered as a leading ingredient in the power utilization in routers while scaling down the technology into a nanometer systems. Also, the effectiveness of the NoC can be influenced by the most important component called buffer because it consumes more power. The area overhead of the NoC architecture design must be minimized for improving the efficiency of the design. In this thesis work a power-gating method is utilized to reduce static power by disabling the power delivered to the routers during their idle condition. Also, an enhanced bypass path method is introduced for reducing the latency during the low traffic condition. But, the main limitations of NoC arbitrations are traffic starvation, worse speed, complication, pipelining, and weak fairness difficulties. The method proposed in this thesis gives suitable solutions to the above limitations.

In the fields of multiprocessing chip architecture and elevated computation, NoCs are becoming increasingly significant. System execution can be upgraded by reducing use of superfluous hardware in router architecture without activating all settings. This study conducts a practical review of several routers that will be used in the future of networking. This analysis looks at the most common interconnection network technologies as well as some new topologies. To reduce latency, enhance throughput of a router, reduce loss of power, design area are the utmost outcomes of this project. A brief comparison of previously constructed several routers as well as design factors for the 3D Torus router is discussed in this thesis work. Also examined were their performance along with their advantages and disadvantages. NoCs is a popular communication channel for connecting several processors and memory modules on a single chip. NoCs

utilize a bigger portion of the whole chip architecture, resulting in higher power costs. The issue comes when the transistor is scaled down.

NoC provides an important router design on comparison with SoCs. NoC provides superior results to the ad-hoc based and bus-based designs since it offers cheap latency, low scalability, and power over processing elements that are linked to a chip. When there is less traffic, the advanced bypass path approach is employed to reduce packet arrival latency. On-chip design area occupancy also gets reduced to improve chip performance. In router design, an EB (Elastic Buffer) control mechanism is utilized to eliminate the cost of the buffer. In such situations, , it becomes essential to propose router with power-efficient routing as well as discard buffer cost In order to make a power-efficient router design, low power NoC router architecture based on Easy Pass (EZ-Pass) routing with IRR and UFDQ is proposed in this system. An advanced NoC router architecture is initiated to enhance the EZ-pass routing and input-port modules of the router architecture with IRR and UFDQ respectively. The proposed circuit includes both a conventional router and an EZ-Pass switch to handle high-traffic, sporadic and low-traffic modes respectively. The IRR arbiter has very short arbitration latency, low power consumption, and a small chip area. In a traditional port topology, the number of multiplexers is grown exponentially as the area of the input buffer is enlarged. Critical track latency, router hardware, and power consumption overhead will skyrocket in this instance. To address these concerns, UFDQ is presented as a way to boost router performance. UFDQ improves router performance at varied injection rates while consuming less power.

A basic partition table is being used by UFDQ for controlling the input port buffer structure. NoC's performance analysis design which is using BLESS, TCMP, BBUS NoC and CHIPPER router design is explained. The NoC module in router architecture is, responsible for connecting chip cores and memory components. Bus and ad-hoc architectures were employed in previous attempts however, NoC is a better option. It provides low scalability, low power, and low latency between computing components embedded on-chip. An improved bypass method is being used when there is less traffic to

reduce packet arrival delay. To increase area utilization and chip performance in the on-chip design should also be reduced. In router design, an Elastic Buffer control mechanism is utilized to eliminate the expanse of buffers. The usage of virtual channels reduces the chips size, latency as well as power loss.

Here, the model of BBUS NoC is deliberated for tackling the latency issue of CHIPPER-based NoC. The proposed router is synthesized using the family of Virtex 6 with device XC6VLX75TL and package FF484. Simulation result shows the potency of IRR on EZ pass routing through the requirement of 41.05% lesser combinational elements and 75 % lesser registers as compared to the RoR arbiter for 16-bit input formation. Simulation remarks also shows a framework which surges bandwidth of router design which requires only 349 Slice LUT and 277 slice registers on FPGA. This proves the efficiency of the proposed router on 16x16 Mesh topology. Also, the concept of Golden Packets is elaborated in terms of BBUS and CHIPPER routers at a lower rate of injection. However, the area overhead of the BLESS is the same as that of the CHIPPER design. The experimental results show that the IRR-EZ pass switch consumes 11% less power as compared to the VC router with UFDQ for 16x16 Mesh topology. The latency of the proposed structure is about 75% less in comparison to VC router while assuming very low rate of injection of 0.005 flits/cycle/node for low traffic. In sporadic traffic mode when the rate of injection is 0.01 flits/time/unit throughput of the VC router is about 40% and the IRR-EZ-Pass router throughput is 90%. In the low traffic mode when the rate of injection is 0.005 flits/time/unit throughput of the VC router is about 20% and the IRR-EZ-Pass router throughput is 80%. A simulation result signifies that the throughput of the novel IRR-EZ-Pass system is higher in accordance with traditional Virtual Channel Router during low as well as a sporadic bottleneck.

**Keywords:-** Network on Chip (NoC), Mesh Topology, Static Power, Easy pass (EZ), Index based round robin (IRR), Arbiter, VC Router, Buffer-less (BLESS), Ultra-fast Dynamic Queues (UFDQ), TCMP, CHIPPER.

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*“Krishnam Vande Jagadgurum”*

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## ACRONYMS AND ABBREVIATIONS

ALO	Ant Lion Optimized
ANN	Artificial Neural Network
ASIC	Application Specific Integrated Circuit
BiNoC	Bimodal Network on Chip design
BW	Buffer Writes
BPG	Beneficial Power Gating
CBCF	Cycles between consecutive flits
CE	Combinational Elements
CUDA	Compute Unified Device Architecture
CMP	Chip Multiprocessors
CR	Credits
CE	Combinational Elements
DAMQ	Dynamically Allocated Multi-Queue
DEMUX	De-Multiplexer
DVFS	Dynamic Voltage and Frequency Scaling
DT	Detection Time
DSM	Deep Submicron
DOR	Dimension Order Routing
EB	Elastic Buffer
EMI	Electromagnetic Interference
FIFO	First Input First Output
FDTR	Fault-tolerant Defection Routing
FPGA	Field Programmable Gate Array
GPU	Graphics Processing Unit
GPS	Global Positioning System
GLONASS	Global Navigation Satellite System
HASE	Hierarchical Architectural Simulation Environment

IP	Intellectual Properties
IC	Integrated circuit
ISI	Inter Symbol Interference
IRR	Index based Round Robin arbiter
LAN	Local Area Network
LRC	Look ahead Routing Computation
LUT	Look up Table
MDM	Mode Division Multiplexing
MFC	Multi Function Channel
MPSoC	Multiprocessor System on Chip
MUX	Multiplexer
NoC	Network on Chip
NoRD	Node-router decoupling
NI	Network Interface
NDS	NoC Design Search
NAS	Neural Architecture Search
NT	Network Topology
OP	Output port
OVC	Output VC
PE	Processing Elements
PG	Power Gating
QoS	Quality of Service
RTL	Register Transfer Level
RC	Routing Computation
RL	Reinforcement Learning
RoR	Round Robin
RP	Read Pointer
SA	Switch Allocation
SSA	Speculative Switch Allocation

SoC	System on Chip
ST	Switch Traversal
STT_MRAM	Spin Transfer Torque Magneto-Resistive Random Access Memory
SSA	Speculative Switch Allocation
TSV	Through-Silicon vias
UDSM	Ultra Deep Sub Micron
UFDQ	Ultra-fast Dynamic Queues
UBPG	Unbeneficial Power Gating
VC-ID	VC Identifier
VCT	Virtual Cut Through
VC	Virtual Channel
WL	Wake up Latency
WiNoC	Wireless Network on Chip

# CHAPTER 1

## INTRODUCTION

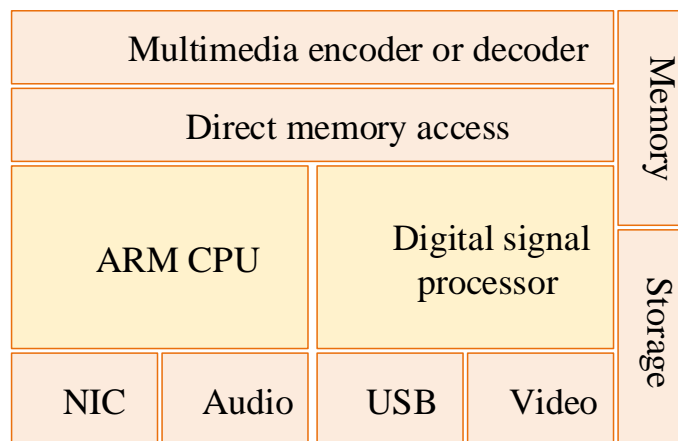
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NoC is a networking technique implemented on an IC which connects each parameter of SoC. It enhances networking techniques in all respects as compared to the conventional bus as well as crossbar systems. NoC architecture is available in a variety of topologies in which research is still in progress. NoC enhances system scalability by reducing power consumption in terms of Static and Dynamic power. Modern networking components use GPU (Graphics Processing Unit) and allied parts. NoC is widely used in Artificial Intelligence enhancement, gaming zones, and also in Visual Graphics. NoC has substantial growth estimates in the future as multi-core computer process becomes the most popular nowadays. This chapter provides fundamental information regarding the NoC architectural representation and routing technologies for the NoC.

### 1.1 Basics of SOC (System on Chip)

SoC is relatively a novel design model that integrates a CPU or several memories, processors, and a peripheral set linked through buses on a single chip. The trend towards multi-core processing processors is now well established based on Moore's law. Because computing power is developed based on dynamic power dissipation calculation exponentially most designers prefer energy-efficient CPUs paired with hardware acceleration to provide the best combination of performance and power consumption [1]. The SoC essentially is an IC (Integrated Circuit) which merges the entire computing modules in a unique platform. I/O ports, CPU, and internal memories are some of the components that an SoC attempts to combine inside it. SoC provides multiple operations like Artificial Intelligence, Neural Networks as well as Mobile Computing [2]. SoC systems are developed by aiming for power saving, and low chip size to reduce the overall cost of the system. SoC meets all objectives by embedding multiple chip modules

onto a single chip with an aim to reduce power and design area [3]. SoC chips help to construct compact devices which can be comfortably carried with us anytime, anywhere without sacrificing the capacity and performance of the gadgets. As a result, they are commonly utilized in systems related to IoT, Embedded Designs, Mobile Phones, Automobiles, and many more areas. Whereas just a few decades ago, an SoC was nothing more than a term, it has now become an essential component of modern technology and the electronics field. Figure 1.1 shows the basic SoC Architecture.



**Figure 1.1: Basic SoC Architecture**

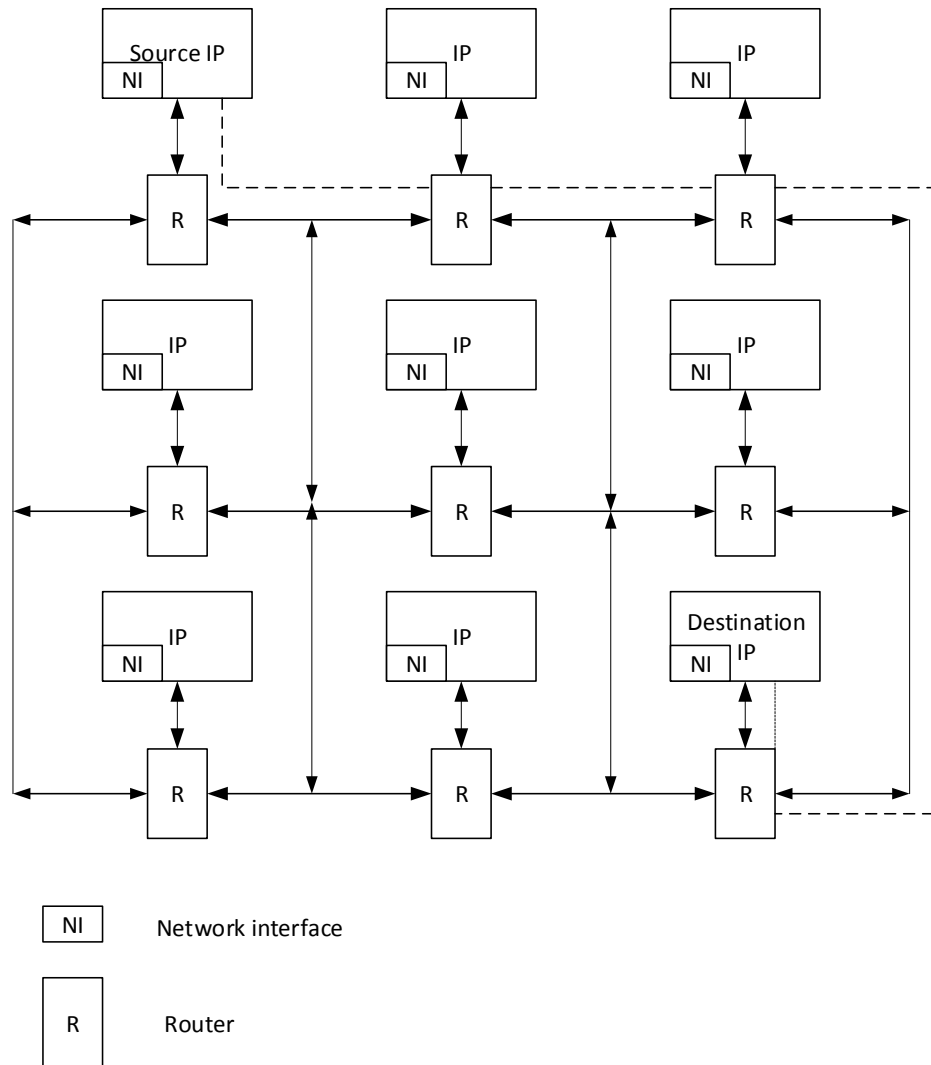
The practical applications of SoCs are essentially endless and priceless. They are found in almost all portable devices including smart phones, optical lenses, i-pods as well as wireless technology. The Cell Phone is the best paradigm showing how SoC operates. More than making or receiving calls, a person also plays games, browses the internet, makes voice and video calls, makes digital payments, and so on mobile phones. These activities are possible because of web connectivity, Graphics Interface Cards, GPS, and GLONASS systems. SoC technology allows users to reduce the size of the system, and make it more compact which can be easy handled and easier to carry. SoC allows users to reduce battery usage, improve browsing time as well as surge the performance of a system. But due to certain limitations in SoC design, the technology is shifted towards implementing NoC design.

## **1.2 NoC Architecture and Function**

A major issue in NoC design is router architecture, which impacts on price and performance of the system. The thesis highlights on design and implementation of a novel router for better performance of the system. Despite the increased number of processing components, SoC designers are facing some challenges of scalability and connecting on-chip components. Traditional systems including buses and buffers are incapable of meeting the rising scalability, performance, timing closure, power, and other features [4].

### **1.2.1 NoC Architecture:**

An organized and scalable connectivity model for NoC is developed for minimizing complicated on-chip design problems for addressing the signal integrity and design productivity concerns of designing a next-generation system [5]. An application may be conceived of as a collection of computer units that need to interact with one another via a collection of communication blocks. To differentiate the impact of these two critical elements on compute time, performance is influenced by delay in gate signals. Computing time is affected by the delay in gate signals while Communication time is affected by wire delay. Ad-hoc communication block can be conducted when the number of processing units is modest. However, as transistor sizes have shrunk in recent years, gate delay has decreased in comparison to wire delay. As a result, in order to put more sophisticated applications on a single chip, we need an organized as well as scalable, and on-chip efficient model.



**Figure 1.2: Basic NoC Architecture**

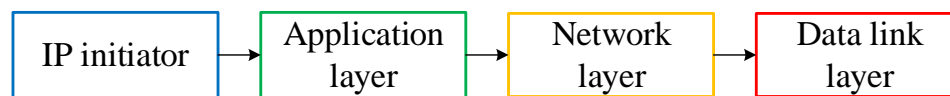
As a result, the on-chip communications architecture design becomes dominant as design concepts are shifted from computing basics to advanced communication techniques. In the face of advancement in communication, the phrase "network on chip" refers to an architecture that maintains a conveniently designable solution. We will go over some key concepts for creating an NoC communication system in this part. Furthermore, the function of NoC may be divided into several levels, which will be brought in the right order. Figure 1.2 indicates the basic NoC Architecture which contains numerous lengths of cables as well as routers. The wire and router type NoC system is designed similarly to the city street grid, while the user is set on wire-separated blocks. The client's logic



processor core data packets are converted to fixed packets by NI modules. Data packet flit is made up of tail flit, header flits as well as in between body packets [6]. This flit array will be sent in the direction hop by hop via adjacent routers.

### 1.2.2 NoC Function:

The NoC function is divided into various layers: network, transport, application, physical and data connection. To provide layer functions, an NoC router needs to have both, software and hardware implementations. Different layers in NoC structure are shown in Figure 1.3



**Figure 1.3: NoC Layer Structure**

#### *Application layer*

The target application is separated into communication activities and computer collection at the application layer allowing performance characteristics such as energy and speed to be regulated. The location of cores on the NoC must be altered in order to minimize overall communication or energy consumption while also taking into consideration the constrain of any single link. Communication scheduling and task mapping are examples of NP-hard restricted quadratic assignment problems. A set of concurrent tasks is described by a given target application with an NoC architecture. There are some fundamental questions to be answered which are (1) how the complex network condition effect is accounted, for which changes at text execution dynamically; and (2) how to put chosen core set on the network components topologically in order to maximize the metrics of interest application. Scheduling and mapping should be reviewed in conjunction with a design range of elements to obtain the best balance of power and performance.

### ***Transport Layer***

In order to minimize buffer overflow and traffic congestion, various organization strategies are supposed to be used to show packet transmission in NoC. Congestion and Flow control concerns are addressed by the transport layer. NoC key performance indicators are high throughput rate and low packet delivery delay, both of which be severely damaged by system congestion induced by source arguments. As a result contention resolution is critical for avoiding network congestion. One of the most important concerns for contention resolution is to improve the available network resources efficiently to achieve higher communication performance under the assumption of a dead-lock and live lock-free routing algorithm.

### ***Network layer***

Network topology is also known as interconnected design. The Network layer becomes important because it influences how network resources are connected and therefore it is referred to static channel configuration node for the associated network. Combining and splitting various communication architecture types in a mixed fashion that provides more customizability and connectivity at the complexity price and area forms irregular topologies. Furthermore, optimizing a topology that affects router connections and the distance between cores is a complex issue. Moreover, the balance between customization and generality is crucial for performance and scalability. The architecting cost along with manufacturing semiconductor cost climbs due to high complexity. A homogeneous NoC employed identical cores and routers, but a heterogeneous design chooses IP library cores and can adjust the communication architecture along with application necessities. Most cutting-edge chip designs employ Mesh and Torus topology for two-dimensional systems as it has better performance with a high degree of scalability, which may not provide the greatest performance for a particular application.

Also, the network layer must dispense with data routing among processing components. The first packetizing algorithm deals with breaking down a single message into small

packets at the source node and assembling them at a destination node. Transmission of packets can then be carried out using a number of routing techniques based on various network topologies. A routing method verifies how a packet will be routed via the source node to the destination node. The router's main responsibilities include identifying flit routes and solving disputes among packets when a similar path is required for boosting on-chip communication speed.

A router's traditional architecture comprises an arbitration controller and circuit-switched fabrics. As long as there is no dispute between these pathways, the crossroad switch can be used to create more than one path in each arbitration decision. VC flow control-based router design is a known approach from an area of multiprocessor networks for most existing switch designs allowing increased elasticity as well as channel usage with reduced space of buffer.

### ***Physical and Data link layer***

The prior purpose of data link layer protocols reducing link dependability to a lower necessary level, assuming that the physical layer is insufficiently dependable on its own. The physical layer's concentration is on signal receivers and drivers and design solutions for pipelining and resorting signals on a wire. Furthermore, when technology evolved to UDSM (Ultra Deep Sub-micron) lower voltage fluctuations and diminishing feature size translates to lower noise margins, on-chip interconnects, lower noise resistance making, and increasing non-determinism likelihood in data transmission across wires. Electric noise caused by radiation-induced charge injection, electromagnetic interference (EMI), and crosstalk would almost certainly result in timing and data mistakes making dependable on-chip connectivity difficult to accomplish. These layers are primarily concerned with error control systems and the use of physical connections to improve dependability. To begin, a plausible fault model must be created. Then a high bandwidth, low-area, low-power, low-latency error control method should be created. Packet-based transmission of data is an effective technique for handling data faults in NoC architecture

since the error effect is presented through packet boundaries which are retrieved flit by flit.

### **1.3 Building blocks of NoC**

A network-on-chip is made up of three primary components [7].

- The most crucial one is the Communication Links that physically link nodes and allow making communication.
- The router is the second block that is responsible for implementing the communication protocol.
- NA (Network Adapter) and NI (Network Interface) is the last construction piece. This block establishes a logical link between networks and IP cores.

#### **1.3.1 Communication Link:**

A communication link is a series of cables that links two routers in a network. A couple of logical channels are required to form links and each is made up of a wire set. The defining of the integration protocol among source as well as target nodes is included in the implementation of connection [8]. It can be analyzed using specified wires during communication and different methods like First Input First Output (FIFO).

#### **1.3.2 Routers:**

An NoC router consists of many input and output ports, a switching matrix that connects IOs as well as a local port that connects to the core IP. The router includes a logic block that executes flow control rules and determines the overall strategy for transferring data through the NoC.

The following are the route's key design elements

- Flow Control - Defines packet flow in an NoC, both globally and locally. The control logic ensures communication performance and quality of service. Control can be either-
  - Centralized or diffused - Routing choices are made globally and implemented to all nodes in centralized control, using a technique that ensures no traffic congestion. This necessitates that all nodes have the same sense of time. Each router makes choices locally in a distributed control system.
  - Routing Algorithm - Logic that chooses one of the output ports to route a packet received at the input port: Deterministic Routing and Adaptive Routing are two types of routing available. In Deterministic Routing, a similar path is considered among two particular nodes to take a packet. Alternative pathways between two nodes may be employed in adaptive routing when a local link or original path is crowded.
  - Arbitration Logic – The Routing Algorithm selects the output port to the packet router's arbitration logic and picks one input port when many flits are present.
  - Buffering - This policy retains information in the router if there is network congestion and packets are not transmitted quickly.
  - Switching - Switching governs how information is shared from source to destination. The payload is not transmitted until the entire route is reserved. This can result in increased delay, but once the path is determined, this strategy provides several assured throughputs for instance. Header creates the link between routers and sends all flits of the packet in a packet-based switching strategy.

### **1.3.3 Network Interference:**

NI block provides a logic link between the network and the IP cores as every IP uses a different network interface protocol [9]. This block is crucial since it provides for the

separation of communication and computation. This enables independent reuse of both communication infrastructure and core.

The adaptor is separated into two parts:

- The front end is in charge of the core plea, and should be not able to detect NoC. It is commonly implemented at VSI Alliance (VCI) sockets, OCPIP (OCP), Philips Semiconductors (DTL), AXI 2011, and so on.
- The Network protocol is handled by a back end (disassembles and assembles the packet. helps the router in storage, reorders buffers, implements synchronization protocols, etc.).

## **1.4 NoC Routing Concept**

NoC is a network-based communication system on a semiconductor IC that is usually used to communicate amongst SoC modules. A system on a chip (SoC) is a chip that incorporates computer components such as a Central Processing Unit (CPU), graphics, and memory interfaces. Pre-designed intellectual property (IP) cores/blocks are becoming increasingly significant in SoC architectures. As semiconductor chip dimensions drop and more IP cores are added to them, many SoC devices have become too complicated to use a typical data bus or crossbar connectivity architecture. Physical resources holding data on chips and service quality begin to deteriorate. NoC technology offers significant advantages over traditional data bus and crossbar communication designs [10]. The purpose of NoC scheme is to organize communication amongst operational modules that are placed on the same chip. The technique boosts the scalability and energy efficiency of complicated SoCs.

Some of the benefits of NoC versus SoC [11] are as follows-

1. NoC provides structured architecture, reducing chip design complexity and expense.
2. NoC enables the re-use of components, architectures, design processes, and tools.
3. Offers an economical and high-performance interconnection
4. Increases the scalability of the communication architecture
5. Establishes a link between processing blocks by routing data packets, allowing for flexible and easy change adaptation.
6. Reduces cable routing congestion and eliminates timing closure difficulties.
7. Reduces the complexity of switching and routing tasks in order to reach greater operating frequencies.

A mechanism is created considering the on-chip IP ports for ensuring proper communication. Proper Algorithm only allows proper communication via source to destination. Previously noted routing algorithms are free of starvations and deadlocks are crucial in chip design. The routing algorithm may be chosen built on a variety of interconnected properties, which results in tradeoffs between associated parameters like energy consumption, packet delay, and footprint which define routing method standards. By keeping the routing simple, power for routing may be less hence the power consumption is decreased. Furthermore, routing tables should be reduced to improve speed. This will aid in assuring reduced latency, increased resilience, a small footprint, and efficient network use. Generally NoC routing methods are divided depending on characteristics like distance, decision state as well as routing paths. NoC algorithms are separated into dynamic and static routing algorithms. Determination of routing choices is

done by using distributed, minimum, source, or non-minimal routing algorithms. The static and dynamic routing algorithms are discussed in this section.

#### **1.4.1 Static Routing:**

The simplest and most often used routing technique in NoCs is Static Routing, also called-deterministic or oblivious routing. It is used for data transport between a given destination and source which uses fixed (predefined) pathways. Furthermore, the present status of the network will not be considered in Static Routing. As a result, if a routing decision is being made, the load on connections and routers is ignored. Static routing needs relatively minimal router logic, making it simple to build. Furthermore, packets can be planned to be shared across numerous pathways between the source and destination. In addition in a case where only one path is used static routing can guarantee in-order packet delivery [12]. In this way, reordering and identification of packets at the destination do not require adding bits at the NI. Static Routing techniques include random walk routing, directed flood, probabilistic flood, Dimension Order Routing (DOR) destination tag, turn model, XY, surrounding XY, and pseudo-adaptive XY. Deterministic distributive routing is a kind of XY routing. The coordination of destination address in this approach is employed to send a packet through a network. The path is then followed along the Y coordinate vertically until it reaches the final destination. XY Routing is a common approach to Mesh as well as Torus topologies since it reduces deadlocks. However, because of the load that is regularly produced in the center of a network, the accompanying traffic may be irregular and the XY algorithm is incapable of eliminating crowded and congested lines.

#### **1.4.2 Dynamic Routing:**

Dynamic and Adaptive Routing depends on the current underlying state of the network. Aspects such as system availability and connection load status are considered while deciding routing decisions in this routing method. As a result, the path between the destination and source may change as application needs and traffic circumstances change [13]. Dynamic routing allows traffic to be distributed across several routers more

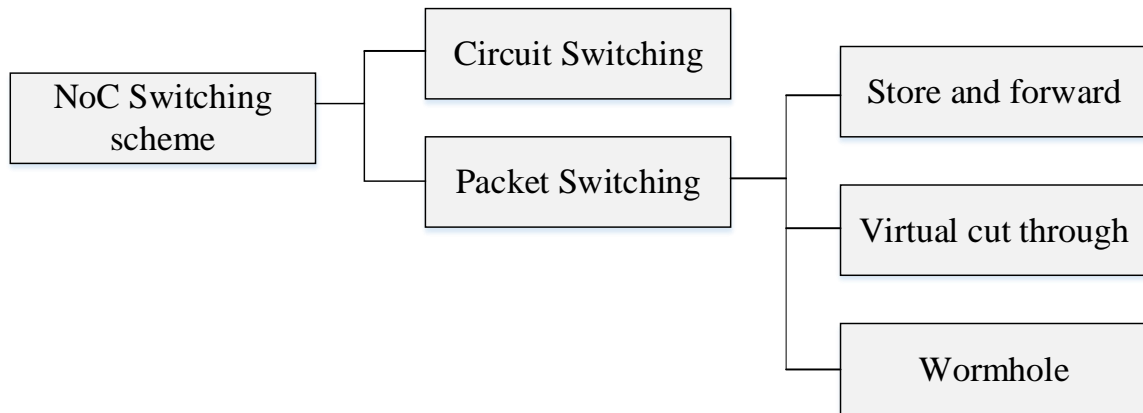


efficiently than static routing. Furthermore, it can employ different channels in the network congestion case in particular NoC lines. In this sense, its topology may be able to support more traffic and network capacity utilization can be minimized. The ability of adaptive routing to employ global information about current traffic status in optimum path selection is one of its distinctive features. The flexibility of this strategy, however, comes as the extra resource requires regular upgrading of network conditions for assuring comparable variable shifts among routing patterns. It typically increases the router's complexity. Furthermore, adaptive routing performance is limited by the amount of global knowledge that can be sent to each router as well as interference. As previously stated, a static routing system is normally utilized in situations where traffic requirements are stable and predictable, whereas dynamic routing is frequently employed in unpredictable and irregular traffic conditions. Slack time aware, turn around-turns back, congestion look-ahead, odd-even, entirely adaptive, turn back when possible, minimal adaptive, and deflection are examples of adaptive navigation algorithms (hot potato). Adaptive and Deterministic routing strategies will be utilized in NoC to communicate between the destination and source. The odd-even routing approach is a non-deadlocking adaptive routing paradigm. East-to-North and East-to-South turns are thus prevented in even columns. As a result, the odd-even routing strategy helps to eliminate potential live locks in the systems. The deflection routing method is economical since no buffers are employed. As a result, arriving packets are not queued by the routers and are routed simultaneously to their destinations using the routing tables. When a busy router gets other packets, misrouting might occur. In such a server environment, distort packets in a network might generate more misrouting, causing every flit to bounce around the network like a hot potato technique. By allowing sufficient gaps between packets, misrouting may be significantly reduced.

## **1.5 NoC Switching**

NoC switching scheme specifies data transmission granularity and identifies the switching strategy used for data control in routers. The primary switching mechanisms in

NoCs are Packet Switching and Circuit Switching [14]. Figure 1.4 denotes the classification of various Switching Schemes in NoC.



**Figure 1.4: Switching Strategies**

### **1.5.1 Circuit Switching:**

Prior to the transmission of data, this switching is dependent on reserved physical channel development between the source & destination which consists of routers and connections. Although circuit switching provides low latency transmission by utilizing the whole connection capacity it wastes existing lines when no data is transmitted posing scalability issues. Virtual-circuit switching can be used to increase network scalability. It allows several virtual links to be multiplexed onto a physical link. Allotted buffers determine the number of essential connections that physical links will sustain.

### **1.5.2 Packet Switching:**

Another prominent switching mechanism is packet switching. In contrast to circuit switching, where the way is established before data transfer there is no requirement to build before packet transfer a route (no link reservation) before packet switching. The transmit packets in this context take distinct pathways from transmitter to receiver. As an outcome, the packets will incur varying delays [15]. Furthermore, unlike circuit switching, which frequently has a certain standby time and minimum latency, this switching has a

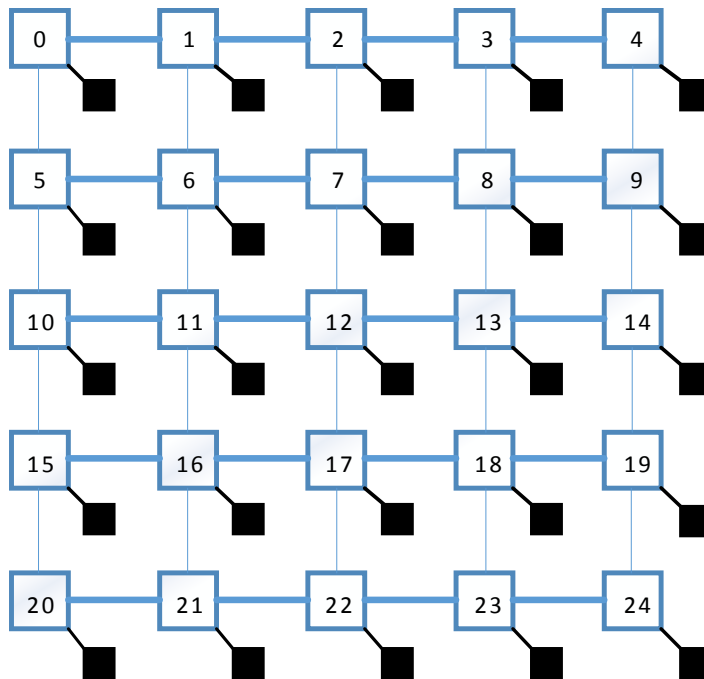
null start-up time and fluctuating delay owing to the congestion. Furthermore, due to the conflict, ensuring QoS (Quality of Service) in packet switching is more exacting as compared to Circuit-Based switching. VCT (Virtual Cut Through), wormhole, store, and forward are common packet-switching strategies.

## **1.6 Topologies used in NoC**

Topology design is quite important in NoC. Throughput, rate of injection, latency, chip area, and hop counts are network performance parameters [16]. The role of NoC in ensuring seamless and effective communication amongst IPs (Intellectual Properties) is critical. Topologies are constructed and classed according to factors like hop counts, throughput, latency, and injection rates.

### **1.6.1 Mesh Topology:**

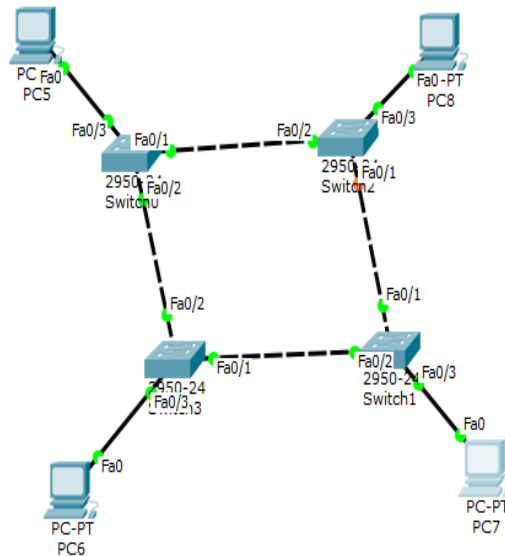
It is a sort of direct topology in which nodes are connected directly to one another. It increases route variety while simultaneously improving scalability. Mesh topology was originally created for military uses, but it is now employed in home automation, multimedia processing, and smart cities. This data is shared among all nodes. It has several sources-to-destination paths and an efficient addressing method that prevents network disruption. All the nodes are linked together in form of a 2D lattice and nearby nodes are linked together. In Mesh Topology inter-switch delays and network, robustness may be avoided. Figure 1.5 shows a model of Mesh Topology in NoC.



**Figure1.5: Model of Mesh Topology in NoC**

### 1.6.2 Ring Topology:

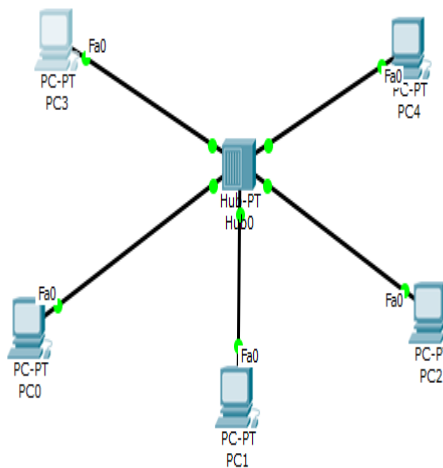
It is a network architecture where a circular link is built to convey data between nodes. It is a one-way ring network in which packets only move in a single direction. It is regarded as one of the most popular topologies. Because each neighboring node is connected by a single cable, each node has two nearby neighbors. Figure 1.6 shows the Ring Topology [Source: CISCO Packet Tracer]. Because equal bandwidth is supplied to each node, the degree of each node in the Ring topology is two [17]. The shortcoming of Ring topology is that if a single cable fails, the entire network fails and as a result network growth affects overall network performance. The data is routed via each node in the ring until it arrives at the target node.



**Figure1.6: Ring Topology**

**1.6.3 Star Topology:**

Star topology is simple among all other existing topologies in terms of construction [18].

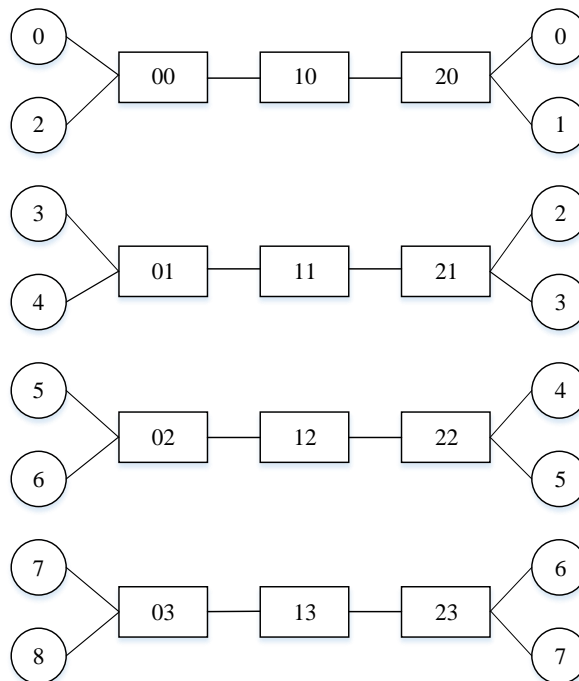


**Figure1.7: Star Topology**

It is a Local Area Connection (LAN) structure where each node is connected to a central location similar to a hub. This design needs extra wires than other typical topologies. The fundamental disadvantage of star topology is that if the central node fails, the entire network fails. The width of the center node grows as the number of nearby nodes connecting to it grows. Figure 1.7 shows the Star Topology model [Source: CISCO Packet Tracer].

### 1.6.4 Butterfly Topology:

This architecture connects a large number of computers to extremely fast networks. The main components of this design are processor nodes, routers, and connections. The node connections are depicted in the model. Butterfly topology design and implementation take into account network factors such as bisection bandwidth, degree, and diameter. Figure 1.8 shows the Butterfly Topology in NoC



**Figure1.8: Butterfly topology in NoC**

## 1.7 Metrics for Comparing Various Topologies

**Degree:** The number of links at each node refers to a degree. The Ring Topology as shown in Figure 1.6 has two links at every node. Hence it has a degree of 2. The Torus Topology has a degree of 4 as every node has four links connected to four neighboring nodes. The implementation complexity has increased to a greater degree and needs maximum ports at the routers.

**Maximum Channel Load:** This parameter is useful to estimate as a proxy the higher bandwidth supported by the network. It is somewhat synonymous with the injection bandwidth. If the channel load is two determines the load on a channel is twice the injection bandwidth.

**Hop Count:** When a packet is passed from one network segment to another is called a hop count. Hops are useful as proxy methods used to calculate network latency. The diameter of a network determines the maximum hop count. The hop count for Star Topology is 4 as shown in Figure 1.7, for Mesh Topology hop count is also 4, while for Torus Topology the hop count improves to 2.

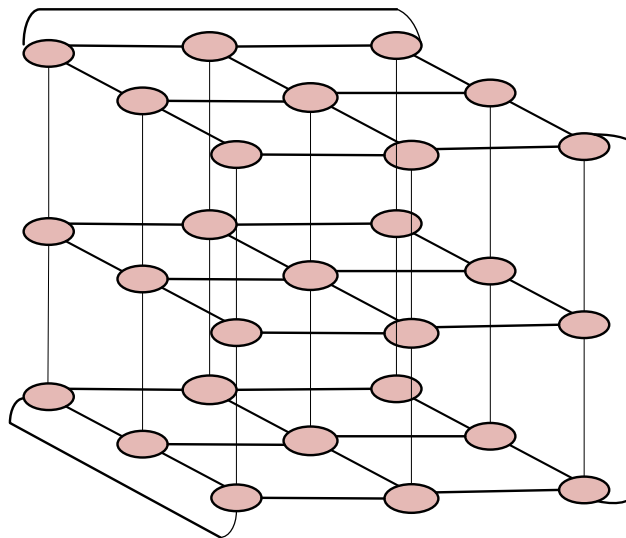
**Data Packets:** The Bundle protocols link numerous subnets to a common single network. Bundles consume less channel width. A system can have a modified or variable bundle length. Generally, a bundle will be prefixed with data about the destination. In a system, with variable-length parcels, the length is to be integrated at the end of the bundle. Typically the parcels are split into bounces. The bounce is having the same size as that of channel width, which is the biggest measure of information that can be parallel moved.

## 1.8 Router Architecture design for 3D Torus

The router is built using a credit-based flow control method. It entails the design of an adaptive routing algorithm that uses switching techniques to execute virtual cuts. Torus is a donut-shaped object represented as an O ring which is formed by rotating a circle via three dimension spaces about the axis that lies in the same. The mathematical expression in Cartesian coordinate for torus is mentioned in Equation No.1.1

$$Centre_C = \sqrt{u^2 - v^2 + z^2} = R^2 \quad (1.1)$$

Where the radius of the torus from the center of the circle to the Centre of the Torus tube is represented as  $Centre_C$ , u-v-z is the indication of three axes and  $R^2$  represents the radius of the tube. The router is built to support a novel topology known as 3D Torus [19]. Figure 1.9 shows the 3D Torus Architecture. It has 1 port that is connected to the PE port and 6 ports that are connected to neighboring nodes. The hardware parameters of the 3D Torus are implemented on devices like the Xilinx Kinetic 7 and confirmed using the Xilinx 14.7 tool as illustrated.



**Figure 1.9: 3D Torus Architecture**



- i. **Buffer:** Buffers are FIFO (First Input First Output) devices that store flits and packets while the output port is busy.
- ii. **Routing Path Controller:** It is used to perform adaptive routing algorithms and manages the path for packets to be sent across the network.
- iii. **Virtual Channel Controller:** This component manages any system deadlocks. VCs are driven by adaptive routing algorithms, which give a fixed route for packets coming via numerous channels.
- iv. **Arbiter:** The Arbiter connects both input and output connections. It is put through a fairness test. Basic arbiters include variable priority arbiters, round-robin arbiters, and fixed concern arbiters.
- v. **Allocator:** Its purpose is to create switching between input and output channels. The allocator aids in the management of connections between both channels while taking into account requests made via a specific channel.

## 1.9 NoC design in Tiers

As per the abilities and expertise of NoC designers as well as the complex issues they deal with in multi-tier architecture for network operations center design help properly share duties with different NoC levels [20].

### 1.9.1 NoC Tier 1 - first aid:

At this level, the NoC receives architecture-related queries and handles network issues including login difficulties and network configuration checks. NoC Tier 1 professional employee's problem-solving scripts that include step-by-step guidance for efficiently resolving difficulties. NoC Tier 2 professionals are assigned to problems that demand a higher level of technical competence.

### 1.9.2 NoC Tier 2 - More complex issues:

This level is made up of more complex professionals and deals with more complicated network difficulties which typically need a better grasp of the supporting IT architecture.

Resolving configuration difficulties, account management, and service restart are all regular responsibilities of NoC Tier 2. If a problem necessitates additional in-depth investigation at the code level, it is escalated to NoC Tier 3.

### 1.9.3 NOC Tier 3 - Advanced problems:

Tier 3 serves as a top escalation point for NOC Tier 1 and Tier 2 specialists. Tier 3 architects are responsible for handling issues on the code and database levels and providing hotfixes. Resolving issues at NOC Tier 3 requires major skills, so you can either keep it in-house or outsource to a vendor who is ready to work at the backend level.

### 1.9.4 Build an orderly NoC:

The foundation for well functioning network operations center is a well-chosen structure. We may tackle various issues of complex variables quickly making our network architecture genuinely trustworthy by adopting a multi-user model with correct escalation protocols for our NoC.

## 1.10 Advantages of Mesh Topology

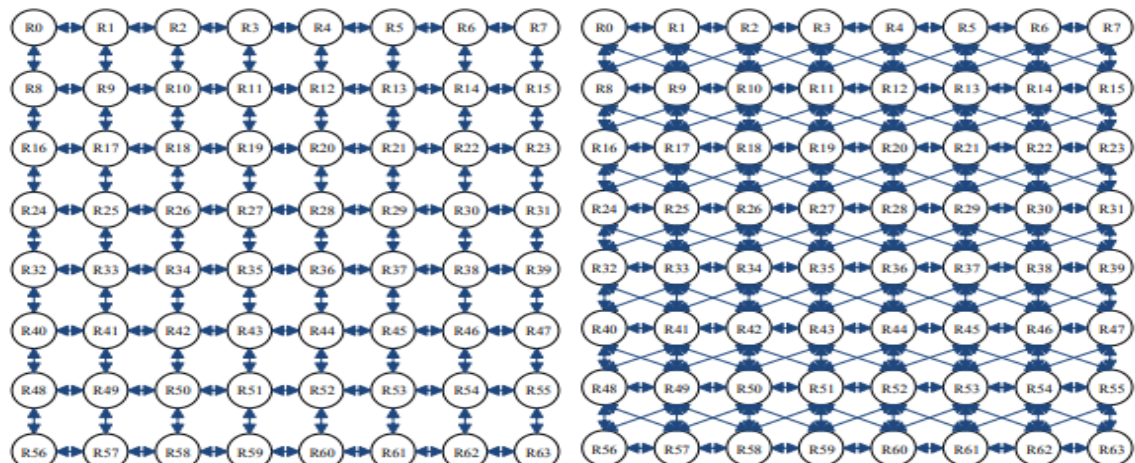


Figure 1.10: Node arrangements in Mesh and Full Mesh Topologies (Ng Yen et al.)

[21]

The diameter for node arrangements in Mesh and Full Mesh Topologies is given by  $2n-2$  where  $n$  equals the number of nodes. The bisection of Mesh is given by  $n$ . The Mesh topology improves network performance by considering power reduction and less latency. Figure 1.10 indicates Node arrangements in terms of hops for Mesh and Full Mesh Topologies. Table 1.1 denotes Hop Counts in Mesh and Full Mesh Topologies respectively.

**Table 1.1: Hop Counts-Mesh and Full Mesh**

		Path		Hop counts	
Transmitter	Reception	Mesh Topology	Full Mesh Topology	Mesh	Full Mesh
0	63	0-8-16-24-32-40-48-56-57-58-59-60-61-62-63	0-9-18-27-36-45-54-63	14	7
5	35	5-3-21-29-37-36-35	5-13-21-28-35	6	4
20	38	20-28-36-37-38	20-29-38	4	2

### 1.11 Motivation for Thesis

A packet-based NoC, in general is made up of routers, Network Interface between the routers, the processing units, and the interconnection networks. Each processing unit can be a general-purpose CPU, DSP an embedded memory, or something else entirely. Each processing unit is linked to a router, which links it to the processing units next to it. Later in the article, we will refer to a processing unit and its associated router as a node. The

main motivation for developing this thesis is to propose an EZ-Pass Architecture for improved performance and energy-efficient NoC.

The following issues must be addressed in the design of an NoC system.

**Scalability:** The interconnection network in an NoC system plays a vital role in offering scalability to accept a higher number of transistors and close the design productivity gap. To keep wire lengths short, on-chip networks will most likely adopt networks with reduced dimensions.

**Energy Efficiency:** When developing an NoC system, power must be considered as a primary design constraint because the interconnection network consumes a substantial amount of power. The interconnection network's power consumption is mostly determined by the energy consumed by the routers and the energy consumed on behalf of interconnections, which is connected to the architecture itself, the routing and switching strategies used and the power implementation approaches.

**Re-configure:** One of the most essential architectural paradigms for meeting the concurrent needs for application performance and adaptability is to re-configure the architecture. Re-configured architecture is especially appealing to reality applications owing to high efficiency, cost savings, reaching markets faster, increased flexibility, and upgradability[22]. Topology selection, communication protocol selection, and application mapping to processing units are all critical trade-offs in the design of NoCs. Systematic classification of NoC design concerns, an overview of the topologies and communication protocols utilized in NoCs is presented here as they are directly connected to router design.

## **1.12 Research Challenges**

The primary purpose of the communication-centric design and the NoC paradigm is to improve design productivity and performance by dealing with rising parallelism, manufacturing complexity, wiring issues, and dependability. According to Owens et al.,

the three main hurdles for NoC are power, latency, and CAD compatibility. Several ways for networks-on-chip to solve the issues associated with bus-based interconnects have been developed allowing increased reusability and programmability through the use of standardized and layered communication protocols thus leaving reuse of communication resources and enabling increased reusability and programmability. A common strategy for NoCs is to use a regular Mesh Topology with packet switching which allows total system capacity to raise for each additional network node as the number of concurrent communication channels increases [23]. In contrast to shared bus techniques, NoCs offer better performance scalability and handle several concurrent transactions, resulting in more efficient network resource consumption. Furthermore, the relationship between wire length and system size is affected by the distribution of area between network components, and hence by the network's regularity, 2D mesh NoC assumes a constant wire length, regardless of system size. To boost system productivity, an architect must be able to abstract, represent, and handle the majority of design challenges and concerns at a high degree of abstraction. The system-level design allows one to swiftly trade-off between several QoS criteria like latency, power, cost, size, and ease of integration by reviewing many potential software-hardware architectures that match the functional standards equally well. Similarly, there are various NoC concerns to consider including the type of the NoC link, link length, serial versus parallel links, bus versus packet-based switching, and leakage current.

### ***Serial versus Parallel Link***

The transfer of data packets between cores in an NoC can be accomplished via either a serial or a parallel connection. Parallel connections have a buffer-based design and may be run at a lower clock rate to save power dissipation. However, the silicon cost of these parallel lines will be considerable due to inter-wire spacing, shielding, and repeaters. This can be reduced to a certain extent by using additional metal layers. Serial connections, on the other hand, provide for wire space reductions, reduced signal interference and noise, and the elimination of the requirement for buffers. Serial linkages provide the benefits of a simpler layout and easier timing verification. When running at high clock rates, serial

connections might experience ISI (Inter symbol Interference) between subsequent signals [24]. Nonetheless, such limitations can be mitigated using encoding and asynchronous communication methods.

### ***Interconnect Optimization***

Communication in NoC is based on modules connected by a network of routers with extended interconnects between the routers. As a result, it is critical reducing interconnects in order to achieve the desired system performance. The installation of repeaters is commonly used to optimize the timing of global wires. It has a considerable impact on cost, area, and power usage. According to recent research, inverters acting as repeaters will consume a significant percentage of chip resources in the near future. As a result, there is a need to optimize power on the NoC. Encoding is an efficient method of lowering dynamic power use. To make NoC designs more successful, novel approaches to optimizing the power spent by on-chip repeaters must be developed.

## **1.13 Applications**

Messages can travel from the source module to the destination module over many links that include routing choices at switches in a network on a chip. It has several point-to-point data lines that are linked together via switches. It may be categorized as a scalable homogeneous switching fabric network [25].

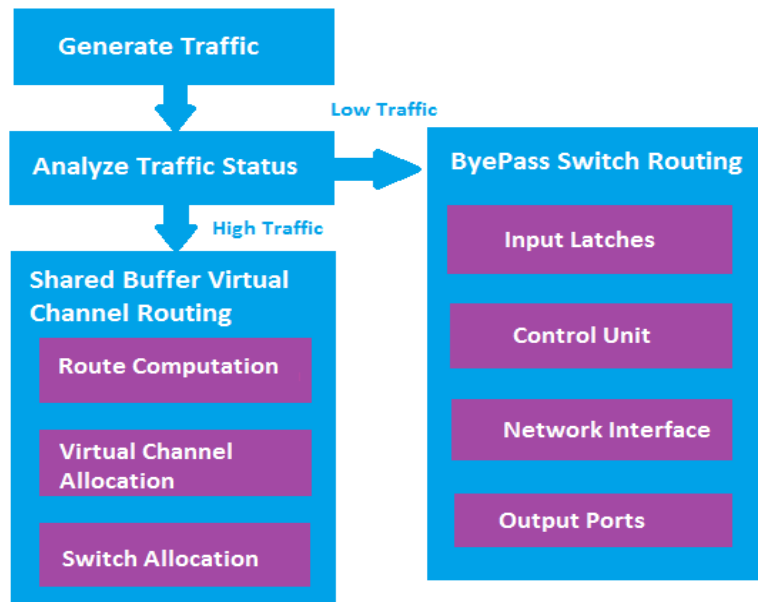
The following characteristics are found in NoC which are as below

- NoC reduces the amount of hardware required for routing and switching activities.
- Different portions of the network can provide multi-topology and multi-option support.
- When integrated with a network on a chip, scalability, interoperability, and feature development are improved.

- When compared to alternative designs, a network on a chip improves the power efficiency of complicated system-on-chips.
- Synchronization problems are addressed more effectively than in previous approaches. The network on a chip also handles wire routing congestion better than other system-on-chips.
- Network-on-chip enables higher operating frequencies, and timing closure is considerably simpler to implement.
- Because of its well-designed and tiered strategy, problem verification is significantly easier.

### **1.14 Research Methodology**

Basically, NoCs consume large amounts of entire chip power in a range of 10% to 36%. Hence a Novel approach to reduce power loss in terms of Static and Dynamic must be implemented. NoC connects various memory modules on a chip. Hence the architecture is proposed to reduce Static Power by Power Gating Techniques and reduce Dynamic Power by shared buffer concept to improve systems performance. Figure 1.11 indicates the proposed methodology.



**Figure 1.11: Proposed Methodology**

### 1.15 Thesis Outline

**Chapter 1:** This chapter is a brief introduction to NoC and its functions. It also includes NoC architecture, Network Interface, Building block of NoC, Routers, NoC routing, Static routing, Dynamic routing, Switching strategy, NoC topology, Router architecture design for 3D Torus, NoC topology, NoC design in tiers, Motivation, Challenges, Application, and problem statement.

**Chapter 2:** This Chapter includes a literature review of the different techniques used in the design and implementation of EZ-pass routers for energy and performance-efficient NoC design. Several methods are used in energy and performance-efficient NoC design, they are included in this chapter with the advantages and disadvantages of each standard. Also includes the emerging trends used in NoC design, different performances used in NoC designs, and different frameworks used for designing energy and performance-efficient NoC designs can be analyzed using various techniques with advantages and disadvantages - analyzed with existing methods.



**Chapter 3:** This Chapter offers a realistic review of numerous routers that will be utilized in networking in the future. This chapter examines the most widely used interconnection network technologies, as well as several novel topologies. To reduce latency, enhance the throughput of a router, reduce power consumption and design area are the major outcomes of this chapter. This chapter includes a brief comparison of previously built routers as well as design criteria for the 3D Torus router. Examine their performance and build a list of their benefits and drawbacks. NoCs are a common communication route used to connect several processors and memory modules on a single device.

**Chapter 4:** In this chapter, a new NoC router design is proposed by extending the router architecture's Easy Pass routing and input-port modules with IRR and UFDQ respectively. This system comprised both a traditional VC router and an EZ-Pass switch to manage heavy traffic as well as intermittent and low-traffic modes. It also employed a control block and the power gating approach to turn off routers after a period of inactivity. The simulation results show that the proposed IRR-EZ pass switch has very low latency, reduced chip area, and power consumption when compared to a typical VC router. Furthermore, the addition of UFDQ and IRR helps to increase the router's performance at diverse injection rates while consuming minimal power due to its simplest hardware construction.

**Chapter 5:** In this chapter, the performance analysis of NoC design using BLESS, BBUS NoC, TCMP, and CHIPPER router design. When compared to standard buffer-less routers, the use of a permutation deflection network with parallel output port allocation minimizes the average flit latency of CHIPPER. The Golden Era is vastly superior in BBUS. The normalized critical path and normalized router areas of CHIPPER routers were reduced by 29.1 % and 36.2 %, respectively. When nodes require a diverse number of packets before data processing, the proposed BBUS technique can be credibly implemented. Better results are the product of high-quality effort. The approach proposed enables the development of multi-core processors.

**Chapter 6:** This Chapter includes concluding remarks, applications, and the future scope of the proposed architecture.

## CHAPTER-2

### LITERATURE SURVEY

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This chapter summarizes the different techniques used in the design and implementation of EZ-pass routers for energy and performance-efficient NoC design. Several methods are used in energy and performance efficient of NoC design is included in this chapter with advantages and disadvantages of each standard. Also includes the emerging trends used in NoC design, different performance parameters used in NoC designs and different frameworks used for designing energy and performance-efficient NoC can be analyzed using various techniques with advantages and disadvantages compared with existing methods.

#### 2.1 Emerging Trends in Network on Chip Design

Monemi et al. [26] propose a multiple-core SoC module to design low-latency NoC. In this work, the Network-on-Chip (NoC) is integrated with rapid prototyping which validates the NoC-based many-core system-on-chip projects to target the field-programmable gate array devices. The proposed Pro-NoC model consists of the most improved NoC features they are virtual network, several routing algorithms, support of virtual channels, and low latency routing. The experimental result of the proposed model interconnects the Pro-NoC outperforms CONNECT which enhances the maximum operating frequency, lower logic cell utilization, lower average communication latency, and saturation throughput. In addition to that Pro-NoC methods are embedded with GUI which ensures MC-SoC enhancement through the FPGA platform.

Boyapati et al. [27] established a Network on Chip architecture by using a data approximation framework. In this work the Approximation Network on Chip (APPROX-NoC) framework is proposed which is a hardware data approximation used in online data error for a control mechanism used to enhance the NoC performance.Using APPROX-

NoC method ensures the related match of pattern to suppress data capacity in the chip. The experimental results of established work enhance the performance of NoC data compression which also reduces the low application error. In addition to that the data-intensive graph process applications are used to obtain a 36.7% of latency reduction.

Abadal et al. [28] analyze MAC in wireless NoC efficiently. In this work, the performance objectives, physical constraints, and traffic characteristics of the on-chip communication framework are analyzed clearly. In addition to that, the major relationship between traditional wireless scenarios and the implications design of the MAC protocol for many cores is also discussed. The analysis of Network on Chip highlights the reliability, latency, and variability of traffic.

Wu et al. [29] introduced a silicon photonic Network on Chip by mode division multiplexing. In this work the intra-chip for Mode Division Multiplexing (MDM) communication link employs improved oscillations along with double modes of waveguides. Here the dense wavelength link maintains the required Gbps mode multiplexed capacity. Here mode multiplexer, mode de-multiplexer, micro ring modulators at the transmitter integrated germanium on silicon photo detector, and multimode waveguide interconnect all consist of network components.

Frey et al. [30] utilize the runtime hardware to make solid NoC router design more efficient. Also, unauthorized access to a company is studied to avoid illegal entry. Performance regarding runtime hardware enhances the number of packets received in the range of 70.1% than other existing models. The HT manages the NoC packets in the destination address. Also, study regarding throughput surge and reduction in latency is done. Table 2.1 represents the comparison of existing works based on emerging trends in NoC design.

**Table 2.1: The comparison of Related Works based on Emerging Trends in NoC Design.**

<b>Authors Name</b>	<b>Features Used</b>	<b>Objectives</b>	<b>Merits</b>	<b>Demerits</b>
Monemi et al.[26]	Proposed ProNoC for validation of MCSoc (Many core SoC) projects.	Supports virtual channel, virtual network, low latency routing and different routing algorithms	As compared with CONNECT, ProNoC has low latency, lower area, max frequency.	Saturation in throughput is occurred.
Boyapati et al. [27]	Proposed APPROX-NoC hardware Data approximation framework with online data error control mechanism.	Approximate matching of data patterns reducing the volume of data movement across the chip	Achieves 9% latency reduction & 60% throughput improvement	Fails to connect large number of on chip components.
Abadal et al. [28]	Proposed MAC protocols for many core	Physical constraints and traffic parameters are analyzed	It highlights the reliability, latency & variability of	Affects system performance in wireless medium

	WNoC. Tiled Chip Multiprocessor (TCMP) concept is explained.	correctly	traffic.	
Wu et al.[29]	Proposed intra chip MDM (Mode Division Multiplexing) employing advanced modulation formats with two waveguide modes.	The intra-chip for Mode Division Multiplexing (MDM) communication link t employ the improved modulation formats with two waveguide modes.	Insertion loss for the two channels are less than 1.2 dB and the mode crosstalk between two channels are less than $-22.2\text{ dB}$	Noise performance of the system is not upto the mark.
Frey et al.[30]	Proposed a dynamic permutation and flit integrity check for HTs (Hardware	To avoid unauthorized system management and provide integrity of flits grouping	The number of received packets are improved by up-to 70.1% over other	It does not reduce the usage of excess amount of hardware in router design.

	Trojans)		methods.	
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## 2.2 Performance of Efficient Network on Chips

Zheng et al. [31] presented a scalable NoC design with efficient router framework by using power gating technique. In this work Easy Pass (EZ-pass) router is proposed with huge wake-up latency overheads as to ensure essential static power savings. In network, presented model increase the idle resources that interface with the router to transport packets without waking it up. In addition to that the wake-up latency is hidden by presented approach which are continued to provide a transmission of packet during the phase of wake-up. EZ-pass router evaluates the entire system simulation via 8x8 Mesh NoC including PARSEC tool. The result of presented model minimizes the static power by the range of 31% and the overall network latency to 32 %.

Louri et al. [32] proposed a reinforcement learning to design a energy efficient Network on Chip. In this work the reinforcement learning (RL) method are used to learn automatically the better control policy to enhance the energy efficiency of NoC design. Initially the DVFS (Dynamic Voltage and Frequency Scaling) as well as PG (Power Gating) is deployed to minimize power of the system. In addition to that Artificial Neural Network (ANN) is implemented along with RL. The result of proposed model provides a better power consumption up to 26 % to enhance the performance of system by 7 % which are better than combined PG and DVFS design without RL.

Schoeberl et al. [33] introduced a high performance NI with a revolutionary dynamic buffer allocation that improves resource consumption and overall on chip network performance, because the traditional reordering approaches do not make optimal use of resources consequently. To be compatible with current IP cores, the proposed design uses the AXI transaction based protocol. The suggested design outperforms the current architecture in terms of latency, according to experimental results using a simulated test

scenario. The micro architectures of the planned master and slave side NIs that are compatible with the AMBA AXI protocol have also been revealed. The suggested architectures efficiency was assessed using a cycle accurate simulator. The suggested designs showed reduced average communication delays than the baseline architecture in a uniform traffic scenario with a high traffic load.

It is a major problem to design power efficient NoCs for 3D SoCs that meet application performance requirements while adhering to 3D technological limits. To overcome this difficulty Murali et al. [34] addressed and a synthesis technique for developing power performance efficient 3D NoCs. Methods for determining the optimum topology, computing routes and placing NoCs components in each 3D layer are presented. We validate the methodologies using tests on a variety of actual SoC benchmarks as well as a comparison analysis of the resultant 3D NoC designs with 3D optimized mesh topologies. When compared to standard NoC designs, the NoCs developed using our synthesis process result in considerable internal energy reductions to 38% as well as latency reductions to 25%.

Right now, multi tasking systems waste a lot of resources in sending information via system interconnections. The situation becomes even worse when parameters like image recognition and machine learning exhibits on such systems. To overcome this Chen and Louri et.al [35] investigated application fault tolerance and provided an approximate communication model for NoC to improve power consumption and latency. Proposed system includes a quality check approach and data approximation mechanism. In comparison to previous approximate communication techniques our cycle accurate simulation using the Ax-Bench tool reduces the Latency and power as per proposed.

Zheng et al. [36] presented a advanced NoC by reducing power consumption in system. DVFS reduces power by using gating techniques. Here DVFS is integrated along with transistors and supply for improving performance. The presented Agile NoC design includes various framework modules along with DVFS and RL algorithms. The network connectivity is managed by the simple bypass to eliminate the frequency in waking off



routers. In which the network latency are reduced by optimized pipeline and Reinforcement Learning techniques.

Gupta et al. [37] proposed a Network on Chip micro architecture by using blended buffers. STT\_MRAM (Spin Transfer Torque Magneto-Resistive Random Access Memory) is used for ensuring an optimal solution with less leakage power. The result shows micro architecture enhances the average packet latency as 12.3 % which are better than SRAM based router and achieves less energy loss.

Wang et al.[38] suggests a power efficient network on chips by using the dynamic bypass approach. In this work the dynamic bypass approach are proposed which consists reservation techniques. The performance results of suggested method provides low hardware overhead as well as utilizes very low power up-to 22.2% as compared to other existing works based on NoCs.

Wang et al. [39] established an efficient on chip communication for multiple cores by a certain module for power savings. In this work the Intelligent NoC (IntelliNoC) design architecture are established and utilizes RL algorithm to for controlling complexity and efficiency in the design. Proposed structure utilizes the dynamic power off NoC component to avoid fatigue and overheating. The performance of established method enhance the energy efficiency by 67 % and mean-time-to-failure (MTTF) by 77 % which also reduce the area requirement by 25 % and end-to-end packet latency by 32 % of NoC design system.

Venkataraman et al. [40] introduced a Network on Chip design based on Ant Lion Optimized (ALO) buffer less routing in low power application design with specialized design. In this work the optimization algorithm used with beefless routing in chip design are proposed. This method is used in buffer less router to obtain very less power consumption. In which the power dissipation of ALO buffer-less method are computed with conventional topologies which are octagon, cliché and spin. Xilinx ISE design 14.5 are utilized for validating and designing the planned work which are compared with

hierarchical FTDR and fault-tolerant defection routing in terms of fault rate and throughput. ALO-based buffer less routing method achieves operational frequency with 0.413 mW power consumption. The comparison of Related Works based on Performance of Efficient Network on Chips is represented in Table 2.2.

**Table 2.2: The comparison of Related Works based on Performance of Efficient NoC**

<b>Author Name</b>	<b>Features Used</b>	<b>Objectives</b>	<b>Merits</b>	<b>Demerits</b>
Zheng et al.[31]	A scalable NoC design with power gating module as compared to conventional VC routers	EZ-pass router is proposed with huge wake-up latency overheads as to ensure essential static power savings.	Result minimizes static power by 31% & network latency by 32%	Does not reduce the deflection rate without minimizing the operating speed
Louri et al.[32]	An RL algorithm to design high performance NoC.	DVFS and PG is deployed to reduce power consumption in NoC routers.	Results shown in proposed model provides a better power consumption up to 26 % to enhance the performance of system by 7 %	Do not reduce power optimally.

Schoeberl et al. [33]	Advanced NI Architecture for Network on Chip	To promote memory parallelism and resource usage, on- chip NI design was developed	Network performance is improved via dynamic buffer allocation, which improves resource consumption.	In contrast to the baseline design, the alternative architectures exhibited shorter average communication latency.
Murali et al. [34]	Proposed power-performance efficient 3D NoCs.	Describes a synthesis method for developing 3D NoCs with high power efficiency using TSVs (Through Silicon Vias)	Reduction in power by 38% reduction in latency by 25%	TSV constraints of link data is not met also yields of 3D NoCs is not improved.
Chen Y et al. [35]	Proposed an approximate communication network to reduce power consumption, latency for NoCs	To reduce power and network latency by reducing packet size.	Reduction in size of packets to decrease power and delay by using control system mechanism.	Future NoC designs will require creative power and latency reduction strategies.

Zheng et al.[36]	An efficient Network on Chip module applying learning enabled energy savings in the system.	DVFS (The Dynamic Voltage and Frequency Scaling ) is used for reducing power consumption of the system	RL control policy detects traffic directions from NoC as well as decide power usage, frequency and voltage status at real time	Energy and performance efficient are not precise.
Gupta et al.[37]	Proposed STT-MRAM (Spin Transfer Torque Magneto resistive RAM) which provides improved solution having zero leakage power and high packet density.	To improve average packet latency, reduced power loss and area.	Enhance the average packet latency as 12.3% & 65% of power which are better than SRAM based router.	Static power reduces the performance penalty of the system.
Nikam et al. [38]	Proposed Dynamic (D-Bypass) approach to transfer packets	To reduce the shortcomings in related power gating approaches for performance	Packets can be transferred along their shortest routing paths	Does not provide an optimal reliability and energy

	through powered off routers in any hop counts and in any directions.	improvement of system.	in the system	efficiency
Wang et al. [39]	An authentic on chip medium of communications for multiple cores module is proposed for energy savings. Also Buffer-less NoC (BLESS) concept is elaborated.	The Intelligent NoC (IntelliNoC) and reinforcement learning are used to control the design complexity and optimize the performance of reliability, energy efficiency in a holistic manner.	Enhance the power consumption and MTTF (Mean Time to Failure) which reduces the area requirement by 27% as well as 33% reduction in latency	Does not provide an optimal reliability and energy efficiency.
Venkataraman et al. [40]	A NoC design based on Ant Lion Optimized (ALO) uses BLESS routing to improve performance	The power dissipation of ALO buffer-less method is computed with conventional topology	Achieves operational frequency with 0.413 mW power consumption.	Leakage of power reduces the system performance

## 2.3 Different Framework for Power Efficient NoC Design

Keutzer et al. [41] introduced a framework for enhancing the power savings in wireless NoC architecture. In this work the novel energy managing method are used for Wireless Network on Chip (WiNoC), which is used to enhance the efficiency of energy in wireless modules like radio kernel. Experimental results of introduced method provide 25 % of energy consumption for total communication to enhance system performance with reduced design area.

Mirhosseini et al. [42] proposes a CPU-GPU heterogeneous system by proposing a BiNoC (Bimodal NoC) module. Here the BiNoC system is proposed heterogeneous systems. BiNoC optimizes system performance with low hop count. The experimental result of proposed BiNoC enhances the performance of CPU and GPU by 34% to 57% as compared to other networks.

Yang et al. [43] suggested a real time artificial intelligence based on investigating Artificial Neural Network and NoC. Also proposed NAS (Neural Architecture Search) and NDS (NoC Design Search) to enhance rate of throughput and accuracy. In which the detecting and alleviate the timing performance of bottleneck to permit reliable exploration of NDS space. The experimental result of suggested method provides 42.99% of efficient throughput and also enhance the rate of accuracy as 1.58% but does not find any feasible solution.

Ramadevi et al. [44] establish an improvement in network on chips based on the machine learning methods for enhancing the energy and performance. In this work the 2.5D integrated microprocessor die, accelerator die, memory die and 2.5D silicon interposer of input/output is presented. By using the 2.5D integrated microprocessor it ensures accelerator with higher speed up in H.264 decoder and core memory with 4x storage capacity. The experimental result of established model achieves higher bandwidth surges energy efficiency. It also enhances significant performance in improvement of energy efficiency and throughput.

Varghese et al. [45] presented a 8x8 core NoC co-processor based on programming adaptive epiphany. In this work the epiphany architecture is proposed with less energy utilization for performance improvement using RISC using Mesh Topology. Performance of presented method enhances the communication data of performance by achieving the efficiency of power. It also relatively slows for external shared memory interface to detect the huge problem sizes.

Rajamanikkam et al. [46] proposed Boost-NoC architecture for gateway computing. The design of threshold ensures a promising approach to enhance efficiency of energy computing. In this work the performance bottleneck are analyzed by a conventional network on chips framework in several core of NTC system. To overcome the performance loss because of sub-optimal of NoC design, proposed module is useful. Boost-NoC provides efficient power consumption with multiple layer NoC modules. Proposed Boost NoC design enhances the performance of system as 2X over a conventional NTC system which also enhance the efficiency of energy by 104X with the use of drowsy routers.

Selvaraj et al. [47] proposed an expandable efficient NoC by introducing advanced buffer architecture. In this work the novel low power reconfigurable network on chip framework with repeaters between the routers are proposed. In which the repeater requires a zero buffer among the inter link routers which are worked based on the store process and forward process principles which are implemented in mesh network topology. The experimental result of presented framework lowers power consumption and chip area by 56% and 60% respectively. But the throughput is reduces by 3% as buffers are used in proposed module.

Catania et al. [48] suggested a cycle error free NoC module with Noxim. Based on NoC paradigm MPSoC are designed. NoC architecture does not provide a reliable performance on power consumption, reliability requirements based on multiple core architecture. Therefore in this work the Wireless Network on Chip (WiNoCs) is proposed for candidate solution to overcome the scalability limitation of traditional NoC design. Does

not provide a support for broadcast and multicast communication for multithread simulation for more sophisticated wireless communication system.

Ditomaso et al. [49] established an NoC module based on the tough as well as energy coherent multiple channel buffer. Here QORE are proposed for liability NoC design using MFC (Multiple Channel Buffer). This method detects the traffic flow direction to more efficiently reverse links to enhance the speedup by 1.3X and 2.3X throughput. Also do not optimize the network power with minimal control overhead.

Naik et al. [50] presented a heterogeneous circuit switched routers for building structured NoC design. Here CLOS module is also described to enhance power and area. The experimental analysis of presented model provides a CLOS switch network which improves the reduction by 32% of area energy by 25%. But for NoC diversified computing solution does not provide better energy efficiency to NoC design.

Chen et al. [51] suggested a CUDA module along with FPGA for well organized NoC design. In this work a customized network on chip framework are proposed with directory based data sharing mechanism with CUDA (Compute Unified Device Architecture) for providing a scalability which enhances throughput of system. Experimental results of suggested method provide an efficient and scalable system to enhance the execution time by 63X and minimize the external memory reads by 81% for single hardware code implementation.

The comparison of Related Works based on Different Framework for Power Efficient NoC Design is represented in Table 2.3 clearly. Also Table 2.4 represents Analysis of Power Reduction Techniques.



**Table 2.3: Comparison of Related Works based on Different Framework for Power Efficient NoC Design**

<b>Author Name</b>	<b>Method Used</b>	<b>Objectives</b>	<b>Advantage</b>	<b>Disadvantage</b>
Wu et al. [41]	Proposed a aggressive fine grained power gating of flit sized buffer entries by adopting back-pressure less flow control in an input-buffered network	To avoid packet truncation modification in packet injection architecture is performed	Design saves up to 59% network power consumption in both a fault free and faulty NoC	Do not assume MAC as well as its adaptation
Mirhosseini et al. [42]	Introduced BiNoCHS a reconfigurable voltage-scalable on-chip network for heterogeneous systems.	The performance of system is enhanced by CPU controlled lower traffic. Also the Bi-NoC is used to operate at low voltage and frequency	BiNoCHS improves CPU/GPU performance by 57% / 34% over a latency-optimized network under congested conditions	Does not provide a higher bandwidth in unloaded conditions.

		using low hop count.		
Yang et al. [43]	A real time artificial intelligence based on ANN module for NoC design	Proposed NAS (Neural Architecture Search) and NDS (NoC Design Search) to enhance rate of throughput and accuracy.	Result of suggested method provides 42.99% of efficient throughput and also enhance the rate of accuracy as 1.58%	Does not find any feasible solution for real time artificial intelligence.
Reddy BN et al. [44]	Proposed applied Machine Learning Techniques to predict energy consumption of mapped NoC	To perform better execution time and energy consumption simulation results	Achieves 80% & 75% accuracy for execution time and energy consumption.	Performance prediction can be less constructive for ongoing processors.
Varghese et al. [45]	A 8x8 core NoC co-processor based on programming adaptive	Proposed architecture utilizes less energy to improve the	Enhances the performance of system by achieving low power	It also relatively slows for external shared memory interface to

	epiphany. Also CHIPPER Router concepts is highlighted.	performance using RISC	consumption.	detect the huge problem sizes.
Rajamanikkam et al. [46]	A Boost-NoC power efficient network on chip architecture which used near threshold computing.	To overcome the performance loss due to the sub-optimal of NoC design, the Boost-NoC is proposed. Boost-NoC provides efficient power consumption with multiple layered NoC module.	The performance of proposed Boost NoC design enhances the performance of module as 2X over a conventional NTC system which also enhance the efficiency of energy by 104X with the use of drowsy routers.	Overhead occurred between layers which are accounted for performance evaluation.
Selvaraj et al. [47]	A novel low power reconfigurable	The repeater requires a zero buffer among	The experimental result of	But the throughput is reduces by 3%

	network on chip framework with repeaters between the routers are proposed	the inter link routers which are worked based on the store process and forward process principles which are implemented in mesh network topology.	presented framework lowers power consumption and chip area by 56% and 60% respectively	as buffers are used in proposed module.
Catania et al. [48]	A cycle error free NoC module with Noxim	The WiNoCs is proposed for candidate solution to overcome the scalability limitation of traditional multiple hop NoC module.	Based on NoC paradigm MPSoC are designed. NoC architecture does not provide a reliable performance on power consumption, reliability requirements based on multiple core	Does not provide a support for broadcast and multicast communication for multithread simulation for more sophisticated wireless communication system.

			architecture	
Ditomaso et al. [49]	Established an NoC module based on the tough as well as energy coherent multiple channel buffer.	Here QORE are proposed for liability NoC design using MFC (Multiple Channel Buffer).	Detects the traffic flow direction to more efficiently reverse links to enhance the speedup by 1.3x and 2.3x throughput.	Does not optimize the network power with minimal control overhead.
Naik et al. [50]	A heterogeneous circuit switched routers is proposed for an efficient NoC design.	Energy efficiency of NoC design is enhanced by using buffered along with buffer less routers.	The experimental analysis of presented model provide a CLOS switch network which improves the reduction by 32% in area and 26% reduction in power consumption.	But the network on chip communication for single chip heterogeneous computing solution does not provide better energy efficiency to NoC design.

Chen et al. [51]	Suggested a CUDA module along with FPGA (FCUDA) for well organized NoC design.  Compute Unified Device Architecture (CUDA)	Customized network on chip framework is proposed for CUDA to provide an improved and organized system.	Enhances the execution time by 63X and minimize the external memory reads by up to 81%	Does not provide system efficiency along with CUDA concept.
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**Table 2.4: Analysis of Power Reduction Techniques**

<b>Author Name</b>	<b>Power Saving Method</b>	<b>Energy Saved</b>
Boyapati et al. [27]	Low micro-architecture implementation of FP-VAXX method	Reduces dynamic power by 5.4%
Abdal et al. [28]	MAC protocols are used for many core WNoC	Calculated by source address & actual received power
Frey et al.[30]	Trojan Mitigation Methods	Dynamic power consumption is increased by 13.1% over baseline
Zheng et al. [31]	Power gating, IRR arbiter & UFDQ	Static power is reduced by 31%
Chen et.al. [35]	Simplified buffer & arbitration technique	Reduces overall power by 29.7% compared to smart NoC

## 2.4 Key Research Problems in NoC Design

Fully tailored topologies can increase overall network performance, but they damage the grid structure's regularity. It results in connections with wildly disparate lengths, efficiency and energy consumption are produced. As a result improved logical connection comes at the price of a penalty in the organized form of the wiring, which is one of the key advantages provided by standard on-chip networks. In the worst-case scenario completely customized solutions may resemble ASIC-style architectures in which individual modules interact via packet switching. As a result the standard issues of cross-talk, temporal closure, global wiring and so on may weaken the overall advantage

obtained by customization. Fortunately, these two extreme design points (i.e. designs based on strictly regular or completely customized topologies) is not the sole options for NoC router architectures. In reality, it is worth noting that many technical, biological, and social networks are neither entirely regular nor completely irregular. The typical problems that arise in NoC Design are Topology Synthesis Problem, Channel width problem, Buffer Size Problem, Routing and Switching Problem.

## **2.5 Research Objectives**

- Analysis of power reduction techniques using suitable topologies in router design.
- Design EZ-Pass Router Architecture to examine sporadic and low traffic modes.
- To improve system performance with enhanced wake-up latency, throughput and reduced design area.
- Implementation and validation of proposed architecture using Xilinx platform.

## **2.6 Summary of the Chapter**

This chapter provides a complete survey about Network on Chip (NoC) design by discussing about the different techniques used for with energy and performance efficient methods. Emerging trends used in network on chip design are used with different standard are also included in this chapter. Among these techniques the modern method provides a high efficiency with minimum delay and energy saving. But all the existing approaches have its own advantages that are not given by any other methods and disadvantages to design energy and power efficient network on chip.



## CHAPTER 3

### EFFICIENT 3D TOURS ROUTER FOR NETWORK ON CHIP (NOC) WITH DIFFERENT TOPOLOGIES

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#### Overview

NoC is an idea wherein big scale communication elements to extremely large scale infrastructures implemented on a single silicon chip. NoC is the greatest integrated option for high-end System on Chip designs. Reduced latency, increased bandwidth, low energy usage and scalability are some of the benefits of NoC with respect to specialized wire and buses. Researchers evaluate reductions in latency, energy usage, probability loss and speed of response while optimizing network-on-chip topologies. In the fields of multiprocessing chip architecture and elevated computation, NoC usage increases significantly. The system performance may be improved by reducing the use of superfluous hardware in router architecture without activating all settings. This study conducts a practical review of several routers that will be used in the future of networking. This chapter deals at the most common interconnection network technologies as well as some new topologies. Considering power savings, area efficiency and throughput improvement is studied in detail in this chapter. A brief comparison of previously constructed several routers as well as design factors for the 3D Torus router is produced in this chapter. Also examine their performance and to list of their advantages and disadvantages. NoCs are a popular communication channel for connecting several processors and memory modules on a single chip. NoCs utilize a bigger portion of the whole chip architecture, resulting in higher power costs. The issue comes when the transistor is scaled down.

### 3.1 Introduction

Networks-on-chip (NoCs) have supplanted the traditional SoC. It is a better approach for enabling communication between multi-core processors (SoC). The design of Topologies is extremely important in NoC. Throughput, rate of injection, minimum chip area, latency and hop counts are all parameters that increase performance of the network. NoC is essential for seamless and effective interaction between IPs (Intellectual Properties). On the basis of factors such as number of hops, latency, throughput and injection rates various topologies are created and classified. A comparative analysis of several topologies will be used to investigate some recent developments in NoC design. The NoC is a packet-switched on chip telecommunication service that connects multilayer techniques to packets routing.

Data is routed from the sender to the recipient PE through packets via a network fabric made up of switching and connecting connections. NoCs are an approach to start reducing large-scale network ideas. (SoCs) make use of sharing bus topologies [52]. A NoC era began when Dally and Towels advocated substituting specialized, design-specific cables with a general-purpose network. Developers study and create SoCs using network design technologies according to the NoC design methodology. Designers see a SoC as a micro-network of elements in other words. NoC is a communication capability on a chip that is distinct from computer activities. The topology of a network affects the latency and bandwidth by defining how nodes are linked and located. Because the routing method and flow management methods are significantly determined by the topology, selecting a topology of the network is the first stage in creating a network [53].

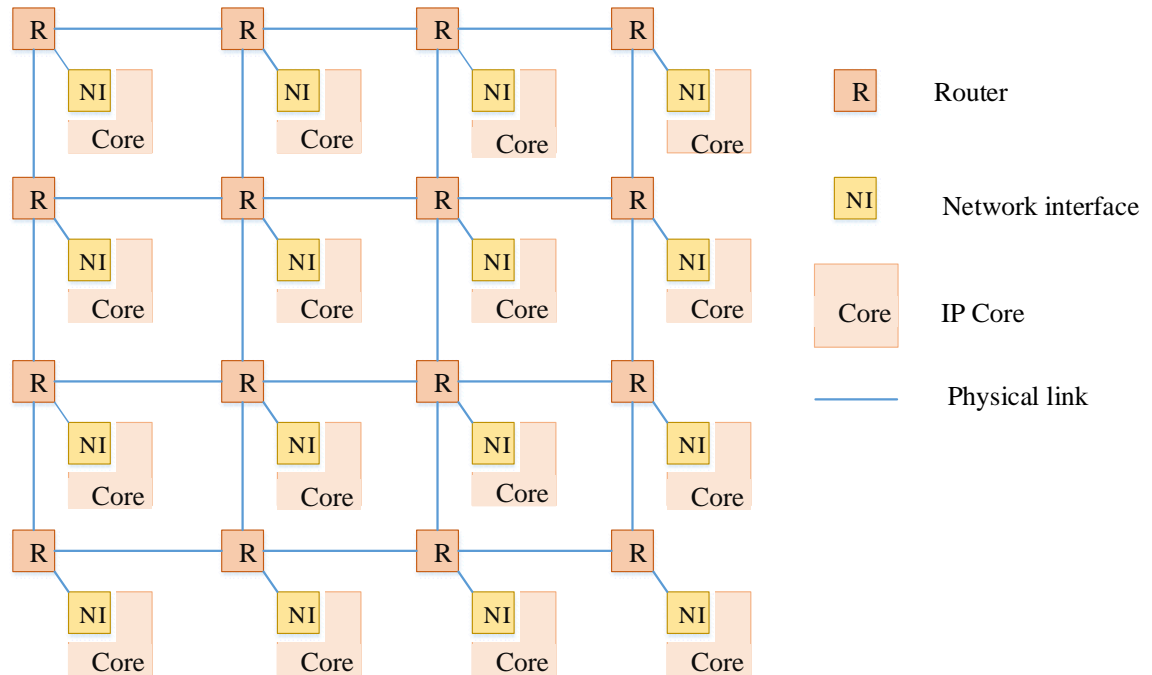
## **3.2 Performance Inspection of various Frameworks of NoC for different Topologies**

### **3.2.1 NoC (Network-on-Chip):**

Networking subsystems on an integrated circuit (often referred to as a "chip") generally among IP system core on chip is known as a network on chip (NoC). The structured NoC is shown in Figure 3.1. The NoC has the following fundamental properties:

- It distinguishes between communication and computation.
- For communication, it avoids the use of a worldwide centralized controller.
- Allows for an unlimited number of terminals.

Network interfaces, IP core, routers and connections make up the NoC. A network interface connects every core of NoC to a switch [54]. A network interface's job is to specify how data packets are prepared for transportation and routing. Data is sent through routers over multiple lines (hops). Switches are linked to gateways or any other switches through links. The NoC architecture consists of different topology such as Mesh, Tours, Ring, Star and Butterfly [55].

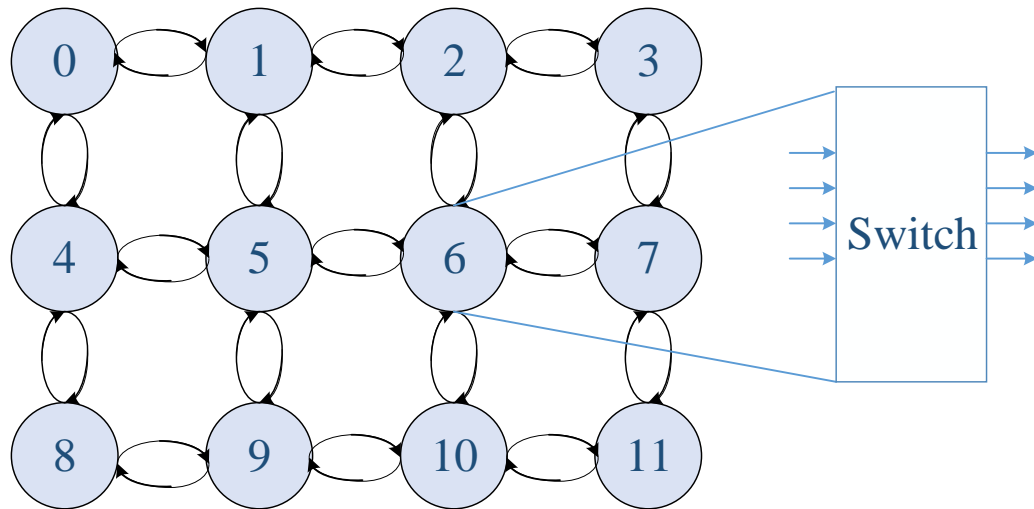


**Figure 3.1: Structure of NoC**

### 3.2.2 Topologies:

**Mesh topology:** It is among the basic topologies applied by scholars in NoC development. This is a sort of straight topology in which the nodes have direct connections. It delivers a high level of route variation while simultaneously ensuring scalability. Mesh topologies were originally developed for military uses, but they are now widely utilized in smart cities, remote monitoring and multimedia analysis. The data is shared throughout all nodes. It features many suppliers to target paths as well as an effective routing technique that prevents network disruption. All nodes are linked together in a 2D lattice [56] and nearby nodes are linked together as well. In Mesh architecture, inter-switch delays and network resilience may be avoided. The connectivity of different networking components (links, nodes and so on) is known as network topology (NT). The NT influences the design of NoC router design. The Mesh network topology is among the most often used network topologies. Because of its flat layout, it is one of the simplest topologies to build on a silicon chip. There are m columns and n rows

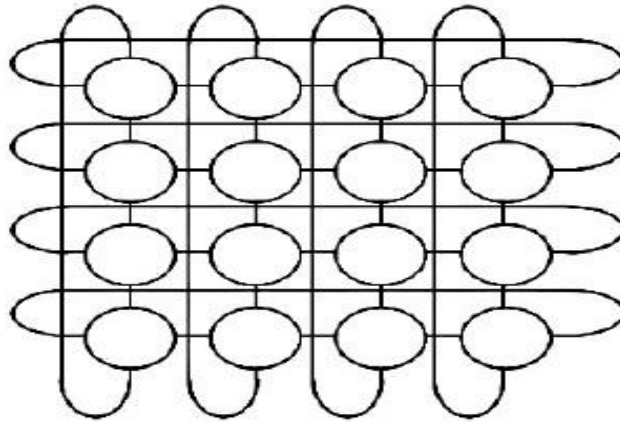
in a mesh-shaped system [57]. The computing resources are close to the routers, which are located at the intersection of two cables. Router and service addresses may be readily specified in mesh as x-y coordinates. Mesh topology is simple to build since all nodes are spaced evenly, as demonstrated in Figure 3.2.



**Figure 3.2: 2D Mesh topology in Network-on-Chip**

Because of its flat layout, it is among the simplest topologies to build on a silicon chip. The amount of node rows is  $R$ , and the amount of node columns is  $C$ , hence the mesh size is  $R \times C$ . Mesh is a regular topology, as are cube and hypercube.

**Tours topology:** Torus topology is a more advanced form of Mesh Topology. It is a straight topological instance. It varies from of Mesh topology in that each columns head links to the tails of the same columns and every row left most node links to the column's right end corner node. The key benefit of this topology is that it may increase path variety since its edge topology is symmetric, and has a very low hop count  $H$ . The major drawback of the architecture is that latency grows as the length of cable connecting nodes in both columns as well as rows increases [58]. Figure 3.3 indicates Tours topology.

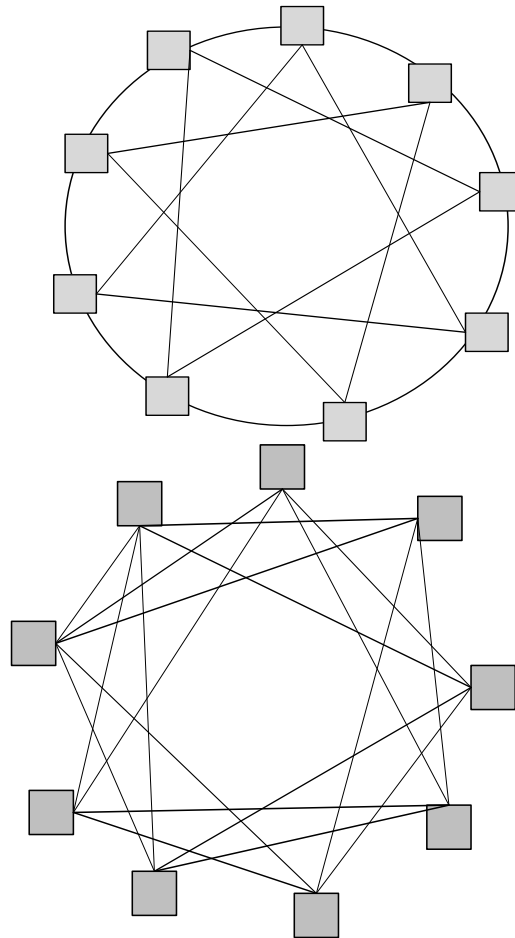


**Figure 3.3: Tours Topology**

The advantage such as Lower latency, reduced usage of energy, greater justice and higher speed because opposing edges are connected data has more alternatives for travelling from one node to another result in a significant boost in speed. The largest distance among nodes in a 4x4 mesh connection seems to be from upper left corner to bottom right corner. It takes 6 hops for each datum to make the journey the longest path. In a 4x4 Torus link, however the top left corner may go to the bottom right corner in just two hops. Data tends to transit fewer hops resulting in decreased energy use. Also have disadvantages like wiring complexity and expensive cost. Extra wires might complicate the routing procedure during the physical design phase. If we wish to lay down additional wires on a chip, we will either need to raise the amount of metal layers or lower the density on the chip, both of which are more expensive options. Otherwise the wires connecting the opposing edges might be significantly longer than other wires. Because of the RC delay, this disparity in connection lengths might cause issues.

**Ring topology:** A ring topology [59] network is one in which data is transferred between nodes through a circular channel. Ring Topology is a one way ring network, meaning flit moves in one position only. It is regarded as simplest topologies amongst all [60]. NoC based ring circulant topologies is illustrated in Figure 3.4. Because each node receives the same amount of bandwidth, the degree of each node in the Ring topology is two [61, 62].

The shortcomings of this design is that if single cable breaks, the entire network breaks down and as a result, network growth affects performance of the network.



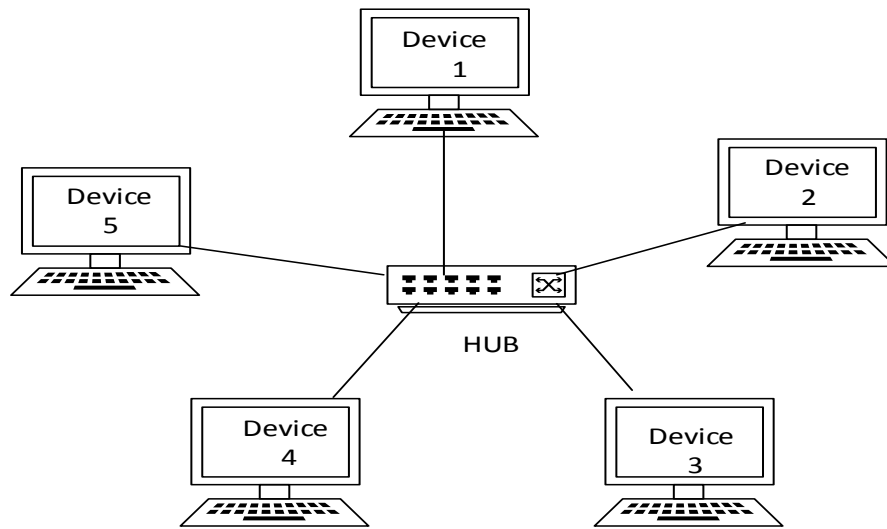
**Figure 3.4: Ring Circulant Topology**

Ring topology is network structure in which each node is connected to precisely two other nodes producing a single uninterrupted signal channel ring. Data is transferred from source to destination node, each node is handling one packet at a time [63].Rings can be either unidirectional (all traffic travels clockwise or counter clockwise) or bidirectional. Because a bidirectional ring network provides only one channel between any two nodes a single link failure can cause unidirectional ring networks to fail. A node loss or wire break might potentially isolate all nodes connected to the ring. Some ring networks respond by adding a C-Ring (Counter Rotating Ring) to provide inessential topology: A

well-organized network in which each equipment has accessibility to the tokens and the ability to send data. Given excessive network demand, it outperforms a bus topology. This does not need the use of a single point to handle computer communication. It is relatively straight forward to setup and modify since adding or subtracting a device only involves altering two connections, thanks to point to point line layout of equipment with a device on either side. It is simple for locating and isolating errors using a point-to-point line arrangement. The benefits of ring security rearrangement for line faults of bidirectional rings are that switching occurs at a high level, and so traffic does not require personal rerouting. Also it has disadvantages like a single failing machine might cause network-wide issues [64]. A dual ring or a button that closes the break can be used to alleviate this problem. Moving ahead adding and altering devices may all have an impact on the network. The amount of nodes in a network determines the communication latency. All links among devices share bandwidth.

***Star topology:*** In terms of building star topology is the simplest of all current topologies [65]. It is a Local Area Connection topology whereby each terminal is connected to the central location similar to a hub. In comparison to other typical topologies this design necessitates more wire. The fundamental disadvantage of this design is that if the main node fails the entire network would fail. The width of the center node rises as the amount of surrounding nodes connecting to it grows [66, 67].



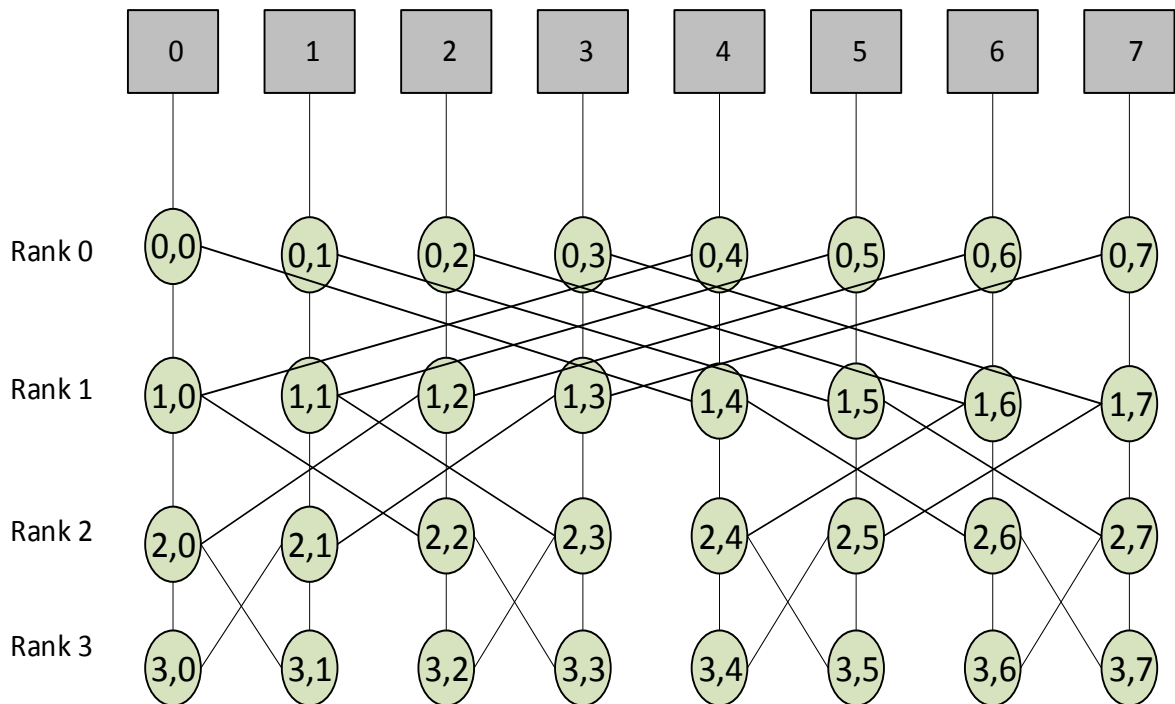


**Figure 3.5: Star Topology**

Figure 3.5 shows Star Topology. A network architecture in which each networking element is directly linked to a central node, including a router, hub or switch is known as a star topology. The center hub functions as a server, while the connected nodes function as clients in a star architecture. Whenever a packet arrives at the central node from a connected node, it can be sent to additional nodes in the network. A star network is another name for a star topology. The effect of a single point of loss is reduced. Every linking node in a star network is separated from the other connected nodes. If one connected node fails the network's remaining connected nodes will continue to function normally. Allows you to easily add and remove individual parts from a network. Because too many devices competing for access to the central node might degrade performance of the network, star networks are normally maintained modest.

**Butterfly topology:** This module connects a large number of computers to a network that operates at extremely fast speeds. The main elements of this topology are processing nodes, routers, and connections. Figure 3.6 illustrates the Butterfly network. The network parameters used in butterfly topology formulation and construction include bisection, band width, diameter and degree. The given butterfly network is a method of connecting several machines to form an elevated network. In a multiprocessor system, this type of

multiple stage interconnect network topology can be utilized to link different nodes. Unlike other network systems, such as local area networks (LANs) or the internet the interconnection network for just a distributed memory multi core processor should have high bandwidth and low latency for three reasons: Because the majority of communications are coherence standard queries and answers without data messages are brief, each read-miss or write-miss creates signals to every node in the system to guarantee coherence messages. Whenever the data is not in the processor's cache and must be acquired from memory or from another processor's cache, read/write misses occur.

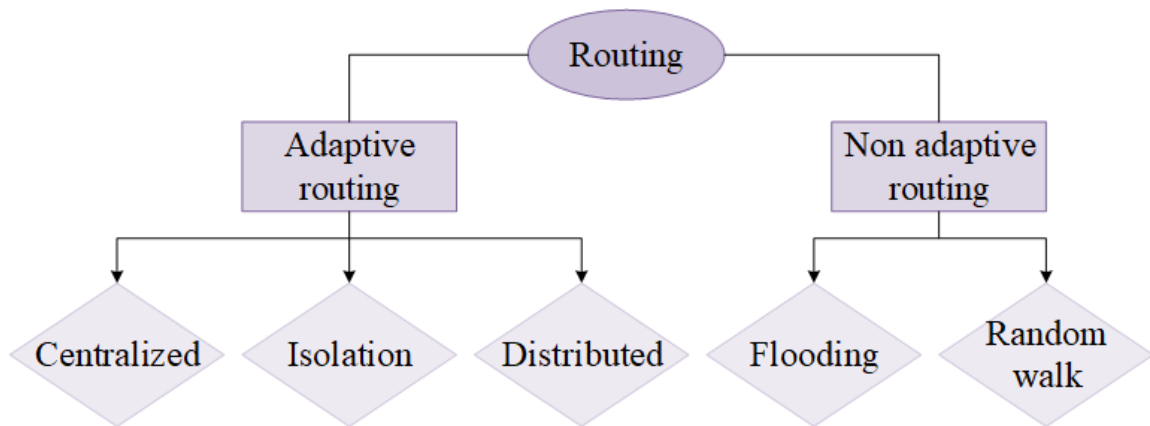


**Figure 3.6: Butterfly Network**

### 3.3 Various Routing Algorithms

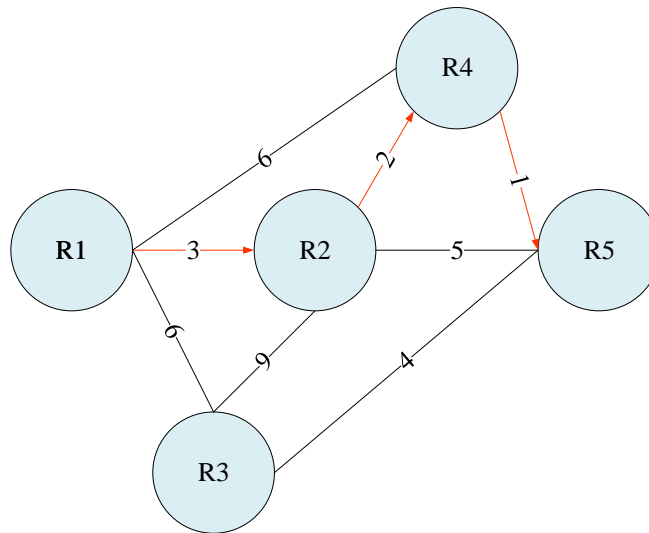
It is a mechanism for determining the path that flits will transfer from source to destination. They contribute in the effective routing of Internet traffic. After leaving its source, a data packet may choose from a number of paths to reach its destination. The

distinguished path or "least-cost path" through which packets can be transferred is calculated by the routing algorithm. There are different numbers of routing algorithms which are given below. Figure 3.7 denotes classification of Routing Algorithms.



**Figure 3.7: Routing Algorithm Classification**

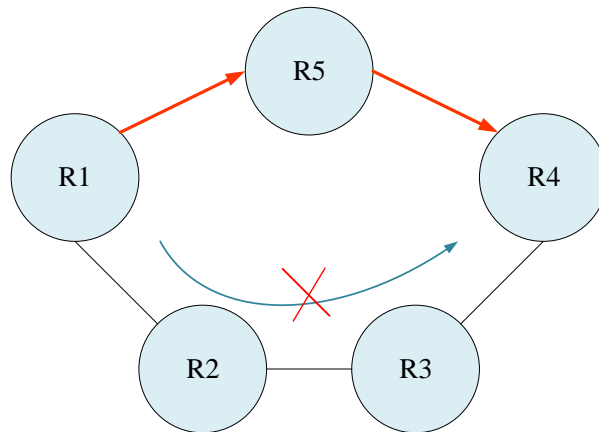
***Adaptive routing algorithm:*** It is generally called as variable routing algorithms. It forms routing decisions in real time based on network conditions. It generates the routing table depending on the network traffic and topology. They seek better route depending on number of transit time, distance and hops. Figure 3.8 demonstrates the Adaptive Routing Algorithm. Here the best route is taken by finding the minimum number of hopes.



**Figure 3.8: Adaptive Routing Algorithm**

- **Centralized:** It searches the global network for the shortest path among source and destination. Also called as the global routing algorithm.
- **Isolated:** This method derives routing information by using local information rather than information from other nodes.
- **Distributed:** This is a distributed, repeatedly computed decentralized method that finds cheapest way towards the goal.

**Non Adaptive Routing Algorithm:** It is often referred to as passive routing algorithms, build a stable routing table to determine which path packet should take. When network is powered up, the static routing table is built using the routing stored information in the routers. Figure 3.9 shows the representation of non-adaptive routing algorithm.



**Figure 3.9: Non Adaptive Routing Algorithm**

- **Flooding:** Whenever an information packet arrives at a router in flooding mode, it is transmitted to all outbound lines except the one on which it arrived. Uncontrolled, controlled or selective flooding are all possibilities.
- **Random walk:** This is a probabilistic mechanism in which the router sends a data packet to any of its neighbors at random.

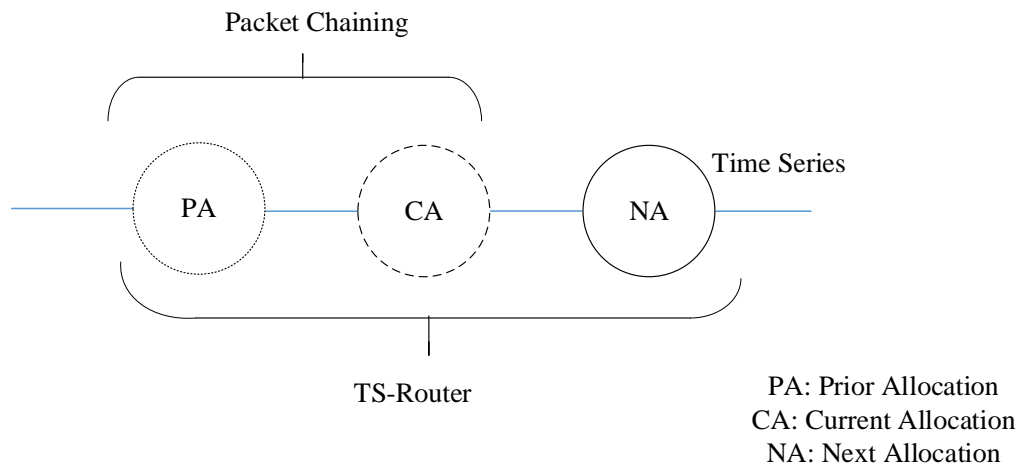
**Round Robin Algorithm:** Round Robin (RR) is a type of scheduling algorithm. In RR each cycle requires same time to process as compared to other cycles in the system. The period allotted is called as TQ (Time Quantum). RR uses the concept of Process Scheduling which monitors the process distributed to the CPU in an order such as to improve the target functions. RR is implemented to improve the system performance and fulfill Operating Systems requirements. RR algorithm can be implemented for better performance of multi-processor systems.

### **3.4 Flow Control**

At the Data Link Layer, flow control is a design concern. It is a mechanism that monitors the correct flow of information from the transmitter to the receiver. It is critical because the transmitter may communicate information and data at a high pace allowing the receiver to receive and digest the information. This can only happen if the receiver has a far higher traffic load than the sender, or if the recipient's computational power is lower than the sender. Flow control is a mechanism that allows two stations to interact with one another even though they are operating and processing at different rates [68,69]. Flow control is a collection of methods that informs the sender how much information or pictures they may move or broadcast before the recipient becomes overwhelmed. In addition the recipient has a limited quantity of velocity and storage for storing data. This is why before reaching a limit the receiver should be able to alert or inform the sender to temporarily halt data transmission or transfer. It also requires a buffer which is a huge block of memory dedicated to just keeping data or images until they are analyzed.

### **3.5 3D Torus Router Module for Structured NoC Design**

NoCs are popular communication channel for connecting several processors and memory modules on a single chip. NoCs utilize a bigger portion of the whole chip architecture resulting in higher power costs. The issue comes when the transistor is scaled down [70, 71]. In future power reduction measures will be critical in the design of NoC routers. The basic goal of a communication system is to transport data with the highest throughput and lowest latencies while utilizing the fewest resources possible. Switch Allocation is crucial stage in design of NoC [72] in which outputs ports are allocated to input ports immediately. Switch Allocation Strategy model is illustrated in Figure No.3.10

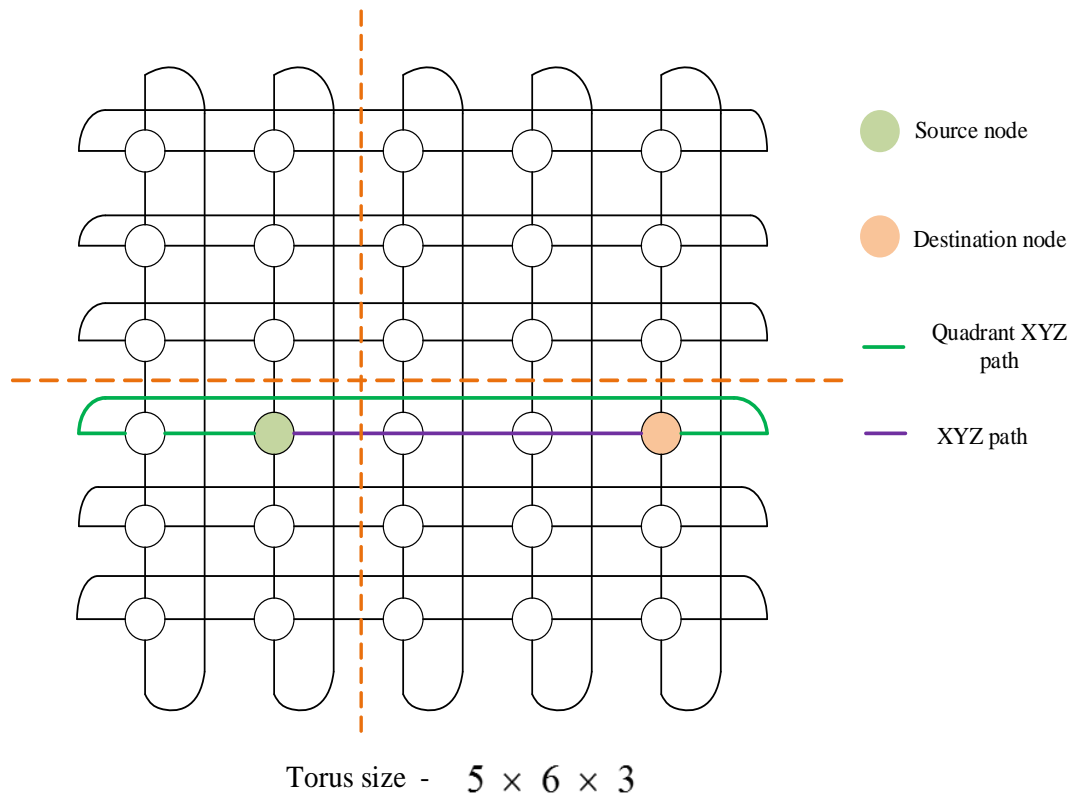


**Figure 3.10: Switch Allocation Strategy**

The NoC provides a flexible and scalable alternative to the System-on-Chip (SoC) instead of using the bus as a mode of transportation system with bandwidth restrictions and other issues using a lot of energy. However as you can see the number of cores on the chip grows and the chip become three-dimensional. Network-on-Chip (3D) is an appealing alternative for short vertical connector to replace the lengthy flat interconnect one that has the benefit of high throughput and low latency as well as minimal power consumption. Many benefits have been realized as a result of the 3D integration. Through-silicon Vias (TSV) can be used to link heterogeneous circuits stacked vertically the communication links are provided by TSVs between many levels. Due to the fact that the hair is so small, fine it provides minimal latency, less power as well as improved bandwidth over their networks [73,74]. TSV development has a massive price and it is a very complicated process with low yields and faults. Rather than employing TSV for all inter layer nodes, which incurs substantial cost and area overhead mixing of 2D as well as 3D routers with very less TSV which can be used. The physical architecture of the interconnection network is determined by the topology. Mesh, Torus, Ring and other topologies are the most frequent for both 2D and 3D NoCs. The graphic depicts the topology of 3D Mesh. The routing algorithm can have a major impact on the efficiency of 3D NoC. It results in designing best routing method for the particular topology is always difficult [75].

### 3.5.1 Router Architecture:

The credit-based traffic control approach is used in the router architecture. It entails the design of a proposed routing method that uses switching mechanisms to perform virtual cuts. The router is meant to execute a 3D Torus topology which is a novel topology. It has one port that is linked to the PE port and six other ports that are linked to other nodes [76,77]. The hardware characteristics of the 3D Torus are provided below in Figure No.3.11 which were implemented on a device such as the Xilinx Kinetic 7 and confirmed using the Xilinx tool [78].The various design parameters of router is illustrated in Table No.3.1



**Figure 3.11: Quadrant based 3D Torus Topology**

**Buffer:** Buffers are FIFO (First In, First Out) devices that store flits and packets when the output port is busy.



**Routing path controller:** It handles the way to push packets ahead in the allocated network and implements adaptive routing algorithm.

**Virtual channel controller:** It is in charge of any system-assigned deadlocks [79]. Adaptive routing algorithms guide VCs, which offer a fixed route for packets coming over numerous channels.

**Arbiter:** Both input and output connections are connected via Arbiter. It is put to test to see if it is fair. Basic arbiters include a variable priority arbiter, a round robin arbiter and a fixed concern arbiter [80].

**Allocator:** Its goal is to improve switching between input and output channels [81]. Allocator aids in the management of connectivity between both channels when a request is made through a certain channel [82].

**Table 3.1: Design Parameters of 3D Torus Router**

<b>Sr.No.</b>	<b>Parameter Considered</b>	<b>Design Value</b>
1	Switching Technique	Virtual Cut Through (VCT)
2	Number of Virtual Channels	3
3	Packet Width	2048 bits
4	Flow Control	Credit based
5	Link Width	256 bits
6	Design Algorithm	ARA

### **3.6 Summary of the Chapter**

This chapter illustrates about Performance Inspection of various Frameworks of NoC for different Topologies. Also 3D Torus Router Module for Structured NoC Design is discussed. Topology design is crucial in any NoC architecture. This section describes several topologies such as Mesh, Ring, Fat Tree, Folded Torus and so on. Traditional bus-based SoC struggle to scale as the network increases. We looked at numerous classic topologies and listed their benefits and drawbacks in this study. Average latency, throughput, injection rates, hop counts and other metrics are taken into account while building topology structures. In the literature review the categorization of various topologies is also briefly discussed. The recently examined topologies have still not been implemented to practice but they do provide prospects for study in the domain of NoC Router architecture. Different routing methods are offered in NOCs but only a small percentage of them are incorporated in the architecture design. The various routing methods are chosen based on the network activity and its state. Common algorithms in NoC Router design include the determinism method and the XY routing protocol. However there are only a few algorithms that are acceptable for the 3D Torus topology giving academics the opportunity to build a viable method for high processing. To minimize deadlocks and live locks in the system the 3D Torus router architecture employs Virtual Channel (VC) and virtual cut through (VCT) switching. In terms of LUTs the proposed Router architecture for 3D Torus is efficient.

## **CHAPTER-4**

### **RESULTS AND DISCUSSIONS BASED ON IRR AND UFDQ TECHNIQUES**

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#### **4.1 Overview**

Network-on-chips [83] provides an important router design on comparison with SoCs (System-on-chips). NoC provides the superior results to ad-hoc based and bus based designs since it offers cheap latency, low scalability and power over processing elements that are linked to a chip. When there is less traffic the advanced bypass path approach is employed to reduce packet arrival latency. On-chip design area occupancy also gets reduced to improve chip performance. In router design an Elastic Buffer (EB) control mechanism is utilized to eliminate the cost of buffer [84-86]. In such situations it is necessary to design a router with power efficient routing and discard buffer cost. More recently an Energy and Performance-Efficient Easy Pass (EZ-Pass) router has been proposed to handle sporadic, low traffic modes and high traffic mode using conventional router and EZ-Pass switch respectively.

Instead of employing a traditional router, the EZ Pass control logic uses a round robin (RoR) technique to route the flit to the NI. A traditional routers data channel consists of ports, crossbar switches, buffers whereas Control Unit is mostly made up of arbiters. With the use of the Virtual Channel technology the arbiter's structure becomes even more complicated. Arbiters are classified according to their fairness (weak, strong and FIFO). Every request is finally accepted by a weak fairness arbitrator. A strong fairness arbiters requests will be approved equally often. First Input First Output (FIFO) request of fairness is approved on early bird basis. The round robin arbiter is basic, straightforward and devoid of famine. When the number of input requests increases the Round Robin arbiter structure expands resulting in a larger chip size, large power utilization, and increased path latency. Addition to this quantity of MUX has been raised exponentially

while the size of the input port buffer has been increased in a traditional input port layout. As a result, the router's hardware overhead, critical path latency and power consumption have all increased dramatically.

To tackle this issue a low power NoC router architecture based on Easy Pass routing with Index based Round Robin arbiter (IRR) and Ultra-fast Dynamic Queues (UFDQ) is proposed in this system. The proposed circuit comprises of both traditional and EZ-pass switch to handle heavy traffic mode, sporadic and low traffic modes. This circuit power off routers by means of control block and the power gating mechanism when consecutive inactive time. The key points are listed as follows:

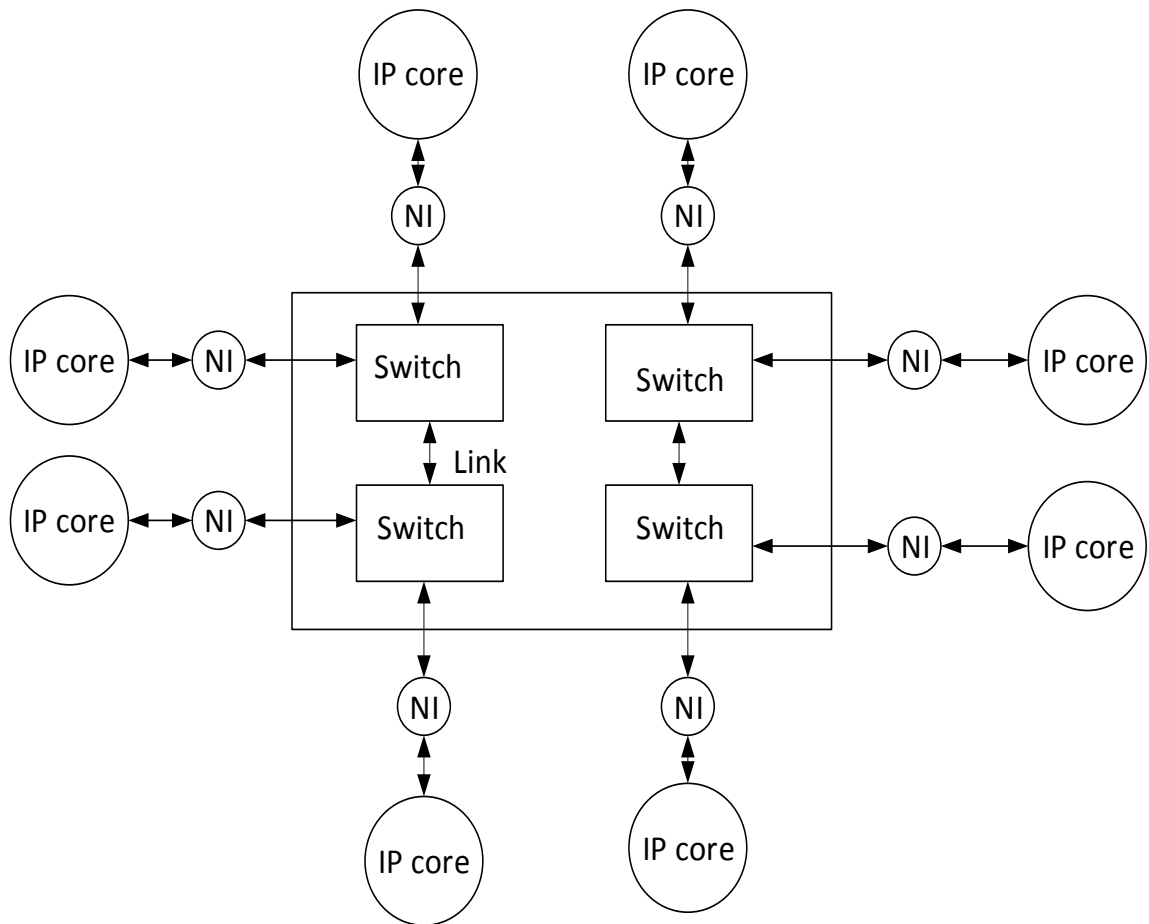
- Enhance the Easy pass routing and input port modules of the router design using IRR and UFDQ in a new NoC router architecture.
- To lower arbitration delay, energy consumption as well as chip area for EZ-pass router using IRR arbiter in the EZ Pass control logic to routes the flit towards NI.
- To reduce the latency at lower flit injection rates by modifying the input-port modules using UFDQ. This UFDQ generates dynamic flow control using a small Slot-State table for managing the structure of the input port buffer.
- To develop an optimal hardware structure for UFDQ to be used in NoC applications where latency is critical.
- To analyze the performance of the proposed router under various injection rates.

## **4.2 Communication in NoCs**

A Virtual Channel (VC) is a process of delivering data by means of packed-switched network that makes physical link between source and destination end systems of data. Virtual channel (VC) [87] is used in this system which helps in reducing the size of chip, latency, static and dynamic power [88]. Arbiter, routing path controller, allocator and buffers are some of the parameters that involve in the router design [89].

### 4.2.1 Communication Module:

To solve cache coherence issues the typical bus concept implementation needs to use the massive multiplexers. As a result bus-based communication is unsuitable for today's multiprocessor SoC architectures [90]. Hence NoCs are more suitable to overcome the complexities. Interconnection wire network between the cores plays an important role in overall performance of Chip Multiprocessors (CMPs) when there is surge in amount of cores. The goal of on chip router design is the reduction of buffers [91] in order to improve SoC portable space. To lower percentage in Latency, area control overheads can be used. The effect of low buffering also reduces router design latency by using a single cycle design.

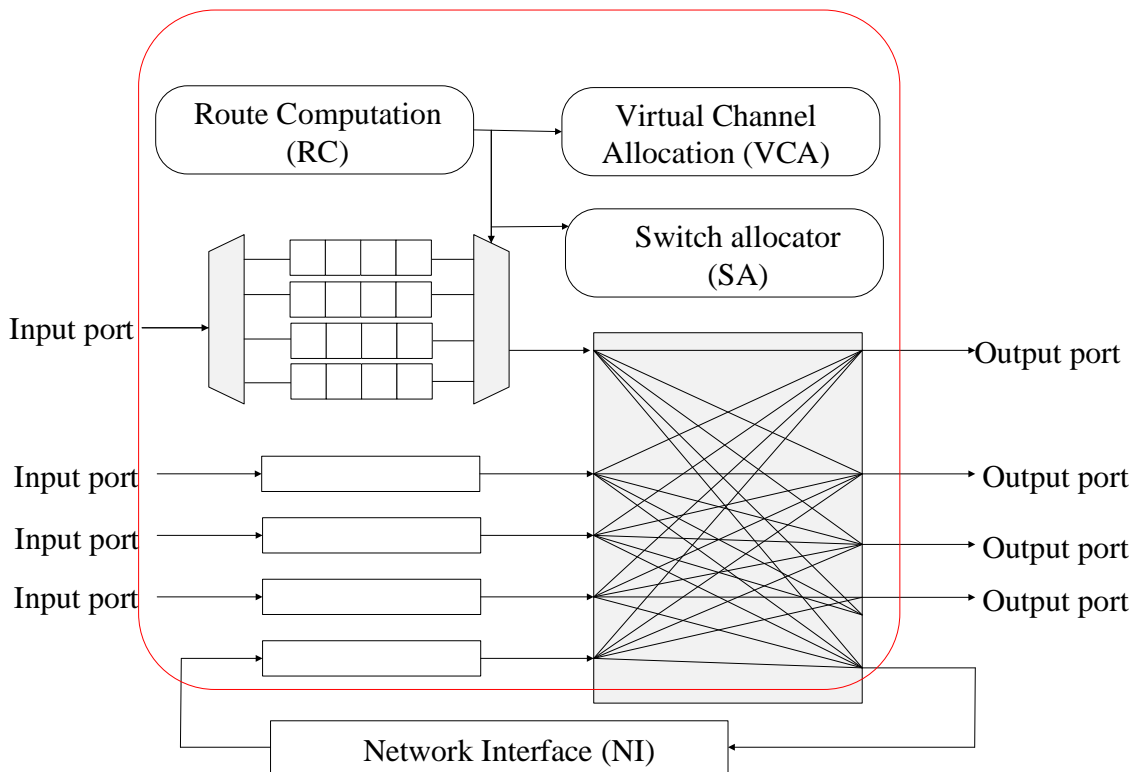


**Figure 4.1: Point to Point Communication in NoC**

In Figure 4.1 the architecture aims to use point to point channels in networks to overcome the difficulties of larger chip area design. As a result the system signal loss, power loss and latency are reduced. The Hierarchical Architectural Simulation Environment (HASE) is used to analyze the VC network model. Only the single cycle implementation of the router is considered in the overall simulation results. The results are computed for crossbar implementations that are unrestricted or restricted.

### 4.3 Virtual Channel NoC Router Architecture

The architecture of VC NoC is presented with 4 stages. Packet processing logic consists of VCs to store arriving packets, five input ports wormhole NoC router , VC allocation for flow control, wormhole routing, Routing computation (RC) for calculating packet route and SA (Switch Allocation) for the allocation of input port on to crossbar is indicated in Figure 4.2.



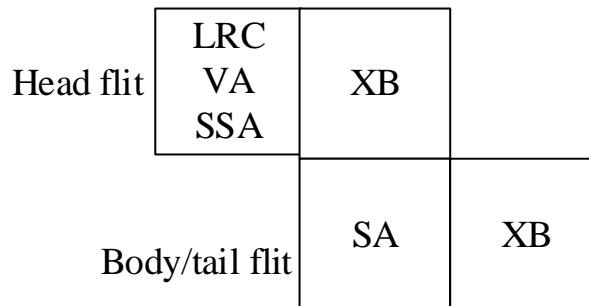
**Figure 4.2: VC NoC Router Architecture**

Here single packet is divided in-to numerous body flits, single header flit, single tail flit in wormhole routing. VA, SA, RC comprises of control logic reads & computes the header flit route information for routing and storing flits. Flit traverses in four stages: RC, SA, VA and ST (Switch Traversal). Furthermore Credit information is recorded into the VC state tables because wormhole routing is considered as the credit-based router.

Network Interface (NI) connects the router to high rise protocols [92] and it is in charge of sending, receiving and encapsulating the network. Prior research is proposed using the NI to speculative routing and implement source [93] in which Network Interface can perform VA and RC stages rather than respective router.

#### 4.3.1 Router Pipeline:

The router pipeline is depicted in Figure.4.3. A router makes use of pipeline optimizations such as Speculative Switch Allocation (SSA) and Look-ahead Routing Computation (LRC). Look ahead Routing determines a packet's route one hop in advance and eliminates the RC stage from the critical path. The Speculative Switch Allocation (SSA) allows VA and SA to occur concurrently. When speculation is correct, flit will proceed straightly to the XB pipeline stage. When speculation fails flit will have to go through SA again.



**Figure 4.3: Router Pipeline**

### **4.3.2 Components of Architecture:**

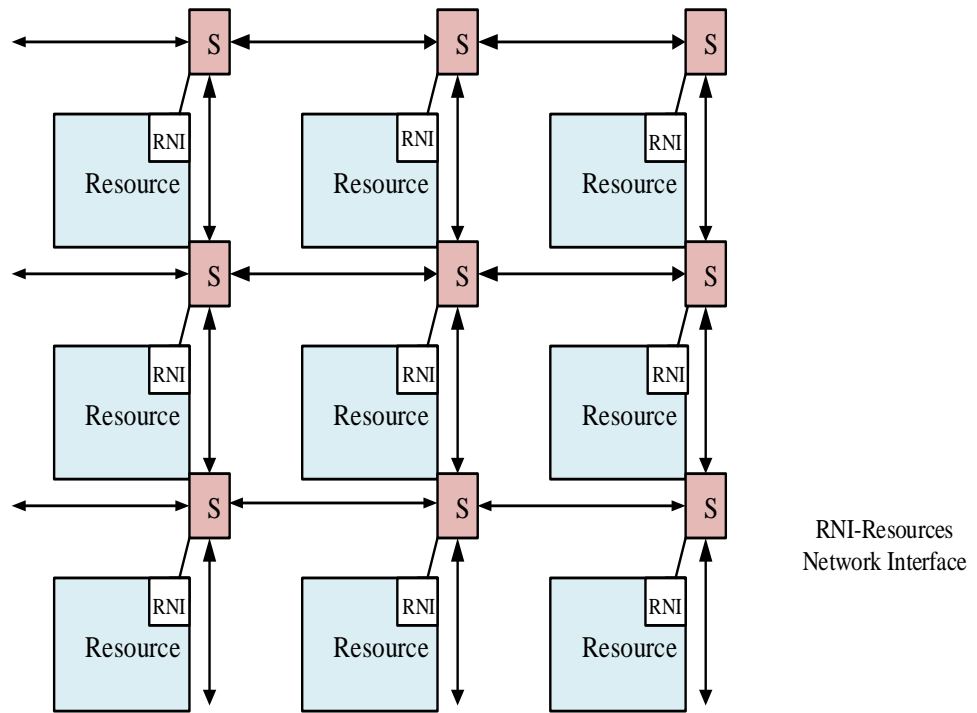
#### ***Input buffer***

Buffer is arranged as numerous fixed length queues in a NoC router. Each queue is referred as Virtual Channel. A physical channel is shared by all virtual channels. Every new incoming flits are placed inside VC buffer identified via VC identification.

#### ***Route Computation (RC)***

Routing Algorithm helps to construct low-power NOCs. Different routing algorithms consist of a significant effect on chip attributes including power, performance, area and temperature. A routing method influences router logic, buffer size, the number of links that are recorded along this way, the live lock of packets and probability of deadlock of packets. Each of these factors influences power, delay and chip temperature. Simple router logic on the other hand facilitates better VLSI design. Routing algorithms are classified into three types: Deterministic, Partially Adaptive and fully adaptive. In deterministic algorithms, just one route among source and a destination can be utilized.





**Figure 4.4 : 3x3 Network Topology with 9 resources and switches**

These algorithms frequently use simple routing logic and are simple to implement. There are multiple pathways between source as well as destination in fully Adaptive Routing Algorithms. When and how internal switches link their inputs to outputs, as well as the time at which message components is transported through these channels, are determined by switching strategies. We use the same technique for all routing algorithms when it comes to uniformity. Switching techniques are classified as Packet Switching, Circuit Switching and Wormhole Switching. 3x3 network topology with 9 resources and switches is illustrated in Figure 4.4.

Prior to data transmission, a concrete channel from source to destination is reserved in circuit switching. Path is kept open until all data has been sent. The network capacity is reserved for the period of the data is the main advantage of this method.

However, resources are also consumed for the data transmission period, and unnecessary delays occur when there is an end-to-end path. In packet switching data is broken into

fixed-length blocks known as packets and rather than establishing a path before transmitting data the source sends the data wherever it has a packet to send.

In these cases the buffer demand is considerable due to the necessity to store full packet switch in classical packet switching. In a SoC setting switches do not absorb a high proportion of silicon area when compared to IP blocks. The packets in wormhole switching are broken into the input and output buffers and fixed length flow control units (flits) are only looked for the few flits. In such case, the buffer space required in switches will be reduced in comparison to what is typically needed for packet switching. Switches will be small and compact if wormhole switching is used .A packet's initial flit or header flit contain routing information.

The switches define the path with header flit decoding, and following flits simply accompany this path in a pipeline form. So, each incoming message packet data flit is simply transmitted through same output channel as preceding flit data, with no packet reordering needed at destination. When flit encounters a busy channel, following flits also standby their existing positions.

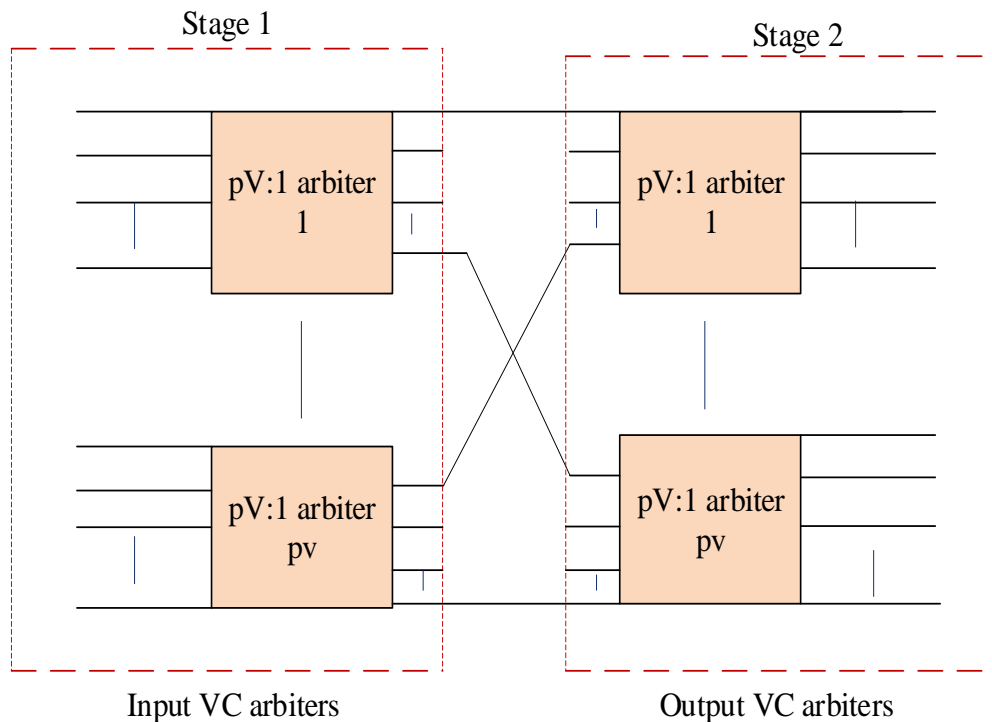
### ***Virtual channel allocation***

The channel buffer arrangement in NoC design supports the Virtual Channels (VC) usage for on chip communication. VC structure can be either dynamic or static. In a dynamic VC structure each VC can use a changeable number of buffer-slots based on traffic conditions in the NoC.

Buffer is a collection of Virtual Channels that is used to store outgoing or incoming packets. The way buffers are employed affects both power consumption and network throughput. They are primarily evaluated by the VC number, VC size and the manner in which they are allocated. A VC queue's size might be either dynamic or static. A static queue consists of a fixed size but a dynamic queue can contract and expand. Though dynamic queue size improves buffer efficiency use by allowing many flits to occur in the buffer it increases the difficulties of corresponding control circuitry. For instance the

DAMQ architecture managed dynamic queue size, resulting in significant delays in each flit arrival/departure by creating a linked list in hardware. Later systems are eliminated by using linked lists, although control logic still had a high cost. The ViChaR [94] design for example may allow VC sizes ranging from single flit to a whole packet yielding a high VC count as the entire size buffer in terms of flits ( $VC \text{ count} = \text{buffer size} / VC \text{ size}$ ). This needs  $f: 1$  arbiter in both switch allocation (SA) stages and VC allocation (VA) where  $f$  is size of buffer. The arbiter cardinality can generate bottleneck latency in the router critical path, limiting frequency of network. As a result, unless high-complexity logic is used for short cycle time, a static VC queue design is considered to contain a high-frequency router design.

In terms of VC allocation a VC can be statistically designated to traffic in one direction or dynamically assigned to any incoming\ outgoing traffic on-demand. Static allocation though less commonly used nowadays offers the advantage of providing equal opportunity for traffic to/from every direction to compete for the switch. Meanwhile, dynamic allocation can sustain burst traffic from a single direction as well as unequal traffic distribution across every direction. Each allocation technique has its own set of advantages is a notable one. A high-throughput router would benefit most from a design that incorporates characteristics from both methods.



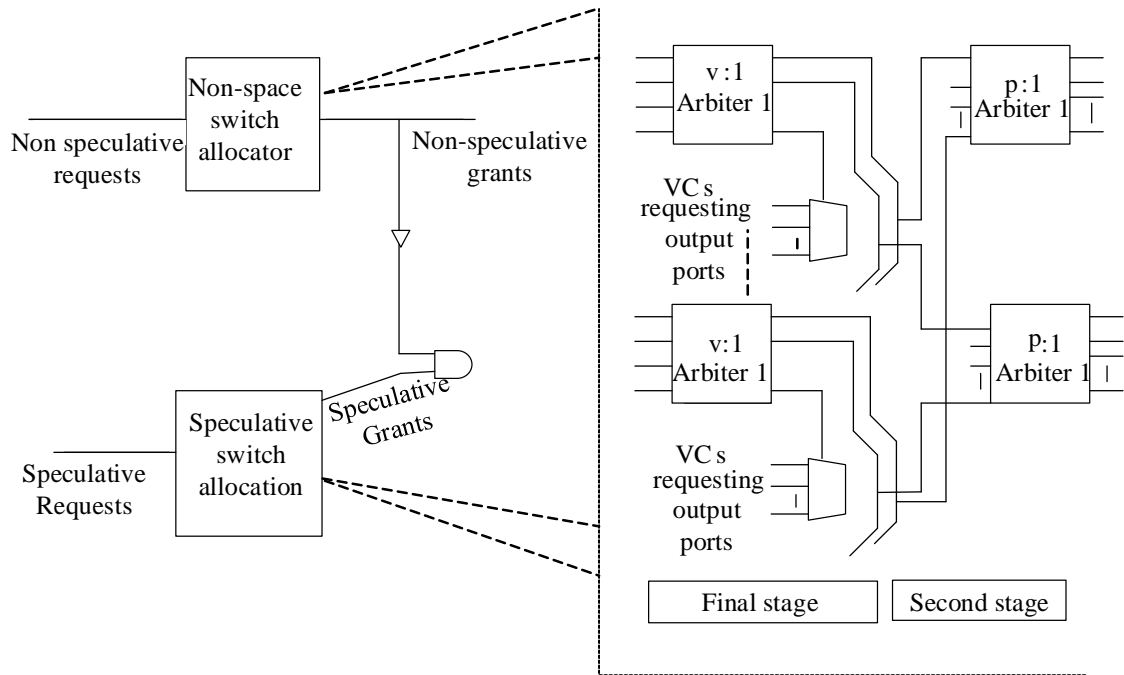
**Figure 4.5 : Virtual Channel Allocation**

In Figure 4.5 a new packet is assigned an unused virtual channel by the virtual channel allocation unit. It only works with the head flit. Above figure depicts figure of a router VCA unit. Initially each input VC with a head flit arbitrates for an empty VC in downstream router at this separable virtual channel allocator. In the second phase, head flits assigned to the same VC compete with one another at the downstream router.

***Switch allocation unit***

In next cycle, the switch allocation unit chooses that which VC input can transfer a flit through the crossbar from an input port. The Switch Allocation unit micro-architecture of a router is indicated in Figure.4.6. It clearly shows the implementation of two switch allocators. The first carries speculative requests, whereas second carries non-speculative requests. Non-speculative requests take precedence among speculative requests.

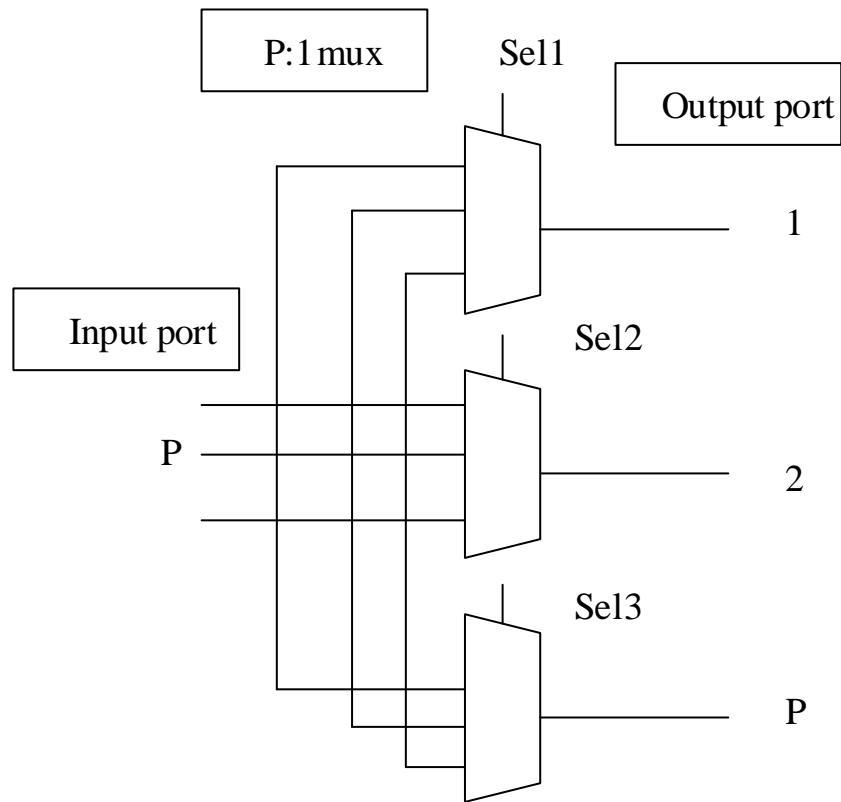
Separable switch allocator diagram is shown in the dotted box. First stage selects VC input via each input port. Second part chooses an output port.



**Figure 4.6: Switch Channel Allocation**

***Crossbar:***

The input and output ports are linked by the crossbar. The crossbar of a NoC router is seen in Figure.4.7 where P indicates number of ports. Every output port has its own MUX. Control signals are generated as a result of SA.

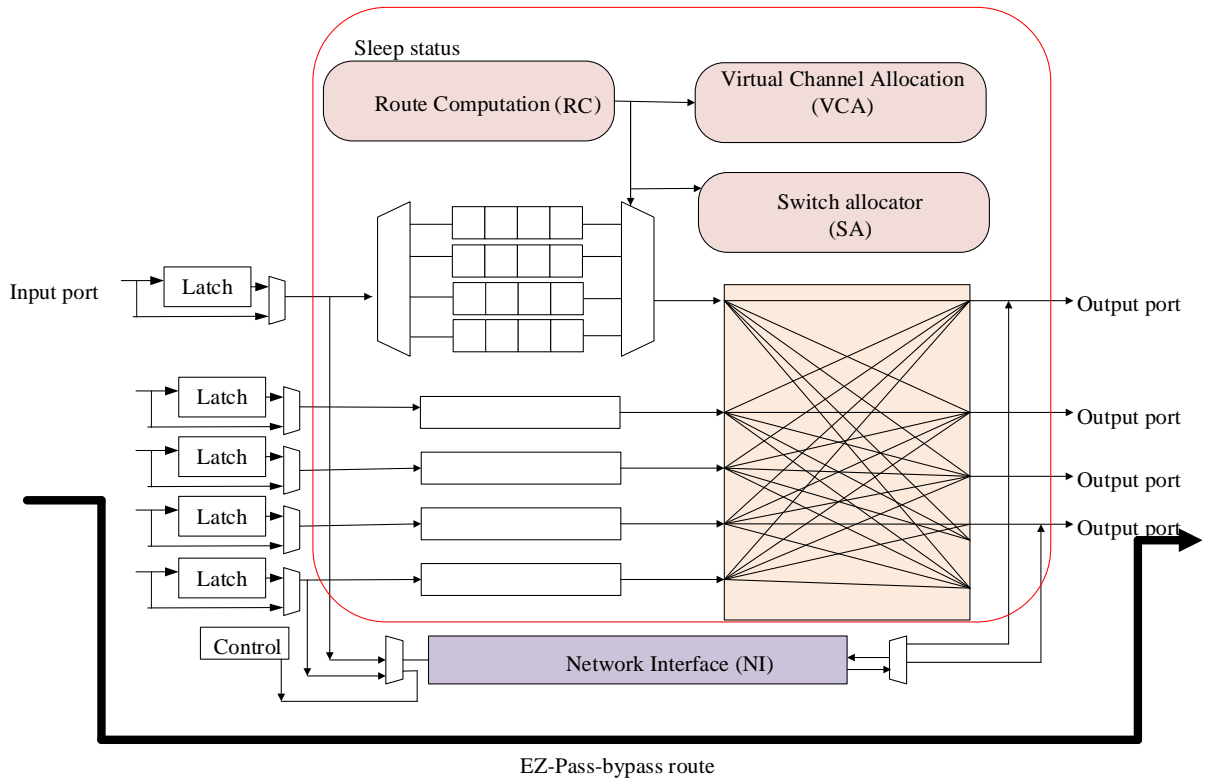


**Figure 4.7: Crossbar**

#### **4.4 EZ- Pass Architecture**

The EZ-pass router proposed design is indicated in Figure 4.8. It has EZ-Pass switch for low traffic modes and intermittent and conventional router for high traffic mode. Incoming flits are routed without waking up router network. Proposed switch which comprises of multiplexers (MUX) de-multiplexers (DEMUX) and single-flit latches represents bypass route [95]. Incoming flits are queued into the single-flit latch when router is turned off. Instead of using a conventional router, the EZ pass control logic directs the flit to the NI by means of an Index based Round Robin arbiter (IRR) [96] approach. The Network Interface interprets the input flit and routes to specified port accordingly as per available slots.

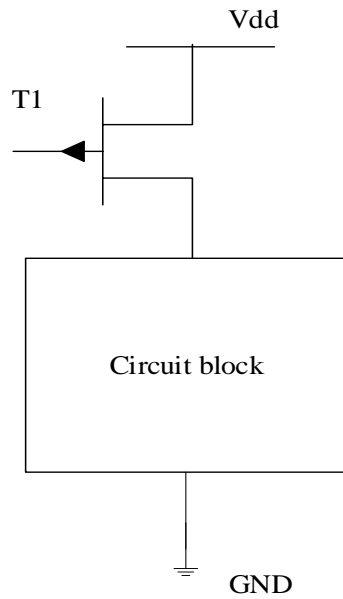
It can be noted that, EZ-Pass router consumes very less power as Static and Dynamic Power is reduced and produces better results when compared with conventional Virtual Channel (VC) router path.



**Figure 4.8: EZ-Pass Router Architecture**

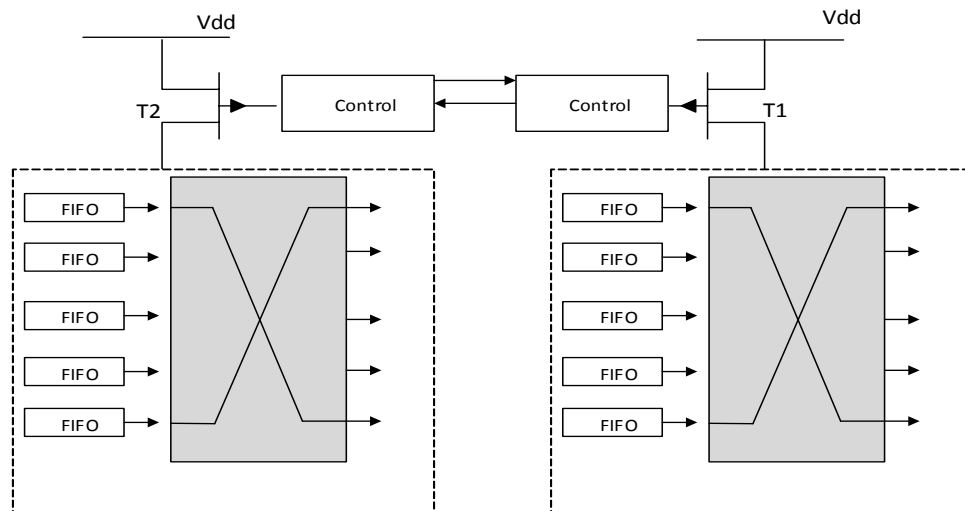
**4.4.1 Power gating of NoC routers:**

Figure 4.9 shows how to utilize Power Gating to turn off an idle block of circuit. Circuit block as shown in figure is monitored by T1 which acts as a switch. Circuit blocks are disconnected from power supply when the transistor is turned off. T1 can be connected in between the block circuit and Vdd or ground and circuit block.



**Figure 4.9: Power Gating Technique**

Figure 4.10 indicates how the power gating method is used in NoC routers. The figure represents two routers powered by two transistors and their related control blocks. The following terms will be used in the following sections.



**Figure 4.10: Usage of Power Gating technique in NoC routers**



- **Cycles between Consecutive flits (CBCF):**

CBCF is the number of cycles between two unrelated flits which arrives at given router.

- **Detection time (DT):**

This is the number of idle cycles identified by the router in a row. This number is used to determine whether or not to turn off the router. Micro architectural techniques for power gating of execution unit shows that DT has 4 cycles.

- **Break even time (BT):**

This is the less number of consecutive cycles that a router must remain in sleep mode to compensate for the energy penalty generated by turning off the switch transistor T2.

- **Beneficial power gating (BPG) state:**

BPG occurs when the number of Cycles between Consecutive Flits is higher than that of breakeven time and detection time.

$$\text{CBCF} > \text{DT} + \text{BT}$$

- **Unbeneficial Power-gating (UPG) state:**

UPG occurs when the number of cycles between consecutive flits is lower than that of breakeven time and the detection time which tends to create offsets the power gating benefits.

$$\text{CBCF} = < \text{DT} + \text{BT}$$

- **Wake up latency (WL):**

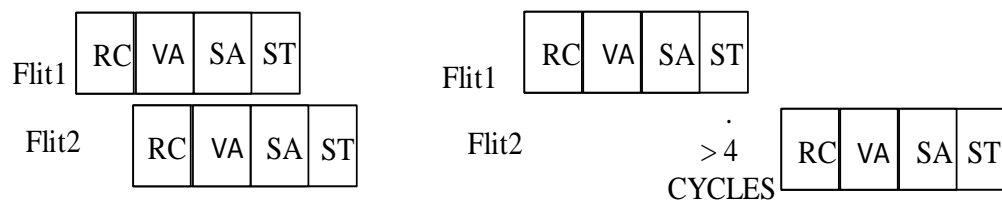
WL represents the number of cycles required for a sleepy router for (e.g. power-off) to continue the full activity (e.g. transitioning from powered-off to active).

NoRD: Node-router decoupling for effective power-gating of on-chip routers has shown that WL can be in 8 cycles.

The power gating saves the amount of energy when the router in number of cycles stays in the sleep mode. Hence router power gating is useful only if CBCF is at least as long as the detection time and the breakeven period or to a minimum of 14 cycles. As CBCF is the gap between the cycles of consecutive flits it provides an advantage for power gating techniques to avoid Static Loss in the system. The CBCF for large cycles is more than 14 cycles which is suitable only for low traffic mode and not suitable for high traffic mode.

The traffic behavior is focused on PARSEC [97] benchmark suites to fully grasp the power-gating benefits for NoCs. Traffic is classified into three groups depending on the number of cycles between consecutive flits (CBCF factor). The first group known as high traffic mode is made up of flits with CBCFs shorter than 4 cycles. The second group known as sporadic mode includes flits with CBCFs ranging from 4 to 14 cycles while the third known as low traffic mode and includes flits with CBCFs greater than 14 cycles. The heavy traffic mode is ineffective for powering down routers due to the four cycle power-gating detection time.

Figure 4.11 indicates Usage of router pipeline in traffic mode. The powered-off router is present in UPG mode when in sporadic mode when CBCF is less than DT and BT. Powered-off routers in low mode are in the BPG state because of high level CBCF than DT and BT.



**Figure 4.11: Usage of router pipeline in traffic mode**

#### 4.4.2 IBRR Arbiter:

This concept describes the Index based Round Robin (IBRR) arbiter, a new arbiter design that uses minimal served order scheme to provide robust and fair arbitration. In comparison to above mentioned arbiters the suggested arbiter has shorter arbitration

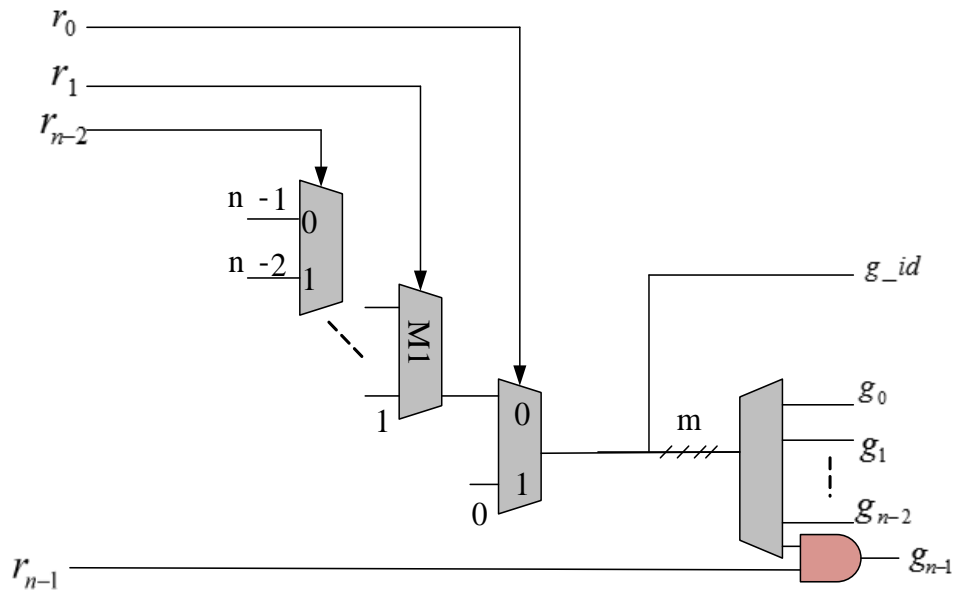
latency a smaller chip area and uses less power. An indivisible and crucial output in arbiter plan before explaining the IRR arbiter architecture is proposed.

### ***Grant Index:***

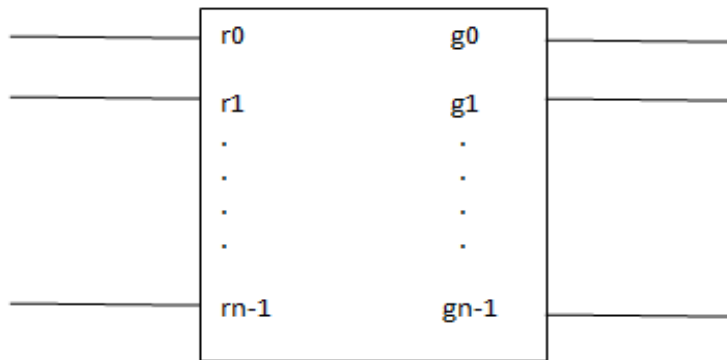
All arbiters have an output array which has the same width as the input array. However in actual designs, the grant signal index  $g\_ia$  in addition is created which marks the demand in various elements including memory, MUX and control tables in router design of NoC. The  $g\_id$  is connected to select terminal of MUX to route approved input to respective output terminal as router crossbar is made up of MUX and it is given in Figure 4.12 (a). The breadth of  $g\_id$  is equal to  $\log 2$  of permitted diameter. In this case utilize  $g\_id$  as first output of proposed design, as  $g\_id$  has a smaller width than other arbiters, our arbiter is smaller and quicker. As  $g\_id$  is so important in router design we shall study every arbiter to re-produce grant as well as  $g\_id$  both at output terminals.

### ***Fixed priority arbiter:***

The preference of requesters remains unaltered in priority arbiter. So if the high priority requester makes another request it will be serviced before the low priority requester previous request. This process is repeated until there are no more requests. The simple priority arbiter is a typical arbitration technique. A fixed priority is allocated to each request and the grant is delivered to the active requester with the greatest priority. For example if the request vector entering the arbiter is req [N-1:0] the highest priority is usually req [0]. Fixed priority is quite simple and more cost effective it is indicated as Figure 4.13 Requests are prioritized linearly and in ascending order in which  $r_0$  contains the top supremacy. Initial submitted request index to be transferred to the output terminal  $g\_ia$ . After this, grant signals are generated by decoding  $g\_id$ . In the last request,  $r_{n-1}$  contains simplified circuit and it is carried out by AND gate by means of  $g_{n-1}$  instead of multiplexed like other requests. Hence if  $r_{n-1}$  is higher then  $g_{n-1}$  also becomes higher. The block diagram of a simple Arbiter is shown in Figure 4.12 (b).



(a) n-input Fixed Priority Arbiter

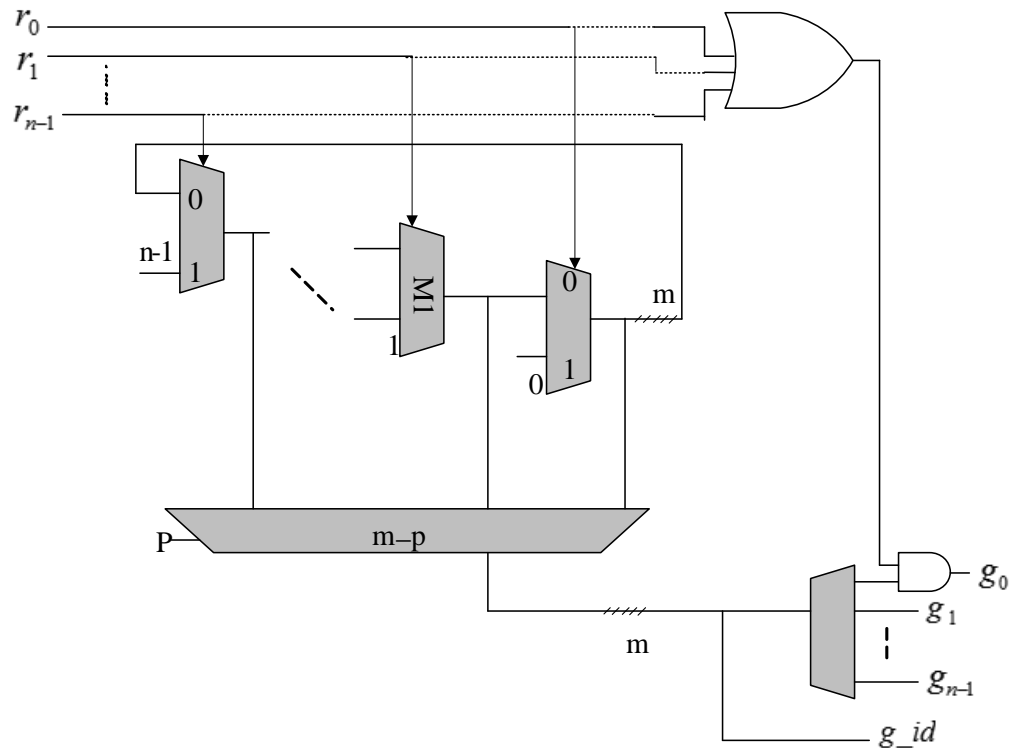


(b) Block diagram of Arbiter

Figure 4.12: (a) n-input Fixed Priority Arbiter (b) Block diagram of Arbiter

***Variable priority arbiter:***

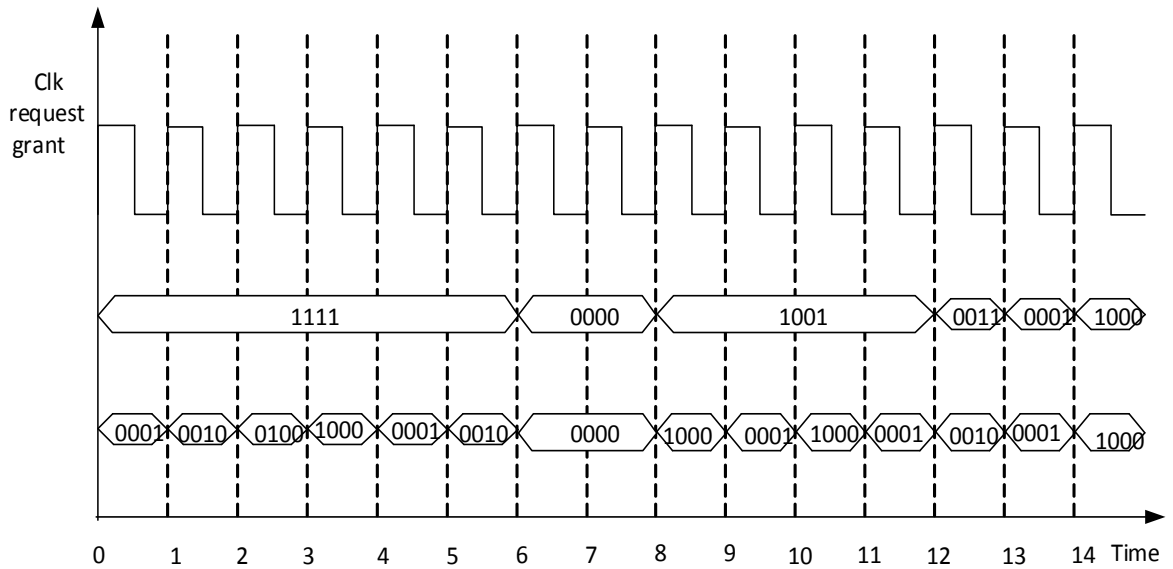
Oblivious arbiters and round robin arbiters are two types of variables priority arbiters. The generated priority in oblivious arbiters is not based on the last grant, but rather on the last cycle priority. As a result, basic circuits like shifters are employed to create the next priority although oblivious arbiters provide a limited level of fairness. Round robin arbiters provide fairness by giving the least important requester the lowest priority. As a result the priority vector that is created is a shifted version of the grant vector. Though  $g\_id$  terminal shown in Figure 4.13 where fixed supremacy arbiter is linked to the last multiplexer, each request acts in such a way that it resumes peak priority via arise loop order. For instance MUX, M1, output generates an index with  $r_1$  consists of the highest priority followed by  $r_2, r_3, and r_0$  for four requests  $r_1, r_2, r_3, and r_0$ . As a result after multiplying the outputs, we shall able to select one input as peak rank appeal as indicated in Figure 4.14 indicates Input request framework for strong fairness RoR arbiters. If no request is made or  $r_0$  is claimed, the  $g\_id$  returns similar digit which is zero. Variations in both conditions, any  $r$  is carried out using AND gate with  $g_0$  such as when all appeals is zero, every permit is also zero. Figure 4.15 indicates Input request framework for weak fairness RoR arbiter.



**Figure 4.13: n-input varying Priority Arbiter**

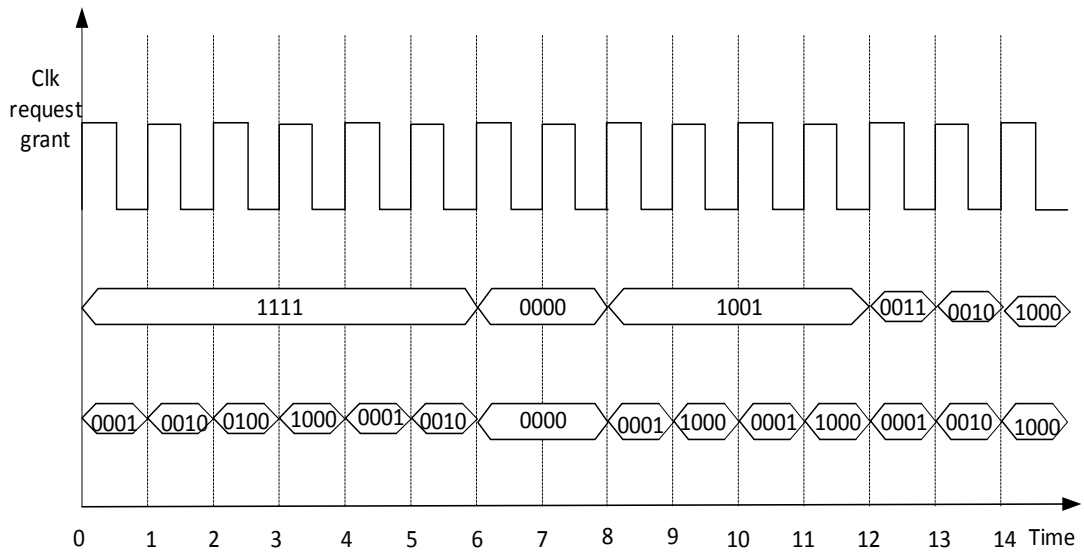
***IRR arbiter:***

IRR arbiter which uses an index structure for input ports to decrease power consumption and circuit latency. If upcoming indication of a permitted plea is selected for later level selection, the present grant request is given least priority as well as following plea is given peak priority amongst the total input requests. Next step,  $g\_ia$  array is to be saved inside the register and the register's output efficiency is increased which is to be connected at multiplexer's select terminal and MP which is indicated in above figure.

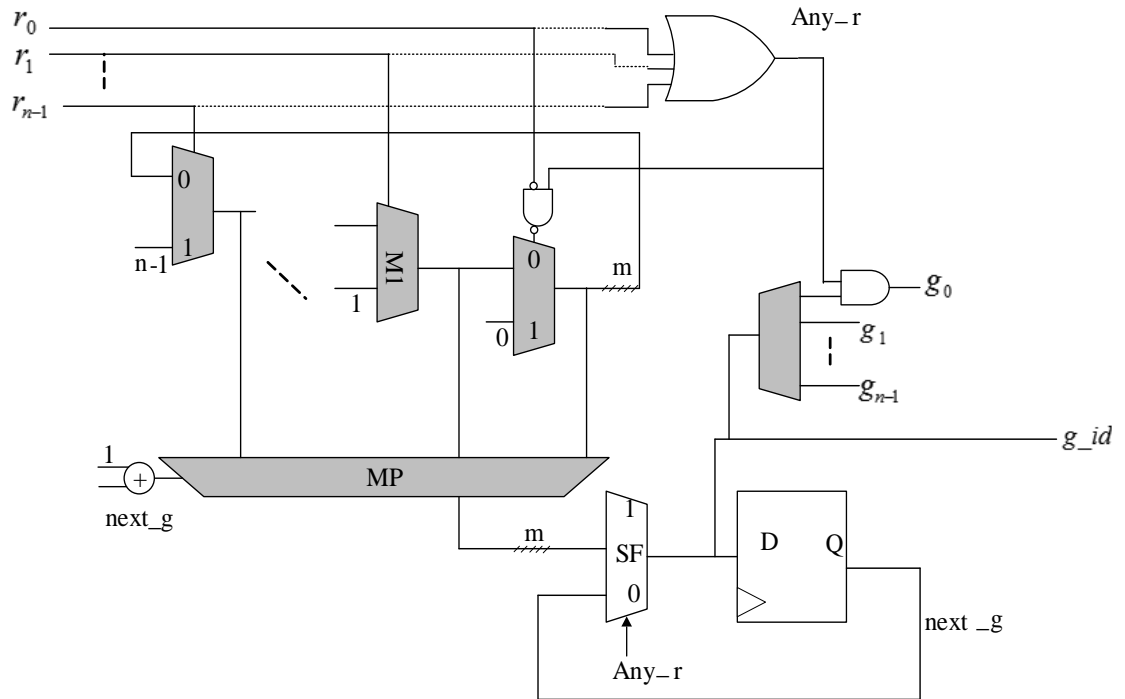


**Figure 4.14: Input request framework for strong fairness RoR arbiters**

The arbiter accompanies lower of late provided priority system or RoR method in this manner. Figure 4.16 indicates the advanced Index-based Round-Robin arbiter which requires only single clock cycle to arbitrate. For maintaining peak request, output of the highest peak registers next\_g is packed backward via SF MUX towards register for handling no requests. It ensures strong fairness arbitration in this design.



**Figure 4.15: Input request framework for weak fairness RoR arbiters**



**Figure 4.16: IRR n- input arbiter**



### ***IRR arbiter functional behavior:***

Figure 4.16 represents IRR n- input arbiter. Throughout time 1-6 a secure input request 1111 is concerned as well as considering each bits each clock tick is granted. Plea is changed to 0000 at time 6 indicating that there is no assertion of no request. When there is no request the procedure of the most recently permitted plea is applied as well as recorded as novel plea is claimed. Since the second bit priority request is logged during time 6 and used at time 8. As a result the fourth request is granted at time 8. Using the request scenario and same test bench, arbiter is tested with some existing arbiter (IPRRA, RoR, PRRA, Matrix, and HDRA). The RoR, IRR and Matrix arbiters record the current priority when no request is inserted. However the IPRRA, PRRA and HDRA are unable to take down the priority and display the various waveforms. The request low significant bit is given the highest priority when there is no request condition for IPRRA, HDRA and PRRA waveforms. Arbitration conduct of HDRA, PRRA and IPRRA occurs because of the absence of loop for handling null request. Superiority using this arbiter occurs as it provides more equity in arbitration.

### ***Simple Incrementing Hardware:***

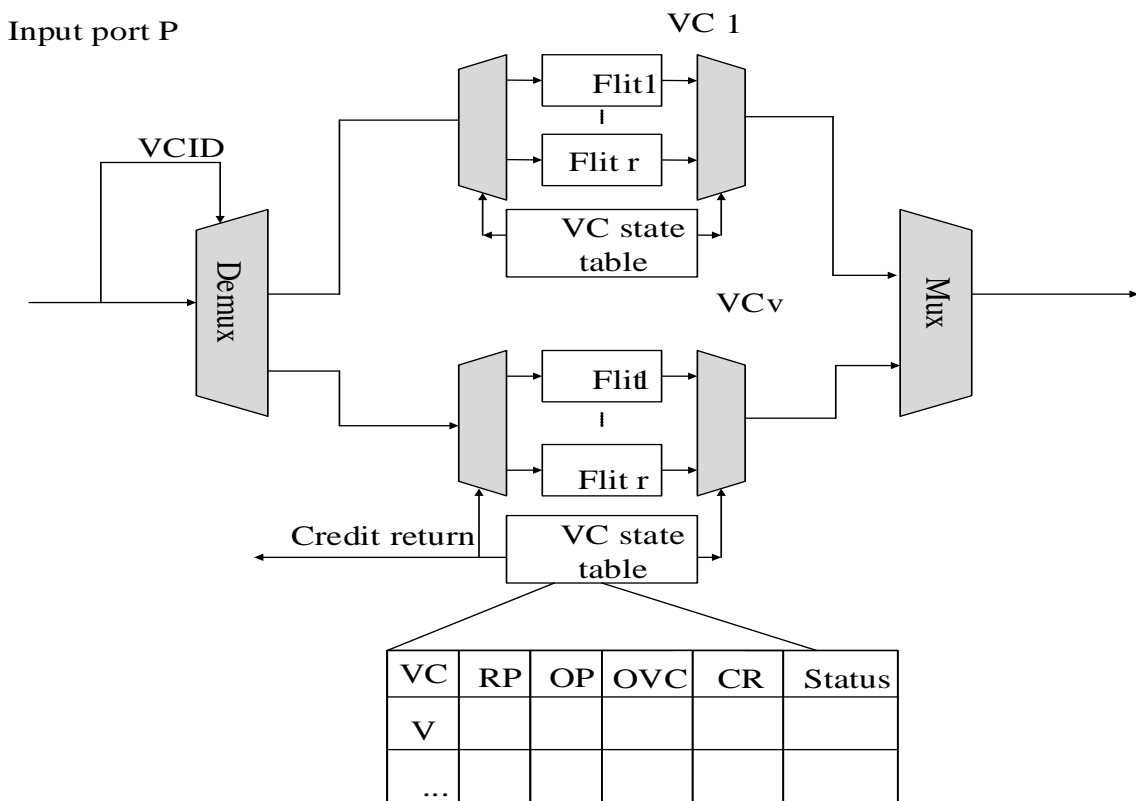
In IRR architecture the adder performs an incrementing operation which can be built in a basic manner. To increment an n-bit operand, n complete adder cells can be linked in serial form and feed 1 to the first cell's carry input and zero as the second operand. We can use half adders rather than complete adders because the second operand has a zero value.

### **4.4.3 Flow Control:**

A flow control policy is required in wormhole routing to regulate communication between routers. Figure 4.17 depicts a Conventional pipelined router for wormhole routing, with a VC stable table connected with each input port. The Output VC (OVC), Read pointer (RP), Output port (OP), credits (CR) and status are all maintained in the VC

state table. However, when we use power-gating to switch off a router, the VC state table is inaccessible affecting the flow control mechanism.

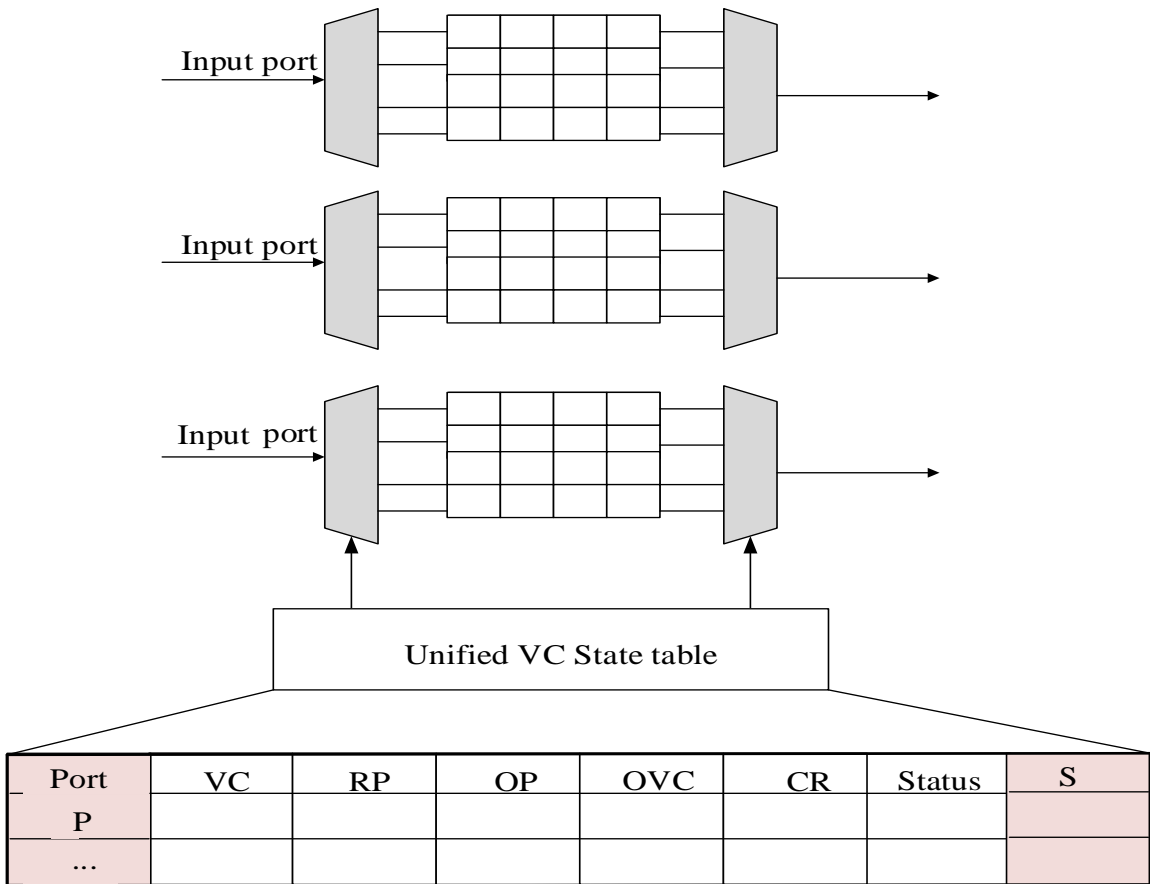
To enable flow management for the developed EZ-Pass router design and to make the VC state table information available during the power-off state we modify the information of VC state by consolidating all VC state tables into a unified table as shown in Figure 4.18 and relocating this information to NI. The unified VC state database is now accessible to both NI and the router. The NI can still access the unified VC status table for flow control even if the router is switched off. As a result, two additional items are added to the unified table: (1) the downstream router status (S) and (2) the input port number (Port).



**Figure 4.17: Conventional Virtual Channels**

The input port associated with the incoming flit is indicated in the input port number. Hence the routing information can be easily identified by the router and NI. The power

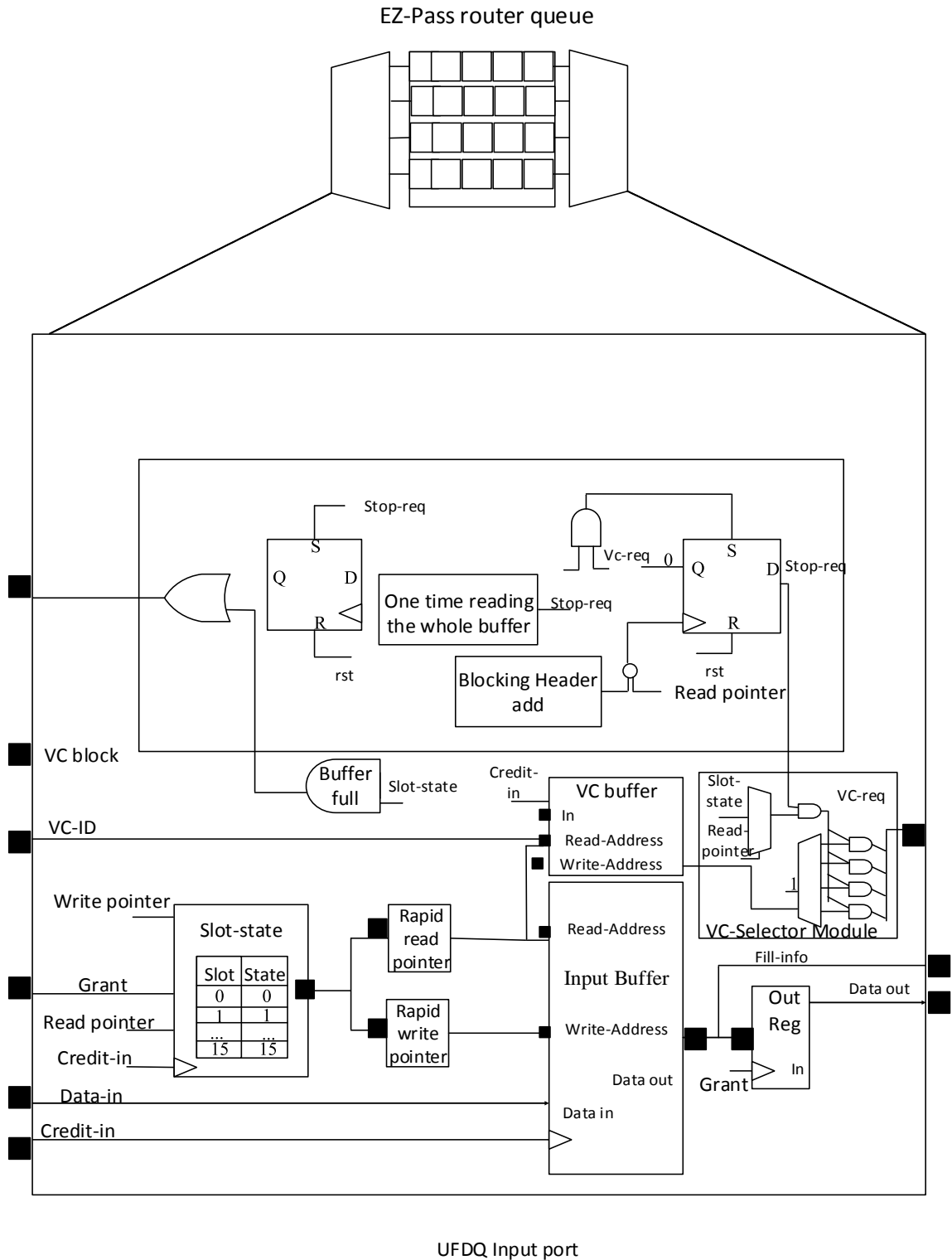
status of the downstream router is denoted by  $S$ . In the unified table, the present router will store credit number of its subsequent router. The VC state table is indicated in Figure 4.18.



**Figure 4.18: VC State Table**

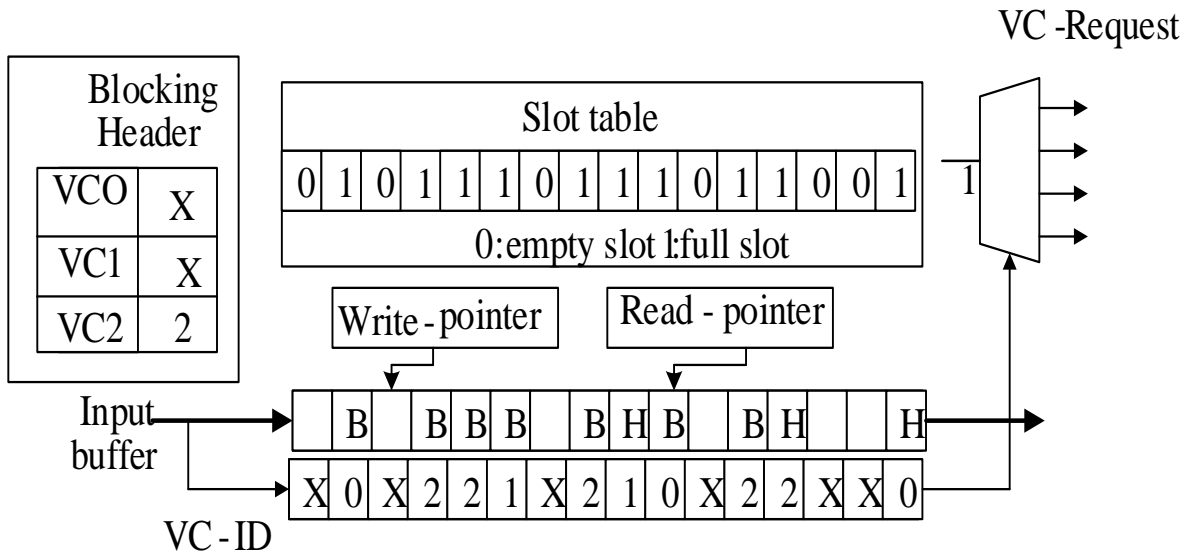
#### 4.4.4 Ultra fast dynamic Queue input port:

The Ultra fast Dynamic Queue (UFDQ) provides a dynamic flow control by utilizing the common properties of a DAMQ (Dynamically Allocated Multi-Queue) input port. When a network has a very heavy load it improves buffer management with excellent throughput. Figure 4.19 indicates Ultra Fast Dynamic Queue input port in EZ-Pass router architecture.



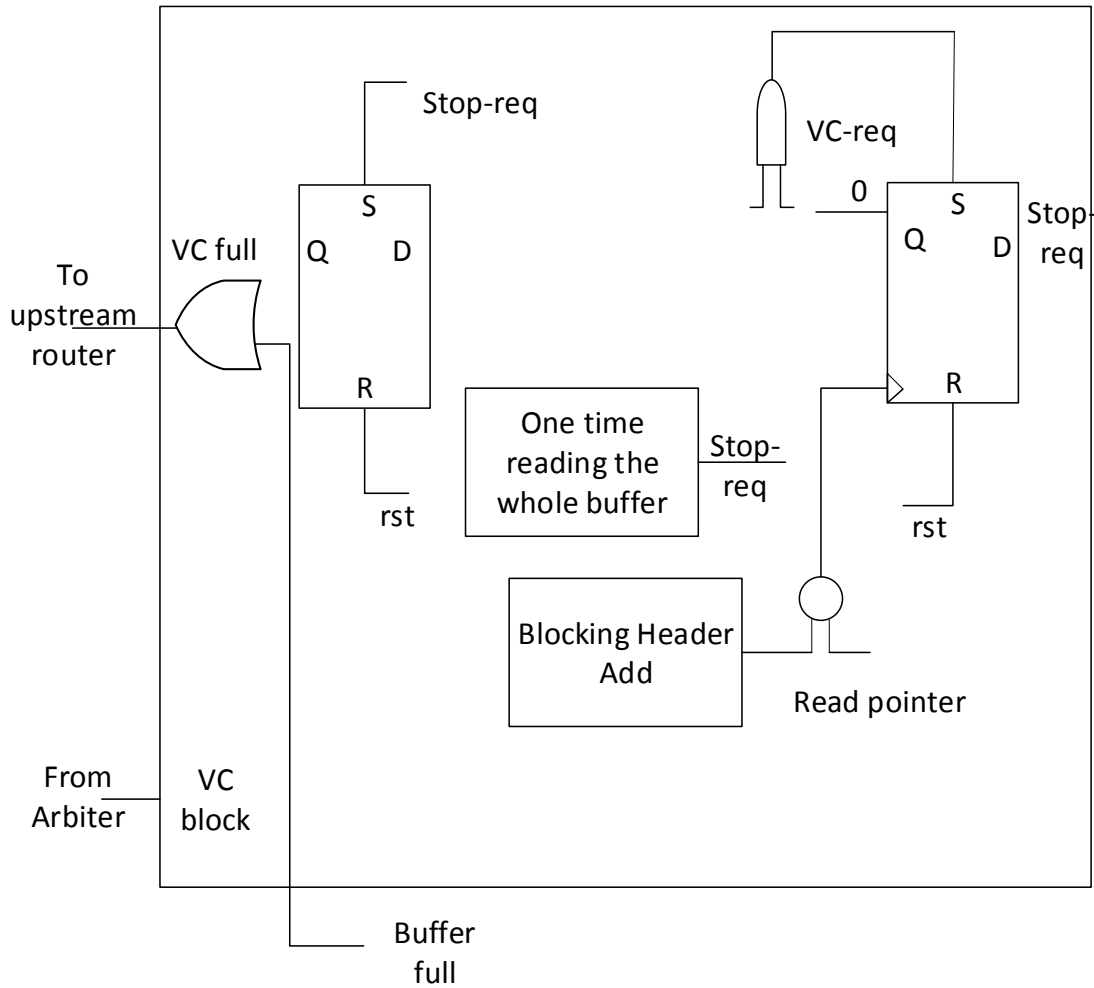
**Figure 4.19: Ultra Fast Dynamic Queue input port in EZ-Pass router architecture**

The VC identifier is being saved along with flits inside the input port buffer which is utilized to issue VC request signals to the router arbiter and it is indicated in the Figure 4.20.



**Figure 4.20: UFDQ Input port operation**

The input port buffer method is managed by a tiny slot-state table (with Boolean values). Each slot-state bit represents the occupancy state of a buffer slot. The read-pointer points to the buffer areas that are occupied every clock cycle. Until a write happens the write-pointer points to the buffers empty position. When a flit hits a blockage, its VC stops issuing requests and does not take any new flits. When a VC ie VC2 is unblocked and the IRR-read-pointer refers to the header flit (position 2) the VC request becomes free causing the read-pointer to read the entire buffer once and send out the flits of liberated VC (VC2). The VC will then begin accepting new flits. VC-full and VC-block signals help during blockage conditions and it is indicated in Figure 4.21.



**Figure 4.21: Blocking Circuit associated with VC**

This blocking circuit is associated with VC. Each VC has a VC full signal that is delivered to the upstream router and signifies the VC's readiness to accept a new flit. The arbiter sends VC block signal which represents the Virtual Channel flit cannot vacate the router. When the VC-block signal is asserted, the VC stops requesting the arbiter (the stop-req signal is asserted) and stops getting novel flits. The RDQ technique also protects a data flow circumstance from occurring in which a reserved empty VC becomes closed.

The VC-req signals and VC-full control the closing and requesting actions respectively. The state of the VC-block is determined by a number of conditions. As previously indicated the VC-block is activated whenever VC is unable for acquiring unconfined VC

of following router input terminal. Consider the first condition, in which the VC-block is reset signaling that there is no communication blockage. The VC-block becomes set for the second condition. The VC is open for the incoming flits if the reader point does not point to the VC flits. When the read-pointer is pointed to a VC flit, the VC-req shifts from 0 to 1 causing the stop-req signal to be set and the VC-req to return to 0. During this time the flit location is saved in the Blocking Header table. In other words, the router no longer receives flits for that VC and no longer requests the arbiter. Until the obstruction is lifted, the sequence of Virtual Channel flits inside buffer port is preserved. VC-block moves from one to zero in the third condition, indicating that the Virtual Channel can replace the arbiter. If Read Pointer do not refer the flit in the stuck VC, it does not send a plea and arbiter does not receive any input flits. As seen on the right side of Figure 4.20 the Read Pointer carry out for pointing the filled slots up to it reach blocked VC's header flit. VC does not allow newer flits to enter. Until the full buffer has been read, the read-pointer will continue to point the filled slots. The VC closing and requesting actions resume hereafter after pointing buffer partition twice.

#### **4.5 Simulation Results**

In this section proposed IRR-EZ-Pass router performance is compared with the conventional VC router design on NoC. Here 4x4 Mesh topology of NoC is considered for validating the proposed router design by simulating it using Xilinx ISE tools. Table 4.1 indicates various Simulation Settings. Also, the proposed router is synthesized using the family of Virtex 6 with device XC6LX75TL and package FF484.

**Virtex 6 FPGA:** It is a next generation 40nm Virtex Product Family. Virtex-6 is used for better system performance improved features and capacity. Virtex-6 is derived from Virtex-5 model. As compared to Virtex-5 model, Virtex-6 model has bigger size, density as well as its cost is reduced. The performance speed is improved with power reduction. The Virtex-6 family has 3 platforms i.e. LXT, SXT, HXT. Virtex-6 uses Flip Chip Technology. The I/Os are spread over the chip which are not limited to the periphery. Up

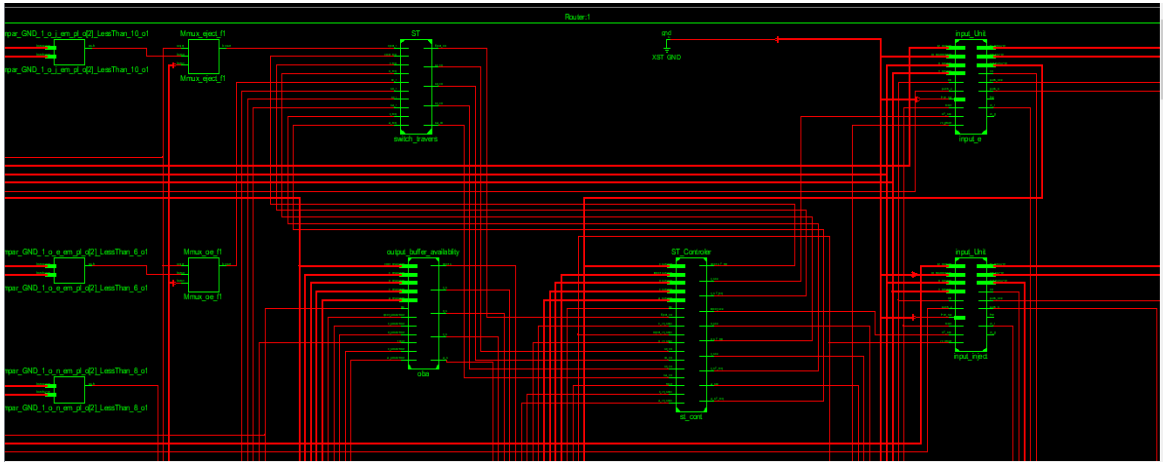
to 8000 micro bumps are attached to the package. Virtex-6 has very low thermal resistance to the board with an improved thermal performance.

**Table 4.1: Simulation Settings**

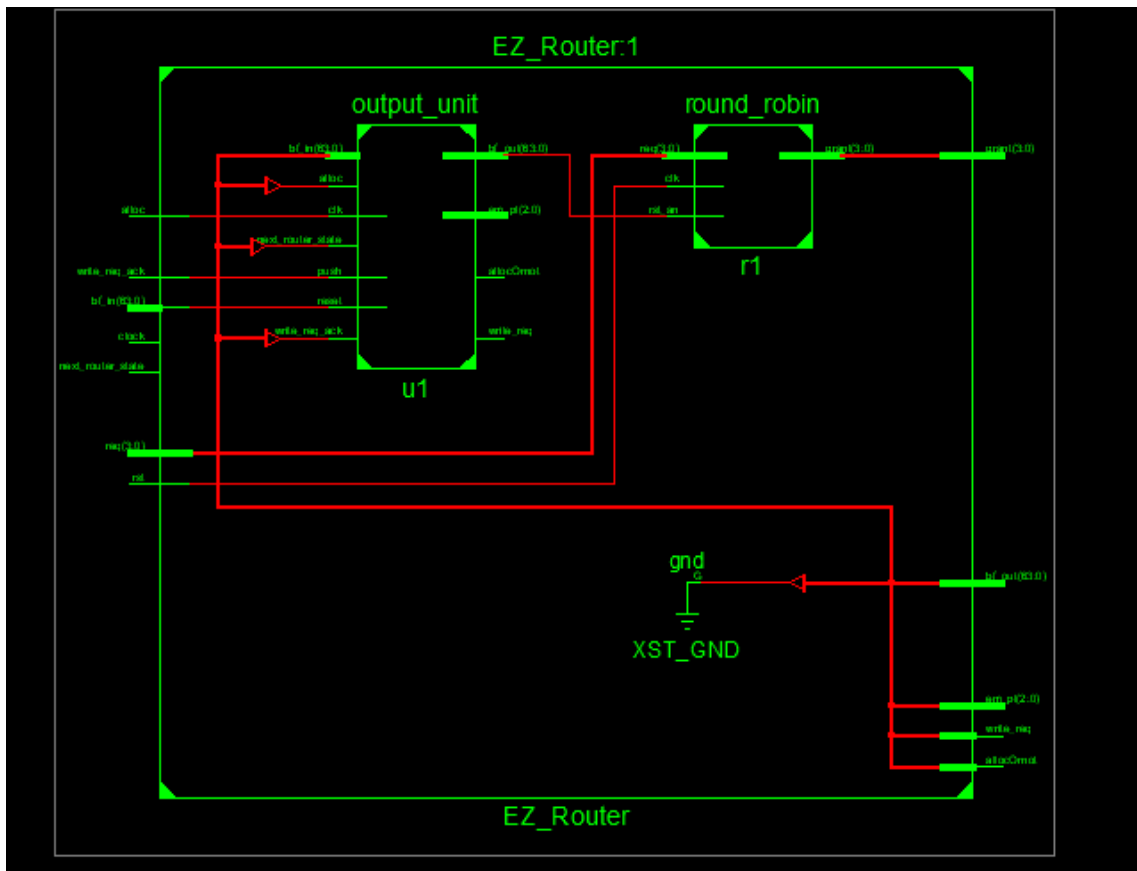
<b>Family</b>	Virtex6 Lower Power	▼
Device	XC6VLX75TL	▼
Package	FF484	▼
Speed	-1L	▼
Synthesis Tool	XST (VHDL/Verilog)	▼
Simulator	ISim (VHDL/Verilog)	▼
Preferred Language	Verilog	▼
Property Specification in Project File	Store all values	▼
Manual Compile Order	<input type="checkbox"/>	
VHDL Source Analysis Standard	VHDL-93	▼

The simulated IRR-EZ-Pass router used conventional VC router during higher traffic mode and EZ-Pass switch during lower traffic modes. The simulation of VC router is carried out by constructing a UFDQ based input port, RC, VA, SA and Crossbar. Furthermore the by-pass route is represented using the proposed IRR-EZ-Pass switch that contains latches, multiplexers and de-multiplexers. In addition a controller is used to route the packets towards NI through IRR during lower and sporadic traffic modes. The FPGA designs should determine the best trade-off between area, power and critical path delay. In this work an efficient IRR arbiter is used in the EZ-Pass switch for reducing area and power consumption in the routers. The RTL schematic of the VC router and the proposed single node IRR-EZ-Pass switch is illustrated in Figure 4.22.





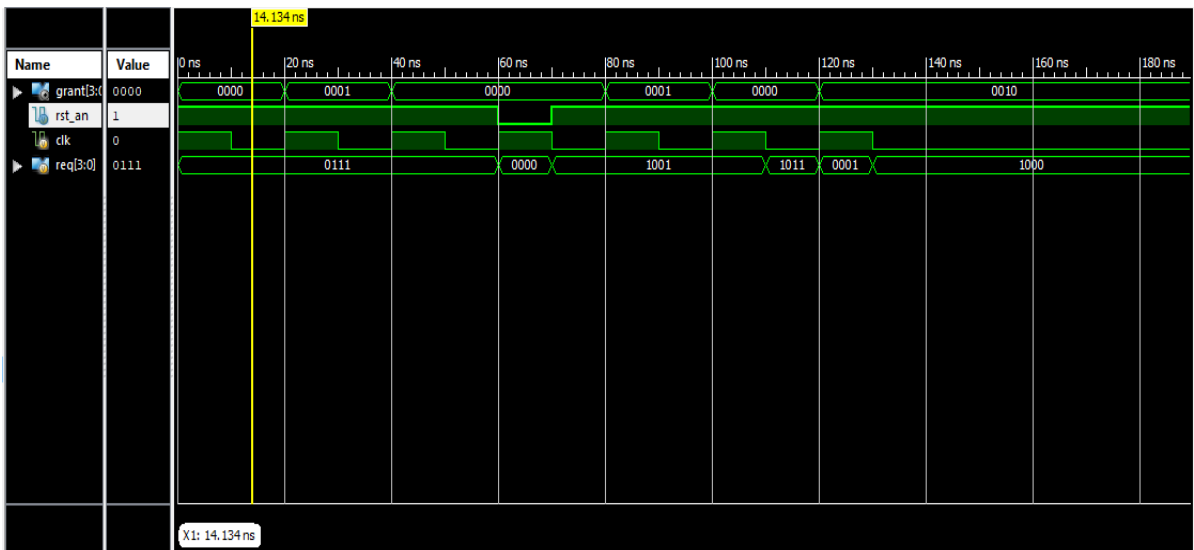
(a)



(b)

Figure 4.22: RTL schematic of Router (a) VC router (b) IRR EZ-Pass switch (single node)

The simulated waveform of the IRR arbiter is shown in Figure 4.23. For each clock cycle the IRR arbiter authorizes each input request bit by bit per method. If no request is claimed the priority of the most recently permitted request is saved and verified after a fresh plea is made. However because the RoR was unable to record the priority it was able to display alternative waveforms. Circumstance causes PRRA, IPRRA, and HDRA to arbitrate as null request is not handled by the circuit. Keeping the last priority when there are no requests has a direct influence on an arbiter's impartiality. The strength of our IRR arbiter fairness arbitration is its first benefit.



**Figure 4.23 : Simulation result of IRR Arbiter**

#### 4.5.1 Hardware requirements of IRR-EZ-Pass router based NoC:

- **Design Area Analysis**

Initially the IRR arbiter is compared with Round Robin (RoR) arbiter for analyzing the efficiency of its hardware design. The features of the IRR and RoR arbiters are listed in Table 4.2 for several formation of input including 4-bit, 8-bit, 16-bit and 32-bit. The function of IRR is differed from RoR based on the input ports index port. The index based arbiter hardware overhead is less due to its simpler and faster design consideration. It is observed that the IRR needs fewer combinational elements and registers as compared to the RoR arbiters. It requires 41.05% low combinational elements and 75% low

registers as compared to RoR arbiter for 16-bit input formation. The chip layout of this IRR design is simple due to the requirement of less number of Registers (R) and also less Combinational Elements (CE). For 32 bit input the reduction in area overhead for CE is 46.82% while for R it is 84.37%.

**Table 4.2: Comparative analysis of IRR and RoR**

<b>Input</b>	<b>Arbiters</b>	<b>Combinational Elements (CE)</b>	<b>Registers (R) bits</b>	<b>Reduction in overhead (%)</b>
4	RoR	13	4	30.76@CE 50@R
	IRR	9	2	
8	RoR	37	8	32.43@CE 62.5@R
	IRR	25	3	
16	RoR	95	16	41.05@CE 75@R
	IRR	56	4	
32	RoR	205	32	46.82@CE 84.37@R
	IRR	109	5	

Figure 4.24 illustrates the RTL schematic of the top view of NOC 4x 4 structure. Here a single pin is allocated for every router in NOC. The nodes can inject the packet into the network. Figure 4.25 provides the simulation results of the 4x4 Mesh Topology.

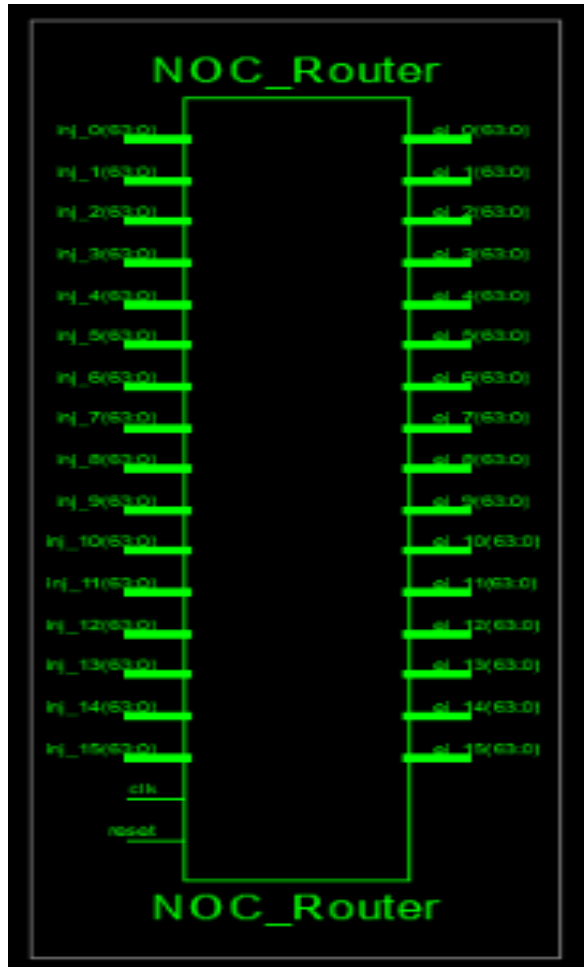
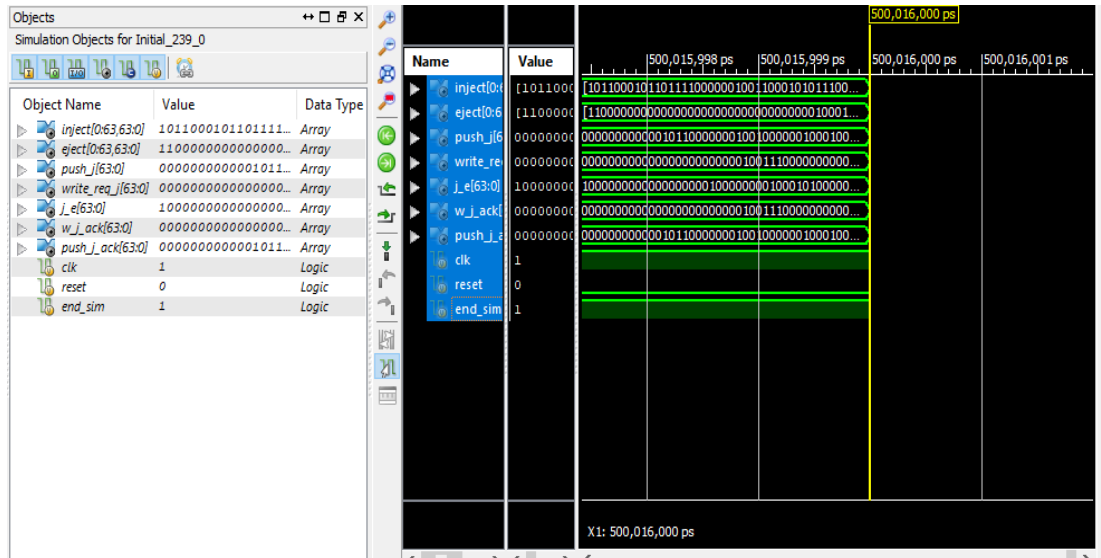


Figure 4.24: RTL schematic of the top view of 4x4 NOC structure



**Figure 4.25: Simulation results of 4x4 Mesh Topology**

Table 4.3 indicates device utilization summary of the proposed IRR-EZ-Pass switch and VC router unit with UFDQ on 4x4 Mesh topology. Here the NoC architecture with IRR EZ-Pass switch reduced the area overhead by consuming 89.92% less slice registers and 88.50% less slice LUTs as compared to VC router with UFDQ. Also it consumed 80.79% less fully used LUT-FF pairs as compared to VC router with UFDQ. Moreover the IRR-EZ-Pass switch uses same number of BUFG/BUFGCTRL/BUFHCEs as compared to VC router. The proposed model also enables the VC router during high traffic mode. Hence we modified the structure of the conventional VC router using ultra-fast Dynamic Queues (UFDQ) to tackle the issues of conventional structures. UFDQ input-ports require a common VC-selector. The hardware overhead of the UFDQ based input-ports is very less while comparing with conventional input port for the similar counts of VCs and buffer slots. But the hardware overhead of the UFDQ based router is increased with respect to AND gates and registers per VC. However the number of multiplexers has been increased exponentially in conventional input port structure while increasing the size of the input-port buffer. Hence hardware overhead, power consumption and critical path delay of conventional router have been increased abruptly as compared to VC router with UFDQ. Also the IRR-EZ-Pass switch reduced the area overhead when it is used only for sporadic and low traffic modes.

**Table 4.3: Device utilization summary of the IRR EZ-Pass switch**

<b>Logic utilization</b>	<b>Available</b>	<b>VC router with UDQ</b>	<b>IRR-EZ-Pass switch</b>	<b>Reduction in area overhead (%)</b>
Number of Slice Registers	1,224,000	2750	277	89.92
Number of Slice LUTs	3036	3036	349	88.50
Number of fully used LUT-FF pairs	3063	1437	276	80.79
Number of BUFG/BUFGCTRL/BUFHCEs	2	2	2	-

The network power consumption is described through the consideration of both static and dynamic power. Static power denotes the leakage power of each hardware component. The performance of dynamic and static power in NoC depends heavily on on-chip traffic intensity. The proposed framework uses IRR-EZ pass switch for low and sporadic mode traffic and VC router with UFDQ for high traffic mode. Hence the total power is considered for evaluating the power consumption. The area for EZ-Pass router is reduced due to usage of less Slice Registers, Slice LUTs and buffers as compared to conventional routers.

- **Power Analysis**

Figure 4.26 compare the total Power Consumption (W) of the IRR-EZ pass switch with VC router. Here the dynamic power of the entire modules including router and NI are considered to monitor execution of dynamic power consumption. This router design changes micro architecture of the conventional VC router by replacing the input port with UFDQ based input port. Also the EZ-pass route is modified by introducing IRR arbiter instead of RoR arbiter. The IRR-EZ pass switch consumes 18% less power as compared to VC router with UDQ for 16x16 Mesh topology. The proposed IRR-EZ pass switch consumes low power due to fast and simple design consideration. Therefore dynamic power consumption of the proposed framework is reduced. Table 4.4 and Table 4.5 indicate Power Analysis using X-Power Analyzer for VC Router and EZ-Pass Router

respectively. Table 4.6 indicates entire power analysis for VC and EZ-Pass Router respectively.

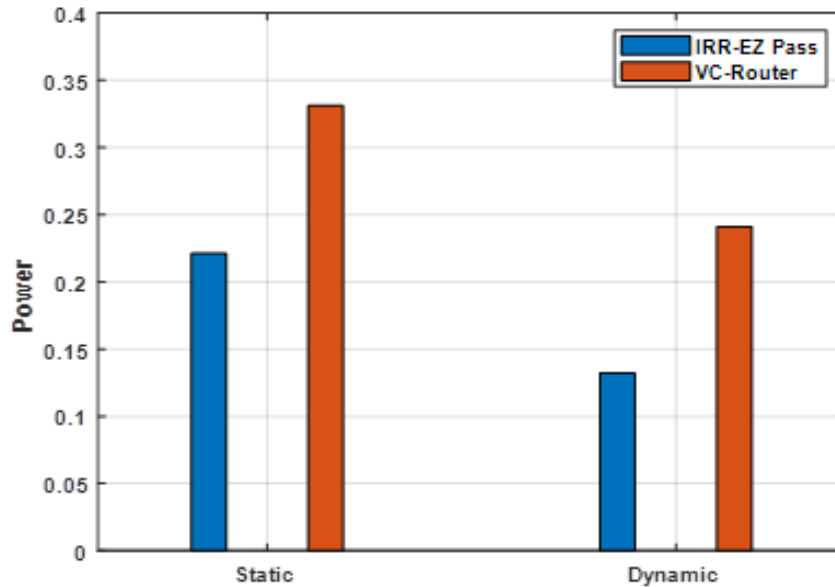


Figure 4.26: Power Analysis

Table 4.4: Power Analysis by X-Power Analyzer for VC Router

A	B	C	D	E	F	G	H	I	J	K	L	M	N
Device		On-Chip	Power (W)	Used	Available	Utilization (%)			Supply	Summary	Total	Dynamic	Quiescent
Family	Virtex7	Clocks	0.000	1	--	--			Source	Voltage	Current (A)	Current (A)	Current (A)
Part	xc7vx980t	Logic	0.000	330	612000	0			Vccint	1.000	0.215	0.000	0.215
Package	ffg1930	Signals	0.000	397	--	--			Vccaux	1.800	0.061	0.000	0.061
Temp Grade	Commercial	IOs	0.000	135	900	15			Vcco18	1.800	0.051	0.000	0.051
Process	Typical	Leakage	0.331						Vccbram	1.000	0.245	0.241	0.004
Speed Grade	-2L	Total	0.331										
Environment		Thermal Properties	Effective TJA	Max Ambient	Junction Temp				Supply	Power (W)	Total	Dynamic	Quiescent
Ambient Temp (C)	25.0		(C/W)	(C)	(C)						0.572	0.241	0.331
Use custom TJA?	No		0.8	84.7	25.3								
Custom TJA (C/W)	NA												
Airflow (LFM)	250												
Heat Sink	Medium Profile												
Custom TSA (C/W)	NA												
Board Selection	Medium (10"x10")												
# of Board Layers	12 to 15												
Custom TJB (C/W)	NA												
Board Temperature (C)	NA												

**Table 4.5: Power Analysis by X-Power Analyzer for EZ-Pass Router**

A	B	C	D	E	F	G	H	I	J	K	L	M	N
Device		On-Chip	Power (W)	Used	Available	Utilization (%)			Supply	Summary	Total	Dynamic	Quiescent
Family	Artix7	Signals	0.000	8	--	--			Source	Voltage	Current (A)	Current (A)	Current (A)
Part	xc7a100t	IOs	0.000	16	210	8			Vccint	1.000	0.017	0.000	0.017
Package	csg324	Leakage	0.082						Vccaux	1.800	0.013	0.000	0.013
Temp Grade	Commercial	Total	0.082						Vcco18	1.800	0.004	0.000	0.004
Process	Typical								Vccbram	1.000	0.289	0.132	0.157
Speed Grade	-3								Vccadc	1.710	0.020	0.000	0.020
		Thermal Properties		Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)							
				4.6	84.6	25.4			Supply Power (W)		Total	Dynamic	Quiescent
Environment											0.343	0.132	0.211
Ambient Temp (C)	25.0												
Use custom TJA?	No												
Custom TJA (C/W)	NA												
Airflow (LFM)	250												
Heat Sink	Medium Profile												
Custom TSA (C/W)	NA												
Board Selection	Medium (10"x10")												
# of Board Layers	12 to 15												
Custom TJB (C/W)	NA												
Board Temperature (C)	NA												
Characterization													
Production	v1.0.2012-07-11												

**Table 4.6: Power Analysis of EZ-Pass versus VC Router**

Power Analysis (W)			
EZ Pass Router		VC Router	
Static	Dynamic	Static	Dynamic
0.211	0.132	0.331	0.241

**4.5.2 Performance Evaluation of Throughput, Dropping probability and Latency:**

- ***Throughput Analysis***

The key performance parameters of NoC are Latency and Throughput. Hence the performance of the proposed IRR-EZ pass switch based NoC structure is validated in terms of Latency and Throughput. They are determined by varying the flit injection rates per time unit. According to the ability of NoC routers for sending the flits the maximum injection rate is taken into consideration. Here the IRR-EZ pass switch can be used only when the source node injects a maximum 0.01 flits per time unit. If the injection rate is



higher than this then the VC router with UFDQ is enabled. Here an extreme level of 0.005 flits per time unit is considered for low traffic mode and 0.01 flits per time unit for sporadic traffic mode for simulation. Throughput is defined as processing rate of a data at any instance. Figure 4.27 illustrate the throughput performance of IRR-EZ pass switch and VC router for (a) Sporadic traffic and (b) Low traffic on 16x16 Mesh topology. Table 4.7 and Table 4.8 represent throughput analysis for Sporadic and Low traffic respectively. For low traffic as there is increase in Inject rate the throughput decreases accordingly.

Throughput can be mathematically calculated as given in Equation No.4.1

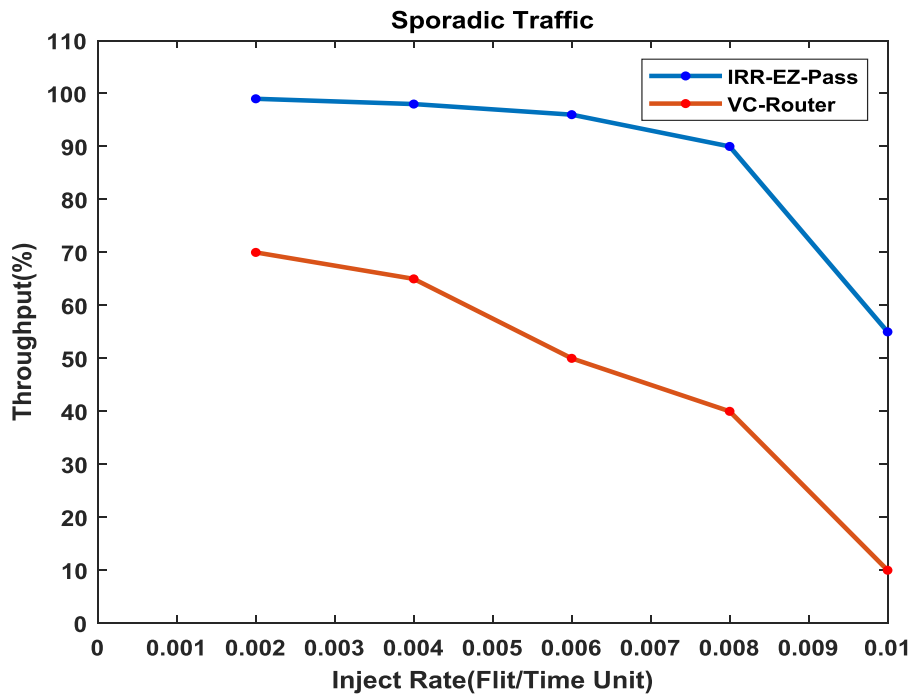
$$\text{Throughput} = \text{data/time} \quad (4.1)$$

**Table 4.7: Throughput Analysis for Sporadic Traffic**

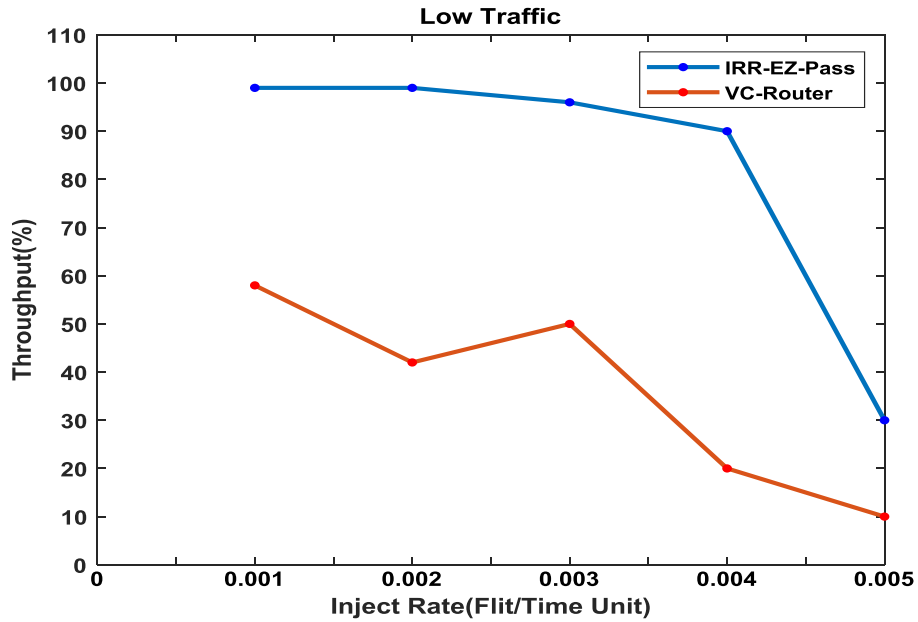
<b>VC Router</b>		<b>EZ-Pass Router</b>	
<b>Inject Rate</b>	<b>Throughput (%)</b>	<b>Inject Rate</b>	<b>Throughput (%)</b>
0.001	70	0.001	100
0.002	70	0.002	100
0.003	68	0.003	98
0.004	65	0.004	95
0.005	55	0.005	93
0.006	50	0.006	92
0.007	45	0.007	90
0.008	40	0.008	88
0.009	25	0.009	75
0.01	15	0.01	55

**Table 4.8: Throughput Analysis for Low Traffic**

VC Router		EZ-Pass Router	
Inject Rate	Throughput (%)	Inject Rate	Throughput (%)
0.001	60	0.001	100
0.002	45	0.002	99
0.003	50	0.003	95
0.004	20	0.004	90
0.005	10	0.005	30



(a)



(b)

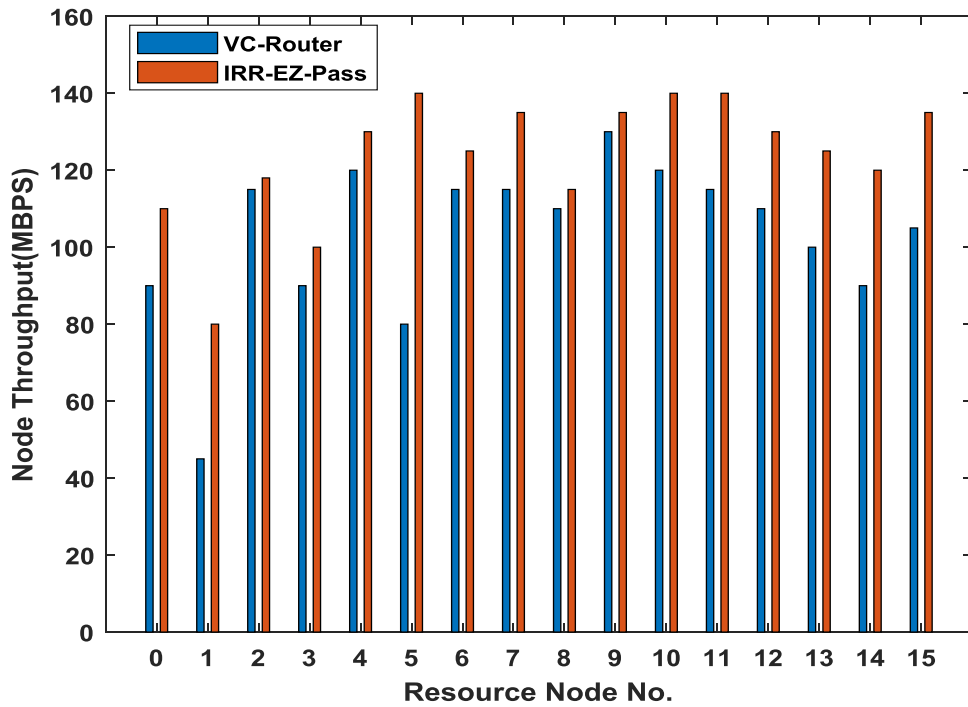
**Figure 4.27: Throughput analysis (a) Sporadic traffic (b) Low traffic**

This analysis shows that the throughput of the proposed IRR-EZ-Pass router is high with respect to traditional VC Router during low as well as sporadic traffic modes. Reason behind this is that the proposed IRR-EZ-Pass switch routes the packets through a simple switching method instead of a complicated pipelined router. Also the IRR arbiter is considered as least recently assisted priority approach for achieving robust fairness arbitration. The arbiter fairness can be affected while maintaining the last priority at some point in no request situation. The IRR arbiter provides powerful fairness arbitration. Hence, it reduces the packet loss for improving the throughput.

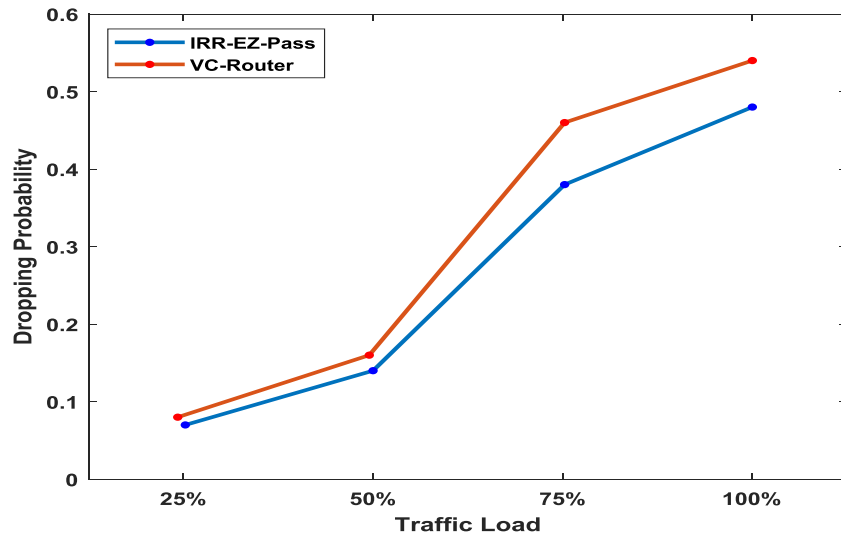
- **Dropping Probability**

Execution of proposed architecture is also validated considering 100% traffic load. If all the source nodes transmit maximum packets then it is considered as 100% traffic load. Figure 4.28 (a) shows the throughput output of every target nodes. The dropping probability is obtained by calculating the ratio of packets input to packets output from

every source node. Figure 4.28 (b) illustrates the changes of dropping probability with respect to the traffic load. IRR-EZ-Pass router on 4x4 mesh topology reduced the dropping probability due to the consideration of a simple switching method and a least recently assisted priority approach. Table 4.9 represents dropping analysis for 100% traffic load.



(a)



(b)

**Figure 4.28: Analysis for 100 % traffic load (a) Throughput (b) Dropping probability**

**Table 4.9: Dropping Probability for 100% Traffic Load**

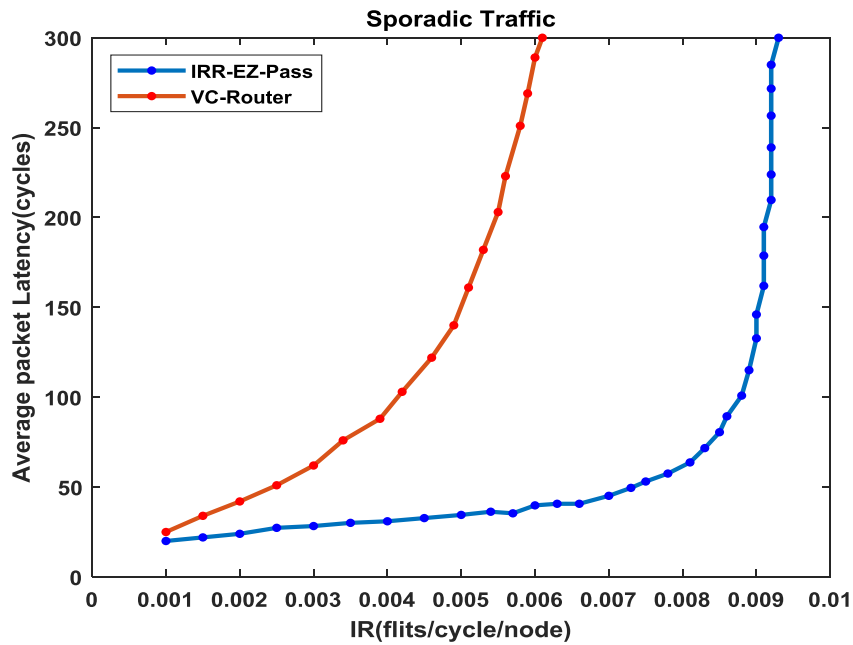
VC Router		EZ-Pass Router	
Traffic Load	Dropping Probability	Traffic Load	Dropping Probability
25	0.09	25	0.08
50	0.15	50	0.14
75	0.45	75	0.35
100	0.55	100	0.45

- **Latency Analysis**

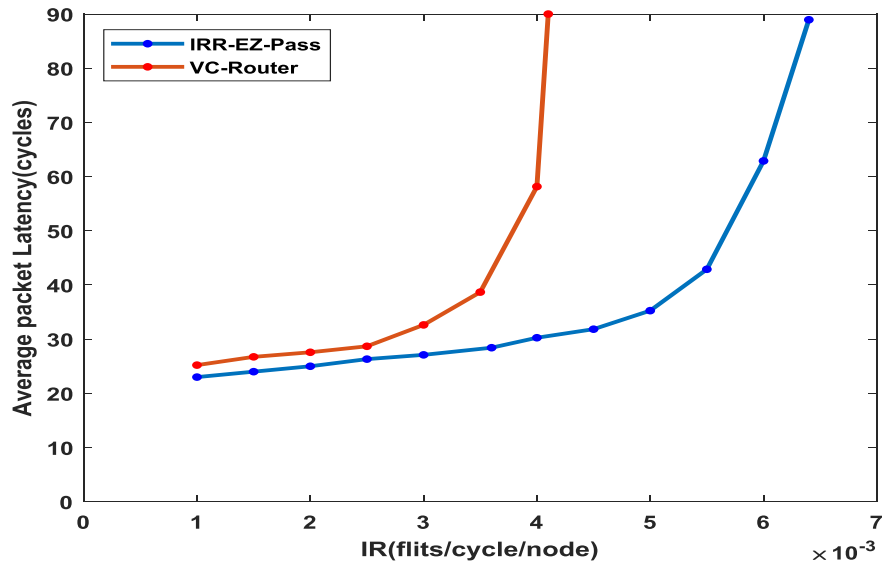
The time delay related to the leaving and entering of certain number of packets in NoC is used to measure the average latency. The following formula given in Equation No. 4.2 is used to estimate the Average Latency (AL).

$$AL = \frac{\tau_{TR} - \tau_{TT}}{N_{TF}} \quad (4.2)$$

Where  $\tau_{TR}$  denotes the total received time of flits,  $\tau_{TT}$  denotes the total ideal transmitted times of flits and  $N_{TF}$  denotes the total count of transmitted flits. The extreme latency of the proposed design does not exceed the particular limit. Because it does not considered the injection rate of above 0.01 flits/cycle/node. Also the  $\tau_{TR}$  will not be varied if the flit injection rate is higher than 0.01. However  $\tau_{TT}$  may turn out to be zero hypothetically. Here,  $N_{TF}$  is not varied and it can be calculated by multiplying the amount of injected packets, amount of sources and the flits/packet. Hence the maximum average latency is  $\frac{\tau_{TR}}{N_{TF}}$  and it is not varied. Figure 4.29 illustrates the latency performance of IRR-EZ pass switch and VC router for low traffic and sporadic traffic on 16x16 Mesh topology. Table 4.10 and 4.11 represents latency analysis for sporadic and low traffic respectively.



(a)



(b)

Figure 4.29: Latency analysis (a) Sporadic traffic (b) low traffic

Table 4.10: Latency for Sporadic Traffic

VC Router		EZ-Pass Router	
Inject Rate	Average Packet Latency (ms)	Inject Rate	Average Packet Latency (ms)
0.001	35	0.001	30
0.002	40	0.002	35
0.003	60	0.003	35
0.004	90	0.004	40
0.005	150	0.005	45
0.06	250	0.06	48
0.007	300	0.007	50
0.008	300	0.008	55
0.009	300	0.009	98
0.01	300	0.01	300

**Table 4.11: Latency for Low Traffic**

<b>VC Router</b>		<b>EZ-Pass Router</b>	
Inject Rate	Average Packet Latency (ms)	Inject Rate	Average Packet Latency (ms)
0.001	28	0.001	25
0.002	30	0.002	28
0.003	35	0.003	30
0.004	60	0.004	35
0.005	90	0.005	40
0.06	90	0.06	65
0.007	90	0.007	90

Figure 4.30 (a) represents RTL Schematic of EZ-Pass Router while (b) represents Simulation results for EZ-Pass router. A conventional VC router increases the latency at lower flit injection rates due to its higher buffer capacity. However, the proposed router uses simple switching scheme for sporadic and low traffic modes. Hence it reduces the average packet latency. Table 4.12 represents Delay Analysis for VC and EZ-Pass routers respectively. Table 4.13 represents Frequency Analysis for VC and EZ-Pass routers respectively.

- *Delay Analysis*

**Table 4.12: Delay Analysis**

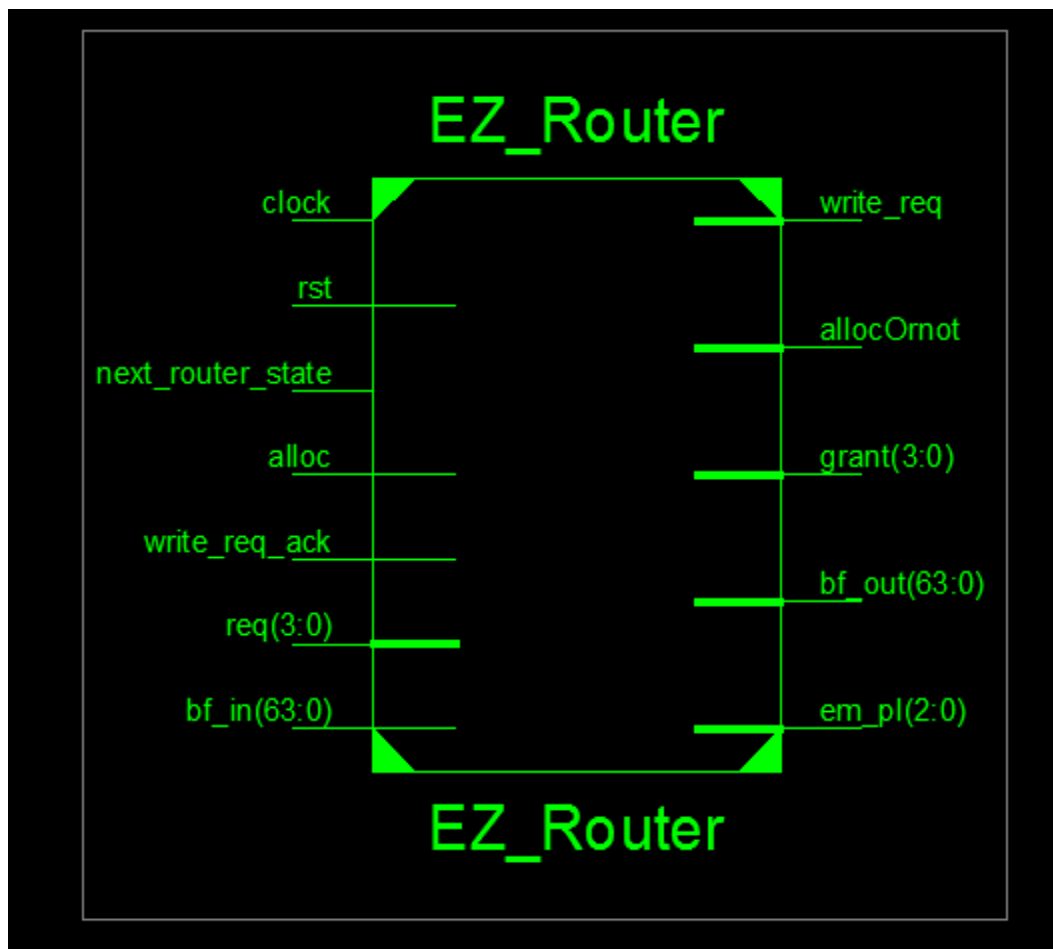
<b>Delay Analysis</b>	<b>VC Router</b>	<b>EZ-Pass Router</b>
	3.450 ns	1.77 ns



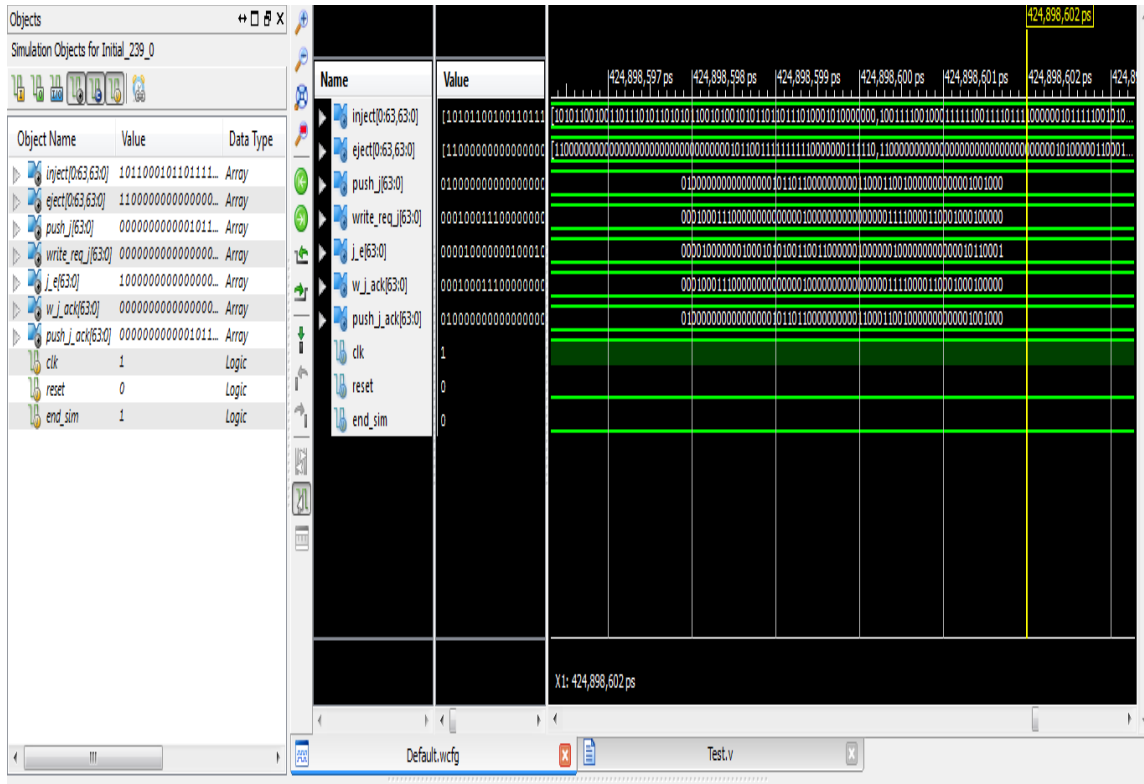
- *Frequency Analysis*

**Table 4.13: Frequency Analysis**

Parameter	VC Router	EZ-Pass Router
Maximum Frequency	242.468 MHz	724.061 MHz
Minimum Input arrival time before clock	6.237 ns	1.550 ns
Maximum Input arrival time after clock	3.058ns	0.723ns
Maximum Combinational path delay	1.971ns	No path found



(a)



(b)

**Figure 4.30: (a) RTL Schematic of EZ-Pass Router (b) Implementation simulation result for EZ-Pass router**

## 4.6 Summary of the Chapter

In this chapter, a new NoC router architecture is proposed by enhancing the Easy Pass routing and input-port modules of the router architecture with IRR and UFDQ respectively. This structure includes both conventional VC router and EZ-Pass switch to handle high traffic mode and sporadic and low traffic modes respectively. Also it used a control block and the power gating method to powering off routers during consecutive idle time. It is observed from the simulation results that the delay, power consumption and chip area of developed IRR-EZ pass switch are very low as compared to the conventional VC router. Also the introduction of UFDQ and IRR helps to improve the

performance of the router under different injection rates and consume low power due to its simplest hardware structure. The simulation results also show that the developed architecture consumes a total of 0.343W power which is much better than the conventional VC router which consumes total power of 0.572W. Also performance of system is improved in terms of throughput and latency.

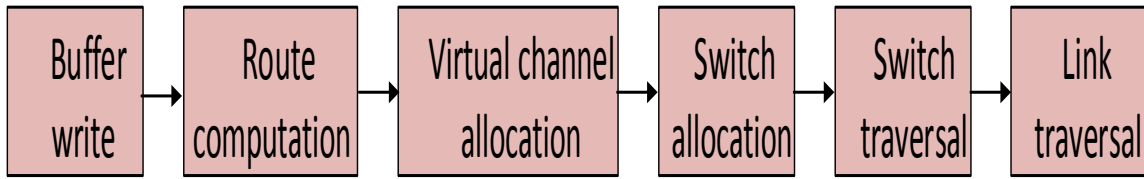
## CHAPTER-5

### PERFORMANCE ANALYSIS OF NOC USING BLESS, BBUS, TCMP AND CHIPPER ROUTER CONCEPT

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#### 5.1 Introduction

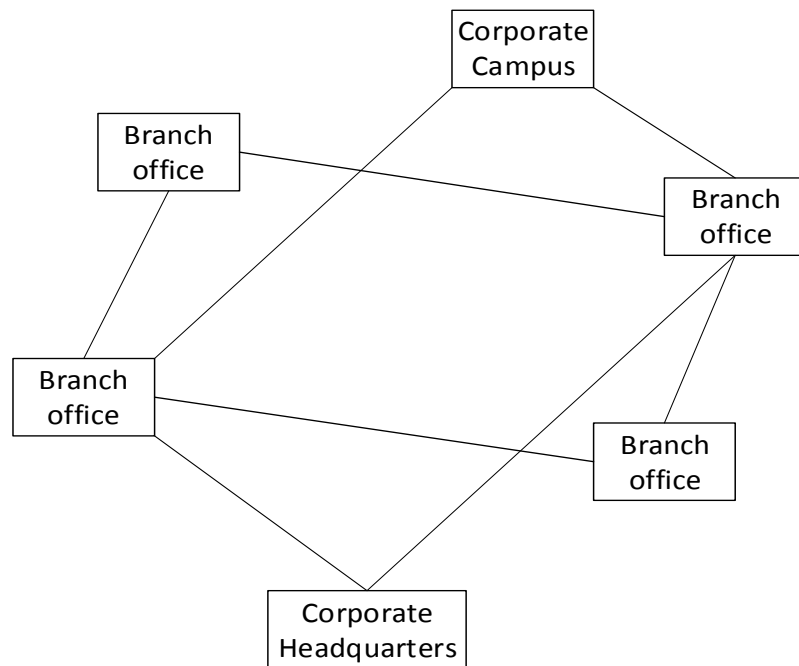
Network on chips (NoC) have now become crucial elements in router architecture, with significantly better outcomes than system on chips. NoC is an essential module in router design which connects cores on chips and memory components [98]. Previous approaches [99] used bus and ad hoc architectures, but NoC is a preferable alternative. Between processing elements linked on a chip, it provides low scalability, low power and low latency. When there is less traffic, the advanced bypass path approach is employed to minimize packet arrival latency [100]. The following are the functionalities of a NoC router: Virtual channel allocation (VA), Buffer writes (BW), Switch traversal (ST), Switch allocation (SA) and Route computation (RC). Figure 5.1 depicts the sequence in which flits go via the virtual channel. To increase area utilization and chip performance in the on-chip design should also be reduced [101]. In router design an Elastic buffer control mechanism is utilized to eliminate the expense of buffers. The usage of virtual channels [102] reduces the chips size, static and dynamic power and latency. Buffers, virtual channel controller, allocator, arbiter and routing path controller are some of the characteristics that go into a good router design. The static power can be lowered using the power gating approach. Thermal buffers are created by TCMP which lowers the temperature of nearby tiles. Virtual channels and X-Y routing are utilized on both ends to increase data transmission [103]. The static power can be lowered using the power gating approach.



**Figure 5.1: NoC Router Pipeline**

## 5.2 Basic Model of NoC router using Mesh

During port disputes packets remains in buffers in VC router design. Excess amount of energy is consumed by buffers. The amount of loose buffers within VC is referred to as credit. Up- stream packets pass credits that will arrive and dwell in buffers; the packets will be routed to the appropriate channel output depending on the routers logic control. Managing strategies for data loss and maintaining signal quality is critical in NoCs. As a result buffers appear to be a critical component of current router architecture, as they retain the flits as illustrated in Figure 5.2.



**Figure 5.2 : NoC basic model using Mesh Topology**

### 5.3 NoC Routing

The conventional bus concept execution necessitates the use of massive multiplexers and the resolution of cache coherence issues. As a result, bus communications for today's modern MPSoC topologies are not scalable [104]. Table 5.1 denotes Mesh NoC Packet flow structure.

**Table 5.1: Mesh NoC Packet flow structure (4x4)**

12	13	14	15
8	9	10	11
4	5	6	7
0	1	2	3

In a  $4 \times 4$  Mesh NoC using XY routing packet 13 injected into a router 7 as shown in Table 5.1 the following assertions are correct.

- i) P1 travels through NoC 9 router
- ii) P1 reply packet travels via the router 14.
- iii) Neither the request nor the response packets are sent through the router 10.

The aim of on-chip design router is to minimize the number of buffers in order to improve the useful space of the SoC. Overheads in the control area can be hidden to considerably reduce the latency. By using single cycle architecture, the impact of reduced buffer also reduces latency in router design.

The cores of this 25 core computer are grouped in a typical square mesh topology. From core number 18, a packet P1 is created and sent to core 6. The system takes the shortest

route minimal north last. Below is a list of the unique minimum pathways ranging from 18 to 6.

18-17-16-11-6;

18-17-12-11-6;

18-17-12-7-6;

18-13-12-11-6;

18-13-12-7-6;

18-13-8-7-6

We had 6 ways in all, ranging from 18 to 6 with the least amount of north last routing. Table 5.2 denotes Square Mesh topology 25 core machines.

**Table 5.2: Square Mesh topology 25 core machines (5x5)**

20	21	22	23	24
15	16	17	18	19
10	11	12	13	14
5	6	7	8	9
0	1	2	3	4

## 5.4 NoC Routing Switch Arbitration

In XY routing, the switch allocation is based on age is specified as.

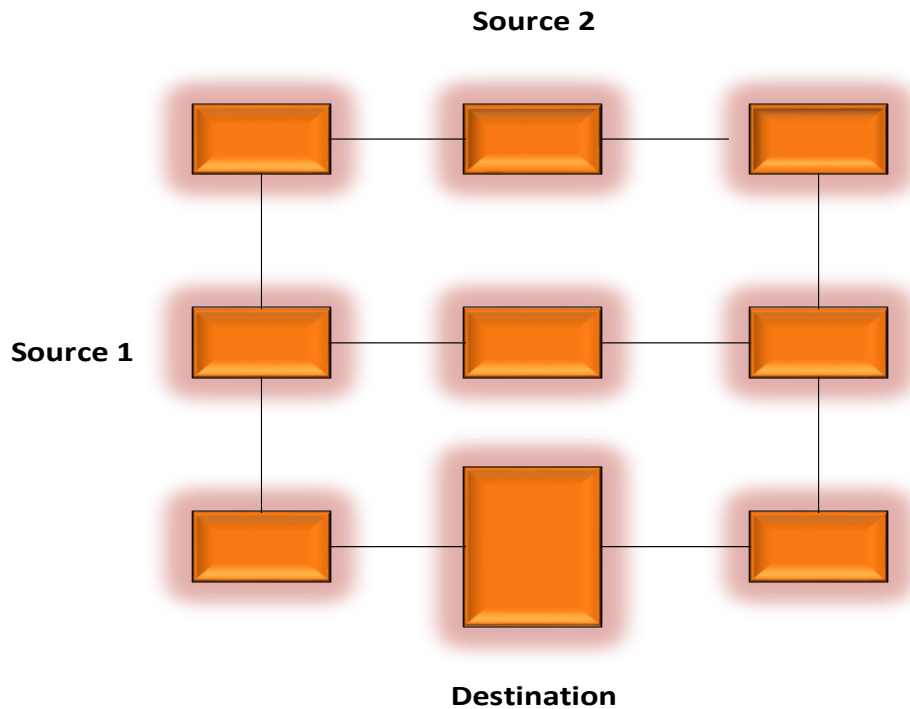
<Number of Packet, age, source, final destination>

If R is denoted as router 10 in a  $4 \times 4$  router NoC the condition must be met. Arbitration of switch is depends on a priority system depends on age. It is given that if there is just one packet contending for a desired output (south and east). However if there is large packets at similar output port, it will select barely the oldest age. Because P3 is older than P1, it gets granted port of west, whilst P2 is buffered.

## 5.5 Buffer less deflection routing

Less deflection routing of buffer is a notion in which buffers of input are not used. In latches packets are buffered on links as shown in Figure 5.3 reducing the impact of power gating [105]. In this Figure Source 1, Source 2 are the routers passing through which the packets are passing, while the others are the adjacent routers. We can use buffers in a traditional VC routing. However in buffer less routing [106] we use latches instead of buffers, which is called as routing logic of deflection. When two packets compete for similar connection, the desired link is granted to one while the other gets diverted. When two packets compete for the same connection, the buffer less deflection router gives packets of one the required link while deflected away of the second packet. Because it is a Mesh topology [107] you may still figure it on the productive path even travelling away from the final destination and it may at close by routers.





**Figure 5.3: Buffer less deflection router**

### 5.5.1 The function of buffers in NoC:

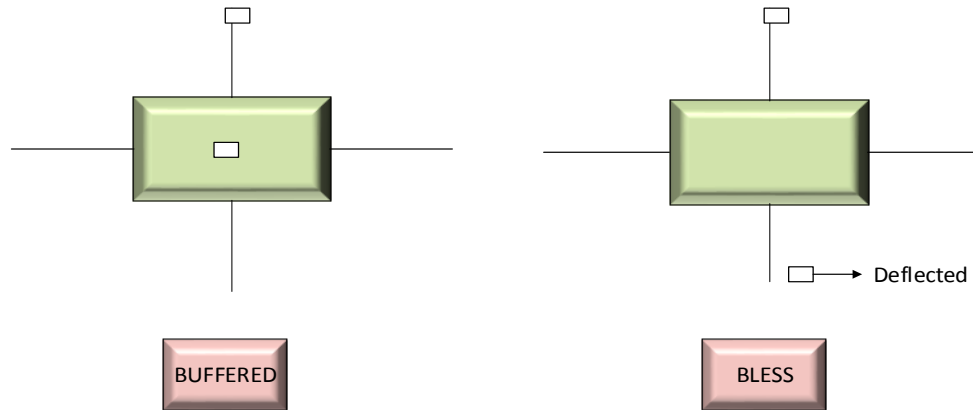
Buffers are essential for improving network performance and latency [108] because they retain packets in the network. Buffers enhance the networks total available bandwidth [109]. The greater the number of buffers the higher the networks throughput. The number of packets that enter the network every cycle is referred as injection rate. As rate of injection which is raised it raises the load and the packets struggle for space. When we have fewer buffers the network saturates sooner, and when we have more buffers, the network saturates later [110]. More buffers means extra packets can be consumed, and extra packets will move ahead. However, if we do not have the buffers, the networks are quickly saturated as shown in Table 5.3.

**Table 5.3: Parameters of Golden Epoch**

<b>Sr.No</b>	<b>Topology</b>	<b>Golden Epoch (Chipper)</b>
1.	Torus	12 cycles of clock(1 Golden epoch)
2.	Mesh	18 cycles of clock(1 Golden epoch)
3.	BBUS	1 cycles of clock(1 Golden epoch)

**5.5.2 BLESS routing concept:**

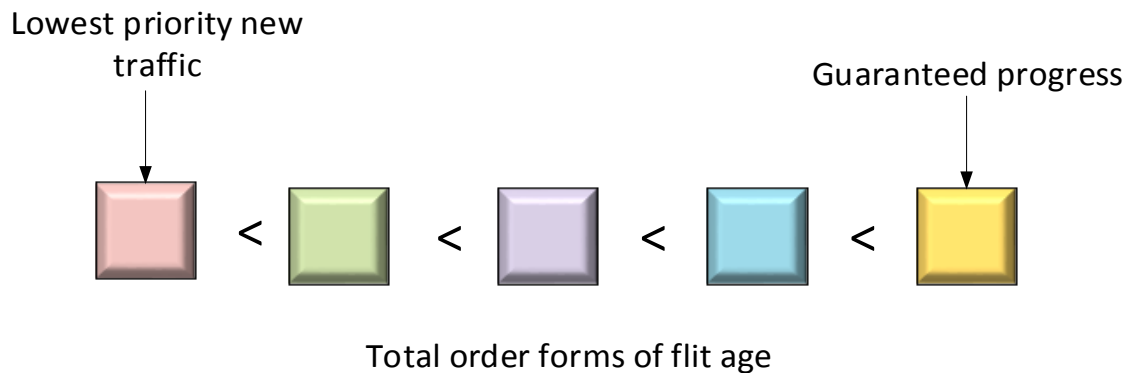
Every flit of input is sent to an output of random under the Hot potato routing concept [111]. If the right direction is not possible, one of the packets is transmitted to a different port while the deflected of second flit [112] as seen in Figure 5.4. Buffered routing considers two flits travelling in the same direction to the router; if one of the flits reaches a port of profitable in the north; the buffered of the other flit, which is a benefit of buffered routing. The sorting of flits and priority allocation to ports are two crucial phases in BLESS. Routed of each flit separately and the priority is determined by the flit of oldest. If at all feasible, flit should be sent to a port of profitable; otherwise, it should be assigned to a non productive port. There is no requirement for a handshake mechanism because flow control is purely local. Flit injection can be done anywhere a port is available. Deadlock is absent since flits are continually moving, and the live lock gets absent because the ranking of the oldest flit idea is utilized [113].



**Figure 5.4 :BLESS Routing Concept**

**5.5.3 BLESS live lock freedom:**

As indicated in Figure 5.5 the conditions that prevent a flit from the deflection indefinitely are that all of the flits must be stamped of time, and the flits of oldest must be allocated to their target ports. The flit of oldest in the system will be assured progress, whereas the systems flit of the newest will be given the priority of lowest [114]. Once time passes, the inserted flits of the new one will become the oldest system and progress will be assured from there. The concept of freedom of live lock is that the flits be ordered in chronological order depends on their age, with the flit of eldest receiving productive port at all times.



**Figure 5.5: Ordering of flits**

#### 5.5.4 Expensive priority depending on age:

The routers parameter that must sorted flits by age determines expensive age based priority. Depending on priority, the oldest flit is transmitted to the specified output. To get to the destination port, lower priority flits follow the highest priority flits. As demonstrated in Figure 5.6 the deflection routing idea and algorithms are applied.

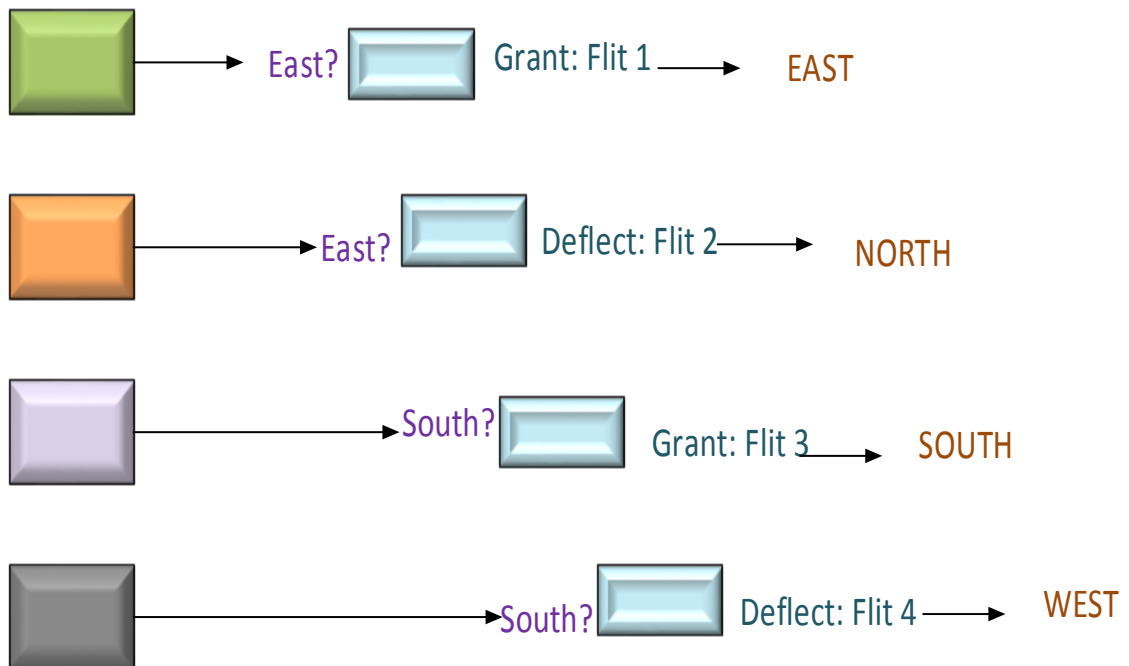
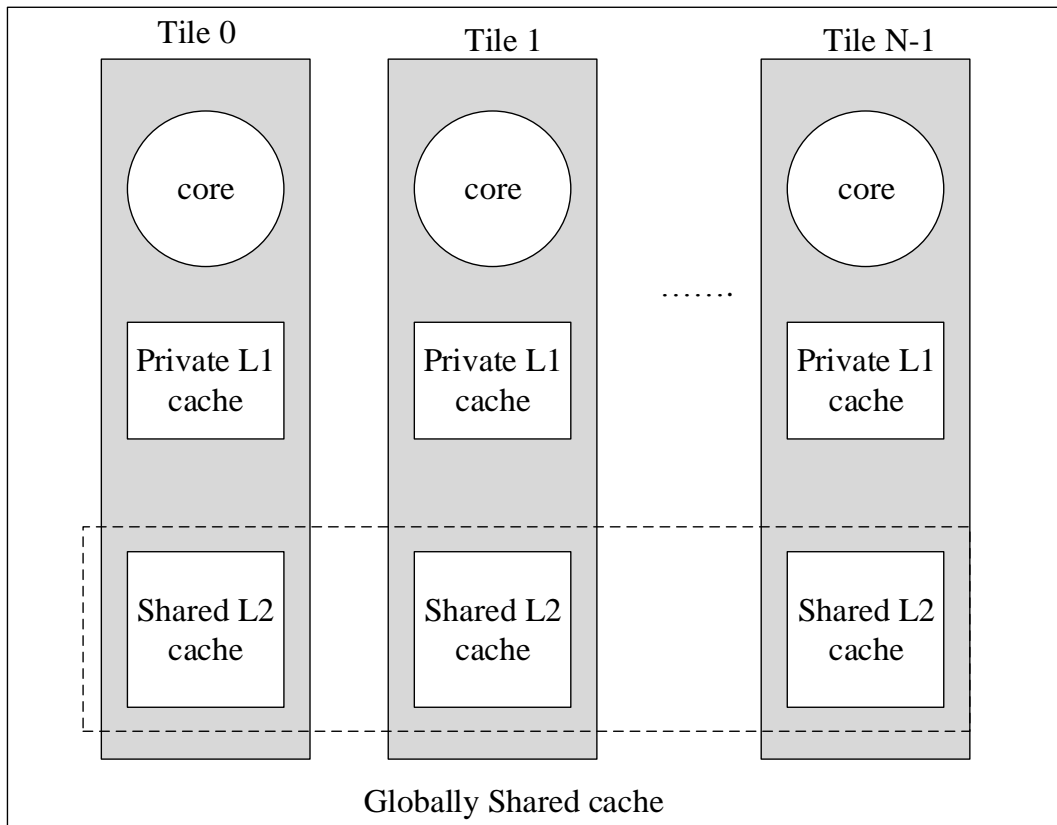


Figure 5.6: Age based flits priority

### 5.6 TCMP Router design

TCMPs provide the architectural backbone for high end embedded systems and smart IoT devices. TCMPs used in the handled device such as mobile phones to servers of the complex data centers. These systems gets designed are the fundamental challenges, to employ policies for utilization of efficient of the resources which was shared. Previous research has found that normal multi-processor workloads use very little NoC resources, with the rate of an average injection of about 5% [115]. The under utilization resources of

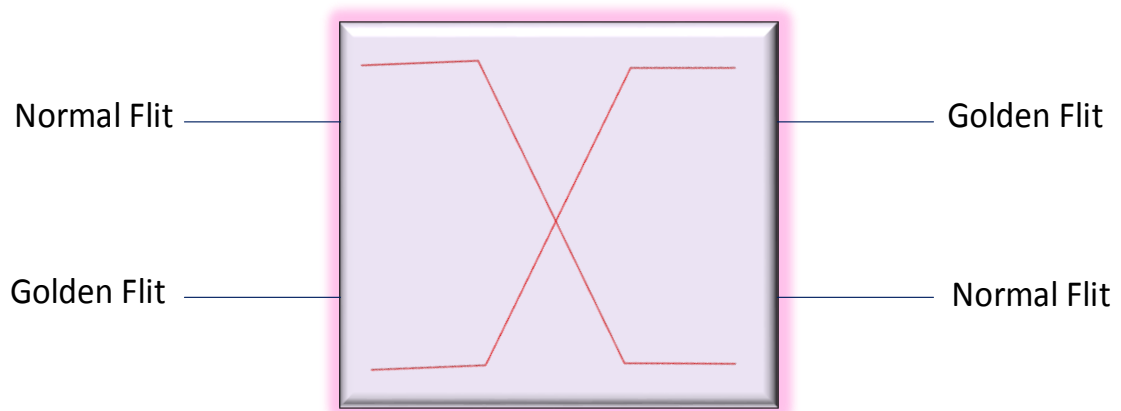
NoC and their ensuing use other kind of on-chip operations is a research potential subject to investigate. Figure 5.7 represents the design of TCMP architecture.



**Figure 5.7: Architecture of TCMP**

### 5.7 Concept of Golden Flit

Golden flits must get routed in a systematic way. It can utilize allocation of the parallel port rather than allocation of series port, also no need a sorting circuit in golden flit concept. As illustrated in Figure 5.8 in a two input port NoC, the winner flit which is golden is assigned the productive port while normal flit is being deflected.



**Figure 5.8: Golden Flit Technique**

## 5.8 Concept of BBUS

By inserting the desired flits inside the intermediately positioned routers, in flits conflicts may be avoided [116]. In CHIPPER the design with free of live lock to the Golden package principle. Within CHIPPER based NoC, clock synchronization is strictly adhered to. The architectures clock gating block reduces power consumption [117]. Golden epoch cycles must be understood by all NoC routers in order to avoid golden packets. At end terminals, buses are being employed to transmit recent golden epochs. Both asynchronous and synchronous bus concepts can be used in simulation. Two alternative strategies [118] can be used to establish synchronization within the clock period. The first method is to add the target address of port coding to the bus. The inclusion of a hardware component of new known as Golden Period Terminator is another method. The golden period terminator component only can adjust the routers present role in the bus. Flits do not collide and so synchronization is established. VHDL programming language is used to analyze the network.

## 5.9 Latency and Pattern

Injection is the method through which tile of local generates a packet of new and injects it into a port of local. Ejection is the process of transferring a packet from a router to a tile. 8x8 Mesh NoC, routing of XY, 1 cycle link and 3 cycle router have all been studied. Source is assigned to packets P1, P2, P3 from 6, 24, and 50 respectively. Each cycle of ejection and injection is examined. The CHIPPER router uses golden packets [119]. Table 5.4 denotes transpose pattern. Two types of traffic patterns which are transpose and bitrev or bit compliment traffic are used. Table 5.5 indicates XY Routing topology of a 8x8 Mesh NoC. Equation No 5.1 denotes Packet Latency.

$$\text{Packet Latency} = (\text{hops} \times 4) + 4 \quad (5.1)$$

**Table 5.4: Traffic Patterns and Packet Latency**

Packet Number	S	D_bitrev	Latency	D-trans	Latency
P1	6	57	$12 \times 4 + 4 = 52$	48	$12 \times 4 + 4 = 52$
P2	24	39	$8 \times 4 + 4 = 36$	3	$6 \times 4 + 4 = 28$
P3	50	13	$8 \times 4 + 4 = 36$	22	$8 \times 4 + 4 = 36$

**Table 5.5: Mesh NoC Topology with XY Routing (8x8)**

	56	57	58	59	60	61	62	63
↑	48	49	50	51	52	53	54	55
	40	41	42	43	44	45	46	47
	32	33	34	35	36	37	38	39
	24	25	26	27	28	29	30	31
	16	17	18	19	20	21	22	23
	8	9	10	11	12	13	14	15
←	0	1	2	3	4	5	6	7

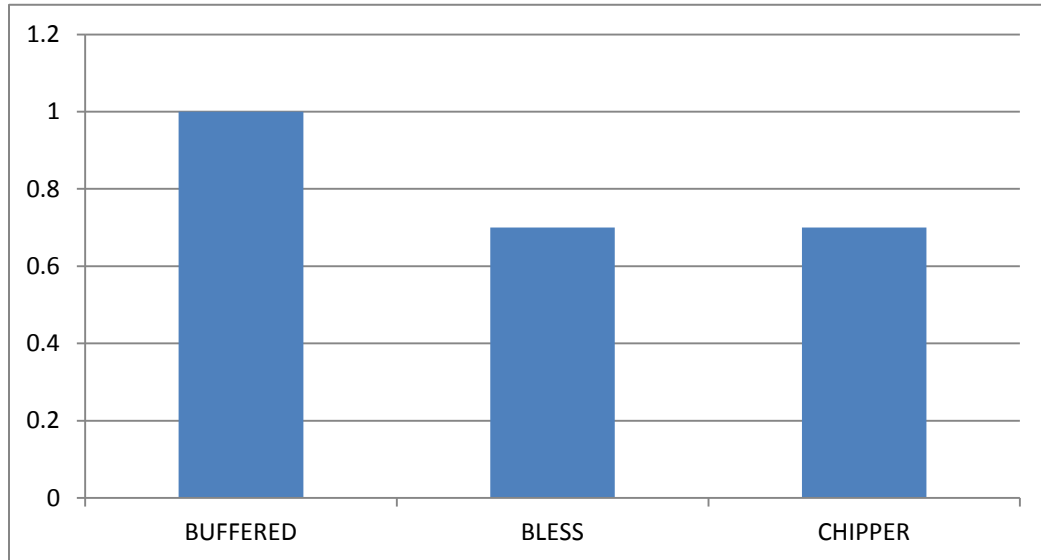
### 5.10 Analysis of CHIPPER router performance

CHIPPERs advanced version has a lower deflection rate and latency than the standard VC router design. The CHIPPER router decreases the area of normalized router by 36.2% when compared with a standard VC buffer router. Rather of using sequential port allocation we are using permutation deflection logic which is a parallel port allocation method. Figure 5.9 and Figure 5.10 denotes Analysis of Normalized Area of Router and Normalized Critical path respectively.



**a. Normalized Router Area**

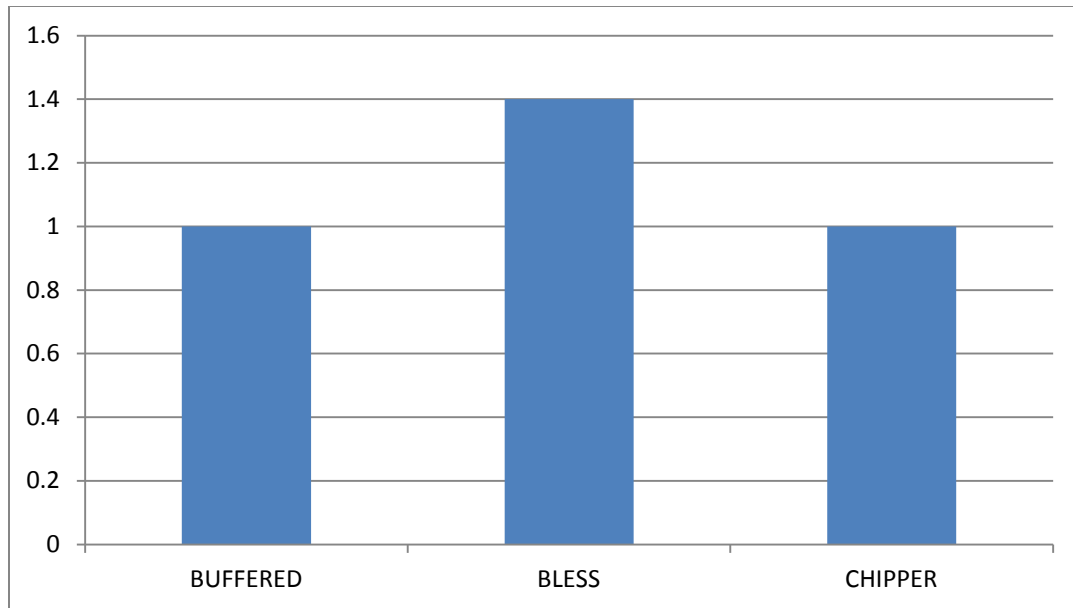
CHIPPER router decreases router area when compared with conventional buffered router by 36.2%. In this case concept is switched towards parallel port rather than using sequential port.



**Figure 5.9: Analysis of Normalized Router Area**

**b. Normalized Critical Path**

CHIPPER router decreases critical path normalized by 29.1% when compared to BLESS router while being nearly identical to a standard buffered router.



**Figure 5.10: Analysis of Normalized Critical path**

## 5.11 Experimental outcomes

The Mesh topology utilized is  $8 \times 8$  Mesh. The concept of Golden epoch explains how to restructure overworked nodes to generate better parameters [120]. Figure 5.11 depicts the simulation analysis of golden epoch rate for Mesh/Torus. Figure 5.12 illustrates the assessment outputs of golden flit rate of BBUS and CHIPPER for Mesh/Torus topology. The golden flutter rate of ejection is used to compare CHIPPER with BBUS. As observed from the data the Golden Epoch packet passing rate is unaffected by injection rate. Golden Epoch is created in MESH for 18 cycles of clock for Chipper while it requires 12 cycles of clock in TORUS. However, the golden epoch rate of BBUS is nearly one per clock cycle while the injection rate is very small. In Mesh topology, the golden flit rate of BBUS is two times higher as compared CHIPPER. Also BBUS enhanced its performance in Torus as compared to Mesh.

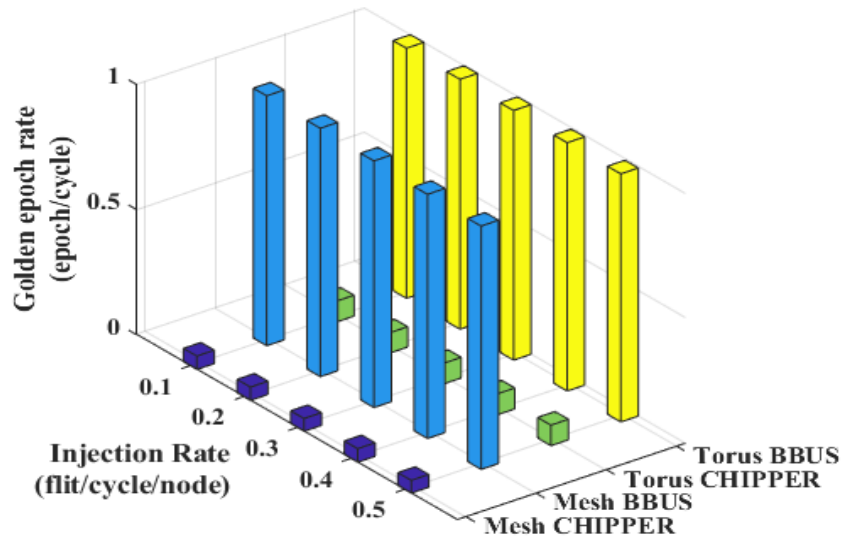
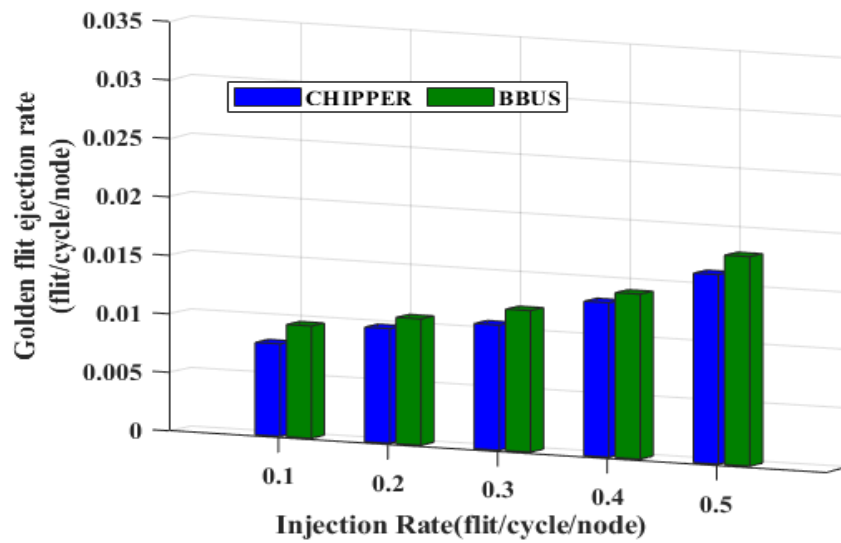
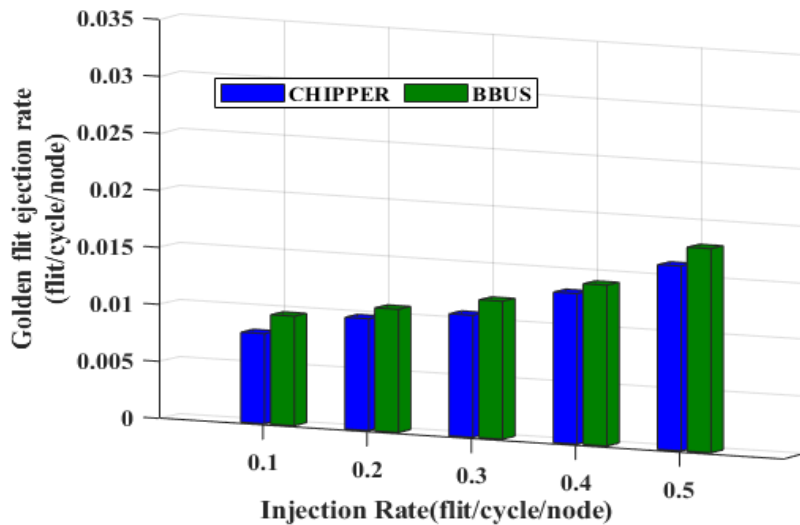


Figure 5.11: Golden epoch Rate of Mesh/Torus Topology



(a)



(b)

**Figure 5.12: Injection Rate (a) Torus Topology (b) Mesh Topology**

Comparison to CHIPPER, pointing the chance of larger flits of golden is substantially higher in BBUS. Particular time necessary for the flits to achieve golden epoch is supplied by both BBUS and CHIPPER approaches. Hardware Description Language is utilized in conjunction along with a conventional FPGA board for a realistic approach. Four bits represent the number of packets allotted to them. Both the input source and output addresses of destination have bits of six each of them representing rows and columns. The topologies of the  $8 \times 8$  Mesh and  $8 \times 8$  Torus are compared [121]. Pseudorandom numbering is used to choose both the source and the destination. In compared to CHIPPER, when injection flits are low, the amount of deflected packets in BBUS is 0. However, when the rate of injection raises, the number of packets increases exponentially in both circumstances. At last, when compared with the experimental data BBUS outperforms CHIPPER by a wide margin. Packets of Golden can be upgraded to some of the adaptive connectivity to live lock improvement in the system. The Cadence

tool is used to examine the transistors parameters that are not in use, also Cadence is used in designing of ICs, SoCs and PCBs [122].

## 5.12 Drawback in BBUS

Other flits are deflected in BBUS owing to Golden packets, which affects throughput compared with CHIPPER because the injection rate is quiet low. Due to additional GPT parameter and couple of lines of buses, increases the extent of design by 6% in a router for 32 bit bus. Across whole router architecture, the area overhead for 128 bit bus is decreased by 1.8%.

## 5.13 Zero Load Latency Review

The Zero Load latency (ZLL) determines latency of any operation any variance. ZLL mathematical analysis depends upon add on latency  $L_{NIi}$  which determined the initiator and  $L_{NIit}$  which determines the target [123]. The add on latency by NoC is denoted by  $L_{NoC}$ .  $L_{AHBM}$  denotes master while  $L_{AHBS}$  denotes the slave which is shown in Equation No.5.2

$$ZLL = L_{NIi} + L_{NIit} + L_{NoC} + L_{AHBM} + L_{AHBS} \quad (5.2)$$

For Fast track NoC the  $ZLL_{NoC}$  can be calculated as shown in Equation No.5.3

$$ZLL_{NoC} = 1 + hops + hops_{turn} + N \text{ clock cycles} \quad (5.3)$$

In above equation hops refer the routers count through which a packet travels in straight direction, +  $hops_{turn}$  is the packet flit turns while indicates total number of flits [124].

In proposed work in this paper every flit latency is equal to combined latency of each flit. In this case only first flit adds latency in entire operation while remaining flits are transferred in the NI block. Hence the final equation becomes as shown in Equation No.5.4

$$ZLL_{NoC} = 1 + 1 + 0 + 1 = 3 \text{ clock cycles} \quad (5.4)$$

### ***ZLL for Single Write Operation***

NI block adds a null latency for 3 flits of the packets. To enter and leave the NoC the first packet requires 3 clock cycles. One clock cycle is needed by target flit for saving head flit in a Virtual Channel buffer while extra clock cycle is needed up to body flit comes along the bus address [125]. Lastly AHB slave to finish the operation and to raise the HREADY signal two additional cycle of latency is added. The single write operation details is mentioned in Equation No.5.5. Parameters calculated are denoted in Table No.5.6.

$$ZLL_{NoC\_W} = 0 + 2 + 3 + 0 + 2 = 7 \text{ clock cycles} \quad (5.5)$$

**Table 5.6: ZLL Calculation for Single Write Operations**

<b>Cores Count</b>	<b>NoC (ZLLns)</b>	<b>BUS (ZLL ns)</b>
4	2.8	0.8
8	2.8	1.2
16	2.8	1.6
32	2.8	2

### ***ZLL for Single Read Operation***

No latency is added by the initiator. The packet head wanders NoC in next 3 clock cycles. NI run through 2 cycles again till address reaches the AMBA slave. Until the results are generated in HRDATA two more cycles are required [126]. To oblique the NoC packets needs three added cycles. The flit will reach the master after 1 clock cycle and is saved through Virtual Channel Buffer. The single read operation details are mentioned in Equation No.5.6. Parameters calculated are denoted in Table No.5.7

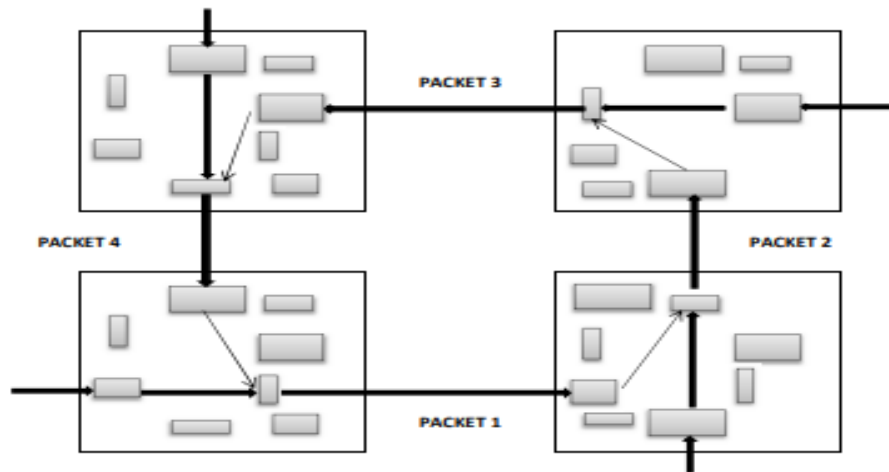
$$ZLL_{NoC\_R} = 0 + 3 + 2 + 2 + 3 + 1 = 11 \text{ clock cycles} \quad (5.6)$$

**Table 5.7: ZLL Calculation for Single Read Operations**

Cores Count	NoC (ZLLns)	BUS (ZLL ns)
4	4.8	0.8
8	4.8	1.2
16	4.8	1.6
32	4.8	2

### 5.14 Concept of Deadlock and Live lock

- Dead lock:** Deadlock is a term where a bunch of flits are unanimously waiting for each other. There is no forward progress that we can make which is created by circular dependencies via resources [127]. Flit waits for a buffer occupied by another packet subsequent. Dimension order routing is used to resolve deadlocks. Figure 5.13 indicates Deadlock concept.



**Figure 5.13: Deadlock Concept**

- **Live lock:** Live lock occurs when a packets never reaches to its destination even though it is routed. The packet travels around the loop but does not find path to reach its destination. Live lock problem majorly occurs due to output Virtual Channel (VCs) are by mistake occupied by other packets [128]. Here the packets follows non minimal path. To avoid the issues, live lock avoidance algorithm is the key concept. This algorithm when used along with Route Computation (RC) checks for live lock avoidance and verifies if the path is live lock free or not. The Live lock is a special case of resource starvation.

### **5.15 Summary of the Chapter**

The lowering of cycle time is a low cost strategy for improving the NoC router performance. The routers latency is greatly decreased without compromising its efficiency. The usage of deflection network of permutation which employs output port of parallel allocation reduces average flit latency of CHIPPER when compared to traditional buffer less routers. The CHIPPER routers normalized critical path and normalized router areas have been lowered by 29.1% and 36.2 % respectively. In CHIPPER, there is little lag and the connection regions are saved. In addition, in compared to CHIPPER the proposed BBUS has a much shorter packet waiting duration. In BBUS, the Golden epoch era is significantly superior. As injection rate exceeds 0.5 node/flit, proposed BBUS approach also maintains the lowest average packet delay. When compared to the CHIPPER, it retains the same increased performance. When nodes demand a diversified quantity of packets before to data processing, the suggested BBUS approach may be convincingly implemented. High quality work leads to better results. The suggested approach allows for the creation of multi core processors.



## CHAPTER-6

### CONCLUSION APPLICATIONS AND FUTURE SCOPE

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This research work explains the improvising performance level of NoC, with the help of routers. Detailed explanations are briefed about the techniques which are used, implemented, and resulted in improving the performance level of NoC in the following conclusion part. It also explains the future scopes and applications of these techniques.

#### 6.1 Conclusion

As Network on chip connects the components of memory and processors it has become a key element in router design in recent years. In comparison to bus-based architectures, NoC is a preferable solution. NoC lowers the number of wires required to route data in SoC which reduces congestion in routing. It delivers low scalability, low power, and low latency among on-chip connected computing components. The classic SoC has been replaced with NoCs. It is a more efficient way of allowing multi-core CPUs to communicate. In NoC, topology design is incredibly crucial. Throughput, latency, hop counts, injection rate, and minimum chip area are all factors that affect network performance. For smooth and effective interaction between IPs, NoC is required. Various parameters of performance analysis of NoC for the variety of topologies are explained in this thesis. Routing algorithm includes adaptive and non-adaptive algorithm routing. Adaptive algorithm routing includes isolated, distributed, and centralized are explained under algorithm routing. Non-adaptive algorithm routing includes the random and flooding walk. The router architecture of 3D torus for network efficiency on the design of the chip, 3D X torus topology is explained and router architecture includes buffer, VC conventional router, controller paths, and arbiter are considered as well as explained as design parameters of router. There are only a few algorithms that are acceptable for the 3D torus topology, allowing academics the opportunity to build a viable method for high

processing. To minimize deadlocks and live locks in the system, the 3D torus router architecture employs VC and VCT switching. In terms of LUTs, the proposed router architecture for 3D torus is efficient.

The NoC router functionalities include BW, VA, SA, ST, and RC as an NoC router pipeline is explained. The deflection routing idea has been proposed to solve the design complications, Dynamic, Static power utilization difficulties for regular Virtual Channel depending on routers. Researchers have developed buffer less and smallest buffer routers to reduce extra power consumption and design space. The specifics of TCMP and CHIPPER router parameters are presented in this work. The router structure of NoC in Mesh topology,  $4 \times 4$  Mesh NoC packet flow structure,  $5 \times 5$  square topology 25 core machines are explained. In deflection routing of buffer less, when two of the packets compete for the same connection, the buffer less deflection router gives one of the packets required link while the packet of second is deflected. If it does not have buffers, the networks get saturated quickly, which was represented in the Golden epoch parameters table.

The routing concept of BLESS, requesting of flits, flits priority of age-based and TCMP router design are explained. Golden flits and BBUS concepts are discussed; golden flits must be routed systematically and it illustrates the input NoC two port, the triumphant flit is golden, and it is assigned to the port of selected, while the deflection of normal flit. The transpose pattern, analysis of CHIPPER router performance by normalized router area, and normalized critical path are explained. Experimental outcomes of ejection rate in the topology of mesh and ejection rate in the topology of Torus of the graph results are discussed. The lowering of cycle time is a low-cost strategy for improving the NoC router performance. The router's latency is greatly decreased without compromising its efficiency. The CHIPPER routers normalized critical path and normalized router areas have been lowered by 29.1% and 36.2 % respectively.

On-chip area possession for the proposed architecture must be minimized so as to increase the system performance. A control for elastic buffer mechanism is utilized in the

architecture of router to eliminate the expense of buffers. This system proposes a low-power NoC router architecture related to simple pass routing using UFDQ and IRR to produce a power-efficient router design. UFDQ and IRR are used in this system to improve the input port modules and easy pass routing of the router architecture. The power consumption, router hardware overhead, and critical path delay are significantly enhanced. To address these concerns, UFDQ is presented as a way to boost router performance. UFDQ improves router performance at varied injection rates while consuming less power. Power efficient VC routers for NoCs on chips network concepts and the architecture of NoC routers are all discussed. The router pipeline of the router makes use of pipeline optimizations like SSA and LRC. The computation of the route, allocation of the VC as well as cross bar is briefly explained. It requires 41.05% low combinational elements and 75 % low registers as compared to the RoR arbiter for 16-bit input formation. The chip layout of this IRR design is so simple due to the requirement of less number of registers and simpler clock tree association. Bypass router which includes the network interface, input ports, sleep status, and output port are explained as EZ pass router architecture. Power gating of NoC routers includes CBCF, DT, Break-even time, BPG, UBPG, and wake-up latency are explained. Using IRR arbiter design is proposed which enables a served priority system in the least recently to ensure arbitration of strong fairness, since arbiter of IRR is proposed in EZ-pass architecture to direct the EZ control flit to NI. It also includes the grant index of the wormhole NoC network, fixed and variable priority arbiter, and IRR arbiter, and their functional behavior is also explained. Rapid dynamic queue input ports in EZ pass router architecture are discussed with the brief procedure. The experimental results show that the IRR-EZ pass switch consumes 11% less power as compared to VC router with UFDQ for 4x4 Mesh topology. The latency of the proposed structure is 74.48 % less in accordance with VC router while assuming the rate of injection as 0.004 flits for sporadic traffic. In sporadic traffic mode while the rate of injection is 0.01 flits through put of VC-Router is about 25% and the IRR-EZ-Pass router throughput is 90%. In the low traffic mode while the injection rate is 0.005 flits/time/unit the through put of the VC-Router is about 20% and the IRR-EZ-Pass

router throughput is 80%. The results indicate that the throughput IRR-EZ-Pass router is better with respect to Virtual Channel Router during low as well as sporadic flit traffic modes.

## **6.2 Applications of the Proposed Architecture**

NoCs are quickly becoming the industry standard for linking cores, caches, and memory controllers on processors. Multi-core processors now feature hundreds of cores, with thousands of cores expected in the future. Machine learning and multimedia applications have been widely deployed on many fundamental systems. Many of these are RMS applications (recognition, mining, and synthesis). The request and reply packets make up NoC traffic, which is made up of routers and connections. Additionally, as the number of apps operating on 4x4 grows, NoC creates greater network traffic. The NoC traffic will be lowered when the number of apps operating on 4x4 NoC is reduced. These applications however have no gold outcomes. As a result, the suggested architecture may be used to make trade-offs between accuracy and other parameters like area analysis and power detection and implementation time. It combines a traditional router for high volume traffic with an Easy-Pass switch for occasional and very less traffic. In terms of space, latency, and power it also beats the present EZ-pass switch. As a result, the suggested structure applies to a wide range of pattern recognition, image processing, and scientific computing tasks. NoCs can be used in wireless base stations, mobile handsets, HDTV, and HD set-top boxes. Also, NoC applications are used in cloud computing techniques.

## **6.3 Future scope**

The suggested design is utilized to concurrently lower the energy consumption and performance of the NoCs. The fundamental concept is based on the concept that routing packets travels via easy switching mechanism as compared to the complicated conventional routers which saves energy during less traffic. Even if the suggested NoC architecture's findings are satisfactory, additional study in this area is required to further

minimize network latency. This study focused solely on router architecture to increase performance related to of area usage, power, and latency. The NoC, on other hand, is made up of routers and connections, with the request and reply packets constituting NoC traffic. To manage high, sporadic, and low traffic modes, we developed several routing topologies. However, calculating the time it takes a packet to reach the asking tile does not minimize network traffic. Recent research further reveals that a variety of approximation computing theories like Image Processing, Artificial Intelligence, and Machine Learning may sustain minor inaccuracies but still produces valid results. The suggested NoC designs for the multi-core processors study are also made in this research work. The following are some prospective developments that might be added in future work based on the work given in this thesis:

- An advanced data compression technique approach for on-chip communication network will be developed to reduce data traffic overhead, data packet loss, latency, and energy consumption.
- To transfer data with adequate precision without wasting excessive power, the approximate communication architecture for NoCs will be considered.
- For improved flow management, the design might be expanded.
- Gating of power, Dynamic Voltage, and Scaling of Frequency are two methods that may be used in NoC design to minimize both static and dynamic power. Finally, bypass techniques may be employed to improve the performance of the network on chips without waking up the virtual channel of unused transistors.
- Future work in bypass channels of asynchronous for NoCs multi-synchronous will be centered on increasing network performance using lower latency synchronization approaches in the turn path and the logic control.
- Researches opinion in NoC routers low latency with the look-ahead bypass, ideal for future multi-core SoC architectures. We intend to investigate ways to allocate internal freeways under a variety of applications of the specific traffic for hot connection patterns in the future to minimize latency.

- To improve the cost model, other metrics will be introduced, such as performance and energy in reliability mapping aware for various topologies of NoC and algorithms routing under limitations of performance. As a result, a full cost model for a trade-off between energy, dependability, and performance might be built as a future inquiry.
- Researchers want to compare the suggested techniques of heterogeneous as well as hybrid cluster topology for NoC to other current NoC topologies such as a fat tree, torus, hypercube, and so on in a future studies. The analytical modeling of the suggested technique will also be discussed as part of this research's future effort.
- Researchers exclusively investigate the transmission of error in links of inter-router in the study of a framework of holistic design for efficient energy and communication of reliable on-chip for many cores. They will look into errors in LUT, NI, and Routing Algorithms to make the system more reliable in the future.
- Researchers have a wide range of scope to study waveguides through ONoC (Optical Network on Chip)

## **6.4 Benefits to Society**

- NoC has replaced global wire connections around a chip with intelligent network architecture.
- Conventional wired communication is changed with packet communication. Network-based topology has replaced the conventional sharing bus method in SoC.
- NoC concept can be used as infrastructure development in upcoming 5G technology.
- NoC technology can also be used in Carbon Nano-tube (CNT) based, photonic waveguide-based, Wireless, and 3D on-chip communication architectures.
- NoCs can solve complex on-chip communication problems.

## **PUBLICATION DETAILS**

### **JOURNAL PUBLICATIONS**

- [1] Ashish Mulajkar, Sanjeet K Sinha & Govind Singh Patel (2021) “ANALYSIS OF IMPROVED EZ-PASS ROUTER DESIGN AND ITS FPGA IMPLEMENTATION”, *Harbin Gongye Daxue Xuebao/Journal of Harbin Institute of Technology*, 53(12), 16–27 (Scopus Indexed SJR 0.2)

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- [2] Ashish Mulajkar & Govind Singh Patel, “VC Router Design For Power Efficient Network On Chips”, *JETIR*, Vol. 6, No.1, pp.1400-1403, January 2019 (UGC Journal)

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- [5] Ashish Mulajkar, Sanjeet K Sinha & Govind Singh Patel (Feb 2022), “Emerging Trends in Network on Chip Design for Low Latency and Enhanced Throughput Applications”, *International Conference on Materials for Emerging Technologies (ICMET-21)*, February 18-19 2022, LPU, Punjab  
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<https://www.taylorfrancis.com/chapters/oa-edit/10.1201/9781003129103-8/single-cycle-low-latency-bypass-router-based-network-chip-ashish-mulajkar-govind-singh-patel>

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