DESIGN AND PERFORMANCE EVALUATION OF GATE ENGINEERED DOUBLE GATE JUNCTIONLESS MOSFET STRUCTURE FOR LOW POWER APPLICATIONS

Thesis Submitted For the Award of the Degree of

DOCTOR OF PHILOSOPHY

in

Electronics and Communication Engineering

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2022

DECLARATION

I hereby declare that the thesis entitled "Design and Performance Evaluation of Gate Engineered Double Gate Junctionless MOSFET Structure Low Power Applications " is submitted by me for the Degree of Doctor of Philosophy in Electronics and Communication Engineering is the result of my original and independent research work carried out under the guidance of Supervisor Dr. Suman Lata Tripathi and Co-Supervisor Dr. Sweta Chander , Professor, Lovely Professional University, Punjab. It has not been submitted for the award of any degree, diploma, associateship, fellowship of any University or Institution.

Place: Phagwara
Date: 24/08/2022

Signature of the Candidate

CERTIFICATE

This thesis entitled "Design and Performance Evaluation of Gate Engineered Double Gate Junctionless MOSFET Structure Low Power Applications" submitted by Namrata Mendiratta of Lovely Professional University is a record of bona fide research work done by her and it has not been submitted for the award of any degree, diploma, associate ship, fellowship of any University/Institution.

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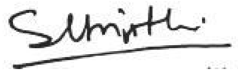

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ABSTRACT

The performance of conventional MOSFETs is good when its channel length exceeds 100 nm. Semiconductor sizes are shrinking all the time, and have now reached the nanoscale range. Because the size of MOSFETs is shrinking, the amount of transistors increases twice every two years. When the MOSFETs size is reduced, the channel length is reduced, resulting in short channel effects and increased leakage of the current. Short channel effects have been caused by the shrinking of semiconductor devices (SCEs). Parasitic capacitances, drain-induced barrier lowering, mobility degradation, and hot carrier effects are only a few of the short channel effects. Devices must be constructed utilising various approaches like as gate engineering and channel engineering to mitigate these effects. Due to extension of breadth of the drain barrier into the drain and the source area barrier lowers, SCEs occur. Many MOSFETs structures have been created to overcome SCEs, including gate all around MOSFETs, double gate MOSFETs , triple gate MOSFETs, SOI MOSFETs & double step buried oxide MOSFETs. The advantages of a double gate MOSFETs over a bulk MOSFETs are numerous. Short channel effects and junction capacitance are reduced. It also offers SOI dielectric isolation (silicon on insulator). It is also employed in CMOS technology as it has speed of performance is high and the power usage is low.

Memory is also stored using MOSFETs and is utilised to make SRAM cells, which are used to store data. For low power applications, an asymmetrical junctionless dopingless (AJ) double gate (DG) MOSFETs, with an 18 nm channel length has been proposed to decrease short channel effects (SCEs). The transistor's main goal is to achieve a desired ON/OFF state current ratio while keeping subthreshold performance characteristics within limits. Various parameters affecting the sensitivity of dopingless AJ DG MOSFETs, such as drain extension and channel lengthgate overlapping and oxide thickness of the AJ DG MOSFET with doped channel region are compared.The ON state current achieved was 3.80 x 10^6 A/m, with an leakage current decrease of up to 1.37 x10^{17} A/m. The suggested device's SS & DIBL are 59.5 $mV/decade$ and 10.5 mV/V, respectively. A nanogap

cavity area is inserted at the gate-oxide interface to create a strongly doped n+ pocket AJ MOSFET for its applications in biomedical . The nanogap cavity region is placed in such a way that when the biomolecules existing in the cavity region are changed, the device demonstrates sensitivity. The research is centred on dielectric modulation, or changes in dielectric properties caused by biomolecule variations in the human body and environment. For the examination of asymmetrical junctionless double-gate MOSFETs, several gate oxide materials such as SiO_2 and HfO_2 are employed, as well as diverse gate contact materials such as aluminium, copper, and polysilicon (AJDG-MOSFET). Temperature analysis was carried out at temperatures of 250 K, 300 K, 350 K, and 400 K. When temperature increases, increase in the OFF state current or the leakage current is observed. The surface potential of an AJDG MOSFET with a channel length of 18 nm and a gate length of 11 nm is calculated using solutions derived from 2-D Poisson's equations. The suggested device is split into three pieces, with the first two acting as single gate MOSFETs and the third acting as a double gate MOSFET. The surface potential calculated using a mathematical model is verified using simulation data.

OBJECTIVES

- To design a double gate junctionless MOSFET by applying gate and channel engineering with the variation in material, dimensions and doping level.
- Suppressing Short Channel Effects (SCEs) for MOSFET below 20 nm technology.
- To derive and analyse the capacitive model of the proposed device structure.
- To design SRAM cell with the help of proposed nMOSFET and pMOSFET structure for low power applications

ACKOWLEGMENT

First and foremost, I am thankful to almighty for making things possible at the right time. I owe my success to my supervisor and would like to sincerely thank Dr. Suman Lata Tripathi and co-supervisor Dr. Sweta Chander for their guidance. I greatly appreciate his support, positive attitude, and their vast knowledge in a wide range of topics. Their guidance not only in terms of giving ideas and solving research problems, but also in terms of giving freedom to do research in my own way has proved to be useful and invaluable. I am deeply influenced by my supervisor's way of guidance and sincerely thankful for standing by my side in tough times. I would like to thank my husband Sidharth Sharma, for his unconditional love, support and encouragement. Last but not least, I would like to thank my family (especially my mother and father) and my friends for their continuous love and support. Finally, special thanks to all the people who helped me in direct and indirect ways to accomplish this work.

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LIST OF ABBRIVATIONS

MOSFET	Metal oxide field effective transistor
SG	Single gate
DG	Double gate
SCE	Short channel effect
SRAM	Static random access memory
2-D	2-dimensional
3-D	3-dimensional
SOI	Silicon on inductor
CMOS	Complementary metal-oxide semiconductor
GAA	Gate all around
RF	Radio Frequency
TM	Triple material
DM	Dual material
JL	Junctionless
SS	Subthreshold slope
DIBL	Drain induced barrier lowering
FET	Field effective transistor
AJ	Asymmetrical junctionless
DSBO	Double step buried oxide
BP	Black phosphorus
RC	Recessed channel
GC	Graded channel

CHAPTER 1

INTRODUCTION

1.1 Evolution of VLSI

In 1947, the introduction of the bipolar transistor took place, the growth being very positive in the semiconductor industry with a social impact. Significant growth in the semiconductor industry in high-resolution (VLSI) integration technology is observed. And this huge growth in VLSI technology has led to the creation of smaller transistors in much smaller sizes. The advantages of having greater packing density, high rotation speed and , low power dispersion are important features of the evolutionary process, leading to the development of modern computers and high-performance communication systems, combined size at a much-reduced cost compared to the previous ones. Global investment in the semiconductor industry will continue as long as tangible terms will be agreed [1]. Bipolar transistor technology was developed in early 1947 and used in the first integrated circuit memory on mainframe computers in 1958. However, the severe power dissipation of bipolar circuits had significantly reduced their integration rate, by approximately 104 circuits per chip. MOSFET on a silicon substrate containing SiO_2 as a gate guard was developed Kahng and Atalla in 1960 [2]. During the 1960's and 1970's n-channel and p-channel MOSFETs were widely used along with bipolar transistors. In 1963, a major breakthrough in the integration phase occurred with the introduction of Complementary Metal Oxide Semiconductor (CMOS) technology by Wanlass and Sah 1963. Frank Wanlass patented CMOS in 1967. In CMOS architecture, both n-channel and p-channel MOSFETs are built together in the same substrate. Another feature of CMOS devices is their high noise protection. Since a single pairing transistor is always turned off, the series combination draws only a significant momentary moments during switching between opening and closing circuits (logical transition of the train line to the train)[3].

As a result, CMOS devices provide high packing density, fast rotation speed, low power dissipation and do not release much waste heat as other types of concepts do such as Transistor Transistor Logic (TTL) or NMOS logic. Therefore, CMOS technology is used to design microprocessors, microcontroller, static RAM and other digital logic circuits. Finally a single transistor DRAM (Dynamic Random Access Memory) cell and microprocessor were developed in 1968 and 1971 respectively. The emergence of VLSI applications occurred in the 1980's .For more than two decades of uninterrupted measurement, CMOS technology has become an existing technology for Very Large Scale Integration (VLSI) applications. These advances have led to more efficient computers and networks and lower costs per capita. Even more significant is the speed at which the reduction of the transistor size is used in order to obtain more instructions for improving performance and reducing costs.

1.2 Moore's law

The law was coined by Intel founder Gordon E. Moore, who described the trend of the number of transistors in integrated circuits compared to the launch year. Moore in 1965 "stated that the amount of units in IC doubled a year from the establishment of an integrated circuit in 1958 until 1965 and predicted that this trend would continue at least ten years"[4]. This doubling was based on 50-60 parts chips produced in 1965 compared to those produced in previous years. Moore in 1975 saw that their predictions proved to be incredibly accurate. However, they predicted that in the future the number of parts of each chip would need about two years to double rather than one year as shown in figure 1.1[5].

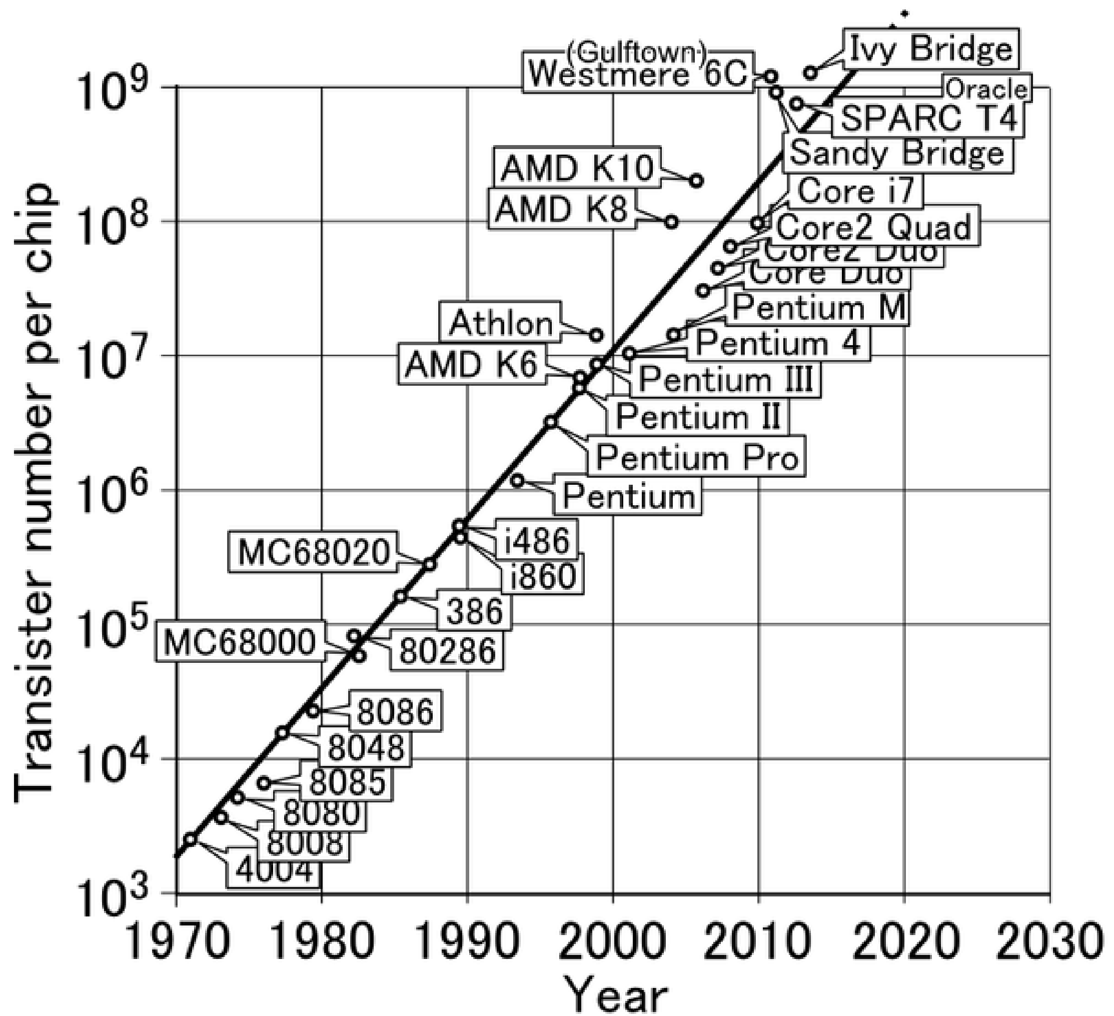


Figure 1.1: Moore's Law

1.3 Basics of MOSFET

MOSFET (metal oxide field effective transistor) is a three terminal device having an insulated gate where voltage controls the flow of current in the device shown in figure 1.2. It is used for switching and amplification of electronic signals[6]. There are three different operation regions in MOSFET , the cut – off region , the triode or linear region and the saturation region. Cut-off region is used as switch OFF. In this region the voltage of gate to source (V_{gs})is always below than the threshold voltage of the device (V_{th})and current does not flows in this region between Drain to Source i.e. $I_d = 0$.Triode region is used for

switching ON . The voltage of gate − source V_{gs} is above the threshold voltage V_{th} and voltage between drain to source V_{ds} is less than the saturation voltage. The current flows from drain to source in this region. Saturation region is used in Amplifier. When the voltage between drain to source is increased and we meet a point on the graph $V_{ds} > V_{gs} - V_{th}$ which is called saturation region and the current does not depends on V_{ds} [2].

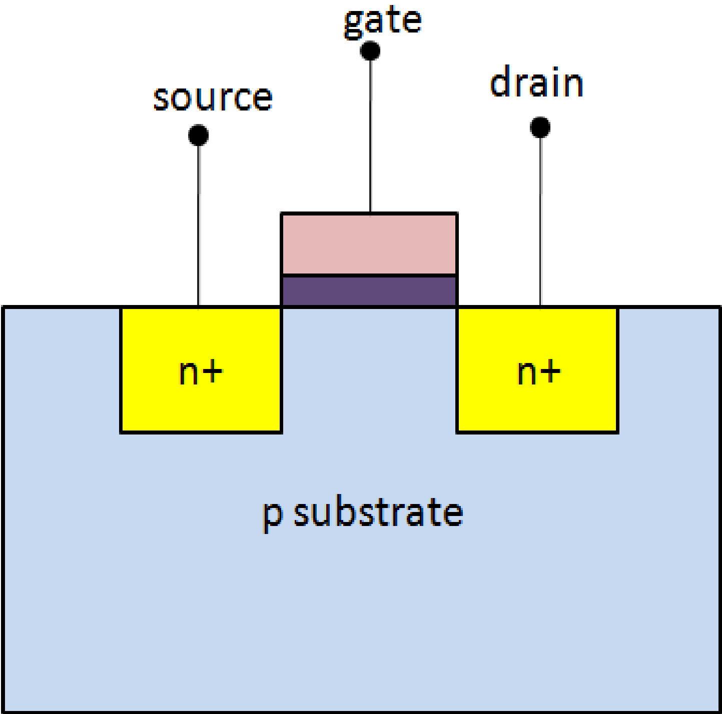


Figure 1.2 : Single gate MOSFET

1.4 Basic operating principle of MOSFET

When positive voltage at the gate terminal is applied, the minority charge carriers (electrons) present in the P substrate is attracted towards the gate and gets accumulated on the gate contact which forms a conductive bridge between the two n+ regions known as channel [7]. Depending upon the strength of the gate voltage applied the number of free electrons accumulates at the gate contact. If the applied voltage is higher the width of

the n-channel formed due to electron accumulation is also greater, therefore the conductivity of the device increases eventually and the drain current (I_D) starts to flowing between the source and drain. In DG MOSFET two gates are used to control the channel from both sides[8].

1.5 Need and challenges

Reduction in the size of the MOSFETs is one of the biggest challenges in IC technology[3]. Scaling of the device is important for integrating more number of transistors in a single chip. MOSFET scaling gives rise to short channel effects (SCEs) that degrades the performance of the MOSFET[4,5]. Single gate or conventional MOSFET does not works when the channel is short. MOSFET scaling decreases the size of SiO_2 to few nm, further reduction in size of SiO_2 is not feasible causing current leakage. There is the need to replace the oxide with high K material having more physical thickness[6]. Methods like channel & gate engineering are implemented to make changes in the structure for decreasing short channel effects (SCEs)[9-15]. An example of gate engineering technique is double gate MOSFET (DG MOSFET) which is one of the techniques for reducing SCEs .The gate to channel coupling is increased, control of gate over the channel gets better in DG MOSFET[16]. Current leakage due to OFF-state is minimized and also provides good mobility. The gates on both sides of the channel region of DG MOSFET controls the electric field and also provides a better subthreshold slope[17]. Hence, improving the performance of the device. Changing the gate contact material from metal to polysilicon also enhances MOSFET performance[18]. MOSFET has applications in various fields like biotechnology as a biosensor for detecting molecules and enzymes, memory application like SRAM cell, low power applications in digital circuits for switching[19-25].

This reduction in device size is important to integrate the maximum amount of devices into Integrated Circuits (ICs). The IC industry adheres to the Moore's Law to date. Today, the semiconductor industry also follows a road map provided by the International

Technology Roadmap for Semiconductor (ITRS) predicting future device sizes and the number of transistors in the IC based on Moore's law.

As a result of Moore's law, each year the length of the MOSFET channel decreases, resulting in Short Channel Effect (SCEs) . SCEs affect the power consumption of circuits. Transistor measurement target has been achieved due to improved lithographic ability to create a shorter / smaller channel. Initially, measurement was possible with conventional structures and material technology, but it is understandable that standard measurement technology could not continue indefinitely. Therefore, the investigation of non-antique device properties has been necessary. As the size of the transistors is reduced, the control of the gate electrode to the power flow in the channel area decreases due to the close proximity between ― source‖ and ―gate. A major problem related to the short channel effect is the reduction of the channel junction of the channel. Reduced gate control reduces fence transmission. Transconductance of a device is very important in its analog use. In the short-term device and transconductance, lowering the water-causing barrier, ballistic transmission by Short Channel Effects (SCEs) can affect device performance. The solution to all the problems lies in increasing the network connection between the gate and the station and the reduction of the electrical connection between the source / trash and the station. Normally, different effects of six short channels can be divided into Drain Induced Barrier Lowering (DIBL) ,Hot Electron Effect, Punch through ,Velocity Saturation ,Impact Ionization ,Surface scattering and Threshold voltage roll-off. As SCEs impose restrictions on device performance and performance of the device deteriorates, these effects should be suppressed or removed, so that a device with a relatively short channel length can maintain the necessary features of the device. Researchers have attempted to overcome these problems by reducing the oxide thickness of the gate and the depth of the spring / water source cross while lowering the gate length to normal MOSFETs. But this measurement has reached a body size limit. As a remedy, high-density dielectric gate materials were used. The use of these high-k materials as gate oxide allowed to achieve an equal thickness of oxide with a larger body size. But declining MOSFET at a sub 10 nm scale is challenging and new technologies were

needed. As per the ITRS predictions and published literature, it is understood that the main research was carried out in two different ways: the possible modification of the layout structure and the use of random 3D structure [26] to push its physical boundaries, or a new way of making transistors using nanomaterials and nanotechnologies such as silicon nanowires, carbon nanotubes or graphene, single electron transistors, and other emerging tools such as quantum cellular automata and spin-based electronics [27]

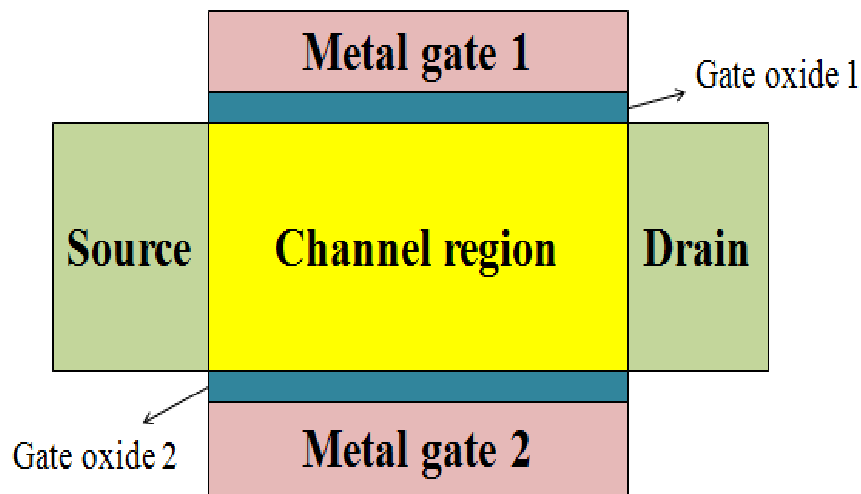


Figure 1.3 : Double gate (DG) MOSFET

1.6 Effects of MOSFET Scaling

1.6.1 Short channel Effects[26][31]

1. Drain – induced barrier lowering (DIBL)
2. Channel Length Modulation (CLM)
3. Punchthrough
4. Channel scattering
5. Velocity saturation
6. Hot carrier effect (HCE)
7. Impact ionization

8. Source/Drain parasitic resistance/capacitances
9. Mobility degradation
10. Gate to source/drain charge sharing
11. Fringing field effects

Drain-induced barrier lowering (DIBL)

DIBL (drain-induced barrier lowering) is a SCE in MOSFETs that indicates a reduction in the transistor's threshold voltage with increasing drain voltages. The channel's potential energy barrier for electrons is decreased. The drain induced barrier lowering (DIBL) happens when the gate length is lowered without the other dimensions being suitably scaled. At first look, the current stream in the channel is depends on creation and control of inversion layer. The electrons that are the carriers in the channel faces a potential barrier that obstructs the stream if the gate predisposition voltage is insufficient to change the surface (Vgs>Vth). The gate voltagewhen increased, lowers the potential barrier and, in the long term, allows the carrier stream effected by the channel electric field.

In a small size MOSFETs , the potential barrier is controlled as voltage between gate to source Vgs & voltage between drain-source Vds. As the drain voltage increases, the potential barrier becomes Channels are shrinking. Reduce potential barriers in the long run allows carriers (electrons) to enter the channel from the source. Generates an increase in drain current. This effect is kmown as drain induced barrier lowering.

Channel Length Modulation (CLM)

Channel Length Modulation (CLM) is to decrease the length of the inverted channel region while increasing the drain offset for large drain offsets. The result of CLM is that when the drain is biased, the current increases and the output impedance decreases. Channel length modulation in MOSFETs occurs due to an increase in the drain depletion layer width as the drain voltage increases as shown in figure 1.4. This shortens the channel length and increases the drain current. The effectiveness of channel length modulation is generally increased in small devices with few doped substrates. Proper

scaling can reduce channel length modulation, i.e. increasing doping density with decreasing gate length.

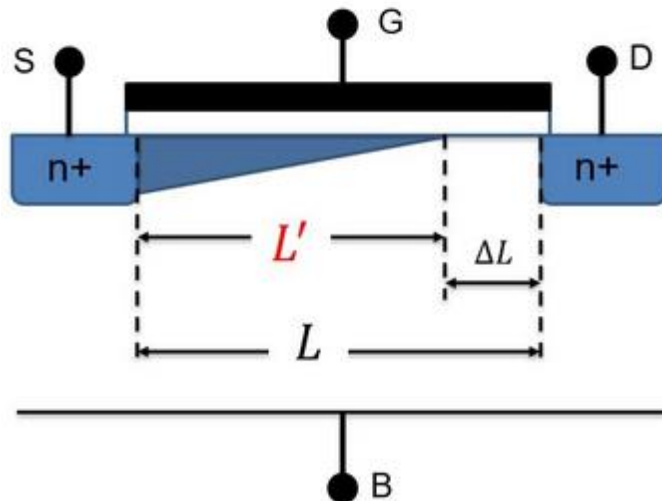


Figure 1.4 : Channel Length Modulation

Punchthrough

In a MOSFET, punchthrough is a case of channel length modulation in which the the drain and source are surrounded by depletion layer and converge into a single depletion zone. The field beneath the gate is then found to be strongly influenced by the drain source voltage. The drain surrounded by depletion zones stretch out to the source, the two depletion layers consolidate $(XdS + XdD = L)$ into a single depletion region, punchthrough occurs. More thinner oxides, larger substrate doping, shallower intersections, and channels with longer length can reduce punchthrough. The field, as well as the depletion current beneath the gate, is then completely dependent on the voltage between drain to source.

Channel scattering

The impacting framework's scattering channel is a quantum situation that exists before or after the collision. The longitudinal electric field portion Ey increases as the channel length decreases due to the lateral expansion of the depletion layer into the channel

region. Surface mobility evolves in this direction, becoming field-subordinate. Channel scattering occurs as a result of the collisions that electrons meet when they are accelerated toward the interface by field Ex. When compared to mass mobility, this results in less normal surface mobility.

Velocity saturation

The highest velocity attained by a charge carrier in a semiconductor, usually an electron, in the presence of extremely strong electric fields is known as saturation velocity. The semiconductor is considered to be in a condition of velocity saturation when this happens. When the dimensions of short-channel devices are scaled without lowering the bias voltages, the device performance degrades, resulting in a reduction in transconductance in the saturation state. The electron drift velocity in the channel is directly proportional to the electric field intensity at low Ey. However, when Ey rises over $104\, V/cm$, the drift velocity slows and eventually reaches a saturation value of $107\ cm/s$ about $y = 105\ \mathrm{V/cm}$ at $300\ \mathrm{K}$. As a result, the drain current is reduced..

Hot carrier effect (HCE)

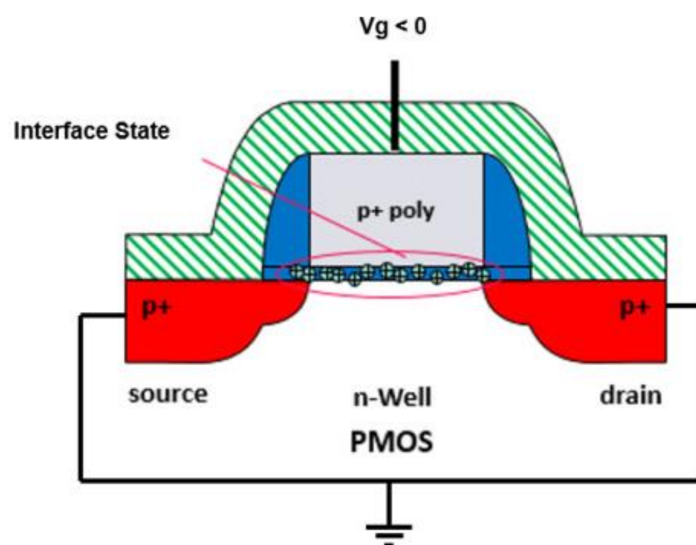


Figure 1.5: Hot Carrier Effect

Another issue associated with strong electric fields is the presence of so-called hot electrons as shown in figure 1.5 [31]. This high-energy electrons can penetrate the oxide and become stuck, resulting in oxide charging, which can damage performance of the device by raising Vth and negatively affecting the gate's control over the drain current. The highest electric field encountered by the carriers present in the channel area towards the end of drain increases when the channel length L, is lowered while the voltage between drain to source remains constant. As the carriers travel from the source to the drain, they accumulate enough kinetic energy in the drain junction's high electric field area to generate impact ionization. Some of them penetrate the oxide after crossing the Si-SiO2 contact. Because they are not in thermal equilibrium with the lattice and have energy greater than thermal energy, these high energy carriers are called as hot carriers (kT). The Channel Hot Carrier Effect is caused by the strong electric field experienced by the carriers from the channel during normal MOSFET operation. The device's performance is harmed when the threshold voltage, Vth, rises, affecting the gate's control over the drain current.

Impact ionization

A primary hot carrier forms a secondary electron-hole pair during impact ionisation shown in figure 1.6 [31]. While the drain current is made up of both primary & secondary electrons in the case of n MOSFET, the secondary holes created by impact ionisation migrate onto the substrate, resulting in the substrate current Ib. The Ib value regulates the heating of channel carriers as well as the electric field in the drain zone. A low Ib number has no negative consequences. However, if the substrate current, Ib, grows too high, the circuit will fail.

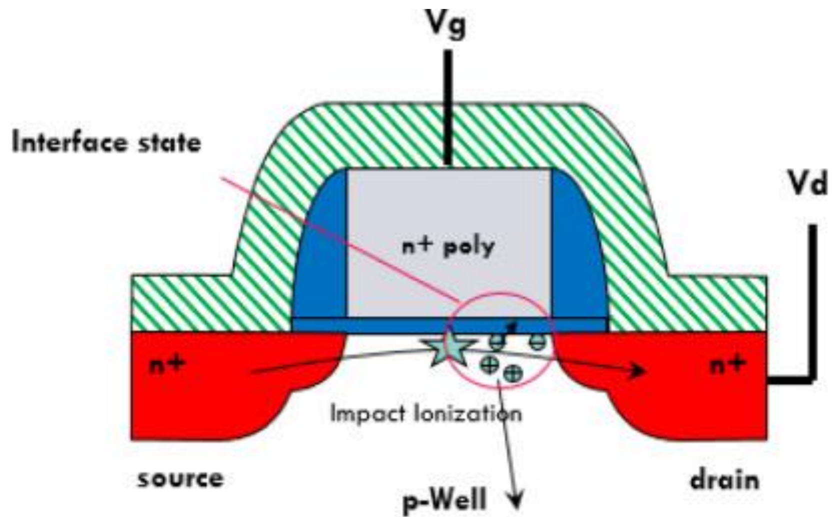


Figure 1.6: Impact Ionization

Source/Drain parasitic resistance/capacitances

A MOSFET's source/drain junction is a parasitic component. Resistance and capacitances (S/D pn junction capacitances and gate-to-source/drain overlap capacitances) are present in these junctions as shown in figure 1.7 [25]. These parasitic components (resistance and capacitances) limit the device's driving capabilities and switching speed and should thus be avoided.

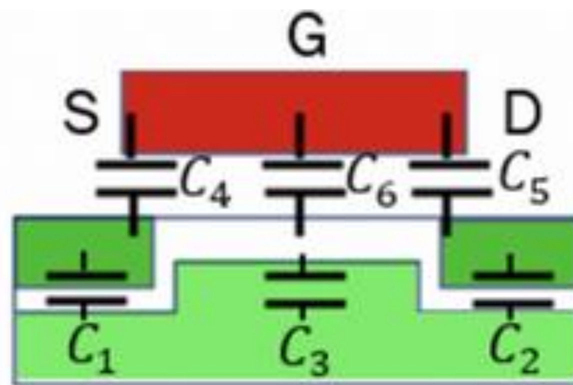


Figure 1.7: Source/ Drain parasitic capacitances

Mobility degradation

Both lateral field Ey (drain voltage) and normal field Ex cause mobility deterioration (gate voltage). As carriers in the channel travel which are influenced by lateral field caused by the drain voltage and normal field caused by the gate voltage, they experience greater dispersion as the fields grow. The reason for this is that the normal field functions in such a way that it accelerates charge carriers towards the surface, causing carriers to disperse more often than in the absence of a gate field The lateral field, on the other hand, causes charge carriers to travel faster, to the point where carriers become velocity saturated at high voltage between drain to source. The device current is more affected by lateral field mobility degradation than by normal field mobility degradation. This is because an increase in the lateral field eventually leads the carriers' velocity to be saturated.

Fringing field effects

The gate overlaps the source and drain areas when the device length and breadth are lowered. Electric field lines grow thick along the channel's side walls as a result of this overlapping. The charge at the channel's borders is effectively increased by these fringing field lines, which has a significant impact on device properties. Ferry calls this phenomena the fringing field effect (1988). Fringing field lines can be seen in a cross-sectional picture of a short channel MOSFET.

Gate to source/drain charge sharing

The absolute value of the threshold voltage drops as the channel length decreases due to the gate's poorer controllability over the channel depletion zone induced by increasing charge sharing from source/drain. SCE is distinguished by the absence of pinch-off and a threshold shift with decrease in channel length at increased drain voltage. Increase in charge sharing from the source/drain reduces gate voltage controllability over the channel.

This deterioration is represented as charge sharing by the electric fields of the gate and drain in the channel depletion layer, which was the first SCE model disclosed.

1.7 Importance of High K Dielectric [27]

- Thinner gate oxides are increasingly required for nanoscale devices as device dimensions continue to shrink for high performance and low power operation.A good solution to this problem is to use double gate MOSFETs with a high dielectric.
- MOSFETs have a greater gate capacitance and are more suitable than pure SiO2 DG MOSFETs because of the higher dielectric constant.
- Reduced Current Leakage

1.8 Reasons for selecting DG MOSFET

The double gate MOSFET was chosen to efficiently regulate the Si channel. The DG MOSFET has superior control over the three critical variables listed below.

.

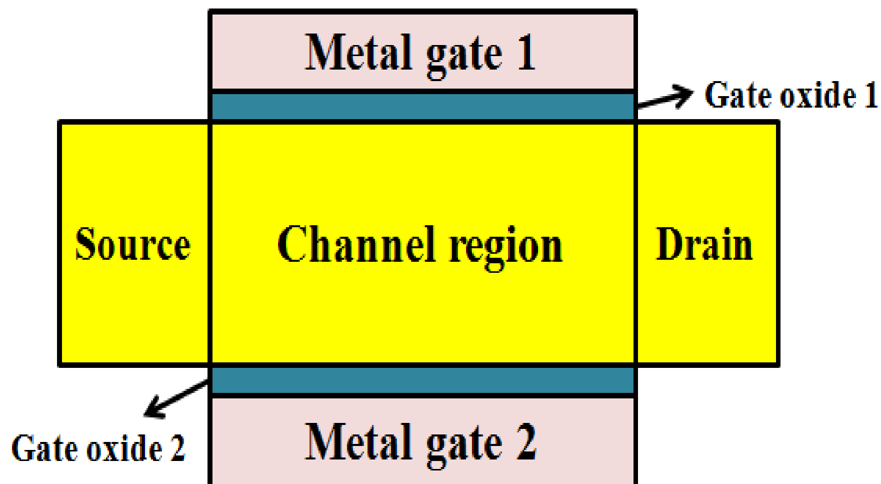
- Threshold voltage roll-off and
- Short channel effects (SCE)
- Drain induced barrier lowering (DIBL)

In comparison to SG MOSFETs, the DG MOSFET has a lower subthreshold swing. All of these factors contribute to the decision to choose a double gate MOSFET.

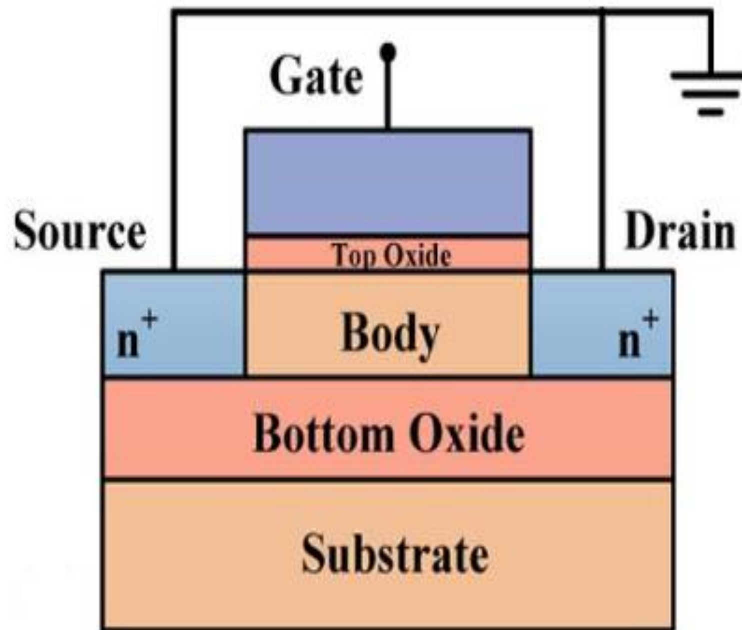
1.9 Different MOSFET structures and Applications

New architectures, such as double gate MOSFETs, tri-gate MOSFETs, and multi-gate MOSFETs[28], have been devised to compensate for SCEs, as illustrated in figure 1.8[28]. These MOSFETs were developed as a replacement for bulk MOSFETs with

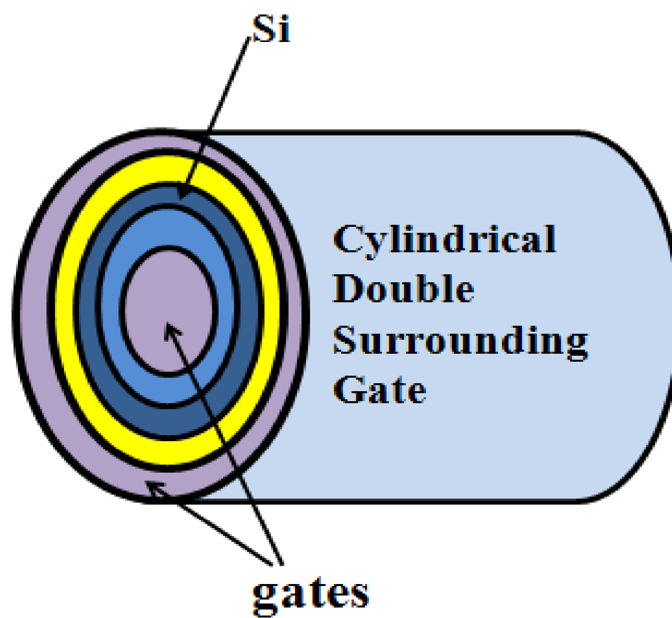
channel lengths more than 45nm. The advantages of a double gate MOSFET over a bulk MOSFET are numerous[29,30]. Short channel effects, junction capacitance, and dielectric isolation are all reduced. SOI (silicon on insulator) is also employed in CMOS technology[31] because of its fast speed and low power consumption. For improved control of short channel effects, DG MOSFETs were employed to create amplifiers[34]. The linearity and analogue performance of TM DG SOI MOSFETs are improved[36]. The square GAA MOSFET was created for device simulators and may be readily integrated into tiny models [34]. MOSFETs with surrounding gates have a wider channel, which improves the driving current[35]. For the enhancement of short channel effects, a capacitance model of material tailored CGT has also been proposed[35]. CSDG MOSFETs were developed to store more energy and increase current flow from source to drain[38]. JL DG MOSFETs also greatly minimise short channel effects[37]. Gate all around junctionless MOSFETs are developed to provide good RF performance. Various structures for like multi channel FINFET and multi channel GAA are developed for further improvement in different performance parameters of the device.



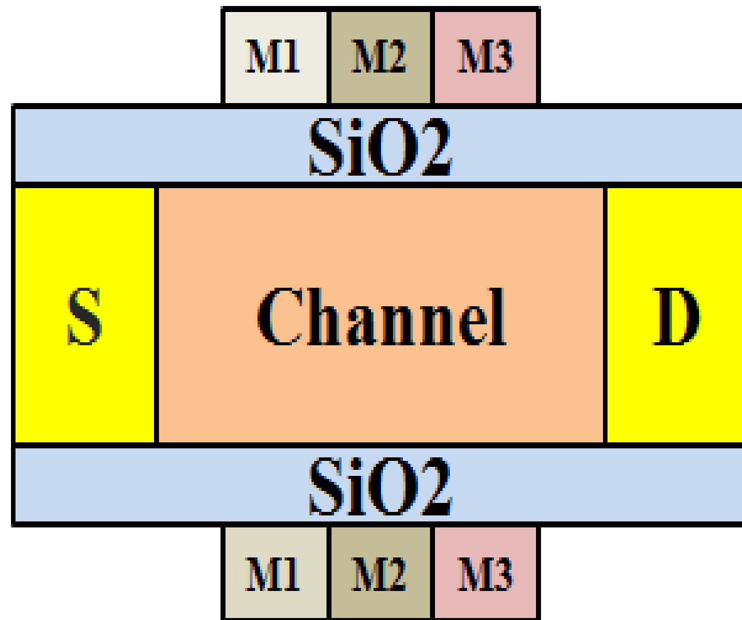
(a) Junctionless DG MOSFET



(b) SOI MOSFET



(c) CDGT MOSFET



(d) TM DG MOSFET

Figure 1.8 : Different advanced MOSFET Structures

1.10 Motivation for Research work

The planar bulk MOSFET structure needs be changed in order to maintain device growth without incurring OFF state leakage current while also attaining increased performance. New device designs are required to give improved gate controllability and reduced short-channel effects (SCEs). Researchers are primarily attempting to tackle the challenges listed above in two ways: I multi-gate architectures for improved gate controllability and larger ON current at constant over-drive voltage, and (ii) channel materials with enhanced carrier mobility. Both solutions were used in this study to minimise SCEs and improve analog/RF performance.

Many advantages of Junctionless MOSFETs over traditional devices have been noted, including increased protection against Short Channel Effects (SCEs), superior scalability, and enhanced drain-induced barrier lowering (DIBL). FinFETs have already surpassed planar MOSFETs as the most popular option at or below the 22-nm technology

node due to their lower Short Channel Effects (SCEs) and superior gate controllability[38]. In compared to planar devices, they also have a larger I_{ON}/I_{OFF} current ratio and a higher driving current per unit area. FinFET device structure fabrication is relatively simple and compatible with traditional CMOS technology.

Lower channel doping is desirable for junctionless MOSFETs in order to produce an appropriate threshold voltage (Vth), low SS, and greater ION/IOFF. Lower channel doping, on the other hand, increases undesired source/drain series resistances. In junctionless FinFETs, an extra doping density in the source and drain regions is used as a solution. Junctionless Accumulation Mode FinFETs have greater doping concentrations in the source and drain regions than in the channel regions and operate in accumulation mode [38]. In compared to SOI FinFETs, FinFETs produced on bulk silicon have higher heat dissipation capabilities, reduced defect density, and cheaper wafer cost. Bulk-FinFETs also aid in the elimination of the floating body effect. As a result, junctionless accumulation mode bulk FinFETs have been a hot issue in current research [39]. High mobility channel materials are being studied for greater driving current and transconductance than Si-based counterparts [40]. By altering the Indium mole percentage of the compound semiconductor, InGaAs-based channel materials provide further advantages in terms of tuneable bandgap [41]. Using an appropriate barrier layer, higher electron mobility and performance can be achieved [42].

As a result, it is critical to analyse and investigate the performance of InGaAs/InP material based MOSFETs with variable barrier layer characteristics and channel composition. When employed in a System of Chip (SoC), analogue and RF circuits of a digital CMOS technology present several obstacles. Device optimization gets more difficult with System on Chip (SoC). As a result, device structure must be investigated in order to improve device performance for digital and analog/RF circuit applications.

The proposed work is focused on the study and design of emerging nanoscale junctionless MOSFETs and their applications, based on the literature review. Different SCEs of the devices under study are investigated in detail, including DIBL, Subthreshold Slope (SS), digital performance parameters such as I_{ON}/I_{OFF}.

1.11 Performance parameters of MOSFET

The performance of different MOSFET structures are based on their ON and OFF-state performance. The deciding factor in further scaling of new MOSFET structures is the ON and OFF state performance. The important transistor performance parameters are as follows:

Surface potential

The difference between the voltage of the MOSFET top layer of polysilicon / metal above the oxide and the voltage in the bulk of the MOSFET is the surface potential of the MOSFET. It is important for determining the gate to source threshold voltage.

ON-state current

When the gate voltage surpasses the threshold voltage, the MOSFET enters the ON state. As a result, when current flows in this condition, it is referred to as ON current, indicated by the symbol Ion, with electrons flowing from source to drain

.

OFF-state current

The MOSFET is in the OFF state when the threshold voltage is more than the gate voltage. However, there is current flow in the OFF state due to minority charge carriers between the drain and source. Subthreshold current is the name given to this type of current.

DIBL (drain induced barrier lowering)

The barrier between the source and channel is reduced when the drain voltage is increased, and electrons flow from source to channel. When the drain bias is raised, the depletion area under the channel expands, lowering the threshold voltage.

$$DIBL = \frac{V_{Th}^{DD} - V_{Th}^{low}}{V_{DD} - V_{D}^{low}}$$

Subthreshold slope

Subthreshold slope is a SCE that occurs in the subthreshold region due to current leakage. SS is calculated as the slope of the gate voltage and drain current during the subthreshold

$$\text{zone.} ss = \frac{dV_{gs}}{d(logI_{d})}$$

Transconductance

In a FET, transconductance is the ratio of change in drain current to change in gate voltage during a short time interval in the drain current vs gate voltage curve. It is denoted as gm.

$$g_m = \frac{2\ I_{DSS}}{|V_P|}(1 - \frac{V_{GS}}{V_P})$$

Junction capacitance

Junction capacitances form in MOSFETs due to charge depletion between the source/drain and the substrate. Depending on the source/drain voltage, the charged depletion changes. The creation of a channel at the surface occurs when the gate voltage surpasses the threshold value.

Stability factor

The stability factor (K) is primarily determined by MOS transistors' two-port equivalent circuit characteristics. It determines whether transistors are conditionally or unconditionally stable in the RF frequency spectrum. The stability factor is calculated as follows:

$$K = \frac{2\ Re[Y_{11}]Re[Y_{22}] + Re[Y_{12}Y_{21}]}{|Y_{12}Y_{21}|}$$

At port 1 and 2, Y_{11} and Y_{22} are the input and output admittance parameters, respectively. Transfer admittances are referred to as the Y_{12} and Y_{21}.

Critical frequency

For a small signal transistor model, as well as maintaining an acceptable AC transistor gain and frequency bandwidth, the critical frequency (fk) is crucial. The critical frequency may be calculated with a stability factor of K = 1. MOSFET capacitance (Cgs, Cgd, and Cds,) and other parasitic capacitances are the main determinants of critical frequency. The critical frequency is denoted by the following:

$$f_k = \frac{f_T N}{\sqrt{g_{ds} g_m R_{gs} M^2 + NM(g_m R_{gd} + 1)}}$$

fT, gds, Rds, and Rgs are the frequencies at unity gain, output conductance, drain to source, and gate to source resistances, respectively. Additionally, the M and N values are given in Cgs and Cgd, respectively.

1.12 TCAD Simulating Tool

TCAD (Technology Computer Aided Design) is an effective method for reducing plan costs, enhancing device design efficiency, and developing superior device and innovation designs. While the cost of building a cutting-edge manufacturing plant continues to climb, owing to Moore's law and subsequent advances in execution, identifying the power has become a comparatively low-cost component. The simulations are used to anticipate the electrical properties of a device design rapidly and affordably, instead of an expensive and time taking process of production. If the display is prepared and the fabrication procedure can be recreated, physical properties like as oxide thickness and doping distribution may be delivered with great precision. Device modeling and simulation describes the electrical characteristics of a certain device architecture. TCAD has a number of advantages, one of which is that it can help you understand the working of semiconductor devices. Evaluation of specific device function, including the change of energy levels and carrier (electrons and holes) with biasing circumstances, can give

useful insight into the link between changes in process conditions or device plan and their impact on device execution. On a speculative basis, these figures are usually impossible to get.

1.13 Gate and channel engineering

1.13.1 Gate Engineering

As device functioning is imbalanced at short gate lengths even with low drain bias, a standard MOS structure will ultimately hit its scaling limit, resulting in Drain Induced Barrier Lowering (DIBL)& (CLM). Asymmetric MOSFET architectures have been presented as a way to overcome the drawbacks in transportation productivity and SCE's (Buti 1989, Chen 1998, Hiroki 1995, Horiuchi 1994, Long 1997 and Zhou 1998). The basic idea behind an asymmetric MOSFET is to change the channel electric-field profile such that it is bigger at the source side to accelerate carriers and smaller at the drain side to reduce short-channel and hot-carrier effects as compared to a symmetric MOSFET. The following are examples of asymmetric MOSFET structures:

- Asymmetric channel doping by Hiroki in 1995 and Kaur in 2007,
- Asymmetric halo source (HS) by Buti in 1989,
- Asymmetric sidewall by Horiuchi in 1994,
- Asymmetric S/D implant by Chen in 1998 and
- Dual-Material-Gate (DMGFET) by Long in 1997, Long in 1999 and Zhou in 1998.

Unlike asymmetric structures with doping engineering given by Buti in 1989, Chen in 1998, Hiroki in 1995, and Horiuchi in 1994, where the channel field distribution is continuous, dual-material gate engineering by Long and Zhou in 1998 introduces a field discontinuity along the channel, resulting in simultaneous transport enhancement and SCE suppression. The gate metal of the Dual Material Gate electrode (DMG) design, as shown in Figure 1.5, is made up of two different materials. The one next to the source

side (M1) has a longer length, L1, and a more noticeable work function, m1, than the other gate's workfunction, m2, which is close to the drain end and has a shorter length, L2 (M2). Unless otherwise stated, the L1 and L2 are maintained equal. The control gate is located at the source end, whereas the screen gate is located near the drain end. When compared to the drain region, the workfunction contrast causes an electric field peak in the channel, resulting in an increase in electric field near to the source area. As a result, the average electron velocity at the source area is substantially greater, which improves carrier transport efficacy and hence reduces the hot electron impact.

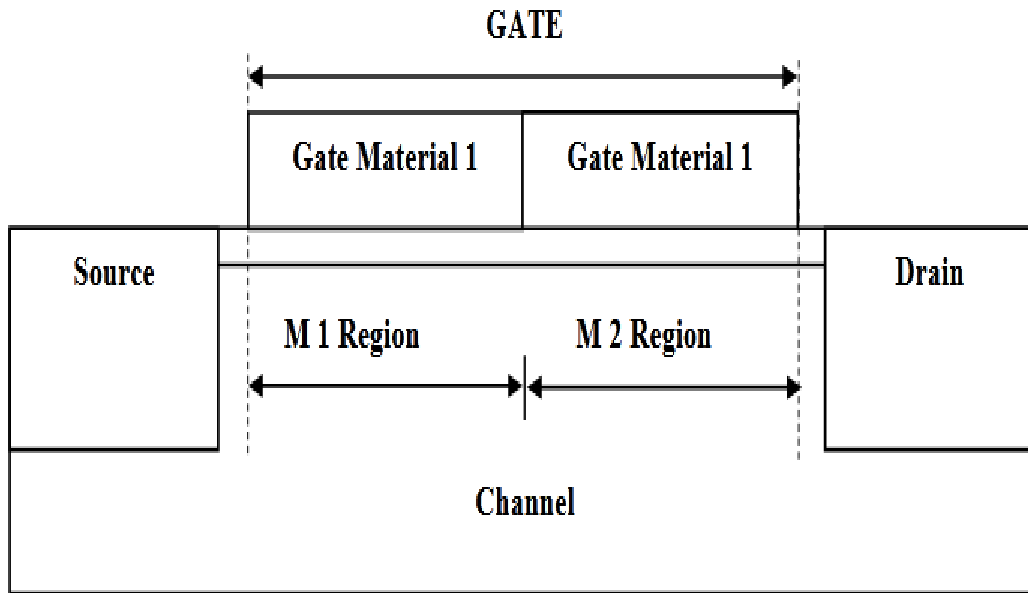


Figure 1.9 Dual material gate FET (DMGFET) structure

In figure 1.9 The DMGFET (dual material gate FET) construction that has been presented. In the case of n-channel FETs, Material 1's work function is bigger than Material 2's, resulting in a higher positive threshold voltage near the source. For p-channel FETs, a reversed configuration is required. MOSFET, MESFET, and HFET are examples of FETs by Long in 1997. The dual material gate electrode architecture's main principle is to add a step function into the channel potential profile, boosting the electric field

distribution present at source side for increasing carrier velocity while screening the drain-potential shift to avoid short channel effects .The screen gate protects the control gate from drain potential variations, which reduces channel length modulation and drain conductance. The drain current and transconductance are both raised when the carrier transport efficiency improves. As a result, considerable gains in device efficiency (gm/Ids)), intrinsic gain (gm/gd), early voltage (Ids/gd), I_{ON}/I_{OFF}, and speed to power dissipation performance (gm-Ion) have been achieved. Various integration schemes are available for fabricating dual material gate architecture, including tilt angle evaporation-metal gate deposition , metal inter diffusion process, chemical mechanical polishing , and fully silicided (FUSI) metal gate fabrication. A poly-silicon gate doping approach is used to effectively create a dual material gate architecture by regulating the source and drain side gates separately. Another type of engineering strategy has been adopted to increase the carrier transport efficiency in the channel, better screening of the channel area from drain bias changes, and therefore enhancing the onstate driving current and DIBL reduction of traditional planar MOSFETs.

1.13.2 Channel engineering

Under the 0.25 micrometre innovation hub, halo doping or a non-uniform channel profile in a parallel bearing was proposed as a new way to limit the dependency of the threshold voltage on channel length. Close to the source and drain implants, halo implants increase the doping. All of the most extremely p-type doped patches in n-channel MOSFETs are near to the channel's two ends. Asymmetrical or symmetrical implants at the source or drain are possible. They're usually added once the gate pattern is complete. Between the source drain junctions with the channel, the implants have a larger degree of impediment.

Channel engineering is in charge of managing the pocket implants or halo implants that are inserted in the channel to adjust the doping convergence and make it doped. Asymmetrical or symmetrical halo implants are available. The presence of halo implants

in a MOSFET tends to lower the surface potential, resulting in an additional step up independent of the number of step-ups induced by channel engineered MOSFETs.

1.14 Thesis Outline

In thesis different advanced structure and their applications are explained . Proposed structures with its detailed dimensions are analyzed in terms of I_{on} /I_{off} current ratio, DIBL and SS .Sensitivity parameters are also analyzed. Different application in biotechnology as well as in low power circuits is designed . Analytical and capacitance modeling of the device is also derived.

Chapter 1 explains the basics of MOSFET, its need and challenges, operating principle different advanced MOSFETs and performance parameter of MOSFET.

Chapter 2 emphasizes that for the sub 45 nm technology node, many gate and channel developed advanced MOSFET architectures are evaluated and compared. The SS I_{ON}/I_{OFF} and DIBL values of several MOSFET architectures are compared.

Chapter 3 explains about the designing of asymmetric gate junctionless MOSFET and its dimension .It also describes results obtained including the ON and OFF current of the device. The sensitivity characteristics of dopingless AJ DG MOSFETs, such as drain extension, gate overlapping length, and oxide thickness, were compared to those of AJ DG MOSFETs with doped channel regions.

Chapter 4 explains the n+ pocket AJ DG MOSFET is analyzed by calculating I_{on} and I_{off} current .The dimensions of the device is mentioned in tabular form and also SCEs like DIBL and SS are also calculated .

Chapter 5 discusses about the applications of asymmetric gate junctionless MOSFET. It describes results obtained for biomedical application and low power application of the proposed device.

Chapter 6 describes surface potential for proposed AJ DG MOSFET of channel length 18 nm and gate length is 11 nm is derived using solutions from 2D Poisson's equations. The proposed device is divided into three segments .The first and third part act as a single

gate MOSFET and the second part as double gate MOSFET. Surface potential for each segment is calculated and added . The capacitance model of the device is also derived. **Chapter 7** explains about the conclusion and future scope of the research work done.

CHAPTER 2

LITERATURE REVIEW

Several sophisticated MOSFET topologies are compared based on their ON and OFF state performance. The performance of innovative transistor designs in both the ON and OFF states will influence future scaling trends. Many applications, such as digital circuits, memory, analog/RF, and medicinal applications, have an impact on MOSFET structure design. To identify application-based MOSFET designs, the study investigates DC and AC performance measures. Using the circuit simulators in the TCAD software, many MOSFET designs are created to test circuit performance. This sort of transistor structure and circuit design analysis is essential for achieving the desired performance while minimising failure or defect in the produced sample.

Various advanced MOSFET architectures are explored and compared for the sub 45 nm technology node in this chapter. Performance characteristics such as ION/IOFF, subthreshold slope, and DIBL values are compared between the structures. Analog/RF performance is evaluated for transconductance, capacitances, and other factors. This chapter also discusses the many uses of MOSFET architectures in various fields.

2.1 Effect of gate engineering on DG MOSFET

Sarkar et al.[52] submitted a study demonstrating the effect of gate engineering on DG MOSFETs in figure 2.1. The use of a completely depleted tri material DG MOSFET is considered. The DM DG MOSFET and SM DG MOSFET are evaluated in terms of RF performance, linearity, and analogue performance. The structure is designed using 35 nm CMOS technology. Varying gate materials with different work functions are taken into account in n-MOSFETs. $M1 = 5.0$ eV, $M2 = 4.75$ eV, and $M3 = 4.5$ eV are the work functions of the materials used. The gate material with the highest work function is positioned closest to the source, while the gate material with the lowest work function is placed closest to the drain. The Si layer $= 10$ nm thick, whereas SiO2 $= 2\ nm$ thick. The source and drain both have a dopant concentration of 10^{20} cm^{-3}. The length ratio of

three distinct materials is calculated as $L1{:}\,L2{:}\ L3 = 1{:}\,1{:}\,0$. The p substrate has a concentration of doping as $10^{16}cm^{-3}$.

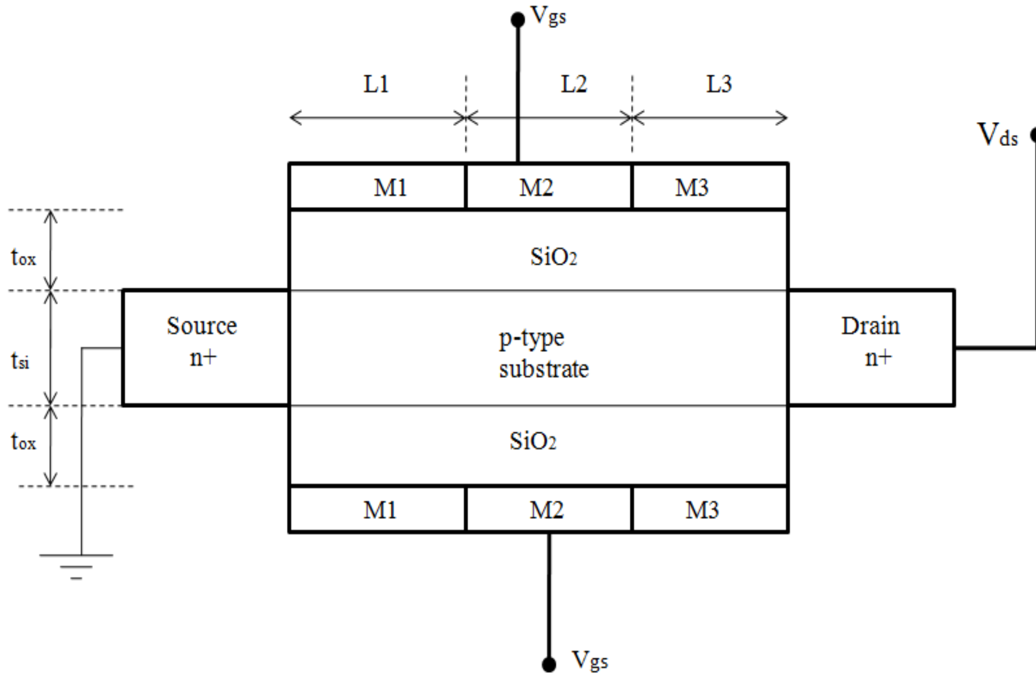


Figure 2.1 : TM-DG MOSFET STRUCTURE

2.2 Gate all around junctionless MOSFET having source/drain extension

F. Djeffal et al.[51] presented a gate-all-around junctionless MOSFET with source/drain extension for better analogue and RF performance, as illustrated in figure 2.2 [51]. The doping concentration of the source and drain extensions is higher in this architecture than the doping concentration of the channel. The doping concentration is indicated by the letters n++/n+/n++. Consider a lengthy channel with a silicon sheet thickness of less than 5nm. The doping concentration of the channel is $10^{18}\ cm^{-3}$, the concentration of both source and drain extension is $10^{19}\ cm^{-3}$, R is 5 nm , L is 100 nm , t_{ox} is $5nm$. The drain current improves by addition of source /drain extension. The GAAJ MOSFET with extensions produces increased current compared to the conventional GAAJ. Therefore, Ion current magnitude increases by 70% with addition of the extensions.

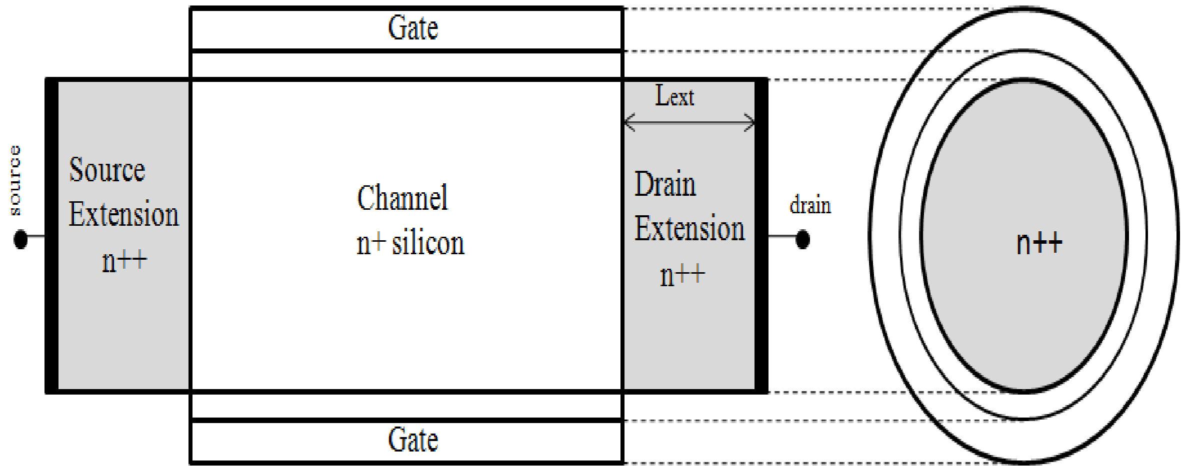


Figure 2.2: GAAJ MOSFET with S/D extensions regions

2.3 Reliability of junctionless double gate (JLDG) MOSFET

Abhinav et al.[55] discussed the reliability concerns with junctionless double gate (JLDG) MOSFETs, as seen in figure 2.3. The effect of gate misalignment on the device's thermal stability between 200K and 500K is investigated. The current is reduced due to the gate misalignment, which deteriorates the JLDG MOSFET performance When the rear gate shifts towards the source or drain side, it causes misalignment. Non-ideal effects result from gate misalignment. The device's gate work function is 5.2 eV, the front and back gate oxide thicknesses are 1nm, the silicon substrate thickness is 5 nm, the channel, drain, and source doping concentrations are 3x10^{19} cm^{-3} and the channel length L is 20 nm.

2.4 A double step buried oxide (DSBO) SOI MOSFET

Figure 2.4 shows a DSBO SOI MOSFET developed by Ali A Ouruji et al. [57].This design combines the benefits of both bulk MOSFETs and SOI MOSFETs.When the form of the buried oxide is modified to a double step shape, the self-heating effects are reduced, and the silicon dioxide thickness is reduced. Heat is easily transferred from the channel to the

substrate. As a result, despite the self-heating effects, the drain current increases. N + source & drain doping is $10^{20}\ cm^{-3}$, N+ source & drain extension doping is $10^{19}\ cm^{-3}$, silicon film doping for P type = $10^{15}\ cm^{-3}$, thickness of thin film = $10\ nm$, source & drain thickness = $50\ nm$, oxide thickness under the source/drain is $100\ nm$, oxide thickness under the channel = $20\ nm$, channel length = $30\ nm$, gate oxide thickness = $1.5\ nm$

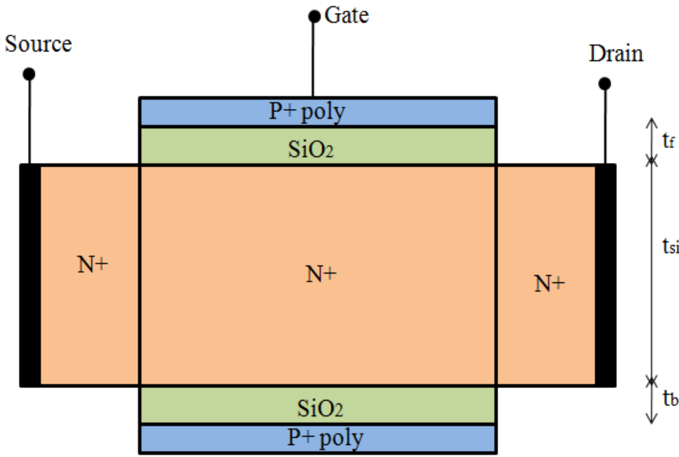


Figure 2.3 :Schematic diagram of n-type JLDG MOSFET

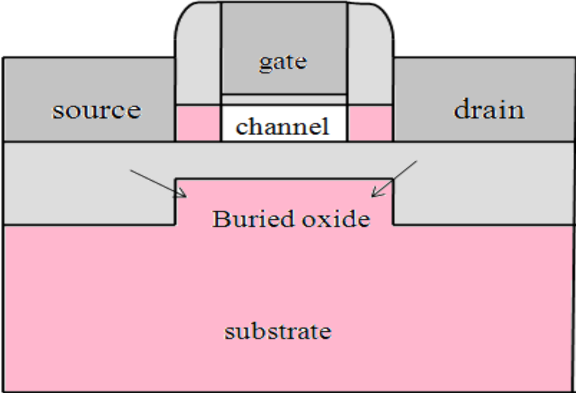


Figure 2.4 :Schematic cross-sectional view of DSBO-SOI structures

2.5 Gate underlap junctionless double gate MOSFET (JL DG MOSFET)

Figures 2.6 and 2.7 show two types of gate underlap JL DG MOSFET suggested by Ajay et al.[58]. The gate underlap region, lying at the end of the source region, is the first example. The gate underlap area is located at the drain end of the JL DG MOSFETS channel region in the second scenario. Using the dielectric modulation approach, these types of structures are employed to detect bio molecules. The surface potential of the JL DG MOSFET is affected by the charged biomolecules. When biomolecules are charged positively, their surface potential rises, and when they are charged negatively, their surface potential falls.

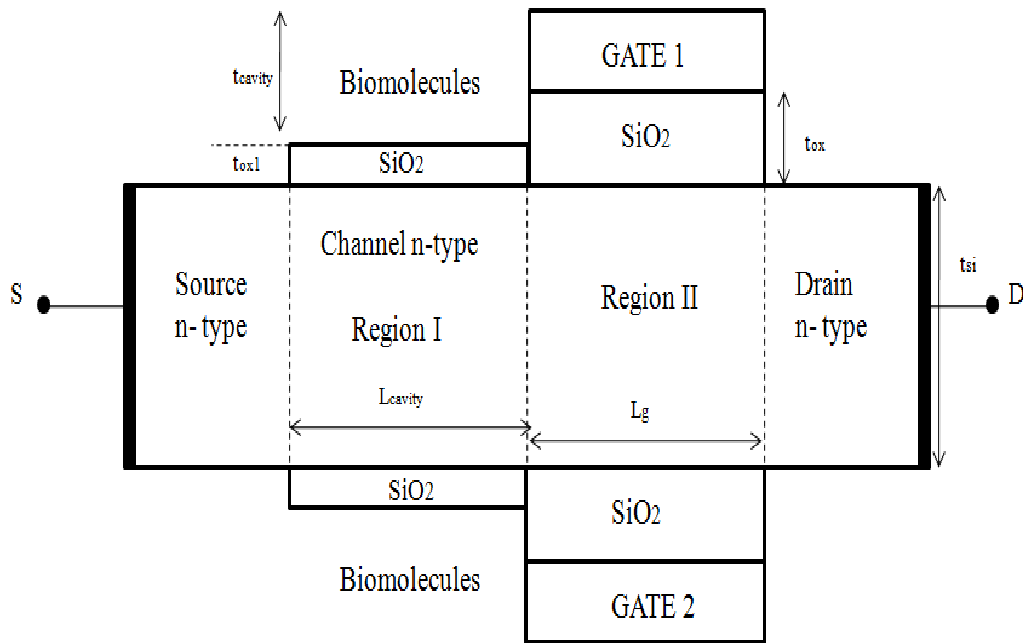


Figure 2.5 : The gate underlap region is considered at the source end of the channel region of JL DG MOSFET.

The gate length $= 50\ nm$, the cavity length $= 50\ nm$, the cavity thickness is $= 19\ nm$, the channel thickness $= 20\ nm$, the gate oxide thickness $= 10\ nm$, the doping in the source & drain and channel is $1x10^{24}$ cm^{-3}, and the oxide layer thickness in the open cavity area $= 1\ nm$.

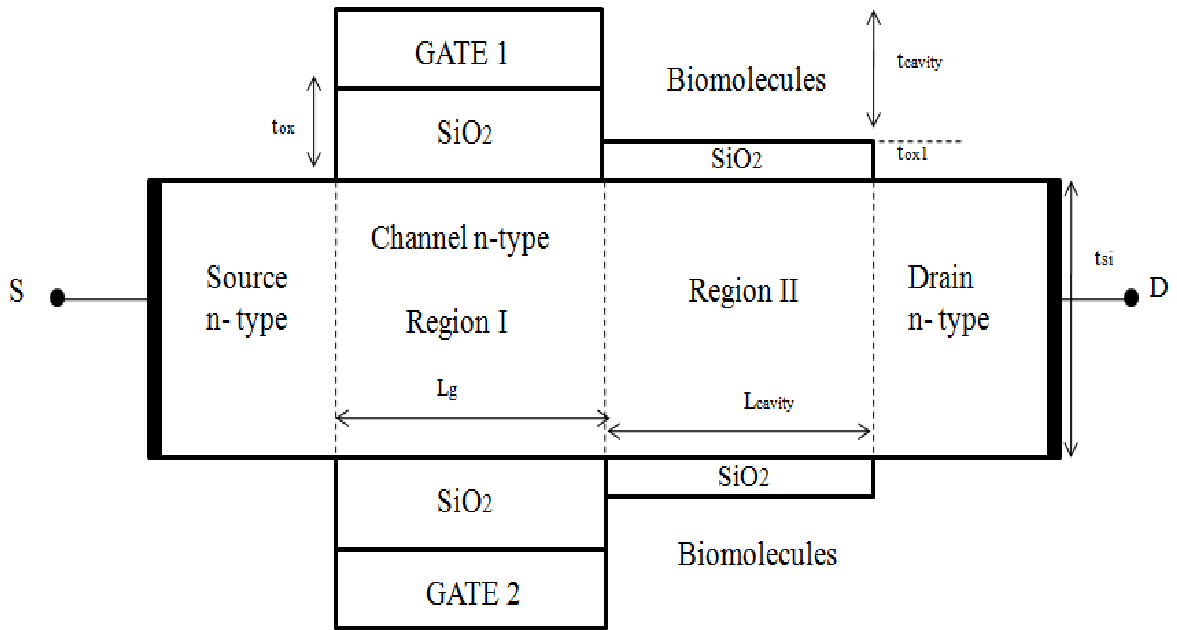


Figure 2.6 :When the gate underlap region is considered at the drain end of the channel region of JL DG MOSFET.

2.6 Silicon based MOSFET

Ikhyeon Kwon et al.[59] submitted a study on silicon-based MOSFETs to improve the device's operation at high temperatures, as illustrated in figure 2.8. This MOSFET is built to withstand the harshest of environments. Local insertion of large band gap material between the source and the channel area is done for high temperature operation. Furthermore, the suggested device is based on an SOI MOSFET structure with buried oxide (BOX) to prevent leakage current from passing through the substrate. The device features a gate length of 100 nanometers, a gate oxide thickness of 3 nanometers, a bottom oxide thickness of 10 nanometers, a barrier width of 10 nanometers, and a barrier depth of 75 nanometers. Source/drain and substrate doping concentrations are 1×10^{20} cm^{-3} and 1×10^{17} cm^{-3}, respectively.

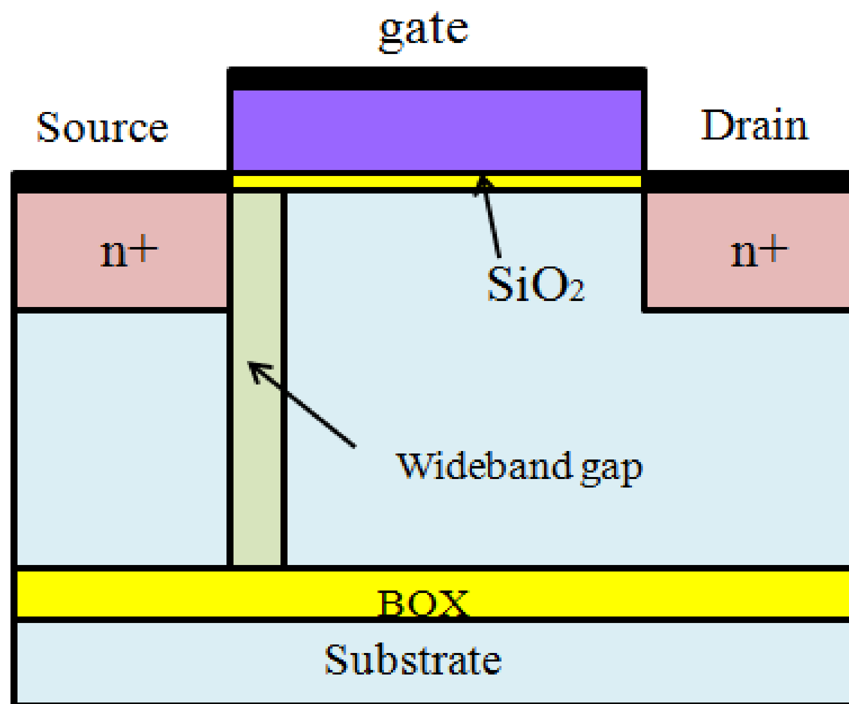


Figure 2.8: Silicon based MOSFET for high temperature operation

2.7 Black phosphorus junctionless recessed channel MOSFET

Figure 2.9 shows a black phosphorus junctionless recessed channel MOSFET built by Ajay Kumar et al. [60] for use in RF applications using 45 nm technology. The junctionless recessed MOSFET is integrated with black phosphorus. The drain current may be increased by up to $0.3\ mA$ using this arrangement. Off current is suppressed, and the SS improved . BP material has a strong ON current and a low OFF current. The gate length $= 20\ nm$, the length of the drain and source region $= 30\ nm$, the device width $= 200\ nm$, the depth of the groove $= 38\ nm$, the length of the channel is $= 44\ nm$, the doping concentration of the drain & source is $5x10^{16} cm^{-3}$, the negative junction depth (NJD) $= 10\ nm$, the voltage of the gate to source $= 1.5\ V$, the thickness of physical oxide $= 2\ nm$, the work

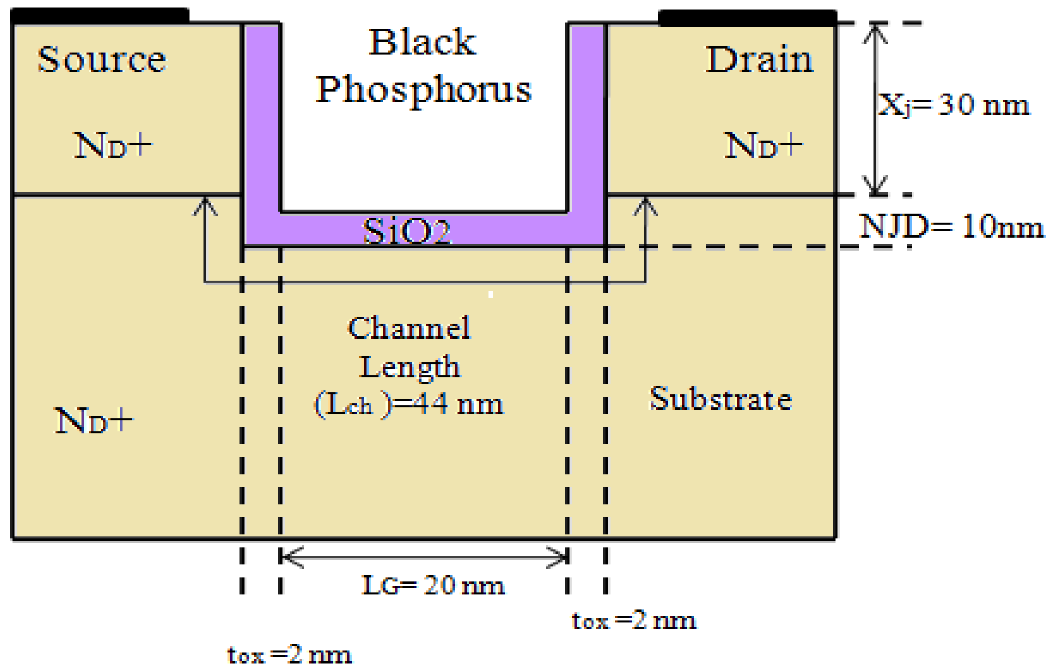


Figure 2.8: Design of BP JL RC MOSFET

2.8 Dual material surrounding gate (DMSG) MOSFET

Figure 2.10 shows the implementation of a 10 nm dual material surrounding gate (DMSG) MOSFET for digital applications by F. Djeffal et al.[51]. The benefits of 50 nm technology and the $\text{multi} - \text{objective genetic algorithms (MOGAs)}$ optimization approach are merged in the DMSG MOSFET. The electrical behaviour of a 10 nm DMSG MOSFET is adjusted and enhanced using the MOGAs technique. The gadget, which is employed in nanoscale digital applications, has a low power consumption and a fast speed. The doping concentration $N_A = 10^{15}\ cm^{-3}$, the drain and source doping concentrations $= 10^{20}\ cm^{-3}$, the channel length L $= 10\ nm$, the oxide thickness $= 2\ nm$, the silicon thickness $= 10\ nm$, and the lengths L1 and L2 are L/2.

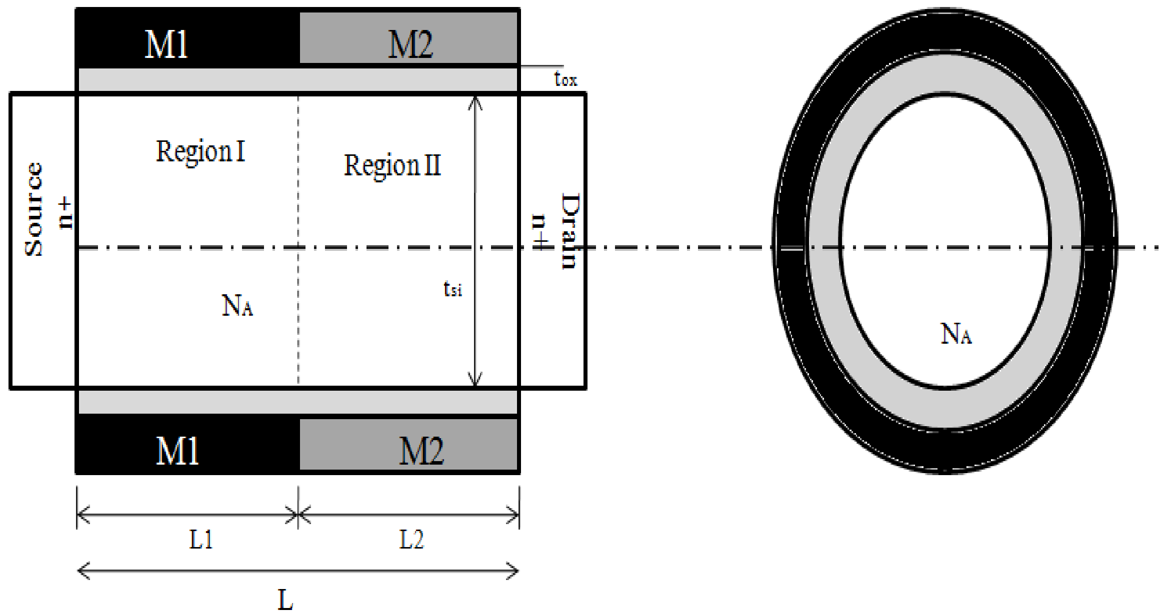


Figure 2.9: Structure of DMSG MOSFET

2.9 Graded channel dual material gate junctionless (GC − DMGJL) MOSFET

Figure 2.11 shows the implementation of a graded channel dual material gate junctionless (GC − DMGJL) MOSFET for analogue applications by Varsha Pathak et al. [61]. The performance of GC − DMGJL and uniform channel dual material gate junctionless (UC − DMGJL) MOSFETs is compared. The GC − DMGJL MOSFET achieves a high drain current while simultaneously lowering SCEs. The device has a high doping concentration of N_{gd}= 2.5x$10^{19}$$cm^{-3}$ near the channel's drain region, and a uniform doping concentration of N_d= 2x10^{19} cm^{-3} in the remaining regions . L (M1):L (M2)is a metal length ratio of 15: 15. W (M1): W (M2) = 5.353: 4.8 is the ratio of the metal's work function. The thickness of the oxide is estimated to be 2 nm. W_{sp}= 10 nm is the length of the spacer. T_{si}= 10 nm is the thickness of silicon.

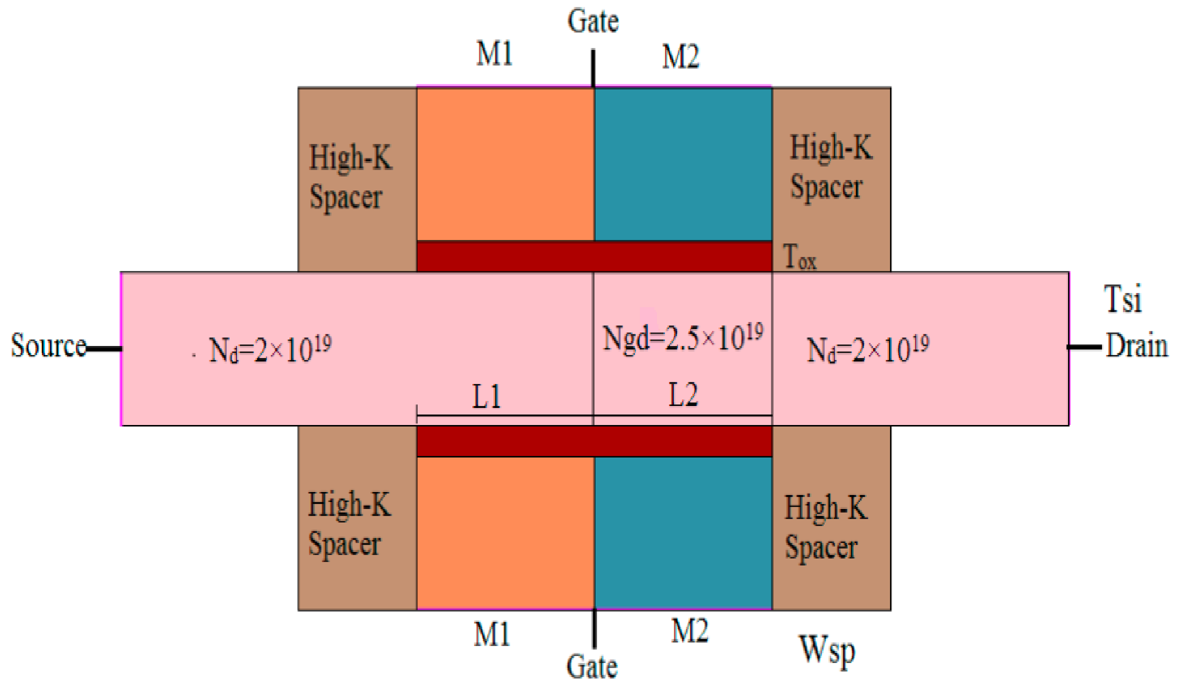


Figure 2.10 : Structure of GC-DMGJL MOSFET

2.10 Junctionless MOSFET structure for detecting biomolecules

Using the dielectric modulation approach illustrated in figure 2.12, Ajay et al.[62] constructed a junctionless metal oxide semiconductor field effective transistor structure that detects biomolecules such as DNA, enzymes, cells, and so on. A nanogap cavity is created by gate oxide etching from both the source & drain sides of the channel. The biomolecules that bonds to the SiO_2 layer present in the nanocavity impact the device's surface potential. The device's dimensions are $t_{bio} = 9\,nm$, $t_{ox1} = 1$ nm, and $t_{si} = 10$ nm, with a doping concentration of $1x10^{25}m^{-3}$ for the source, drain & channel. The lengths of the cavities L1 and L3 = 25 nm, while the length of the oxide $Al_2\,O_3 = 50\,nm$.

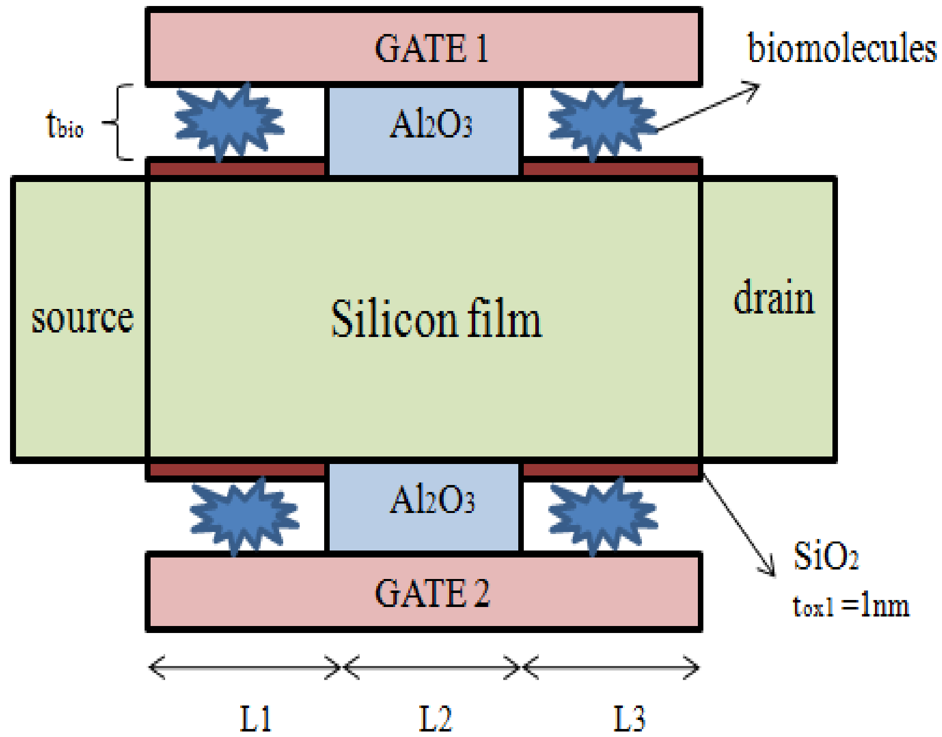


Figure 2.11: Junctionless MOSFET structure for detecting biomolecules

2.11 Pocket of n-MOSFET

Pang et al. [63] designed 0.1 μm pocket of $\mathrm{n-MOSFETs}$ for low voltage applications. Pocket region having high doping concentration is inserted near the drain and source region and center region of the device is lightly doped shown in figure 2.13. This design eliminates short channel effects while meeting OFF and ON current standards. The channel length $= 0.1\mu m$, oxide thickness $= 4\ nm$, the junction depth (r_j) $= 0.06\ \mu m$, pocket doping (N_P) is $1.906x10^{18}cm^{-3}$ and the center region doping (N_c) is $2.175x10^{17}cm^{-3}$, pocket length (L_P).$= 0.024\ \mu m$.

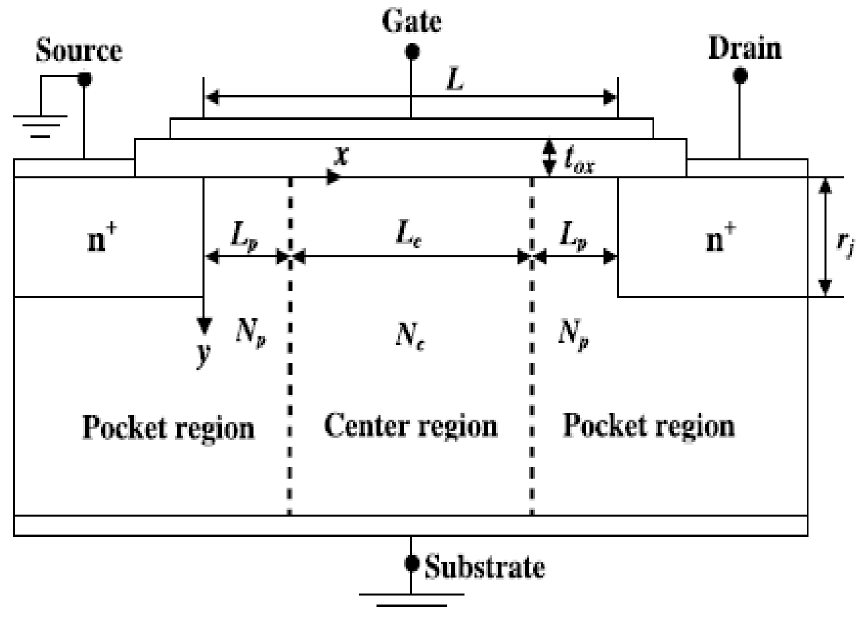


Figure 2.12: Structure of a pocket n-MOSFET

2.12 Nanoscale SOI MOSFET with electrically induced and drain extensions

In Figure 2.14, Ali A. Orouji et al.[64] built a nanoscale SOI MOSFET with a channel length less than $50\ nm$ has source, and drain extensions induced electrically to reduce SCE and hot electron effects. Fabricating a shallow drain and source is challenging, but utilising an EJ SOI MOSFET, a virtual drain and source may be generated electrically. This building has three gates: single main gate and double side gates. Biasing of side gates does not depend on that of the main gate. The virtual drain and source are generated by the inversion layers formed by the side gates.

The doping concentration in the silicon thin layer is $6x10^{16}$ cm^{-3}, the doping concentration in the source and drain is $5x10^{19}$ cm^{-3}, the work function of the side gates $= 4.7\ eV$, main gate work function is $= 4.9\ eV$, buried oxide thickness $= 500\ nm$, the gate oxide thickness $= 2\ nm$, barrier diffusion layer thickness $= 2\ nm$, silicon thin layer thickness $= 50\ nm$.

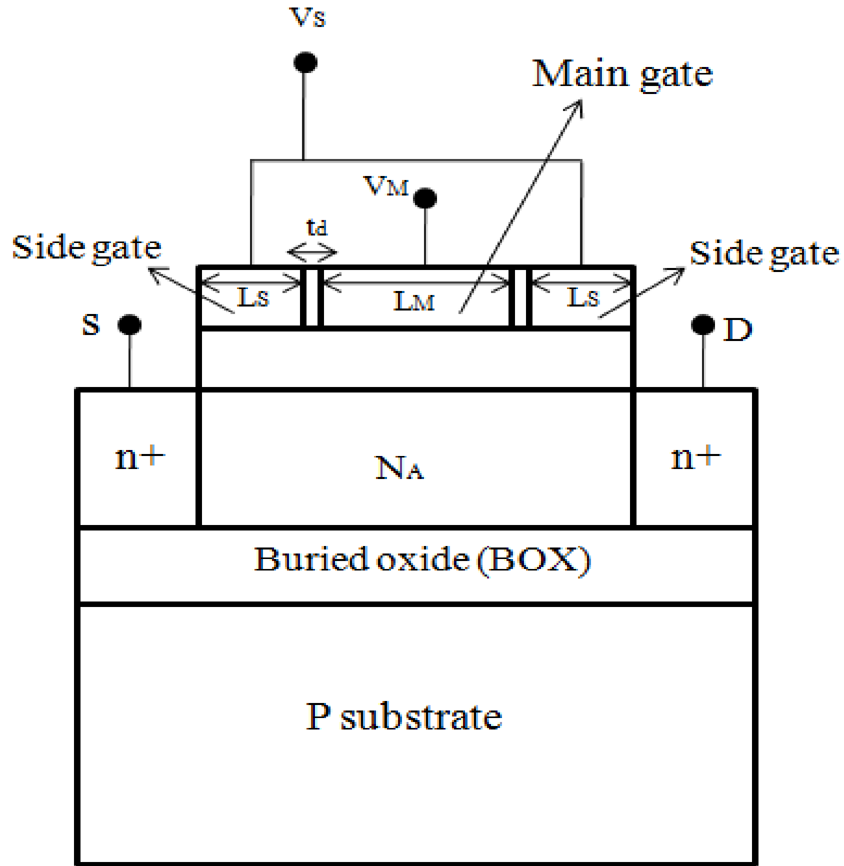


Figure 2.13 : Structure of EJ − SOI MOSFET

2.13 Cylindrical Surrounding gate MOSFET with dual material

To circumvent the SCEs illustrated in figure 2.15, Aurobindo Pal et al. [65] used a surrounding gate MOSFET with dual material. The parabolic approximation approach is used to assess the analytical modelling of threshold voltage, surface potential, and electric field distribution. In terms of SCEs, DMSG and SMSG device structures are compared. SCEs are suppressed more effectively in DMSG MOSFETs than in SMSG MOSFETs, according to the results. Gold M1 has a work function $= 4.8\ eV$, while Cadmium (Cd) has a work function of 4.0 eV. The p −type channel doping zone $= 6x10^{16}cm^{-3}$, while the n + source & drain doping region $= 5x10^{19}cm^{-3}$.

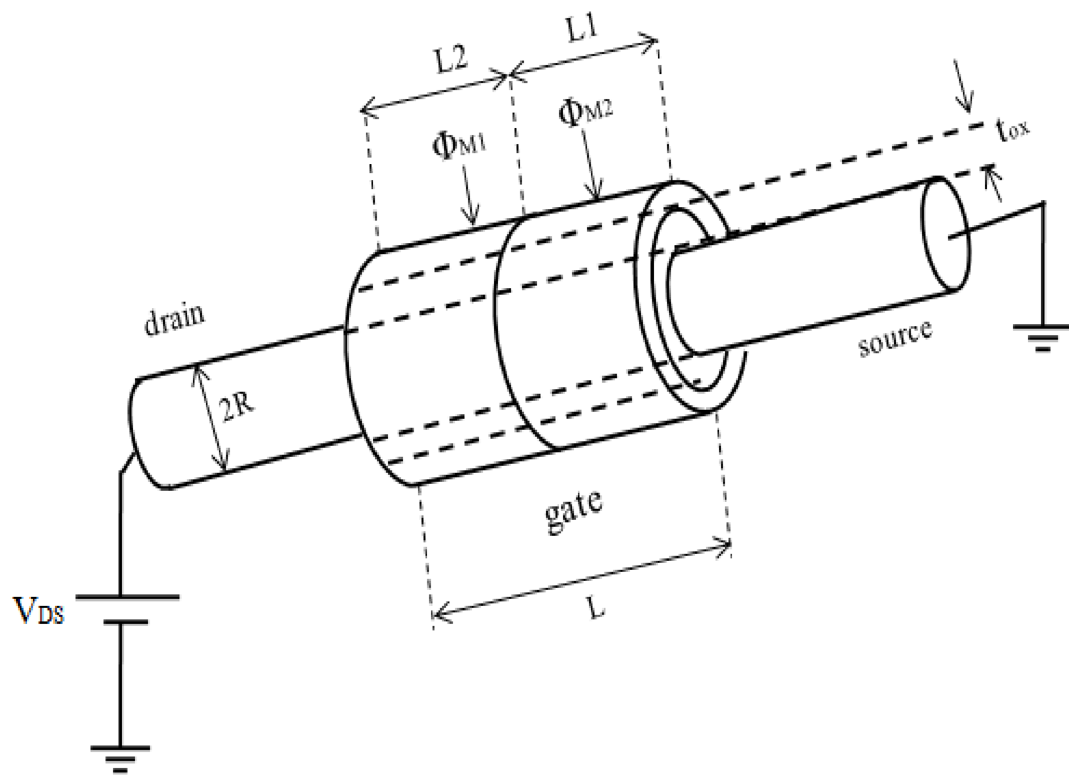


Figure 2.14: Cylindrical Surrounding gate MOSFET

2.14 DG junctionless MOSFET using gate engineered material and source/ drain extensions

Figure 2.16 shows a double-gate junctionless MOSFET built by E. Chebaki et al. [66] employing gate engineered material and source/drain extensions. This arrangement produces an increased drain current and improved RF & analog performance. There is an increase in figure of merit in comparison with the conventional DG junctionless MOSFET. The doping concentration of channel N_d is $5x10^{18}cm^{-3}$, extension has doping concentration $= 5x10^{19}cm^{-3}$, silicon thickness $t_{si} = 10\ nm$, channel length L $=$ $100\ nm$, L1 and L2 are L/2, and the metal M1 has a 5.1 eV work function and a 4.5 eV work function.

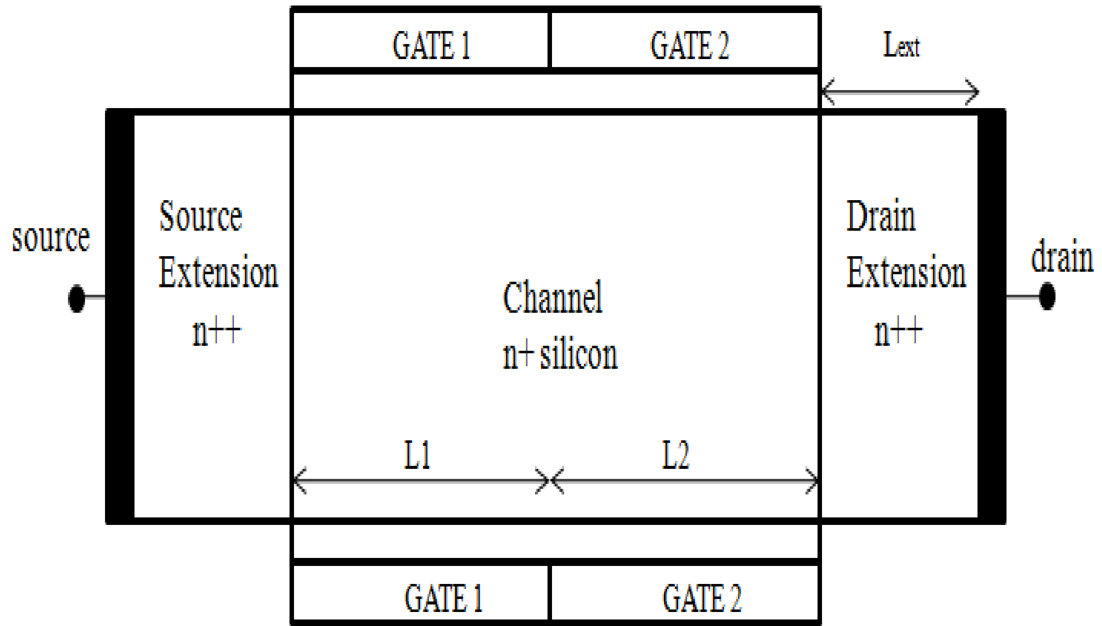


Figure 2.15 : DG junctionless MOSFET with extensions and engineering of gate material.

2.15 Junctionless MOSFET with asymmetrical gates

For superior performance of the device depicted in figure 2.17, Ying Wang et al.[67] developed a junctionless MOSFET with asymmetrical gates. Two gates on are present in asymmetrical manner with overlapping region between them. The channel length of the device depends upon the ON and OFF state of the MOSFET. When the MOSFET is on, the channel length = the combined length of the two gates minus the gate overlap length. When the MOSFET is OFF, the channel length is equal to the combined length of the two gates subtracting the gate overlap length. The the $I_{ON}/\ I_{OFF}$ ratio increases and the sub-threshold slope and DIBL ratio decreases. Gate oxide HfO_2 is 1nm, channel doping concentration is $1x10^{19}cm^{-3}$, gate length is $= 20\ nm$, silicon thickness $= 6\ nm$.

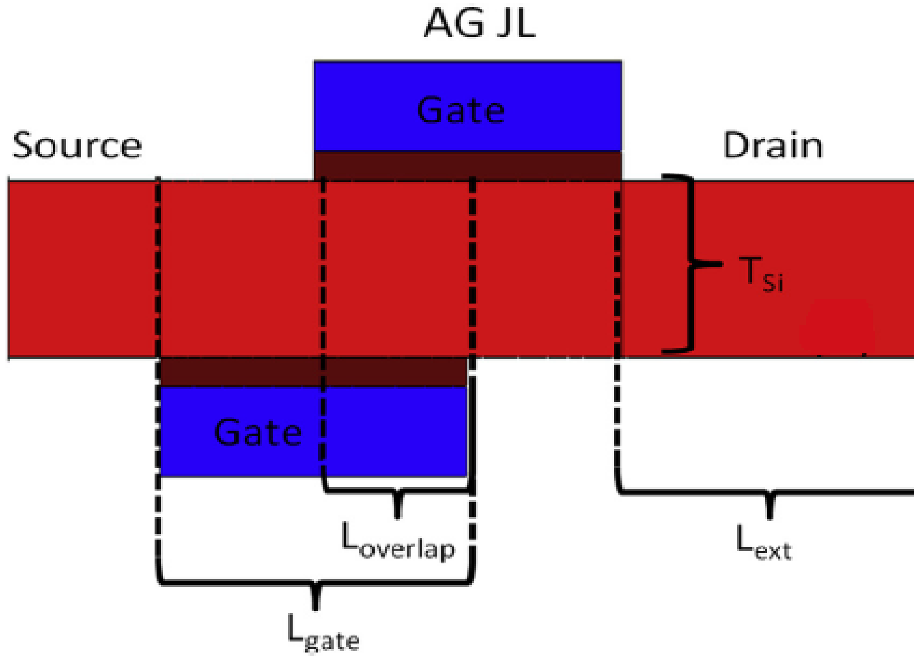


Figure 2.16 : Junctionless MOSFET with asymmetrical gates

2.16 MOSFET with recessed channel and transparent gate

Ajay Kumar et al. [68] investigated the RF performance of a MOSFET having recessed channel along with a transparent gate, as illustrated in figure 2.18. Cut-off frequency, DIBL, transconductance, and maximum oscillator frequency have all been calculated. The suggested structure's results are compared to those of standard recessed channel MOSFETs. The oxide is composed of indium tin oxide, a transparent substance. The cut-off frequency rises 42 percent, whereas the oscillator frequency rises 132 percent. The use of transparent gate material has improved the control of the gate, reducing the SCEs. Channel length (LG) is taken as $30\ nm$, device width is taken as $200\ nm$, depth of groove $= 38\ nm$, source & drain junction depth $= 30\ nm$, negative junction depth(NJD) $= 10\ nm$, substrate doping concentration (N_A) is $1x10^{16} cm^{-3}$, of source & drain doping concentration (N_D) is $1x10^{19}\ cm^{-3}$, physical oxide thickness (t_{ox}) $= 2\ nm$. SiO2 permittivity $\varepsilon_{ox} = 3.9$, voltage of gate to source (VGS) 0.7 V , voltage between drain to source (VDS) 0.5 V, TGRC – MOSFET work function is 4.7 eV ,CRC – MOSFET work function $(\Phi M) = 4.2\ eV$.

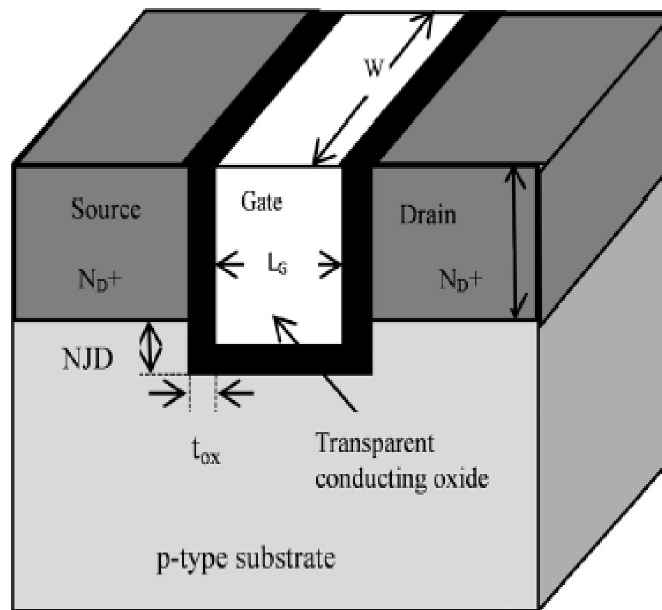


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Figure 2.17 : Structure of recessed channel MOSFET with transparent gate

2.17 Junctionless transistor based 6 − T SRAM cell

Vimal Kumar Mishra et al.[69] used SOI to construct a junctionless transistor-based 6 − T SRAM cell (see figure 2.19). The use of this structure has resulted in a considerable reduction in the size of the devices while also increasing their performance. When compared to double-gate junctionless, there is a rise in I (on)current and a reduction in I OFF. This construction takes up half the space of a traditional building. The suggested structure also improves read and write operations. The ratio of $I_{ON} / I_{OFF} = 10^6$. The area of a junctionless transistor based 6 − T SRAM cell employing SOI = 6.9 μm^2 compared to 11.3 μm^2 for a traditional configuration. .The structure dimension is gate length 18 nm, tox 1nm, tsi channel thickness 10 nm, substrate thickness 10 nm, substrate regions doping density $1x10^{18} cm^{-3}$, channel doping density $1x10^{18} cm^{-3}$, gate material work function 4.9 eV.

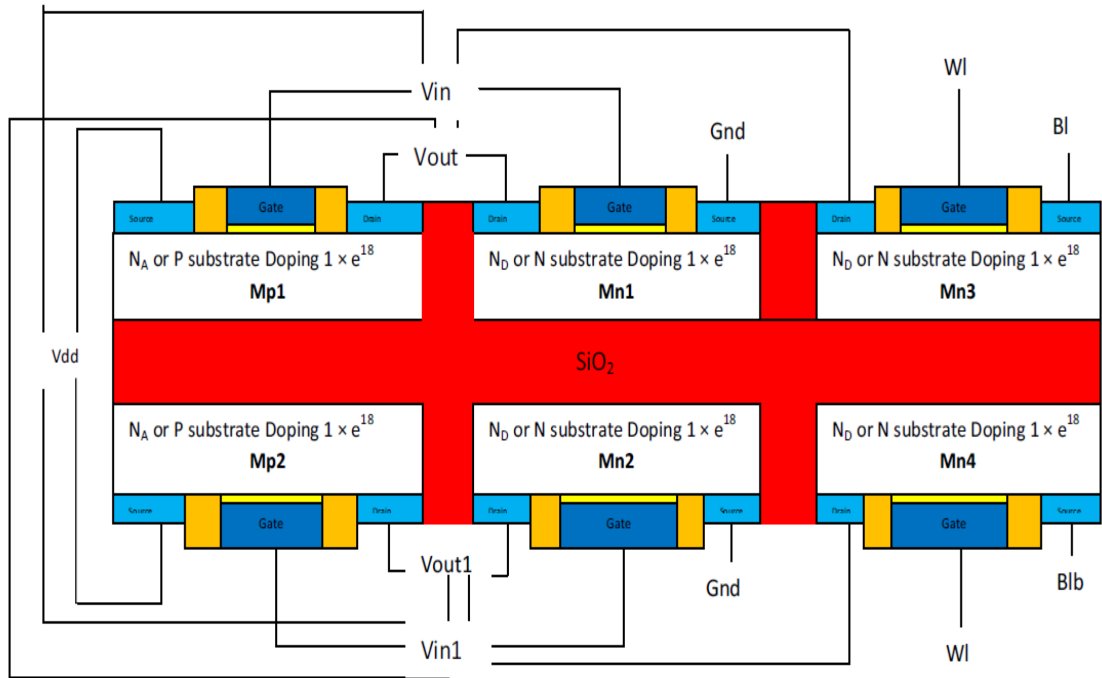

Figure 2.18 : 6T SRAM cell using SOI

2.18 Short channel junctionless DG MOSFET

Figure 2.20 shows a short channel junctionless DG MOSFET presented by Nirmal Ch. Roy et al.[70]. Because channel doping is the equal to the drain & source, there are no p-n junctions in this configuration. The structure's RF & analog performance has been evaluated. The front and back gates are both fed with the same voltage. The DIBL = 75.98 mV/V, the SS = 62.32 mV/decade, and the I_{ON}/I_{OFF} is $4.86\ x\ 10^{9}$. The sub-threshold slope is reduced by 1.61 percent, increase in the I_{ON} and I_{OFF} ratio by 17.08 percent, and DIBL is reduced by 4.52 percent, according to the results. The device's dimensions are: 5.2 eV gate work function, 1 nm oxide thickness of front gate, 1 nm oxide thickness of back gate, 5 nm silicon substrate thickness, N_D 10^{19} to $4x10^{19}$ cm^{-3} doping concentration & channel length L of 20 nm.

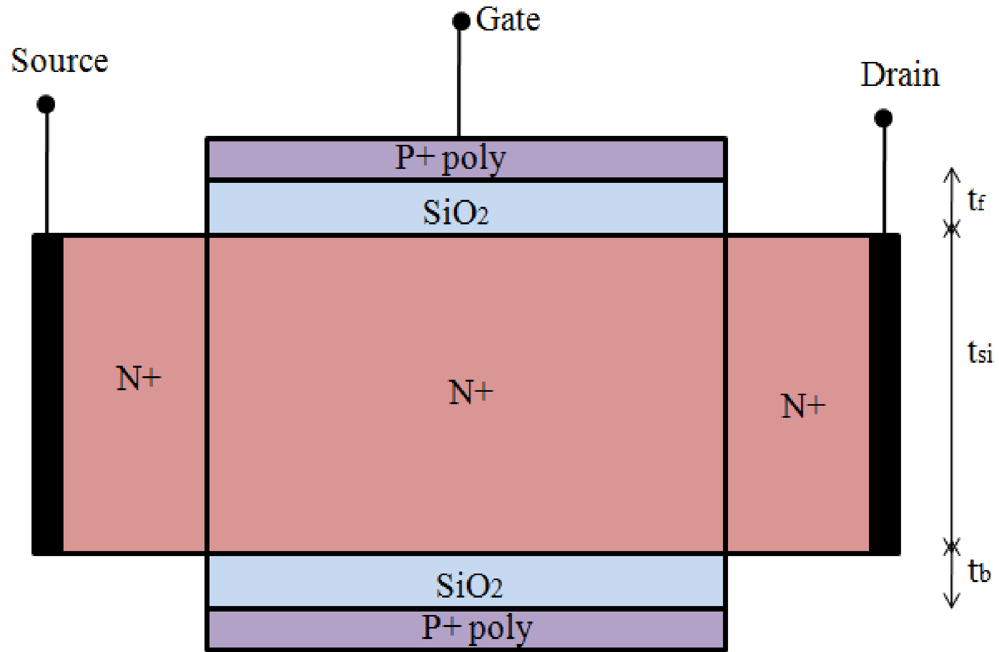

Figure 2.19: Junctionless double-gate MOSFET

2.19 DM gate with short channel with recessed source and drain SOI MOSFET

Figure 2.21 shows a dual metal gate with short channel and recessed source and drain SOI MOSFET suggested by G.K. Saramekala et al. [71]. This device has a strong current output but a low DIBL value. The drain & source regions are doped strongly, whereas the channel area is mildly doped. Work – function of control gate (Φ_{M1}) is taken 4.8 eV (Gold), work-function of screen gate(Φ_{M2}) is taken 4.6 eV (Molybdenum), channel doping (N_a) is taken $10^{15} cm^{-3}$, source & drain doping (N_d) is taken $10^{20} cm^{-3}$, of substrate doping (N_{sub}) is taken $10^{15} cm^{-3}$, oxide thickness of channel (t_{ox}) is taken 1.5– 4 nm , buried thickness (t_{box}) is taken 100– 300 nm, recessed thickness is given as (t_{rsd}) 30– 100 nm, length of recessed (d_{box}) is given 3nm , length of the channel (L) is given 30– 300 nm.

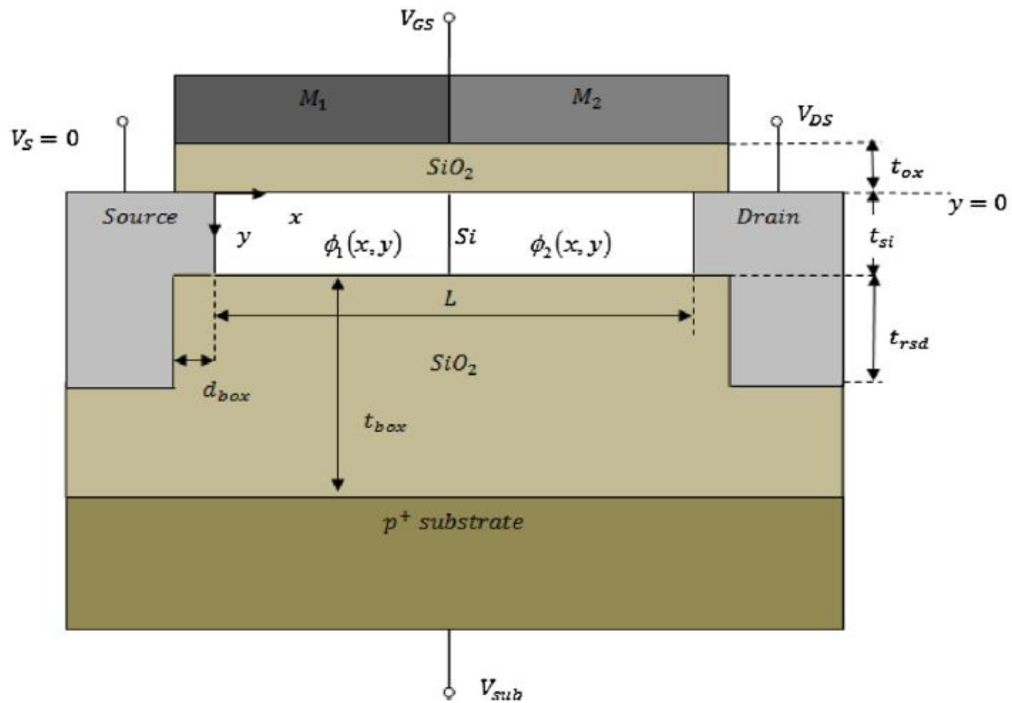

Figure 2.20 : Dual metal gate (DMG) with recessed source and drain UTB SOI MOSFET.

2.20 DG MOSFET

Vijay Kumar Tewari et al.[72] proposed a double gate MOSFET structure as shown in Figure 2.22. .The device is designed in Silvaco-Atlas 2D TCAD tool. The proposed device has two gates, the front and back gate. Large inversion layer of the carrier is generated by double gate MOSFET in comparison to SG MOSFET.The high drive currentis obtained through high inversion in the channels and therefore it can be used in high power applications. At the gate voltage of 1 V and drain voltage of 1 V the drain current of the device obtained as 6 mA.

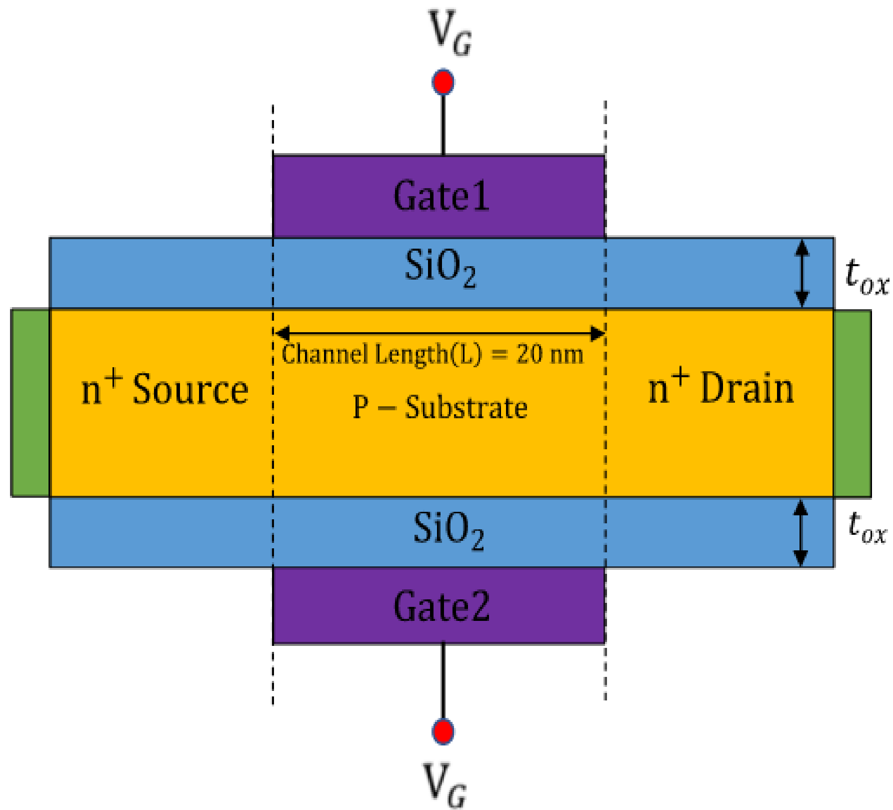

Figure 2.21 : Structure of DG MOSFET

2.22 DG circular MOSFET

Figure 2.23 shows a double gate circular MOSFET presented by Kallepelli Sagar et al.[73] with a channel length 10 nm and has an inner silicon pad that taken as drain. An underlap and high − k (HfO 2) are employed to increase the performance of the proposed device. The DC and AC analysis of effect of high − k and length of the underlap is performed with the help of 3D GENIUS TCAD simulations for Low Power and High Performance applications. The important device parameters are R1 = L = 10 nm, R2 = L = 20 nm, and R3 = L = 30 nm, the thickness of substrate = 20 nm, the gate thickness is 5 nm, buried oxide thickness = 20 nm, gate oxide thickness = 1 nm and thickness of active silicon film = 5 nm. The device I_{ON}/I_{OFF} ratio obtained is 1.55× 10^7 , SS of ~66 mV/ dec, and a DIBL of 56 mV/V is obtained.

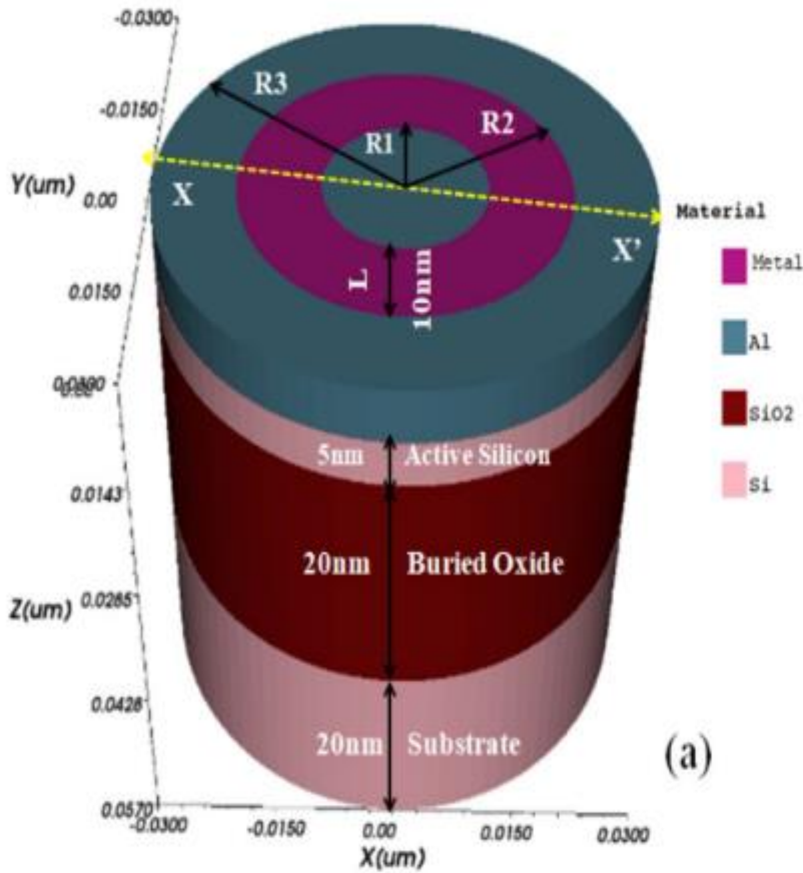

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Figure 2.22 :Double gate Circular MOSFET

2.23 Gate underlap dielectric modulated MOSFET based on charge plasmaas a biosensor

The device depicted in figure 2.24 is a MOSFET with four gates that is used to detect biomolecules such as biotin, protein, APTES, and so on. It is comparable to a twin gate MOSFET with the centre half removed[39]. The central area of the gate is carved in order to capture biomolecules. The structure's gate length (L G) is 300 nm, the region of underlap between the gates (L gap) $= 200\,nm$, the thickness of the back and front gate (toxpad) $= 10\,nm$, the thickness of the SiO 2layer (t si) is 1 nm, the thickness of the silicon body (tsi) is 25 nm, channel doping is 10^6 cm^{-3} and drain and source doping 10^{20} $cm^{-3.}$

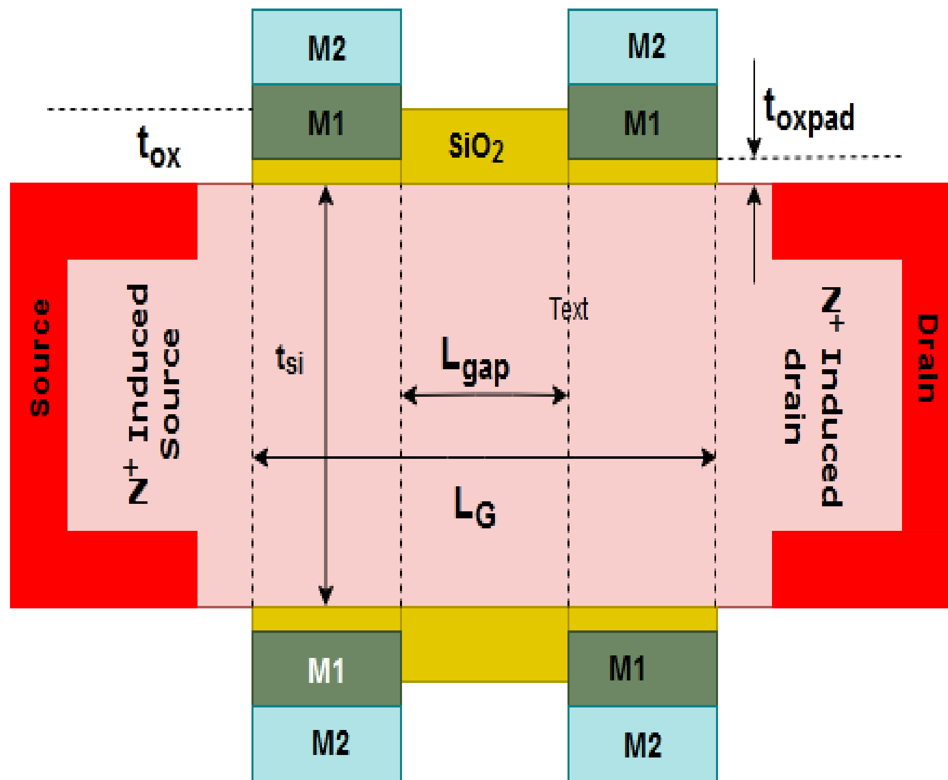


Figure 2.23: Dielectric modulated MOSFET based on charge plasma concept

2.24 Dual material surrounding split gate junctionless transistor(DMSG JLT) as biosensor

Figure 2.25 depicts a DMSG JLT MOSFET developed for biomolecule sensing[89]. The gate area and gate oxide are carved in the middle to create a cavity region for trapping biomolecules. Due to the existence of air in the cavity, the dielectric constant of the cavity is one in the absence of biomolecules. The dielectric constant fluctuates with the entrance of biomolecules since various biomolecules have varying dielectric constants, which alters the threshold voltage and is used to calculate device sensitvity. The device's dimensions are channel length (L_{CH}) of 45 nm, length of the metal M1 (L1) of 15 nm, length of the cavity (L_{CAV}) of 15 nm, length of the metal M2 (L2) of 15 nm, silicon thickness (t si) of 10 nm, SiO_2

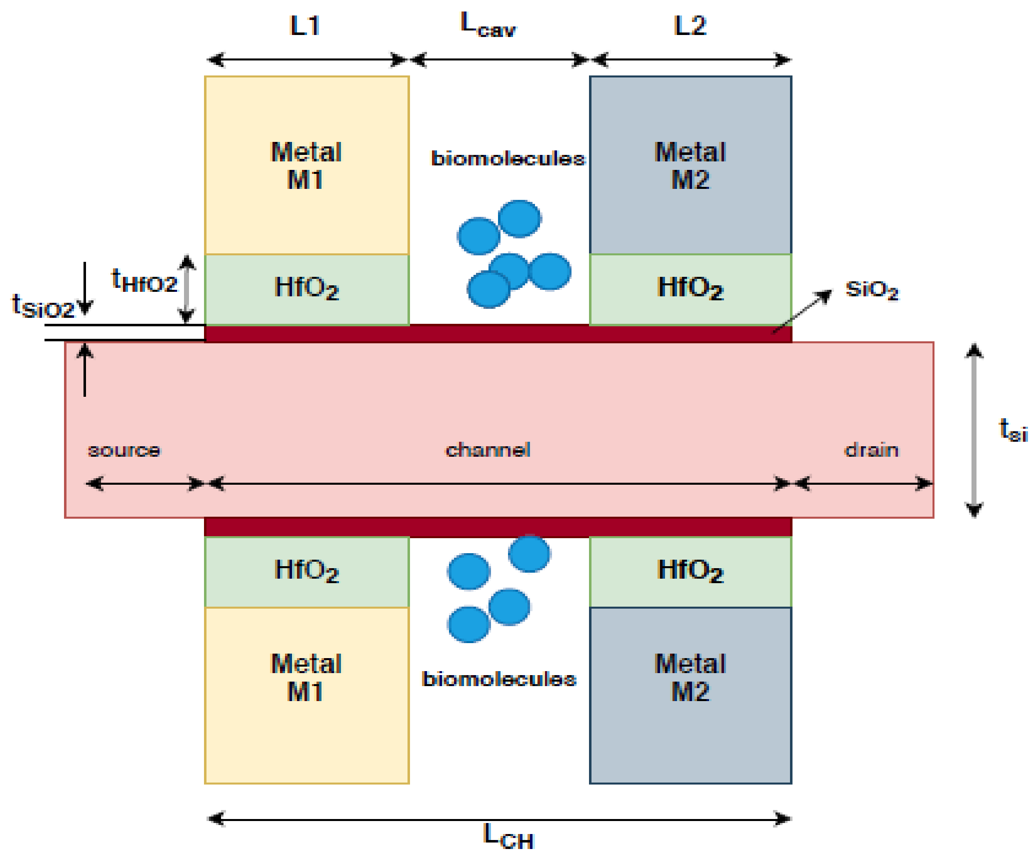


Figure 2.24 : DMSGJLT as biosensor

Table 2.1 : Literature review

Detail of the journal/ Book / Book chapter/ website link	Year of Publication	Indexing of journal (Scopus/ SCI index etc.)	Main findings or conclusion relevant to proposed research work
Vishnu Priya Ammina et al.[74] designed an Optimized Ge Pocket SOI JLT, *Silicon*	2019	SCI	Reduces the temperature of the lattice. The channel length is 20 *nm*.
F. Djeffal et al.[51] designed GAA junctionless MOSFET, *Superlattices and Microstructures*	2003	SCI	The heavily doped areas have also resulted in a 70 percent increase in I_{ON} current magnitude.
Nirmal Ch. Roy et al.[70] performed surface potential modeling of JLDG MOSFET analog/RF circuits, *Microelectronics Journa*	2015	SCI and Scopus	DIBL fell by 4.52 percent, while the sub-threshold slope reduced by 1.61 percent and the ratio climbed by 17.08 percent. length of the channel is 20 nm.

E. Chebaki et al. [66] designed a DG JL MOSFET using gate engineering and drain & source extensions, *Superlattices and Microstructures*	2016	SCI	Enhances RF and analog performance. The merit figure has been raised. The channel length is 100 nanometers.
Ali A. Orouji et al. [64] Nanoscale SOI MOSFETs having electrically induced source & drain extension; *Superlattices and Microstructures*	2006	SCI	Short channel effects are suppressed for channel lengths smaller than 50 nm, as well as hot electron effects.
Ajay et al.[62] designed a DG JL MOSFETs for application as biosensors, *Superlattices and Microstructures*	2015	SCI	Detecting biomolecules like DNA, enzymes , cells etc by dielectric modulation technique. The channel length is 100 nm.

Varsha Pathak et al.[61] designed a GC − DMGJL MOSFET for Analog Applications, *Procedia Computer Scie*	2018	Scopus	Reduces short channel effects by having a high drain current and transconductance. The channel length is 30 nm.
Ajay kumar et al.[60] Analyzed a sub−20 nm BP based JL-recessed channel MOSFET for analog/RF applications, *Superlattices and Microstructures*	2018	SCI	The drain current of the structure rises to 0.3 mA. Sub threshold slope improves as off current decreases. The channel has a length of 44nm.
Angsuman Sarkar et al.[62] analyzed gate engineering effect on DG MOSFETs for analog/*RF* applications ,*Microelectronics Journal*	2012	SCI and Scopus	The performance of the RF system improves. When compared to the DM DG MOSFET and the SM DG MOSFET, the DM DG MOSFET has better linearity and analogperformance. Channel length is 35 nanometers.

Yon-Sup Pang et al.[63] Design of $0.1-\mu m$ pocket n-MOSFETs for low-voltage applications, *Solid-State Electronics*	2002	Scopus	Short channel effects are well-tolerated, and the off-state and on-state current criteria are met. The channel length is 100 nanometers.
Ajay Kumar et al. [68] analyzed the performance of TCAD RF investigation of Transparent Gate Reces Channel MOSFET, *Microelectronics Jourr*	2016	SCI and Scopus	The cut-off frequency has been increased by 42 percent, and the oscillator frequency has been increased by 32 percent. The channel is 30 nm long.
Ajay et al. [58] designed a gate underlap JL DG MOSFET as bio-sensor, Materials Science in Semiconductor Processing	2017	SCI and Scopus	Used to detect the bio molecules using dielectric modulation technique. Channel length is 20 nm.

Ying Wang et al.[67] designed JL MOSFET with asymmetric gate for better performance , *Superlattices and Microstructures*	2016	SCI	Reduce drain caused barrier lowering and insubthreshold slope (68 mV/dec). (65mV/V). The channel length is 20 nm.
Vimal Kumar Mishra et al. [69] designed JL Transistor Based 6 − T SRAM Cell Using SOI Technology, *ECS Journal of Solid State Science a Technology*	2018	SCI	The area of a junctionless transistor based 6-T SRAM cell employing silicon on inductor is 6.9 m-cube, compared to 11.3 m-cube for a traditional construction.
G.K. Saramekala et al.[71] deriveda threshold voltage model for a SC dual-metal-gate (DMG) recessed − source/drain (Re-S/D) SOI MOSFET, *Superlattices and Microstructures*	2013	SCI	This device has a strong current output but a low DIBL value. The channel length ranges from 30 to 300 nanometers.

Arobinda Pal et al.[65] studied a DM SG MOSFET to suppress SCEs, *Engineering Science and Technology*.	2014	SCI and Scopus	DMSG MOSFETs (SCEs) are more efficient than traditional SMSG MOSFETs.
Chunshan Yin et al.[75] investigated S/D Asymmetric Effects Due to Gate Misalignment in Planar DG MOSFETs, *IEEE Transactions on Electron Devices*	2005	SCI and Scopus	The extra overlapped region produces extra overlap capacitance and gate leakage current, while the non overlapped region produces extra series resistance and weak control over channel.
Jae Young Song et al.[76] GAA MOSFETs, *IEEE transaction on Nanotechnology*	2006	SCI	When compared to the double gate MOSFET, the DIBL value dropped to 81.44 mV/V. The current in the ON state is raised, while the current in the OFF state is decreased.

Sheng Chang et al.[77] performed analytical modeling of undoped symmetric DG MOSFETs with small gate oxide thickness asymmetry, *IEEE Transactions on Electron Devices*	2009	SCI and Scopus	Drain current, channel current, transconductance, gate capacitances, and the influence of oxide thickness on MOSFET parameters are all measured.
Shubham Tayal et al. [78] analyzed of JL DG MOSFET based 6T − SRAM with gate stack configuration, *Micro & Nano Letters, IET journal*	2018	SCI	The JL DG-static MOSFET's noise margin is improved by using a high-k dielectric material. The stability of the system suffers as the gate length is reduced.
Mohammad Bavir et al.[28] studied JL DG MOSFET with Symmetrical Side Gates, *Silicon*	2019	SCI and Scopus	Using the side gates, the DIBL and SS improved. The channel's drain voltage impact is lessened, making it easier for the gate to regulate the channel.

Zeinab Ramezani et al. [26] designed a novel DG MOSFET by symmetrical Insulator Packets with Improved SCEs, *International Journal of Electronics*	2017	SCI and Scopus	The reliability of hot electrons is improving. The DIBL value, as well as the On state and OFF state current ratios, have improved.

2.25 Research Gap and Motivation for research work

- New device designs are required to give improved gate controllability and reduced short-channel effects (SCEs). Researchers are primarily attempting to tackle the challenges listed above in two ways: I multi-gate architectures for improved gate controllability and larger ON current at constant over-drive voltage, and (ii) channel materials with enhanced carrier mobility. Both solutions were used in this study to minimise SCEs and improve analog/RF performance.
- Many advantages of Junctionless MOSFETs over traditional devices have been noted, including increased protection against Short Channel Effects (SCEs), superior scalability, and enhanced drain-induced barrier lowering (DIBL).
- Lower channel doping is desirable for junctionless MOSFETs in order to produce an appropriate threshold voltage (Vth), low SS, and greater ION/IOFF. Lower channel doping, on the other hand, increases undesired source/drain series resistances.

2.26 Summary

Various MOSFET architectures have been investigated, along with their structural features and dimensions, as well as their uses. The structure of MOSFETs has been altered primarily to lessen short channel effects such as DIBL and SS values. The primary goal of these structures is to boost ON-state current while lowering OFF-state current. To attain a desirable range of transconductance, transistor gain, stability factor, and critical frequencies, the MOSFET architectures are further examined for optimal analog/ RF performance criteria. Improved subthreshold performance may be achieved using gate designed transistors with high work function metal contacts and varied high-K dielectric regions. This demonstrates that gate-engineered multi-gate junctionless MOSFETs have the ability to satisfy future scaling trends in CMOS technology while also increasing compatibility for digital/analog, portable IoT, and biomedical applications.

CHAPTER 3

18 nm N-CHANNEL AND P-CHANNEL DOPINGLESS ASYMMETRICAL JUNCTIONLESS DG-MOSFET

When the size of the MOSFET is reduced, the channel length is reduced, resulting in a short channel effect and an increase in leakage current [79]. Short channel effects (SCEs) have emerged as semiconductor device sizes have shrunk. Short channel effects include parasitic capacitances, drain-induced barrier lowering, mobility degradation, and hot carrier effects, among others. To counteract these effects, alternative approaches such as gate engineering and channel engineerings [80] must be used to engineer the devices. Gate engineering include modifying the gate's material to suit different job purposes, as well as constructing double, triple, and multi-gate systems. Channel engineering include altering the channel's form and size, as well as the drain and source areas. When the drain barrier's breadth extends into the drain and the source region barrier lowers, SCEs occur.

This chapter explains about the designing of asymmetric gate junctionless MOSFET and its dimension .It also describes results obtained including the ON and OFF current of the device. Comparison of various sensitivity parameters of dopingless AJ DG MOSFET like drain extension, gate overlapping length and oxide thickness with the AJ DG MOSFET with doped channel region has be made.

3.1 Design Methodology

Figure 3.1 represents the design methodology divided into various steps.The first steps for designing AJ DG MOSFET is to perform channel and gate engineering enhancing the performance of device and to reduce SCEs.The second step is to meet all the criteria for ITRS standards while scaling the MOSFET further. The third step is to implement AJ DG MOSFET using Visual TCAD tool in 2-D and 3-D. Graphical analysis is done using MATLAB. After computing the results, they are analyzed . If the desired result is not obtained changes in structural level can be done.

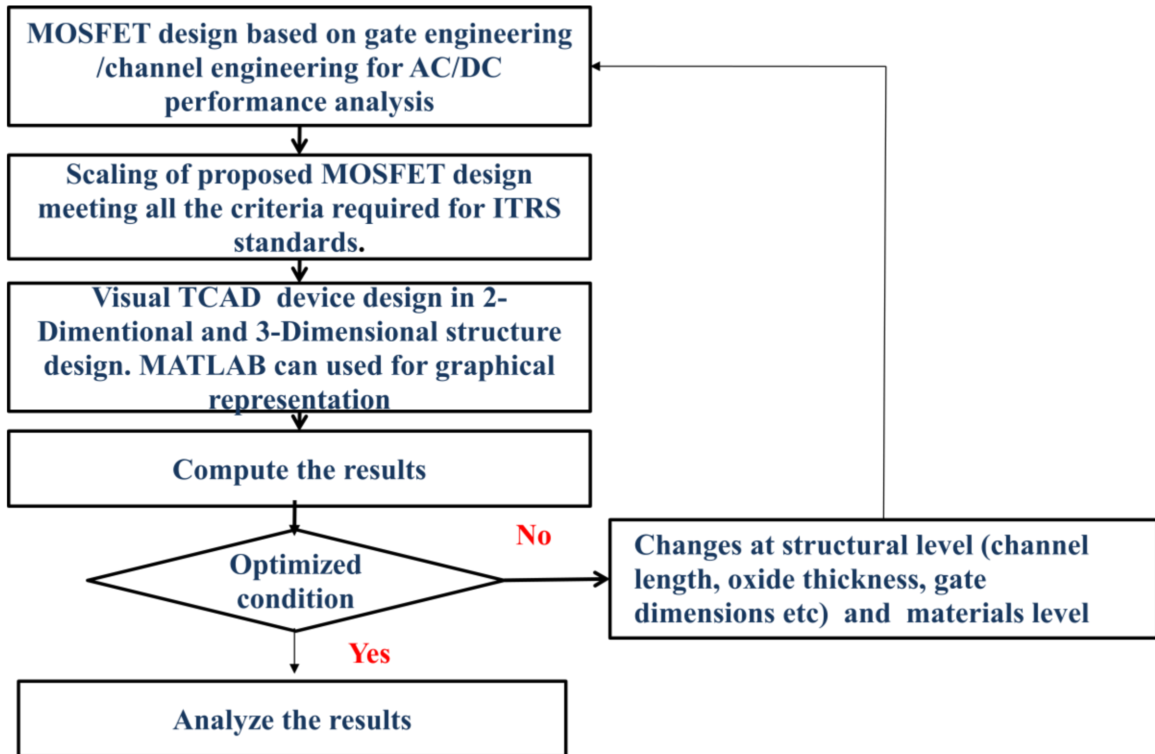


Figure 3.1: Design Methodology

3.2 Device structure and dimension of dopingless asymmetrical junctionless DG MOSFET

The proposed structure dopingless AJ DG MOSFET has two asymmetrical gates as shown in figure 3.1. The gates are in such a manner that they are unsymmetrical to each other The source and drain has different doping concentrations and the channel region is undoped. The channel length is calculated depending on the ON and OFF state of the MOSFET . MOSFET in its ON state has channel length equal to the overlapping region of the gates and MOSFET in its OFF state has channel length equal to the total channel length of the gate excluding the length of the overlapping region. The total channel length of the proposed MOSFET is taken as 18 nm. The channel length is 4 nm when the device

is in ON state (length of the overlapping region) and the channel length is 14 nm when the device is in OFF state (total channel length of MOSFET minus overlapping region). The source region has high doping concentration while the drain region is lightly doped and the channel is undoped having doping concentration as $1x10^{16}\ cm^{-3}$. The higher value of I_{ON} (ON-state current) with less value of I_{OFF} (OFF-current) has proven a satisfactory choice for low power and high speed applications. Visual TCAD is used for implementation of design .The dimensions of the device is given in table 3.1. Figure 3.2 and 3.3 shows the dopingless AJ DG MOSFET along with mesh when simulated in TCAD tool.

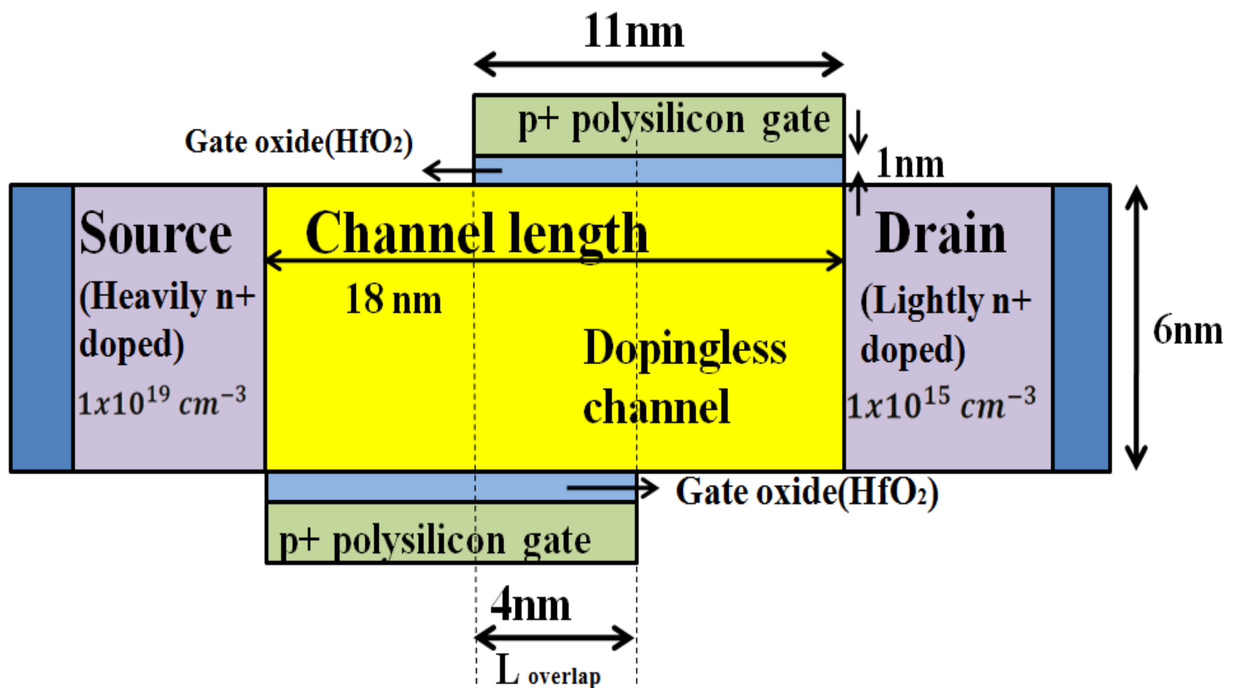


Figure 3.2 : Dopingless asymmetrical junctionless DG MOSFET

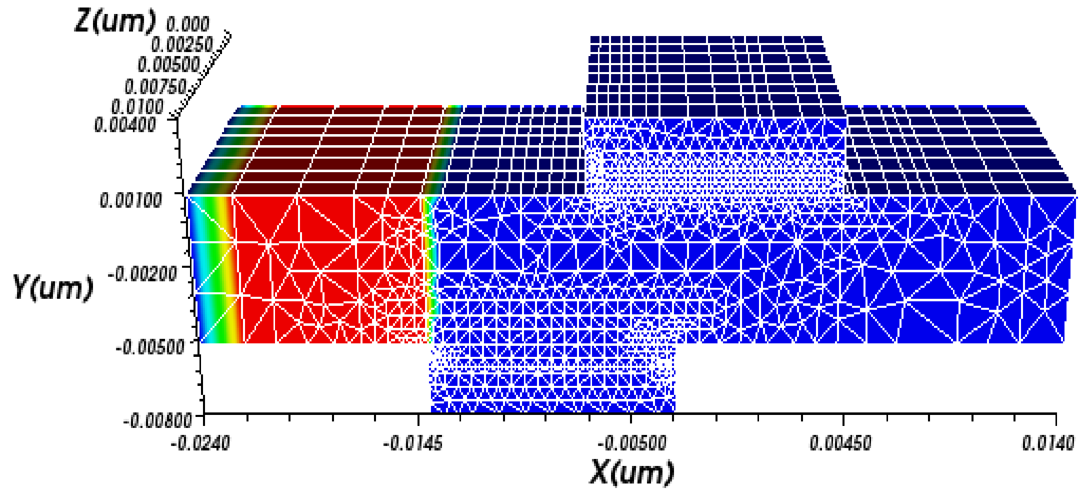


Figure 3.3 : 3-D view of simulated *dopingless AJ DG MOSFET along with mesh*

Table 3.1: Dimensions of the proposed dopingless AJ DG MOSFET

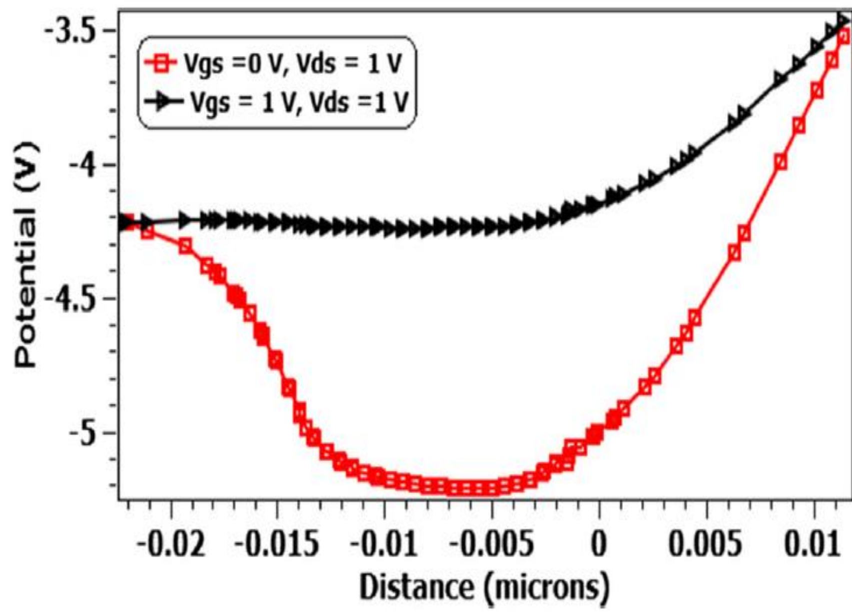
Region	Dimension
$Channel\ length$	$18\ nm$
$Gate\ length$	$11\ nm$
$Length\ of\ the\ overlap\ region$	$4\ nm$
$Thickness\ of\ silicon$	$6\ nm$
$Length\ of\ source/drain$	$8\ nm$
$Gate\ oxide\ thickness\ (HfO2)$	$1\ nm$
$Doping\ Concentration\ of\ source$	$1x10^{19}\ cm^{-3}$
$Doping\ Concentration\ of\ drain$	$1x10^{15}\ cm^{-3}$
$Doping\ Concentration\ of\ dopingless\ channel$	$1x10^{16}\ cm^{-3}$

3.3 Result and discussion

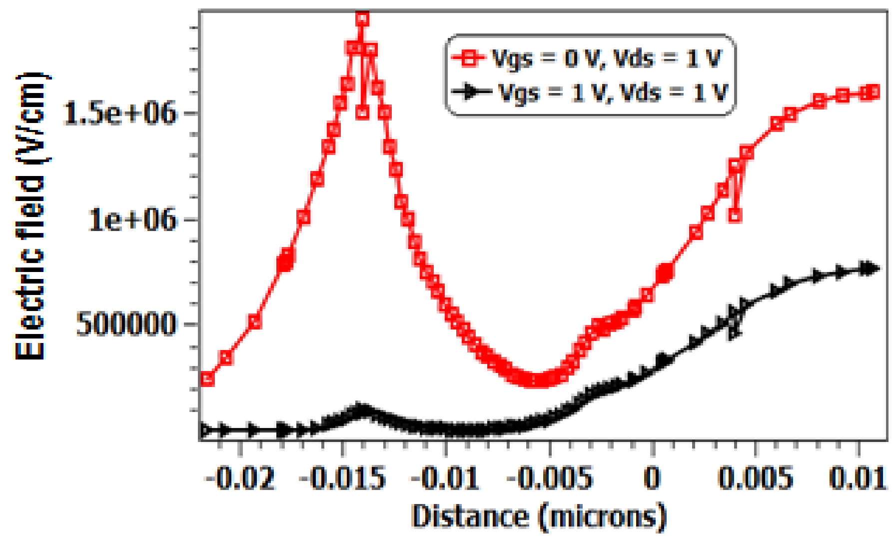
The proposed dopingless asymmetrical junctionless double gate MOSFET with 18 nm channel length is analyzed by using visual TCAD device simulator.

3.3.1 Electric potential , electric field and energy band diagram

Figure 3.4(a) depicts the fluctuation in the electric potential of a dopingless AJ DGMOSFET over time. The potential differential between the gate surface and the MOSFET bulk is known as electric potential. The potential of the channel area is reduced when the gate voltage is reduced. When the gate voltage is increased, the barrier height decreases (i.e. the force of the electric field producing the barrier decreases), and the channel potential rises, increasing the drain current. The electric field of dopingless AJ DG MOSFET along the distance of the channel is shown in figure 3.4(b) . Sudden increase in electric field in the channel region occurs at low voltage suppressing the leakage current during the OFF-state of the device. As voltage bias increases the spike in the electric field also reduces. Figure 3.4 (c) presents the energy band diagram of a dopingless AJ DG MOSFET over the channel length, with Ec and Ev representing the conduction and valence band edges, respectively. When a positive gate voltage ($V_{gs} > 0$) is applied during the ON state, an increase in electron concentration along the oxide and semiconductor interface occurs, lowering the barrier and allowing more electrons to pass from source to drain. The barrier height grows in the OFF state, suppressing leakage current.



(a)



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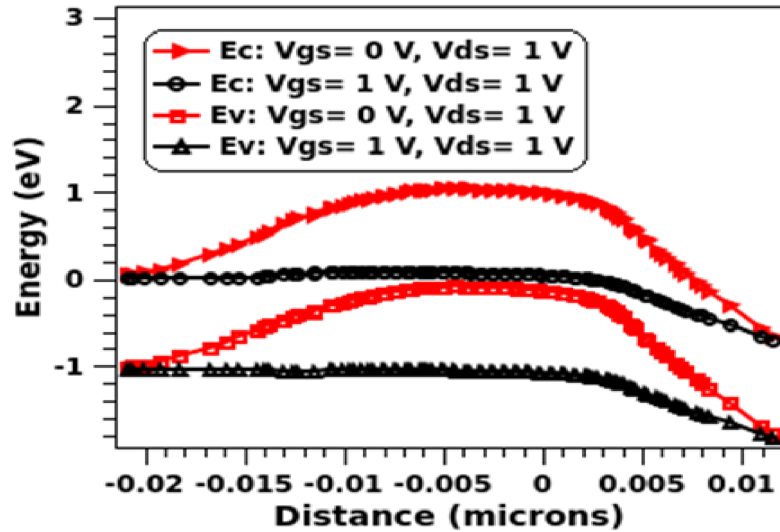


(c)

Figure 3.4: (a) Electric potential of dopingless AJ DG MOSFET (b) Electric field of dopingless AJ DG MOSFET (c) Energy band diagram of dopingless AJ DG MOSFET

3.3.2 ON State Current and OFF State Current of the Proposed Device

The suggested dopingless asymmetrical junctionless double gate MOSFET with 18 nm channel length was investigated using the drift diffusion model in the visual TCAD device simulator. In n channel MOSFETs, electrons make up the majority of charge carriers. The drain, source, and channel all have different doping concentrations. If the concentration of electron density is raised with a commensurate drop in the concentration of holes, gate voltage and drain voltage rise. The doping concentration of the source is increased to $1x10^{19}cm^{-3}$, which is identical to that of the channel area, while the drain is lowered to $1x10^{15}cm^{-3}$. The channel section, which is built of a thin silicon wafer, is undoped with doping concentration $1x10^{16}$ cm^{-3} . To reduce the hot electron impact, the drain area has a reduced doping concentration. Because of MOSFET scaling, the electric field at the drain gets extremely strong, dislodging the holes. As a result, the drain has a reduced doping concentration to reduce such consequences. The undoped channel has a better carrier mobility and decreases threshold voltage variations produced by random

dopant fluctuation. The source, drain, and channel regions are built of a 6 nm thick silicon wafer.

The proposed device has higher ON state current and lower OFF state current therefore increasing the ratio between I_{ON} and I_{OFF} enhancing the performance of the device shown in figure 3.5. The undoped channel has a better carrier mobility, and the threshold voltage change due by random dopant fluctuation is reduced, considerably reducing short channel effects (SCEs).The comparison between ON and OFF state current of dopingless AJ DG MOSFET and doped AJ DG MOSFET of I_{ON} and I_{OFF} current is shown in table 3.2[67][79][80].

Table 3.2: Comparison of ON state and OFF state current of dopingless AJ DG MOSFET and doped AJ DG MOSFET .

Device Structure	I_{ON}	I_{OFF}
Dopingless AJ DG MOSFET	$1.37\ x10^{-17}\ \ A/\mu m$	$3.80\ x\ 10^{-6}\ A/\mu m$
Doped AJ DG MOSFET	$1.15\ x10^{-16}\ A/\mu m$	$7.49\ x\ 10^{-5}\ A/\mu m$

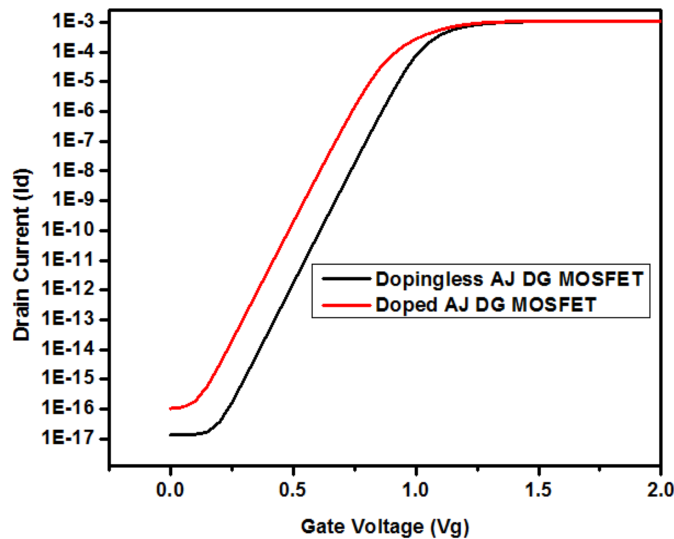
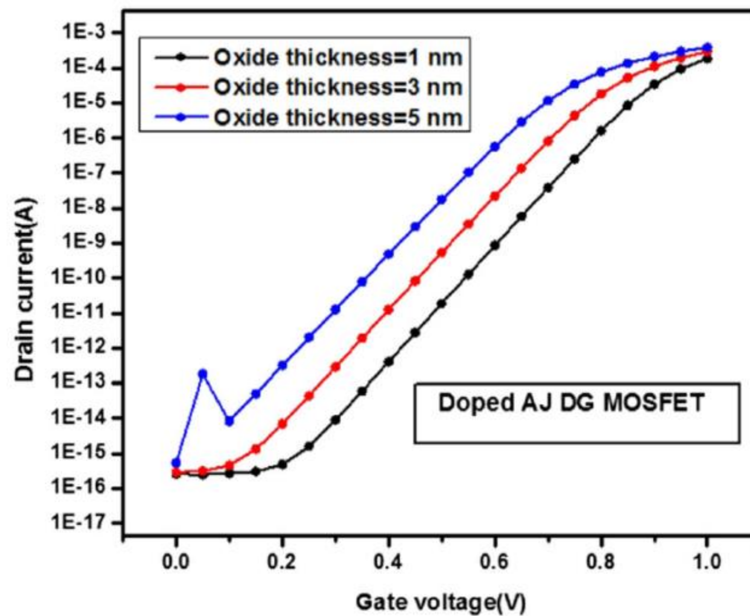


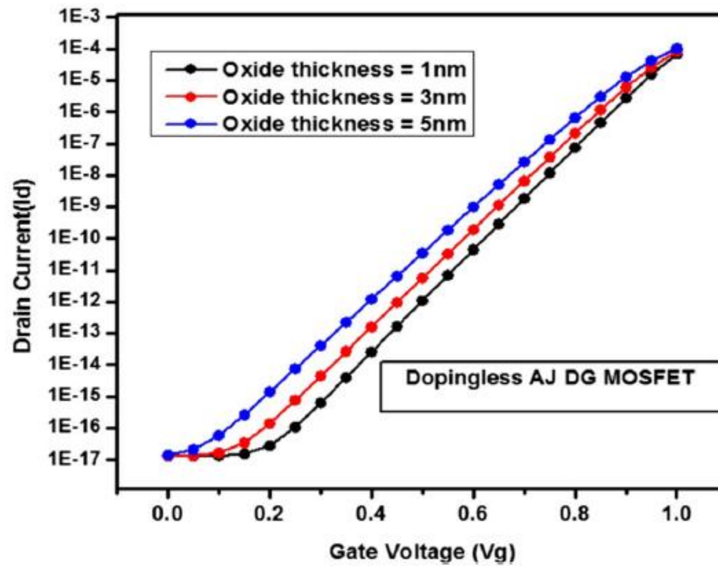
Figure 3.5: V_{gs} versus I_d graph for dopingless AJ DG MOSFET and doped AJ DG MOSFET

3.3.3 Sensitivity Analysis of the Proposed Device

Figure 3.6 (a) and (b) illustrate the sensitivity of 18 nm dopingless AJ DG MOSFETs and 18 nm AJ MOSFETs with equal doping of channel length and a 15% difference in oxide thickness (b). The oxide thicknesses that are taken into account are 1nm, 3nm, and 5nm. The gate has good control over the channel region as the oxide thickness lowers. The drain current of a dopingless AJ DG MOSFET varies consistently throughout the gate voltage, and the OFF-state decreases as the oxide thickness decreases, as seen in the graph. When compared to dopingless AJ DG MOSFET, doped AJ DG MOSFET with equal doping creates a kink at lower voltage and is not uniform. The surface trap at the gate causes the kink in doped AJ DG MOSFETs. The surface trap density grows as the oxide thickness increases, and gate control over the channel decreases, causing the kink to develop. As a result, dopingless AJ DG MOSFETs perform better and are less susceptible to changes in gate oxide thickness.

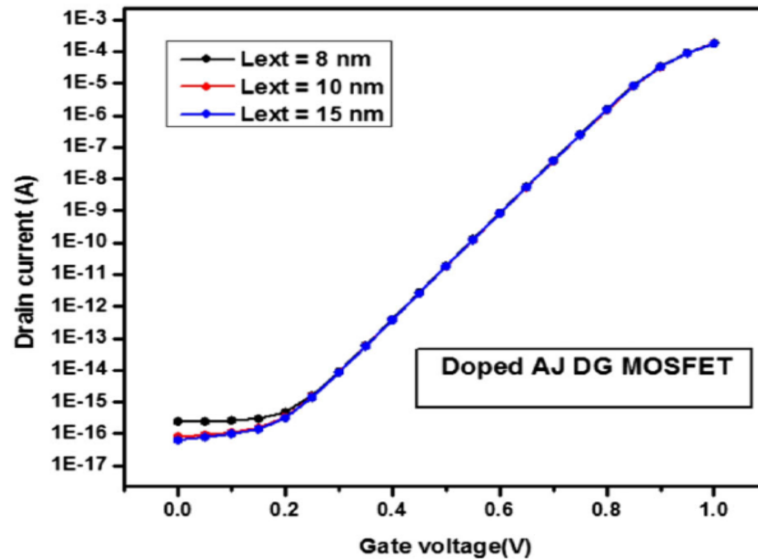


(a)

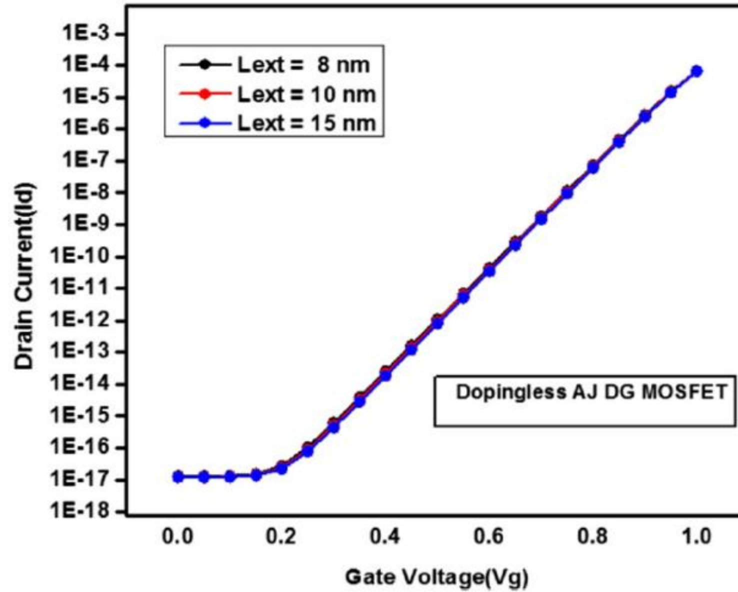


(b)

Figure 3.6: Gate voltage versus drain current graph of (a) Variation in oxide thickness of doped AJ DG MOSFET (b) Variation in oxide thickness of dopingless AJ DG MOSFET of 18nm.



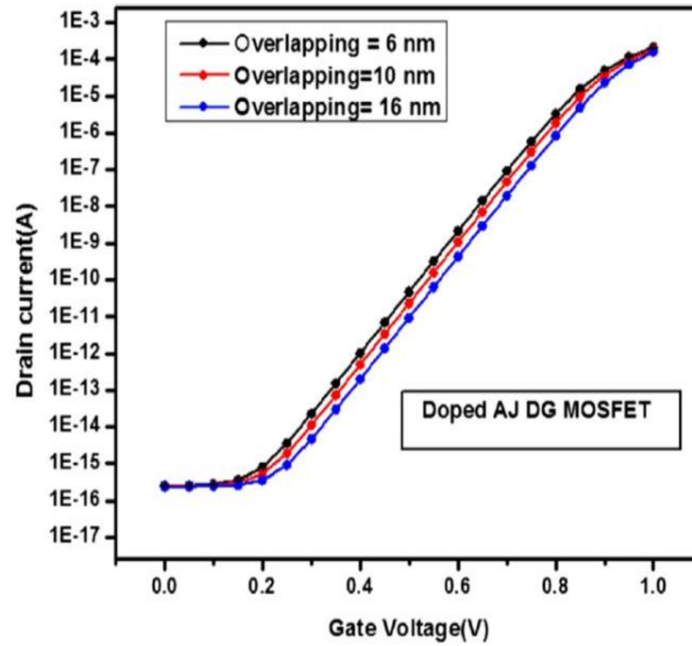
(a)



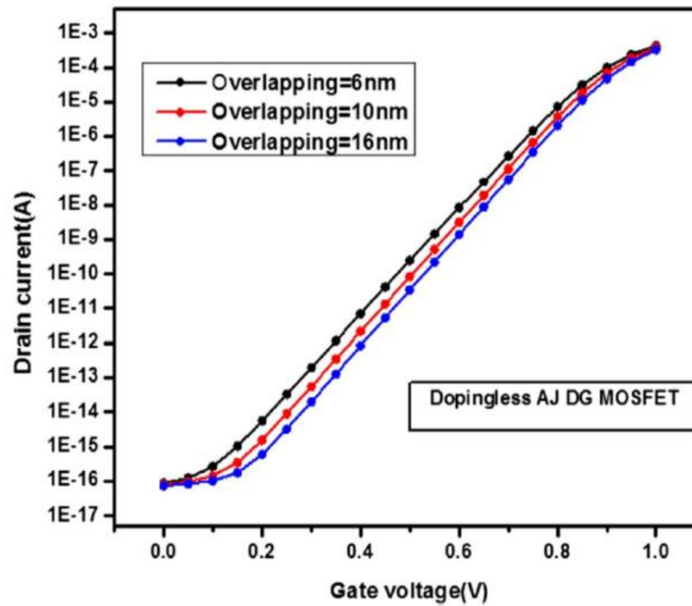
(b)

Figure 3.7 :Gate voltage versus drain current graph of (a) Variation in length of drain extension of doped AJ DG MOSFET (b) Variation in drain extension of dopingless AJ DG MOSFET

Figure 3.7(a) and (b) illustrate the sensitivity of dopingless AJ DG MOSFETs and AJ DG MOSFETs with equivalent doping when the drain length (L_{ext}) is varied (b). Drain lengths of 8nm, 10nm, and 15nm are taken into account. When comparing dopingless AJ DGMOSFETs with 18 nm channel lengths to AJ DG MOSFETs with equal doping, it can be shown that the OFF state current is suppressed. The leakage current of doped AJ DGMOSFETs in the subthreshold region increases due to random dopant fluctuation that causes change in threshold voltage. As a result, dopingless AJ DG MOSFETs are less sensitive than AJ DG MOSFETs with equivalent doping. As a result, dopingless AJ DG MOSFETs are more robust and less sensitive when the drain length is changed, and the change in OFF state current is insignificant.



(a)



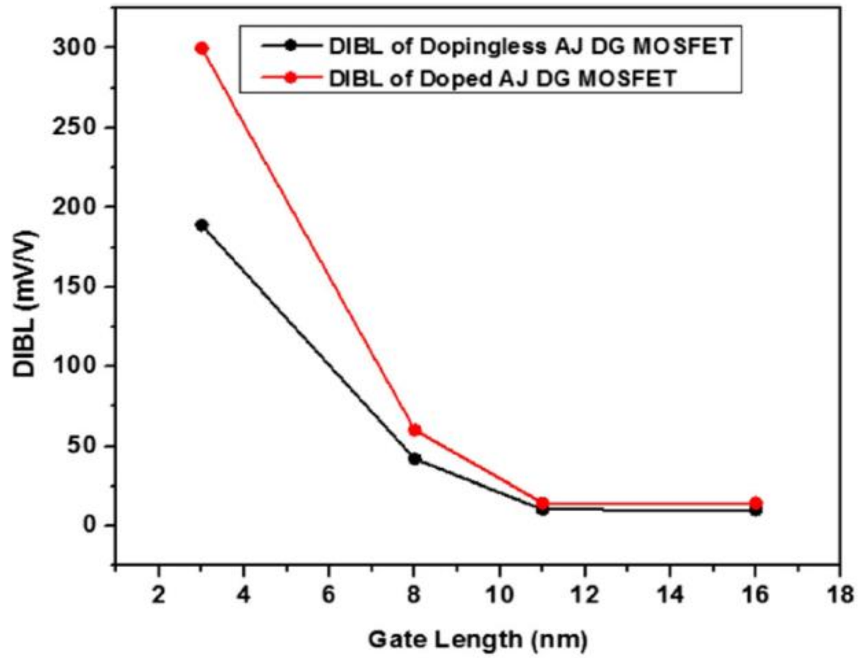
(b)

Figure 3.8: Gate voltage versus drain current graph (a) Variation in the overlapping region of doped AJ DG MOSFET of (b) Variation in an overlapping region of dopingless AJ DG MOSFET

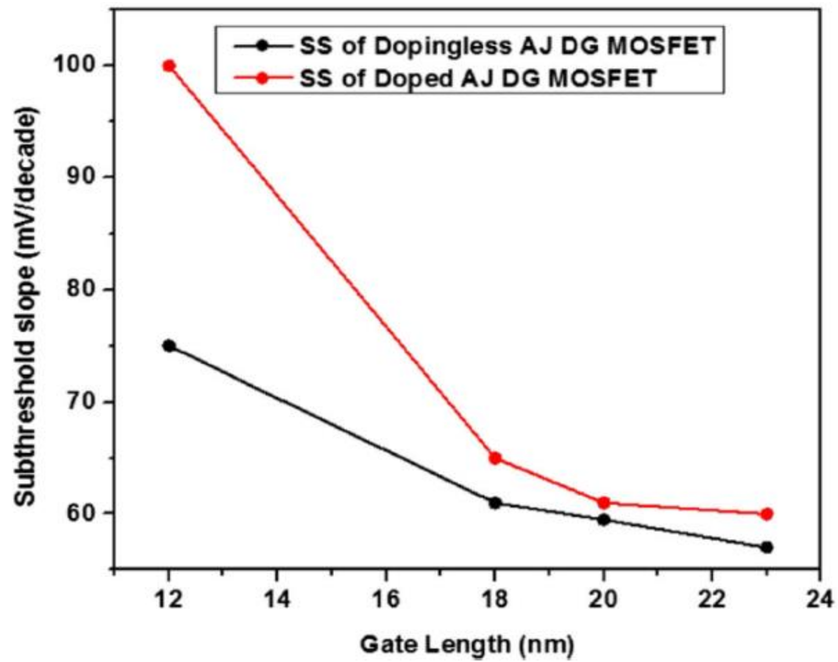
Figures 3.8 (a) and (b) illustrate the gate voltage against drain current for dopingless AJ DG MOSFETs and AJ DG MOSFETs with equal doping when the length of the overlapping zone is adjusted. The overlapping lengths are 6 nm, 10 nm, and 16 nm, respectively. The difference in the graph for dopingless AJ DG MOSFETs is less than for AJ DG MOSFETs with equivalent doping, according to the findings. Variation in overlap area length while maintaining gate length has no influence on subthreshold performance and is advantageous if there is any misalignment. As a result, dopingless AJ DG MOSFETs may be a good fit for high-performance, low-power applications.

3.3.4 Reduction in Short Channel Effects (SCEs)

DIBL (drain induced barrier lowering) is a short-channel phenomenon in which the threshold voltage decreases as the drain voltage increases. The DIBL ratio is calculated mathematically using the dV_{gs}/dV_{ds} formula. For a gate length of 18 nm, the DIBL ratio is 10.5 mV/V. Subthreshold slope ($SS= dV_{gs}/d(logI_d)$) is a SCE that results from leakage current in the subthreshold zone. SS is determined by the slope of the gate voltage and drain during the subthreshold region. The device's performance is harmed by this option. When compared to the other structures in Table 3.3, the suggested structure has an SS of 59.5 mV/decade, which is lower. The DIBL and SS values of dopingless AJ DG MOSFET and doped AJ DG MOSFET are compared in figure 3.9 (a) and (b). In compared to doped AJ DG MOSFET, the DIBL and SS values are suppressed for dopingless AJ DG MOSFET. As a result, the proposed structure outperforms the competition. By constructing biosensing cavity areas of various sizes in the dopingless AJ DG MOSFET, it may be employed as a biosensor [81-83].



(a)



(b)

Figure 3.9 (a) DIBL values at different gate length of dopingless AJ DG MOSFET and doped AJ DG MOSFET (b) SS values at different gate length of dopingless AJ DG MOSFET and doped AJ DG MOSFET

3.3.5 Different gate contact materials

Figure 3.10 depicts the performance of MOSFETs when various gate contacts, such as aluminium, polysilicon, and copper, are employed. When polysilicon is utilised as a gate contact, MOSFETs function better. Metal gates, such as aluminium and copper, operate at voltages ranging from 3 to 5 volts. Polysilicon gate contacts are used when operating voltages are reduced. We can see from the graph that polysilicon gate contacts perform better at lower operating voltages since the OFF-state current is low. Whereas the OFF-state current of MOSFET with copper and aluminum contact is very high that degrades its performance. The MOSFET shown in this paper is operated at 1V. Other reasons for using Polysilicon contact are during the process of fabrication the metal contact like Al and Cu forms misalignment which gives rise to parasitic capacitances and the doping process requires high-temperature annealing process which will melt Al and Cu. The polysilicon does not melt at high temperatures and provides a solution for misalignment by using the self-alignment process[12].

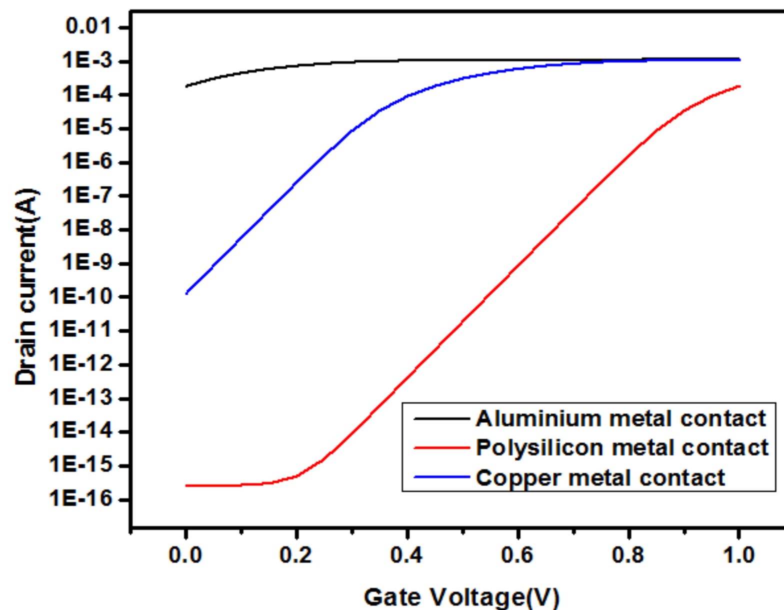


Figure 3.10: Vgs versus Id plot of different gate contact material.

Table 3.3 : Comparison of performance parameters of different MOSFET structures

Reference	I_{ON}	I_{OFF}	I_{ON}/I_{OFF}	**SS(=** $\frac{dV_{gs}}{d(logI_d)}$**)**	**DIBL(=** $\frac{\partial V_{gs}}{\partial V_{ds}}$**)**	**Channel Length**
(GC-DMGJL) MOSFET(2018) [40]	7.695 x 10^{-4} A/µm	3.74x 10^{-10} A/µm	2.06 x10^{6}	73.42 mV/dec	21 mV/V	15 nm
AJ DG MOSFET,(2016) [46]	127 µA/µm	0.001 nA/µm	1.27 x10^{5}	68 mV/dec	65mV/V	20 nm
(DMSG) MOSFET(2011)[30]	-	1.053x 10^{-16} A	-	64.7978 mV/dec	-	10 nm
JLDG, (2012)[31]	-	-	4.86 x10^{9}	62.32 mV/dec	75.98 mV/V	20 nm
DG MOSFET	-	-	4.03 x10^{9}	63.34 mV/dec	79.58 mV/V	20 nm
AJ DG MOSFET with n+ pocket region,(2020)	1.88 x 10^{-4} A/µm	9.7x10^{-17} A/µm	5.15x10^{13}	59 mV/decade	13.4 mV/V	20 nm
Dopingless AJDG MOSFET	3.80 x 10^{-6} A/µm	1.37x 10^{-17} A/µm	2.77x 10^{11}	59.5 mV/decade	10.5 mV/V	18 nm

Table 3.4 : Comparison table of improvement/deterioration in performance parameters of proposed dopingless AJ DG MOSFET in percentage.

Device	**SS**	**DIBL**
Dopingless AJDG MOSFET	4.52 % improvement	87.3 % improvement
AJ DG MOSFET with n+ pocket region	5.32 % improvement	82.36% improvement

3.3.6 Temperature analysis

The temperature analysis of dopingless AJ DG MOSFET is shown in figure 3.11. Variation of temperature ranges from 250 to 400 K with step size 50 K. With increasing temperature the OFF state current increases and ON state current has no significant change. OFF state current obtained at 250 K is 2.36 $x10^{-19}$, 300 K is 3.5 x 10^{-17}, 350 K is 1.64 $x10^{-15}$ and 400 K is 5.56 $x10^{-14}$. When temperature increases, increase in the OFF state current or the leakage current is observed which occurs due to two reasons (1) current produced as result of thermal generation (2) current produced as a result of impact ionization (process that forms electron hole pairs in large amount that causes leakage through the depletion region producing current. Therefore a reduction in I_{ON} /I_{OFF} ratio is observed thereby degrading the device performance.

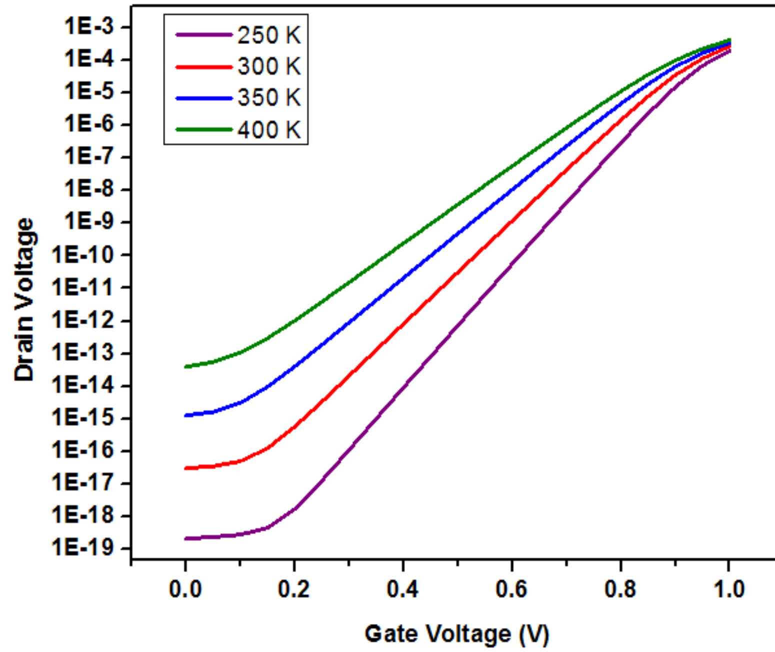


Figure 3.11: Temperature Analysis of dopingless AJ DG MOSFET

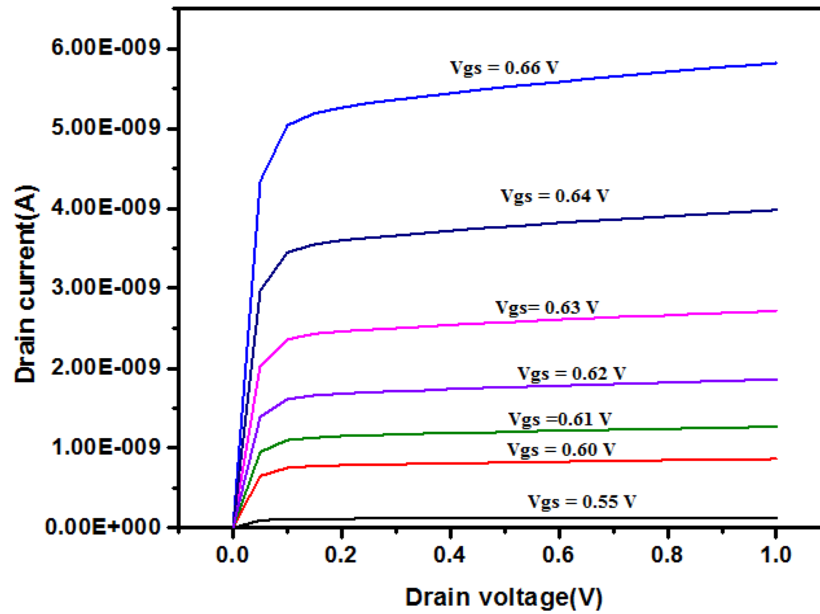


Figure 3.12 : Graph of drain voltage versus drain current

Figure 3.12 depicts a graph of drain current vs. drain voltage, with the gate voltage held constant at 0.55V, 0.60V, 0.61V,0.62V,0.63V, 0.64 V, and 0.66V. When the threshold voltage is 0 in the MOSFET's OFF state, no drain current flows. As the drain voltage rises, the drain current begins to flow and eventually becomes constant, as seen by the horizontal lines. The graph shows that with a substantial change in the drain voltage, the variation in drain current is relatively minimal, indicating that the gate has more control over the channel and a high output impedance, which is perfect for a transistor amplifier circuit.

3.4 Summary

The gates of the proposed 18nm dopingless AJ DG MOSFET are asymmetrical to their other. The drain, source, and channel all have different doping concentrations. Short channel effects (SCEs) are suppressed more in dopingless AJ DG MOSFETs, resulting in improved device performance. The I_{ON}/I_{OFF} ratio increases ($\sim 2.77 \times 10^{11}$), the decrease in the value of SS (59.5 mV/V) and DIBL (10.5 mV/V) value is seen . A sensitivity analysis is carried out and noticed between dopingless AJ DG MOSFETs and AJ DG MOSFETs with equal doping. Different factors relevant to the sensitivity of dopingless AJ DG MOSFETs, such as drain extension, gate overlapping length, and oxide thickness, are varied in both device topologies. The sensitivity of the dopingless AJ DG MOSFET is poor when the parameters are changed, according to the findings. Temperature analysis was carried out at temperatures of 250 K, 300 K, 350 K, and 400 K.

CHAPTER 4

HEAVILY DOPED N+ POCKET ASYMMETRICAL JUNCTIONLESS DOUBLE GATE MOSFET

In this chapter the proposed device is analyzed by calculating I_{on} and I_{off} current .The dimensions of the device are mentioned in tabular form and SCEs like DIBL and SS are calculated . The device simulation is done through 2D visual Technology Computer-Aided Design (TCAD) device simulator.

4.1 Device structure and dimension of dopingless asymmetrical junctionless DG MOSFET with n+ pocket

Heavily n+ doped pocket AJ DG MOSFET has two gates arranged asymmetrically to each other, as shown in figure 4.1. Introduction of a heavily doped n+ pocket region is near the source end of the MOSFET is done.The thickness of the pocket region is taken as $1/3^{rd}$ of the length of the channel. The material used as gate contact is p+ polysilicon. The gate oxide is made up of high-k dielectric material HfO_2. Material used for the drain, source and channel is thin film silicon. The source region has high doping concentration same as that of the n+ pocket region, improving the ON current of the device. The drain region has low doping concentration, to reduce the OFF-state current, therefore providing better I_{ON}/I_{OFF} ratio. The channel length changes during the ON and OFF state of the device. MOSFET in its ON state has channel length equal to the overlapping region of the gates and MOSFET in its OFF state has channel length equal to the total channel length of the gate excluding the length of the overlapping region. Figure 4.2 represents 3-D Schematic of asymmetrical junctionless DG MOSFET with n+ pocket region using TCAD simulation.

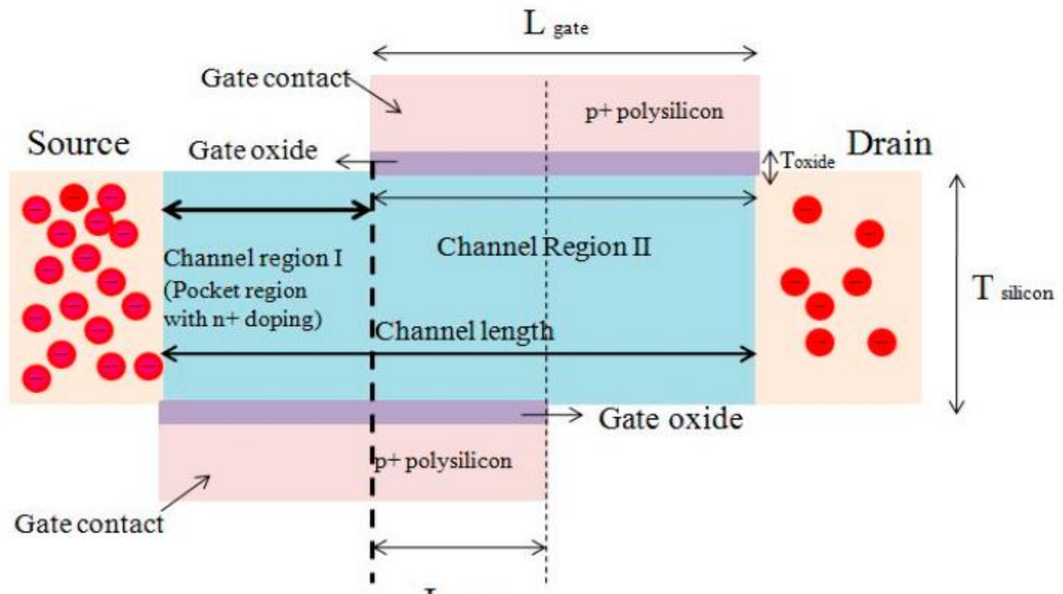


Figure 4.1 : Design of asymmetrical junctionless DG MOSFET with n+ pocket region

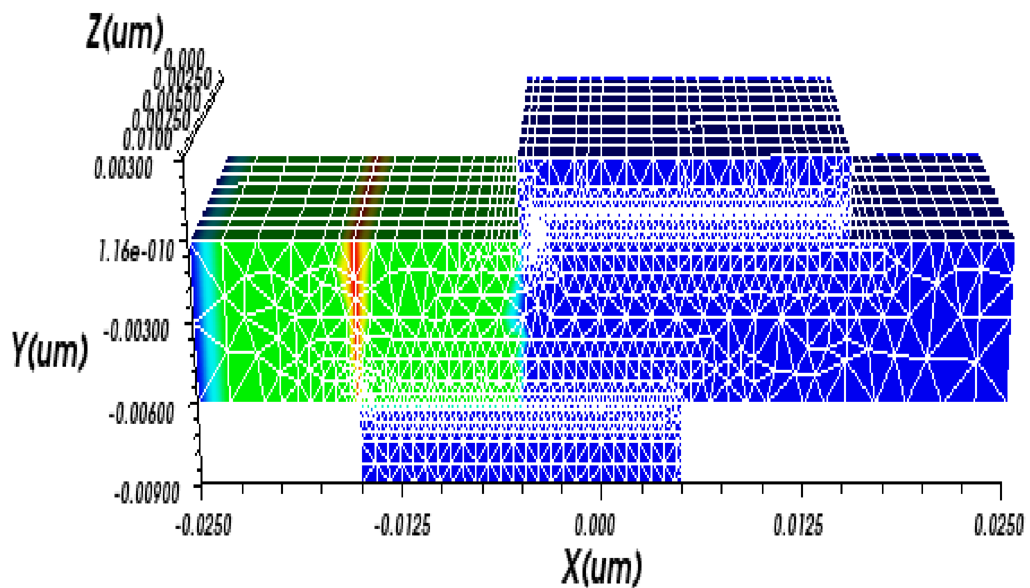


Figure 4.2 : 3-D Schematic of asymmetrical junctionless DG MOSFET with n+ pocket region using TCAD simulation

Table 4.1: Dimensions of the proposed heavily doped n+ pocket AJ DG MOSFET

Region	Dimension
Gate length	20 nm
Length of the overlap region	10 nm
Thickness of silicon	6 nm
Length of the pocket region	10nm
Length of source/drain	8nm
Gate oxide thickness(HfO_2)	1 nm
Doping Concentration of pocket region	$1 \text{x} 10^{22} cm^{-3}$
Doping concentration of channel region II	$1 \text{x} 10^{19} cm^{-3}$

4.2 ON State Current and OFF State Current of the Proposed Device

Figure 4.3 shows comparison between the ON and OFF state of the device with and without the n+ pocket region. The observation made from the figure is that AJ DG MOSFET with an n+ pocket region has greater I_{ON}/I_{OFF} ratio in comparison to AJ DG MOSFET without an n+ pocket region. Table 4.2 compares I_{ON}/I_{OFF} between the different device structures. Heavily doped n+ pocket AJ DG MOSFET has I_{ON}/I_{OFF} ratio as 10^{13}, which is greater than other devices, indicating that proposed device performs better.

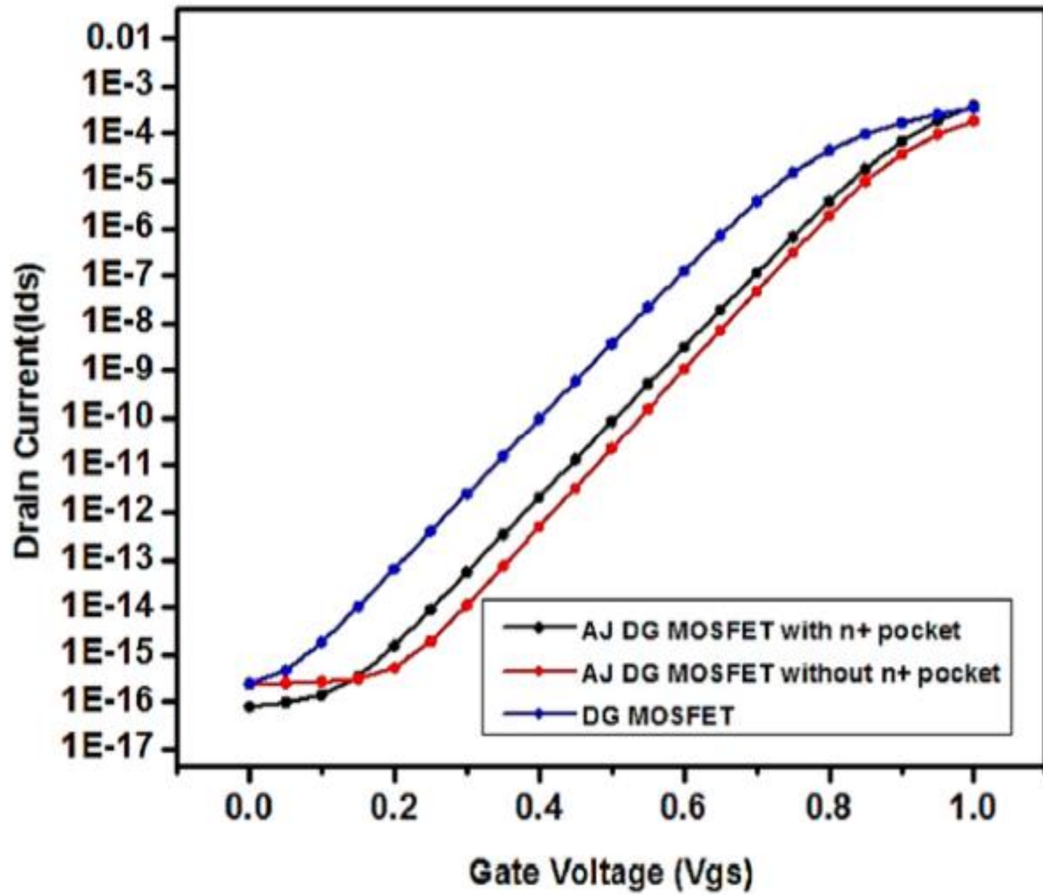


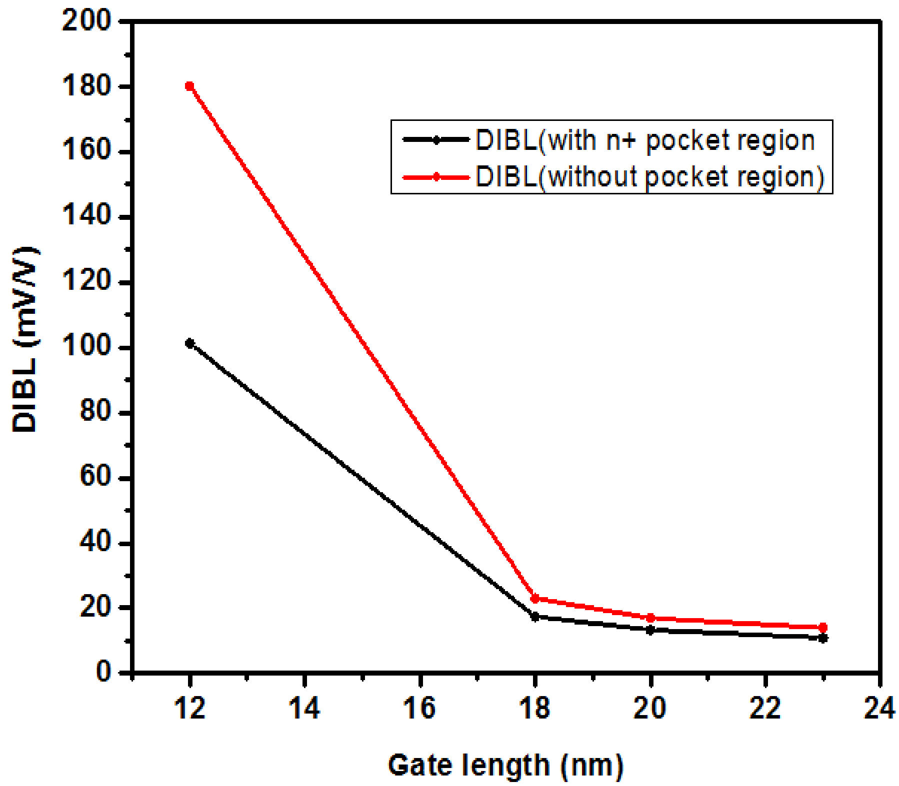
Figure 4.3 :Drain current variations concerning gate voltage for heavily doped n+ pocket AJ DG MOSFET.

Table 4.2: Comparison of ON state and OFF state current of AJ DG MOSFET with n+ pocket region and AJ DG MOSFET without pocket region

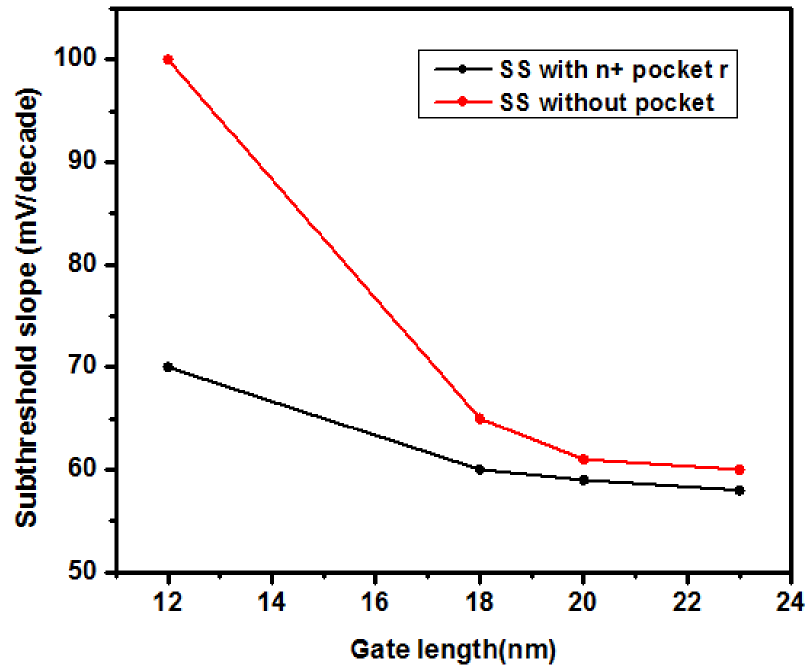
Device structure	I_{ON}	I_{OFF}
Heavily doped n+ pocket AJ DG MOSFET	1.88 x 10^{-4} A/µm	9.7 x 10^{-17} A/µm
AJ DG MOSFET without pocket	1.47 x10^{-4} A/µm	9.60 x 10^{-14}A/µm

4.3 Reduction in Short Channel Effects (SCEs)

The DIBL ratio is calculated mathematically using the V_{gs}/dV_{ds} formula. For a gate length of 20 nm, the DIBL ratio is 13.4 mV/V. Subthreshold slope ($SS= dV_{gs}/d(logI_d)$) is a SCE that results from leakage current in the subthreshold zone. SS is determined by the slope of the gate voltage and drain during the subthreshold region. The device's performance is harmed by this option. Subthreshold slope ($SS= dV_{gs}/d(logI_d)$) is a SCE that results from leakage current in the subthreshold zone. SS is determined by the slope of the gate voltage and drain during the subthreshold region. The suggested device's SS and DIBL values are 59 mV/decade and 13.4 mV/V, respectively. The DIBL and SS comparison between the AJ DG MOSFET with n+ pocket and the AJ DG MOSFET without pocket is shown in Figure 4.4.



(a)



(b)

Figure 4.4 (a) DIBL values at different gate length of AJ DG MOSFET with n+ pocket and AJ DG MOSFET without pocket (b) SS values at different gate length of AJ DG MOSFET with n+ pocket and AJ DG MOSFET without pocket.

Table 4.3: *Comparison of existing MOSFET structures.*

Existing MOSFET structure andmethodology	**Electrical performance and applications**
Ge pockets are inserted in SOI JLT	Lowers the temperature of the lattice. The length of the channel is 20 nm.
GAA JLMOSFET with source and drainextension	The heavily doped areas have also resulted in a 70% rise in the magnitude of I_{ON} current.

Gate engineering using DG MOSFET	The sub-threshold slope is reduced by 1.61 percent, while the ON/OFF current ratio is boosted by 17.08 percent and DIBL is reduced by 4.52 percent. The length of thechannel is 20 nm.
Gate material engineering and drain/source Extensions	Enhances RF and analogue performance. When compared to typical double-gate junctionless MOSFETs, the figure of merit is also boosted. The length of the channel is 100 nm.
Inducing source and drain extensions electrically	Suppresses short-channel effects and hot electron effects for channel lengths less than 50 nm.
Formation of cavity of size in nm by etching of gate oxide inthe channel from both the sidesof source and drain	The dielectric modulation approach is used to detect biomolecules such as DNA, enzymes, and cells. The length of the channel is 100 nm.
GC − DMGJLMOSFET	The GC DMGJL MOSFET as a high drain current and transconductance while also minimising short-channel effects. The channel length is 30 nm

BP is integrated with the JL recessed MOSFET	The structure drain current rises to 0.3 mA. The off current decreases, and the subthreshold slope improves. The length of the channel is 44 nm.
Fully depleted tri material DG MOSFET is used	RF performance, linearity, and analogue performance are improved over DM-DG MOSFETs and single-material DG MOSFETs. The length of the channel is 35 nm.
Pocket region is constructed near the source & drain region and is heavily doped	Good resistance to short-channel effects and ability to fulfill OFF-state and ON-state current standards. The length of the channel is 20 nm.

4.4 Summary

The attributes of an n+ pocket AJ DG MOSFET for low-power subthreshold characteristics are examined in this chapter. The I_{ON}/I_{OFF} current ratio is 10^{13}, which is quite high. The device has an SS of 59 mV/dec and a DIBL of 13.9 mV/V, indicating that it is suited for low-power applications.

CHAPTER 5

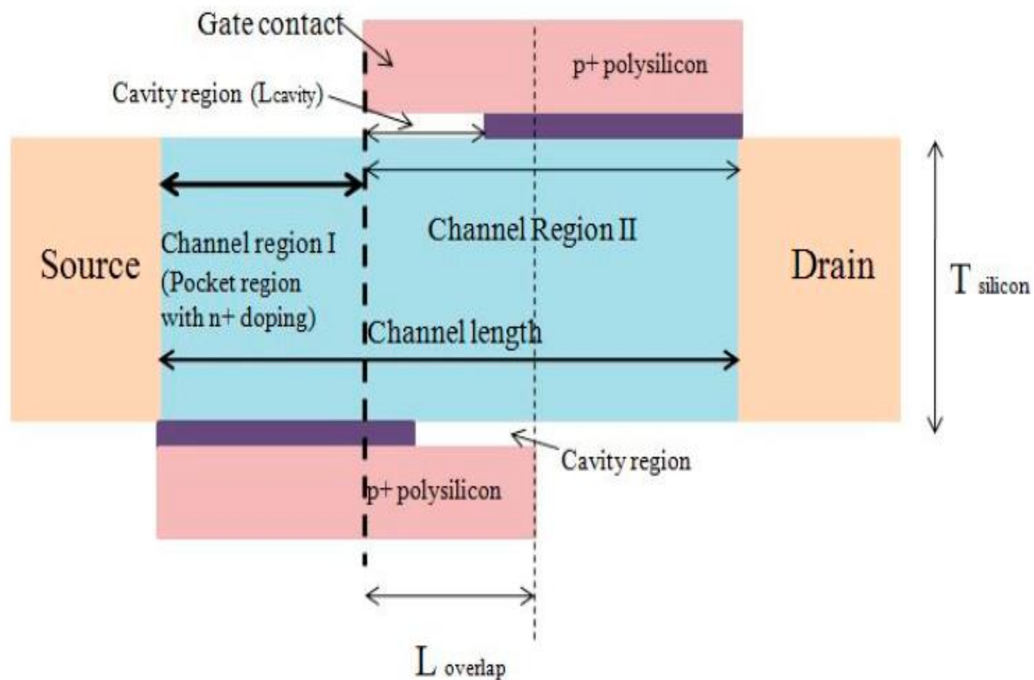
APPLICATIONS OF THE PROPOSED DEVICES

The applications of asymmetric gate junctionless MOSFETs are discussed in this chapter. It outlines the findings gained for the proposed device's biomedical and low-power applications. Detecting illnesses and chemicals such as cancer, antigens, viral infections, and pathogens has proven time-consuming and difficult. Detecting biomolecules such as DNA, enzymes, viruses, cancer, and other biomolecules with biosensors based on field-effect transistors (FET) is cost-effective and time-consuming, and can be utilised for early-stage illness detection [84]. Different biosensors have been developed, including piezoelectric, nanomechanical, optical, and electrochemical sensors, however they need expensive production procedures and equipment. MOSFET-based biosensors provide a straightforward detection mechanism that does not need the usage of a transducer [85]. The fabrication industry can make junctionless transistors for sensing biomolecules in huge numbers at a low cost [86]. The ISFET (ion-sensitive field effective transistor) used in FET-based biomolecule detection recognises charged biomolecules but not neutrally charged biomolecules. FET-based biosensors work by using the electrical characteristics of the devices (i.e., ON-state current, threshold voltage and capacitances, etc.). In dielectrically modulated FETs, a cavity is created in the gate dielectric (DM FETs).

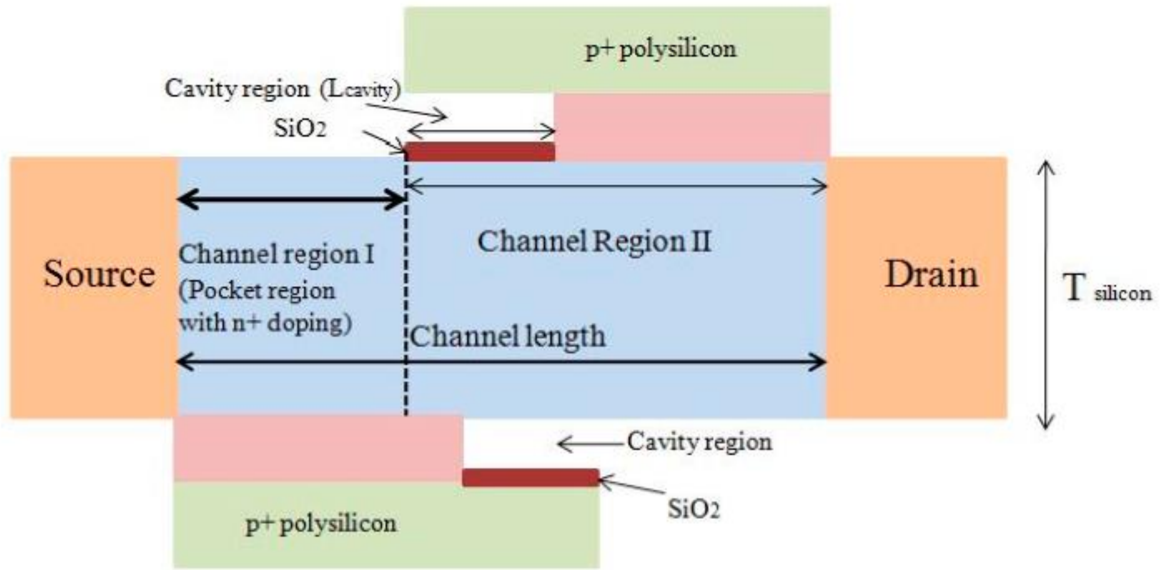
5.1 Proposed Heavily Doped n+ Pocket AJ DG MOSFET with a Nanogap-Cavity Region

In gate oxide region of n+ Pocket AJ DG MOSFET a cavity a formed and a dielectric material is filled in it as shown in figure 5.1 . Variation in the length and height of the nanogap cavity region and variation in dielectric materials is done for analyzing the sensitivity of device required for detecting biomolecules. Dielectric materials like air, SiO_2, HfO_2 and $S3N_4$ were considered for the analysis. Electrical characteristics such as the dielectric constant are used to detect phenomena. The cavity's height (Hcavity) is 1 nm. Figure (b) shows n+ pocket AJ DG MOSFET having SiO_2 layer with a cavity region

to provide binding of biomolecules entering the cavity for restricting their movements. The cavity height (H_{cavity}) is taken as 2.7 nm and the width SiO_2 is taken as 0.3 nm. For analyzing device sensitivity for the detection charged particles were introduced in the cavity[87] . A thin layer deposition technique and wet etching process is used for formation of cavity region. The sensitivity of cavity region for biomoleclues detection is analyzed using the dielectric modulation technique based on the threshold voltage shifting by varying the dielectric properties. Many biomolecules like DNA, enzymes, etc., are charged. Therefore the affect in DM AJ DG MOSFET can be observed the when charge biomolecules enters the cavity area [88].



(a)



(b)

Figure 5.1: (a) n+ pocket AJ DG MOSFET with a cavity region; (b) n+ pocket AJ DG MOSFET with a cavity region over a SiO_2 layer

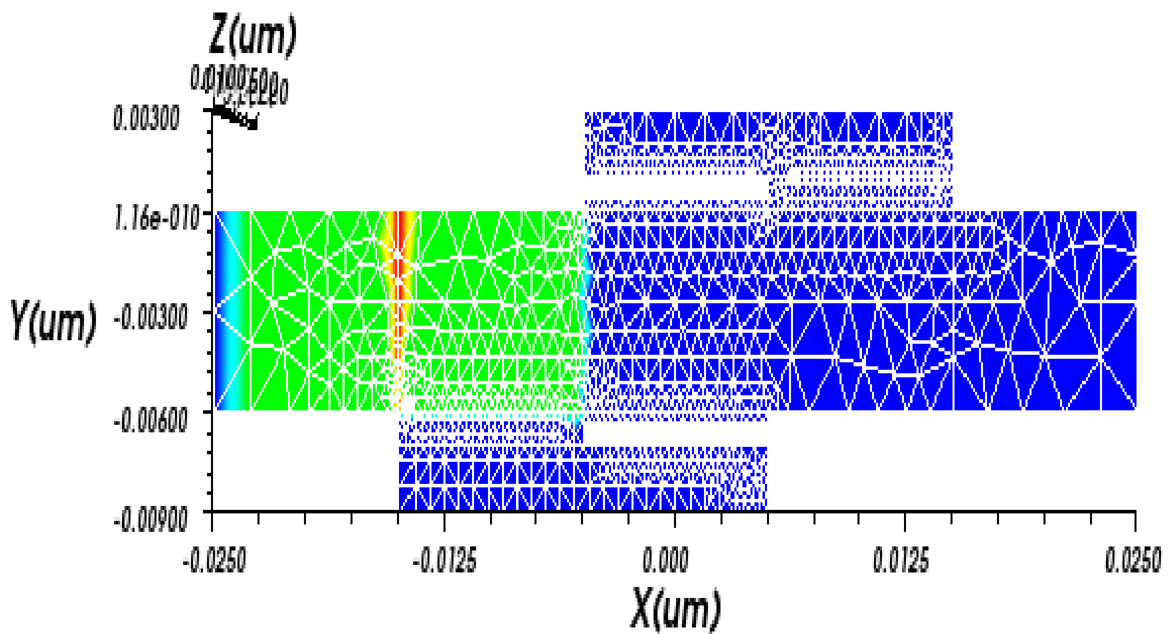
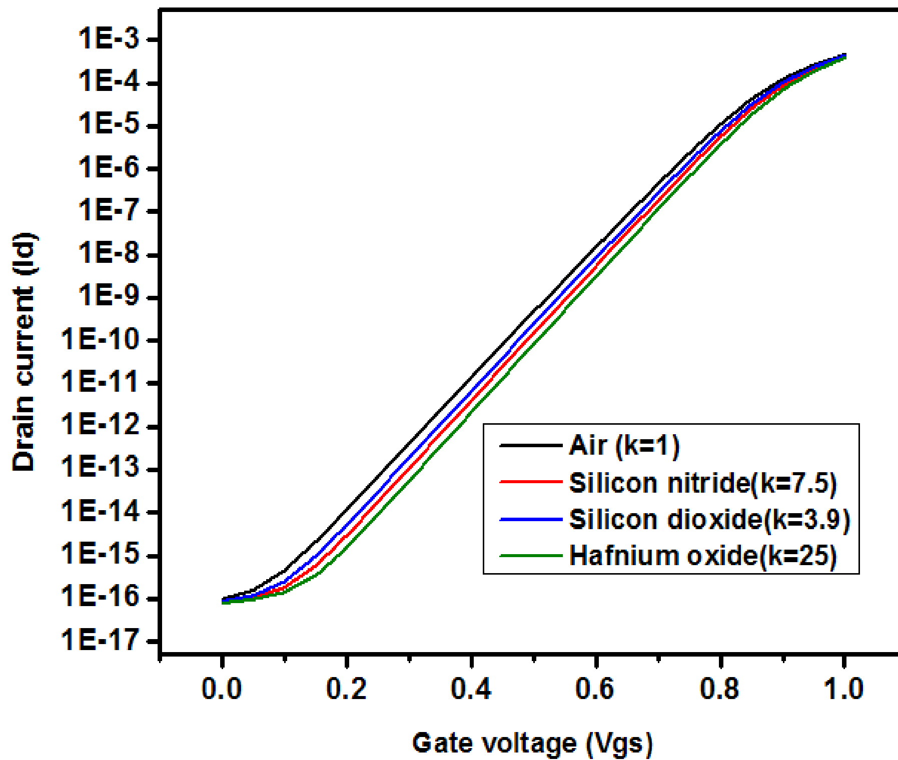


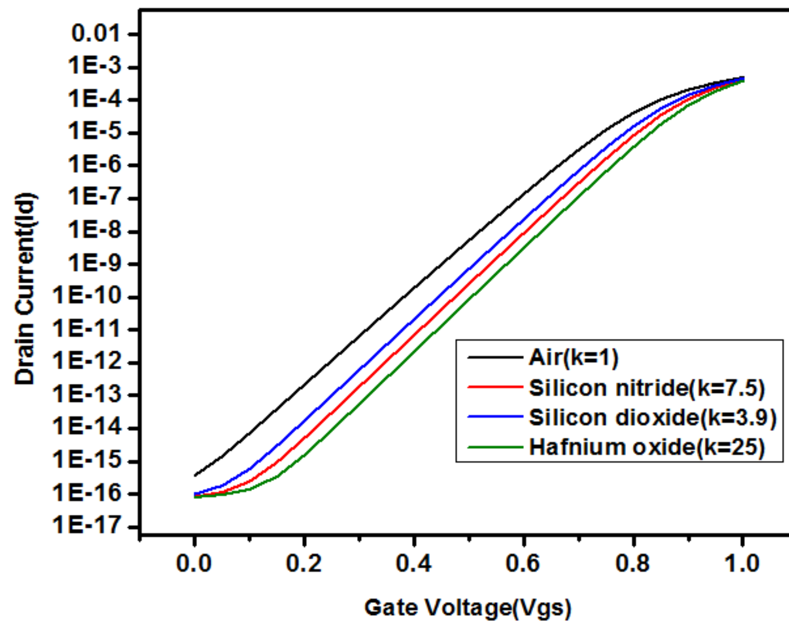
Figure 5.2 : Simulation of n+ pocket AJ DG MOSFET with a cavity region using TCAD

5.2 Sensitivity of the device for detecting biomolecules

Figure 5.3 (a) ,(b) and (c) shows increases in threshold voltage when the dielectric constant of the cavity decreases by introducing different dielectric material . Threshold voltage is also varied with change in the length of the cavity. From figure 5 (a) it is observed that the threshold shows less variation when length of the cavity is 3 nm when compared to figure 5 (b) and (c) where the cavity length is 5 nm and 7 nm respectively. Therefore, when dielectric constant increases the threshold voltage decreases significantly. Hence, the proposed device shows high sensitivity with change in dielectric constant helpful in detecting biomolecules.



(a)



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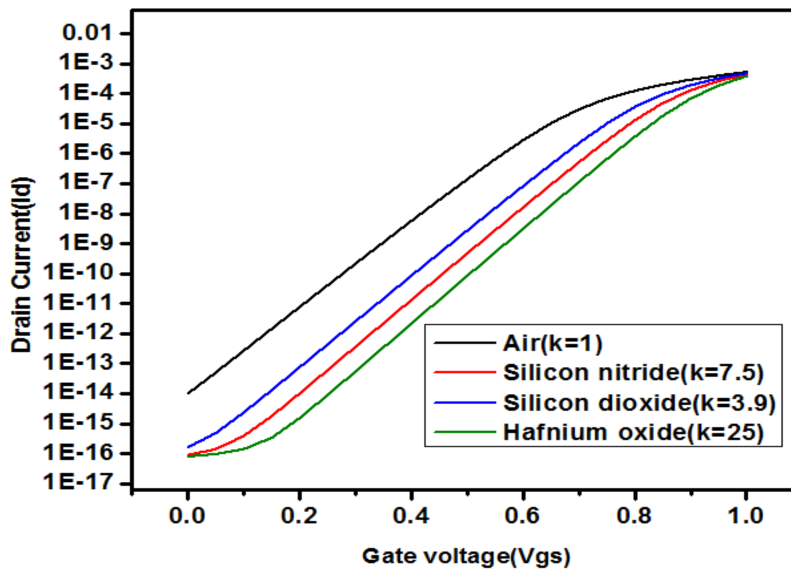
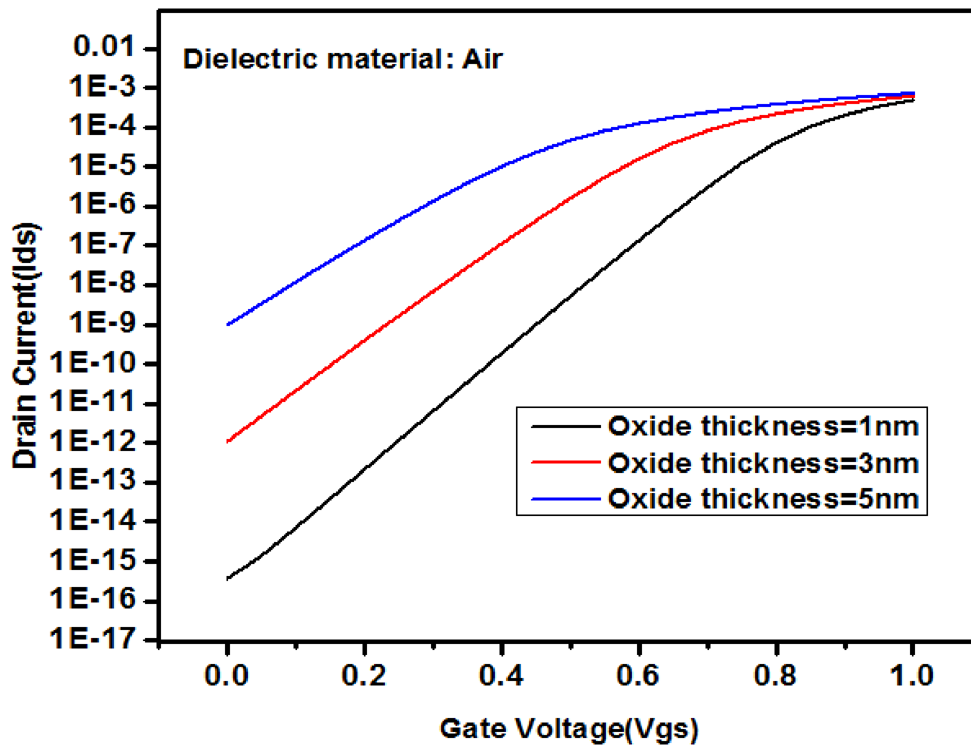


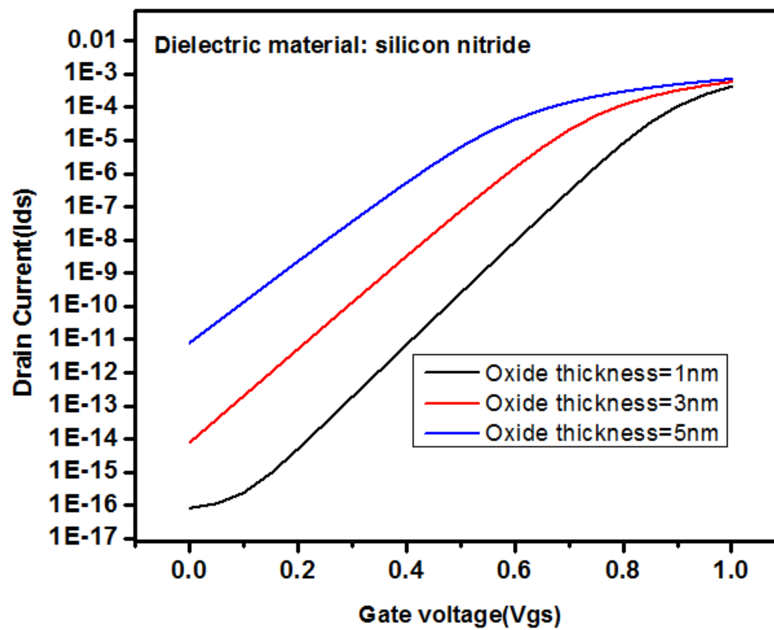
(c)

Figure 5.3 :(a) Id v/s Vgs with different dielectric constants (L_{cavity} = 3 nm) (b) Drain current versus gate voltage with different dielectric constants (L_{cavity} = 5 nm) (c) Drain current versus gate voltage with different dielectric constants (L_{cavity} = 7 nm).

When the dielectric material is held constant and the oxide thickness is altered, Figure 5.4 (a), (b), and (c) shows the graph of gate voltage vs drain current. The thicknesses of oxides considered were 1 nm, 3 nm, and 5 nm. The cavity is 5 nm long. When the thickness of the oxide is changed, the threshold voltage changes dramatically. The thickness of the cavity changes as the thickness of the oxide changes. Various dielectric materials, such as air, silicon nitride, and silicon dioxide, have different oxide thicknesses. It is observed that by increasing the gate oxide thickness, decrease in the threshold voltage is seen. The proposed device shows high sensitivity to changes made in oxide thickness and cavity height for different dielectric constants. Therefore the proposed device is suitable for detecting biomolecules because of the variation in dielectric constant present in the cavity region[86-87].



(a)



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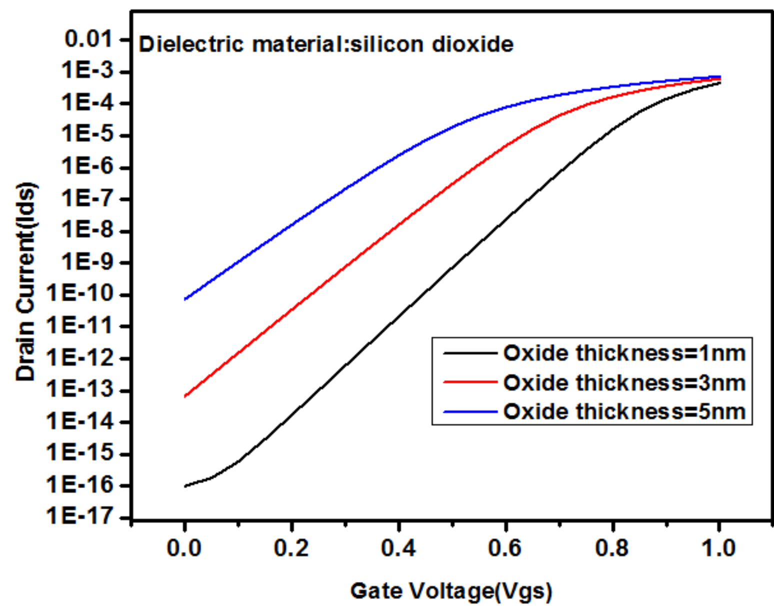
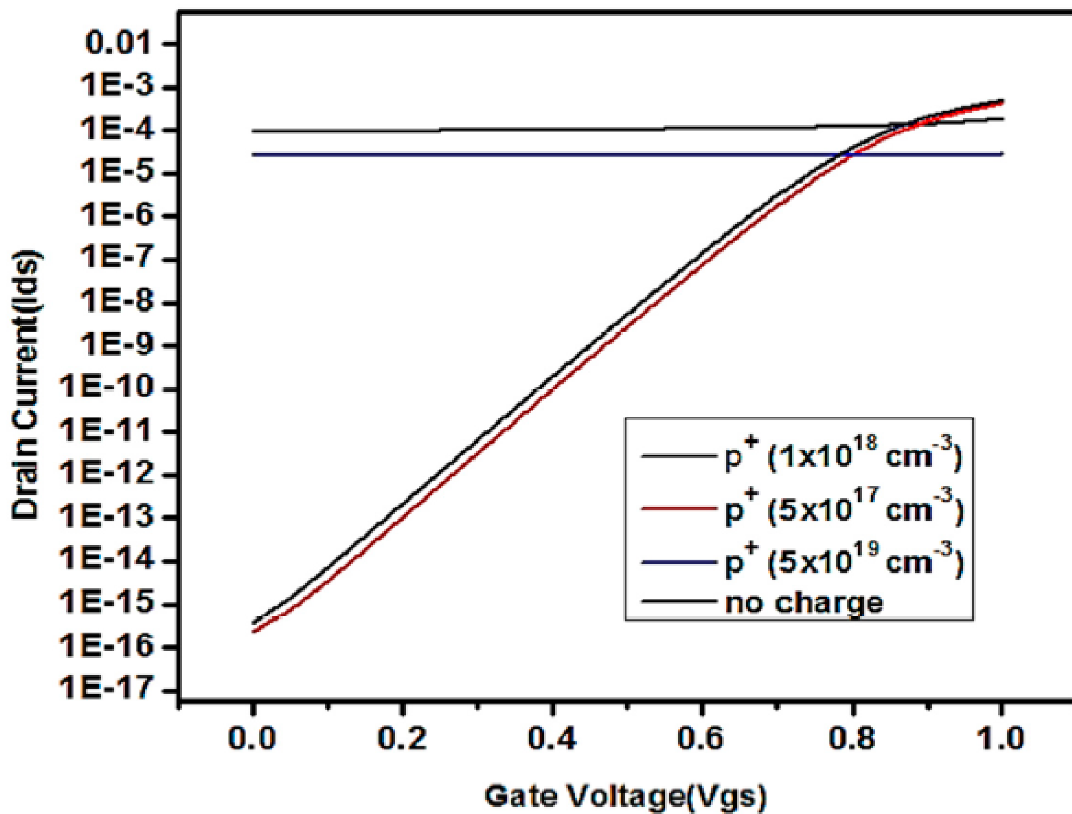


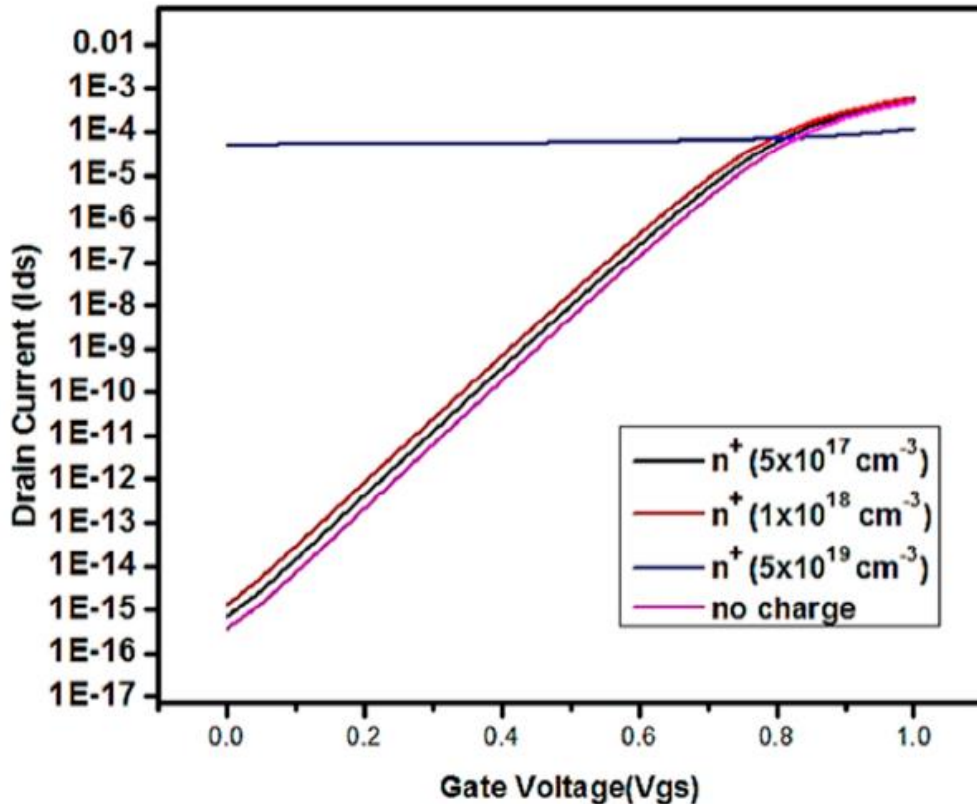
(c)

Figure 5.4: Drain current versus gate voltage curve, with (a) air (K = 1) as the dielectric material (b) silicon nitride (K = 7.5) as the dielectric material (c) silicon dioxide (K = 3.9) as the dielectric material.

Figure 5.5 (a) and (b) shows threshold voltage variation when the introduction of different charged particles is done in the cavity. The observation made is that threshold voltage varies with change in concentration of charged particles, and changes in OFF-state current is also seen. As a result, this gadget is helpful for detecting changes in charged particles (positive and negative). The change in charged particle concentration (from 5 x 10^{19} to 10^{18}) causes a significant shift in OFF-state leakage current. As a result, the proposed device can detect biomolecules with a variety of dielectric constants and charge concentrations.



(a)



(b)

Figure 5.5 : (a) Drain current versus gate voltage of the proposed n+ pocket AJ DG MOSFET for p+ charge concentration in the cavity region (b) Drain current versus gate voltage of the proposed n+ pocket AJ DG MOSFET for n+ charge concentration in the cavity region.

5.3 p-channel dopingless AJ DG MOSFET

Figure 5.6 shows a p-channel dopingless AJ DG MOSFET with an unsymmetrical gate and variable doping concentrations in the drain, source, and gate, with n + polysilicon as the gate contact.The gate oxide (HfO2) has a thickness of 1 nanometer. P type doping is present in the source and drain regions,with concentrations of $1x10^{19}$ cm^{-3} and $1x10^{15}$ cm^{-3}, respectively. There is no doping in the channel region. The channel area is 18 nm long. Overlapping section is 4 nm long. The drain and source portions are 8 nm

long. The matching of nmos and pmos is shown in Figure 10. Pmos and nmos are also compatible since their threshold voltage and drain current changes are identical. As a result, both nmos and pmos may be utilised to create CMOS inverters. A 3-D Schematic p channel asymmetrical junctionless DG MOSFET using TCAD simulation tool is shown in figure 5.7 (a). Figure 5.7(b) depicts V_{gs} versus I_d for 4 p-channel dopingless AJ DG MOSFET and it is observed pmos shows an ideal variation of drain current along with gate voltage.

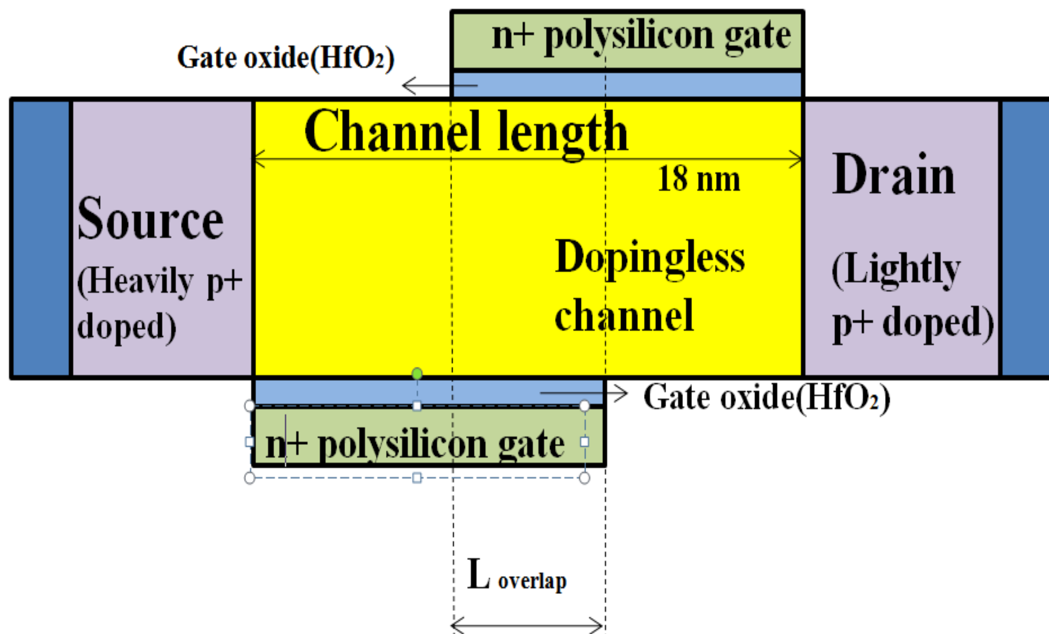
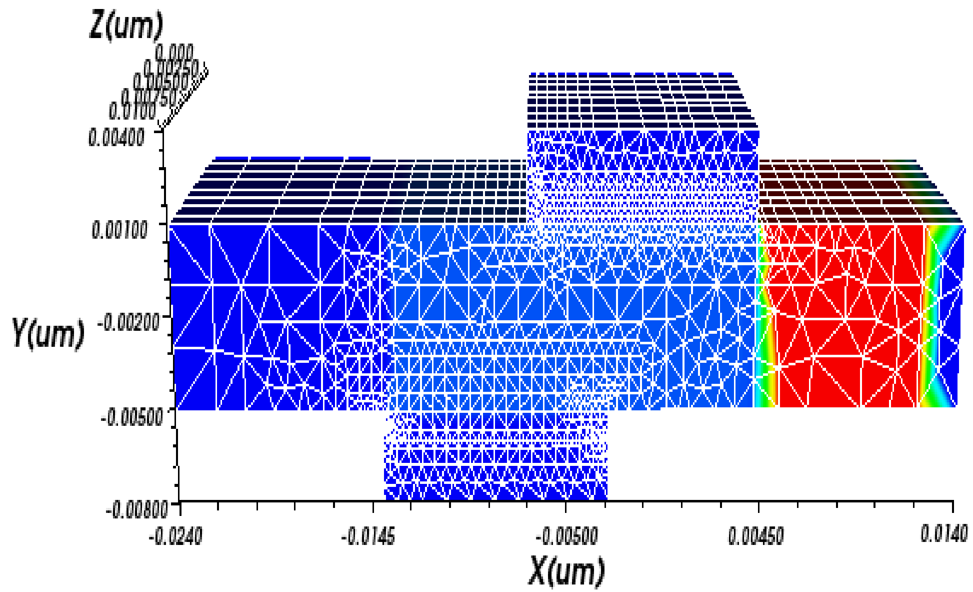
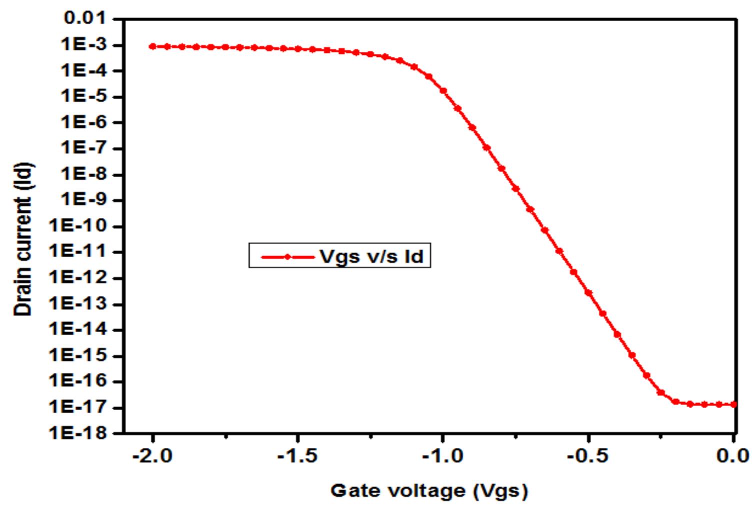


Figure 5.6 : A p-channel dopingless AJ DG MOSFET



(a)



(b)

Figure 5.7: (a) 3-D Schematic p channel asymmetrical junctionless DG MOSFET using TCAD simulation tool (b) Vgs versus Id for 4 p-channel dopingless AJ DG MOSFET

5.4 CMOS based logic and memory design

5.4.1 CMOS inverter design using proposed transistor

Figure 5.10 (a) represents the compatibility between nmos and pmos. There is compatibility pmos and nmos are because they have similarity in threshold voltage and variation in drain current. Therefore, nmos and pmos of dopingless AJ DG MOSFET is capable for CMOS inverter designing [58]. Design of inverter using proposed NMOS and PMOS is shown in figure 5.8 . Gate contacts of nmos and pmos is used to give input to the inverter. The ratio between the width of PMOS and NMOS is 2:1. The four gates of the inverter are connected to each other. Interconnected drain 1 and drain 2 gives the output of the device. Figure 5.9 represents 3-D Schematic of inverter using TCAD simulation tool**.** When the input voltage is less than the threshold voltage, the NMOS is in cut-off mode, and the PMOS is in linear mode. NMOS and PMOS also have zero drain currents. The output voltage is identical to the supply voltage in this scenario. When the provided input voltage is greater than the threshold voltage + supply voltage, the PMOS is in the cut off area. Because the drain current is zero and the output is coupled to the ground, NMOS operates in the linear area. The connection is made between VDD and Source 1 and between GND and source 2. Interconnection is made between drain 1and drain 2. The output and input signals of the inverter is shown in figure .The output 0 is obtained when input 1 is provided at the gate and vice-versa. From the graph it is observed that the variation in input output signals of the represents an ideal behaviour having perfect logic 0 and 1. Hence, the proposed dopingless AJ DG MOSFET shows its compatibility in CMOS technology and is capable for low power application and designing of SRAM and DRAM cell. The major issue in low power application is leakage current. Dual material gate can be further used for reducing leakage current [59]. The device can further explored for analog/RF performance by designing an amplifier with proposed n-channel and p-channel MOSFET [60].

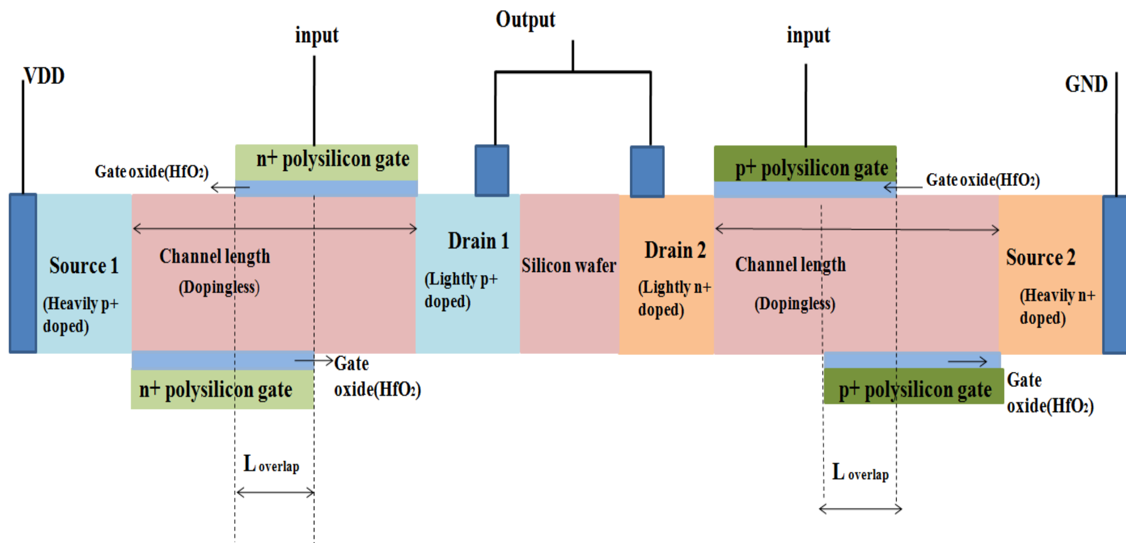


Figure 5.8: Design of inverter using nmos and pmos of dopingless AJ DG MOSFET

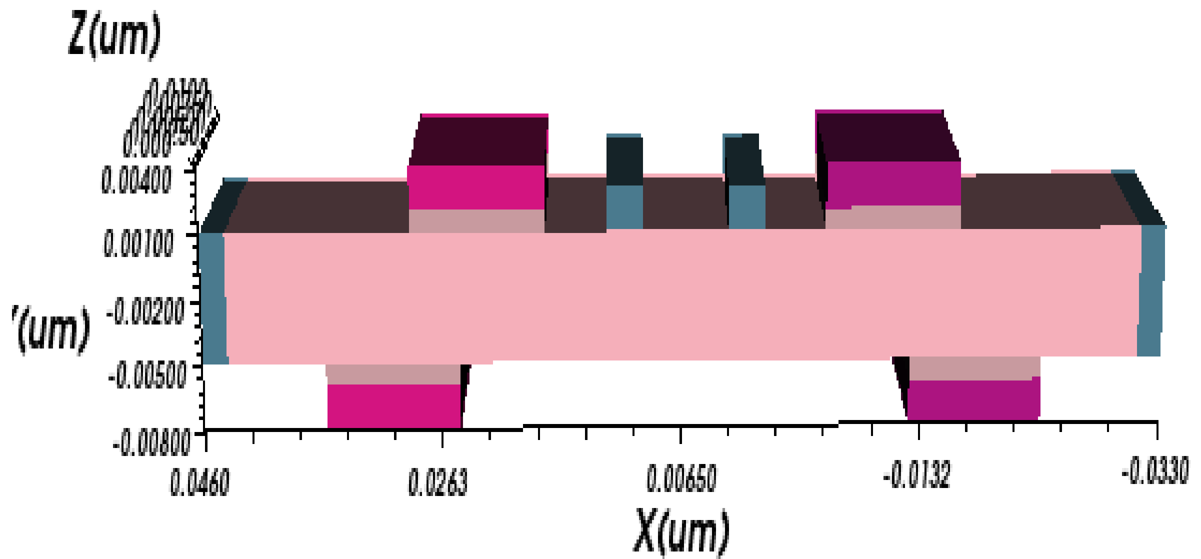
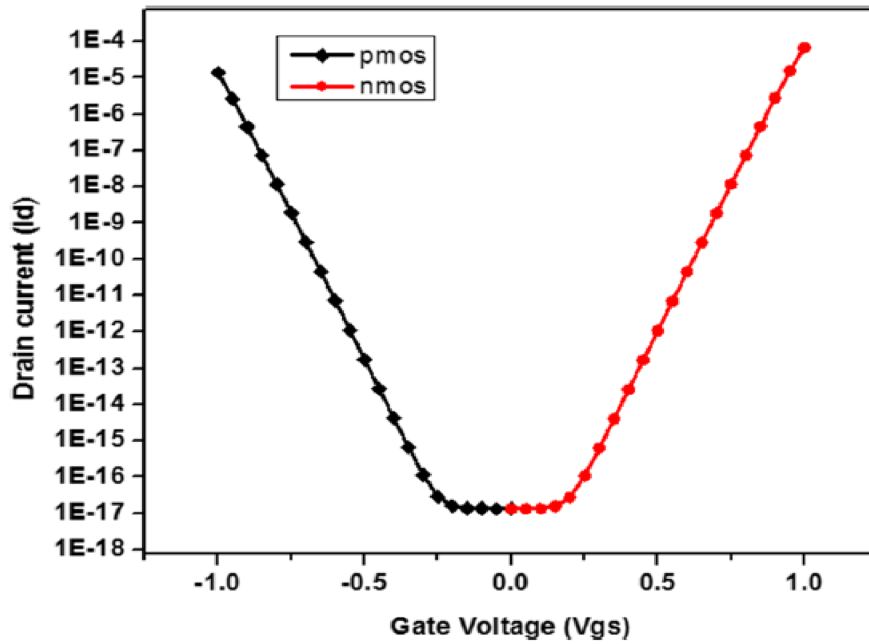
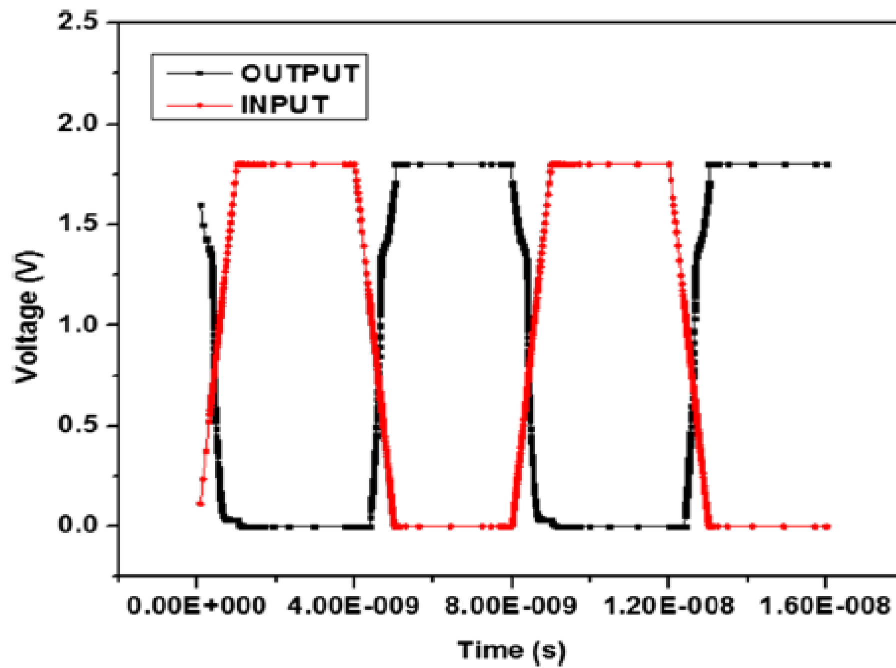


Figure 5.9 : 3-D Schematic of inverter using TCAD simulation tool



(a)



(b)

Figure 5.10: (a). Matching of nmos and pmos of dopingless AJ DG MOSFET (b) INPUT and OUTPUT response for the CMOS inverter with respect to time

5.4.2 6T SRAM CELL with Proposed Transistors

6T SRAM cell is represented in figure 5.11 [48] where dopingless AJ DG MOSFET is used for its designing. WI, BI, Blb represents the nodes. The connection of these nodes are made with the probe to study voltage level. Cross connection between the inverters represents the probe. Connection is made between the drain of PMOS 1 and the drain of the NMOS 1. The drain of the PMOS 2 is connected to the drain of the NMOS 2. PMOS 1 and PMOS 2 sources are linked to Vdd, whereas NMOS 1 and NMOS 2 sources are connected to ground. The NMOS1 and PMOS1 gates are linked, as well as the node linking the PMOS 2 and NMOS 2 drains. The NMOS2 and PMOS2 gates are linked together, as well as the node linking the NMOS and PMOS drains of the first inverter.

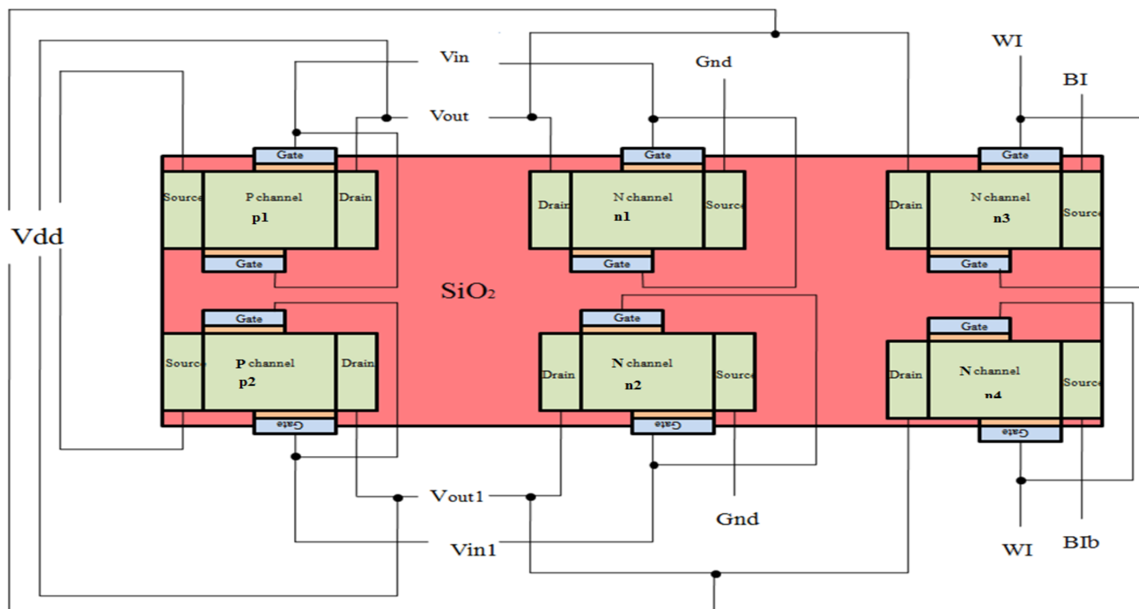
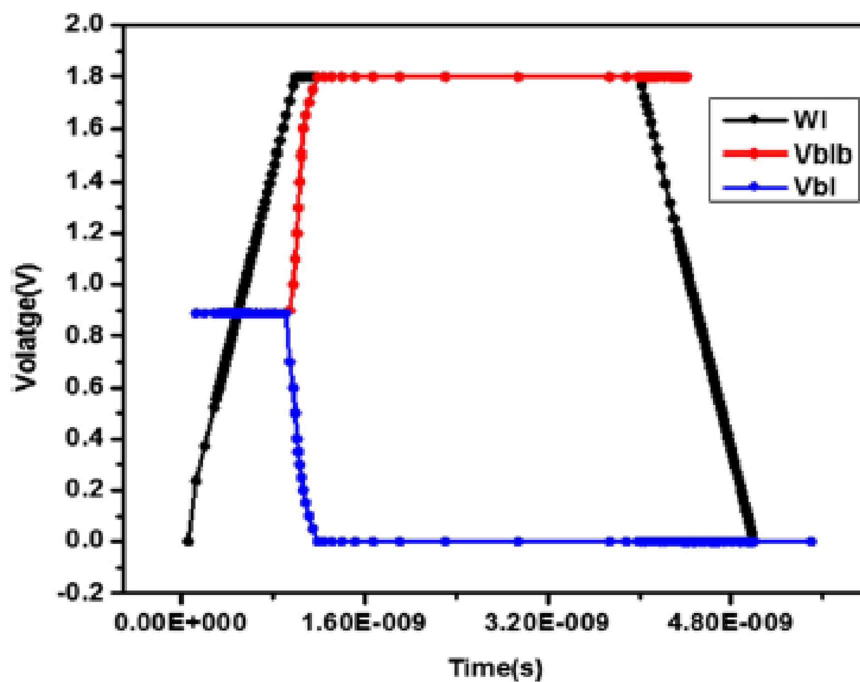


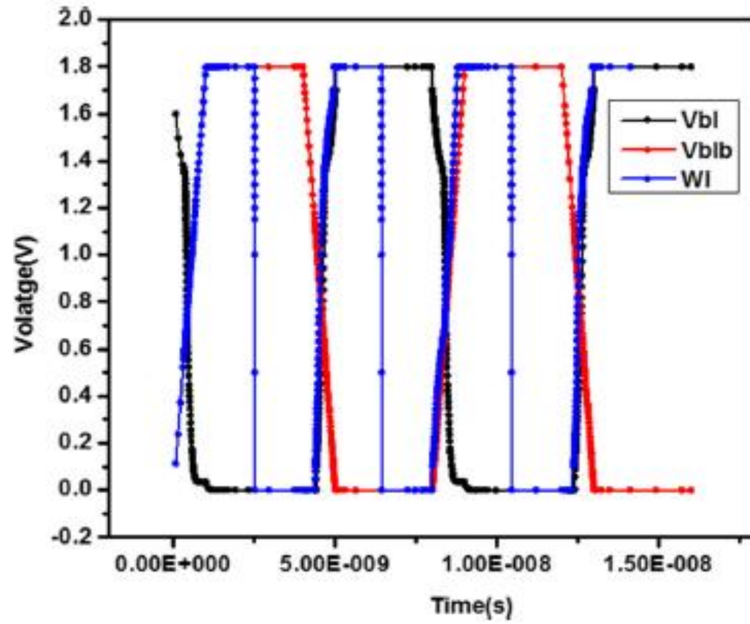
Figure 5.11: 6T SRAM cell using dopingless AJ DG MOSFET

Figure 5.12(a) depicts the hold state of a 6-T SRAM cell . When an SRAM cell is in hold, the data is stored in a static state. When the word line is 0 V, the transistors n3 and n4 are turned off, and the values 0 and 1 are preserved in the inverter, as shown in the diagram. Figure 5.8(b) depicts the read procedure for a 6-T SRAM cell . Bit lines bl and blb are

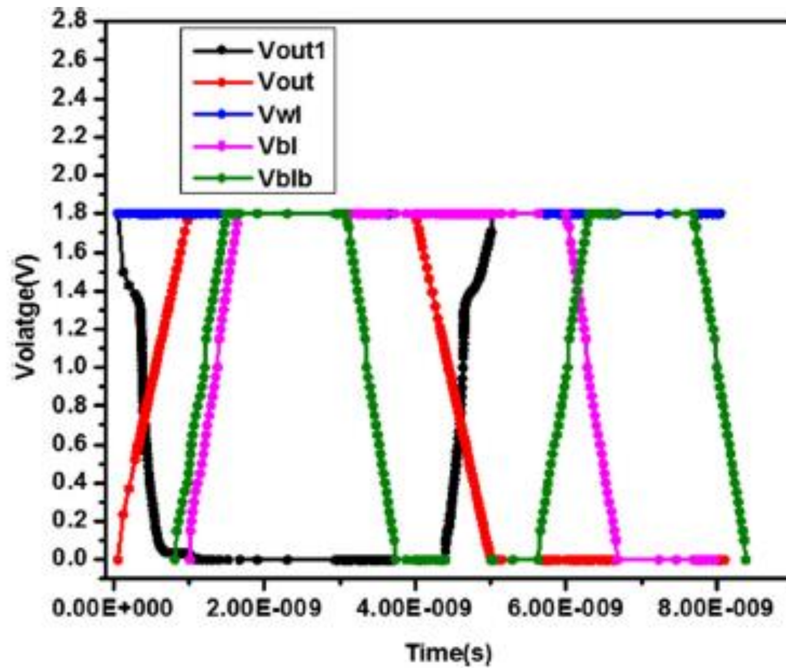
pre-charged in the read operation, and when the word line is raised, the node that is storing 0 pulls bit line bl or blb, whichever is associated to it, down, while the other bit line remains at the voltage level of bit lines. When the pass transistor is turned on (Wl=1), bl and blb retain the same data from vout and vout1. Figure 5.8 depicts the write procedure for a 6T SRAM cell (c). The write operation is performed by connecting one of the transistors n3 or n4 to VDD or GND. For writing 1 to Vout1, the bit lines bl and blb are charged to VDD. To enable the transistors n3 and n4, the word line is asserted to VDD. The output for inverter 1 and inverter 2 is altered correspondingly by pushing the values 1 or 0 to the bit lines bl and blb, as shown in the diagram.



(a)



(b)



(c)

Figure 5.12: (a) Hold state analysis of proposed 6T SRAM cell. (b) Read analysis of proposed 6T SRAM cell (c) Write analysis of proposed 6T SRAM cell

5.5 Proposed Fabrication steps of Inverter

As illustrated in Fig. 5.13 the fabrication of a CMOS inverter is done utilising NMOS and PMOS integrated on the same silicon wafer. Fabrication involves procedures such as silicon wafer creation, oxidation, UV exposure via a particular glass mask depending on mask layout, and active window creation for n-MOSFET and p-MOSFET, followed by metallisation. The substrate is a silicon wafer with a doping concentration of $1x10^{16}$cm 3 that has been flattened down to 6 nm. For NMOS and PMOS, 1 nm gate oxide HfO2 is formed on both sides of the wafer. To introduce contaminants to the drain and source regions, ion implantation is utilised. The dopants are accelerated to 20–100 keV in this approach, and the depth of penetration may be controlled by adjusting the accelerating voltage of the ions. Chemical vapour deposition is used to build a polysilicon gate layer over the oxide area. Silane or trichlorosilane is used to deposit the polysilicon gate. To assure the layer's development, pure silane or a silane solution containing 70–80 percent nitrogen is utilised at temperatures ranging from 600 to 6500 degrees Celsius with pressure of 25 and 150 Pa. .

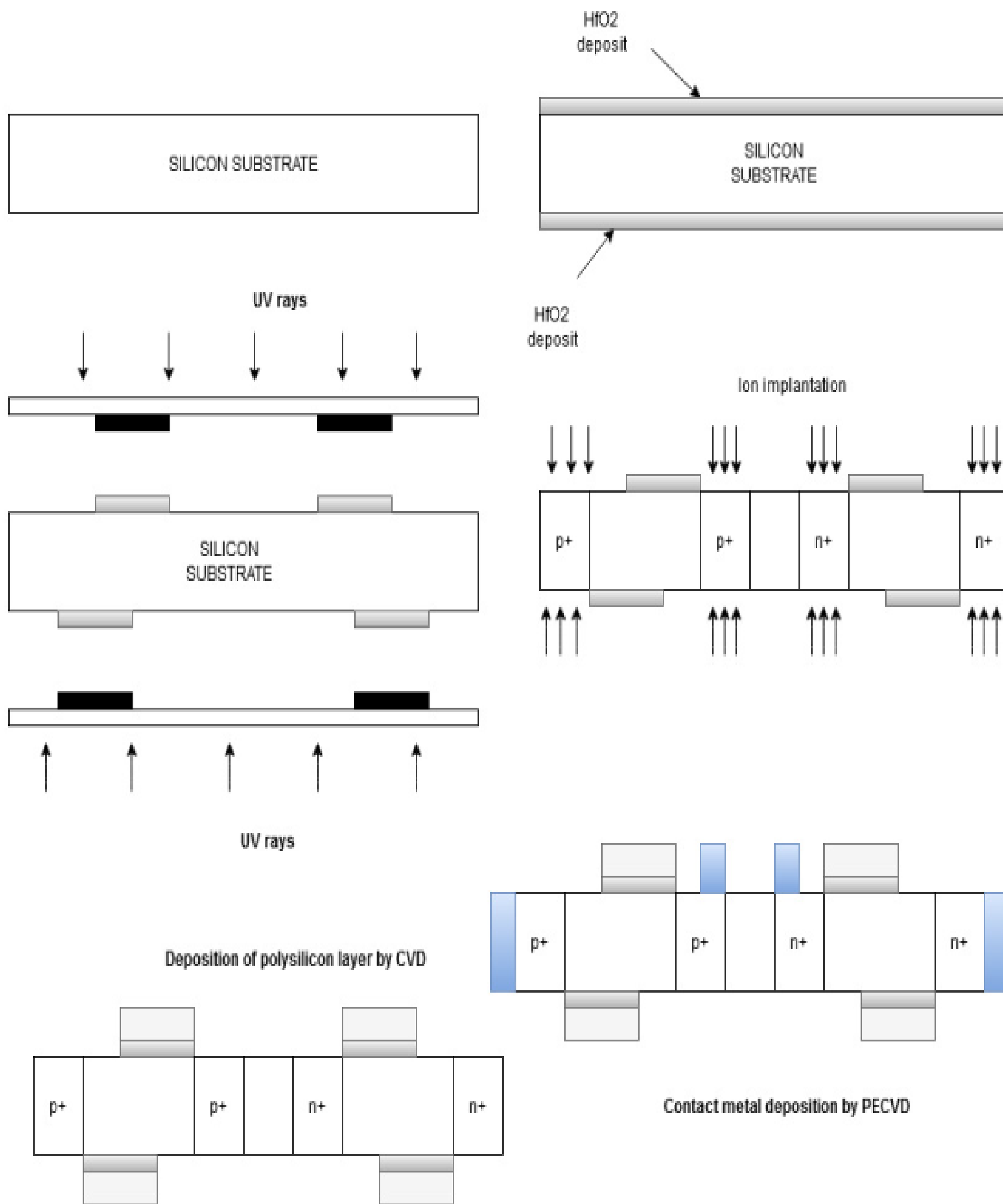


Figure 5.13: Fabrication steps of Inverter

5.6 Summary

In this chapter, different applications of proposed AJ DG MOSFET is explored such as biosensor developed for the rapid detection of different enzymes, infections, and antigens. With the use of FET-based biosensors, it is simple to detect a disease at an early stage. By generating a nanogap at the gate-oxide contact, a steep subthreshold highly doped n+ pocket asymmetrical JL MOSFET is utilized for biomedical applications. The gadget is analysed using dielectric modulation. Biosensor for detecting diseases all runs on low power. It is demonstrated that p channel and n channel dopingless AJ DG MOSFETs are compatible for CMOS based logic circuit design which is shown with the help of inverter circuit. Inverter is used to power light , fans etc with run on low power of 75 to 80 watts. The use of n-channel and p-channel dopingless AJ DG MOSFET is presented for reduced power inverter circuit and a 6T SRAM cell. SRAM cell uses minimum power supply of only 1V to work. It is used in processor , DSP which are low power devices

CHAPTER 6

ANALYTICAL MODELING OF PROPOSED AJ DG MOSFET:SURFACE POTENTIAL & CAPACITANCE MODEL

A double-gate MOSFET (DGMOSFET) is the first multi-gate MOSFET to be constructed, with two gates situated opposite each other and a channel area in between. Two gates provide for better control of channel inversion on both sides, improving the device's performance. Short channel effects (SCEs) are caused by shrinking the size of the devices, which brings the drain, source, channel, and gate oxide closer together. The use of a double-gate MOSFET structure in the MOSFET structure helps to reduce (SCEs)[3]. These SCEs have an impact on the device's performance, modeling, and reliability. Undoped silicon wafers offer an advantage over other MOSFET configurations in that they do not suffer from dopant fluctuation and charge carrier mobility is increased. Understanding and studying the device's performance necessitates the use of device modelling. Analytical modeling is a useful tool for determining the device's performance [89]. It is used to simulate and forecast the device's mechanics. Two-dimensional modelling is required to comprehend the mechanism of a nanoscale device. The modelling for the AJ DG MOSFET was done utilising the 2D Poisson's equation [90,110]. Modeling is necessary for gaining a physical understanding of the device's surface potential. Marina et al.[111] suggested a Poisson's equation and continuity equation-based explicit analytical charge-based model. Drain current and inversion charge expressions are produced.

In this chapter surface potential for proposed AJ DG MOSFET of channel length 18 nm and gate length is 11 nm is derived using solutions from 2D Poisson's equations. The proposed device is divided into three segments shown in figure 6.1 .The first and third part act as a single gate MOSFET and the second part as double gate MOSFET. Surface

potential for each segment is calculated and added . The capacitance model of the device is also derived,

6.1 Surface potential for proposed AJDG MOSFET

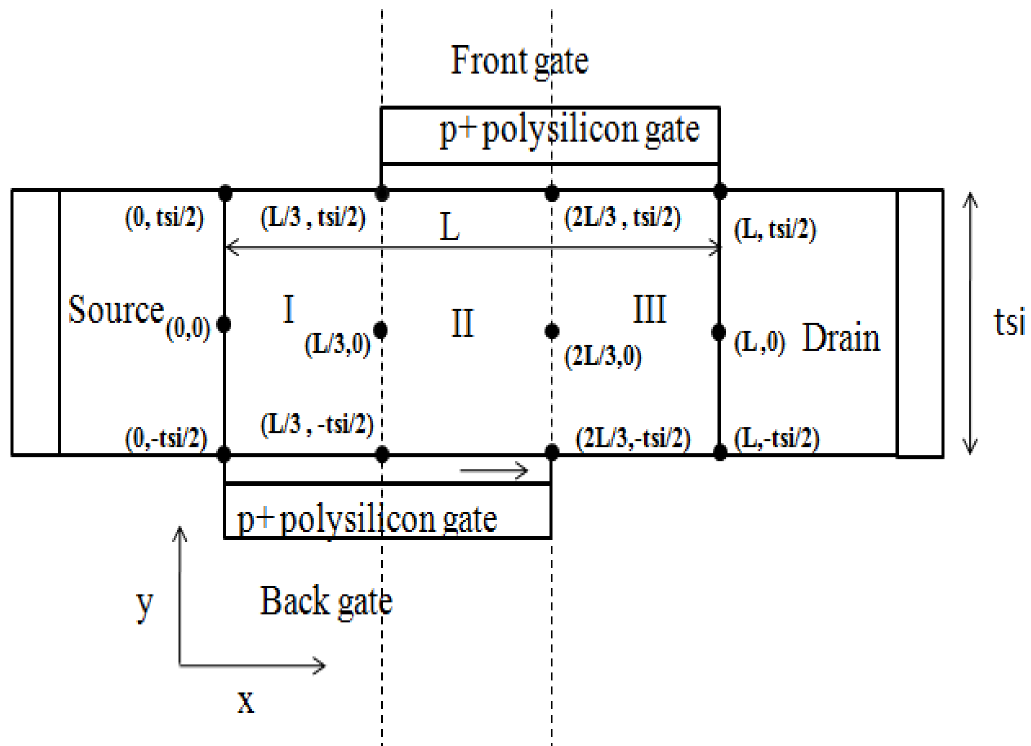


Figure 6.1: AJ DG MOSFET divided into three parts

Surface potential is the voltage difference between polysilicon's the top layer and the bulk. The characteristics of drain current depends on voltage of channel surface which is controlled by gate contact potential[111-115]. In AJDG MOSFET, has overlap and non overlap regions with two gates facing each other assymetrically.

AJ DG MOSFET is divided into three parts with different gate contact regions for calculation of surface potential represented in figure 2. The first and third segment is a SG MOSFET and the second segment is DG MOSFET .Surface potential is calculated

individually for all the segments and addition of surface potential of each part gives total surface potential for the proposed AJ DG MOSFET[115-127]. Different parameters used for the calculating surface potential is presented in table 6.1.

i) Surface potential for part I

Part 1 has boundary conditions given as

a) $\boldsymbol{\Phi_C(x) = \Phi(x , y) \,|_{y=0}}$

d) $\boldsymbol{\varepsilon_{si} \frac{\delta\Phi(x,y)}{\delta y} \,|_{y=-tsi/2} = -\varepsilon_{ins} \frac{[Vgs2- \Phi_{s2}(x)- \Phi_{ms2}]}{t_{in2}}}$

e) $\boldsymbol{\varepsilon_{si} \frac{\delta\Phi(x,y)}{\delta y} \,|_{y=+tsi/2} = 0}$

Parabolic potential function having parabolic in y direction is

$$\Phi(x , y) = A_1(x) + A_2(x)\, y + A_3(x)\, y^2 \qquad (1)$$

Substituting boundary condition (a) in equation (1)

$$A_1(x) = \Phi_C(x) \qquad (2)$$

Using the boundary conditions (d) ,(e) and equation (1), A_2 and A_3 are obtained

$$A_2(x) = -\frac{\varepsilon_{ins}}{2\,\varepsilon_{si}} \frac{[Vgs2- \Phi_{s2}(x)- \Phi_{ms2}]}{t_{in2}} \qquad (3)$$

$$A_3(x) = \frac{\varepsilon_{ins}}{2\, t_{si}\varepsilon_{si}} \frac{[Vgs2- \Phi_{s2}(x)- \Phi_{ms2}]}{t_{in2}} \qquad (4)$$

Therefore, surface potential for part I is obtained by substituting (2), (3) and (4) in (1)

$$\Phi(x , y)_I = \Phi_C(x) - \frac{\varepsilon_{ins}}{2\,\varepsilon_{si}} \frac{[Vgs2- \Phi_{s2}(x)- \Phi_{ms2}]}{t_{in2}} y + \frac{\varepsilon_{ins}}{2\, t_{si}\varepsilon_{si}} \frac{[Vgs2- \Phi_{s2}(x)- \Phi_{ms2}]}{t_{in2}} y^2 \qquad (5)$$

ii) Surface potential for part II

Part II boundary condition given below

a) $\boldsymbol{\Phi_C(x) = \Phi(x , y) \,|_{y=0}}$

b) $\boldsymbol{\Phi_{s1}}$**(x) = Φ(x , y)** $|_{y=+tsi/2}$

$\boldsymbol{\Phi_{s2}}$**(x) = Φ(x , y)** $|_{y=-tsi/2}$

c) $\boldsymbol{\varepsilon_{si}\frac{\delta\Phi(x,y)}{\delta y}\Big|_{y=+tsi/2} = \varepsilon_{ins}\frac{[Vgs1- \Phi_{s1}(x)- \Phi_{ms1}]}{t_{in1}}}$

d) $\boldsymbol{\varepsilon_{si}\frac{\delta\Phi(x,y)}{\delta y}\Big|_{y=-tsi/2} = -\varepsilon_{ins}\frac{[Vgs2- \Phi_{s2}(x)- \Phi_{ms2}]}{t_{in2}}}$

Table 6.1 : Parameters along with their symbol for Surface potential of AJ DG MOSFET

Parameters	**Symbol**
Centre potential	Φ_C(x)
Surface potential at the front gate	Φ_{s1} (x)
Surface potential at the back gate	Φ_{s2}(x)
Voltage at front gate	V_{gs1}
Voltage at back gate	V_{gs2}
Permittivity of insulator	ε_{ins}
Permittivity of silicon	ε_{si}
Thickness of silicon	t_{si}
Insulator layer thickness for front gate	t_{in1}
Insulator layer thickness for back gate	t_{in2}
Work function differences between the front gate and silicon channel	Φ_{ms1}
Work function differences between the back gate and silicon channel	Φ_{ms2}

Parabolic potential function having parabolic in y direction is given as

$$\Phi(x , y) = D_1(x) + D_2(x)\, y + D_3(x)\, y^2 \qquad (6)$$

from the boundary condition (a)

$D_1(\mathrm{x}) = \Phi_C(\mathrm{x})$ (7)

From boundary condition (c), (d) and equation (6) the following is obtained

$$D_2(\mathrm{x}) = \frac{\varepsilon_{\mathrm{ins}}}{2\,\varepsilon_{\mathrm{si}}}\left(\frac{[\mathrm{Vgs1}- \quad \Phi_{\mathrm{s1}}(\mathrm{x})- \quad \Phi_{\mathrm{ms1}}]}{\mathrm{t_{in1}}} - \frac{[\mathrm{Vgs2}- \quad \Phi_{\mathrm{s2}}(\mathrm{x})- \quad \Phi_{\mathrm{ms2}}]}{\mathrm{t_{in2}}}\right) \quad (8)$$

$$D_3(\mathrm{x}) = \frac{\varepsilon_{\mathrm{ins}}}{2\ \mathrm{t_{si}}\varepsilon_{\mathrm{si}}}\left(\frac{[\mathrm{Vgs1}- \quad \Phi_{\mathrm{s1}}(\mathrm{x})- \quad \Phi_{\mathrm{ms1}}]}{\mathrm{t_{in1}}} + \frac{[\mathrm{Vgs2}- \quad \Phi_{\mathrm{s2}}(\mathrm{x})- \quad \Phi_{\mathrm{ms2}}]}{\mathrm{t_{in2}}}\right) \quad (9)$$

Therefore, surface potential for part II is obtained from substituting (7), (8) and (9) in (6)

$$\Phi(\mathrm{x}\,,\mathrm{y})_{\mathrm{II}} = \Phi_C(\mathrm{x}) + \frac{\varepsilon_{\mathrm{ins}}}{2\,\varepsilon_{\mathrm{si}}}\left(\frac{[\mathrm{Vgs1}- \quad \Phi_{\mathrm{s1}}(\mathrm{x})- \quad \Phi_{\mathrm{ms1}}]}{\mathrm{t_{in1}}} - \frac{[\mathrm{Vgs2}- \quad \Phi_{\mathrm{s2}}(\mathrm{x})- \quad \Phi_{\mathrm{ms2}}]}{\mathrm{t_{in2}}}\right) \mathrm{y} + \frac{\varepsilon_{\mathrm{ins}}}{2\ \mathrm{t_{si}}\varepsilon_{\mathrm{si}}} \left(\frac{[\mathrm{Vgs1}- \quad \Phi_{\mathrm{s1}}(\mathrm{x})- \quad \Phi_{\mathrm{ms1}}]}{\mathrm{t_{in1}}} + \frac{[\mathrm{Vgs2}- \quad \Phi_{\mathrm{s2}}(\mathrm{x})- \quad \Phi_{\mathrm{ms2}}]}{\mathrm{t_{in2}}}\right) y^2 \quad (10)$$

iii) Surface potential for part III

Part III has boundary conditions as

a) $\boldsymbol{\Phi_C(\mathrm{x}) = \Phi(\mathrm{x}\,,\mathrm{y})\ |_{y=0}}$

c) $\boldsymbol{\varepsilon_{si}\frac{\delta\Phi(\mathrm{x}\,,\mathrm{y})}{\delta y}\ |_{y=+tsi/2} = \varepsilon_{ins}\frac{[Vgs1- \quad \Phi_{s1}(\mathrm{x})- \quad \Phi_{ms1}]}{t_{in1}}}$

f) $\boldsymbol{\varepsilon_{si}\frac{\delta\Phi(\mathrm{x}\,,\mathrm{y})}{\delta y}\ |_{y=-tsi/2} = 0}$

Parabolic potential function considering parabolic in y direction is given by

$\Phi(\mathrm{x}\,,\mathrm{y}) = B_1(\mathrm{x}) + B_2(\mathrm{x})\ \mathrm{y} + B_3(\mathrm{x})\ y^2$ (11)

substituting boundary condition (a) in (11)

$B_1(\mathrm{x}) = \Phi_C(x)$ (12)

Using boundary condition (c) ,(f) and equation (11) $B_2$and B_3 are obtained below

$$B_2(x) = \frac{\varepsilon_{ins}}{2\,\varepsilon_{si}} \frac{[Vgs1 - \Phi_{s1}(x) - \Phi_{ms1}]}{t_{in1}} \tag{13}$$

$$B_3(x) = \frac{\varepsilon_{ins}}{2\ t_{si}\varepsilon_{si}} \frac{[Vgs1 - \Phi_{s1}(x) - \Phi_{ms1}]}{t_{in1}} \tag{14}$$

Therefore, surface potential for part III is obtained from substituting (12), (13) and (14) in (11)

$$\Phi(x\,,y)_{III} = \Phi_C(x) + \frac{\varepsilon_{ins}}{2\,\varepsilon_{si}} \frac{[Vgs1 - \Phi_{s1}(x) - \Phi_{ms1}]}{t_{in1}} y + \frac{\varepsilon_{ins}}{2\ t_{si}\varepsilon_{si}} \frac{[Vgs1 - \Phi_{s1}(x) - \Phi_{ms1}]}{t_{in1}} y^2 \tag{15}$$

Therefore the total surface potential is obtained by adding surface potentials of part I , II and III

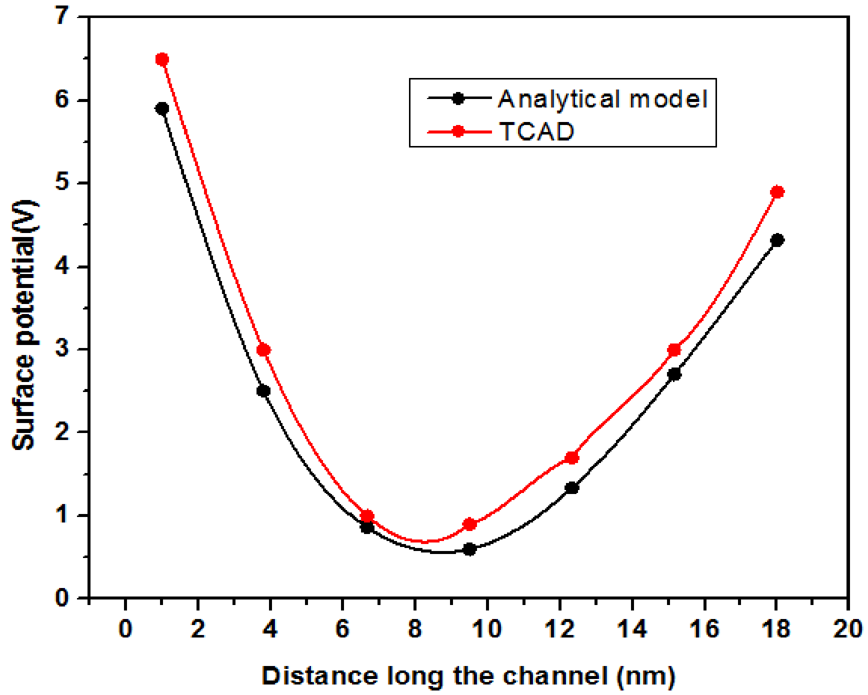
$$\Phi(x\,,y) = \Phi(x\,,y)_I + \Phi(x\,,y)_{II} + \Phi(x\,,y)_{III}$$

$$\Phi(x\,,y) = \Phi_C(x) - \frac{\varepsilon_{ins}}{2\,\varepsilon_{si}} \frac{[Vgs2 - \Phi_{s2}(x) - \Phi_{ms2}]}{t_{in2}}\ y + \frac{\varepsilon_{ins}}{2\ t_{si}\varepsilon_{si}} \frac{[Vgs2 - \Phi_{s2}(x) - \Phi_{ms2}]}{t_{in2}} y^2 + \Phi_C(x)$$
$$+ \frac{\varepsilon_{ins}}{2\,\varepsilon_{si}}\left(\frac{[Vgs1 - \Phi_{s1}(x) - \Phi_{ms1}]}{t_{in1}} - \frac{[Vgs2 - \Phi_{s2}(x) - \Phi_{ms2}]}{t_{in2}}\right) y + \frac{\varepsilon_{ins}}{2\ t_{si}\varepsilon_{si}}\left(\frac{[Vgs1 - \Phi_{s1}(x) - \Phi_{ms1}]}{t_{in1}} +\right.$$
$$\left.\frac{[Vgs2 - \Phi_{s2}(x) - \Phi_{ms2}]}{t_{in2}}\right) y^2 + \Phi_C(x) + \frac{\varepsilon_{ins}}{2\,\varepsilon_{si}} \frac{[Vgs1 - \Phi_{s1}(x) - \Phi_{ms1}]}{t_{in1}}\ y$$
$$+ \quad \frac{\varepsilon_{ins}}{2\ t_{si}\varepsilon_{si}} \frac{[Vgs1 - \Phi_{s1}(x) - \Phi_{ms1}]}{t_{in1}} y^2 \tag{16}$$

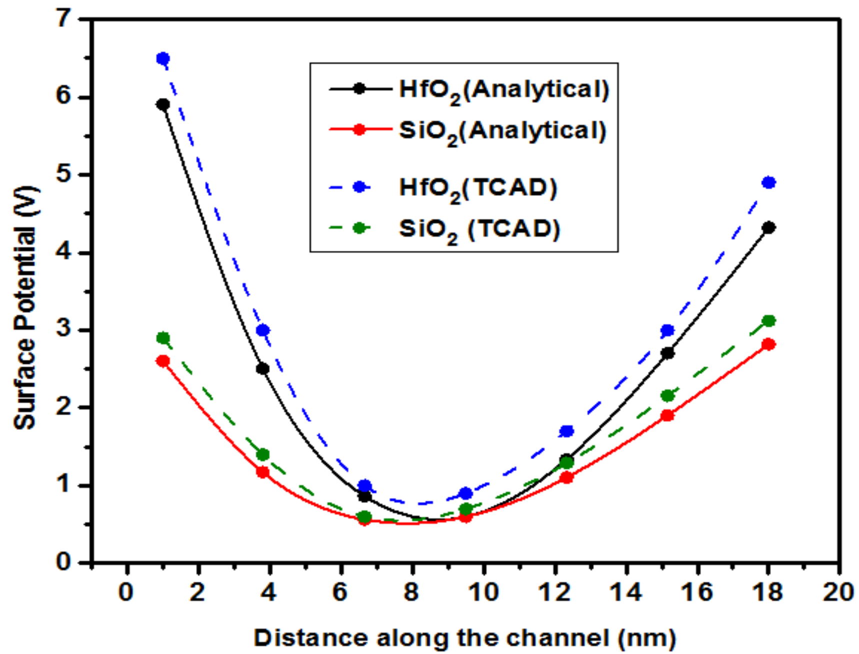
Total surface potential obtained after solving (16)

$$\Phi(x\,,y) = 3\Phi_C(x) + \frac{\varepsilon_{ins}}{2\,\varepsilon_{si}}\left(2\frac{[Vgs1 - \Phi_{s1}(x) - \Phi_{ms1}]}{t_{in1}} - 2\frac{[Vgs2 - \Phi_{s2}(x) - \Phi_{ms2}]}{t_{in2}}\right) y +$$
$$\frac{\varepsilon_{ins}}{2\ t_{si}\varepsilon_{si}}\left(2\frac{[Vgs1 - \Phi_{s1}(x) - \Phi_{ms1}]}{t_{in1}} + 2\frac{[Vgs2 - \Phi_{s2}(x) - \Phi_{ms2}]}{t_{in2}}\right) y^2 \tag{17}$$

6.2 Results and discussion for analytical model of surface potential



(a)



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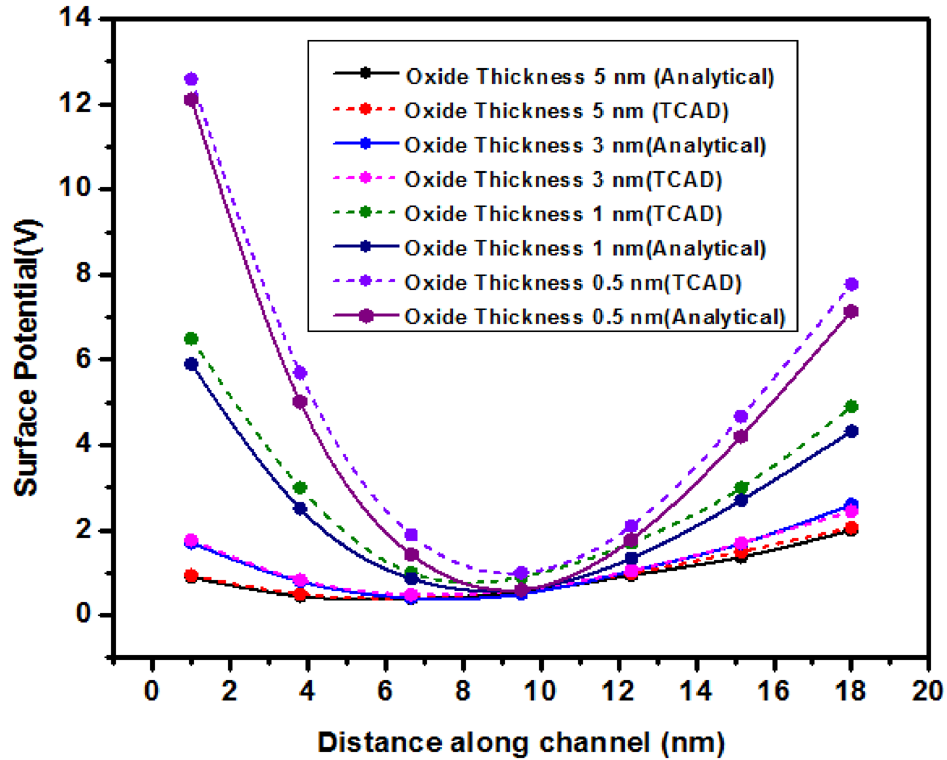


(c)

Figure 6.2 : (a) Variation of Surface potential along the channel length for analytical model and TCAD simulation (b) Variation of surface potential along the channel length for different gate oxide material SiO_2 and HfO_2 (c)Variation of surface potential along the channel length for different oxide thickness

Figure 6.2 represents the surface potential variation with the channel length for analytical model and TCAD simulation. The observation made is that around the centre of the channel the potential is low. Small difference is noted between the surface potential from TCAD simulation and from analytical modeling. Variation of surface potential with the channel length using gate oxides like SiO_2 and HfO_2 keeping other parameters constant is represented in figure and also the analytical and TCAD analysis is compared in the graph. Therefore, there is small variation between TCAD analysis and an analytical model. The surface potential value less for gate oxide SiO_2 in comparison to

HfO_2. However in both cases, surface potential is least around centre of the channel length 9 nm. Figure 5 represents the variation in surface potential with channel length for different oxide thicknesses. Comparison between TCAD and an analytical model is shown in the figure and there is a small variation in TCAD and analytical models. Therefore by increasing gate oxide thickness the surface potential reduces. the surface potential is inversely proportional to gate oxide thickness as shown in equation(17).

Table 6.2 : Comparison table of surface potenial for Analytical model and TCAD model of proposed AJ DG MOSFET along the channel length.

Channel length	Surface Potential of AJ DG MOSFET through Analytical model on MATLAB	Surface Potential of AJ DG MOSFET through TCAD based model simulation
2 nm	5.2 V	6 V
4 nm	2.5 V	3 V
8 nm	0.7 V	0.9 V
14 nm	1.8 V	2.5 V
18 nm	4.5 V	5 V

6.3 Capacitance Model

Different parasitic capacitances formed between gate, source and drain is shown in figure 6.3. The transistor capacitance model parameters are separately described in table 6. 2. Capacitance C_{sb} and C_{db} are not considered because the proposed device is junctionless and C_{gb} is zero in saturation as well as linear region. For calculating R_{ON} the capacitances along R_{on1} and R_{on2} is calculated [128,129].

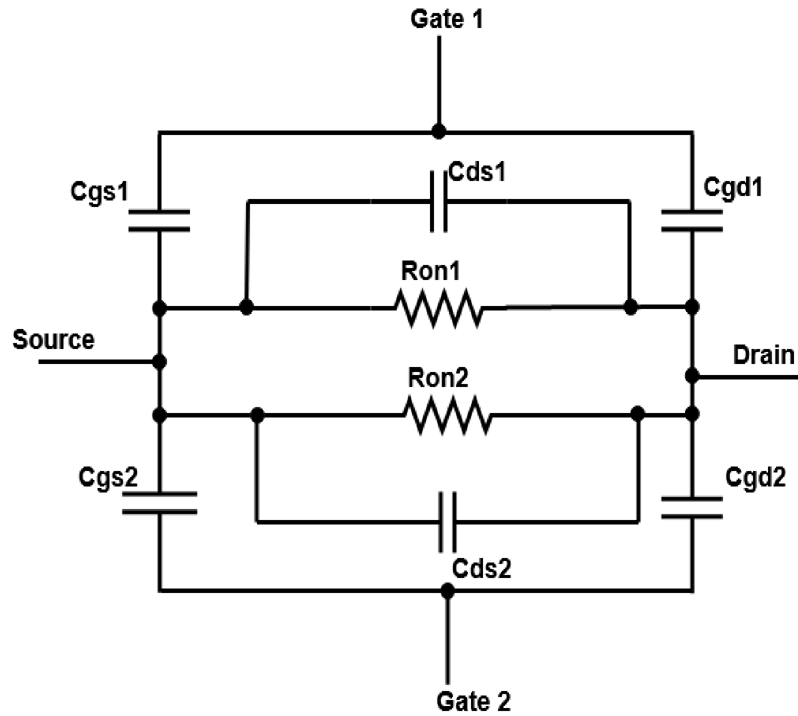


Figure 6.3: Equivalent capacitance model

Table 6.3: Parameters along with their symbol for capacitance model of AJ DG MOSFET

Parameters	Symbol
Oxide related gate to source capacitance for gate1	C_{gs1}
Oxide related gate to source capacitance for gate 2	C_{gs2}
Oxide related gate to drain capacitance for gate 1	C_{gd1}
Oxide related gate to drain capacitance for gate 2	C_{gd2}
Drain to source capacitance for gate 1	C_{ds1}
Drain to source capacitance for gate 2	C_{ds2}
ON resistance for gate 1	R_{on1}
ON resistance for gate 2	R_{on2}
Source to substrate junction capacitance	C_{sb}
Drain to substrate junction capacitance	C_{db}

Taking the capacitive reactance of C_{ds1}

C_{ds1} and C_{gd1} are in parallel

Therefore, the resistance across R_1 is

$$Ron = \frac{Ron1 \cdot Ron2}{Ron1 + Ron2} \quad (18)$$

Capacitance across R_{on1}

$$C_1 = \frac{Cgs1 \cdot Cgd1}{Cgs1 + Cgd1} + C_{ds1} \quad (19)$$

Capacitance across R_{on2}

$$C_2 = \frac{Cgs2 \cdot Cgd2}{Cgs2 + Cgd2} + C_{ds2} \quad (21)$$

Total capacitance

$$C_{gd} = \frac{Cgs1 \cdot Cgd1}{Cgs1 + Cgd1} + C_{ds1} + \frac{Cgs2 \cdot Cgd2}{Cgs2 + Cgd2} + C_{ds2} \quad (22)$$

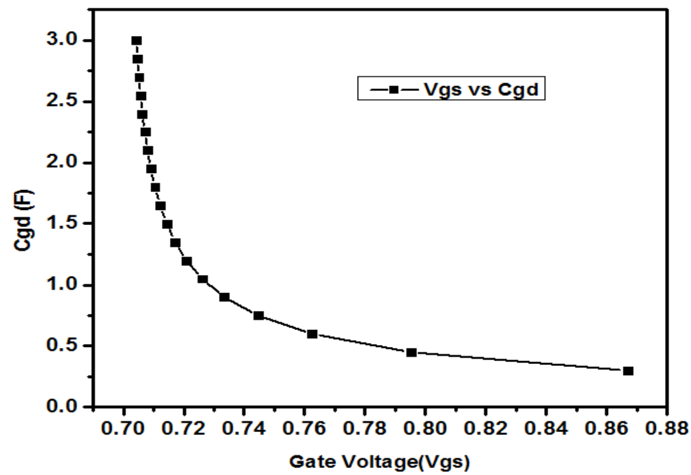


Figure 6.4: Variation of respect to gate voltage with respect to capacitance

Therefore, drain current for capacitance model is given as

$$I_{AJDG} = \frac{V_{ds}}{R_{ON}} \quad (23)$$

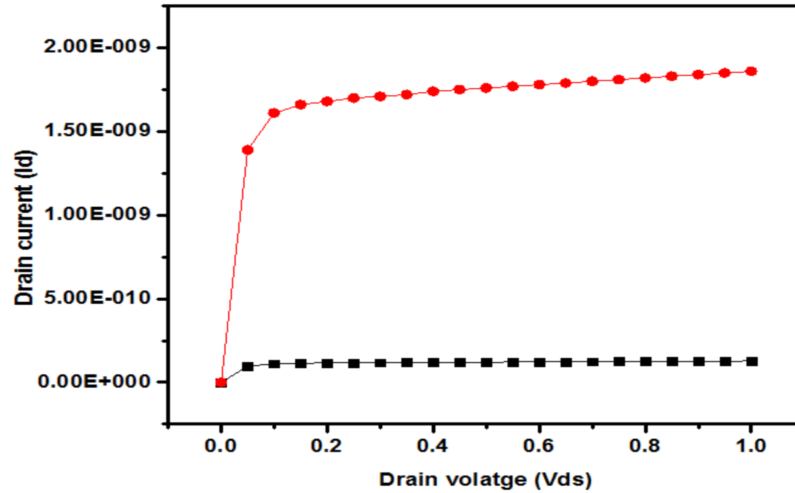


Figure 6.5: Variation of drain voltage with drain current

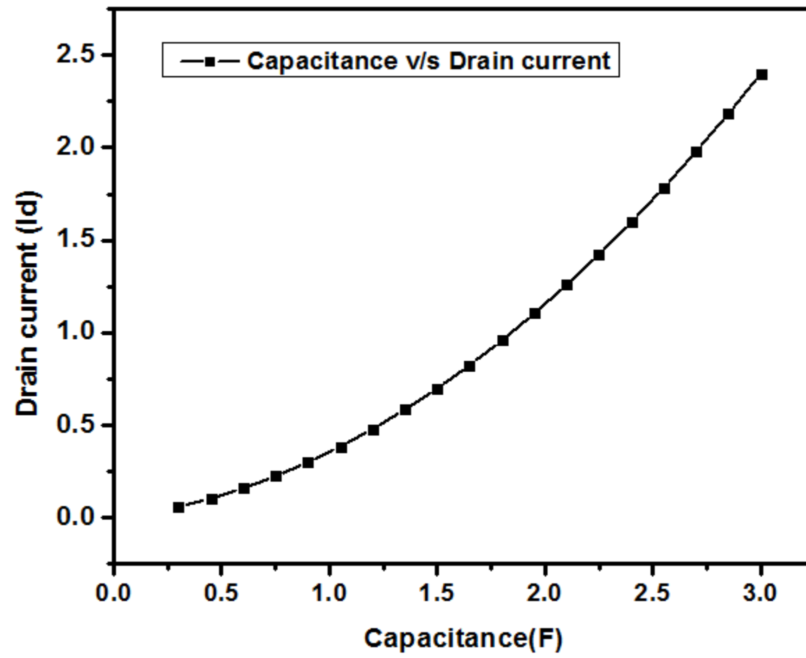
When both transistors of the DG MOSFET are turned on, Csb and Cdb are not present, hence less signals are connected to the substrate since the substrate is not present in this configuration. As a result, there is no dissipation in the Rb substrate resistance. When the transistor is in the cut-off zone, a rise in Cds1, Cds2, Cgd1, Cgd2, Cgs1 and Cgs2 leads to greater isolation between the source and drain owing to the absence of capacitive coupling between these terminals. Figure 7 shows the variation of total capacitance (Cgd) with gate voltage (Vgs). From the graph, it is observed that as the gate voltage increases the capacitance decreases. The gate voltage is inversely proportional to capacitance from equations (i) and (iii). This shows that the proposed transistor shows good switching characteristics with low ON-state switching capacitance leading to the low value of transistor delay.

Figure 8 shows the variation of drain voltage with drain current. It is observed with a large change in drain voltage the change in drain current is very small which shows that gate

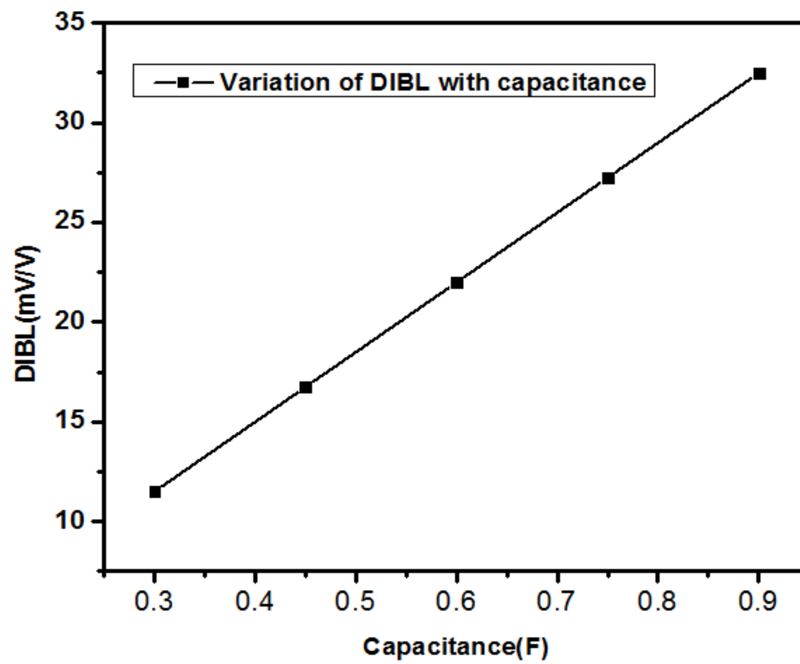
has good control over the channel. With the change in drain voltage the drain current starts flowing and after a certain point becomes constant.

6.4 Subthreshold parameter variations with gate capacitance

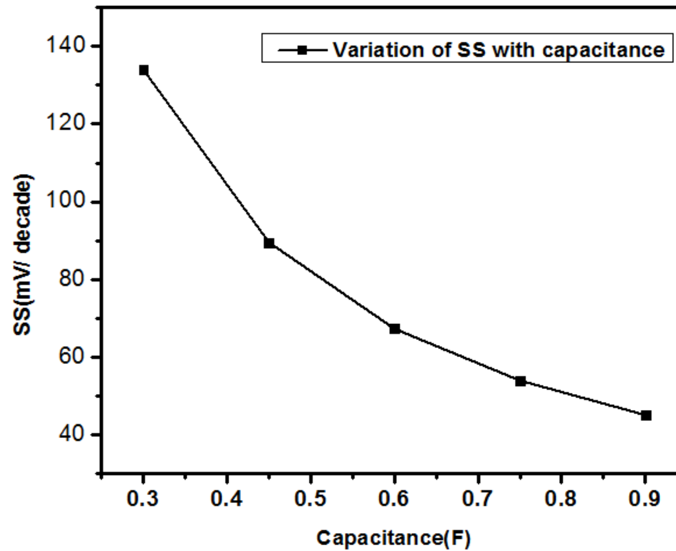
From figure 6.6 (a) it is observed that the value of capacitance increases with an increase in drain current. DIBL (drain-induced barrier lowering) is a SCE. When the drain bias is applied it reduces the potential barrier from source and drain that allows the flow of electrons from source to drain. Variation of DIBL with capacitance is shown in figure 6.6(b) DIBL ratio is given as $\delta V_{gs}/\delta V_{ds}$. DIBL is proportional to the capacitance. With the increase in capacitance, there is an increase in the DIBL ratio. The subthreshold slope is the slope between the drain current and gate voltage during the subthreshold region. The subthreshold slope is given as SS=$\frac{dV_{gs}}{d(logI_{d})}$. It is one of the SCE which degrades the performance of the device. Figure 6.6 (c) shows the variation of SS with capacitance. With the increase in SS the capacitance decreases. SS is inversely proportional to the capacitance.



(a)



(b)



(c)

Figure 6.6 : (a) Variation of capacitance with drain current(b) Variation of DIBL with capacitance (c) Variation of SS with capacitance

6.5 Summary

In this chapter analysis of surface potential is performed for AJDG MOSFETMOSFET having channel length as 18 nm and gate length is 11 nm is derived based on solutions obtained from 2D Poisson's equations. The proposed device is divided into three parts where the first and third part behaves as single gate MOSFET and the second part as double gate MOSFET. Surface potential determined through mathematical model is validated through simulation data. The surface potential model results are in closer proximity to the simulation results obtained using TCAD device simulator. Variation of surface potential along channel length shows an ideal behavior for different gate oxide materials and gate oxide thickness. Equivalent capacitance model is designed for calculating the total capacitance of the device and its effects on subthreshold parameters are analyzed. DIBL and SS curves with respect to capacitance is showing smooth variations.

CHAPTER 7

CONCLUSION AND FUTURE SCOPE

7.1 Conclusion

The the proposed structure 18 nm dopingless AJ DG MOSFET has two gates placed in an asymmetrical manner to each other. The drain, source, and channel all have different doping concentrations. Short channel effects (SCEs) are suppressed more in dopingless AJ DG MOSFETs, resulting in improved device performance. The I_{ON}/I_{OFF}(2.77x 10^{11}) ratio increases by more than 100%, but the SS (59.5 mV/V) and DIBL (10.5 mV/V) values also drop.Therefore SS and DIBL are reduced significantly by 4.52 % and 87.3% respectively. A sensitivity analysis is carried out and noticed between dopingless AJ DG MOSFETs and AJ DG MOSFETs with equal doping. Different factors relevant to the sensitivity of dopingless AJ DG MOSFETs, such as drain extension, gate overlapping length, and oxide thickness, are varied in both device topologies. When the settings are changed, the sensitivity of the dopingless AJ DG MOSFET is poor, according to the findings. Temperature analysis was carried out at temperatures of 250 K, 300 K, 350 K, and 400 K. A MOSFET-based biosensor is designed to detect a variety of enzymes, infections, and antigens in a short amount of time. With the use of FET-based biosensors, it is simple to detect a disease at an early stage. By generating a nanogap at the gate-oxide contact, a steep subthreshold highly doped n+ pocket asymmetrical JL MOSFET is exploited for biomedical applications. The gadget is analysed using dielectric modulation. It is demonstrated that p channel and n channel dopingless AJ DG MOSFETs are compatible. The use of dopingless AJ DG MOSFET n-channel and p-channel to design a reduced power inverter circuit and a 6T SRAM cell is demonstrated. The surface potential of an AJDG MOSFET with a channel length of 18 nm and a gate length of 11 nm is calculated using solutions derived from 2-D Poisson's equations. The suggested device is split into three pieces, with the first two acting as single gate MOSFETs and the

third acting as a DG MOSFET. The surface potential calculated using a mathematical model is verified using simulation data. The simulation results achieved with the TCAD device simulator are closer to the surface potential model findings. For varied gate oxide materials and gate oxide thicknesses, variations in surface potential throughout channel length demonstrate an optimum behaviour. The equivalent capacitance model is used to calculate the device's total capacitance and to investigate its influence on subthreshold parameters. With regard to capacitance, the DIBL and SS curves exhibit smooth fluctuations.

7.2 Future Scope

- Analog and RF study of the short-channel of 18 nm JL DG MOSFET can be carried out.
- Equivalent circuit models of the 18 nm JL DG MOSFET for both the low and high frequencies could be useful for the design and simulation of the analog and digital circuits.
- The fabrication and testing of a 18 nm DG JL MOSFET can be carried out

7. 3 Major Contributions

- A novel Dopingless AJ DG MOSFET of 18 nm channel length and n+ pocket AJ DG MOSFET are designed.
- SCEs such as DIBL and SS are significantly reduced thereby enhancing the performance of the device.
- The I_{ON}/I_{OFF} ratio of the proposed device is significatly increased.
- Different application such as biosensor , inverter, SRAM cell using the proposed device are implemented.

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LIST OF PUBLICATIONS

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