DESIGN AND OPTIMIZATION OF HETEROJUNCTION MULTIGATE FINFETS WITH PROCESS VARIATION.

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Electronics and Communication Engineering

By

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LOVELY PROFESSIONAL UNIVERSITY
PUNJAB
2022

DECLARATION

I declare that the thesis entitled **“Design and Optimization of Heterojunction Multigate FinFETs with Process Variation”** has been prepared by me under the guidance of **Dr. Suman Lata Tripathi,** Associate Professor, School of **Electronics and Electrical Engineering** at **Lovely Professional University, Punjab, India**. No part of this thesis has been included in or has formed the basis for the award of any Degree or Diploma or Fellowship of any institution or university anywhere previously.

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ABSTRACT

Expeditious magnification and Inception of FinFET mechanization has inculcated new paradigms in the vertical of Nanotechnology. It can be defined through feigning for FinFET that it may be spanned down to almost 10 nm. Though the synthesis of ultra-thin fin may trigger the short channel repercussions. FinFet introduces the ionization characteristics which depicts it as an inheritor to the Single gate MOSFET, further the simplicity of the process of formulation of FinFET in comparison with the MOSFET, it may become a highly usable product. All the modern-day technologies and industries based upon Silicon are foreseeing FinFET transistors as highly productive, usable, agile, robust, and due to which it can participate as one of the crucial members in the never ending new- developmental arena. The retardation and speed spins are an important aspect in ICs as both of them are complementary to each other. MOSFEST's gauging has given a new dimension to the size of the IC's. Short Channel Effects (SCEs) kicks-in with MOSFET, if we dig down to nanometer architecture which impacts the attainment and dependability which further can be addressed using FinFET as they have minimum efflux, less threshold voltage and perfect gate control. Although there are certain issues with them as well, like if we go beyond 10nm, leakage problem creeps in which gives rise to other important concerns such as threshold flattening, increase in power density and thermal dissipation. However, with the respect to the matter of heat dissipation, FinFET composition is less coherent as heat can be collected on the fins, thus resulting in the inception of altogether a naïve vertical of design rule – the design for thermal though there are other rules exists already such as design for manufacturability. All these devices are nearing their extinction, so one has to be ready with some new alternatives or inventions with respect to device structure so that the weaknesses can be addressed and also to see the possibility of using new material types instead of currently used materials like silicon. Among them, Carbon Nanotube (CNT) FET, Gate-All-Around Nanowire FET, or FinFETs with compound semiconductors may prove as promising solutions in future technology nodes.

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High achievement always takes place in the framework of high expectations. The expectation was there and I begin with determined resolve and put in sustained hard work. It has been rightly said that every successful individual knows that his or her achievement depends on a community of persons working together but the satisfaction that accompanies the successful completion of any task would be incomplete without the mention of the people who made it possible.

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ABBREVIATIONS

2D	Two Dimensional
3D	Three Dimensional
BOX	Buried Oxide
BTBT	Band-to-Band Tunneling
C_{ds}	Drain to Source Capacitance
Cg	Gate Capacitance
CMOS	Complementary Metal Oxide Semiconductor
CV	Characteristics Capacitance-Voltage Characteristics
CVD	Chemical Vapor Deposition
DIBL	Drain Induced Barrier Lowering
E_{dyn}	Dynamic Energy
E_{leak}	Leakage Energy
EOT	Effective Oxide Thickness
E_{total}	Total Energy
FET	Field Effect Transistor
FinFET	Fin based 3D Field Effect
GAA	Gate All Around
GIDL	Gate Induced Drain Leakage
I_C	Integrated Circuits
I_{off}	Off Current
I_{on}	On Current
ITRS	International Technology Roadmap for Semiconductor
IV	Characteristics Current-Voltage Characteristics
MOS	Metal oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
NMOS	N-channel MOSFET
PMOS	P-channel MOSFET
SCE	Short Channel Effect

TCAD	Technology Computer Aided Design
TEM	Transmission Electron Microscopy
T_{ext}	Extension Thickness
T_{ox}	Oxide Thickness
T_{si}	Fin Thickness
T_{sp}	Spacer Thickness
VDD	Supply voltage

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Chapter 1

Introduction

1.1 OVERVIEW OF METAL-OXIDE FIELD-EFFECT TRANSISTOR

Downscaling is a significant and effective approach to attaining semiconductor devices' highest performance regardless of technological challenges. The channel length is noticeably shortened due to the scaling of the devices. As per Moore's law, the size of the transistors will double every two years. These components must be scaled as the number of components on the chip grows while keeping the space constraint in mind. Moore's law is most likely responsible for the evolution of digital technology. This rule should be regarded as an observation rather than a physical rule. As devices become smaller, several limitations affect the devices' performance. When devices are scaled, short channel effects become visible. New transistor technologies that are free of junctions are known as junctionless technology [1], [2], [3] and are used to achieve the precise and optimal performance of devices during scaling.

There are seven sections in this chapter. Section I provides a high-level overview of the research topic. FinFETs and their importance in VLSI circuits are introduced in Sections II and III. The research's objective is described in Section IV, and the numerous research gaps are depicted in Section V. Finally, Sections VI and VII contain the work's aims and thesis organization.

1.2 RETRENCHMENT OF DEVICES

The speed, power consumption, and area of a digital system are the key impediments. All three pitfalls can't be fixed at the same time. There is no need to make concessions on any of these flaws. To boost the device's speed, we must reduce its physical dimensions, which reduces its area. However, SCE enters the scene and begins to increase power dissipation, increasing power consumption. Devices are scaled from 10um to 5nm in the International

Technology Roadmap for Semiconductors, with 5nm projected in 2020 [2], [3]. The scaling trend of devices is depicted in Table 1.1 from 1971 to 2022. The projected years for achieving the physical gate length of devices are listed in the table below. Etching, photolithography, metal deposition, and other procedures are used in the development of integrated circuits. When it comes to scaling, all of these procedures represent a roadblock for the fabrication business. There are many more parameters that must be scaled when scaling devices, such as the power supply [4], [5], [6], [7]. The change of physical channel length over time is shown in Table 1.1 [4].

TABLE 1.1: Scaling Trend [4]

Channel length	**Years**
7 µm	1974
2 µm	1982
700 nm	1989
450 nm	1995
350nm	1997
280nm	1999
180nm	2001
90nm	2004
55nm	2006
45nm	2008
32nm	2010
20 nm	2012
10 nm	2016-2017
7 nm	2018-2019

5 nm	2020-2021

1.3 TRADITIONAL METAL-OXIDE-SEMICONDUCTOR TECHNOLOGY

All transistors rely on the induction of various types of doping to produce junctions in the substrate. Metal oxide semiconductors are made with source and drain junctions (MOS). A P-N junction is formed when trivalent type impurity p-type and donor type impurity n-type semiconductors are joined. Diffusion is the movement of carriers from one concentration to another as a result of a concentration gradient [8]. Electrons begin to transition from n-type to p-type, while holes begin to transition from p-type to n-type during the diffusion process. When this happens, some electrons and holes along their path recombine, leaving positive and negative ions in their wake. As a result, a depletion zone develops where there are no mobile providers. The space charge area of the p-n junction is represented in fig 1.1.

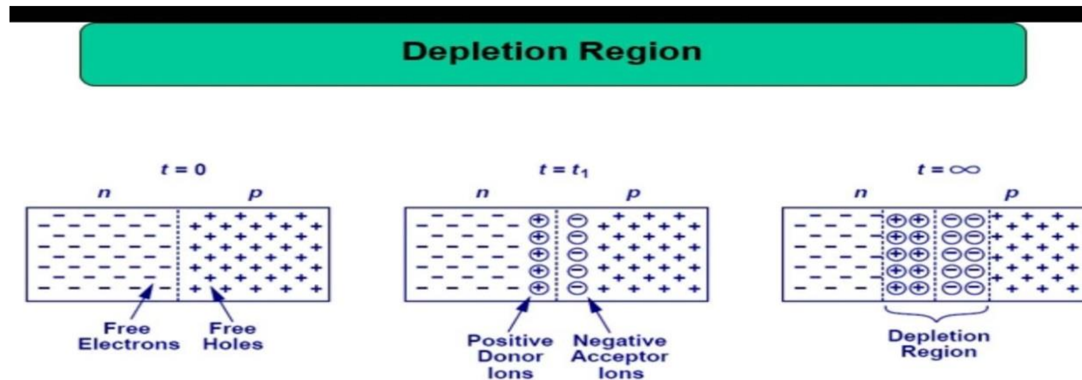


Fig 1.1 Generation of the depletion region.[9]

A doping gradient is present in conventional transistors, resulting in the formation of P-N junctions. The current starts or stops flowing depending on the bias supplied to the junction. There are two junctions in a MOSFET. The physical length of the channel is measured by the space between drain and source. There are two gates coupled together in a traditional double gate MOS. The source and drain of an N channel transistor are n-type, while the

substrate is p-type. The device operates in three modes in conventional type MOS, called inversion, depletion, and accumulation. The majority of charge carriers are accumulated in the accumulation mode, removed in the depletion mode, and the n channel is formed from the p-substrate in the inversion model. When voltages are applied to the gate then, all of these modes are triggered. Two back-to-back diodes exist between the source and drain when the gate voltage is not applied. Between the drain (n+) and the substrate, one diode is made, and between the source (n+) and the p substrate, the other is formed. These diodes prevent conduction between the source and the drain even when the drain voltage is applied. As a result, conduction requires the gate voltage [10].

When a negative voltage is applied to the gate terminal of an N channel MOS, it begins to attract the holes in the channel area, which is known as the accumulation mode. When the gate voltage is set positive after accumulation, depletion-mode enters the scene. When the gate voltage reaches the point where the surface concentration of electrons equals the bulk concentration of holes, the threshold voltage is attained. At this voltage, the MOS begins to invert. When voltage is added to the gate, accumulation begins, and the direction of the electric field shifts to point towards the gate. The conduction band and the valence band are both bent upwards. A voltage is formed when both bands become flat, and this is referred to as flat band voltage. In an NPN transistor, if positive fixed charges are present in the oxide, these charges will suck the electron from the substrate even if no voltage is applied, resulting in the production of an inversion layer. While such devices are downscaled to channel lengths of 10nm or less, adding shallow junctions in the device becomes extremely difficult. Fabricating large-sized devices has become a significant issue for the semiconductor industry.

1.4 DG-MOSFET

A MOSFET with two gates for controlling the channel is known as a double gate MOSFET (DG-FET). The DG-MOSFET is shown schematically in figure 1.2.

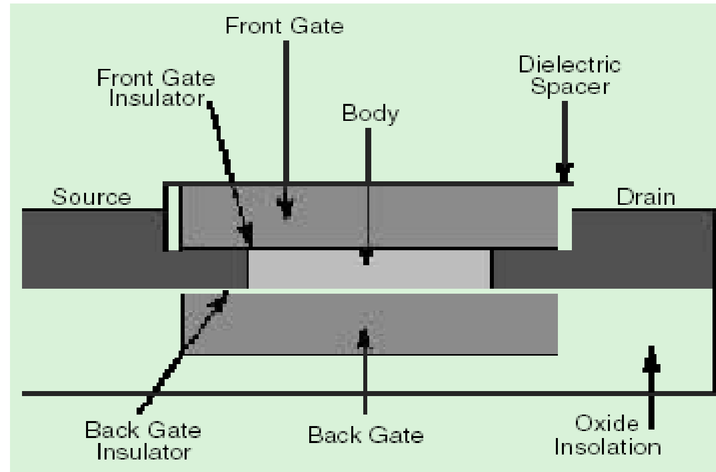


Fig. 1.2: Cross-section of Double Gate FET. [11]

Its main advantage is improved gate-channel control. Because all of the drain field lines are unable to reach the source, it also results in lower SCE when utilized in conjunction with ultrathin bodies in an SOI implementation (FDSOI DG-FET). This is owing to the lower dielectric constant of the gate oxide than Si (assuming SiO2), as well as the ultra-thinness of the body. Because it is more resistant to SCE and has superior gate-channel control, the physical gate thickness can be increased (compared to planar MOSFET). As a result, there are fewer leakage currents (D/S leakage and gate leakage).

There are two types of double-gate FETs:

- Asymmetric
- Symmetric

The front and rear gates of symmetric DG-FETs feature identical gate electrode materials (i.e. bottom and top gates). The channel has generated on both surfaces when symmetrically driven. The bottom gate and top gate electrode materials can differ in an asymmetric DG-FET (for example, p+ poly and n+ poly). When driven symmetrically, this will only build a channel on one of the surfaces. Both have their benefits and drawbacks. In a later section of this study, recent work on them will be discussed. Figures 1.3 and 1.4 show symmetrical and asymmetrical DG-FET energy band graphs.

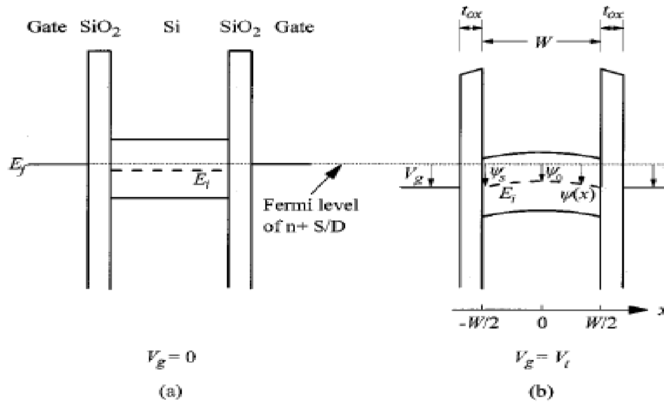


Fig. 1.3: Energy band diagram of Symmetrical DG-FET [12]

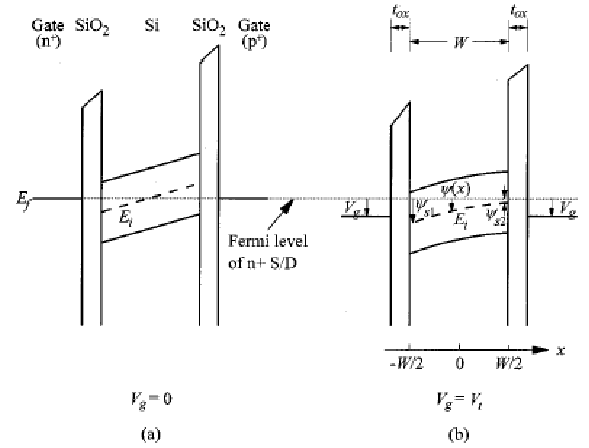


Fig. 1.4: Energy band diagram of Asymmetrical DG-FET.[12]

The manufacture of DG-FETs is the major, and possibly only, stumbling block. There are three approaches [7, 4] to make a double gate FET, which are labeled with type 1, type 2, and type 3 in the figure. 1.5. Fabrication issues plague Types 1 and 2, making it difficult to construct both gates of the same size and precisely aligned to each other. It's also difficult to align the source/drain areas to the gate margins precisely. Furthermore, because the bottom gate is buried in Type 1 DG-FETs, it is difficult to produce an area-efficient contact and low resistance.

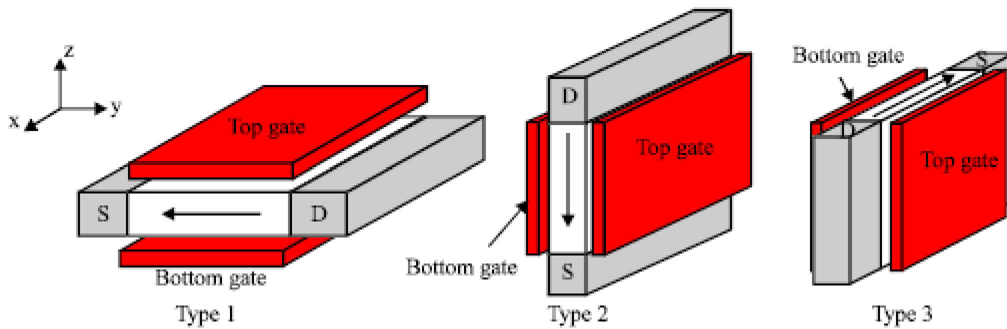


Fig 1.5: Three possible realizations of DG-FETs.[13]

1.5 FINFETs

FinFETs are DG-FETs of type 3. Even though current conduction occurs in the wafer's plane, it is not strictly a planar device. Instead, it's referred to as a quasi-planar device since its vertical geometry (i.e. fin height) has an impact on device behavior. The FinFET is the simplest of the DG-FET types to manufacture. Figure 1.6 illustrates its schematic.

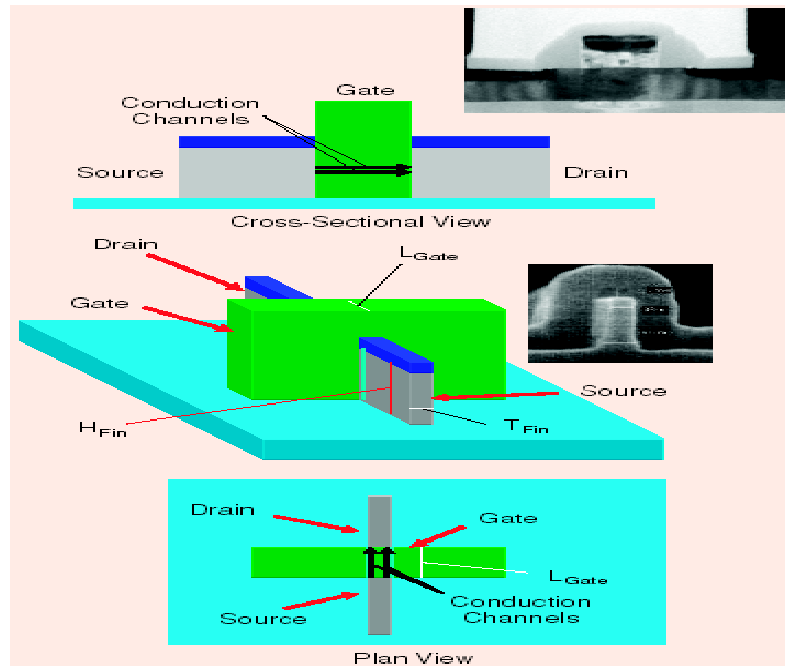


Fig. 1.6: FinFET structure. [14]

It's called a fin because of the vertically narrow channel structure, which looks like a fin of fish, that's why called a FinFET. A gate can also be added to the top of the fin, resulting in a triple gate FET. Alternatively, the oxide above the fin can be thickened to the point where the gate is virtually non-existent.

While the gate length L of a FinFET is identical to that of a regular planar FET, the device width W is somewhat different. The width of the fin is defined as:

$$W = 2H_{fin} + T_{fin} \tag{1.1}$$

where T_{fin} is thickness and H_{fin} is the fin height. The rationale becomes clear when one realizes that W, as indicated above, is the breadth of the gate region in contact with (and

thus in control of) the channel in the fin (albeit with a dielectric in between). This is particularly noticeable when the gate is opened (i.e. unwraps it).

The width definition for a triple gate FinFET is shown above. If the gate above the fin is missing or ineffective, the T_{fin} term in the preceding definition is omitted. On the surface, this upward freedom (the ability to increase H_{fin}) appears to be a highly desirable characteristic because it permits the device width W to be increased without expanding the planar layout area (Increasing W raises the Ion, which is a good thing.) However, because there is a certain range (in relation to Tfin) beyond which Hfin should not be increased, or else SCE will occur [15, 16], Hfin should not be increased beyond that range. FinFET scaling and greater drive current for future devices have been made achievable by gate work function engineering, thinner gate oxide, and more streamlined FinFET processes [17]. In 2011, Intel Corporation created a new transistor technology called "3D Trigate." [18]

1.6 MULTIGATE FET

A multi-gate device has numerous gates on multiple surfaces around the channel to effectively suppress "off-state" leakage current. Multi-gate devices also allow for higher current per region in the "on" state. These advantages equate to lower leakage power consumption and better device performance. Nonplanar transistors are also more compact than planar transistors, enabling higher transistor density and chip size reduction.

Furthermore, several gate layouts such as Tri-gate, Si nanowire FET, Fin FET, planar double-gate, and Gate-All-Around (GAA), and others have been proposed and proven. The multi-gate Si FinFETs are schematically illustrated in figure 1.7.

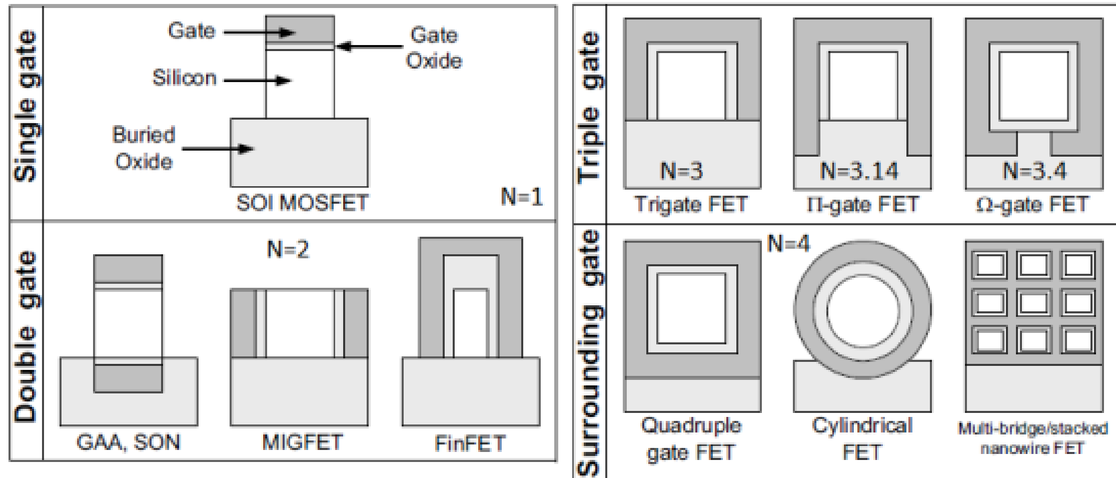


Fig. 1.7 Multigate device structures. [19]

1.7 NEED FOR LOWER POWER-BASED DEVICES.

The internet of things (IoT) has become an increasingly prominent topic of discussion in recent years. The goal of the Internet of Things is to connect any device to the Internet. This category includes cellphones, coffee makers, washing machines, wearable devices, and almost everything else we can think of. By 2020, Cisco and Ericson expect that there will be more than 50 billion connected devices. [20]

The evolution of personal electronics such as cell phones, computers, laptops, and tablets is depicted in figure 1.8. The world's population, on the other hand, limits its growth. The actual increase is being driven by all of these linked gadgets in areas like home automation, hospitals, and transportation. There will be a near-infinite number of gadgets available. All of these devices should be energy efficient and have a long battery life, but not at the expense of performance.

1.8 MOTIVATION

The growth of microelectronic devices occurs rapidly in terms of cost, size, and performance. The scaling of the device dimensions acts as a kick point for the

semiconductor industry that allows the manufacturing of the integrated circuit with reduced size, and the hat further leads to an increase in transistor density.

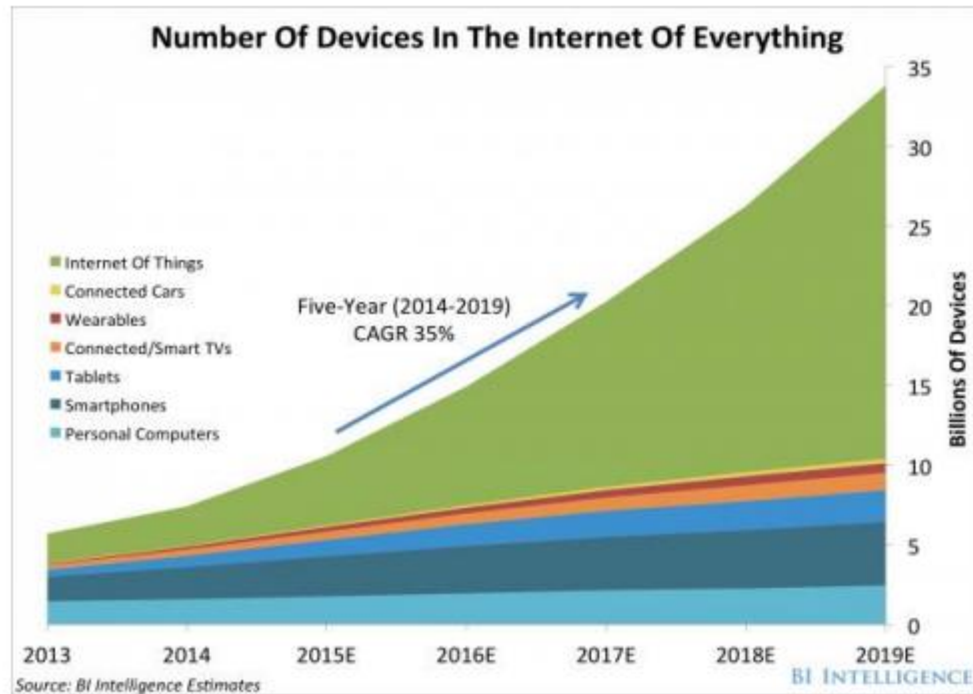


Fig. 1.8 IoT expansion in the market. [20]

As per the current scenario of International Technology Roadmap 2007, the physical gate length of the devices that are used in high-performance circuits are around 20 to 5nm by 2022 [21]. This shows a clear indication of the microelectronic industry entering into a new era of technology that is based on the nano dimension.

FinFET device scaling is a critical part of improving performance and achieving high performance and low power-based VLSI circuits. As a result, an accurate assessment of device performance and properties at the nanoscale is critical for understanding the FinFET device's limit and developing a new concept.

Short Channel Effects (SCEs) rise when the device's channel length decreases, causing the device's performance to suffer [22]. The most challenging aspect in the scaling of MOSFET is to control the SCEs. For better integrity on reduced channel length, the double gate

MOSFETs and FinFET play a vital role in it. FinFETs, on the other hand, have better electrostatics than single gate MOSFETs due to channel controllability [23].

Reducing supply voltage is one of the key parameters to keep the low switching power dissipation. But for attaining the high-performance device, however reduction in threshold voltage (V_{th}) is required. The reduction in the threshold voltage (V_{th}) in MOSFETs, leads to an increase exponentially in leakage current that degraded the static power of the device [24]. So, analysis of FinFETs device on the nanoscale is very important for attaining a high-performance circuit in VLSI.

1.9 RESEARCH GAPS

Even though lots of work was carried out on the FinFET device. There are still a few issues that need to be worked out more thoroughly. A few studies show the process variation impact like temperature variation and oxide thickness variation on heterojunction multigate FinFETs on lower channel length (less than 20nm). Similarly, computational modeling was implemented in a few numbers. In the vast majority of cases, the existing mechanism is chosen for heterojunction multigate FinFETs either by an experimental approach or through the use of a hardware-based modeling environment. Because experimental procedures produce extremely trustworthy results, no research has examined computational complexity to date, making the methodology less relevant in real-time and large-scale commercial applications. The hardware-based approach makes use of a specific simulation environment, which limits the computational capability in this case. When the device gate length is scaled below 20nm, FinFETs have a weak subthreshold slope and a large leakage current, hence the primary concerns related to short channel effects persist. This option is critical for creating a low-power application. The impact of fin shape and fin material variation on the performance parameter of the FinFET device has been demonstrated in a few kinds of research.

1.10 OBJECTIVES

The objectives of the work are as follows:

1. To design the heterojunction Multigate FinFET and its comparison with conventional FinFET.
2. To perform process variation on heterojunction Multigate FinFET.
3. To analyze the impact of the fin shape on the performance parameter of the heterojunction multigate FinFET.
4. To perform the verification for desired IOT based performance at different technology based on power and speed factor.

1.11 THESIS ORGANIZATION

The following are the six chapters that comprise the thesis:

Chapter 1 provides the introduction and limitation of the planer MOSFET and the need for low power devices for future technology nodes followed by the introduction of FinFET. Further, the motivation, research gaps, objectives of the proposed work have been discussed in the same section.

Chapter 2 provided the review of existing literature for the proposed work. In this review, the different techniques for reducing the SCEs and fin shape impact on the performance parameter have been discussed. This chapter also discusses the obstacles, simulated and measured outcomes, and their applications.

Chapter 3 covers the models used in device modeling and describes the simulation approach for 14nm gate length Heterojunction FinFETs. The current-voltage characteristics of simulated models are compared to experimental results to calibrate the models.

Chapter 4 shows the simulation of the inverted T-shaped 14-nm heterojunction FinFET and its comparison with rectzoidal shaped FinFET and rectangular-shaped FinFET. In this chapter impact of the Mole fraction (Si_{1-x} Ge_x) in the fin, the material was also analyzed.

Chapter 5 shows the synthesis of the inverter circuit by using the proposed design and analyzing its performance as per transient and dc analysis.

The future scope of the suggested study is discussed in Chapter 6.

Chapter 2

Literature Survey

2.1 INTRODUCTION

The dimension of the transistor has been reducing on a scale of nanometers with passing years. Scaling of the transistors acts as an advantageous step for attaining the higher packaging density and high performance with low power consumption [25]. In the future, microelectronic devices play a key role in the future of the VLSI circuits. Both microelectronic and nanoelectronics make a hybrid model that will boost up a powerful system and structures. Certain modifications in the traditional CMOS transistor will lay a foundation of some novel nanodevices like Double Gate (DG) Metal Oxide Semiconductor Field Effect Transistor (MOSFET, Silicon on Insulator (SOI), and FinFET [26]. For overcoming the limitation of the CMOS transistor, is very important to understand these new device operations and structures.

It's very easy to scaled-down the SOI devices with multigate like double-gate FinFET or Multi-Gate FinFET as compared to the conventional bulk-Si devices [27] [28]. The important feature of Multigate SOI MOSFET is good to hold on channel region through a gate that minimized the SCE effects in the device. Quantum Mechanical plays an important role in these devices due to its ultra-thin Si-body and gate dielectric [29]. Because of the high leakage current and short channel impact below 50nm, typical CMOS devices limit scaling. Minimizing the leakage current requires a thin gate dielectric with a heavily doped body that is not feasible in conventional CMOS. Multigate FinFET structures can easily overcome these and other scaling limitations. The multiple gates on the device, make the channel to gate capacitance is double that controls the channel potential in a better manner by the gate electrode that further limits the leakage current.

As compared to the bulk planner MOSFETs, FinFET shows the simple process and compatibility with the current flow. The property of self-alignment of the FinFET structure, makes it more advantageous in comparison to bulk MOSFETs or double gate MOSFET

due to the lower value of gate to drain capacitance and intrinsic gate to source, which is a result of high-speed operation. Due to the fast progress of the processing technique, the size of the MOSFET device is quite aggressive. But as the MOSFET device scaled down that led to an increase in the short channel effect [30]. A little modification in the import atom inside the limited area of the Si channel has a substantial impact on the effective doping density when the device is scaled down. As a result of the variation in doping density, managing threshold voltage is always a difficult task, as there is a typical link between threshold voltage and doping density. For regulating the threshold voltage (Vth), many studies have always concentrated on high doping density [31],[32],[33].

2.2 EFFECT OF SHORT-CHANNEL

As the size of the device shrinks, the distance between the drain and the source shrinks, affecting the controllability of the gate electrode over the channel region, causing the short-channel effect. This effect will be limiting the scaling of the MOSFETs [34]. With the help of the voltage-doping transformation, the technique can translate the effects of shrinking device parameters like drain voltage or gate length into the electrical parameter. Drain-induced barrier lowering (DIBL) and short-channel effects (SCE) can be derived from the voltage doping transformation model [35].

$$\mathrm{SCE} = 0.64\,\frac{\varepsilon_{Si}}{\varepsilon_{ox}}\left[1+\frac{x_j^2}{L_{el}^2}\right]\frac{t_{ox}}{L_{el}}\frac{t_{dep}}{L_{el}}V_{bi} = 0.64\,\frac{\varepsilon_{Si}}{\varepsilon_{ox}}\,\mathrm{EI}\,V_{bi} \tag{2.1}$$

and

$$\mathrm{DIBL} = 0.80\,\frac{\varepsilon_{Si}}{\varepsilon_{ox}}\left[1+\frac{x_j^2}{L_{el}^2}\right]\frac{t_{ox}}{L_{el}}\frac{t_{dep}}{L_{el}}V_{DS} = 0.80\,\frac{\varepsilon_{Si}}{\varepsilon_{ox}}\,\mathrm{EI}\,V_{DS} \tag{2.2}$$

Where V_{bi} is the drain or source built-in potential, x_j is the drain and source junction depth and L_{el} is the effective channel length, t_{dep} is the penetration depth of the electric field from gate to channel region. Here EI factor is known as the electrostatic integrity. This electrostatic integrity depends on the dimension of the device and it measures the influence of the electric field on the channel region that is lined up from the drain region. So, this

factor caused the DIBL and SCE effects on the device [36]. So as per the above expressions 2.1 and 2.2, the threshold voltage of a MOSFET can be calculated fo a channel length L_{el}.

$$V_{TH} = V_{TH\infty} - SCE - DIBL \quad (2.3)$$

Where $V_{TH\infty}$ is represented here as a threshold voltage of a long channel device. If the gate length of the devices decreases then the threshold voltage is also decreasing and this concept is called threshold voltage roll-off [37]. For reducing the short-channel effects then as per equation 2.1, junction depth and thickness of the gate oxide need to be minimized by increasing the doping concentration.

2.3 SCALING OF METAL OXIDE SEMICONDUCTOR FIELD-EFFECT TRANSISTOR

The usage of bulk silicon MOSFET as shown in figure 2.1 in the semiconductor industry on large scale over the last 5 past decades. In nineteen, many other alternatives of bulk Si-based MOSFET have been proposed and invented. However, scaling down bulk Si MOSFETs below the 20nm node is challenging due to an increase in the capacitive coupling of the channel to the source as gate length decreases, which increases SCE effects. The main objective is to reduce the dimension of the device to increase the chip density and low cost per function with a high speed of operation. So, device scaling required a balance between the device's reliability and device performance. So, smaller devices required a uniformity scale for channel length. This is known as Drain Induced Barrier Lowering (DIBL) because it expresses itself as a) threshold voltage roll-off, b) increased off-state leakage current, and c) lowering of threshold voltage with higher drain bias [38].

Various technological advancements, such as ultra-thin gate dielectric [39], halo implant, ultra-shallow drain/source junction [40], and advanced channel dopant method [41], have been required to retain the relatively robust gate control of the channel potential device. Each of these technologies is approaching a basic physical limit, which will further limit the device's scalability [42].

In a MOSFET device, the thickness of the gate dielectric is one of the parameters for enabling

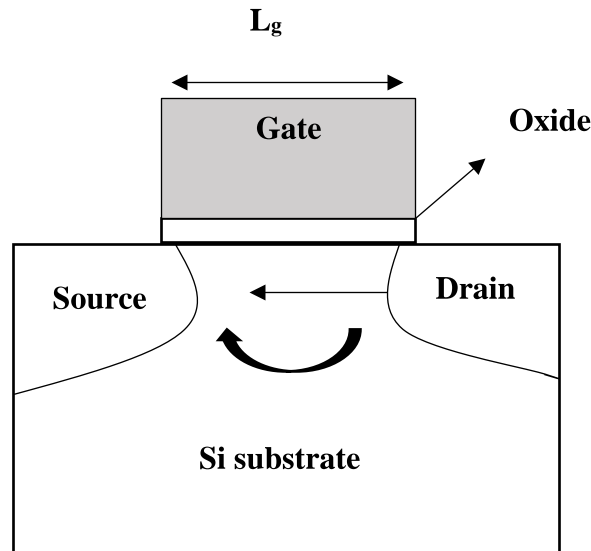


Fig. 2.1 MOSFET

the device scaling. But a thin gate increases the coupling capacitance from gate to channel that reduces the impact of source/drain on the channel region. However, larger gate capacitance increased the on-state current by increasing the inversion layer [43]. Because the capacitive coupling of the channel to the source increases as gate length decreases, scaling down bulk Si MOSFETs below the 20nm node is challenging due to increased SCE effects. [44]. To overcome this problem, another alternative solution of usage of high- k gate dielectric material has been proposed that provides an effective gate control for L_{el} scaling to control the leakage current [45].

2.4 CHALLENGES IN BULK CMOS

There are many challenges in CMOS technology to reduce the impact of the short channel effect, a high degree of dopant activation and ultra-shallow junctions with high doping are required [46]. Currently, many types of research are carried out on laser annealing and flash lamp annealing but these methods are not suitable for future technology nodes [47]. A polysilicon gate depletion effect hampers the threshold voltage and performance by contributing towards the effective oxide thickness. By using the metal gate technology, this effect can be eliminated. However, a separate gate material is required for PMOS and

NMOS devices to achieve the required work function which further leads to complexity in process integration. As polysilicon gates with a combination of silicon dioxide gate dielectric in bulk CMOS technology play the most suitable technology but the above challenges required a strong push for other alternative device structures and process techniques [48].

The major concern in bulk CMOS is static power consumption due to leakage current and short channel effect [49] and this leakage current is due to quantum mechanical tunneling, junction leakage, and subthreshold leakage. Using the high-k dielectric material in replace of Silicon dioxide insulator will sort out the leakage problem but not subthreshold leakage [50]. So new metal gate material is required along with high-k dielectric material to overcome this issue like strained silicon germanium or double gate MOSFET etc.

2.5 FINFET STRUCTURE

FinFET originally originated from the depleted lean channel transistor (DELTA) as shown in figure 2.2 [51].

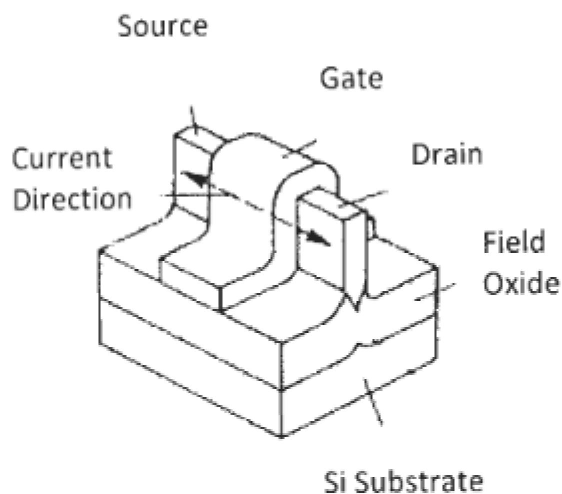


Fig. 2.2 DELTA [51]

Both DELTA and FinFET transistors work on the same principle. In FinFET and DELTA, the thin structure of the body known as the fin is connected with large source/drain pads. The sides of the fin are covered with the gate material and it is masked with high- k

dielectric material. The current conduction always takes place at the center of the fin and device current can be increased by using the parallel fins. In FinFET, the channel width is always defined by the fin height and if it is compared with the conventional MOSFET it will be twice the fin height.

The concept of a novel scaling technique, such as high-k/metal-gate and channel strain, was introduced to increase the transistor's performance and achieve superior stability concerning speed, power, and cost in the VLSI Circuit [52]. Due to the invention of the FinFET, it is now possible to scale down the length of the channel from 24nm to 6nm, resulting in improved channel electrostatics. The double gate structure is based on the historical channel length scaling trend, with the addition of a new scaling parameter known as channel thickness. The three-dimensional nature of the FinFET is shown in figure 1.2, which overall lowered the footprint of the transistor, and a new performance parameter known as a 'Fin-Effect' (W/Fin-Pitch) that is not present in MOSFETs structure has been introduced. FinFET performance is affected by fin height (H_{fin}), fin width (W), gate length (L_{gate}), as well as oxide thickness. These settings can be changed to improve the performance of FinFET devices [53].

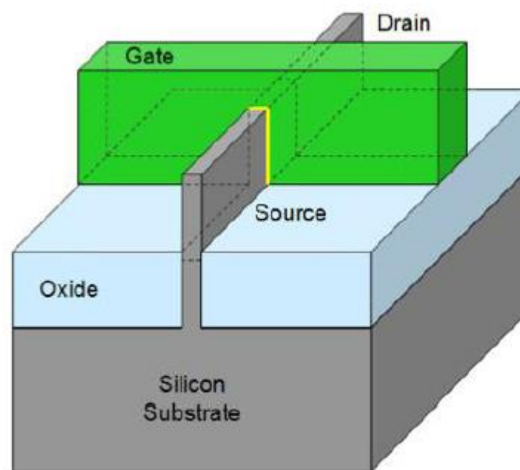


Fig. 2.3 Three-dimensional structure of tri-gate FinFET. [53]

However, to reduce the SCE, these parameters must be kept to a minimum, such as a fin thickness being equal to one-third of the length of the channel [54]. By adding a high-k dielectric material into the gate stack, leakage current can be reduced [55]. In general, the dielectric gate stack (typically high-k material) reduced oxide layer deterioration and enhanced capacitive coupling between gates and channels. FinFETs are difficult to construct a compact model for due to their reduced size and three-dimensional nature. By increasing the height of the fins, the Short Channel Effect in FinFETs can be mitigated, resulting in significant DIBL and a superior subthreshold slope.

When the Fins Effect is combined with the channel length, a superior result is achieved in terms of contact area reduction, which boosts contact resistance and device performance [56]. The two types of FinFETs available are SOI and Bulk FinFETs. The substrate fin is not attached to the substrate in the case of SOI; nevertheless, the substrate fin is directly linked to the substrate in the case of SOI. By minimizing direct contact between the fin and the substrate, SOI provides excellent insulation while also increasing the self-heating effect. Because of this self-heating, monitoring the temperature's impact on the FinFET device is crucial. The leakage current is reduced when the oxide material is replaced with hafnium oxide, although the temperature effect of this addition on the device is difficult to measure [57]. The off current can be reduced and the short channel effects can be reduced by using a spacer. To eliminate short channel effects in fin materials, metal gate contacts can be used instead of polysilicon [58], and GaAs can be used instead of silicon.

The fins in many FinFETs devices are constructed in a trapezoidal shape [60] to increase transistor performance at smaller sizes. When scaling down devices over a decade, the lowest value of subthreshold slope (SS) is limited to 60mV due to short channel effects (SCEs), and DIBL values should be as low as possible. Several scaling solutions, such as channel strain with diverse materials such as Ge, GaAs, and SiGe, high-k/metal-gate, can improve VLSI Circuit device performance in terms of cost, power, and speed [62].

When the VDD is lowered, the effect of the drain-induced field grows, forcing changes in overall transistor architecture from a single gate to many gates or gate overall around [63] to improve channel gate control by reducing subthreshold performance. The subthreshold slope of FinFETs can be increased by raising fin height, which minimizes oxide layer degradation and boosts capacitive coupling between channel and gates DIBL [64]. The contact area is reduced when the fins effect is paired with the channel length, increasing contact resistance and boosting device performance [65]. The SOI and bulk type structures that are available can be used to design the FinFET. In SOI, the substrate fin is not physically linked to the substrate, but in bulk, the substrate fin is physically attached to the substrate [66]. By minimizing direct contact between the fin and the substrate, SOI provides improved insulation, resulting in decreased leakage current and increased self-heating. Because of this self-heating, it's critical to keep an eye on the temperature's impact on the FinFET device [67]. By replacing the oxide material with hafnium oxide, the leakage current is reduced, albeit the temperature effect of this addition on the device is difficult to measure [68]. If the channel material is strained SiGe, fluctuations in the strained SiGe channel can cause a shift in transconductance and threshold voltage [69]. Modeling Challenges: As the size of electronic gadgets decreases, they become increasingly complex in terms of processing power [70]. This makes it very difficult to analyze and forecast the appearance of the gadget in its ultimate state. It consequently provides a considerable modeling difficulty for bodily processes. The field-level transistors (FINFET) that have the potential to replace the majority of MOS in nanotechnology. This is because FINFET fabrication process is nearly equivalent to that of a normal MOS transistor [71].

Due to its resistance to Short Channel Effects as well as conventional design, nanowires and FINFET have attracted a great deal of attention. Silicon NW FinFET (SNWFT) will be evaluated as a contender for CMOS nomination at 32 nm node because to its excellent performance, strong gate control, and travel improvements [72]. The compact controlled body and several gates give FINFET with strong short-term control, electrostatic protection against body inclusions, and relaxing drug or pocket-packing channels, which are crucial in planetary technology for preventing threshold voltage (V_{th}) emissions. Metal gates with

High-k (HKMG) dielectric Stacks give the Vth required for performance adjustment and minimizing gate leakage, making it possible to use gate engineering to produce devices with enough V_{th}. The three-dimensional nature of FINFET provides several advantages, such as the ability to increase the driving current while maintaining the same footprint. By using a channel switch that utilizes characteristics like carbon nanotubes (CNTs) or graphene, device performance on the micro scale may be enhanced via increased Ion/Ioff ratios and decreased leaks, resulting in lower power consumption. [73].

2.6 SUMMARY

Semiconductor industry research is driven by the incessant desire for miniaturization and improvement in semiconductor electronic devices. As traditional devices were shrunk to sizes below 50 nm in SCE, the necessity arose for the creation of new FETs. The electrical properties of the device, such as the threshold voltage, DIBL, SS, etc., are negatively impacted by SCE. The channel of multigate transistors may be controlled more precisely, and SCE is automatically muted. Studies on various multigate transistors are being conducted with an eye toward their eventual commercialization. It is generally agreed that FinFETs are the transistors of the future because of the sub-20 nanometer domain into which they may be scaled. However, it introduces new parasitic that degrade FinFET functionality. In this chapter, we have gone over the fundamentals of a FinFET and how it works, with special emphasis on two variations: the shorted gate and independent gate FinFETs. Different varieties benefit from different features. FinFET devices, like other MOSFET devices, are susceptible to device variability. Due to the nanoscale nature of FinFET production, several process variances cannot be avoided. The following chapter will concentrate on these FinFET device characteristics.

Chapter 3

Design of Multigate Heterojunction FinFET

3.1 INTRODUCTION

The main focus of this chapter is to study and describe the basic design procedure of Heterojunction FinFET and its comparison with conventional FinFET. As discussed in chapter 2, multiple techniques have been employed by the researchers to achieve the FinFET for lower applications. However, the initial step of all the mentioned designs is to achieve the Low power-based high-performance device for the VLSI circuit.

A basic FinFET device needs to possess certain characteristics such as minimum short channel effect, minimum off current, and high on current as stated in earlier chapters. The design process of the multigate Heterojunction FinFET device contains a few steps that are mentioned below:

- Selection of the structure design of FinFET i.e. SOI-based structure or Bulk-based structure.
- Finding the channel length, fin height, fin width and oxide thickness, and gate length of the device.
- Selection of the dielectric material for gate oxide.
- Selection of material composition for creating the Heterojunction
- Selection of the doping level for fin, source, and drain
- Parametric study of the device for optimal results

Based on these steps Fig. 3.1 demonstrates the basic design methodology used to design the multigate Heterojunction FinFET for low power applications. The purpose is to understand the basic simulation of the multigate Heterojunction FinFET. In this chapter, we have designed the 14-nm Heterojunction FinFET by using the SOI-based structure.

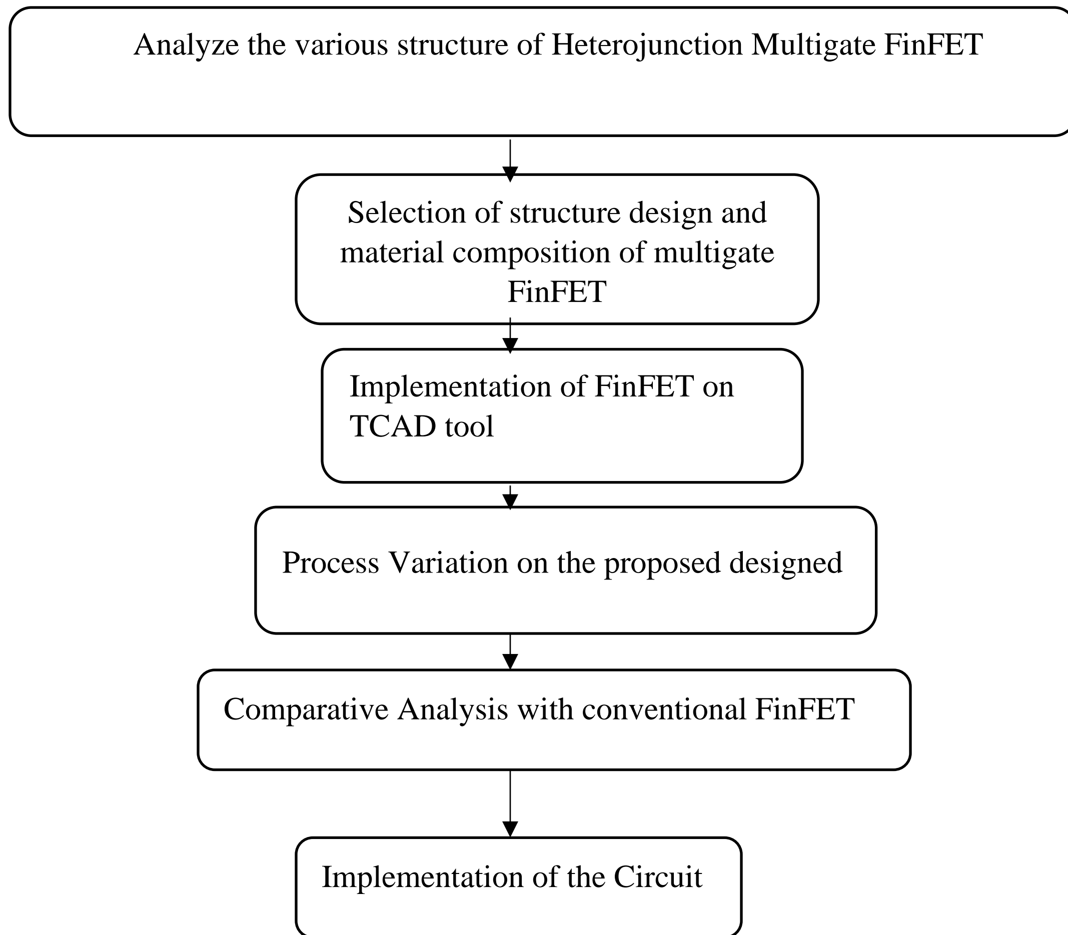


Fig. 3.1 Basic design methodology for Heterojunction FinFET

This chapter is organized into four sections. Section I represents the basic structural design and material composition of FinFET. Further, section II shows the comparisons of the proposed design with conventional FinFET and section III shows the process variation on the proposed design.

3.2 MATERIAL COMPOSITION & STRUCTURE DESIGN

The Bulk type and the SOI type are the two different structure kinds for designing FinFETs [74-76]. The fin of the FinFET is not directly attached to the substrate in the SOI type structure, but the fin is directly attached to the substrate in the Bulk type. As a result of the lack of direct contact between the fin and the substrate, the SOI type structure provides

better insulation and reduces the short channel effect in the device. As a result, we employed the SOI type structure in the suggested device, and figure 3.2 depicts the FinFETs basic diagram.

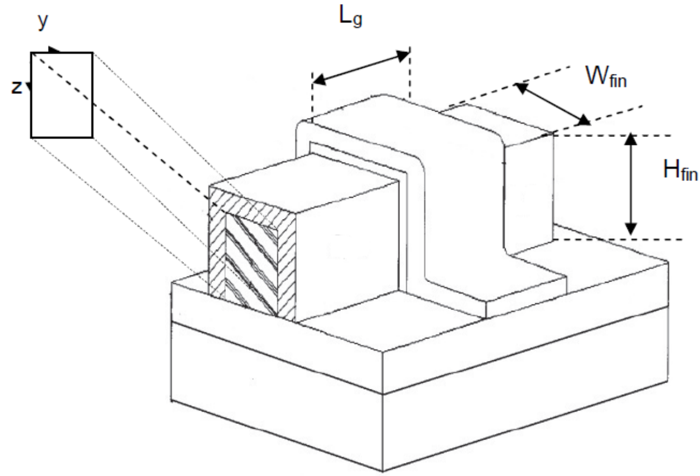


Fig. 3.2 Basic diagram of FinFET

Table 3.1: Dimension of the Device Region of 14-nm Heterojunction N-FinFET

Region of device	Material	Region Length	Region Width	Region Height	Doping Level
Extended Source -1 (a)	Silicon	13nm	10nm	20nm	$1x10^{20}$ /cm^3
Extended Source-2 (b)	Silicon	20nm	24nm	20nm	$1x10^{20}$ /cm^3
Extended Drain-1 (d)	Silicon	13nm	10nm	20nm	$1x10^{18}$ /cm^3
Extended Drain-2 (e)	Silicon	20nm	24nm	20nm	$1x10^{18}$ /cm^3
Fin (Channel)	Silicon-Germanium ($Si_{1-x}Ge_x$)	14nm	10nm	20nm	$1x10^{18}$ /cm^3
Gate (c)	PPolySi	14nm	2nm	23nm	-
Oxide	HFO_2	14nm	2nm	21nm	-
Contact Of source & drain (f)	Aluminum	20nm	1nm	20nm	-

Table 3.1, shows the dimension of the different regions of the 14nm Heterojunction N-FinFET and figure 3.3, shows the 3 D view of the 14-nm Heterojunction N-FinFET.

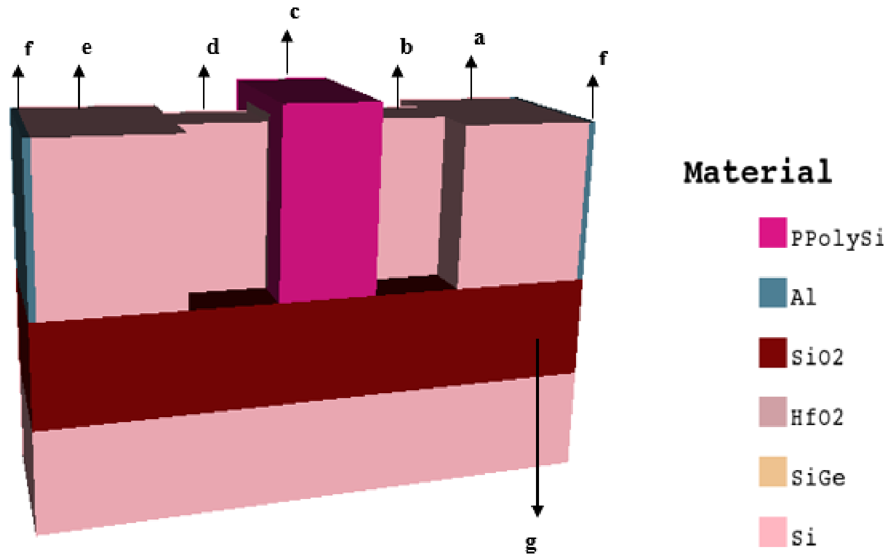


Fig 3.3 14-nm Heterojunction N-FinFET

In the above device, we mainly focus on designing a FinFET structure that can show good performance in terms of reduction in short-channel effects and improved on current/off current ratio in comparison with the existing structure for smaller gate length. For the proposed design, hafnium oxide (HFO_2) is used as an oxide material and has a higher value of dielectric and polysilicon material (Φ_m =4.25 eV) for a gate. As aluminum material (Φ_m =4.1 eV) used for making the contact of a substrate, source, and drain. In the same design, we covered the fin from three sides (top, right side, and left side) with oxide material then by gate material and work function value set at 4.17eV.

For designing the P-FinFET, we used the same dimension structure as used for the N-FinFET. Table 3.2 and figure 3.4 show the dimension and 3D view of the 14-nm Heterojunction P-FinFET. In the same design, we change the gate material with Npoly Silicon and the doping level of the source, drain, and channel region. Variation in the work function value in P-FinFET was done to match the features of both the devices P-FinFET and N-FinFET.

For both devices, a rectangular-shaped fin was used that was covered by the three sides of the oxide layer of HFO_2 and then further covered by the gate material. This leads to control the short effect in the device and figure 3.5 represents the analytic expression of high-k dielectric with high work function for the same.

Table 3.2: Dimension of the Device Region of 14-nm Heterojunction P-FinFET

Region of device	Material	Region Length	Region Width	Region Height	Doping Level
Extended Source -1 (a)	Silicon-Germanium ($Si_{1-x}Ge_x$)	13nm	10nm	20nm	$1x10^{20}/cm^3$
Extended Source-2 (b)	Silicon	20nm	24nm	20nm	$1x10^{20}/cm^3$
Extended Drain-1 (e)	Silicon	13nm	10nm	20nm	$1x10^{18}/cm^3$
Extended Drain-2 (d)	Silicon	20nm	24nm	20nm	$1x10^{18}/cm^3$
Fin (Channel)	Silicon	14nm	10nm	20nm	$1x10^{17}/cm^3$
Gate (c)	NPolySi	14nm	2nm	23nm	-
Oxide	HFO_2	14nm	2nm	21nm	-
Source & Drain Contact (f0	Aluminum	20nm	1nm	20nm	-

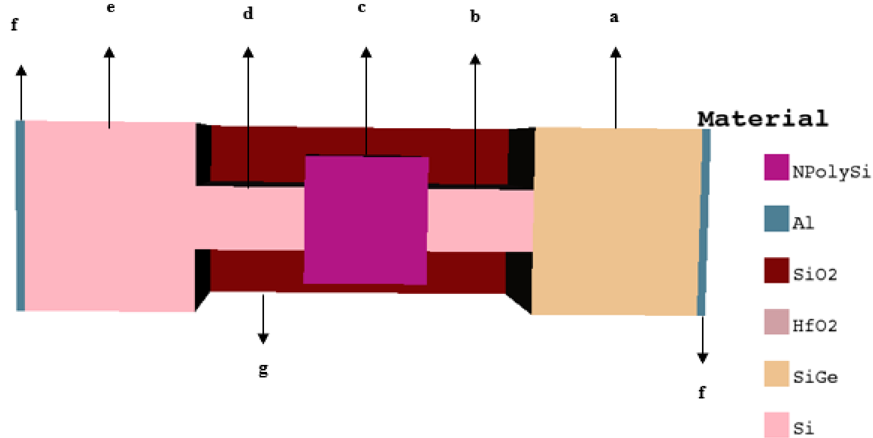


Fig 3.4 14-nm Heterojunction P-FinFET

In both designs, Heterojunction was created between the fin and extended source-2 by using the two different materials silicon and Silicon-Germanium (Si_{1-x} Ge_x).

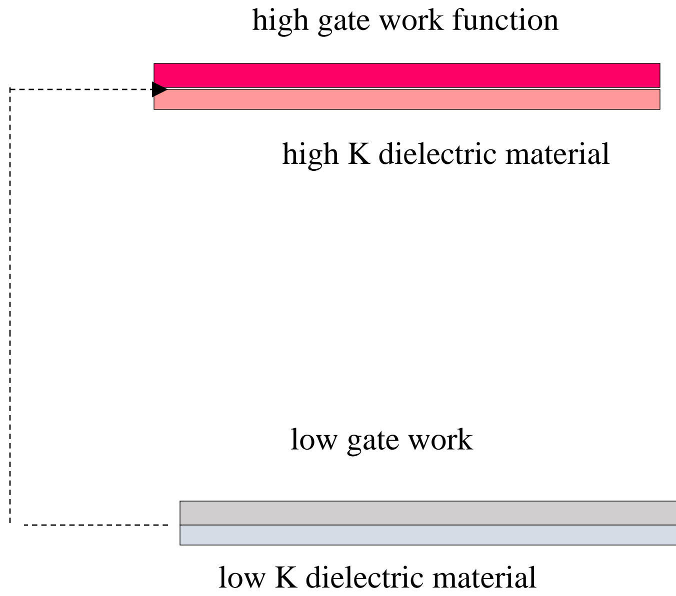


Fig 3.5 Analytic description of 14-nm Heterojunction N-FinFET

Table 3.3: Dimension of Compared Devices

Parameter of the Device	**Channel Length (L_g) (nm)**	**Fin Width (W_{fin}) (nm)**	**Height of Fin (H_{fin}) (nm)**	**Gate Oxide thickness (T_{ox}) (nm)**
Proposed 14-nm Heterojunction FinFET	14	10	20	2
Conventional FinFET [78]	14	10	20	2
Source Step-FinFET [77]	40	14	40	1.5
FinFET-1 [79]	20	15	25	1
FinFET-2 [79]	5	1	8	1

The dimensions of various parameters for the standard FinFET, Source Step-FinFET, and the proposed 14-nm Heterojunction FinFET are listed in Table 3.3.

3.3 PHYSICAL SIMULATION OF PROPOSED FINFET

The Cogenda tool and the Lombard equation for device modeling [80] were used to generate all of the results and simulations. The doping-dependent mobility model was also utilized to investigate the impact of carrier mobility in the 14nm Heterojunction N-FinFET. The drift-diffusion model and Boltzmann statistics were utilized in this simulation [81]. The recombination rate is calculated using the sum of direct recombination and Shockley read hall recombination. While simulating the proposed design, Boltzmann statistics and the drift-diffusion model were used. The recombination rate is calculated by adding the results of Shockley read hall recombination and direct combination. Drift-diffusion equations, high field mobility dependency, doping dependent mobility degradations, Lombardi as a mobility model, and high field mobility dependency were all enabled during the simulation of the proposed device. We used a global command on the device to set the external temperature to 300K. Electron and hole concentrations were introduced to the simulation as shown in equations 3.1 [82].

$$\nabla_n = -((h^2\gamma n)/(6qm_n^*)) * ((\nabla^2 \sqrt{n})/(\sqrt{n})) \quad (3.1)$$

$$\nabla_p = -((h^2\gamma n)/(6qm_p^*)) * ((\nabla^2 \sqrt{p})/(\sqrt{p})) \quad (3.2)$$

Where p and n indicate electron concentration, hole concentration, and valance band in the conduction band, h and q represent Planck's constant and electron charge, while mn* and mp* represent hole and electron effective mass.

The relationship between the temperature and energy bandgap can be represented by equation 3 [83-84].

$$E_g(T) = E_g(0) - \alpha ET^2/(T + \beta_E) \quad (3.3)$$

Where, α for Si = 5.41×10-4 eV/K and Eg = 1.42 eV, β_E = 206 K

The term electrical width of FinFET is defined as

$$\mathrm{W} = 2\mathrm{H_{fin}} + \mathrm{T_{fin}} \quad (3.4)$$

Where H_{fin} represents fin-height and T_{fin} represents the fin-thickness.

Following the model was used while simulating the device.

a) Auger-Auger recombination has a three-particle transition in which the mobile carrier is either released or trapped. When an electron recombines, energy is transferred to the conduction band's third electron, which thermalizes near the conduction band's edge. Auger recombination was modeled using the following expression (3.5) [85].

$$R_{Auger} = C_n n(np - n_{ie}^2) + C_p p(np - n_{ie}^2) \quad (3.5)$$

Where p, n represent the concentration of hole and electron respectively and n_{ie} is intrinsic concentration, C_p, C_n are constant. In the proposed design we used the standard model of auger recombination for both devices.

b) Shockley Recombination (SRH) - Recombination through defects is also known as Shockley Recombination. It's a two-part procedure.
   1) An electron or hole is caught by an energy level present in a forbidden gap due to crystal defects.
   2) The SRH recombination rate [86] happens when the hole reaches the same energy level as the electron before being thermally heated to the conduction band.

$$R_{SRH} = \frac{n_p - n_{ie}^2}{\tau_p(n + n_{ie}\, e^{(+ETRP/kT_L)}) + \tau_n(p + n_{ie}\, e^{(-ETRP/kT_L)})} \quad (3.6)$$

   p and n are the electron and hole life cycles, n and p are the electron and hole concentrations, n_{ie} is the effective intrinsic concentration, and TL is the lattice temperature. ETRAP stands for the difference between the trap energy level and the intrinsic fermi level. The concentration-dependent SRH lifetime model calculates carrier lifetime as a function of impurity concentration.

c) Model of Lombardi mobility - The Lombardi models used in this work are a hybrid model that considers both low field and transverse field influences on mobility. The

effects of doping, temperature, and the inversion layer are also taken into account [86]. The mobilities of electrons and holes are represented as

$$\frac{1}{\mu} = \frac{1}{\mu_i} + \frac{1}{\mu_s} + \frac{1}{\mu_p} \qquad (3.7)$$

Carrier Mobility (μ) depend on the phonon scattering (μ_p), surface roughness scattering (μ_s) and ionized impurity scattering (μ_i). Equation 3.7 shows the mathematic formula of carrier mobility (μ).

3.4 TRANSFER CHARACTERISTICS OF 14-nm HETEROJUNCTION N-FINFET.

Different performance parameters of the device were analyzed for the 14-nm Heterojunction N-FinFET.

a) Drain current of the device calculated as per equation 3.8

$$I_d = \emptyset + \mu C_{ox} \left(\frac{W_g}{L_g}\right)\left(\frac{(V_{gs}-V_{th})}{2m}\right) \qquad (3.8)$$

Where Ø is work function of gate material, I_d is drain current, threshold voltage (V_{th}), W_g is gate width and L_g is gate length, μ is the mobility, gate to source voltage (V_{gs}) and C_{ox} is oxide capacitance of gate, T_{ox} is oxide thickness of gate and W_{si} is fin thickness.

$$m = 1 + \frac{3T_{ox}}{W_{si}} \qquad (3.9)$$

b) Sub-threshold Swing as per equation 3.10, it defined as the change in gate to source voltage with respect to change in the drain current for per decade.

$$\mathrm{SS} = {\partial \mathrm{V_g}}/{\partial \log_{10} \mathrm{I_d}} \qquad (3.10)$$

c) Drain Induced Barrier Lowering (DIBL) is a method used to determine the reduction in threshold voltage when the gate to source voltage is increased. Equation 3.11 will be used to compute this value in the proposed design.

$$\text{DIBL} = \frac{\Delta V_{th}}{\Delta V_d} \quad (3.11)$$

d) Transconductance - Transconductance is an important metric in FinFETs because it describes how current changes in response to changes in gate voltage. Equation 3.2 shown the mathematical expression of transconductance.

$$g_m = \frac{\partial I_d}{\partial V_{GS}} \quad (3.12)$$

Where V_{GS} is gate to source voltage and I_d is drain current of the device.

Figure 3.6 shows the comparison of transfer characteristics of the proposed design -1 and proposed design- 2 with conventional FinFET. In both the design we used the mole fraction value of 0.3.

a) Proposed-1 14nm Heterojunction FinFET – In this design, Heterojunction created between the drain-1 and source-1 by using the two different semiconductor material like Silicon Germanium (Si_{1-x} Ge_x) and Silicon. The doping level kept at 10^{20} /cm^{-3} for the fin region and for source and drain region at 10^{18} /cm^{-3} , 10^{20} /cm^{-3}, separately.

b) Proposed-2 14nm Heterojunction FinFET – In this design, Heterojunction created between the drain-1 and source-1 by using the two different material like Silicon Germanium (Si_{1-x} Ge_x) and Silicon. The doping level kept at 10^{18} /cm^{-3} for the fin region and for source and drain region at 10^{18} /cm^{-3} , 10^{20} /cm^{-3} separately.

So, proposed- 2 is the improvement version of the proposed-1. In proposed-2, Off current, current ratio, subthreshold swing value and DIBL have better value in comparison with conventional FinFET [78], Source Step FinFET [77] and FinFET [79] as per figure 3.6 and table 3.4 & 3.5.

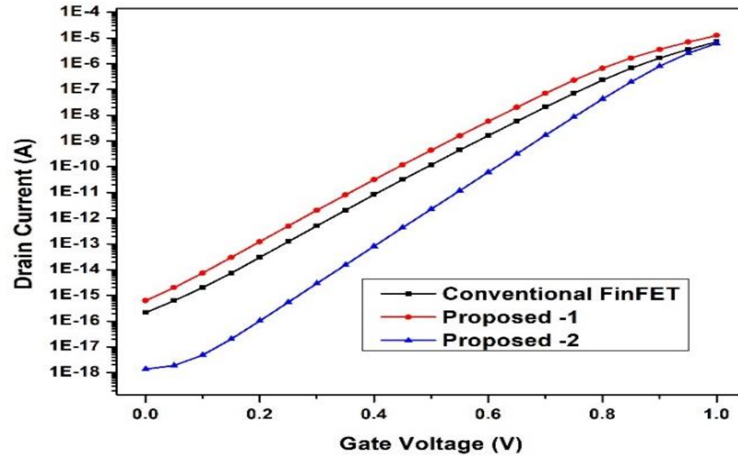


Fig 3.6 Transfer Characteristics of Compared Devices.

Table 3.4: Comparison of Performance Parameter

Performance Parameters	**Conventional FinFET [78]**	**Proposed-1 14nm heterojunction FinFET**	**Proposed-2 14nm heterojunction FinFET**	**Source Step-FinFET [77]**	**FinFET-20nm [79]**	**FinFET-5nm [79]**
On Current I_{on} (A)	7.06×10^{-06}	1.26×10^{-05}	6.21×10^{-06}	$\sim10^{-3}$	1.00×10^{-03}	1.70×10^{-03}
Off Current I_{Off} (A)	2.15×10^{-16}	6.27×10^{-16}	1.38×10^{-18}	$\sim10^{-11}$	6.67×10^{-11}	6.45×10^{-11}
Current Ratio I_{On}/I_{Off}	3.29×10^{10}	2.01×10^{10}	4.51×10^{12}	$3.11\text{x}10^{8}$	15.00×10^{06}	15.50×10^{06}
SS (mV/dec)	64.21	67.96	58.56	64.77	86	60
DIBL (mV/V)	54.32	68.45	52.37	35.31	55	80

Table 3.5: Comparison of Drain Current Vs Gate voltage for Different FinFET

Gate voltage (V)	Drain Current (A)		
	Conventional FinFET [78]	**Proposed-1 14nm Heterojunction FinFET**	**Proposed-2 14nm Heterojunction FinFET**
0.0	$2.15x10^{-16}$	$6.27x10^{-16}$	$1.38x10^{-18}$
0.05	$6.25x10^{-16}$	$2.03x10^{-15}$	$1.89x10^{-18}$
0.1	$2.02x10^{-15}$	$7.44x10^{-15}$	$4.80x10^{-18}$
0.15	$7.44x10^{-15}$	$3.01x10^{-14}$	$2.05x10^{-17}$
0.2	$3.02x10^{-14}$	$1.23x10^{-13}$	$1.04x10^{-16}$
0.25	$1.24x10^{-13}$	$5.02x10^{-13}$	$5.50x10^{-16}$
0.3	$5.04x10^{-13}$	$2.03x10^{-12}$	$2.92x10^{-15}$
0.35	$2.04x10^{-12}$	$8.08x10^{-12}$	$1.54x10^{-14}$
0.4	$8.11x10^{-12}$	$3.14x10^{-11}$	$8.13x10^{-14}$
0.45	$3.15x10^{-11}$	$1.19x10^{-10}$	$4.27x10^{-13}$
0.5	$1.19x10^{-10}$	$4.39x10^{-10}$	$2.24x10^{-12}$
0.55	$4.42x10^{-10}$	$1.60x10^{-09}$	$1.17x10^{-11}$
0.6	$1.61x10^{-09}$	$5.74x10^{-09}$	$6.13x10^{-11}$
0.65	$5.78x10^{-09}$	$2.04x10^{-08}$	$3.20x10^{-10}$
0.7	$2.05x10^{-08}$	$7.06x10^{-08}$	$1.66x10^{-09}$
0.75	$7.09x10^{-08}$	$2.31x10^{-07}$	$8.53x10^{-09}$
0.8	$2.32x10^{-07}$	$6.72x10^{-07}$	$4.26x10^{-08}$
0.85	$6.74x10^{-07}$	$1.67x10^{-07}$	$1.99x10^{-07}$
0.9	$1.68x10^{-06}$	$3.60x10^{-06}$	$8.07x10^{-07}$
0.95	$3.6x10^{-06}$	$6.97x10^{-06}$	$2.57x10^{-06}$
1.0	$7.06x10^{-06}$	$1.26x10^{-05}$	$6.21x10^{-06}$

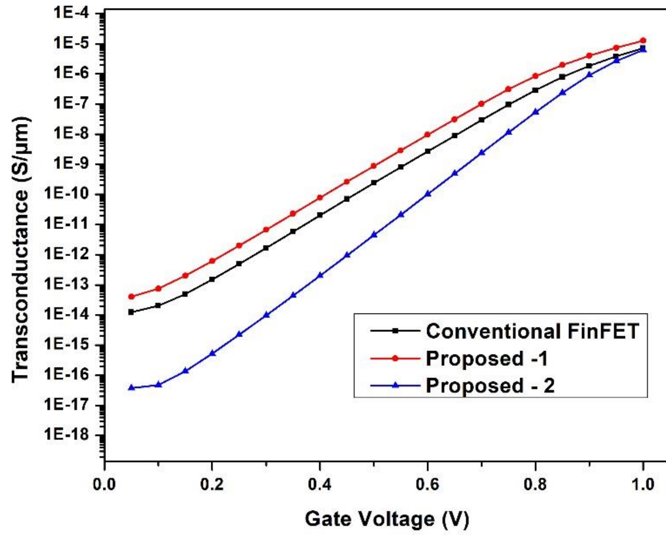


Fig 3.7 Transconductance of Compared Devices.

Figure 3.7, shown the comparative analysis of the proposed design-1 & 2 with conventional FinFET in relation with transconductance vs Gate Voltage.

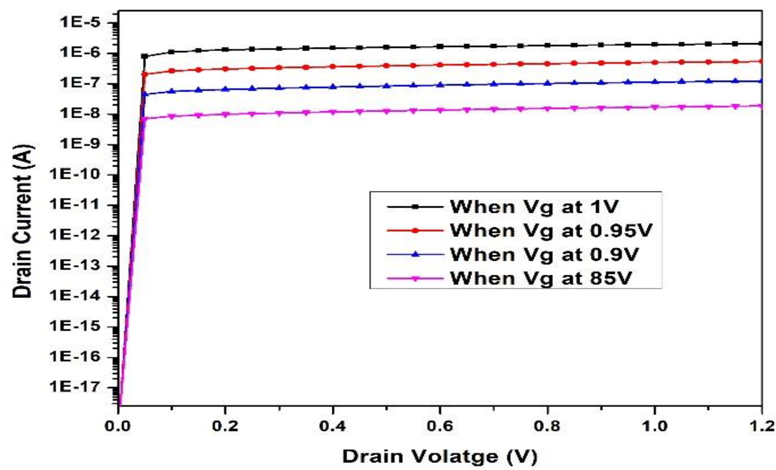


Fig 3.8 Output characteristics of Proposed -2 14nm Heterojunction FinFET.

Output characteristics of Proposed – 2 14nm Heterojunction FinFET mentioned in fig 3.8 on different value of the gate to source voltage (1V, 0.95V, 0.9V and 0.85V respectively).

As per table 3.4, proposed 14-nm Heterojunction shown the good result in terms of I_{off}, ratio of I_{on}/I_{Off}, with minimum value of subthreshold swing and DIBL in comparison with conventional FinFET and Source Step FinFET. So, in next section 3.5 shown the various analysis on performance parameter of the proposed-2 14nm Heterojunction FinFET.

3.5 PROCESS VARIATION ON PERFORMANCE PARAMETER OF PROPOSED 14-nm HETEROJUNCTION FinFET.

In this section, we discussed the process variation impact on the performance parameter of proposed 14-nm Heterojunction FinFET. As process variation is very important analysis for any device to see the post impact on device performance.

1) Impact of Different Fin Material- For minimizing the short channel effect in the device, different material investigates for the fin region [87]. As we change the fin material from silicon to silicon germanium, it shows the minimum short channel effect by minimizing the off current and increasing the current ratio as per figure 3.9. Fin of silicon germanium gives the better thermal conductivity (0.0712 W-cm-1K -1) as compared to the silicon or germanium material [88]. Although germanium has superior electron and hole mobility than silicon, due to alloy scattering, SiGe with a low germanium mole fraction (30%) has poorer mobility than silicon. By raising the mole fraction value in SiGe, the effective mass of SiGe decreases, resulting in improved mobility. Due to a narrower bandgap in germanium, the mobility of the channel is reduced, resulting in an increase in junction leakage current, which reduces the device's performance when compared to the other two fin materials. The relationship between drain current and gate voltage for various fin materials is shown in Table 3.6 and Figure 3.9. Because silicon mobility is lower than that of germanium, when silicon is used as a fin material, the on current is low, but the off current is higher due to the high mobility of germanium material. The thermal stability of Ge-based fins is less implemented than that of silicon due to the higher peak inverse voltage. As shown in figure 3.9 and table 3.6, the Si-Ge based

fin structure outperforms germanium and silicon, making the suggested device more suited in terms of heat conductivity and mobility.

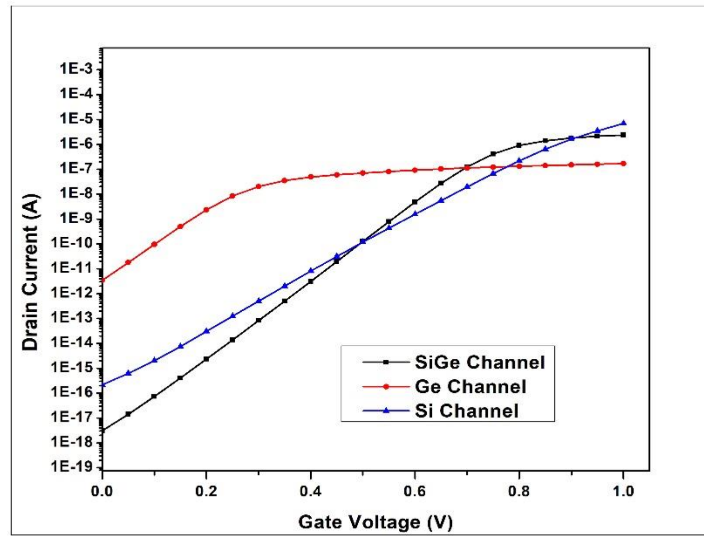


Fig 3.9 Drain Current Vs gate voltage on different fin material

Table 3.6: Comparison of transfer characteristics on different fin material.

V_g (V)	I_d (A)		
	Fin of Ge material	**Fin of $Si_{1-x}Ge_x$ material**	**Fin of Si material**
0	$3.41*10^{-12}$	$3.11*10^{-18}$	$2.15*10^{-16}$
0.05	$1.78*10^{-11}$	$1.40*10^{-17}$	$6.26*10^{-16}$
0.1	$9.46*10^{-11}$	$7.23*10^{-17}$	$2.02*10^{-15}$
0.15	$4.94*10^{-10}$	$4.05*10^{-16}$	$7.44*10^{-15}$
0.2	$2.48*10^{-10}$	$2.35*10^{-15}$	$3.02*10^{-14}$
0.25	$3.25*10^{-10}$	$1.38*10^{-14}$	$1.23*10^{-13}$
0.3	$2.01*10^{-09}$	$8.29*10^{-14}$	$5.01*10^{-13}$
0.35	$3.51*10^{-08}$	$4.99*10^{-13}$	$2.02*10^{-12}$

0.4	$4.90*10^{-08}$	$3.07*10^{-12}$	$8.01*10^{-12}$
0.45	$6.00*10^{-08}$	$1.94*10^{-11}$	$3.10*10^{-11}$
0.5	$6.98*10^{-08}$	$1.24*10^{-10}$	$1.16*10^{-10}$
0.55	$8.04*10^{-08}$	$7.88*10^{-10}$	$4.28*10^{-10}$
0.6	$9.21*10^{-08}$	$4.82*10^{-09}$	$1.55*10^{-09}$
0.65	$1.03*10^{-07}$	$2.72*10^{-08}$	$5.52*10^{-09}$
0.7	$1.13*10^{-07}$	$1.26*10^{-07}$	$1.94*10^{-08}$
0.75	$1.22*10^{-07}$	$4.1*10^{-07}$	$6.68*10^{-08}$
0.8	$1.31*10^{-07}$	$8.99*10^{-07}$	$2.19*10^{-07}$
0.85	$1.41*10^{-07}$	$1.41*10^{-06}$	$6.41*10^{-07}$
0.9	$1.50*10^{-07}$	$1.81*10^{-06}$	$1.61*10^{-06}$
0.95	$1.60*10^{-07}$	$2.12*10^{-06}$	$3.51*10^{-06}$
1	$1.69*10^{-07}$	$2.36*10^{-06}$	$6.91*10^{-06}$

2) Impact of Mole Fraction – As per the figure 3.11, impact of mole fraction on the proposed design is very less when it varies from 0.1 to 0.3. It mostly affects the Ioff current, which increases as the mole percentage is reduced from 0.3 to 0.1 due to a decrease in the threshold voltage. To apply biaxial strain to the channel, strain Si is grown on relaxed SiGe or relaxed SiGe generated on a Silicon Substrate in the conventional method [89]. In the recommended design, the Si source creates uniaxial strain in the channel, which increases strain due to a mismatch in the Si to SiGe lattice. As a result, the carrier's mobility inside the channel improves. The impact of strain on SiGe and Si is seen in Figure 3.10. The impact of strain on SiGe and Si is seen in Figure 3.10. Figure 3.10 shows that strain increases the electron affinity of the Silicon source, and unstrained Silicon has a higher conduction band energy than strained Silicon, lowering the bandgap.

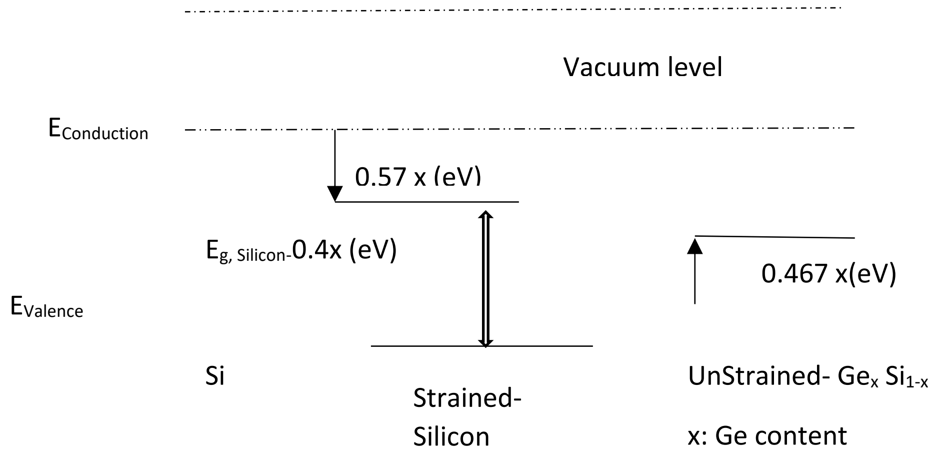


Figure 3.10 Impact of strain on band structure of Silicon-Germanium ($Si_{1-x}Ge_x$) and Silicon (Si) [78]

The energy of the valence band on the SiGe layer, on the other hand, increases as the germanium content in Si_{1-x} Ge_x increases. As a result of the strain, the effective mass of the carrier is reduced, resulting in a fall in the density of the state of holes in the valence band. Based on available studies, the effect of strain on Si is represented in equation 3.13.

$$(\Delta E_C)_{s-Si} = 0.57x \tag{3.13}$$

$$(\Delta E_g)_{s-Si} = 0.4x \tag{3.14}$$

$$V_T \ln\left({N_{V,Si}}/{N_{V,s-Si}}\right) = V_T \ln\left({m^*_{hole,Si}}/{m^*_{hole,s-Si}}\right) \cong 0.075x \tag{3.15}$$

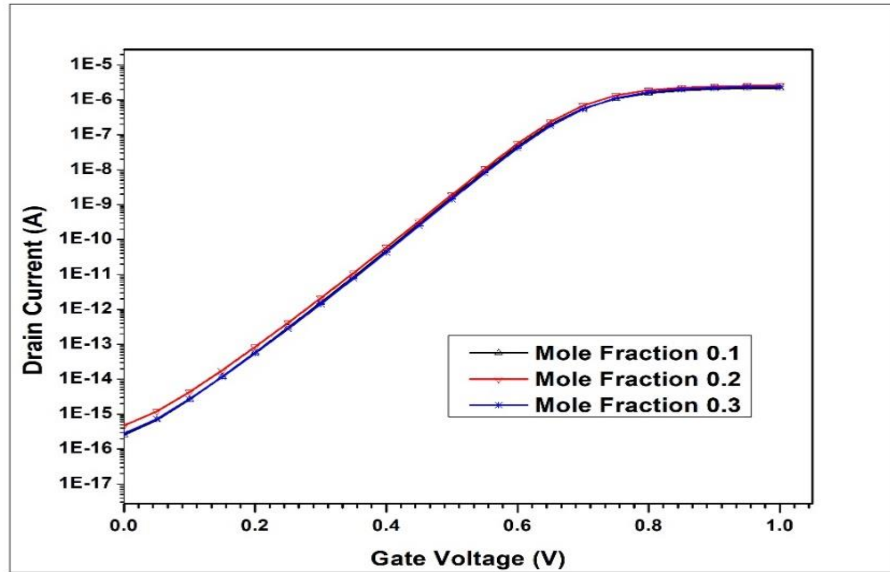


Fig 3.11 Impact of Mole fraction on Proposed -2 14nm Heterojunction FinFET.

x denotes the variation in germanium content in Si_{1-x} Ge_x, $(\Delta E_g)_{s-Si}$ and $(\Delta E_C)_{s-Si}$ is represent the decrease in conduction band due to the strain that further reduces the electron affinity. State density of valence band for the strained silicon and unstrained silicon represented by the $N_{V,s-Si}$ and $N_{V,s-Si}$. Thermal voltage of the device denoted by V_T and effective mass of hole charge carrier for strained silicon and unstrained silicon, respectively. $m^*_{hole,Si}$ and $m^*_{hole,s-Si}$. Figure 3.11 shows that as the mole percentage in Si_{1-x} Ge_x grows from 0.1 to 0.3, in both the region saturation and linear region drain current values get increases. The electron affinity reduces, resulting in a drop in the bandgap and a rise in carrier mobility due to the strain impact from SiGe to Si.

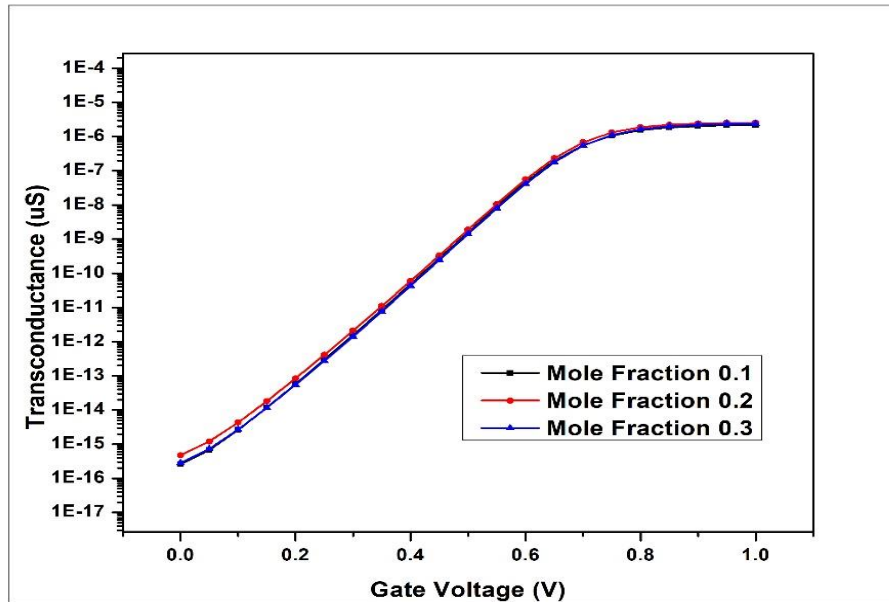


Fig 3.12 Transconductance vs Mole fraction

The effect of changing the mole fraction value in Si_{1-x} Ge_x from 0.1 to 0.3 on the transconductance of the proposed design is shown in figure 3.12. This factor describes how the current changes when the gate voltage changes, and it's a crucial circuit design metric. This factor, g_m/I_d, is a direct measure of the FinFETs efficiency because it shows the device's amplification per unit energy required to make the drain current. The greater the FinFETs ability to act as a power-saving technology, the higher this number [90]. The peak value of g_m increases as the mole fraction increases, which is linked to an increase in the carrier's mobility.

3. Impact of Oxide thickness: As per the figure 3.13, impact of the oxide thickness variation from 2nm to 4nm shown on the transfer characteristics of the device. As oxide thickness (t_{ox}) varies from 2 nm to 4nm, it decreases the value of drain current due to increase in the oxide capacitance of the gate terminal. According to equation 3.8, the value of m is directly proportional to the oxide thickness, while the oxide capacitance is inversely proportional. The oxide capacitance and value of m drop as the oxide thickness increases, lowering the drain current of the device. Furthermore, variations in oxide thickness have an impact on

the device's threshold voltage, which increases as the oxide thickness grows from 2nm to 3nm, as seen in figure 3.13, resulting in a drop in the device's off current.

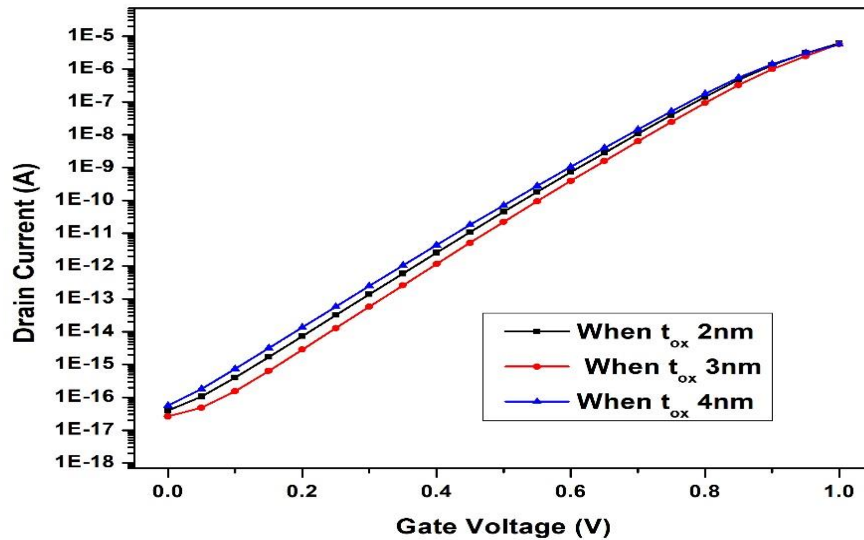


Fig 3.13 Variation in oxide thickness when drain voltage at 1V.

Figure 3.14 shown the impact of oxide thickness on the drain current when V_{ds} at 0.1 V. In this case, maximum impact shown on the threshold voltage that increases the off current (I_{off}) as oxide thickness varies from 2 nm to 4nm.

4 Impact of temperature variation: figure 3.15 & 3.16 shows the impact of the temperature variation from 200K to 350K on the proposed design.

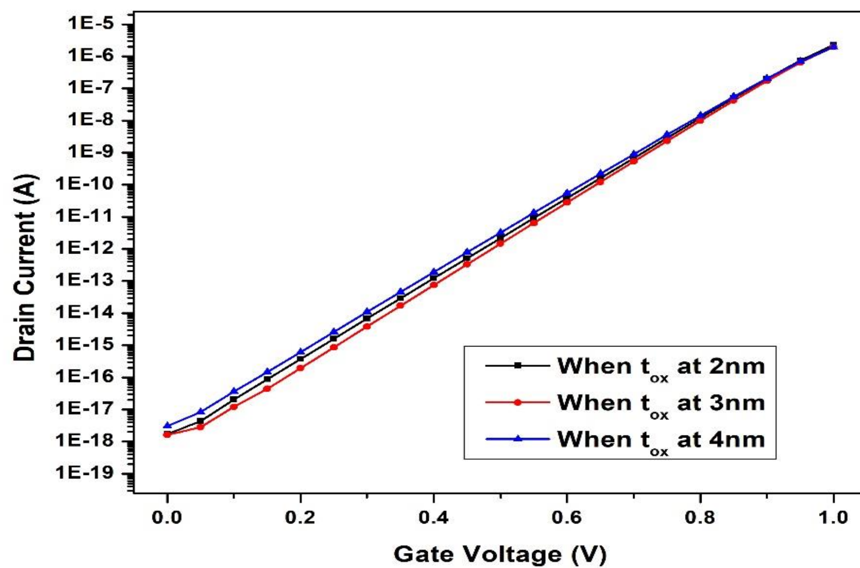


Fig 3.14 Variation in oxide thickness when drain voltage at 0.1V.

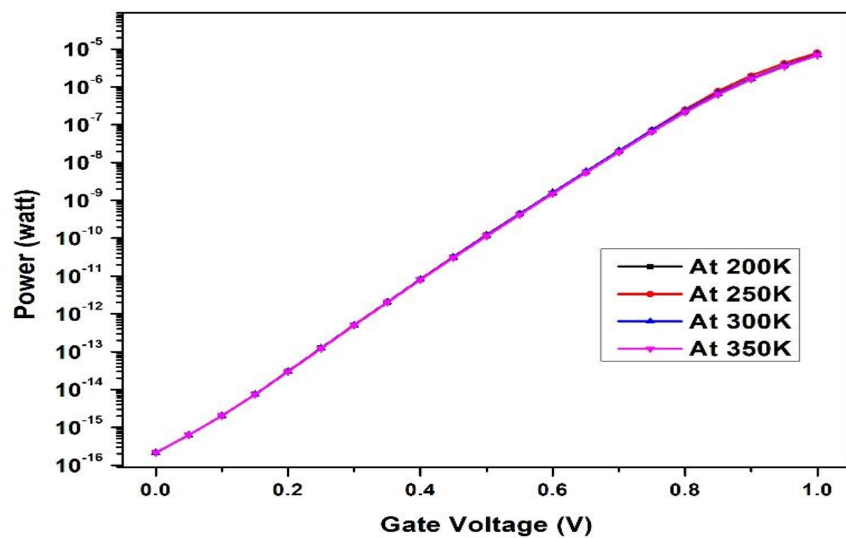


Fig 3.15 Impact of temperature variation on power of Proposed -2 14nm Heterojunction FinFET.

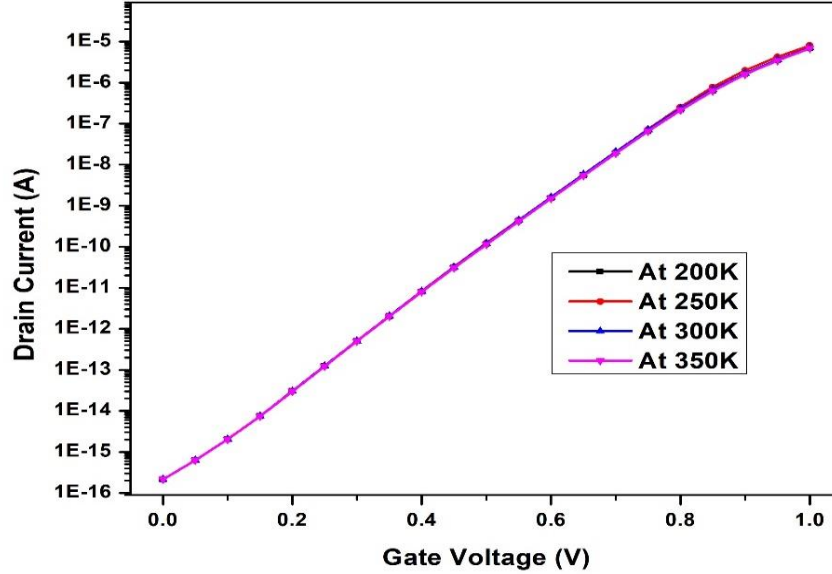


Fig 3.16 Variation of temperature vs drain current.

$$V_{th} = \text{Ø} + \left(\frac{KT}{q}\right) \ln\left(\frac{2\, C_{OX} KT}{q^2 n_i t_{SI}}\right) + \left(\frac{h^2 \pi^2}{2 m_{ds} w_{si}^2}\right) \qquad (3.16)$$

Where K is Boltzmann's constant, n_i is intrinsic Si concentration, t_{si} is fin thickness $_h$ is Planck's constant, q is charge of electron, W_{si} denoted a fin width, V_{th} is threshold voltage, T is temperature (K).

$$\mathrm{N_i} = 5.2 * 10^{15} * \mathrm{T}_{\frac{3}{2}} * \; \mathrm{e}^{(\frac{-\mathrm{Eg}}{2\mathrm{kT}})} \qquad (3.17)$$

The energy gap and temperature can be expressed as shown in equation 3.17, where Eg represents the energy gap.

With increase in the charge carrier due to rise in the temperature will reduces the bandgap between the fermi level and conduction band [91]. Phonon scattering more dominated when the temperature rises due to this mobility of the device get decreases due to increase in the charge carrier. But in the proposed design, less impact of temperature observed from the figure 3.16 and 3.15.

3.6 FABRICATION STEP FOR 14-nm HETROJUNCTION FINFETS

First step for designing the FinFET, we need to take substrate box and need to perform a hard masking. By Using the Self-Aligned Quadruple double patterning technique for creating the fins and this process known as lithography. With the help of silicon nitride or silicon dioxide and patterned resist layer, hardmask created on the substrate as shown in figure 3.17 in step a and step b. In this process mandrels created on the substrate then after with help of the spacers cover around the mandrels as shown in figure 3.17 in step c. Etch back layer used to create a spacer on the mandrels. In step d, fin patterning will do by removing the sacrificial layer and etched the silicon layer to form the fins on the substrate. To isolate the fins with each other than oxidation process is used as shown in figure 3.17 in step e. After this, planarization process will occur on the deposit oxide material by using the chemical polishing and here hard mask acts a stop layer. Another etch process is required to recess the oxide film for making an isolation on the fins. With the help of the thermal oxidation, oxide layer form on the top of the fins to isolate the channel from the gate electrode. As shown in figure 3.17 in step f, polysilicon layer is deposited on the top of the fins and forms a gate on three side that wrap the channel from all three directions. This process will be done by low pressure chemical vapor deposition. In the last step stressors apply on the channel for improving the mobility. For creating the extended source and drain region, epitaxial process used on the fins area. In this step different material can used for creating a hetrojunction by using two different material.

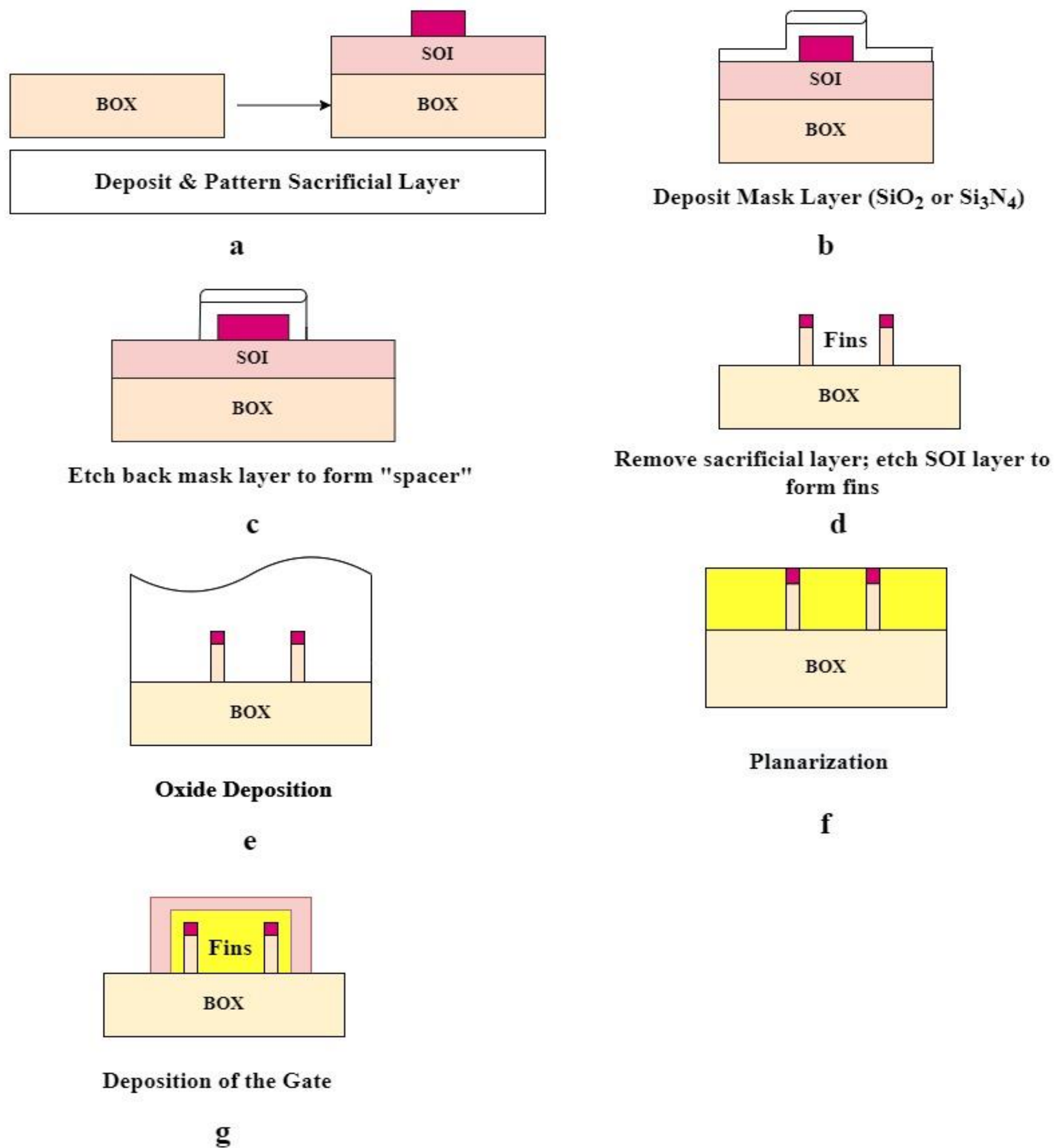


Fig 3.17 Fabrications Step for FinFET.

3.7 SUMMARY.

A new heterojunction rectangular shaped N-FinFETs has been proposed and its comparative analysis is performed with other FinFET at 14nm ,20nm and 5nm technology

node on different performance parameter. This paper the proposed heterojunction rectangular N-FinFET shows a higher On-current (6.21×10^{-6} A), higher I_{on}/I_{off} current ratio (4.51×10^{12}) with minimum Off-current, DIBL and SS values of 1.38×10^{-18} A, 52.37 mV/V) and 58.56 mV/Dec respectively as compared to the FinFET. Process variation performed on the proposed heterojunction N-FinFET on different parameters like work function, mole fraction (x) in Silicon Germanium ($Si_{1-x} Ge_x$) material and temperature.

Chapter 4

Impact of Fin shape on Heterojunction FinFET

4.1 INTRODUCTION

The main objective of this chapter is to study and describe the different shape of fin for Heterojunction FinFET and its comparison with different shape of FinFET. As discussed in chapter 2, different shaped have been employed by the researchers to achieve the FinFET for lower application. However, the initial step of all the mentioned designs is to achieve the minimize short channel effect for designing of high-performance device for VLSI circuit.

Many characteristics in FinFETs, including as height, doping profile, fin shape, and fin thickness, are important in determining device performance and behavior [92]. The rectangular fin form in FinFETs devices has been investigated in a number of academic papers, as well as mathematical modelling and simulations. Even on a commercial scale, Intel removes the scanning electron microscopy (SEM) image of FinFETs fins in rectangular shapes where transistors have inclined or sloped sidewalls [92]. At a later stage, many researchers assessed the performance of trapezoidal-shaped FinFETs. SCEs are influenced by the fin inclination angle, which leads to the narrow fin that controls current via the gate in the center region of the fin [93].

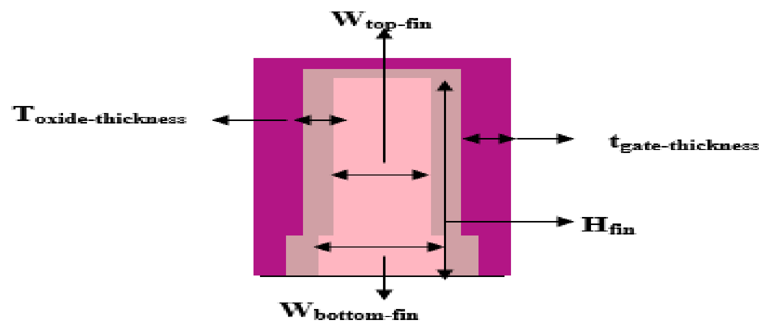
On insulator FinFETs, the width of the fin base grows as the fin shape changes from rectangular to triangular to trapezoidal, causing a rise in leakage current [94]. Work function modifications in tapered fins increased subthreshold characteristics while lowering on-state current when compared to rectangular fins [95]. Because the fin width and work function influence the leakage current, the on/off current ratio in triangular fin-shaped devices improves when compared to rectangular FinFETs. With the right selection of top fin width and fin height in tapered shaped based fins, such transistors can perform well on below 5nm technology nodes [96]. Fin geometries including convex, concave, rectangular, and trapezoidal were studied in 10-nm FinFETs for digital and analogue

properties [97]. FinFETs are being used by a growing number of companies, including Taiwan Semiconductor Manufacturing Company (TMSC), AMD, and IBM, to create their latest microprocessors [98-100].

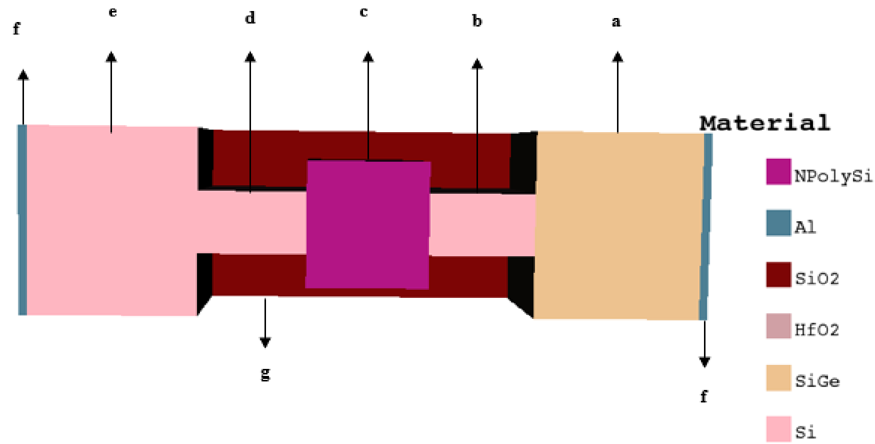
This chapter develops a new inverted-T FinFETs structure that outperforms the present structure in terms of reducing short channel impact for shorter channel and gate lengths. The supplied FinFET structure has a rectangular shape due to the fact that the upper half of the fin is thinner than the lower half, resulting in an inverted-T shape fin. The inverted-T FinFET offers greater controllability over the drain current than rectangular and rectzoidal layouts. There are four sections in this chapter. The numerous shapes of FinFETs fins are represented in Section I. Sections II and III illustrate comparisons of the proposed design with various fin-shaped based FinFETs, as well as process variations on the proposed design.

4.2 STRUCTURE DESIGN PARAMETER AND MATERIAL COMPOSITION.

Figure 4.1 an illustrates a sectional view of the 14-nm heterojunction's inverted t-shaped fin, whereas figure 4.1 b depicts a three-dimensional perspective of the inverted t-shaped fin. A rectzoidal FinFET [33] is shown in cross-section in Figure 4.2.



(a)



(b)

Fig. 4.1 **(a)** 14-nm heterojunction inverted-T P-FinFET **(b)** Three-dimensional of 14-nm heterojunction inverted-T P-FinFET.

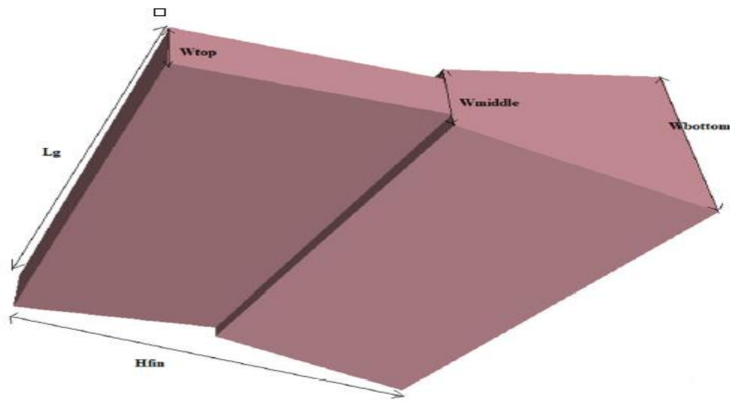


Fig. 4.2 Rectzoidal-fin shaped FinFET [33].

Table 4.2 shows the different dimension of the inverted T shaped fin, rectzoidal shaped based fin and rectangular shaped based fin of FinFET. In the proposed design we have designed an inverted T shaped fin for proposed FinFET and Heterojunction created by using the two different semiconductor material. In the proposed designed, Heterojunction terminal created in between the channel and source region by using the silicon and silicon germanium ($Si_{1-x}Ge_x$) material. A heterojunction region was produced between the source

and channel in the proposed-1 device using silicon germanium ($Si_{1-x}Ge_x$) material, whereas a heterojunction region was created between the source and drain region in the proposed-2 device utilizing silicon germanium as the channel material ($Si_{1-x}Ge_x$). In both designs, the mole fraction value was kept at 0.3. (proposed-1, proposed-2).

Table 4.1: Dimension of proposed -1 & 2 Heterojunction N-FinFET

Region of device	**Material**	**Region Length**	**Region Width**	**Region Height**	**Doping Level**
Extended Source -1 (a)	Silicon Germanium ($Si_{1-x}Ge_x$)	13nm	10nm	20nm	$1x10^{20}$ /cm^3
Extended Source-2 (b)	Silicon	20nm	24nm	20nm	$1x10^{20}$ /cm^3
Extended Drain-1 (d)	Silicon	13nm	10nm	20nm	$1x10^{18}$ /cm^3
Extended Drain-2 (e)	Silicon	20nm	24nm	20nm	$1x10^{18}$ /cm^3
Fin (Channel)	Silicon	14nm	10nm	20nm	$1x10^{18}$ /cm^3
Gate (c)	PPolySi	14nm	2nm	23nm	-
Oxide	HFO_2	14nm	2nm	21nm	-
Contact Of source & drain (f)	Aluminum	20nm	1nm	20nm	-

Table 4.2: Dimension of the Compared Devices

Compared Parameter	**Inverted T shaped (nm)**	**Rectzoidal Shaped Fin [33] (nm)**	**Rectangular shaped Fin [78] (nm)**
$T_{oxide-thickness}$	1	1	1
H_{fin}	20	30	20
W_{fin} ($W_{top-fin}$ / $W_{bottom-fin}$)	4/8	10	10
L_g	14	20	14

In the same way as proposed-1, the heterojunction area is made of rectangular-shaped Si-fin. On insulator FinFETs, the width of the fin base grows as the fin shape changes from rectangular to triangular to trapezoidal, causing a rise in leakage current [101]. As a result, the proposed design employs an inverted T shape fin, in which the top fin width is narrower than the bottom fin width, hence minimizing the device's feature size.

4.3 PHYSICAL SIMULATION OF T SHAPED FIN.

The cogenda tool and the lombard equation for device modelling were used to generate all of the results and simulations. The doping dependent mobility model was also utilized to investigate the impact of carrier mobility in the 14nm Heterojunction N-FinFET. The drift-diffusion model and Boltzmann statistics were utilized in this simulation. The recombination rate is calculated using the sum of direct recombination and shockley read hall recombination. We used a global command on the device to set the external temperature to 300K. Electron and hole concentrations were introduced to the simulation as shown in equations 4.1.

$$\nabla_n = -((h^2 \gamma n)/(6qm_n^*)) * ((\nabla^2 \sqrt{n})/(\sqrt{n})) \quad (4.1)$$

$$\nabla_p = -((h^2 \gamma n)/(6qm_p^*)) * ((\nabla^2 \sqrt{p})/(\sqrt{p})) \quad (4.2)$$

Where p and n indicate electron concentration, hole concentration, and valance band in the conduction band, h and q represent Planck's constant and electron charge, while m_n* and m_p* represent hole and electron effective mass.

The relationship between the temperature and energy bandgap can be represented by equation 3 [101].

$$E_g(T) = E_g(0) - \alpha E T^2/(T + \beta_E) \quad (4.3)$$

Where, α for Si = 5.41×10-4 eV/K and Eg = 1.42 eV, β_E = 206 K

The term electrical width of FinFET is defined as

$$\mathrm{W} = 2\mathrm{H}_{\mathrm{fin}} + \mathrm{T}_{\mathrm{fin}} \quad (4.4)$$

Where H_{fin} represents the fin-height and T_{fin} represents the fin-thickness

For the inverted T shaped fin of N-FinFET different parameter like On-state current (I_{on}), current ratio (I_{on} / I_{off}), off current (I_{off}), DIBL and SS have been evaluated.
Variation in the drain current per decade with respect to changes in the gate voltage is known as a subthreshold Swing and it is calculated as per equation 5

$$SS = \frac{\Delta V_g}{\Delta \log_{10} I_d} \qquad (4.5)$$

Reduction in threshold voltage on higher value drain voltage is defined as a DIBL and it is calculated as per equation 6.

$$DIBL = \frac{\Delta V_{th}}{\Delta V_d} \qquad (4.6)$$

mobility of the hole and electron for FinFET device calculated as per equation 7

$$\mu_v^L = \mu_{v,300}^L \left(\frac{T_L}{300K}\right)^{\gamma 0,v} \qquad (4.7)$$

Lattice temperature denoted by L and v represented the hole or electron.
Mathematically I_D (drain current) is represented as per equation 8

$$I_d = \emptyset + \mu C_{ox} \left(\frac{W_g}{L_g}\right)\left(\frac{(V_{gs} - V_{th})}{2m}\right) \qquad (4.8)$$

Here, μ represent electron mobility, L_g represent gate length, Ø represent the metal gate work function. C_{ox} is considered for oxide capacitance, W_g represent gate width. The term V_{gs} and V_{th} are gate to source voltage and threshold voltage or transistor. The oxide thickness and Fin thickness are presented by T_{ox} and W_{si} respectively.

$$m = 1 + \frac{3T_{ox}}{W_{si}} \qquad (4.9)$$

4.4 CURRENT CHARACTERISTICS OF INVERTED T N-FINFET.

The transfer characteristics of the proposed design -1 and proposed design-2 with rectangular shaped fin based FinFET are compared in Figure 4.3. The mole fraction value of 0.3 was used in both design proposals 1 and 2.

a) Proposed-1 14nm Heterojunction FinFET – In this design, Heterojunction created between the source-1 and channel by using the two different semiconductor material like Silicon Germanium (Si_{1-x} Ge_x) and Silicon.

b) Proposed-2 14nm Heterojunction FinFET – In this design, Heterojunction created between the drain-1 and source-2 by using the two different material like Silicon Germanium (Si_{1-x} Ge_x) and Silicon.

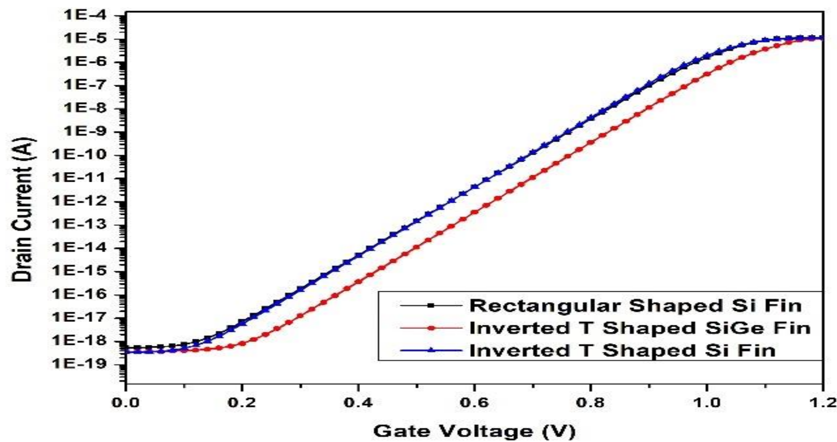


Fig. 4.3 Transfer characteristics comparison with different fin shaped.

The drain current in rectangular shaped fins (11.61 A) is the largest (compared to rectzoidal and T shaped fins) due to the rectangle's higher conducting area (see Figure 4.3 and Table 4.3). Proposed design-1, on the other hand, has a higher drain current than the rectzoidal shaped fin due to the SiGe effect used on the source end and the heterojunction created between the Source and the channel region. The SiGe material in the source location causes the uniaxial compressive strain on the channel. This results in a lattice mismatch between SiGe and Si, increasing channel strain.

Table 4.3: Comparison of Performance Parameter

Performance Parameters	**Proposed-1 T shaped Fin**	**Proposed -2 T shaped Fin**	**Rectzoidal Shaped Fin [33]**	**Rectangular shaped Fin [78]**	**Broadwell FinFET [102]**	**Trapezoidal FinFET [103]**
On Current I_{on} (A)	11.05×10^{-06}	10.50×10^{-06}	8.8×10^{-06}	11.61×10^{-06}	1.62×10^{-05}	1.80×10^{-05}
Off Current I_{Off} (A)	3.40×10^{-19}	3.61×10^{-19}	1.98×10^{-11}	5.33×10^{-19}	1.68×10^{-11}	1.98×10^{-11}
Current Ratio I_{On}/I_{Off}	3.25×10^{13}	2.9×10^{13}	4.43×10^{5}	$2.17\text{x}10^{13}$	$9.64\text{x}10^{06}$	$9.09\text{x}10^{06}$
SS (millivolt/decade)	56.83	55.94	65.8	63.48	63.35	64
DIBL (millivolt/volt)	26.3	23.02	50.3	29.84	28	31
Area of Fin (nm^2)	92	92	380	200	-	-

- *Not Calculated

Proposed -1 shows the better results in terms of off current, current ratio, subthreshold slope and drain induced barrier lowering in comparisons to rectangular shaped based FinFET and rectzoidal shaped based FinFET. In comparisons to rectangular shaped based FinFET and rectzoidal shaped based FinFET shows the lesser area for the footprint of fin in the proposed 1 & 2 design as per table 4.3.

When compared to traditional FinFETs, the complexity level of fin production in the suggested design is slightly higher from a fabrication standpoint. In the case of T shaped based FinFET, formation of the fin will be occurred in two steps. With the help of plasma etching and optical lithography, a down fin with a width of 8 nm will be constructed in the early phases for the proposed design. After that, a top fin with a width of 4nm and a height of 17nm will be produced using optical lithography, followed by plasma etching. The sidewall of the fin will be rough after manufacture, which can be smoothed out using oxidation and H2 annealing. Only the fin creation in the proposed design will be difficult, but with the help of the aforementioned processes, we can easily overcome this difficulty, as the provided design produced superior results in terms of current gain and off current,

improving the SCE effects in the design. The next sections show the performance analysis of the proposed-1 inverted-T shaped Si fin-based 14nm heterojunction FinFET.

4.5 PROCESS VARIATION ON PERFORMANCE PARAMETER OF PROPOSED FinFET.

In this section, we discussed the process variation impact on the performance of T shaped based fin of heterojunction FinFET. As process variation is very important analysis for any device to see the post impact on device performance.

1) Impact of Mole Fraction – As per the figure 4.5, impact of mole fraction on the proposed design is very less when it varies from 0.1 to 0.4. The Ioff current increases as the mole fraction is reduced from 0.4 to 0.1, owing to the lower threshold voltage. To apply biaxial strain to the channel, strain Si is grown on relaxed SiGe or relaxed SiGe generated on a Silicon Substrate [104]. Due to a mismatch in the Si to SiGe lattice, the Si source creates uniaxial strain in the channel in the recommended configuration, which increases strain. As a result, the carrier's channel mobility improves. Strain's effect on SiGe and Si is seen in figure 4.4. Figure 4.4 shows that strain increases the silicon source's electron affinity, and the conduction band energy of unstrained Silicon is higher than that of strained Silicon, lowering the bandgap. On the other hand, the energy of the valence band on the SiGe layer increases as the germanium content in Si1-x Gex increases. As a result of the strain, the effective mass of the carrier will decrease, resulting in a fall in the density of the state of holes in the valence band. Based on available studies, equation 4.12 depicts the effect of strain on Si.

$$(\Delta E_C)_{s-Si} = 0.57x \tag{4.10}$$

$$(\Delta E_g)_{s-Si} = 0.4x \tag{4.11}$$

$$V_T \ln\left(N_{V,Si}/N_{V,s-Si}\right) = V_T \ln\left(m^*_{h,Si}/m^*_{h,s-Si}\right) \cong 0.075x \tag{4.12}$$

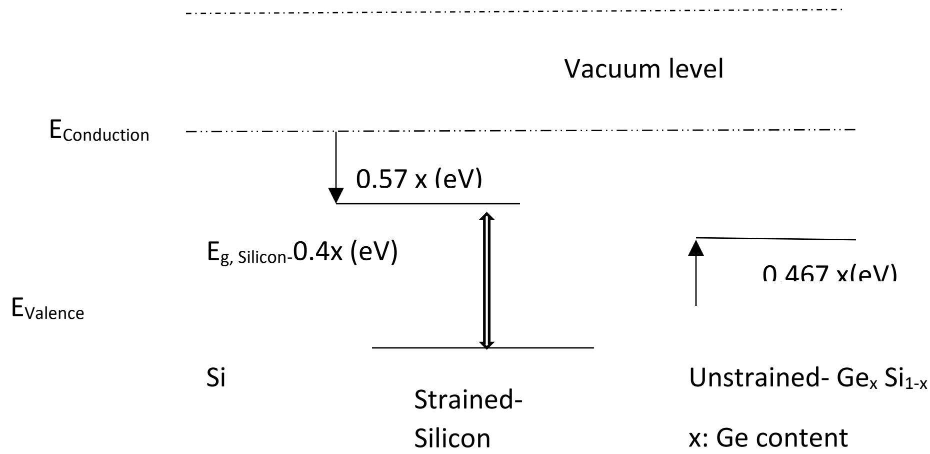


Fig. 4.4 Impact of strain on band structure of Silicon-Germanium ($Si_{1-x}Ge_x$) and Silicon (Si) [78]

x denotes the variation in germanium content in $Si_{1-x}\ Ge_x$, $(\Delta E_g)_{s-Si}$ and $(\Delta E_C)_{s-Si}$ is represent the decrease in conduction band due to the strain that further reduces the electron affinity. State density of valence band for the strained silicon and unstrained silicon represented by the $N_{V,s-Si}$ and $N_{V,s-Si}$. Thermal voltage of the device denoted by V_T and effective mass of hole charge carrier for strained silicon and unstrained silicon, respectively. $m^*_{h,Si}$ and $m^*_{h,s-Si}$

2. Impact of Temperature: Figure 4.6 a showed the effects on drain current when temperature changes from 250K to 400K. The threshold voltage of the proposed-1 FinFET decreases as the temperature rises from 250 K to 400 K due to increased electron density, which limits mobility. As the minority(hole) carrier drops, the FinFETs patristics resistance lowers, as illustrated in equation 10. The maximum deviation in the off current value as the temperature rises from 250K to 400K is shown in proposed-1 design due to lowering threshold voltage, which increases the drain current, but mobility, on the other hand, reduces the drain current due to an increase in temperature, causing the off current to degrade as compared to the on current.

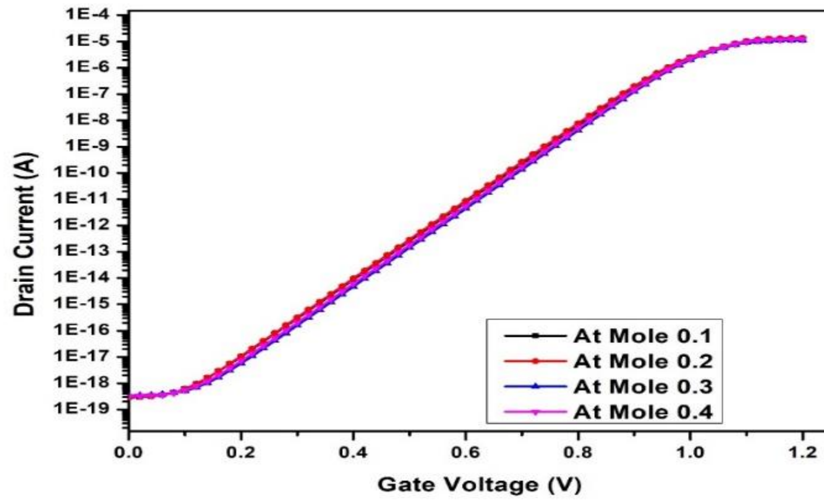
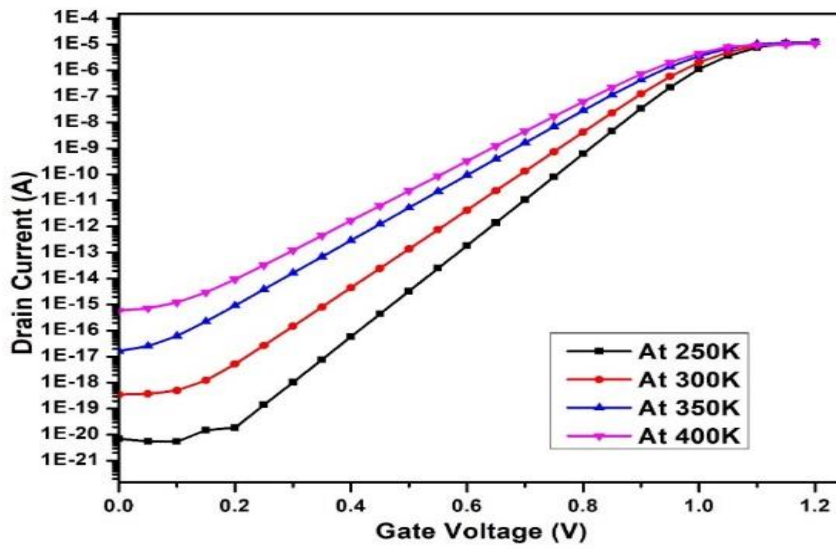
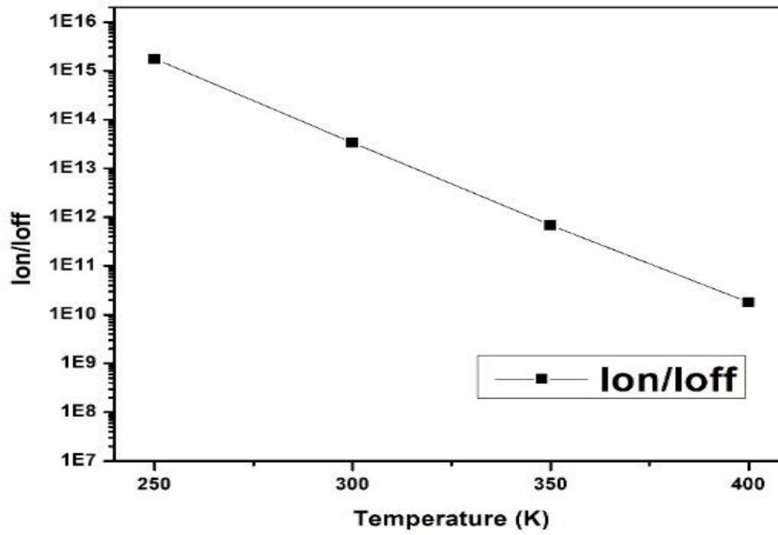


Fig. 4.5 Transfer characteristics on different mole values



(a)



(b)

Fig. 4.6 a) Transfer characteristics at different temperature b) Current ratio (I_{on}/I_{off}) at different temperature.

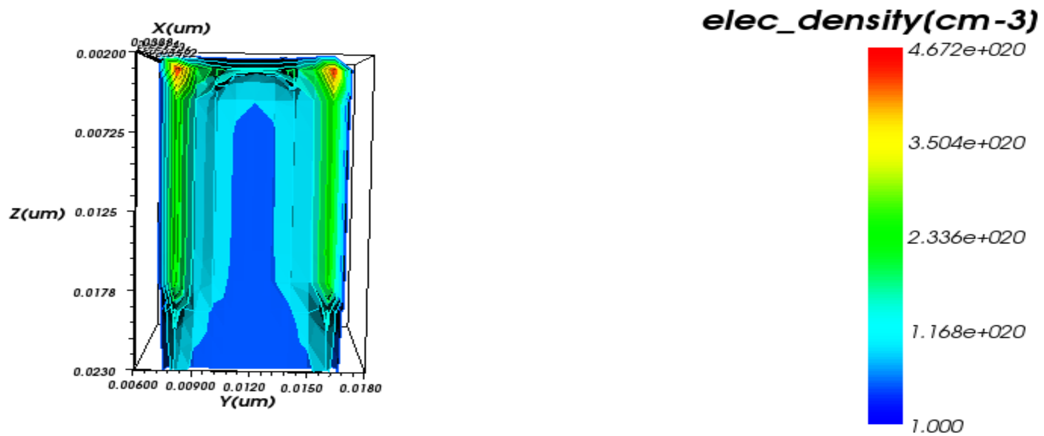


Fig. 4.7 Electron density inside the fin of T shaped FinFET.

The transistor switching application uses the on/off ratio (I_{on}/I_{off}) as a key parameter. Figure 4.6 b shows that the on/off ratio is substantially higher at low temperatures (I_{on}/I_{off}) than at

high temperatures (I_{on}/I_{off}). The fin in the suggested design is formed like an inverted T, which means that the electron concentration is dispersed from the bottom to the top of the fin, as illustrated in figure 4.7. As a result, the area of electron confinement at the bottom of the fin is greater than that at the top. As a result of the geometrical constriction of the channel, the phonon scattering rate increases, increasing mobility according to equation 4.12, resulting in an increase in drain current for the suggested design.

3. Effect of doping level: Figure 4.8 shows the effect of altering the doping from 10^{16} to 10^{19} cm^{-3} on the drain current of the inverted-T shaped Si fin. In general, a lower doping profile will have a higher drain current due to the lower threshold voltage, whereas a higher doping profile will have a higher threshold voltage due to the higher charge concentration, resulting in a lower drain current. The threshold voltage reduces as the doping profile increases, resulting in a rise in the off current and a rise in the short channel effect.

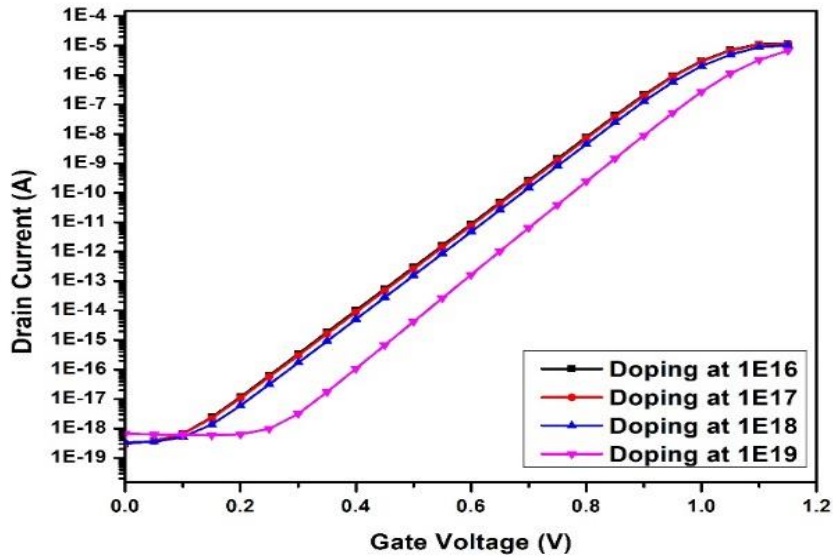


Fig. 4.8 Doping impact on T shaped FinFET.

As a result, when the doping profile for the proposed-1 design is retained at 10^{19}, the I_{off} increases due to an increase in the V_T, which reduces the I_{on}, as shown in equation 4.8. However, changing the doping profile from 10^{16} to 10^{18} cm-3 results in less variance that makes this device more stable.

4.Impacts of different fin width: When we adjust the bottom fin width to 8nm, 7nm, and 6nm while retaining the fin height at 20nm, we see less variation in the I_{on} and I_{off} in the suggested design, as shown in figure 4.9. The threshold voltage increases as the fin width decreases, but the current drops [105]. Table 4.4 shows that when the fin width is kept at 6nm, 7nm, and 8nm, then I_{on} values attain at 2.12A, 2.02A, and 1.99A, respectively and I_{off} values attain at 3.13×10^{-19} A, 3.32×10^{-19} A, and 3.4×10^{-19} A, respectively. Current ratio attains at 6.77×10^{12}, 6.08×10^{12}, and 5.78×10^{12}, respectively.

Table 4.4: Variation of Fin Width on T shaped FinFET

Parameter	**$W_{top\text{-}Fin}$ 6nm**	**$W_{top\text{-}Fin}$ 8nm**	**$W_{top\text{-}Fin}$ 7nm**
I_{on} (μA)	2.12	1.99	2.02
I_{off} (A)	3.13E-19	3.4E-19	3.32E-19
I_{on}/I_{off}	6.77E12	5.78E12	6.08E12
DIBL (mV/V)	56.66	26.23	42.22

5.Effect of different Gate length: The proposed device's fin width and fin height were set to 8nm and 20nm, respectively, to investigate the effect of gate length on the performance parameter. The on current of the proposed device increases to 1.72 A, 1.99 A, and 2.13 A, respectively, when the gate length is retained at 14nm, 16nm, and 18nm, and the off current lowers to 4.57×10^{-19} A, 3.40×10^{-19} A, and 3.34×10^{-19} A, according to table 4.5 and figure 4.10. When the gate length is shortened, the device's threshold voltage is dropped, and the short channel effect becomes more dominant; therefore, when designing a low-power device, choosing the right gate length is crucial. As gate length varies in the suggested design, the performance metric displays reduced fluctuation.

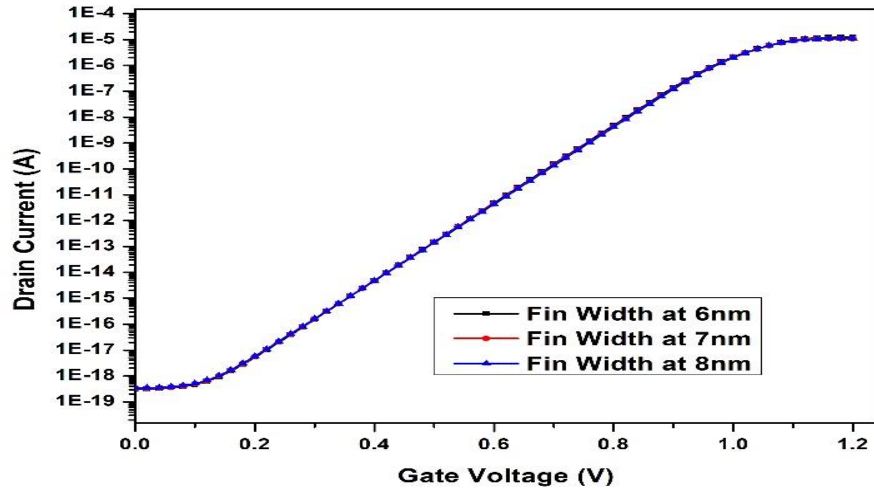


Fig. 4.9 Variation of Fin Width on T shaped FinFET.

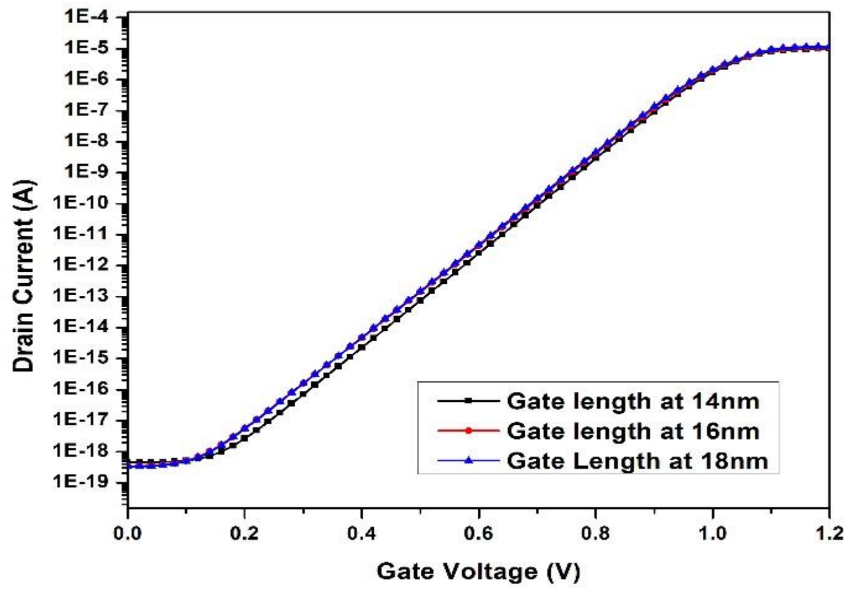


Fig. 4.10 Variation of gate length on T shaped FinFET

Table 4.5: Variation of Gate length on T shaped FinFET

Parameter	L_{gate} **14nm**	L_{gate} **16nm**	L_{gate} **18nm**
I_{on} (µA)	1.72	1.99	2.13
I_{off} (A)	4.57E-19	3.40E-19	3.34E-19
I_{on}/I_{off}	3.76E12	5.85E12	6.37E12
V_{th} (mV)	101	113	124

4.6 CURRENT FLOW INSIDE THE FIN.

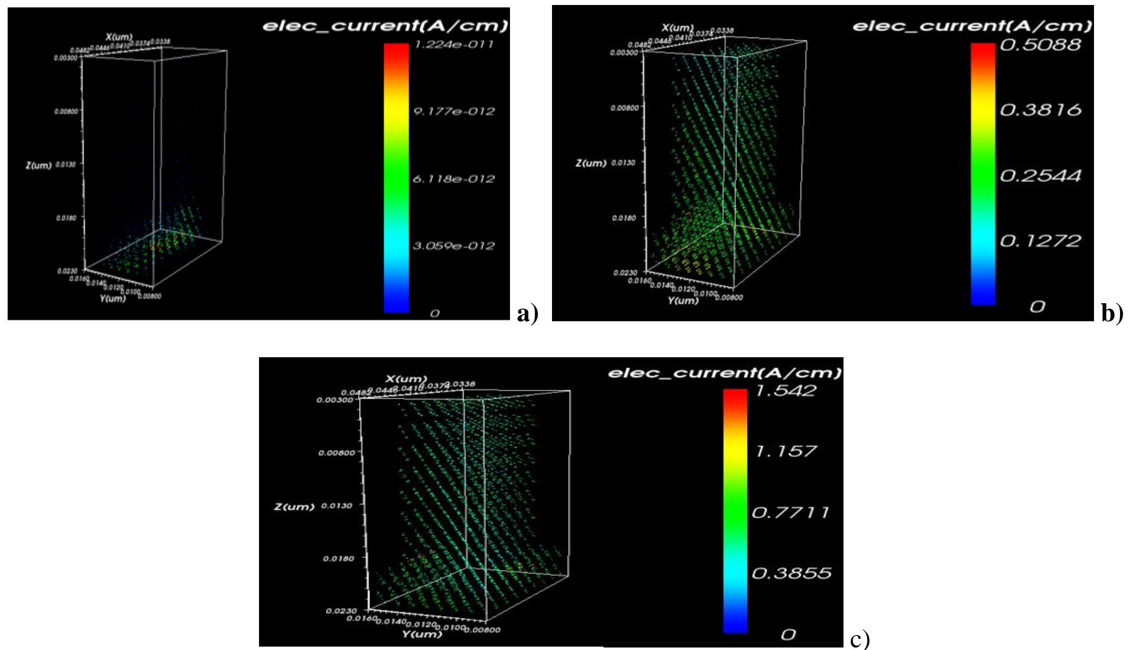


Fig. 4.11 Current Flow a) When V_{gs} is 0.18V b) When V_{gs} is 0.96V c) When V_{gs} is 1V

Figures 4.11 a, b, and c depict current flow within a 14nm heterojunction FinFETs inverted-T fin at 0.18V, 0.96V, and 1V, respectively. The current (3.03x10-18 A) flows from the drain to the source region through the bottom of the fin instead of the top when the voltage is 0.18V. Because the top fin is 4nm wide and the bottom fin is 8nm wide, current flows from the bottom of the fin first due to the large conducting surface. Figure 4.11 c shows the maximum current flow from drain to source area when the gate voltage is 1V.

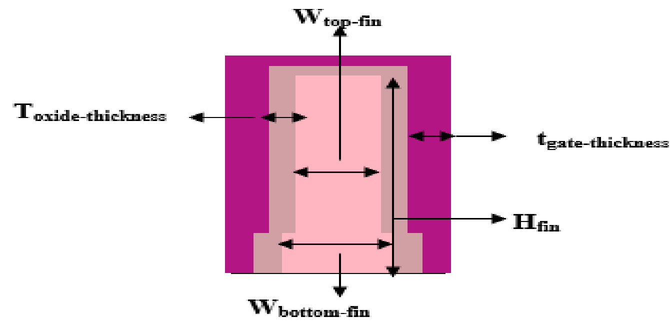
4.7 DEVICE DESIGN PARAMETER & SIMULATION OF P-FinFET

The Cogenda TCAD design tool was used to create the suggested inverted-T shaped heterojunction P-FinFET structure. Both gate engineering and channel engineering concepts are utilized in the P-FinFET design by altering the channel doping concentration and work function. The parameters that were taken into account while designing the N-FinFET and P-FinFET devices are shown in table 4.6.

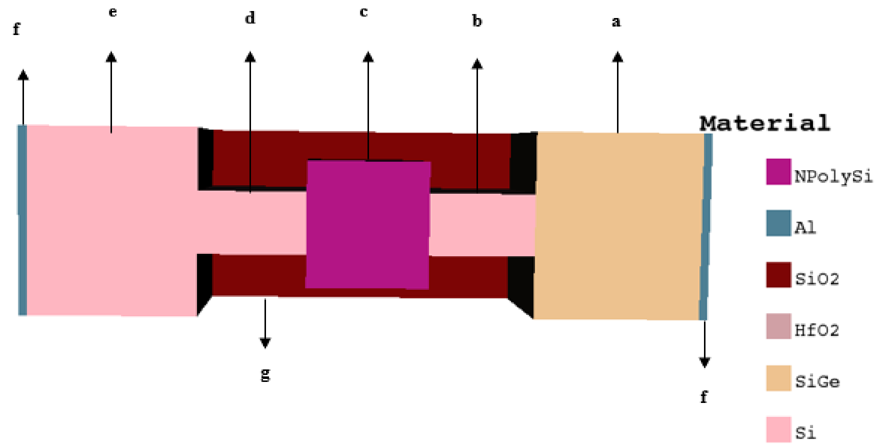
Table 4.6: Device design parameter of 14-nm heterojunction N-FinFET and P-FinFET of T shaped fin.

Parameter	**P-FinFET**		**N-FinFET [105]**	
	Material	**Dimension**	**Material**	**Dimension**
Extended Source -1 (a)	Silicon Germanium	13nm	Silicon Germanium	13nm
Extended Source-2 (b)	Silicon	20nm	Silicon	20nm
Extended Drain-1 (e)	Silicon	13nm	Silicon	13nm
Extended Drain-2 (d)	Silicon	20nm	Silicon	20nm
T shaped Fin (Channel length)	Silicon	14nm	Silicon	14nm
Gate (c)	NPolySi	14nm	PPolySi	14nm
Height of Fin (H_{fin})	-	20nm	-	20nm
Thickness of Fin ($W_{top-fin}$ / $W_{bottom-fin}$)	-	4nm/8nm	-	4nm/8nm
Gate Oxide Thickness ($t_{oxide-thickness}$) ($t_{top-oxide}$ /$t_{bottom-oxide}$)	Hafnium oxide	3nm/2nm	Hafnium oxide	3nm/2nm
Source & drain Contact (f)	Aluminum	20nm	Aluminum	20nm

Figure 4.12 a show the inner view of the P-FinFET and figure 4.12.b shows the three-dimension view of the same device.



(a)



(b)

Fig. 4.12 (a) 14-nm heterojunction inverted-T P-FinFET (b) Three-dimensional of 14-nm heterojunction inverted-T P-FinFET

In both P-FinFET and N-FinFET, a heterojunction point was created between a-region (extended source-1) and b-region (extended source-2) by using the two different semiconductor materials. As per figure 1. b, the g- region represent the SiO_2 that provided the insulation to the fin from the substrate region to avoid the leakage current. For b-region, silicon material was used and for a-region silicon germanium (Si_{1-x} Ge_x) material by keeping the mole fraction fixed at 0.2. For the P-FinFET, effective width will be calculated as per equation 4.13.

$$W_{\text{eff}} = 2H_{fin} + W_{fin} \qquad (4.13)$$

For matching the transfer characteristic of both the devices P-FinFET and N-FinFET, change the doping level and increased the work function value in the P-FinFET. In P-FinFET, the doping level of the channel region is kept at $1\text{x}10^{18}$ /cm^3 and for the source and drain region at $1\text{x}10^{20}$ /cm^3, $1\text{x}10^{17}$ /cm^3 respectively. Work function value in P-FinFET kept at 4.36 eV and in N-FinFET at 4.17 eV for simulation purposes. To analyze the current characteristics of the 14-nm P-FinFET, the voltage on the gate terminal ramp from 0 to 1.2 volt and kept the drain voltage at 1 volt and source voltage at 0V.

4.8 COMPARISION OF A PERFORMANCE PARAMETER OF P-FinFET & N-FinFET.

Table 4.7, shows a comparison of the performance parameter of N-FinFET and P-FinFET. In the case of P-FinFET, the current ratio (On/Off) is $6.77\text{x}10^{12}$, on current is 2.21 µA and off current is $3.26\text{x}10^{-19}$ when mole fraction at 0.2 and When mole fraction at 0.1 than current ratio (On/Off) is $1.99\text{x}10^{13}$, on current is 6.61 µA and off current is $3.32\text{x}10^{-19}$. In comparison to the N-FinFET, off current is minimum in P-FinFET. As in the case of P-FinFET, the majority carrier is a hole that's why P-FinFET always shows lesser current as compared to the N-FinFET where the majority carrier is the electron. Electron shows the higher affinity as compared to the hole that's why the on current in N-FinFET [23]. But at mole fraction 0.1, P-FinFET attains the higher on-current (I_{ON} = 6.61µA) in comparison to the other proposed P-FinFET where mole fraction is 0.2. Due to lesser content of Ge in Si_{1-x} Ge_x material reduces the recombination rate inside the fin and germanium material hold a higher value of electron affinity value as compared to the silicon material that why less electron populated from the extended source towards the fin of P-FinFET. As compared to the planar PMOS, the proposed design of P-FinFET shows the higher on/off ratio (1.99 $\text{x}10^{13}$), minimum I_{off} current ($3.32\text{x}10^{-19}$ A) and minimum SS and DIBL on the same technology node.

Table 4.7: Performance Parameter Comparison of P-FinFET.

Device Performance Parameter	T shaped 14-nm Heterojunction P-FinFET When mole fraction 0.2	T shaped 14-nm Heterojunction P-FinFET when mole fraction 0.1	Planar PMOS [100]	FinFET at 7nm [103]	FDSOI [106]	FinFET [107] IRDS 2020
On Current (I_{on}) (A)	$2.21x10^{-6}$	$6.61x10^{-6}$	10^{-2}	$12.9x10^{-6}$	$3.04x10^{-4}$	$5.84x10^{-05}$
Off Current (I_{off}) (A)	$3.26x10^{-19}$	$3.32x10^{-19}$	10^{-8}	$17.5x10^{-12}$	$4.8x10^{-09}$	$1.5x10^{-09}$
I_{on}/I_{off}	$6.77\ x10^{12}$	$1.99\ x10^{13}$	10^{5}	$7.37\ x10^{05}$	$6.33x10^{4}$	$3.89x10^{5}$
SS (mV/Dec)	52.2	43.2	76.98	81.558	-	72
DIBL (mV/V)	28.55	15.44	68.57	-	-	50

-*Not Calculated

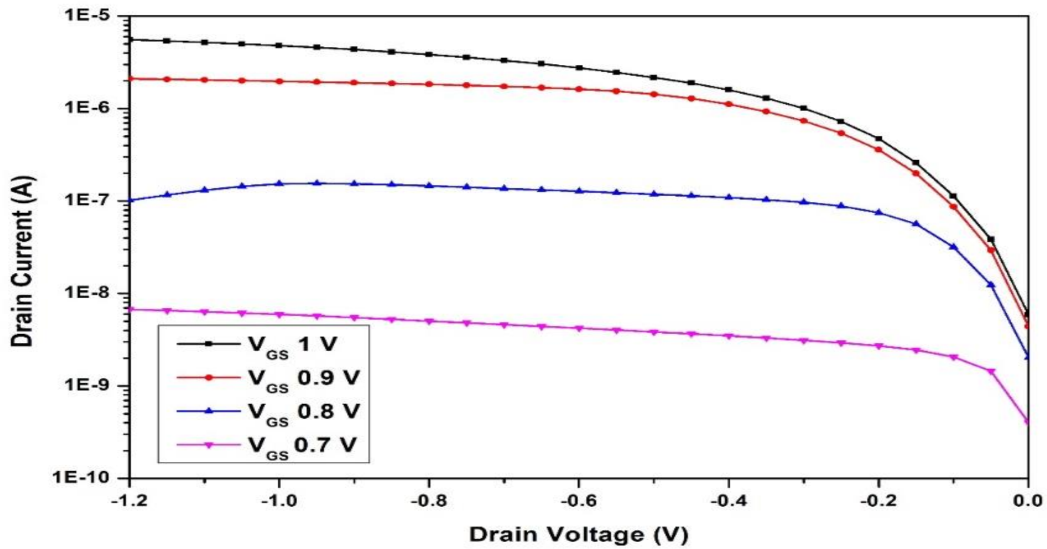


Fig. 4.13 Output characteristics of Inverted T shaped P-FinFET

Output characteristics of the 14-nm heterojunction inverted-T FinFET shown by figure 4.13 on different gate voltage. For getting the output characteristics of the P-FinFET, drain voltage ramp from 0 to 1.2 voltage on different gate voltage (V_{gs}) 0.9V,0.85V,0.80V and

0.7V. So as per figure 2, after pinch off voltage drain current get constant as drain voltage increases till 1.2V at fixed gate voltage. As the gate voltage decreases, then on current in the P-FinFET also decreases due to lesser quantity of majority carrier (hole) inside the channel region (T shaped).

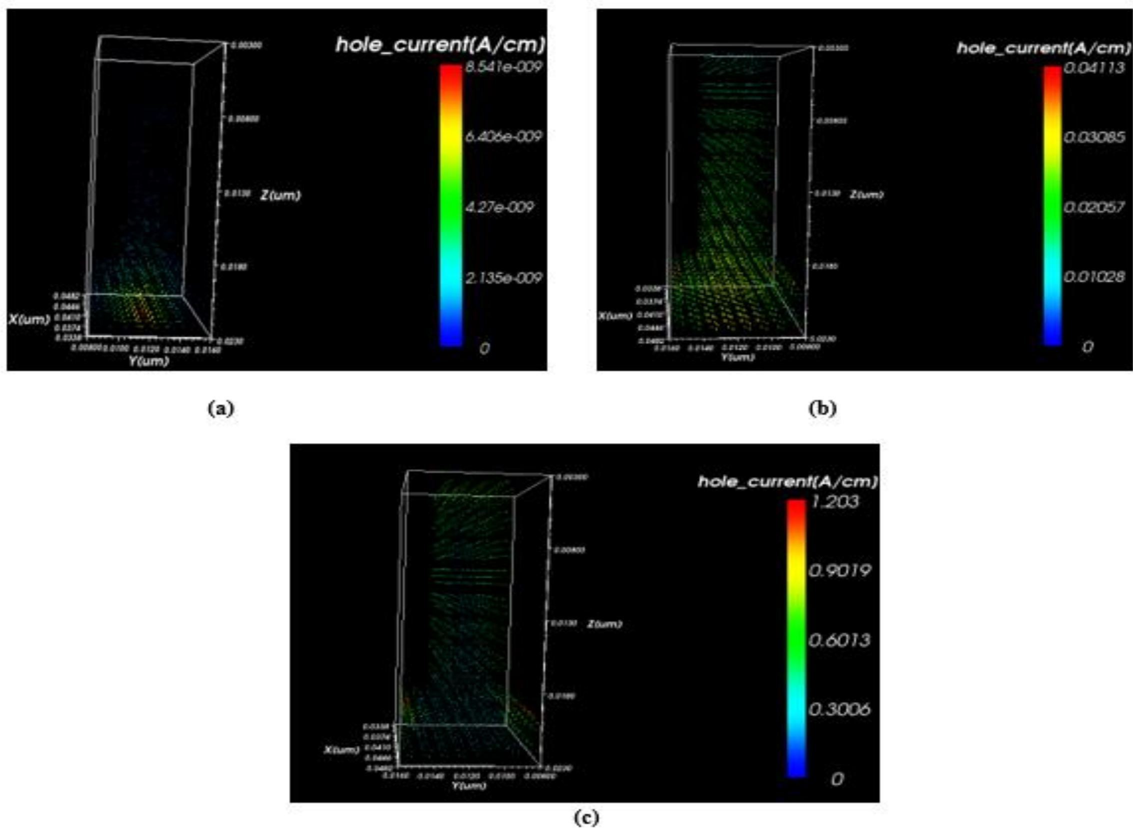


Fig. 4.14 Hole current Flow inside the T shaped P-FinFET **a)** When V_{gs} at 0.3V **b)** When V_{gs} at 0.7V **c)** When V_{gs} at 1V

Figure 4.14, shows the flow of current due to hole carrier inside the P-FinFET on the different gate voltage. When V_{gs} at 0.3V (figure 4.14.a) then hole movement is maximum at the bottom part of the fin due to larger width (8nm) and minimum at the top part of the fin due to minimum width (4nm). But as Vgs increases from 0.3 to 1 V, then maximum current flow due to the hole charge carrier from bottom to the upper part of the entire fin and the same shown in fig. 4.14.b and fig. 4.14.c. As per equation 4.8, when the V_{gs} value

increase and overcome the threshold voltage then the drain current also increases.

4.9 PROCESS VARIATION ON PERFORMANCE PARAMETER OF PROPOSED INVERTED T SHAPED 14-nm HETEROJUNCTION P-FinFET.

1. Impact of work function on I_d versus V_{gs} characteristics of P-FinFET

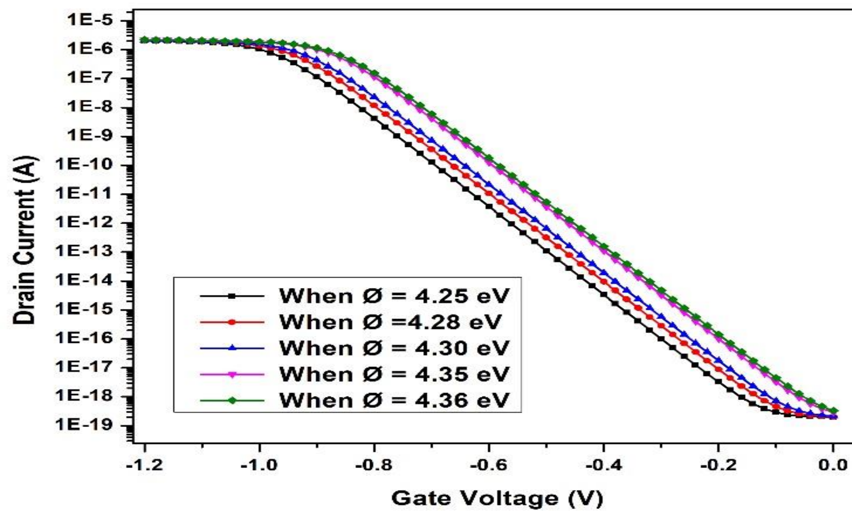


Fig. 4.15 I_d versus V_{gs} characteristics of heterojunction inverted-T P-FinFET with different gate contact work functions.

Figure 4.15 shows the drain current characteristics with respect to the gate to source voltage of the P-FinFET in logarithmic scale on a different value of the work function (Ø) and these curves help us to evaluate the on current, off current, and on/off current ratio of the device. As per figure 4, the drain current (on current) of the device increases exponentially with respect to the work function when it varies from 4.25 eV to 4.36 eV. As per equation 8, the drain current of the device is directly proportional to the work function that's why at 4.36 eV, P-FinFET shows the maximum current value of 2.21 µA.

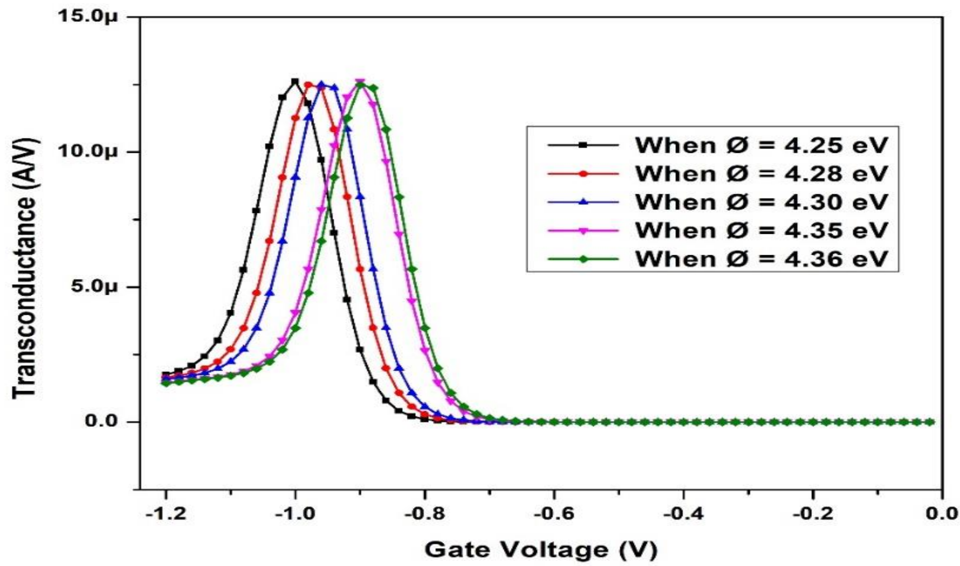


Figure 4.16 Transconductance versus Gate Voltage of heterojunction inverted-T P-FinFET with different gate contact work functions

Figure 4.16 shows the change in the transconductance of the P-FinFET of T-shaped fin. The transconductance (g_m) define the change in drain current as a function of the gate to source voltage change, and describe it quantitatively using equation 4.14.

$$\mathbf{g_m} = \frac{\Delta I_d}{\Delta V_{gs}} \tag{4.14}$$

The maximum value of the transconductance of the P-FinFET of T-shaped fin constant for all values of work function as per figure 4.16. This factor is an important design statistic for circuit-based applications, and a higher value of transconductance indicates that the FinFET has a greater capacity to operate as a power-saving device.

2 Impact of X in Si_{1-X} Ge_x on the drain current characteristics with respect to the gate to source voltage of P-FinFET

Impact of mole fraction (x) shown by figure 4.17, on the drain current characteristics with respect to the gate to source voltage characteristics of the P-FinFET. In this analysis, the

value of x varies from 0.1 to 0.5 with the division of 0.1 and drain voltage kept constant at - 1V and gate to source voltage ramp from 0 to -1.2V on the division of - 0.05V. Increasing the value of x in Si_{1-x} Ge_x, increases the concentration of germanium as per equation 11in the extended source that further increasing the affinity of the electron as germanium holds higher affinity value as compared to the silicon material. Due to this strain increases the population rate of the electron from the source region to the channel. As per equation 4.15, the bandgap of the strained silicon further increases the recombination rate in the channel region and decreases the hole concentration [108]. That's why on the higher value x, on current attain lesser value. The impact on the ratio of I_{on} / I_{off} current due to mole fraction is shown in figure 4.18. The variation in the off current is minimum for the proposed design due to the geometry of the fin that makes this device more suitable for minimizing the short channel effects (SCEs) if the desired mole fraction (x) not attained while fabricating the device. SiGe material provides a good thermal conductivity that's why used in the P-FinFET & N-FinFET. Band parameter for SiGe energy shown as per equation 4.15, 4.16 & 4.17 [109-126]

$$N_{\text{Valence band}} = \left(0.6\text{x} + 1{,}04(1 - \text{x})\right) * 10^{19}\text{cm}^{-3} \qquad (4.15)$$

$$\in = 11.8 + 4.2\text{x} \qquad (4.16)$$

$$(\Delta \mathbf{E_g})_{\mathbf{SiGe}} = 0.467x \qquad (4.17)$$

where, $\in$ is the permittivity of Silicon Germanium, $(\Delta E_g)_{SiGe}$ is a reduction in bandgap Si_{1-x} Ge_x from that of Si and $N_{Valence}$ band represent the density of state in unstrained Si_{1-x} Ge_x,.

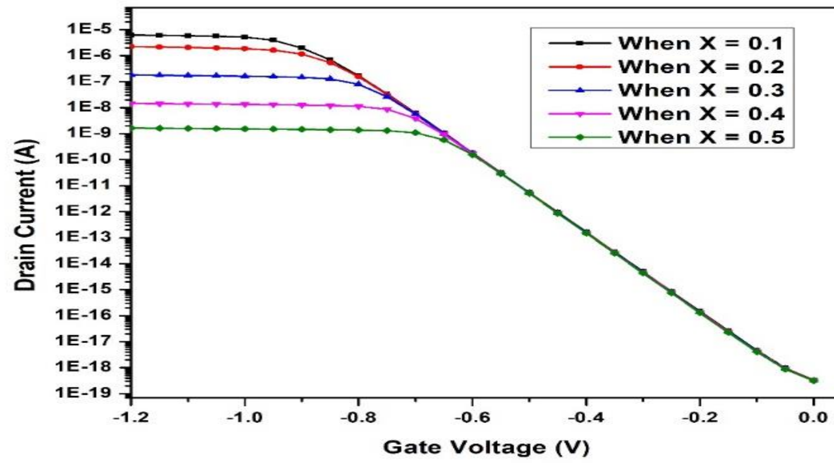


Fig. 4.17 Transfer characteristics of P-FinFET on different Mole fraction.

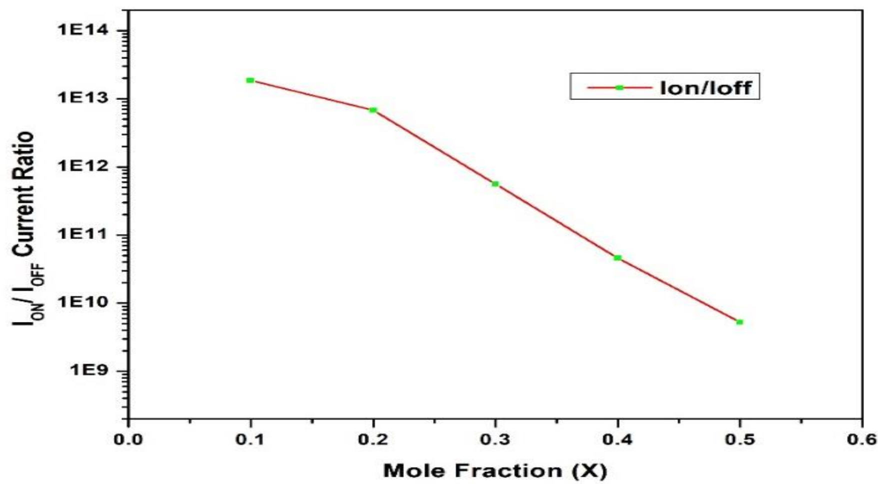


Fig. 4.18 Current ratio versus mole fraction for P-FinFET

3.Analysis of the drain current characteristics with respect to the gate to source voltage of P-FinFET on different temperature

As several electrical parameters behavior of the device are sensitive with an increase or decrease in temperature. The drain current was mostly impacted by mobility and threshold

voltage, as shown in equation 4.14. Figure 4.19 shows the impact on drain current when temperature varies from 200K to 400K on a step of 50K. The V_{th} of the device, exponentially depends on the temperature and with increases in temperature from 200K to 400K, degraded the threshold voltage of the P-FinFET. As a result, an increase in hole density, reduces the mobility of the charge carrier. As shown in equation 7, the patristics resistance decreases as the minority(electron) carrier decrease in P-FinFET. By lowering the threshold voltage, the drain current is increased; nevertheless, mobility reduces the drain current owing to an increase in temperature, which causes the off current to degrade in comparison to the on current. Figure 4.20, shows the impact on current ratio on different value of the temperature. As the temperature increases from the 200K to 400K, device shows the descending order in the current ratio that make this device reliable in between the 250K to 350K. With increase in the temperature, the mobility of the holes gets decreased that increases the hole density as result increased in the on current.

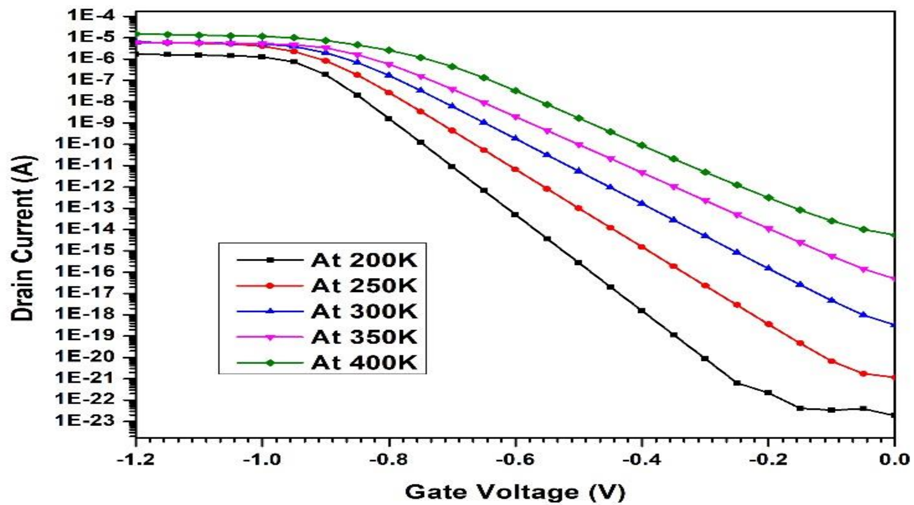


Fig. 4.19 Transfer characteristics of P-FinFET on different temperature

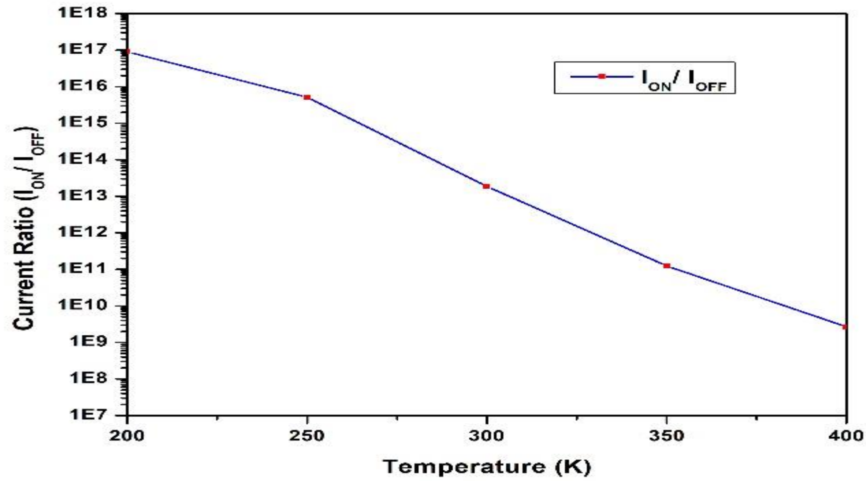


Fig. 4.20 Current Ratio Vs Temperature for P-FinFET

4.10 SUMMARY

A new heterojunction inverted-T shaped P-FinFETs and N-FinFETs has been proposed which is derived from rectangular Fin shape and its comparative analysis is performed with other planer PMOS, FinFET at 7nm technology node on different performance parameter. This paper the proposed heterojunction inverted-T P-FinFET shows a higher On-current ($6.61 x 10^{-6}$ A), higher I_{on}/I_{off} current ratio ($1.99 x 10^{13}$) with minimum Off-current, DIBL and SS values of $3.32 x 10^{-19}$ A, 15.4 mV/V) and 43.2 mV/Dec respectively as compared to the planer PMOS. The T shaped based N-FinFET shown current ratio is $3.25*10^{13}$, an off current is $3.40*10^{-19}$A, subthreshold swing is 56.83 mV/dec and DIBL is 26.3 mV/V which is better than the other FinFET of 7nm technology node. Process variation performed on the proposed heterojunction P-FinFET and N-FinFET on different parameters like work function, mole fraction (x) in Silicon Germanium ($Si_{1-x} Ge_x$) material and temperature.

Chapter 5

Application as an inverter by using the rectangular shaped FinFET and T shaped FinFET.

5.1 INTRODUCTION

The main objective of this chapter is to study and design an application as an inverter by using the proposed 14-nm Heterojunction FinFET and its comparison with others inverter. As discussed in chapter 2, different kind of inverter have been employed by the researchers to achieve the IOT based device for lower application. Inverter circuit is very important for designing any ALU unit or memory unit and play crucial role for deciding the performance of any VLSI circuit. In this chapter we proposed two kind of inverter one we designed by using the rectangular shaped based P-FinFET and N-FinFET and other one designed by using the inverted T shaped P-FinFET and N-FinFET.

1. **Design of inverter by using the T shaped FinFET**

For analyze the circuit performance, inverter circuit design by using the heterojunction-based P-FinFET and N-FinFET. The different performance parameter of the inverter t_{PHL} and t_{PLH}, high noise margin (NM_H), average delay and low noise margin (NM_L) has been evaluated. For matching the transfer characteristic of both the devices P-FinFET and N-FinFET, change the doping level and increased the work function value in the P-FinFET. In P-FinFET, the doping level of the channel region is kept at $1x10^{18}$ /cm^3 and for the source and drain region at $1x10^{20}$ /cm^3, $1x10^{17}$ /cm^3 respectively. Work function value in P-FinFET kept at 4.36 eV and in N-FinFET at 4.17 eV. The transfer characteristics of the P-FinFET and N-FinFET, are shown in figure 5.1. Transfer characteristics of the N-FinFET matched with the two designs of P-FinFET. In one design value of mole fraction x of Si_{1-x} Ge_x is used as 0.1 and the other for 0.2 respectively. A perfect matching of I_d versus V_{gs} characteristics is obtained for mole fraction x=0.1 which is further used in CMOS based inverter design. In both the design of P-FinFET, other parameters kept the same like doping

level of the channel region kept at $1x10^{18}$ /cm^3 and for source and drain region at $1x10^{20}$ /cm^3, $1x10^{17}$ /cm^3 and work function at 4.36eV.

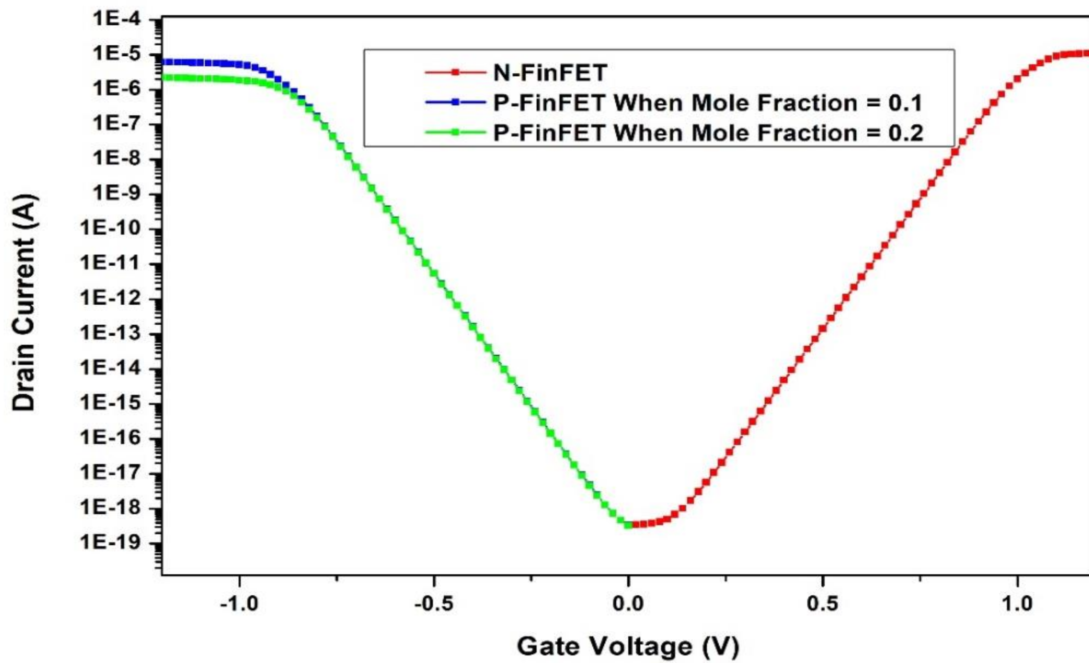


Fig. 5.1 Transfer characteristics of heterojunction P-FinFET & N-FinFET of T-shaped fin.

The inverter circuit diagram shown in figure 5.2, that was designed with the help of heterojunction P-FinFET and N-FinFET where the fin shape resembles T. For simulation purposes, load resistance R_L is kept 1 kiloohm. DC and Transient analysis done on the inverter circuit.

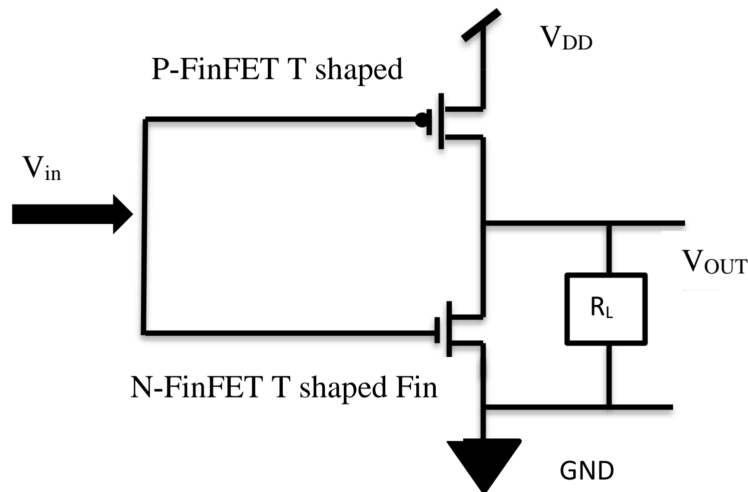


Fig. 5.2 Inverter Circuit by using the T-shaped P-FinFET & N-FinFET.

2. **Design of inverter by using the rectangular shaped FinFET**

For matching the transfer characteristic of both the devices P-FinFET and N-FinFET of rectangular shaped fin, changes done in the doping level of source/channel region and slightly increased in the work function value in the P-FinFET. In P-FinFET, the doping level of the channel region is kept at $1x10^{18}$ /cm^3 and for the source and drain region at $1x10^{20}$ /cm^3, $1x10^{17}$ /cm^3 respectively. Work function value in P-FinFET kept at 4.36 eV and in N-FinFET at 4.17 eV. The transfer characteristics of the P-FinFET and N-FinFET, are shown in figure 5.3. In both the cases value of mole fraction x of Si_{1-x} Ge_x is used as 0.3.

The inverter circuit diagram shown in figure 5.4, that was designed with the help of heterojunction P-FinFET and N-FinFET where the shape of the fin is rectangular. For simulation purposes, load resistance R_L is kept 1 kiloohm. DC and Transient analysis done on the inverter circuit and calculate the different performance parameter of the inverter t_{PHL} and t_{PLH}, high noise margin (NM_H), average delay and low noise margin (NM_L)

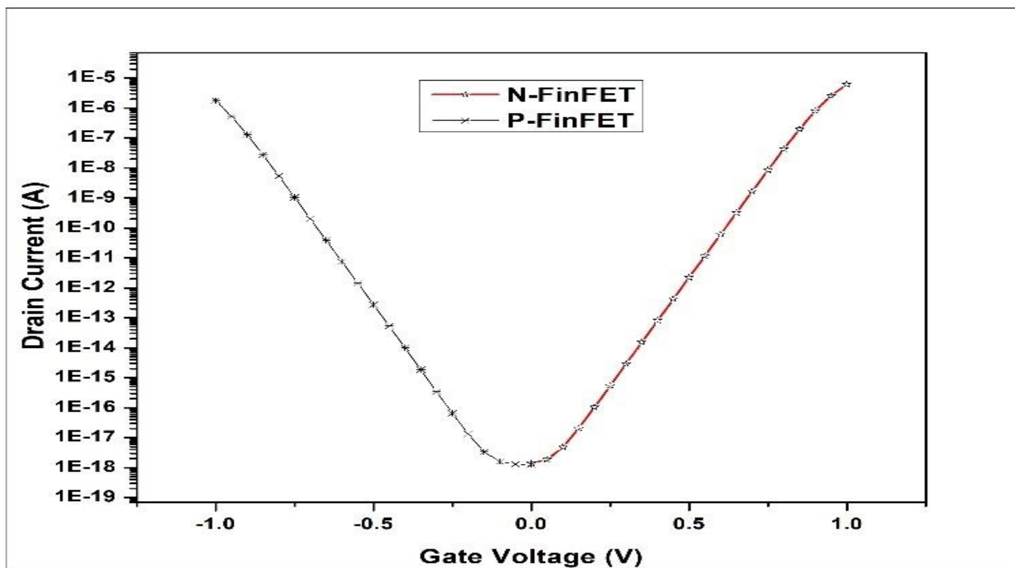


Fig. 5.3 Transfer characteristics of heterojunction P-FinFET & N-FinFET of rectangular -shaped fin.

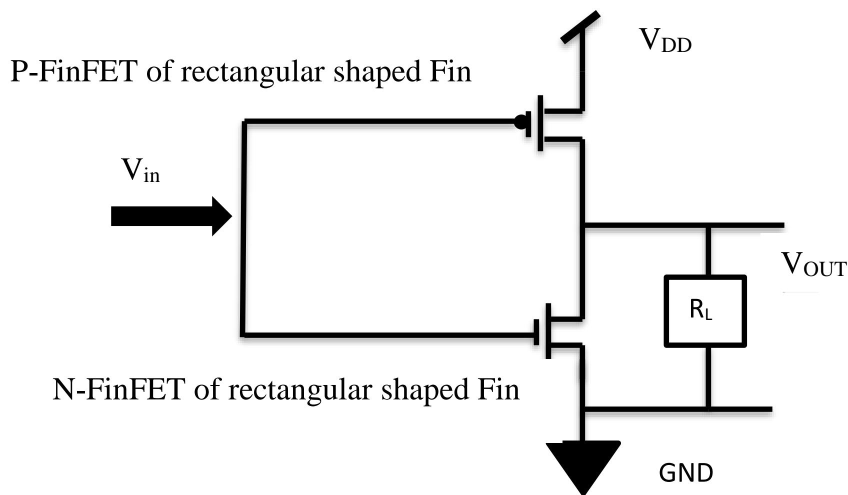


Fig. 5.4 Inverter Circuit by using the rectangular-shaped P-FinFET & N-FinFET.

5.2 DC ANALYSIS FOR RECTANGULAR & T SHAPED FIN OF FINFET

1) DC analysis for rectangular shaped fin of FinFET: Figure 5.5, shown the voltage transfer characteristic of rectangular shaped fin of inverter and it help us to examine the DC characteristics of the circuit. In this case input voltage of ramp from 0 to 1 V.

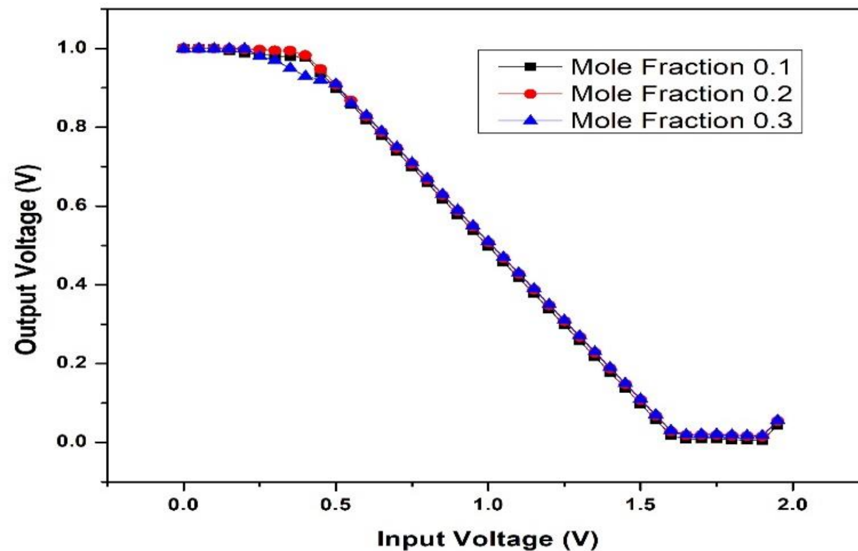


Fig. 5.5 VTC curve of rectangular -shaped fin.

This curve helps us to understand the switching of the device with respect to the input voltage. So as per figure 5.5, perfect switching observed at the mole fraction 0.3 when the input voltage changes its value from 0 to 1.

Table 5.1 shows that increasing the value of x from 0.1 to 0.3 increases the noise margin. The overall DC static characteristic of mole fraction 0.3 is superior, even though the noise margin values change slightly from mole fraction 0.1 to 0.3. Because the difference between the low and high noise margins is more than 25% of the supply voltage V_{dd}, the suggested transistors are noise-resistant.

Table 5.1: DC analysis of rectangular shaped fin of FinFET

Mole Fraction	Voltage level (V)					
	Output high V_{OH}	Output Low V_{OL}	Input high V_{IH}	Input Low V_{IL}	Noise Margin High (NM_H)	Noise Margin Low NM_L
x= 0.1	0.96	0.008	1.51	0.54	0.55	0.532
x=0.2	0.975	0.018	1.54	0.53	0.56	0.512
x=0.3	0.98	0.02	1.56	0.51	0.58	0.49

2) DC analysis for T shaped fin of FinFET

Figure 5.6, depicts the input and output voltage transfer characteristics (VTC) of the inverter circuit. It shows a perfect transition of output low and high values for input high and low values respectively.

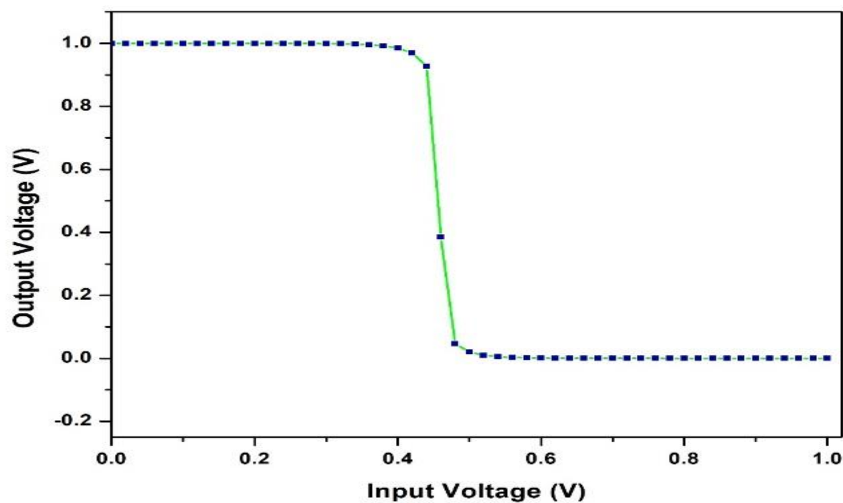


Fig. 5.6 VTC curve of T -shaped fin.

Table 5.2: Comparison of DC Analysis for different inverter

DC Analysis	**T shaped fin-based Inverter**	**CMOS inverter of $Si_{1-x}Ge_x$ source FinFET [77]**	**Rectangular shaped fin-based inverter [78]**
Output high V_{OH} (V)	0.99	1.91	0.96
Output Low V_{OL} (V)	0.03	0.031	0.008
Input high V_{IH} (V)	0.48	1.28	1.51
Input Low V_{IL} (V)	0.41	0.71	0.54
Noise Margin High (NM_H)	0.51	0.63	0.55
Noise Margin Low NM_L	0.38	0.679	0.532

Table 5.2, shows the comparative analysis of the proposed inverter with other designs on the basis of dc analysis. The proposed inverter shows a good noise margin as compared to another inverter [77] & [78]. The difference between the high and low noise margins is greater than 25% of the supply voltage V_{dd}, indicating an improved noise immunity of transistor.

5.3 TRANSIENT ANALYSIS FOR RECTANGULAR & T SHAPED FIN OF FINFET

1) Transient analysis of rectangular shaped FinFET

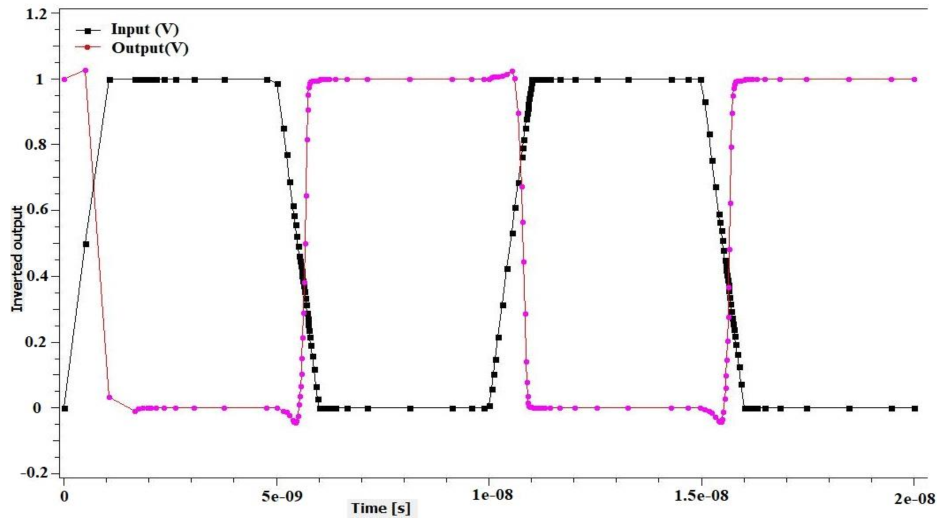


Fig. 5.7 Transient curve of the rectangular shaped fin at 0.1.

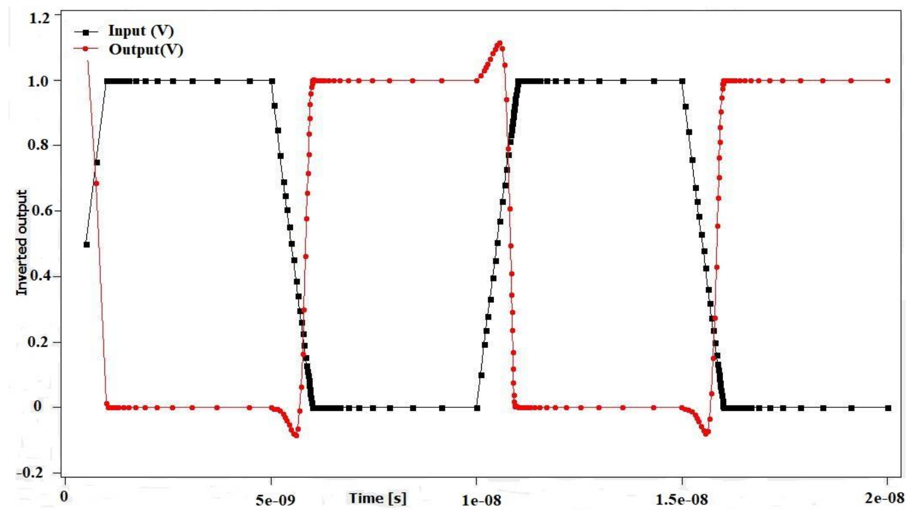


Fig. 5.8 Transient curve of the rectangular shaped fin at 0.2.

The transient analysis of the inverter are explored at different value of x (X=0.1, 0.2, and 0.3), as shown in figures 5.7, 5.8, and 5.9. In compared to mole fraction 0.3, few overshoots are visible at x=0.2, indicating unstable output behavior. With increasing value of x, the

value of V_T decreases dramatically.

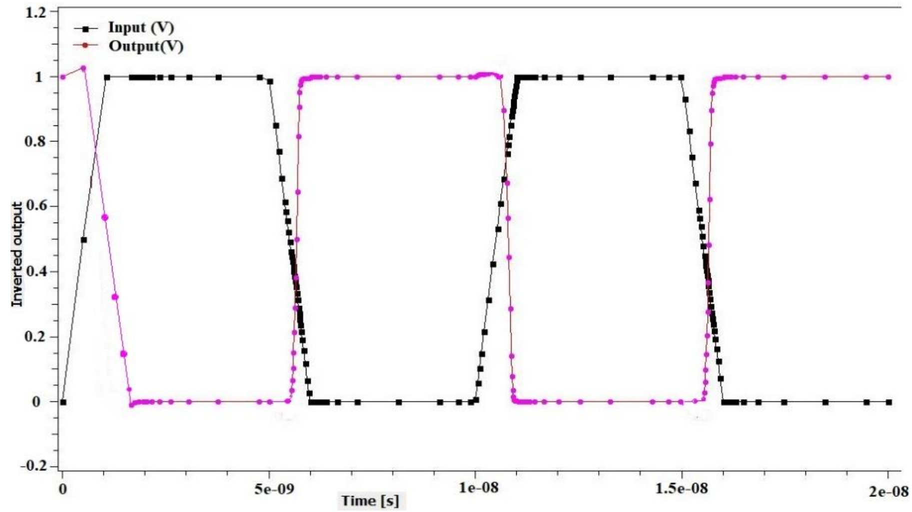


Fig. 5.9 Transient curve of the rectangular shaped fin at 0.3 mole fraction.

Table 5.3: Comparison of transient analysis for the rectangular shaped fin of inverter

Mole Fraction	Delay Parameter			Average Power(μW)
	t_{PHL} (ns)	t_{PLH} (ns)	Average Delay (ns)	
x= 0.1	0.5	1.4	0.95	4.97
x=0.2	0.6	1.6	1.1	4.61
x=0.3	0.7	1.8	1.25	4.31

As the mole value increases, the average latency climbs dramatically, but its average power reduces. This demonstrates a trade-off between delay and device subthreshold and ON/OFF performance.

2) Transient analysis of T shaped FinFET

As per figure 5.10, there are a few overshoots that demonstrate unstable output behavior

at 0.12ns. The threshold voltage varies with varying channel lengths and mole fraction x, which meets ITRS standards. That's why the output little unstable behavior at 0.12ns as the voltage rises. As per table 5.4, the proposed inverter shows the minimum average delay as compared to the inverter that was designed through the rectangular-shaped FinFET and also consumes less power.

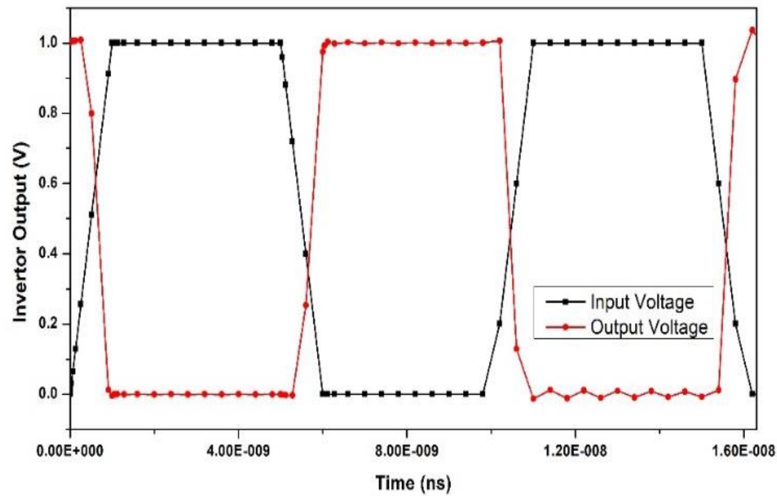


Fig. 5.10 Transient Curve of T shaped fin at 0.3 mole fraction

Table 5.4: Comparison of Transient Analysis for different inverter

Transient Analysis	**T shaped fin-based Inverter**	**Rectangular shaped fin-based inverter [78]**
t_{PHL} (ns)	0.590	0.5
t_{PLH} (ns)	0.780	1.4
Average Delay (ns)	0.685	0.95
Average Power μW	2.35	4.97

5.4 Summary

A new heterojunction inverted-T shaped P-FinFETs has been proposed which is derived from rectangular Fin shape and its comparative analysis is performed with other planer PMOS or FinFET for different performance parameter. This paper the proposed heterojunction inverted-T P-FinFET shows a higher On-current (6.61×10^{-6} A), higher I_{on}/I_{off} current ratio (1.99×10^{13}) with minimum Off-current, DIBL and SS values of 3.32×10^{-19} A, 15.4 mV/V) and 43.2 mV/Dec respectively as compared to the planer PMOS. Process variation performed on the proposed heterojunction P-FinFET on different parameters like work function, mole fraction (x) in Silicon Germanium ($Si_{1-x}\,Ge_x$) material and temperature. Further, low power circuit like inverter designed in this paper with help of heterojunction based P-FinFET and N-FinFET of T shaped fin and compared its performance parameter like noise margin, average delay and average power to the other inverter circuit. So, this device has perfect transient and static characteristics for logic inverters and it indicates that they are suitable for bulk memory applications and low-power digital logic.

Chapter 6

Scope for Future Work

In this chapter, the conclusions of the thesis work based on the analytical study carried out in the field of device modeling where 14-nm heterojunction based FinFETs and its application as an inverter have been presented. The prime objective of the study was to evaluate the performance of the FinFETs and identify the existing research gaps. On the basis of these gaps, new 14-nm hetrojunction based FinFET designed with fin shape of inverted T have been presented in this work and further implemented a inverter for low power based VLSI circuit

6.1 CONCLUSIONS

In chapter 1, a brief introduction carried out the transistor and its evolution. How the long channel device replaces by the short channel device as the transistor density double every year. The applications and advantageous of the FinFET also discussed. Further we have discussed the various types of the structure of the FinFET and its comparison with the traditional devices. Based on this, an exhaustive literature survey of the various techniques employed by the researchers to achieve the minimum short channel effect in the FinFET has been presented in chapter 2.

In chapter 3, designed a FinFET of 14-nm channel length and created a heterojunction region between the drain and source region by using the two different semiconductor material like silicon and silicon germanium. Further, we have compared that design with the conventional FinFET and other design that already designed by other researchers. Process variation on different parameter like temperature, mole fraction and oxide thickness carried out on the proposed design and obtain the optimize result for attaining the low power-based device.

In the chapter 4, we have changed the shape of the fin for proposed design and suggested an inverted T shaped. We have analyzed its transfer characteristics by comparing with other shaped that invented by the other researchers. Further we have done the process variation

on the proposed design on different parameter like oxide thickness, gate length, wok function and mole fraction, different material to see its current characteristics behavior.

An inverter designed by using rectangular shaped based FinFET and T shaped based FinFET in chapter 5. In this section we design the P-FinFET for the both the shape rectangular and T shaped. Further we analyzed the separately DC analysis and transient analysis for both the inverter and compared it with another inverter circuit. It has been identified both the inverter shows the good result in terms of noise margin and delay in comparison to other circuit.

The main contributions of this thesis work are summarized as:

- Comparative analysis of conventional FinFET with the proposed heterojunction FinFET on technology node of 14-nm.
- Process variation carried out for the proposed design on different parameter like temperature, oxide thickness, work function and mole fraction to analyze the post fabrication effect.
- Different fin shape analysis carried out on the proposed design and compare its characteristics with other available shapes of the FinFET.
- Design a application of inverter by using the proposed design and compare its characteristics with other available circuit of inverter.
- Performance validation of the proposed work with the existing state of the art

6.2 Future works

As discussed, the main focus of this research to design a heterojunction based FinFET device of different fin shaped on the technology node of 14-nm. The work has been carried out extensively based on the research gaps identified in the literature. However, there are still a few dimensions of this work that need to be touched in the future. Hence, here are a few issues that can be addressed in future work:

- Design and performance evaluation of FinFET for mixed-signal applications

- Fabrication of the proposed design and analyze its performance characteristics for another VLSI circuit.
- Design and performance evaluation of FinFET on lower technology node. Its circuit analysis of other biosensor-based applications.

Tool description

7.1 Introduction

In this chapter, we have demonstrated the tool description for designing the FinFET by using the 2D or 3D modelling. In my thesis, visual TCAD tool by cogenda for designing the FinFET on different technology node. This tool is capable of using the physical model like the current continuity and poisson equation for understanding the behavior of semiconductor devices. Moreover, we can do the advance analysis on the device like radiation or stress or optical impact on the performance parameter. In section one we discussed the basic steps for designing the device, second section cover the simulation analysis of the device and in third section discussed the different mechanism or tool for anglaise the results.

7.1.1 **Steps for designing the device by graphical interface**

Visual Tcad gives the flexibility to the researcher for designing the two-dimensional device by using the graphical interface and programing interface.

a) By using the graphical interface – in this case designer use the drawing interface for designing the device on different technology node with minimum limitation of the channel length for the device is 10nm.
b) Figure 7.1 shows the drawing surface on the visual Tcad where the designer with help of the toolbox can design any device of the two dimensional.
c) Visual Tcad supported the multiple meshing option for the designed tool that very important at the simulation time for analyzing the junction point or current point
d) Its support the triangular meshing to tetrahedron meshing depending on the dimension of the design.
e) We can use the different semiconductor material and oxide material and contact material for the device designing.
f) After covering the device region then we can apply the meshing as per the device dimension.

g) We can add the doping level on the different region as per the requirement by using the different technique like uniform doping level or gaussian doping level or mixed level doping as per the device.

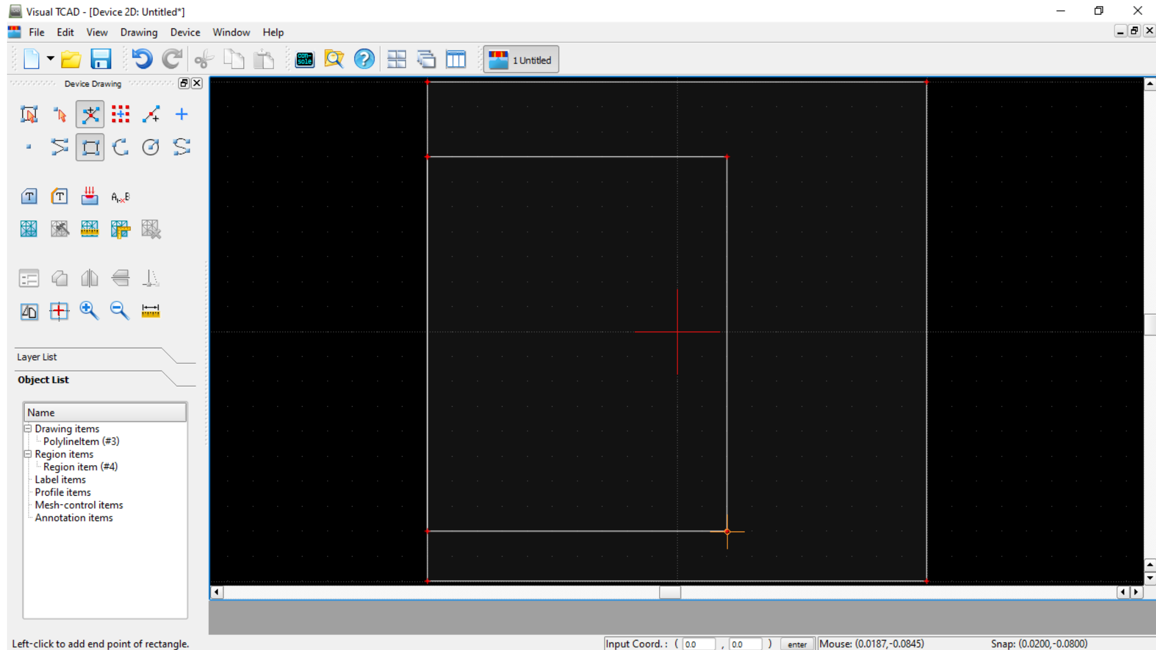


Fig. 7.1 Device drawing on the visual Tcad

h) At last we can save that file with the extension of .tif that further we can used for the simulation purposes.

7.1.2 **Steps for designing the device by programming interface.**

Visual Tcad supported the python language for designing the device in three dimensional or two dimensional. It's very user-friendly language that easy to implement as per the requirement of device.

a) In programing part first, we defined the global parameter of the device like temperature or meshing or dimension of the device that we need to design as mentioned in fig 7.2.

b) After this we need to defined the coordinates of the device like for two dimensional device x and y coordinates or for three dimensions x,y and z coordinates with

meshing.

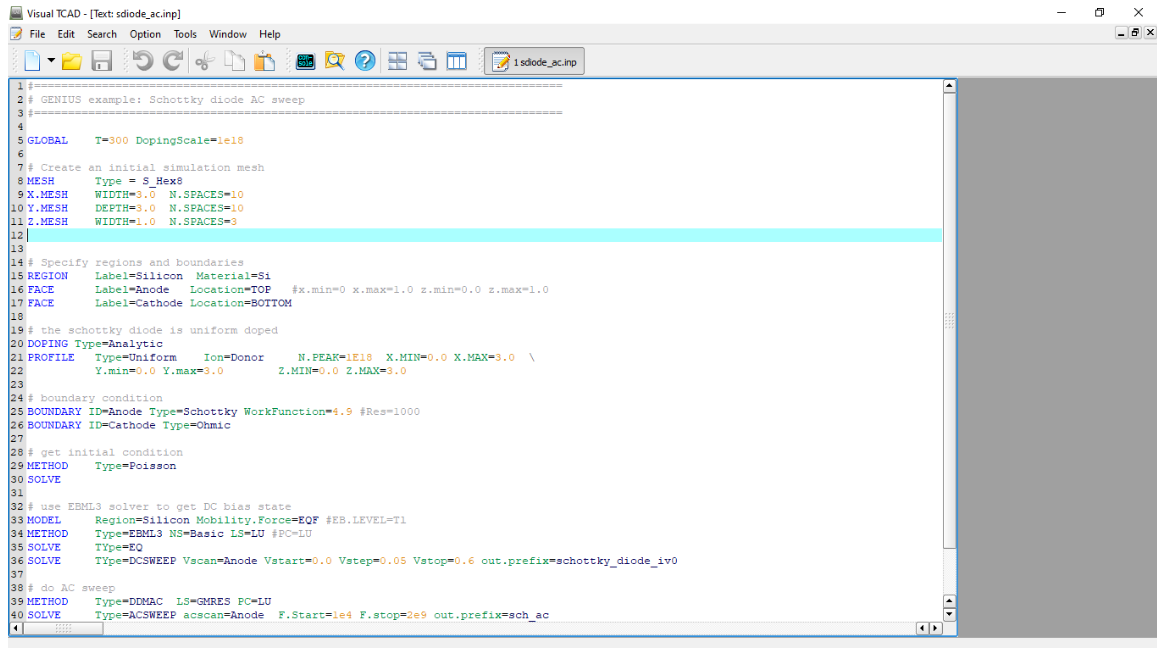


Fig. 7.2 Device programming on the visual Tcad.

c) After defining the coordinates of the device, need to mentioned the different region of the device by using the command line region for each region along with its object name and dimensions of each coordinates.

d) In above step we can use the polygon command for defining the region of the devices as per the requirement.

e) Then after we need to mentioned the doping level of the region as per the device like NMOS or PMOS by using the command line of doping with acceptor or donor.

f) We can use the different doping methodology here for each region like uniform or gaussian doping for each region.

g) After defining the doping command, we can export the device in two formats. cgns and .vtu. Both the extension has their own use like .cgns file we can use that file for simulation purposed of the device through the graphical interface as shown in fig 7.3. Extension. vtu we can use for analyse the different region of the device in terms of potential or conduction or valence band etc of the devices.

h) We can use the graphical interface also for the simulation of the device as mentioned in fig 7.4.

i) We can do various simulation mode on the device like static or transient or circuit and Ac sweep as per the requirement of the analysis.

j) In this step, we can combine the region also by using the function of network like multiple gate terminal need to combine with one terminal like other.

k) At above stage we can set the different simulation modelling for the device through the command prompt like doping concentration or work function of the device.

l) At last after simulation we can analyse the result of the device and prepare a different graph like linear or logarithmic for deep analysis of the device.

m) We can import the result and graph of the device performance on the excel sheet format further analysis.

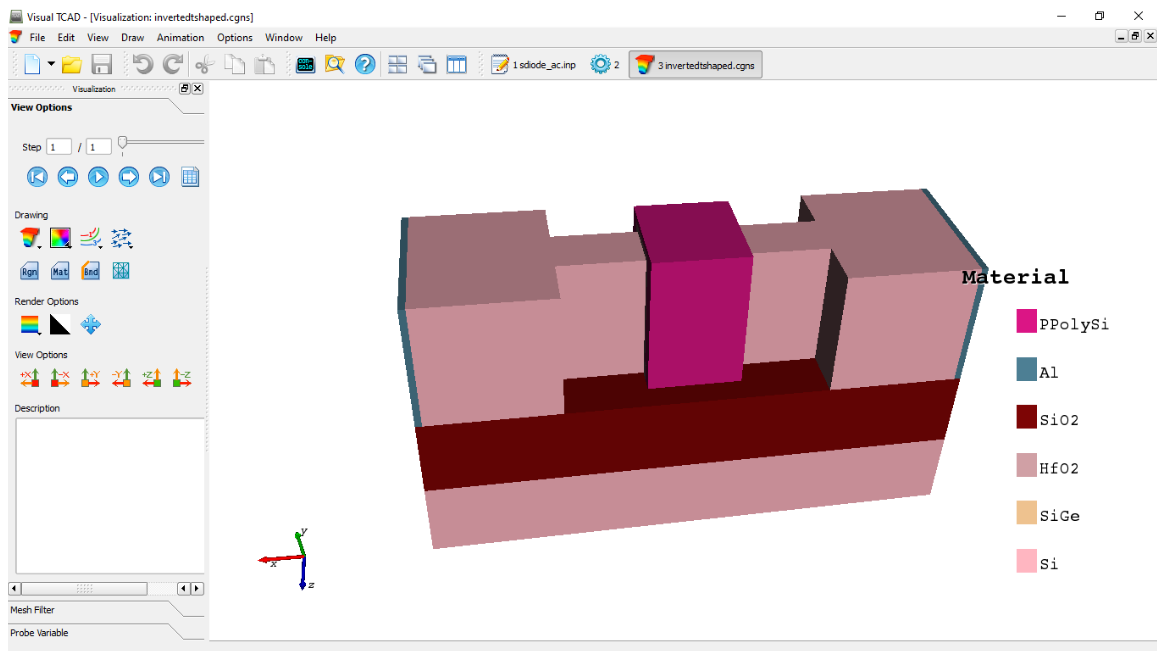


Fig. 7.3 Device visualization on the visual Tcad.

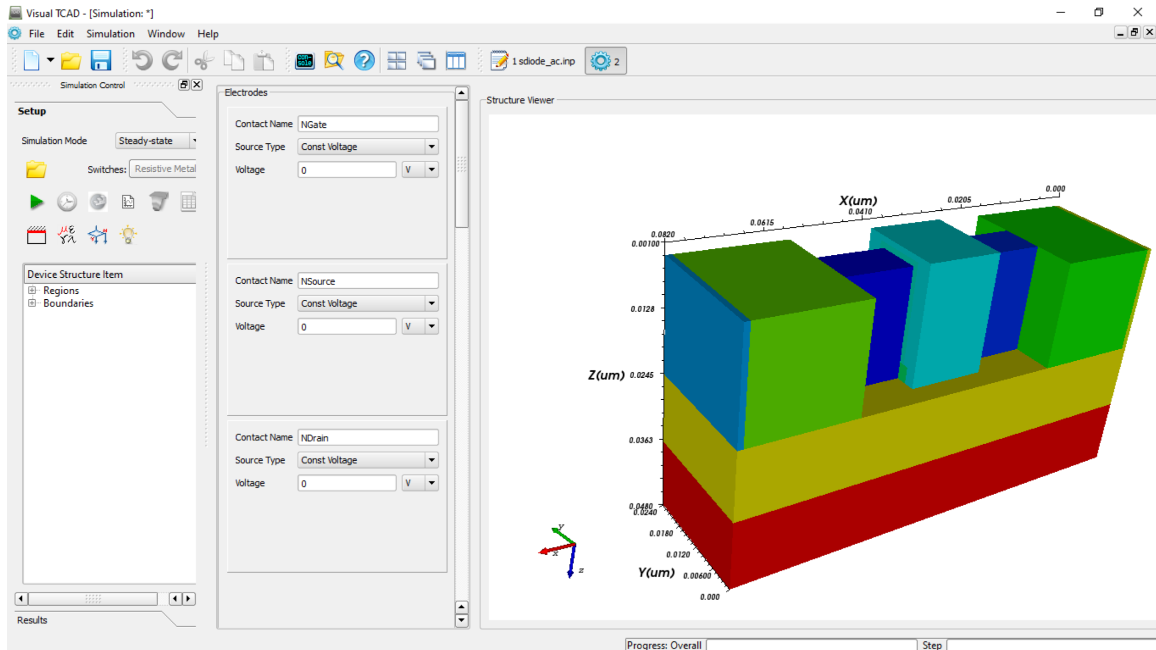


Fig. 7.4 Device simulation on the visual Tcad.

7.2 Simulation Result

In this section we will discuss the various kind of analysis that we can perform on the device and how we can carry out the simulation on the visual Tcad

a) First, we need to load the extension of file .cgns or .tif on the simulation window for loading the device design.
b) Through the console window we can see the progress of loading of the device.
c) Once the device fully loaded on the simulation window then we set the various parameter on which we want to perform the analysis.
d) We can set the electrical property of the device like region resistance value or temperature and thermal property of the device like temperature.
e) In this stage we can set the boundary condition of the device that helpful for understanding the behavior of the device.
f) Figure 7.5 showing the loading of the device on the visual Tcad.

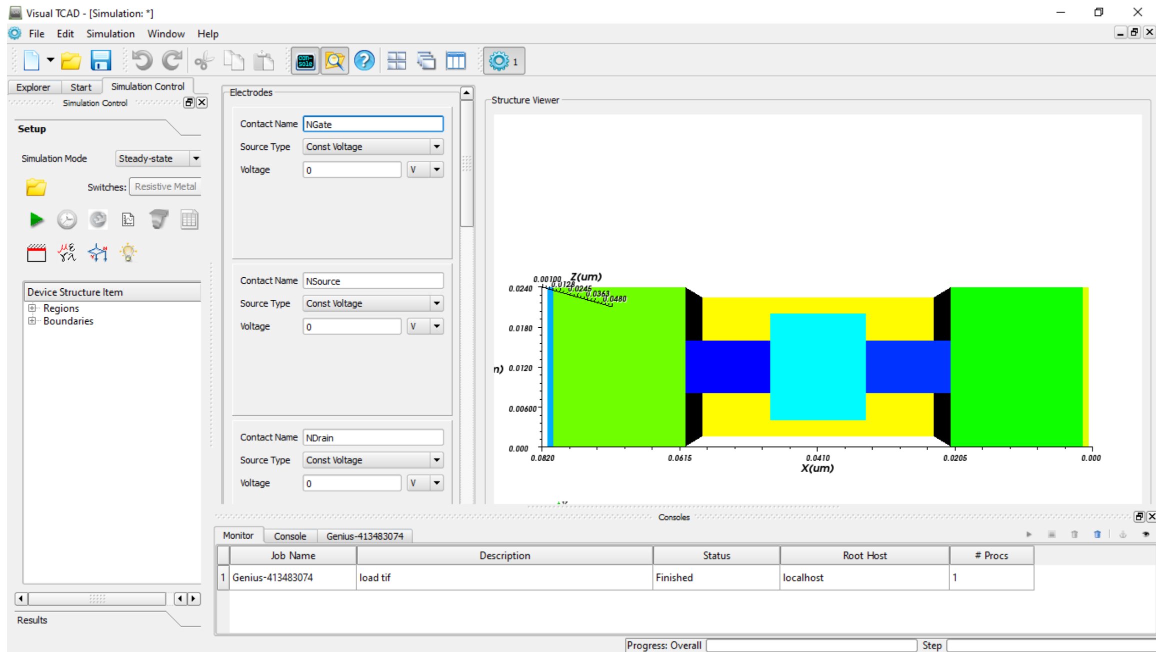


Fig. 7.5 Device loading on the visual Tcad.

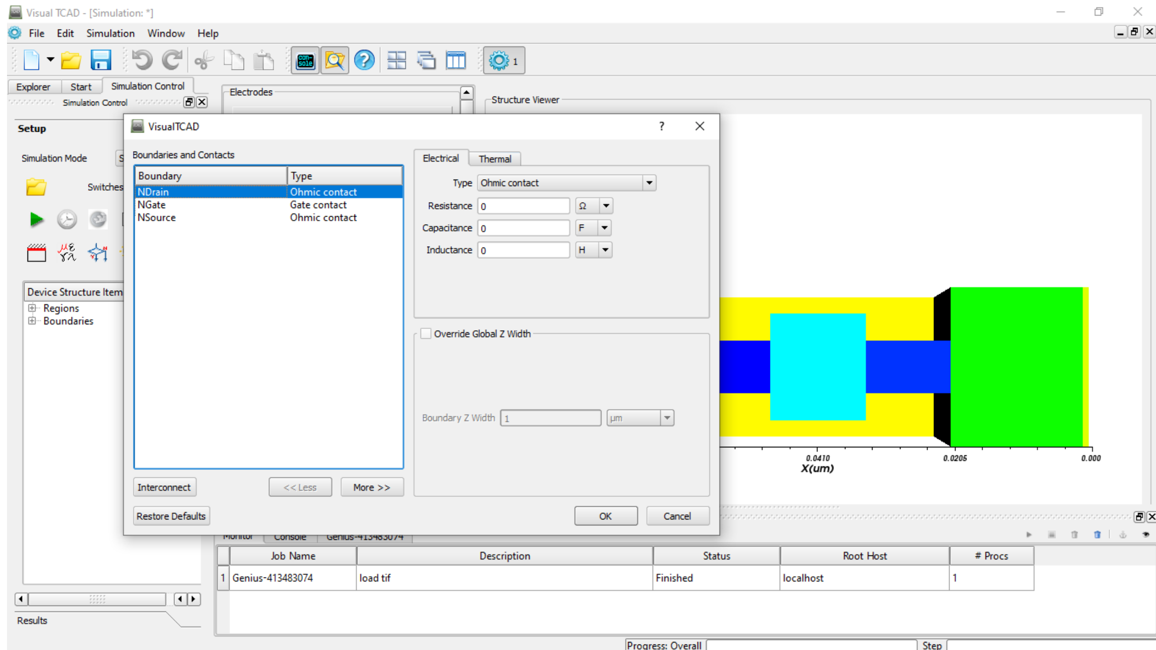


Fig. 7.6 Boundary condition of the device

g) Figure 7.6 showing the boundary condition of the device that we can set for the

simulation purposes.

h) Figure 7.7 showing the interconnect window where we can merge the multiple region of the device into single entity for the simulation purposes and we can set the electrical property like resistance or capacitance and inductance value of the device.

i) Physical model also we can set for the device as shown in figure 7.8. In this stage we can set the vector property of the device like electric field direction or band to band tunneling.

j) In this stage we can set the material model of the device that we used for designing of the device as mentioned in figure 7.9.

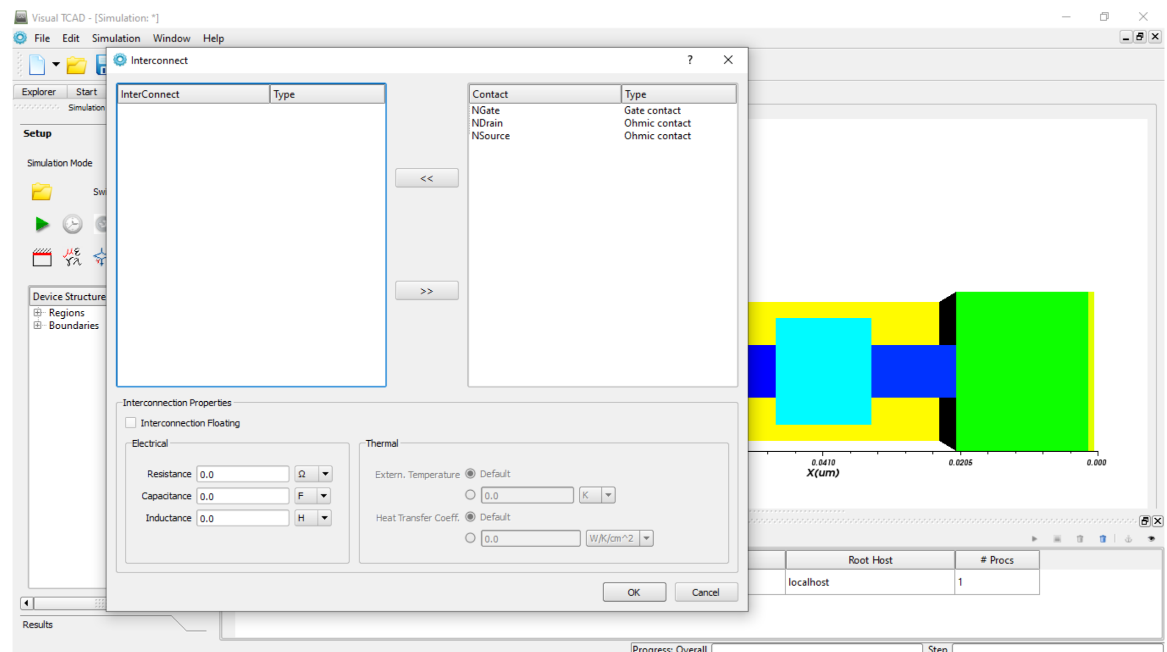


Fig. 7.7 Interconnection of the device terminal

k) In material model we can select the impact, band, optical and basic property of each material that used while designing the device. Visual Tcad gives the flexibility to change the parameter value of these model and simulation will be carried out accordingly.

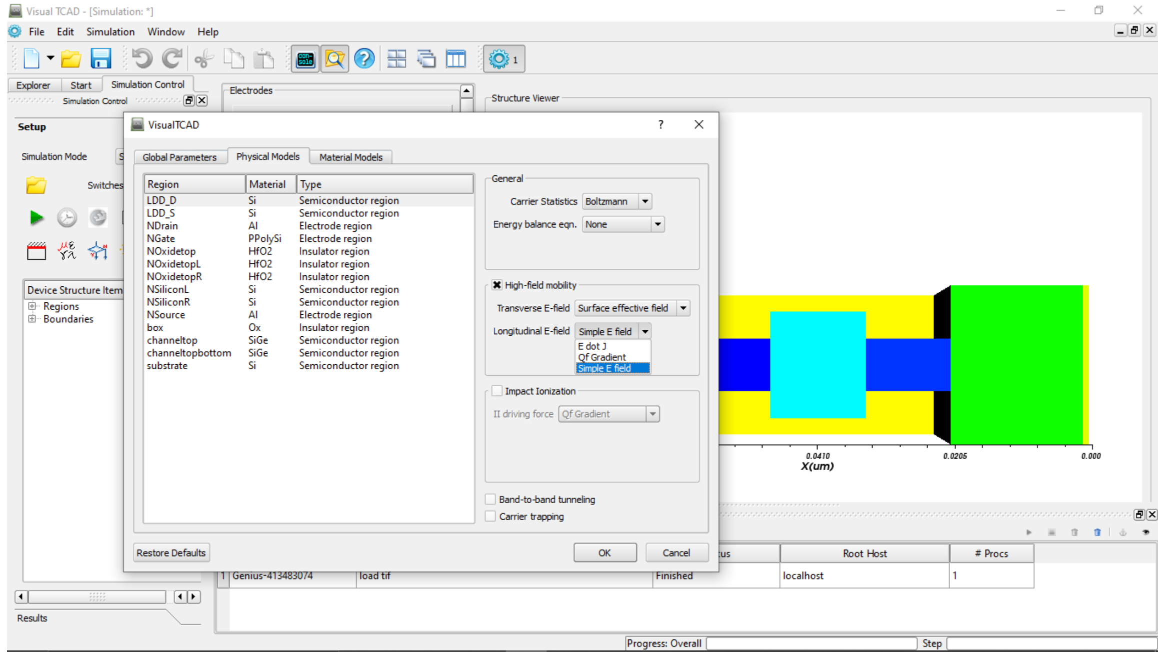


Fig. 7.8 Physical Model of the device terminal

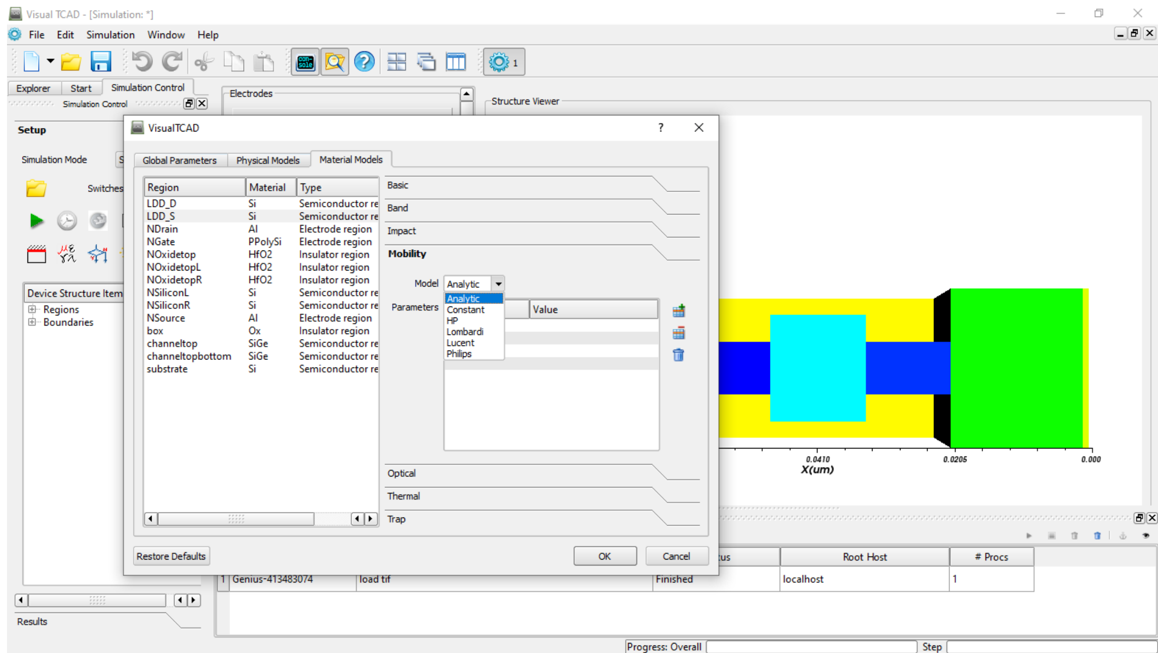


Fig. 7.9 Physical Model of the device terminal

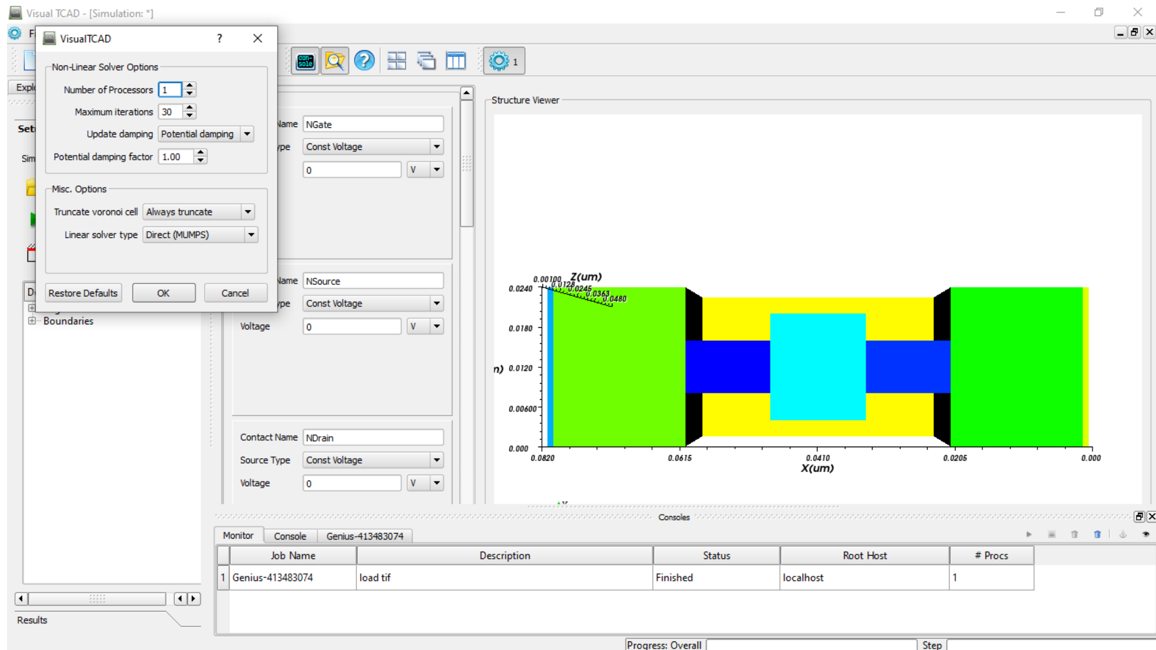


Fig. 7.10 Physical Model of the device terminal.

l) Figure 7.10 shows the solver window that help to simulate the device by using the different model. In visual Tcad four types of linear solver provided for measuring the electrical property of the device on each point.

m) By default, MUMPS linear solver set for the simulation of the device here. On this stage we can set the iteration value that we want to put for the calculation of electrical property of the device.

7.3 Result Analysis

In this part we will discuss the various kind of graph that we can design from the result file after the simulation of the device.

a) Figure 7.11 showing the result file that open in the visual Tcad and from this file we can select the any parameter against which we want to make graph.

b) One limitation of this part is here we can design only the two-dimensional graph of the device.

c) Figure 7.12 showing the graph that we have generated on the visual Tcad.

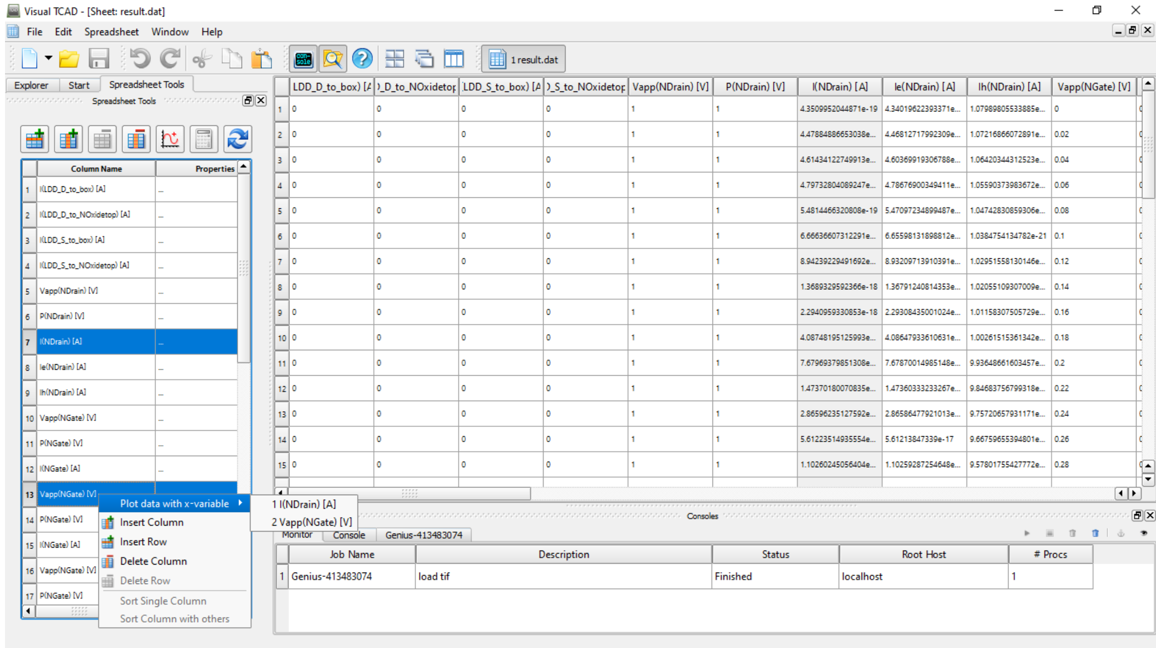


Fig. 7.11 Result File of the device after simulation

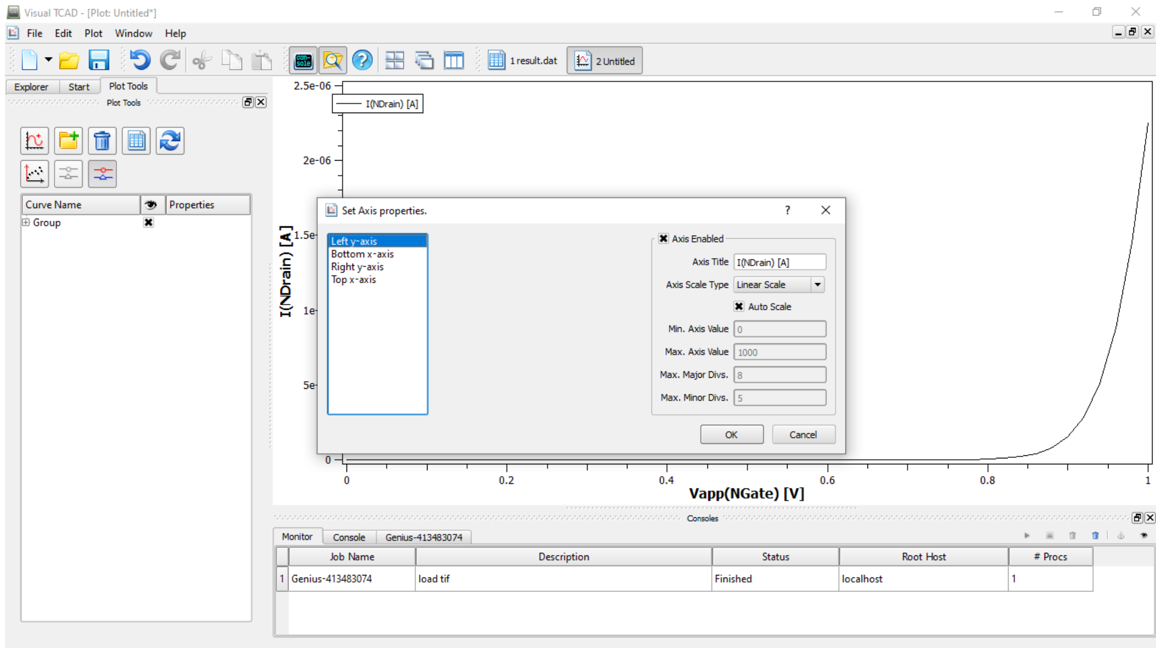


Fig. 7.12 Graph of the device.

d) Figure 7.13 showing the clubbing of the two result if we want show the comparative analysis of the device with any other device.

e) We can plot the three different kind of graph in visual Tcad like linear or logarithmic and absolute logarithmic for the result.

f) In this stage we can use the multiple legend on the graph that will highlight the basic points of the result on the graph.

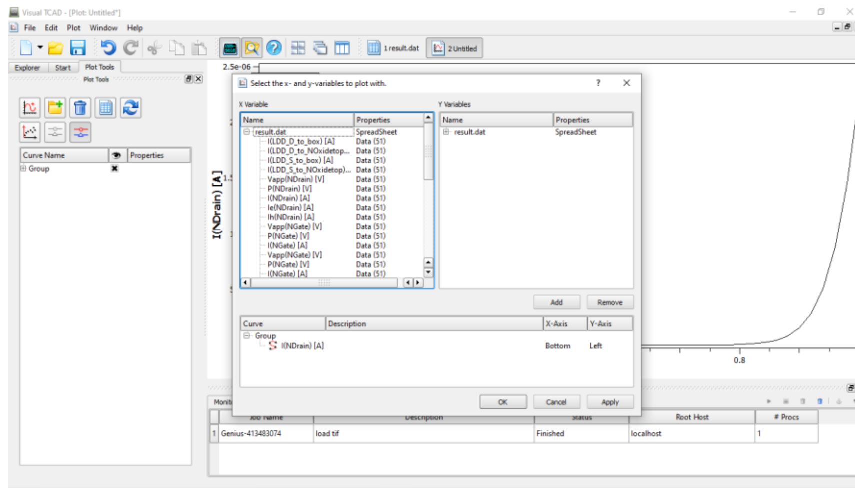


Fig. 7.13 Clubbing of the Graph.

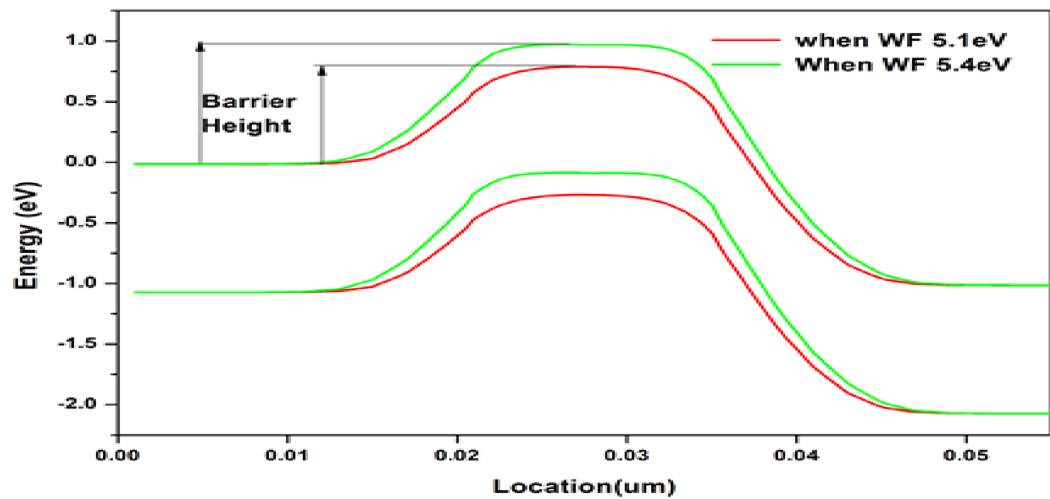


Fig. 7.14 Energy Diagram

List of Publications

Patent Published

[1] One patent published with patent number 09/2022 on 4th March 2022 on the topic of "A NOVEL STACKED T-SHAPED FIN-FIELD EFFECT TRANSISTOR FOR HIGH ONOFFCURRENT RATIO"

Copy Right Published

[1] One copyright published with copyright number 11571/2022-CO/L on 2nd May 2022 on the topic of "Design and Optimization of Heterojunction Multigate FinFETs."

Journal

[1] Verma, S., Tripathi, S.L. Impact & Analysis of Inverted-T shaped Fin on the Performance parameters of 14-nm heterojunction FinFET. *Silicon* (2022). https://doi.org/10.1007/s12633-022-01708-5

[2] Verma, S., Tripathi, S.L. Effect of Mole fraction and Fin Material on Performance Parameter of 14 nm Heterojunction $Si_{1-x}Ge_x$ FinFET and Application as an Inverter. *Silicon* (2022). https://doi.org/10.1007/s12633-021-01592-5.

[3] Verma, S., Tripathi, S. L., & Kumar, N. (2019). Comparative Analysis of FinFETs Device on Technology Scale of 14nm vs 20nm. *Think India Journal*, *22*(17), 2745-2752. Retrieved from https://thinkindiaquarterly.org/index.php/think-india/article/view/17026.

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International Conference

[1] S. Verma, S. L. Tripathi and M. Bassi, "Performance Analysis of FinFET device Using Qualitative Approach for Low-Power applications," *2019 Devices for Integrated Circuit (DevIC)*, 2019, pp. 84-88, doi: 10.1109/DEVIC.2019.8783754.

[2] Shekhar Verma and Suman Lata Tripathi "Process variation and analysis of FinFET for low-power applications" 2020 *IOP Conf. Ser.: Mater. Sci. Eng.* **872** 012015 https://doi.org/10.1088/1757-899x/872/1/012015.

Book Chapter

[1] S. Verma, S. L. Tripathi, "Performance Analysis of FinFET device Using Qualitative Approach for Low-Power applications Impact of temperature on 14 nm FINFET with high-K different oxide material," *2021 Intelligent Circuits and Systems* 2021, pp. 181-186, DOI: 10.1201/9781003129103-30, eBook ISBN9781003129103

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