MODELLING, SIMULATION AND VALIDATION OF ACTIVE SEMICONDUCTOR DEVICES USING FLOATING ADMITTANCE TECHNIQUE

A Thesis

Submitted in partial fulfilment of the requirements for the award of the degree of

DOCTOR OF PHILOSOPHY

in

Electronics and Communication Engineering

By

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2022

DECLARATION

I declare that the thesis entitled, **"Modelling, Simulation and Validation of Active Semiconductor Devices using Floating Admittance Technique"** under the guidance of **Dr. Kamal Kumar Sharma,** Professor, School of Electronics and Communication Engineering, Lovely Professional University, Punjab, India, No part of this thesis has formed the basis for the award of a degree or fellowship previously.

I further declare that there is no falsification or manipulation in terms of research materials, equipment or process, experiments, methods, modelling, data, data analysis, results, or theoretical work.

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CERTIFICATE

It is to certify that **Sanjay Kumar Roy (41900208)** has completed the scientific formulation of the thesis entitled**, "Modelling, Simulation and Validation of Active Semiconductor Devices using Floating Admittance Technique"** under my guidance and supervision. To the best of my knowledge, the present work is the result of their original investigation and study. No part of the thesis has ever been submitted for any other degree at any University.

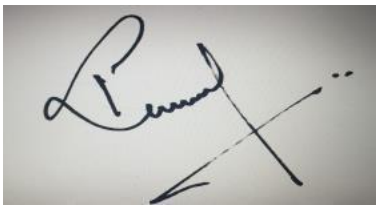

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Table 1 List of Figures:

Table 2 List of Abbreviations

S.N.	Abbreviations	Stands for
1	FAM	Floating Admittance Matrix
2	BJT	Bipolar Transistor
3	FET	Field Effect Transistor
4	MOSFET	Metal Oxide Semiconductor Field Effect Transistor
5	A_v	Voltage gain without source resistance
6	A_{vs}	Voltage gain with source resistance
7	A_i	Current gain
8	A_P	Power gain
9	R_{in}	Input resistance
10	R_o	Output resistance
11	CE	Common Emitter
12	CB	Common Base
13	CC	Common Collector
14	CS	Common Source
15	CD	Common Drain
16	CG	Common Gate
17	I_B, i_b	DC and AC base currents
18	I_C, i_c	DC and AC collector currents
19	I_E, i_e	DC and AC emitter currents
20	V_B, v_b	DC and AC base voltages
21	V_C, v_c	DC and AC collector voltages
22	V_E, v_e	DC and AC emitter voltages
23	V_{CC}, V_{DD}	DC collector and Drain supply voltages
24	$\pm V_{BB}$	Base supply voltage
25	$-V_{EE}$, V_{SS}	Emitter and Source supply voltages.
26	Int. J.	International Journal

Abstract

The dynamics of any system, whether *mechanical, electrical, thermal, economical, biological* and so on, may be described in terms of difference or differential or integral equations. Such equations may be obtained by using physical laws governing a particular system, for example, Newton's laws for mechanical systems, Kirchhoff's laws for electrical systems, etc. We should continually keep in mind that deriving a reasonable, if not the best, mathematical model is an essential part of the complete analysis of any system.

The modelling assumes many different forms. Depending on the particular system and circumstances, one model may be better suited than others in given conditions. For example, using the state-space model in the optical control modelling is advantageous. On the other hand, the transfer function representation may be more convenient than any other for a transient response or the frequency response analysis of single-input-single-output, linear time-invariant systems. After developing the mathematical model of a system, various analytical and computational tools can be used for analysis and synthesis purposes.

Models of any system in science come in a wide variety of forms. The well-known modelling expert, Babour G. Ian, lists four types of models in his extensive discussion of models. According to him, different modelling types are categorised under one of the following methods: *material model, mathematical models, logical models, theoretical models*. The simplified scaled-down or up miniatures, e.g., the wind tunnels, hydrodynamic models or analogue models, e.g., an electric circuit having the same behaviour as a mechanical system of springs & dampers, are available in the literature. They are helpful when it is too difficult to experiment on the actual system or when the mathematical equations are unknown or too complex to solve. Some models can be better than others, but that model also gives an idea of the functioning of the physical behaviour of the system. The *model* is a *mental construct* of the physical behaviour of any system.

A set of equations describes the mathematical model of a system's behaviour's functioning. We focus on developing dynamic models that will ultimately result in

differential equations. How to represent such differential equations in the form of a block diagram? It is not possible to develop a precise model of any Physical system. Many processes cannot be modelled even. So Model error or model **uncertainties** occur. Even if a model describes a part of the reality, it can be very useful for analysis and design if it describes the dominating dynamic properties of the system. Some models are based on the physical principles of the system. Models can also be developed from experimental (historical) data. This way of mathematical modelling is called system identification.

Most of the books on electronic circuits deal with the analysis of various types of passive and active circuits (containing BJTs, FETs, MOSFETs, and Operational Amplifiers) in the conventional way of replacing the BJTS, FETs, MOSFETs, and Operational Amplifiers by its small-signal equivalent circuits. Then the well-known tools of KCL, KVL, Thevenin's, Norton's etc., are taken to advantage for the solution of the given network. Chirlian. P. "Electronic Circuits-Physical Principles Analysis and Design" proposed a generalised network analysis method containing the BJTs, FET, MOSFETs, and Operational Amplifiers.

The model proposed by Chirlian was so general that this method seemed to be very cumbersome. The proposed work defines different functions of electronic circuits, the active ones, to solve them elegantly using the Floating Admittance Matrix (***FAM)*** approach. This matrix is called floating as because the reference terminal (ground) for the potential is arbitrary and lies outside the selected multi-pole network. For any network solution, the floating admittance matrixes of active and passive networks are written separately and then merged according to the node numbers. Once the overall floating admittance matrix of the complete amplifier or any circuit (active device and passive components) is obtained, its various transfer and self-port functions such as the input impedance (resistance), the output impedance (resistance), the voltage gain, the current gain and the power gains are obtained in terms of the co-factors of the derived floating admittance matrix. The voltage-current relationship for even complicated passive networks is usually linear, and hence, the solution of such a network is simple, using well-known tools like the KCL, the KVL, the Thevenin's, the Norton's etc.

On the contrary, electronic devices such as the BJT, FET, MOSFET, and Operational Amplifier are governed by current-voltage relationships that are typically

nonlinear and somewhat complex. In general, it is not easy to analyse devices that obey nonlinear equations because there are much less developed design methods for circuits that include these devices. The basic concept of modelling of an electronic device is to replace the device as the circuit with linear components that approximate the voltage-current characteristics of the device as the *piecewise linear* models. A model can then be defined as a collection of simple components or elements used to represent a more complex electronic device. Once the device is replaced in the circuit by the model, well-known tools for the circuit analysis can be applied.

The necessity of modelling for engineering lies in the very nature of technology and its advancement. As technology approaches its limit, i.e. fundamental changes do not occur as used to occur previously, and the engineers have to find a suitable substitute.

Our aim is to simplification of the analog circuit combining BJT, FET, MOSFET, and their combinations along with resisters and capacitors using properties of the Floating Admittance Matrix (FAM) technique. The gist of the development of the Thesis reviles as following.

1) We have developed formulae for the Voltage gain, Current gain, Input Impedance, Output Impedance, and Power Gain using our technique (FAM) for all types of Circuit using BJT, FET/MOSFET, Op-Amp including resistances and Capacitances in the form of its cofactors.
2) Solving Complicated Circuits such as Twin-T and Bridge T Networks is a very good example of applying our technique for achieving a simple solution.
3) The Zero-Sum Property of all elements of any Row or any Column of FAM satisfies the superposition theorem.
4) Once the FAM of any network is written, it is easy to find out transfer or self-port functions between as many ports as possible.
5) We have shown that the FAM technique to solve cascaded or cascoded circuits become very easy with respect to conventional Methods.

Organization of the Thesis

The thesis has been divided in six chapters. The first chapter deals with the modelling technique vis-à-vis literature survey. All types of transfer (voltage gain, current gain, power gain) or self-port functions (input and output resistances) have been derived in Chapter-2 in the form of cofactors of the floating admittance matrix of any circuit. Chapters-3 and 4 show the beauty of the FAM to obtain all types of transfer and self-node functions easily in the form of cofactors only of the BJT and the FET/MOSFET amplifiers. Chapter-5 discusses the drawback of the four terminal MOSFET, if its body is not connected to the source terminal and this effect is included on its small-signal model. Thus, all the four terminals of a MOSFET play active role in functioning of the MOSFET. The sixth chapter is devoted the discussion and conclusion derived from Chapter-1 to Chapter-5.

Chapter 1

Modelling: Review of Literature

1.1 Introduction

We start with the question 'what is modelling'? Modelling is the process of making models. Its most straightforward answer would be that models are often simplified versions of a complicated one. We might have played with a small toy car during our childhood. It can be called a model of an actual car. They gave us a unique idea of what a real car looks like, but they are much smaller and oversimplified. A model cannot always be accurate. We must realize this so that we do not build up an incorrect idea about something.

One way of defining the model is that it is the essential theoretical construct of anything. It exists in our brain, and we use it to explain how the phenomena of any object work. What is gravity? It is almost like a black box or an abstract. We cannot touch it, but we get to develop models that help us to predict it. What was the gravity for Einstein? What was he doing when the model was already developed by Sir Isaac Newton? He was looking at the construct of the model. He was able to improve on that model based on the data he had received. So why does an apple fall to the Earth? It is not that there is some magical force pulling it there. What did Einstein say that they are wrapping time and these objects are travelling through the shortest path? Was he able to confirm that using data? Yes.

The model of any system might be of different in nature. It is important to note that a model is not the real world but merely a human construct to understand real-world systems better. In general, all models include information input, an information processor, and the output of expected results.

The models are inherently inexact as they only approximate natural phenomena. The mathematical description may be imperfect, and/or our understanding of the phenomenon may or may not be complete. The mathematical

input parameters used in models to represent real processes might be uncertain as these input parameters are empirically determined or represent multiple input/output. Additionally, the initial conditions and/or the boundary conditions in a model may not be exactly known.

Despite the above-stated weaknesses, models are effective tools for describing natural processes. Often, models are the only means to extrapolate to large spatial scales. Because of their importance in the earth sciences, we assess model accuracy by calibrating and validating models. To quantify the model's uncertainty, we correlate the result's sensitivity to the model parameters.

It is well known that an atom is the smallest part of the element that can further be divided by nuclear reactions only. An atom is an ensemble of the smallest particles of energy that make up everything on the Earth. A variety of models have been used over the past decades to speculate on how an atom works and what particles it contains.

Before more discussion here, we describe first, the 4-research objectives to formulate the problem statement for the thesis. The third and the fourth objectives have been implemented in the papers published, which forms the basis of the problem statements.

1.2 Objectives

Objective 1: ***Design to formulate the mathematical model for active semiconductor devices.***

The proposed technique of the floating admittance matrix is an elegant mathematical modelling approach for both active and passive circuits. The fundamental benefit of the floating admittance matrix approach is that the algebraic sum of all elements in any row or column producing zero serves as a preliminary check that the circuit analysis and design process is going in the right direction. The remaining entries in the floating admittance matrix whole circuit incorporating passive components can be written by inspection without much difficulty once the floating admittance matrix of the active device is understood. This technique can be used to avoid performing a rigorous equivalent circuit analysis with more active devices in any circuit. Mathematical modelling should be the foundation of every educational system, especially engineering

education, because it shows where to put the right tools to get the job done. It is needless to say that stakeholders are students, guardians, faculty positions, management groups, and, very importantly, the industrialist as employers and others. These variables are correctly set in the mathematical model to achieve the desired outcome. If the desired result is not reached for a given set of inputs from all stakeholders, the mathematical modelling is revisited, with fine-tuning of one or more variables increased or decreased to get the desired result. As a result, mathematical modelling variables should be fine-tuned so that the desired result is attained quickly and elegantly. (A paper as presented on "Mathematical modelling of semiconductor devices and circuits: A review," 3rd International Conference on Intelligent Circuits and Systems (ICICS 2020) held on June 26-27th, 2020, organis*ed by "The School of Electronics and Electrical Engineering" at Lovely Professional University, Punjab (India) DOI:10.1201/9781003129103-14*).

Objective 2: ***Performance validation of the developed models using the floating admittance technique*****.**

Problem Statement: Using the floating admittance matrix approach, all forms of transfer and self-port functions such as voltage gain, current gain, input resistance (impedance), output resistance (impedance), and power gains of any complicated circuit may be easily generated. The superposition theorem is nicely satisfied by this FAM approach. Because the method only uses co-factors from the created FAM, the computer can be used for complex networks.

Work Explanation: The conventional approach to a mathematical model of the actives devices such as BJT, FET, MOSFET, and Op. Amp uses its equivalent circuit as per the requirement of (a) either large signal or small-signal models, (b) low frequency or high-frequency models, so and so forth. The typical way of equivalent circuit approach becomes quite onerous for cascaded or cascoded connections of several devices (BJTs. FETs, MOSFETs, and Op Amps) or combinations of BJTs & FETs, MOSFETs, and Op Amps in any circuit. "Mathematical Modelling of Simple Passive RC Filters Using (FAM) Floating Admittance Technique" (***2020 IEEE International Conference for Innovation in Technology (INOCON) Technically Cosponsored by IEEE Bangalore***

Section 06th - 08th November 2020 *DOI: 978-1-7281-9744-9/20/$31.00 ©2020 IEEE)* was presented (IEEE, SCOPUS).

In this article, the problems relating to modelling simple electrical circuits consisting of resistors, capacitors, voltage sources, and current sources were taken up. Generally, we avoid using passive inductors because the planar spiral inductors are heavy, take more space, and dissipate considerable power with respect to resistors and capacitors. On the other hand, simulated inductances are frequently utilised in filters to achieve good performance, but that is the realm of active filters. Mesh equations, node equations, or Thevenin or Norton equivalent methods are used to solve fundamental networks consisting of resistances (R), capacitances (C), voltage sources, and current sources. These techniques do not conform to the state-space form of the mathematical model or, even later, cannot be converted by any means to the state space form.

The fundamental understanding of transfer function characterisation provides sufficient information to determine whether proper functioning has been attained. The circuit structure's input impedance and output impedances, power supply coupling and uncoupling, circuit component change, and other dynamic behaviour are all significant elements.

Objective 3: ***Simulation and analysis of developed models using MATLAB/ SIMULINK/*** *LTSpice.*

Problem Statement: The analysis becomes lucid and corroborates the transfer functions obtained in the literature. These transfer functions are solely dependent on the co-factors of FAM of any circuit, whether active, passive or a combination of both. The floating admittance matrix has the distinct advantage of being able to be written by inspection for basic circuits.

Work Explanation: The modelling and simulation of bridge -T network has been carried out using MATLAB's Simulink system environment. This paper provides simulated and numerical validation of two forms of bridge -T network used for band pass filter. The MATLAB program developed for the transfer function for both types of the RC bridge-T network are plotted in the form of magnitude and phase w.r.t. frequency. The input and output impedances are derived and drawn using the FAM technique.

"Mathematical Modelling and Simulation of Band Pass Filters using the Floating Admittance Matrix Method" (WSEAS TRANSACTIONS on CIRCUITS and SYSTEMS E-ISSN: 2224-266X DOI: 10.37394/23201.2021.20.24) was another paper published (SCOPUS).

Objective 4: ***Comparative analysis of floating-point admittance technique with existing methods for active semiconductor devices***

Problem Statement: The traditional analysis approach employs one of the widely used tools, such as KCL, KVL, Thevenin's, Norton's, and others, depending on the circuit's suitability, whether active or passive. The floating admittance matrix technique proposed here is unique, and it may be used to any type of circuit. The matrix partitioning method is used to benefit the difficult network. The fact that all elements of any row or column add up to zero gives you the confidence to go deeper into analysis or re-observe the circuit at the first equation to save time and energy. **Work Explanation**: The floating admittance mathematical model presented here is so simple that anybody with slight knowledge of electronic devices, but an understanding of matrix maneuvering, can analyse the circuits to derive all types of transfer functions provided the parameters of devices are known to them. The floating admittance matrix model is used to analyse and subsequently build any circuit. It is based on pure mathematical maneuvering of matrix elements of the circuit. All transfer or self-port functions are defined as the ratios of co-factors of the first and or second order of the FAM. The FAM approach's mathematical modelling allows the designer to adjust their design style at any analysis stage comfortably.

"Unique Analysis Approach to Bridge-T Network using Floating Admittance Matrix Method" (INTERNATIONAL JOURNAL OF CIRCUITS, SYSTEMS AND SIGNAL PROCESSING Volume 15, 2021 DOI: 10.46300/9106.2021.15.140) was published (SCOPUS)**.**

Another paper, "**Unique Analysis Technique for 4-Terminal MOSFET Amplifiers using Floating Admittance Matrix Approach"** ***2022 International Conference for Advancement in Technology (ICONAT) Goa, India. Jan 21-22, 2022,*** **DOI: 978-1-6654-2577-3/22/$31.00 ©2022 IEE** was published (IEEE, SCOPUS)**.**

The paper presents an elegant technique of analysing the 4-terminal MOSFET amplifier circuit. The proposed technique helps in writing the floating admittance matrix (FAM) of any circuits by inspection once the FAM of electronic devices (BJT/FET/ MOSFET) is known. The matrix partitioning technique suits an extensive network well using the proposed technique. The proposed floating admittance matrix technique does not assume any reference terminal. For this reason, it is called the floating admittance matrix approach.

1.3 Mathematics in modelling

Mathematics helps engineers form, analyse, and optimize the functionality of the phenomena to design and develop a system. Mathematics enhances teachers' and students' ability to engage in abstract thinking and arouses their imagination. Innovative engineers and scientists are creative, and creativity is essential for strong imagination and abstract thinking. As a result, a successful innovative engineer is likely to have a solid understanding of mathematics.

1.4 Modelling of physical environment

Modelling also refers to the study of processes and items in one physical environment utilising processes and objects from another physical environment as models to replicate the system's behaviour. Collins, Brown, and Newman [1] believe modelling shows how and why an expert does a task. It is one method that is critical to expert teaching regarding any procedure or process.

The complexity of the processes in modern engineering, economics, and other systems is so powerful that they expect to have useful information and the characteristics of the complete systems and predictions of the consequences of their behaviours.

Modelling is a powerful technique that may be used in various fields. It's "a natural requirement of practically any engineering course," according to the author Crawley et al. [2]. *Massoud Moussavi* [3] in 1998 submitted a Ph.D. dissertation on Mathematics, Modelling, and Modular Curriculum. Grinter [4] proposed retraining programs in Engineering for *Johnson & Wales University and School of Technology* to emphasize the maneuverability of *mathematical models* in the curriculum.

Modelling is part of the management process nowadays at every stage of human involvement. Engineering colleges/institutes should, for example, investigate the efficiency and efficacy of an engineering curriculum by:

- Predict the program performance of the proposed curriculum.
- Evaluate and assess the proposed curriculum.
- Identify the points of deficiencies.

Modelling becomes a powerful tool to accomplish these tasks for them. Fig. 1.1 shows a typical model for an effective engineering education program.

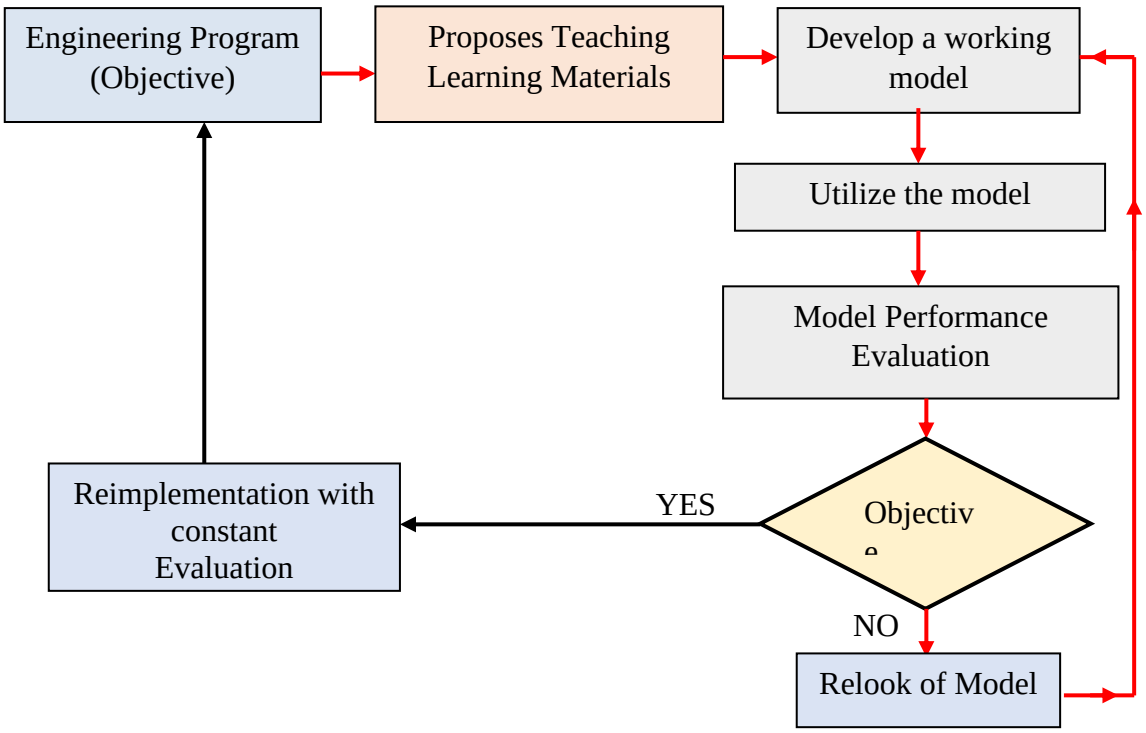

Fig. 1.1 Model of an Effective Engineering Education Program

This model helps engineering education to continuously evaluate their proposed program, identify its deficiencies, and improve and modify it in a timely manner.

To model an effective engineering program, as an example, for Electronics Engineering students, we have first to define the Program's Educational Objectives as;

(a) To enrol students having a basic knowledge of *mathematics* and science.

(b) To train students so that they will be able to maintain and handle electronics systems, equipment, and component parts with creativity and critical spirit in

the technological development as per necessity and viability, globally, and especially for our country.

(c) To enable the student to achieve employment in Electronics, Communication, and IT-related industries with appropriate title and compensation.

(d) To enable the student to innovate, design, and develop hardware and software components and equip the student with technical and communication skills to function in national/international/multi-cultural corporations and organizations.

(e) To build strong fundamental knowledge amongst students to pursue higher education and continue professional development in Electronics and other related fields.

The syllabi's design comes into the picture as per the stated objectives with the target set. The working model defines the mechanism to meet the targeted objective. The working model is divided into many subheadings: Assignments, Quizzes, mid-term examinations, end-term examinations, seminars, projects, etc. The marks distribution is as per the weightage of all such subheadings assigned. The students go through this process, and their performance is analysed to suit the stated objectives. If the *working model* matches 75% to 80% of the objective set, then we assume the working model is successful. Even if the desired model results in acceptable limits, we try to input components from all stakeholders, such as students, alumni, guardians, industrialists, etc., to improve the model management. If the model does not result in an acceptable limit, we do in-house brainstorming, inviting experts to strengthen the program objectives to match the desired result.

1.5 Advantages of Modelling

Modelling provides several advantages for engineers at the design and development stage. The modelling helps engineers to evaluate the unknown properties of objects. Modelling may become the sole viable approach for engineers to design, develop, and optimise new systems due to limited resources and options. Modelling is a valuable tool for engineers to avoid the consequences of bad technical decisions. Let us take another example of the automated manufacturing of an automobile. The

decision of optimum weight, speed, fuel consumption, etc., are designed and tested on the computer, and then only the industrialists go to manufacture the automobile. What should be the weight of the automobile if the break is suddenly applied when it is running at a certain speed so that it does not overturn? Many more iterations are performed on the computer before the final design is accepted for manufacturing.

Engineers may proceed in the following ways with regard to methods and methodology. They aim to acquire as much relevant information as possible for each challenge. Then they look for connections between the various themes to create a workable model. They then propose solutions that must be optimised for a variety of factors such as time, cost, size, and performance. According to Rodencker [5], the designing process is "a transition of knowledge, leading from the abstract to the concrete." He proposed eight rules for developing a technical system that starts by defining and abstracting the requirements.

Rodencker's rules are:

(a) Clarify the task (the required relationship)
(b) Establish the function structure (the logical relationship)
(c) Choose the physical process (the physical relationship)
(d) Determine the embodiment (the constructional relationship)
(e) The appropriate calculation can check the logical, physical, and constructional relationships.
(f) Eliminate disturbing factors and errors.
(g) Finalize the overall design.
(h) Review the chosen design.

What Rodencker tried to establish is a model that employs *mathematics* to design a technical system. Rules' 'd', 'e,' and 'f' are nothing but formalizing the system using mathematics. In fact, these three rules are the heart of the design process. They show that a scientific, efficient, and cost-effective design would be possible only by the employment of *modelling*.

Electronic processes and *objects*, in general, are used as *models* because electronic systems have an unusual combination of properties and characteristics. The electronic process parameters and the structure of the connection between individual

elements can also be changed easily, explicitly, or implicitly. Along with rapid progress in the field of electronics, the calculation and designing of electrical devices and networks have become a much more sophisticated and challenging task than ever been taken.

Consequently, Electronic engineers must continuously improve the mathematical description, numerical analysis, and computer-aided design of electronic devices and systems. *Modelling* is the only effective technique that responds to the current marketplace, demanding fast and inexpensive design and production methods.

Mathematical *modelling* helps electronic engineers extensively to study and investigate the dynamic behaviour of electrical networks. Verlan [6] has developed a mathematical model called an integral equation. This is essentially the procedure which finds the integral mathematical relationships between the known source of data and unknown network parameters. The following brief description of Verlan's work depicts how *mathematical modelling* helps engineers study a system's behaviour to further develop a more accurate system.

The RC circuit can act as a simple integrator or a first-order low-pass filter. The signals of low frequencies pass approximately unchanged through the filter, while signals of high frequencies are filtered out (stopped). We will find the *mathematical model* to analyze it relating V_{in} and $V_{out} = V_C$. We start by considering the following RC circuit of Fig. 1.2.

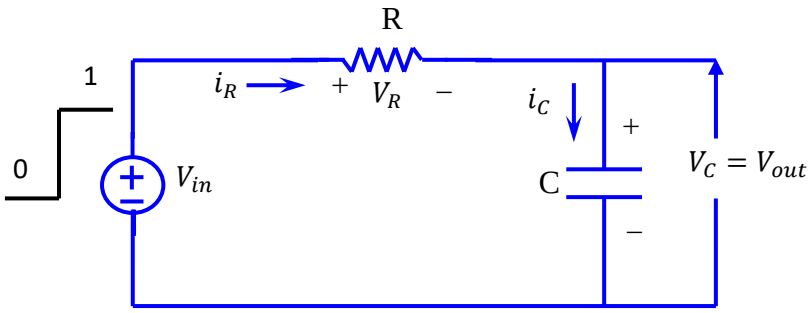

Fig. 1.2 Circuit Model of a passive RC Integrator

We apply Kirchhoff's voltage law (KVL) in the circuit, which contains the input voltage terminals, the resistor, and the capacitor, considering the voltage drop positive in the clockwise direction. The non-homogeneous equation delineates the RC circuit's

response to a step input to the register's interconnected terminals and capacitance.If a step voltage (V_{in}) is applied at $t = 0$, what is the form of the output?

Writing the KVL yields

$$-V_i + V_R + V_C = 0 \quad (1.5)$$

If a step voltage (V_{in}) is applied at $t = 0$, what is the form of the output?

For a capacitor $i_C = C\frac{dV_C}{dt}$ (1.6)

Current through the resistor = $i_R = \frac{V_R}{R}$ (1.7)

Since there is a single path for the current through the resistor and the capacitor, we can write

$$i_R = i_C \quad (1.8)$$

Then, $i_R = \frac{V_R}{R} = i_C = C\frac{dV_C}{dt}$ (1.9)

$$V_R = RC\frac{dV_C}{dt} \quad (1.10)$$

Substituting $V_R = V_{in} - V_C$ and rearranging yields

$$RC\frac{dV_C}{dt} = V_R = V_{in} - V_C \quad (1.11)$$

Now separating the variables as

$$dt = RC\frac{dV_C}{V_{in}-V_C} \quad (1.12)$$

Integrating $\int dt = RC\int \frac{dV_C}{V_{in}-V_C}$ (1.13)

Thus, $t = -RC\ ln\{V_{in} - V_C\} + k(constant)$ (1.14)

For $t = 0, V_C = 0$ (1.15)

Slowly the charge builds up across the capacitor from zero value.

$0 = -RC\ ln\{V_{in} - 0\} + k$

$k = RC\ lnV_{in}$ (1.16)

Now, $t = -RC\ ln\{V_{in} - V_C\} + RC\ lnV_{in} = RC\ [ln\{V_{in} - (V_{in} - V_C)\}]$ (1.17)

$$\frac{t}{RC} = ln\{V_{in} - (V_{in} - V_C)\} = ln\frac{V_{in}}{V_{in}-V_C} \quad (1.18)$$

$$exp\left(\frac{t}{RC}\right) = \frac{V_{in}}{V_{in}-V_C}$$

$$\{V_{in} - V_C\} = \frac{V_{in}}{exp\left(\frac{t}{RC}\right)}$$

$$V_C = V_{in} - \frac{V_{in}}{exp\left(\frac{t}{RC}\right)} \quad (1.19)$$

$$V_C = V_{in}\left[1 - \frac{1}{exp\left(\frac{t}{RC}\right)}\right] = V_{in}\left[1 - exp\left(-\frac{t}{RC}\right)\right] \quad (1.20)$$

If we substitute $t = 0$ in Eq. (1.20), $V_C = V_{in}[1 - exp(-0)] = 0$ (1.21)

This condition verifies that at the moment $t = 0$, the capacitor was fully discharged.

At $t = \infty, V_C = V_{in}[1 - exp(-\infty)] = V_{in}$ (1.22)

Equation (1.22) reveals that the capacitor is charged to the input voltage's full value after a considerable time. The plot of this response for unit values of capacitor C, resistor R, and input step voltage V_{in} is given as in Fig. 1.3.

The RC is the product of resistance R (Ohms), and capacitance C (Farads) has the unit of seconds and is always constant. The Greek letter τ (tau) is usually used to denote this variable.

The output voltage (V_C) reaches 63.2% of its final value in 1 time constant (1 second in this case). The time taken to reach a particular value is related to the number of time constants given in Table 1.1.

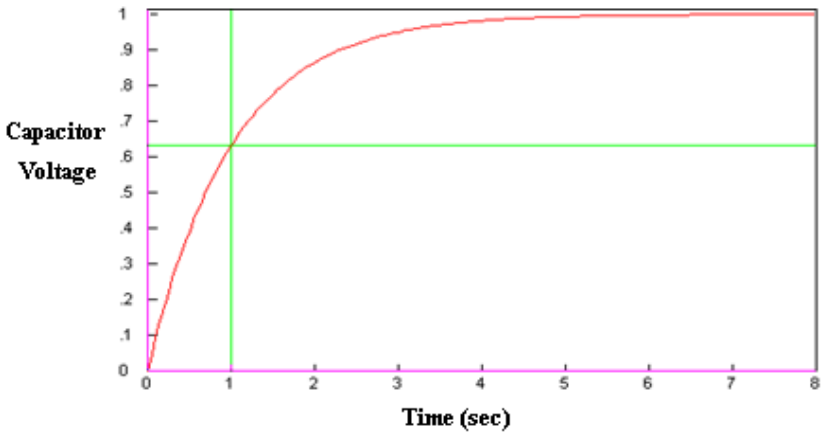

Fig. 1.3 Response of RC Integrator for input step

Table 1.1 Required number of time constants to reach a proportion of the final value						
τ	2τ	3τ	4τ	5τ	6τ	7τ
63.2%	86.5%	95.0%	98.2%	99.3%	99.7%	99.9%

Reducing the value of τ (i.e., reducing R or C) means that the output will change faster, and any given voltage will be reached sooner.

Thus, the integral equations provide a most common and convenient means to examine and determine the inherent and the induced part of the components of processes that may take place in linear circuits. The use of integral equations for describing electrical networks' dynamic behaviour results in several specific methods for their quantitative and numerical analysis.

Another straightforward example of mathematical modelling is the relationship between the voltage across and current through a resistor. The relationship between current and voltage for the resistor, capacitor, and inductor is depicted in Fig. 1.4.

If the current through the component is I (A) and the voltage drop across the component is v (V). The current and voltage are then related as follows.

Resistor→ $Ri(t) \rightarrow Ohm's\ Law$ (1.23)

Capacitor → $i(t) = C\frac{dv(t)}{dt}$ (1.24)

Inductor → $v(t) = L\frac{di(t)}{dt}$ (1.25)

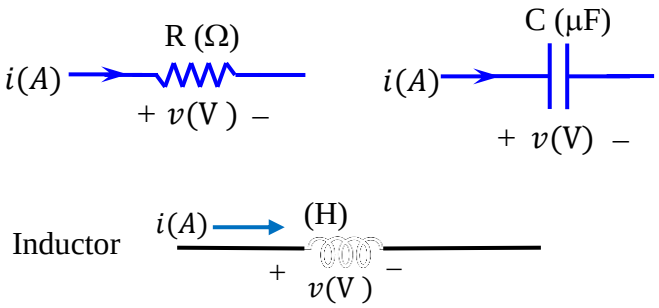

Fig. 1.4 Circuit symbol Model of Resistor, Capacitor, and Inductor

Power →Instantaneous Power:

When current $i(t)$ flows through the resistor (R), the power delivered to the resistor is given as;

$P(t) = v(t)i(t)$ (1.26)

Mean Power: When an alternating (sinusoidal) current of amplitude I flows through a resistor R (for example, a heating element), the mean or average power delivered to the resistor is written as;

$$\hat{P} = \frac{1}{2}RI^2 = \frac{1}{2}\frac{V^2}{R} \quad (1.27)$$

A resistor is a two-terminal component described by the mathematical model in terms of voltage and current as;

$$\text{R (Ohm)} = \frac{V(volt)}{I\,(amp)} \quad (1.28)$$

Where V and I are the voltage across and current through the resistor, the large signal Model of the resistor is described by Eq. (1.28). However, a resistor dissipates power, and as it dissipates power, it gets heated. Depending upon the material of the resistor, the heat can change the value of the resistor. Hence, considering the effect of heat, the large-signal model of the resistor could be written as;

$$R(t) = R(t_o)f_1(t - t_o) \quad (1.29)$$

Where $R(t_o)$ is the resistance at the reference temperature t_o and $f(t - t_o)$ is a suitable function that represents the variation in the value of the resistor. This function is dependent on the power dissipation in the resistor and its thermal properties. So, we can write the value of the resistor at any terminal voltage as

$$R(V) = R(V_o)f_2(V - V_o) \quad (1.30)$$

Where R(V) is the value of resistance at a reference voltage V_o and f_2 is a function of terminal voltage V and the reference voltage V_o. It is possible to interrelate the function f_1 and f_2 through the physics of heating and thermal properties of the material. The nature of these functions also depends upon the nature of variation of resistance with temperature. The resistance of metal film resistors increases linearly with temperature. On the contrary, the resistance of a Thermistor made of semiconducting material decreases linearly with temperature. Therefore, we may have a simple or a complex large-signal model of the resistor depending on the resistor's material.

The small-signal model of a resistor is simply a dynamic resistance that changes with respect to the change in the operating points that can be represented by

$$\Delta R(V) = \frac{\Delta V}{\Delta I} \quad (1.31)$$

Where $\Delta R(V)$ is the ratio of $\frac{\Delta V}{\Delta I}$ and ΔI and ΔV are small signal variations.

Modelling is one of the most important means for accelerating scientific and technological progress.

The modelling also intensifies the development of science and the economy, but unfortunately, it is given the least priority in Indian engineering education, mainly at the Undergraduate College Level. Several factors play a role in de-emphasizing modelling in engineering education globally. The Grinter [4] report supports converting engineering colleges to research institutes and takes away the engineering curriculum design. The Grinter report is one of the essential documents followed in engineering education in the United States.

The U.S. had much better resources and options after World War II than any other well-developed nation. The defence budget and military spending were very high, and engineering colleges were funded by the armed forces and Government. "Only research that helped to war-making was rewarded," presumably, "to keep alive the expectations of a perpetual war economy." by Ferguson [7]. Almost unlimited resources left no room for modelling instead, a philosophy of "trial-and-error" became popular in engineering development and design.

As global marketplaces got more intensive in their pursuit of re-engineering, American companies have adapted to the concepts of re-engineering, continuous design, just-in-time strategy, and product cost reduction. Consequently, *modelling* is getting attention among engineers and engineering schools.

A mathematical model uses mathematical language to explain a system. Mathematical models area unit used not solely within the natural sciences and engineering disciplines (such as physics, biology, natural science, meteorology, and electrical engineering) however conjointly within the social sciences (such as political economy, sociology, and political science); physicists, engineers, pc scientists, and economists use mathematical models most extensively. Eykhoff [8] outlined a mathematical model as an illustration of the essential aspects of the Associate in Nursing existing system (or a system to be constructed) that presents information of that system in usable form'. However, mathematical models will take several forms, not restricted to resurgent systems, applied math models, differential equations, or game-theoretic models. These different kinds of models will overlap with a given model involving a range of abstract structures.

1.6 Background of Modelling

Often, once engineers analyze a controlled or optimized system, they use a mathematical model. Within the analysis, engineers will build a descriptive model of the system as a hypothesis; however, the system might work or try {an} estimate. However, an unpredictable event might affect the system. Similarly, engineers will try totally different management approaches in simulations on top of things of a system.

The mathematical model typically describes a system by a collection of variables and a collection of equations that establish relationships between the variables. The values of the variables are often anything; real or numbers, Boolean values, or strings, for instance. The variables are some properties of the system; as an example, the measured system outputs typically within the variety of signals, temporal arrangement knowledge, counters, and event prevalence (yes/no). The particular model is the set of functions describing the various variables' relations.

1.7 Building Blocks of Modelling

There are six basic groups of variables; input variables, state variables, exogenous variables, random variables, and output variables. Since there may be several variables of every sort, the variables are typically denoted by vectors, call variables, or are typically referred to as freelance variables. Exogenous variables are typically referred to as parameters or constants. The variables do not seem to be freelance of every alternative because the state variables are captivated by the choice, input, random, and exogenous variables. Moreover, the output variables are captivated by the state of the system. The system's objectives and constraints are represented as functions of the output variables or state variables. The target functions can depend upon the angle of the model's user. Counting on the context, the Associate in Nursing objective operates additionally referred to as the Associate in Nursing index of performance because it is a few life of interest to the user. Though there is no limit to the number of objective functions and constraints a model will have, mistreatment or optimizing it becomes an additional concern (computationally).

1.8 Classification of Mathematical Models

Mathematical models may be classified in some of the following ways;

(a) *Linear vs nonlinear*→the linear systems are of two types, namely,

- Linear time-invariant, and
- Linear time-varying systems.

A differential equation is linear if its coefficients are constants or functions of the only independent variable. Dynamic systems composed of linear time-invariant lumped-parameter may be described by a linear time-invariant (or linear constant-coefficient) system. Systems that are represented by differential equations with their coefficients as functions of time are called linear time-varying systems. An example of a time-varying control system is a spacecraft control system—the mass of the aircraft changes due to fuel consumption.

Nonlinear Systems: A nonlinear system where the principle of superposition does not hold well. The response to two inputs cannot be calculated by treating the one input at a time and adding the result for a nonlinear system. Examples of nonlinear differential equations are;

$$\frac{d^2x}{dt^2} + \left(\frac{dx}{dt}\right)^2 + x = A\sin\omega t \tag{1.32}$$

$$\frac{d^2x}{dt^2} + (x^2 - 1)\frac{dx}{dt} + x = 0 \tag{1.33}$$

$$\frac{d^2x}{dt^2} + \frac{dx}{dt} + x + x^3 = 0 \tag{1.34}$$

If operators in a mathematical model are linear, the resulting mathematical model of the linear system suggested by Olof Staffans [9] is linear; otherwise, a model is considered nonlinear.

The question of linearity and nonlinearity depends on the context. A linear model might have nonlinear expressions. For instance, a linear statistical model assumes a linear relationship in parameters, but it might be nonlinear among predictor variables.

Similarly, a differential equation is alleged to be linear if it is often written with linear differential operators. However, it will still have nonlinear expressions in it. In an exceedingly mathematical programming model, if the target functions and constraints square measure diagrammatic entirely by linear equations, then the model is thought to be a linear model. If one or a lot of the target functions or constraints square measure diagrammatic with a nonlinear equation, then the model is thought of as a nonlinear model. Even in relatively simple systems, nonlinearity is usually related

to phenomena like chaos and un-changeableness. Though there square measure exceptions, nonlinear systems and models tend to be tougher to check than linear ones. a typical approach to nonlinear issues is linearization. However, this could be problematic if one attempts to check aspects like un-changeableness, that square measure powerfully tied to nonlinearity.

(b) *Deterministic vs probabilistic (stochastic)*→ A deterministic model of Lin and Segel [10] is one within which variable states are unambiguously determined by parameters within the model and by sets of previous states of those variables. Therefore, settled models perform a similar method for a given set of initial conditions. Conversely, randomness is a gift in an exceedingly random model, and variable states don't seem to be delineated by distinctive values but rather by likelihood distributions.

(c) *Static vs dynamic*→ the static model does not account for the time of elements, but a dynamic model does. Dynamic models are represented either in the form of difference or differential expressions.

(d) *Lumped versus distributed parameters*→ if the model is homogeneous, the parameters are lumped. If the model is heterogeneous (a varying state within the system), then the System's parameters are distributed. Distributed parameters are represented with partial differential equations and in many more ways.

1.9 Priori Information of Models

According to how much *a priori* information suggested by Jason and Jenkins [11,12] is available, Black box and white box models are commonly used to classify mathematical modelling difficulties. A *black-box* model is a system in which there is no a priori information available. A *white-box* model is known as a system where all necessary information required is available for use. In practice, all systems fall in-between *black-box* and *white-box* models. So, this concept works as an intuitive guide only.

It is desirable to use the maximum amount of a priori data to make the model a lot of correct predictions. The white-box models are typically thought of as softer due to acquired knowledge correctly; the model can behave appropriately. Often, a priori

data comes within the type of knowing the kind of functions regarding totally different variables. For Associate Nursing instance, if we tend to create a model of how a drug works in a human system, we all know that the number of drugs within the blood is associated with Nursing exponentially decaying performance. However, our tendency is still to live with many unknown parameters. How speedily will the medication quantity decay, and what is the initial quantity of drugs in the blood? In this instance, it is not a very simple white-box model. These parameters have to be calculable through some suggestions before using the model.

In black-box models, one tries to estimate each useful type of relationship between variables and, therefore, the numerical parameters in those functions. Employing a priori data, we tend to find ourselves, for instance, with a group of functions that most likely may describe the system adequately. If there is no a priori data, we will try to use functions as general as possible to hide all different models. In Nursing's often-used approach for black-box models, associates are neural networks that generally do not assume nearly one thing regarding the incoming information. Using a vast set of functions to elucidate a system estimates the parameters becomes increasingly powerful once the number of parameters (and different types of functions) increases.

1.10 Subjective Information of Models

Many a time, incorporating subjective information into a mathematical model is useful. This may be done based on *intuition, experience, expert opinion,* or mathematical convenience.

Bayesian statistics suggest a theoretical framework for incorporating a subjective approach in rigorous analysis. One specifies a prior subjective probability distribution and then updates it based on empirical data. An example of one such Associate in Nursing approach would be a necessary scenario within which an Associate in Nursing experimenter bends a coin slightly and tosses it once, recording whether or not the head comes up gives a chance of predictions that the following flip comes up heads. The probability of the coin coming up with a head after tossing is unknown. So, the experimenter makes an arbitrary decision (perhaps by looking at the shape of the coin)

about what prior distribution to use. Incorporating subjective information is necessary to predict the next flip accurately; being head would lead to wrong predictions.

MacKay's contribution to machine learning and information theory is based on the development of Bayesian methods for neural networks, called the rediscovery (with Radford M. Neal Shahbaba, B. and Neal, R. M. (2005). Improving classification when a class hierarchy is available using a hierarchy-based prior (Technical Report No. 0510, Dept. of Statistics, 11 pages.) of low-density parity-check codes and the invention of *Dasher*. This software application for communication was most popular with those who cannot use a traditional keyboard. MacKay [13] in 2003 he published a book on Information Theory, Inference, and Learning Algorithms based on the above statements.

1.11 Complexity of Models

Usually, the model complexity involves a trade-off between the simplicity and accuracy of the model. *Occam Razor's* [14] principle is particularly relevant to modelling; the essential idea is that the simplest one is the most desirable among models with roughly equal predictive power. On the one hand, adding complexity usually improves the fit of a model; it may make the model too difficult to understand and work with and pose computational problems, including *Numerical instability*. *Thomas Kuhn* [15] argues that explanations become more complex as science progresses before a *Paradigm shift* offers radical simplification. For example, when modelling an aircraft's flight, we embed each mechanical part of the aircraft into our model to acquire an almost *white-box* model of the system. Moreover, the computational cost of adding such a massive amount of details would not allow the use of such a complicated model.

Additionally, the uncertainty would increase thanks to a very sophisticated system due to every separate half induces some quantity of variance in the model. It is, therefore, typically acceptable to create some approximations to scale back the model to an acceptable size. Engineers typically will settle for some approximations to get a lot of sturdy and easy models. As an example, Newton's classical mechanics is an approximate model of the real world. Still, Newton's model is comfortable for many ordinary-life things, that is, as long as particle speeds are well below the sunshine's speed and we solely study macro-particles.

1.12 Training of Models

Any model which is not a pure white box contains some parameters that may be accustomed to match the model of the system it describes. If a neural network completes the modelling, the optimization of parameters is named coaching. In addition, standard modelling through expressly given mathematical functions determines parameters by curve fitting.

1.13 Model Evaluation

A crucial part of the modelling method is evaluating whether a given mathematical model accurately describes a system. This question will be challenging to answer because it involves many different kinds of analysis.

1.14 Model Fitting of Empirical Data

Usually, the best part of the model analysis checks whether or not a model fits experimental measurements or different empirical information. A typical approach to check this work is to separate {the information} into 2 disjoint subsets in models with parameters: coaching information and verification data. The coaching information measure would not estimate the model parameters. The correct associate model can closely match the verification information even though it did not set the model's parameters. The cross-validation of the regression model by Richard and Dennis [16] was presented in statistics.

Defining a metric to live the deviation between ascertained and foretold knowledge could be an excellent tool for assessing model work. A loss performs a similar role in statistics, call theory, and a few economic models. It is very tough to check the validity of a model's general mathematical kind when it is comparatively simple to check the parameters' appropriateness. In general, additional mathematical tools are developed to check applied math models' work than models involving Differential equations. Tools from statistic statistics will typically not measure; however, good knowledge fits a known distribution or comes back up with a general model that creates marginal assumptions regarding the model's mathematical kind.

1.15 Model's Scope

Assessing the model's scope is crucial. What things the model applies to may be less straightforward. If the model was created supported by a collection of information, one should confirm what systems or things could be a typical set of information. Whether or not the model describes well the properties of the system between knowledge points is named interpolation and it was suggested by Crochiere and Rabiner [17], and therefore the same question for events or knowledge points outside the determined knowledge is named extrapolation That was the suggestion of Brezinski and Zaglia [18]. Likewise, he did not include molecules' movements and different tiny particles. However, macroparticles were solely considered. It is then not stunning that his model does not extrapolate well into these domains, although his model is entirely decent for standard life physics.

1.16 Philosophical Considerations of Models

Many types of modelling implicitly involve claims concerning relation. This is often typically (but not always) true of models involving differential equations because modelling aims to extend our understanding of the globe. However, the validity of a model rests not solely on its acceptable empirical observations but also on its ability to extrapolate to things or information on the far side that was originally delineated within the model. One argues that a model is nugatory unless it provides some insight that goes on the far side of what's already notable from the development's direct investigation.

An example of such criticism is that the mathematical models of the optimum forage theory projected by Graham H. Pyke [19] do not supply insight that goes on the far side of the common-sense conclusions of evolution and alternative basic principles of ecology. We would discuss the general topic of deriving equivalent circuits from the differential equations that determine a given system's response. This is the procedure usually followed in modelling solid-state devices, where the distributed parameters of the equivalent circuits are derived from the solutions to Laplace or Poisson equations. The circuital visualization of this process provides insights that are extremely helpful in understanding the system response.

Mathematical modelling is the process of representing a physical system (structure, automobiles, graphs, diagrams, scattered plots, tree diagrams, circuits, etc.)

in the form of mathematical expressions that can predict the behaviour of the system. The model provides an insight into the physical system that reduces the problem to its essential characteristics.

A continuous model can use an ordinary or partial differential equation to describe a physical problem. This type of model may not necessarily contain any analytical solution. Hence, they require approximate solution methods such as finite differences, boundary elements, finite volumes, etc. These methods involve splitting the region of interest into a set of small elements. These elements produce a discrete approximation of the differential equations in each element and are required to solve all the discrete approximations simultaneously. Brief uses of continuous modelling are;

- Heat flow
- Acoustic
- Electromagnetic wave propagation
- Vibration analysis
- Active device modelling

As stated previously, mathematical modelling is a powerful tool in engineering education that enables its users to minimize time and cost in the design process. Also, mathematical modelling usage facilitates the process of redesign or concurrent engineering, a relatively new addition to American engineering education.

We are particularly interested in the mathematical modelling of electronic devices and their integration with passive components using a neat method called "Floating Admittance Matrix (FAM)"[20,21]. First, we would like to develop a floating admittance matrix of one of the devices, the Field Effect Transistor ($FET\ or\ MOSFET$) and then Bipolar Junction Transistor (BJT), and then integrate them in all types of circuits. The failure mechanism modelling of devices was taken up by Li ,Tian, and Wang [22].

Thus, the methodology of analysis used is to form a Floating Admittance Matrix of the circuit, including active devices and passive components (resistances and capacitances) for any complicated circuit. Then any mathematical tool such as MATLAB or MATHEMATICA can be used to get the result of the simulated mathematical model in the form of the matrix for complicated active circuits.

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Chapter 2

Transfer Function Generation of Three Terminal Devices (Two-Port Model)

2.1 Introduction

The small-signal models of a transistor (BJT), FET, MOSFET, and Op Amp can either be in terms of mathematical relationships between input and output variables or in the form of equivalent circuits. Equivalent circuit models are popular for several reasons, such as;

- Circuit designers tend to feel more at ease with a circuit diagram rather than a set of numbers or mathematical relationships.
- Transistor and integrated circuit designers prefer a model that reflects the device's construction, enabling modifications to the construction to be mapped onto the model.
- Many circuit analysis packages are now available that use equivalent circuit models of transistors and other devices used in larger circuits to be analysed.

In general, it is easy to analyse an electrical network with its equivalent model, giving the relationship between input and output variables. This is the reason we use a two-port [1-14] representation for any network. Port-1 functions as the input port and two-2 functions as the output port [4-7, 10-12]. In one port network, the current enters from one terminal and leaves from the other terminal. All types of passive components such as resistors, capacitors, and inductors are examples of one-port networks because each of them has only two terminals indicated in Fig. 2.1.

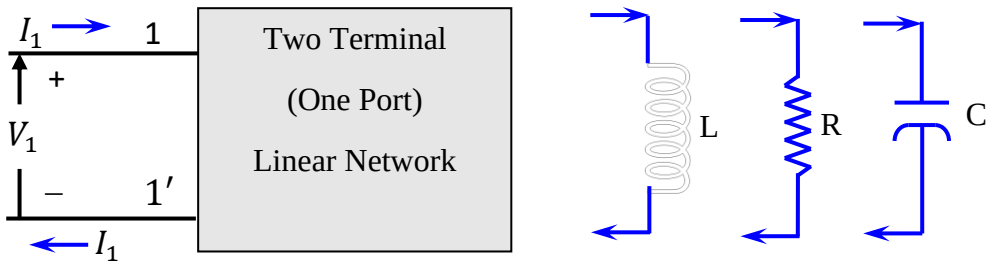


Fig. 2.1 Circuit Model of One Port Network

The pair of terminals, 1 & 1′, represents a port, i.e., port-1. This is the case of only one port because it has only two terminals.

2.2 Two-Port Network Model

Similarly, a two-port network has four terminals. A pair of two-terminal electrical networks in which current enters through one terminal and leaves through another terminal of each port. The two-port network representation is shown in Fig. 2.2.

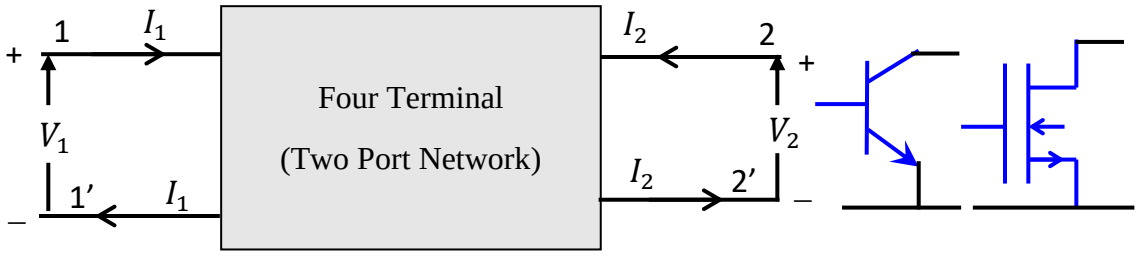


Fig. 2.2 Circuit Model of Two-Port Network

The pair of terminals, 1 & 1′, represents one port called the input port-1, and the other pair of terminals, 2 & 2′, represents another port, which is called the output port-2.

The two-port network has four variables V_1, V_2, I_1, and I_2 as shown in Fig. 2.2. Out of these four variables, we can choose any two variables as independent, and then another two variables become dependent on them. It results in six possible pairs of equations. These equations have dependent variables and independent variables. The coefficients of independent variables are called parameters. Thus, each pair of equations results in 4-parameters.

A single-phase transformer is an *ideal example* of a two-port network shown in 2.2 (b).

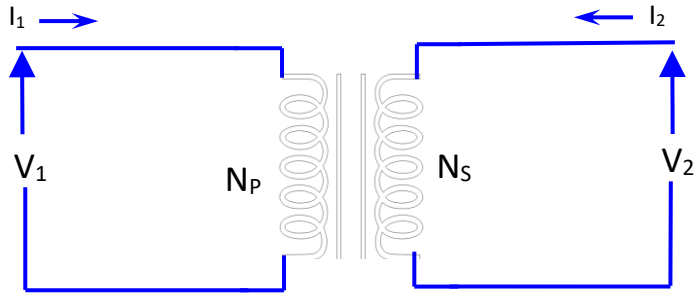


Fig. 2.2 (b) Circuit Model of Single-Phase Transformer as two-port Network

2.3 Two-Port Network Model Parameters

The parameters of a 2-port network are called two-port network parameters or, only, two-port parameters. The following are the important types of two-port network parameters [1-13].

- Z parameters
- Y-parameters
- h-parameters
- g-parameters

We proceed with the discussion about the above-mentioned 2-port parameters one by one. in the sequence.

Z-parameters

Assuming variables V_1 & V_2 as dependent and I_1 & I_2 as independent, results in the following two sets of equations. The coefficients of independent variables, I_1 and I_2 are called Z parameters.

$$V_1 = Z_{11}I_1 + Z_{12}I_2$$

$$V_2 = Z_{21}I_1 + Z_{22}I_2$$

The Z parameters are

$$Z_{11} = \frac{V_1}{I_1}\Big|_{I_2=0} \text{ (Open circuit parameter)}$$

$$Z_{12} = \frac{V_1}{I_2}\Big|_{I_1=0} \text{ (Open circuit parameter)}$$

$$Z_{21} = \frac{V_2}{I_1}\Big|_{I_2=0} \text{ (Open circuit parameter)}$$

$$Z_{22} = \frac{V_2}{I_2}\Big|_{I_1=0} \text{ (Open circuit parameter)}$$

The Z-parameters are called impedance parameters because these are simply the ratios of voltages and currents. The units of Z parameters are Ohm (Ω).

We can obtain two Z-parameters, Z_{11} and Z_{21} by opening the circuit of port-2. Similarly, we may obtain the other two Z parameters, Z_{12} and Z_{22} by opening the circuit of port-. So, the Z parameters are the open circuit parameter.

Y-parameters

Assuming variables I_1 & I_2 as dependent and V_1 & V_2 as independent, two sets of equations will result. The coefficients of independent variables, V_1 and V_2 are called Y parameters.

$$I_1 = Y_{11}V_1 + Y_{12}V_2$$

$$I_2 = Y_{21}V_1 + Y_{22}V_2$$

The Y parameters are

$$Y_{11} = \frac{I_1}{V_1}\Big|_{V_2=0} \text{ (Short circuit parameter)}$$

$$Y_{12} = \frac{I_1}{V_2}\Big|_{V_1=0} \text{ (Short circuit parameter)}$$

$$Y_{21} = \frac{I_2}{V_1}\Big|_{V_2=0} \text{ (Short circuit parameter)}$$

$$Y_{22} = \frac{I_2}{V_2}\Big|_{V_1=0} \text{ (Short circuit parameter)}$$

The Y-parameters are called admittance parameters because these are simply the ratios of currents and voltages. Units of Y-parameters are mho.

We can obtain two Y-parameters, Y_{11} and Y_{21} by doing a short-circuiting of port-2. Similarly, we can obtain the other two Y parameters, Y_{12} and Y_{22} by short-circuiting of port-1. Hence, the Y-parameters are also called short-circuit admittance parameters.

h-parameters

Assuming $\boldsymbol{V_1}$ & $\boldsymbol{I_2}$ as dependent variables and $\boldsymbol{I_1}$ & $\boldsymbol{V_2}$ as independent variables, results in the following two sets of equations. The coefficients of independent variables, $\boldsymbol{I_1}$ and $\boldsymbol{V_2}$ are called h-parameters.

$$V_1 = h_{11}I_1 + h_{12}V_2$$

$$I_2 = h_{21}I_1 + h_{22}V_2$$

The h-parameters are defined as;

$$h_{11} = \frac{V_1}{I_1}\Big|_{V_2=0}$$ (Short circuit parameter)

$$h_{12} = \frac{V_1}{V_2}\Big|_{I_1=0}$$ (Open circuit parameter)

$$h_{21} = \frac{I_2}{I_1}\Big|_{V_2=0}$$ (Short circuit parameter)

$$h_{22} = \frac{I_2}{V_2}\Big|_{I_1=0}$$ (Open circuit parameter)

The h-parameters are called hybrid parameters. The parameters h_{12} and h_{21} are unitless since those are the ratio of similar quantities, i.e., either ratio of two currents or two voltages and become dimensionless. The units of parameters, h_{11} and h_{22} are Ohm and Mho, respectively.

We can obtain two parameters, h_{11} and h_{21} by doing short-circuiting of port2. Similarly, we can obtain the other two parameters, h_{12} and h_{22} by opening the circuit of port-1. For modelling the transistor (BJT), the h-parameters or hybrid parameters are useful.

g-parameters

Assuming variables I_1 & V_2 as dependent and V_1 & I_2 as independent, two sets of equations result. The coefficients of independent variables, V_1 and I_2 are called g-parameters.

$$I_1 = g_{11}V_1 + g_{12}I_2$$

$$V_2 = g_{21}V_1 + g_{22}I_2$$

The g-parameters are defined as;

$$g_{11} = \frac{I_1}{V_1}\Big|_{I_2=0}$$ (Open circuit parameter)

$$g_{12} = \frac{I_1}{V_2}\Big|_{V_1=0}$$ (Short circuit parameter)

$$g_{21} = \frac{V_2}{V_1}\Big|_{I_2=0}$$ (Open circuit parameter)

$$g_{22} = \frac{V_2}{I_2}\Big|_{V_1=0}$$ (Short circuit parameter)

The g-parameters are called inverse hybrid parameters. The parameters, g_{12} and g_{21} are unitless since those are ratios of similar quantities. The units of parameters, g_{11} and g_{22} hybrid parameters are mho and ohm, respectively.

We can obtain two parameters, g_{11} and g_{21} by doing open circuiting of port-2. Similarly, we can obtain the other two parameters, g_{12} and g_{22} by doing short-circuiting of port-1. These two-port models have been described here only for academic purposes. Presently, it is very rarely used in the design and analysis of active devices.

The BJTs, FETs, MOSFETs, and Op. Amp. are important three-terminal electronic devices that may be modelled as four-terminal or two-port devices. Electronic circuits' performance evaluation appropriately incorporating electronic devices is a difficult proposition in the absence of a mathematical model. The usual practice is to visualize the circuit physically and make measurements in the absence of a mathematical model, but very often, it is not feasible, and we have to choose the alternative method called simulation. For simulation also, we need all the variables affecting the properties and behaviour of devices and circuits. The properties of the devices are captured using mathematical relationships among different variables of the devices. The passive and active electrical and electronic components are characterized by terminal voltages and the current relationship between them. Therefore, the circuits and devices' behaviour is modelled by thinking a voltage depends on currents, or currents depend on a voltage, or the suitable combination of one set of currents and voltages depends on another set of currents and voltages.

This dependency of one variable or a set of variables on the other set of variables of any device or circuit is given the name of mathematical modelling. In essence, mathematical modelling predicts the physical behaviour of any device or circuit. The two-port model developed based on voltage, and current variables is used in deriving different transfer functions such as the voltage transfer ratio, the current transfer ratio, the mutual transfer function between current and voltage ratio, and power transfer ratios.

2.4 Model Development of two-port Network

The Model development is a crucial part of the devices and circuits to predict their behaviour. A very simple model may not reflect the devices' complete behaviour and circuits using its terminal voltages and currents. There is not only one relationship

between voltage and current but a set of relationships will be required to accurately predict any circuit and device [1-32].

It is desirable to have one relationship between the terminal voltage and the terminal current of the device for convenience, but most often, it does not serve the purpose. Hence, a number of equations of dependent variables and independents are used to cover all aspects of the devices and circuits' behaviour. However, different applications require a different model, and many times these prove to be contradictory constraints necessitating a compromise between them. A few of the requirements of different models and their applications are listed below:

1. The physical understanding of the device depends on the relationship between its terminal voltage and current.
2. Representation of device in circuits with
   (i) Accuracy for achieving the desired characteristic
   (ii) Simplicity to use in the real-world problem.
   (iii) Division of nonlinear characteristics of the device in different zones for better understanding and model development
   (iv) The use of an empirical relationship that fits in the voltage-current relationship to predict the expected characteristics.
   (v) Observable effects in the variation of the values of the variables.
   (vi) A minimum number of parameters to describe the behaviour of the device completely.
3. Process control should be
   (i) Simple
   (ii) Reversible
   (iii) Available off the self.

The state-of-the-art technology encounters many physical effects in the manufacturing of any device. While the development of a complete theoretical model of any device based on physical effects is practically intractable. The Development of a Mathematical model base on empirical data results in a loss of predictive capabilities. It suggests a compromise between them to model the device for circuit simulation.

The device model should be of two basic categories:

- Primary, and
- Secondary

The model's primary category has a close relationship between understanding of device physics and aid to process control.

The secondary category of the model partly uses empirical relation to simplify the desired characteristics.

The device's mathematical equation should be such that it directly affects the variation of its characteristic. Sometimes different parameters affect the device characteristics in different zones. This helps in decoupling the model parameters with minimal iterations and its extraction.

The Newton-Rapson is a very well-known numerical technique for convergence of the relationship between terminal current or charges with its terminal voltages' continuous function. This method takes the help of the computation based on its 1st derivative. However, in some cases, it is very tedious, cumbersome, and prone to error to compute its derivatives analytically. The finite difference is another method to be used in such a situation, but it increases the computation time.

The device's operating ranges are often divided into different regions of its operation to formulate the model equation easily. Different mathematical models are developed in different device operations zones with the condition that the device current and voltages are continuous across the zones of boundaries to make the problems simpler. The terminal capacitance should be based on the charge control model of the device.

The modelling paradox states that a complex model is potentially better capable of producing accurate characteristics of the device. On the contrary, it is more difficult to extract all the parameters from such a complex model, and if the model parameters are not specified properly, it may not result in the device's desired characteristics.

2.5 Model Specifications

We start the explanation of model specification with an example of the model of the transistor [2-13]. The model development of the transistor depends on three pieces of information;

1. Fundamental constant
2. Operating conditions, and
3. Model parameters.

The fundamental constants, such as electronic charges or currents, are defined in the circuit. The operating condition defines the environment in which the model equations are evaluated. For instance, the bias voltage is taken as one of the operating conditions for transistors' model development [1-15]. The temperature variations are another operating condition that disturbs the device's quiescent point, and its parameters change as per the temperature variations. The values of any transistor's parameters vary very widely on the variation of the bias conditions and temperature.

The third condition requires the extraction of a set of model parameters for each and every device in a given circuit. The discrete circuit may have many discrete devices of similar types. A similar type of device in an integrated circuit undergoes similar types of fabrication steps. They may exhibit similar behaviour. Hence, such model parameters can be specified only once instead of repeating for all such components. So, there is a large number of parameters, which are common to similar devices. These parameters are generally related to the device geometry in an integrated circuit. The mathematical equation using terminal voltage and currents are used to realize any circuit. Such circuits are given the name of the equivalent circuit [11-22]. In essence, the model and the equivalent circuit mimic the property of components very closely.

As already discussed, many electronic or electrical components cannot be expressed by a single mathematical model or by a single equivalent circuit in all their operations regions. Then the models are developed in the regions valid and usable under the restricted condition such as terminal voltages, currents, and regions of operation and or other external conditions to cite the temperatures. The development of low-frequency models, high-frequency models, small-signal models, and large-signal models are important model development schemes for analyzing and designing amplifiers incorporating electronic devices such as BJT, FETs, MOSFETs, and Op Amp. The switching model, noise model, and thermal model are developed

for special functions of the devices and circuits, but small signal and large signal models are prevalent in the analysis of circuits containing electronic devices.

2.6. Large Signal Model

A large-signal model takes into account the fact that the large signal does affect the operating point. Also, elements are nonlinear, and power supply values can limit circuits. A small-signal model ignores simultaneous variations in the gain and supply values.

The large-signal model [5-6, 9-11] of the active and passive components must be used when components are subjected to large signal variation with respect to the maximum permissible swing that the device can withstand without getting damaged. The large-signal model development is based on the nonlinear nature of the components. The popular use of large-signal models of the BJT is in the circuits of power amplifiers, switches, comparators, limiters, etc. It is said that most of the time, large-signal models are inaccurate, as they have to represent devices over a wide range of terminal voltage and current with nonlinearity. The large-signal model of a diode and a BJT are shown in Figs. 2.3 and 2.4, respectively.

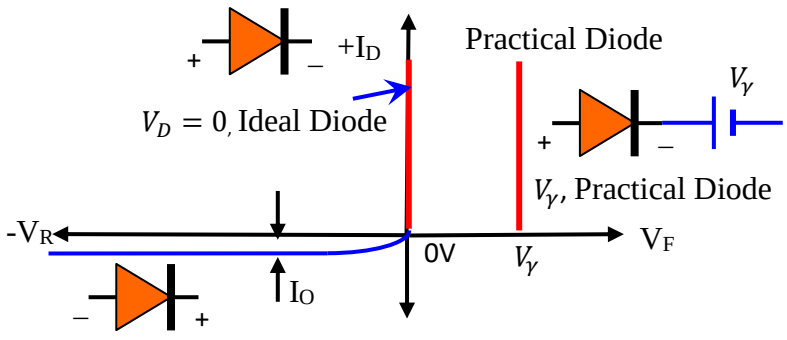


Fig. 2.3 Large-signal model of Semiconductor Diode

$I_D = I_0\left(e^{V_D/\eta V_T} - 1\right) = -I_0$, Reverse biased constant current

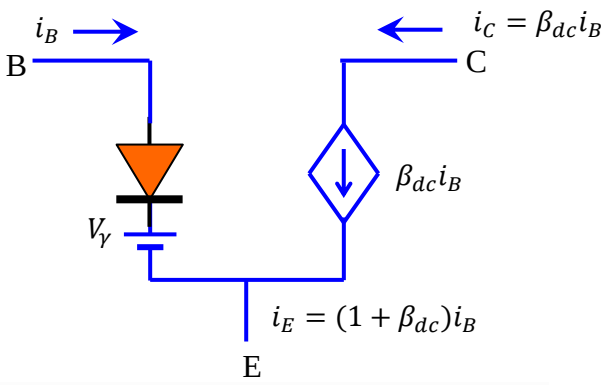


Fig. 2.4 Large Signal circuit Model of the BJT

The built-in potential, V_γ is the internal DC voltage present across the base-emitter junction as in Fig. 2.4. The base-emitter junction is forward-biased if the externally applied voltage across V_{BE} is more than V_γ. In an ideal diode, it is assumed that $V_\gamma = 0$, and hence the diode current becomes infinite for $V_{BE} = 0$ as in Fig. 2.3. If $V_\gamma \neq 0$, the device is a practical diode, and current once again becomes infinite at $V_{BE} = V_\gamma$ as in Fig. 2.3.

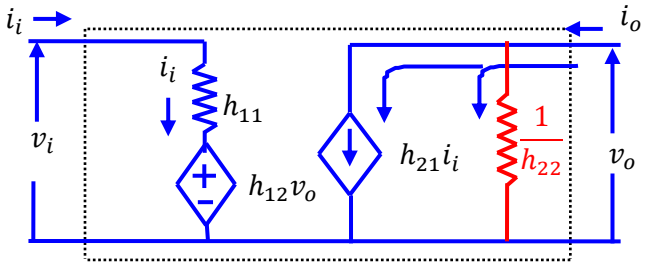
2.7. Small-Signal Model

As the name suggests, "small signal" deals with very low amplitude signals. With the quiescent point concept, we may say that the small-signal operation of a BJT or, for that matter, MOSFETs, JFETs, anything should not disturb the quiescent point. In essence, the types of signals which are small enough and do not push the circuit out of its linearity (should not be confused with the linear region of MOSFET/ BJT).

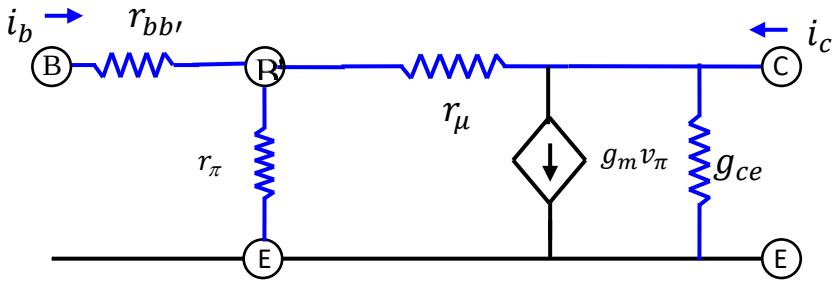
The small-signal model [5-16, 18-32] is based on very small fluctuations in the device's current and voltage around its Q-point. How do we quantify this small fluctuation of voltage and current? This is taken as small as measurable. Someone can measure it in microvolt, but others can measure it in millivolts. Hence, the small quantity is different for different people. The accuracy may be more for the measurement in microvolt than the measurement is done in millivolt.

The small-signal model is called the linear model, as the voltage and current produce small signal variations in magnitude. The small-signal models are used in all configurations of BJT amplifiers, FET, MOSFET, and Op. Amp., differential amplifiers, low noise amplifiers, and filters. A very important property of a small

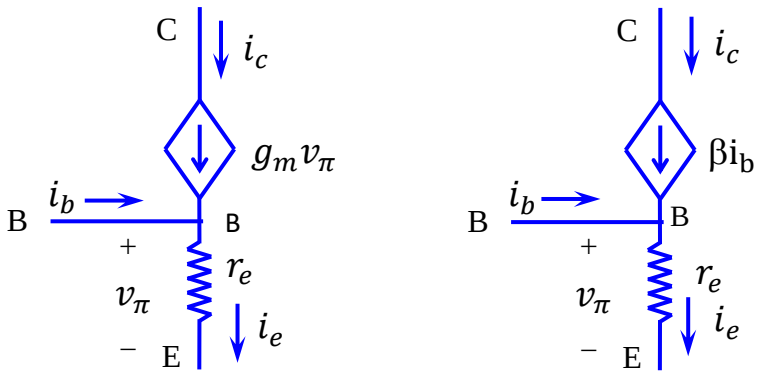
signal model for any linear amplifier circuit is that the superposition theorem should hold good and produces accurate results. The small-signal models are generally used to analyze all transfer functions (voltage gain, current gain, input resistance, output resistance, power gain) of any amplifier configuration. The hybrid, hybrid-π, and T-model of the BJT is shown in Fig. 2.5. Fig. 2.5 includes the small-signal FET/ MOSFET model also.



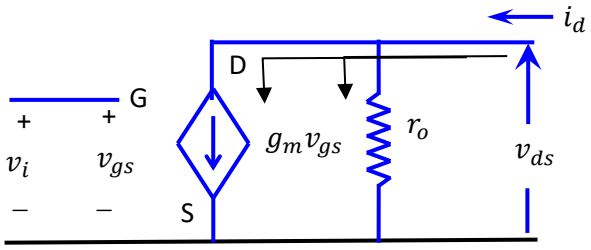
(a) L.F. Hybrid model of a BJT



(b) L.F. hybrid-π model of a BJT



(c) T-model of a BJT



(d) L. F. small-signal model of a MOSFET

Fig. 2.5 Small-signal circuit models of BJT & FET

2.8. Low-Frequency Model

The same electronic and electrical circuit components behave differently at low and high frequencies. At high frequencies, parasitic capacitances start appearing across the device and components. As the impedance of capacitance is frequency-dependent, the value of its impedance changes with a change in frequencies. The low-frequency models [4-16] are used both at low and medium frequency ranges. The model developed for the low-frequency range does not operate appropriately at high frequencies. Hence, each electronic device has its equivalent circuit model different at different frequencies: low frequency, medium frequency, and high-frequency models. The low-frequency representation of common emitter and Common-source devices is shown in Fig. 2.6. The low-frequency model is also called the mid-band model because there is no capacitive reactance present in this frequency range. The small-signal models drawn in Fig. 2.5 also do not have any capacitance.

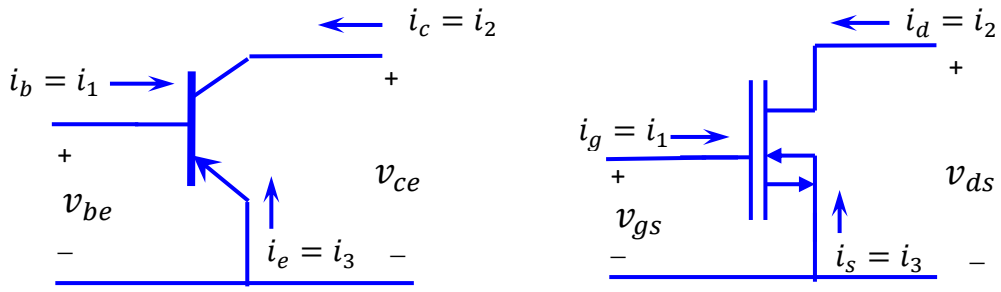


Fig. 2.6 Low-Frequency Symbolic Models of the BJT, MOSFET

Generally, the hybrid-π model) is used for analysis at a high frequency of any amplifier, including the parasitic capacitances. Figure 2.5 also displays the small-signal models at low frequencies.

2.9. High-Frequency Model

The manufacturers specify the operating frequency range of electronic and electrical components for their best use. At high frequency [4-16], the parasitic capacitances appear between the BJT/ FET terminals, resistance, inductance, and even across big capacitors, as in Fig. 2.7.

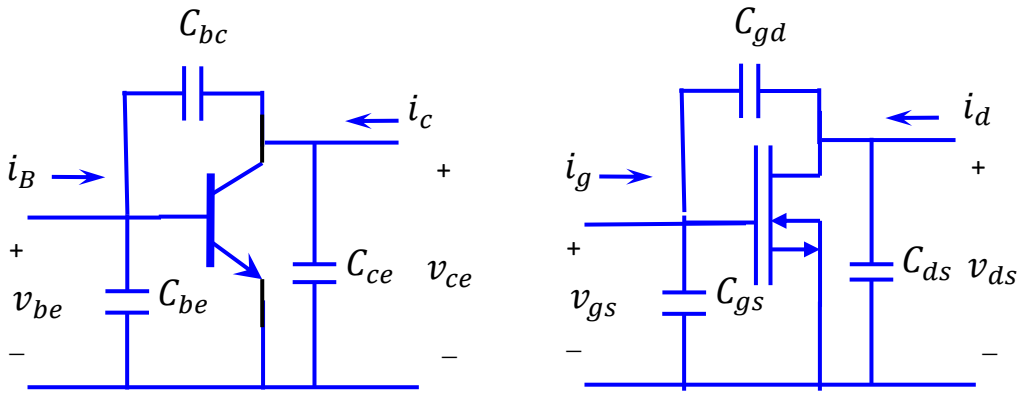


Fig. 2.7 High-Frequency Circuits of BJT & MOSFET

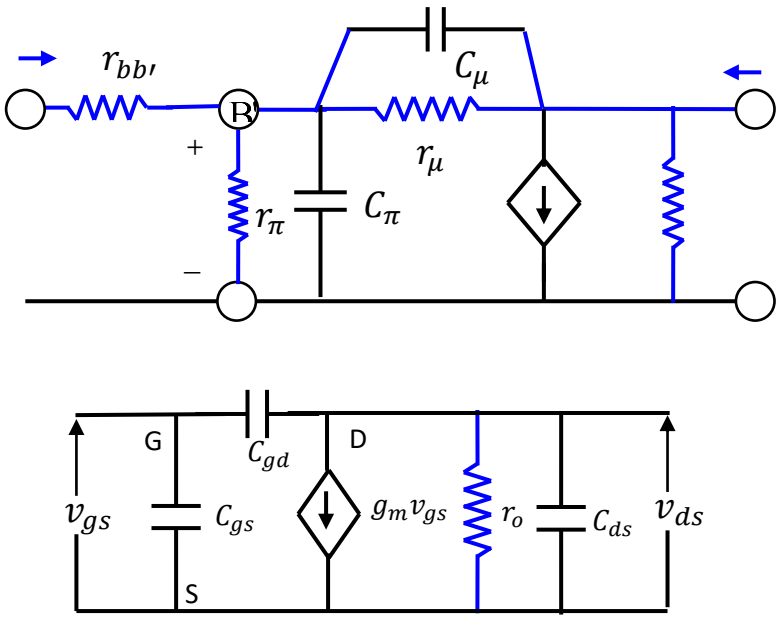


Fig. 2.8 High-Frequency Models of The BJT and MOSFET

The parasitic capacitances across the junctions of active devices start appearing at high frequencies. This parasitic capacitance produces an undesirable effect. The manufacturers specify the value of any device's parasitic capacitance, but it may not be very accurate and hence produce undesirable performance behaviour. For general purposes, manufacturers' parasitic values work well, but they should be measured and used for higher accuracy, such as military purposes. Fig. 2.8 shows the presence of parasitic capacitances $C_{b\prime e}$, $C_{b\prime c}$, C_{ce}, C_{gs}, C_{gd}, and C_{ds} These capacitances provide effective short circuits across the BJTs and FETs junctions and hence gain, or the output voltage starts decreasing as the frequency increases. Apart from these capacitances, the stray capacitances also become effective at high frequencies.

2.10. Floating Admittance Model

We would be proposing a model of the electronic devices using a floating admittance matrix approach. The inverse of resistance R is given as;

$$G = \frac{1}{R}$$

Here, G is given the name of conductance having a dimension of Siemens (S) or mho. Similarly, the inverse of impedance (Z) is admittance (Y) expressed as;

$$Y = \frac{1}{Z}$$

The dimension of Y is again S or mho.

Since the circuit generally consists of active devices and passive components such as resistances and capacitance, the *inverse of resistance* and the inverse of *capacitive impedances* have been given the name of *admittance* for the analysis. Though resistances may be used, yet the name of its inverse is assumed as admittance, not the conductance, for generality.

A new approach in developing models of the active and passive components is proposed here. This method is given the name floating admittance matrix approach [17-25] to the model development, especially for active devices such as BJT and FET/ MOSFET. All network functions of any amplifier incorporating these devices may be obtained in the form of ratios of the 1st-order and or 2nd-order cofactors

[25-32] of the circuit's floating admittance matrix. The conventional analysis of an n-port circuit or amplifier assumes anyone terminal as the reference node, and all other node voltages are defined w.r.t. this reference node. On the contrary, if all nodes of an n-port network are accessible nodes to which external voltage connections are made, it is called an n-port live network of floating nodes. Hence, such networks are named the floating admittance matrix network. The n-port network is very easily analysed using the floating admittance matrix approach. The definite admittance matrix network uses at least one node as a reference node for all other nodes, but the floating admittance matrix approach does not use any reference node.

A general topology of an n-terminal network consisting of arbitrary active and passive components connected in any manner is shown in Fig. 2.9. None of the terminals of Fig. 2.9 is taken as the reference terminal. All terminals are live in this network. In other words, if any reference terminal at all is there, it falls outside the purview of the network. For such a statement to hold good, all node currents are independent, and its initial conditions are set to zero. [17-24].

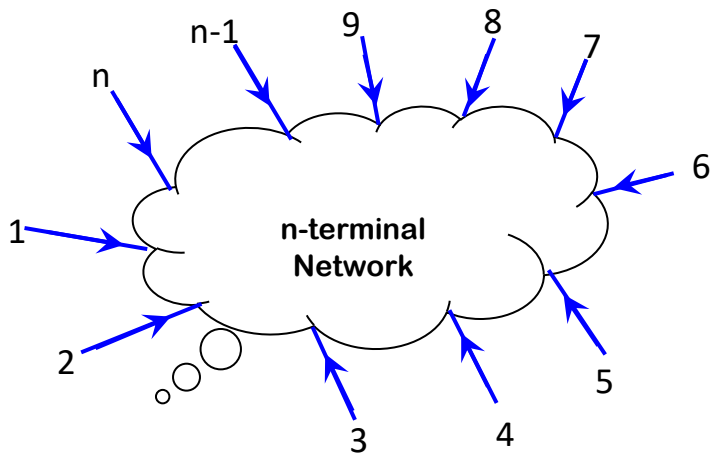


Fig. 2.9 n-terminal Network Model

The current entering from terminal-1 of Fig. 2.9 is expressed as;

$$i_1 = Y_{11}v_1 + Y_{12}v_2 + \ldots\ldots\ldots\ldots Y_{1n}v_n + I_{o1} \quad (2.1)$$

Similarly, the other n-terminal currents of Fig. 2.9 can be expressed as;

$$i_2 = Y_{21}v_1 + Y_{22}v_2 + \ldots\ldots\ldots\ldots Y_{2n}v_n + I_{o2} \quad (2.2)$$

$$\vdots \qquad \vdots \qquad\qquad\qquad \vdots \qquad \vdots$$

$$\vdots \qquad \vdots \qquad\qquad\qquad \vdots \qquad \vdots$$

$$i_n = Y_{n1}v_1 + Y_{n2}v_2 + \ldots\ldots\ldots\ldots Y_{nn}v_n + I_{on} \quad (2.3)$$

where, $v_1, v_2, \ldots\ldots v_n$ are the potentials connected at terminals 1, 2…..n and to some arbitrary but unspecified reference point and i_1, i_2, …….i_n are currents entering through terminals 1, 2, ……n from outside the network with initial conditions I_{o1}, I_{o2}, ……..I_{on}. The n-terminal network, together with the load, is assumed to be linear. Its voltage and current relationship from Eqs. (2.1) through (2.3) can be arranged in the form of a matrix as;

$$\begin{bmatrix} i_1 \\ i_2 \\ \vdots \\ \vdots \\ i_n \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} \ldots. & Y_{1n} \\ & \ldots\ldots\ldots & \\ Y_{21} & Y_{22} \ldots. & Y_{2n} \\ & \ldots\ldots\ldots & \\ & \ldots\ldots\ldots\ldots & \\ & \ldots\ldots\ldots\ldots & \\ Y_{n1} & Y_{n2} \ldots. & Y_{nn} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ \vdots \\ \vdots \\ v_n \end{bmatrix} + \begin{bmatrix} I_{01} \\ I_{02} \\ \vdots \\ \vdots \\ I_{0n} \end{bmatrix} \quad (2.4)$$

Equation (2.4) is further simplified in the form of a mathematical equation relating its terminal voltage and currents as;

$$i_i = Y_{ij}v_n + I_{oi} \quad (2.5)$$

Where in the subscript $'i'$ indicates the row value and $'j'$ the indicates the column value from 1 to n of Y_{ij}.

To verify the special conditions on the row elements of a FAM, if a voltage (v_o) [19-20, 25-32] is added to all existing terminal voltages v_1, v_2, ……v_n, the terminal currents are given by Eq. (2.4) changes to

$$\begin{bmatrix} i_1 \\ i_2 \\ \vdots \\ \vdots \\ i_n \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} & Y_{1n} \\ & \ldots\ldots & \\ Y_{21} & Y_{22} & Y_{2n} \\ & \ldots\ldots & \\ \vdots & \vdots \ldots\ldots & \vdots \\ \vdots & \vdots \ldots\ldots & \vdots \\ Y_{n1} & Y_{n2} \ldots\ldots & Y_{nn} \end{bmatrix} \begin{bmatrix} v_1 + v_0 \\ v_2 + v_0 \\ \vdots \\ \vdots \\ v_n + v_0 \end{bmatrix} + \begin{bmatrix} I_{01} \\ I_{02} \\ \vdots \\ \vdots \\ I_{0n} \end{bmatrix} \quad (2.6)$$

Subtracting Eq. (2.4) from Eq. (2.6) yields as;

$$\begin{bmatrix} i_1 \\ i_2 \\ : \\ : \\ i_n \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} \ldots . Y_{1n} \\ Y_{21} & Y_{22} \ldots . Y_{2n} \\ & \ldots . . \\ : & : \ldots . . \quad : \\ : & : \ldots . . \quad : \\ Y_{n1} & Y_{n2} \ldots . Y_{nn} \end{bmatrix} \begin{bmatrix} v_0 \\ v_0 \\ : \\ : \\ v_0 \end{bmatrix} = 0 \tag{2.7}$$

For quick and better understanding, we would like to reduce this matrix to represent the three-terminal devices such as BJTs, FETs, and MOSFETs using Eq. (2.7). So, Eq. (2.7) simplifies to a 3 x 3 floating admittance matrix of three-terminal electronic devices as;

$$\begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} & Y_{13} \\ Y_{21} & Y_{22} & Y_{23} \\ Y_{31} & Y_{32} & Y_{33} \end{bmatrix} \begin{bmatrix} v_0 \\ v_0 \\ v_0 \end{bmatrix} = 0 \tag{2.8}$$

The equation of each current i_1, i_2, and i_3 from Eq. (2.8) is written as;

$$i_1 = i_2 = i_3 = 0, \tag{2.9}$$

Substituting the values of i_1, i_2 and i_3 from Eq. (2.8) in Eq. (2.9) yields;

$$\left.\begin{aligned} i_1 &= (Y_{11} + Y_{12} + Y_{13})v_o = 0 \\ i_2 &= (Y_{21} + Y_{22} + Y_{23})v_o = 0 \\ i_3 &= (Y_{31} + Y_{32} + Y_{33})v_o = 0 \end{aligned}\right\} \tag{2.10}$$

From Eq. (2.10), $i_1 = (Y_{11} + Y_{12} + Y_{13})v_o = 0$

We have connected v_o, an additional voltage to all terminals, and so $v_o \neq 0$, then

$$Y_{11} + Y_{12} + Y_{13} = 0 \tag{2.11}$$

Similarly, from Eq. (2.10), $i_2 = (y_{21} + y_{22} + y_{23})v_o = 0$ and $v_o \neq 0$, then (2.12)

$$Y_{21} + Y_{22} + Y_{23} = 0 \tag{2.13}$$

Again from Eq. (2.10), $i_3 = (y_{31} + y_{32} + y_{33})v_o = 0$ and $v_o \neq 0$, then (2.14)

$$Y_{31} + Y_{32} + Y_{33} = 0 \tag{2.15}$$

Equations (2.11), (2.13), and (2.15) reveal a very important hypothesis that the *sum of all elements of any row of a floating admittance matrix must be equal to zero.*

Now, we would like to demonstrate the condition of all elements of any column of a floating admittance matrix. It is well known from KCL that the sum of all currents entering the network must be equal to the sum of leaving the currents of the network. In other words, the algebraic sum of the currents in any network must be zero i.e.

$$\begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} & Y_{13} \\ Y_{21} & Y_{22} & Y_{23} \\ Y_{31} & Y_{32} & Y_{33} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \end{bmatrix} + \begin{bmatrix} I_{o1} \\ I_{o2} \\ I_{o3} \end{bmatrix} \tag{2.16}$$

Setting initial conditions zero i.e. $I_{o1} = I_{o2} = I_{o3} = 0$ in Eq. (2.16) yields,

$$\begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} & Y_{13} \\ Y_{21} & Y_{22} & Y_{23} \\ Y_{31} & Y_{32} & Y_{33} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \end{bmatrix} \tag{2.17}$$

Expanding currents i_1, i_2, and i_3 from Eq. (2.17) yields;

$$i_1 = Y_{11}v_1 + Y_{12}v_2 + Y_{13}v_3 \tag{2.18}$$

$$i_2 = Y_{21}v_1 + Y_{22}v_2 + Y_{23}v_3 \tag{2.19}$$

$$i_3 = Y_{31}v_1 + Y_{32}v_2 + Y_{33}v_3 \tag{2.20}$$

As no current comes out from any terminal of Fig. 2.6, currents entering from all the *three-terminal* can be equated as;

$$i_1 + i_2 + i_3 = 0 \tag{2.21}$$

Substituting the values of i_1, i_2, and i_3 from Eqs. (2.18), (2.19), and (2.20) in Eq. (2.21) yield as;

$$Y_{11}v_1 + Y_{12}v_2 + Y_{13}v_3 + Y_{21}v_1 + Y_{22}v_2 + Y_{23}v_3 + Y_{31}v_1 + Y_{32}v_2 + Y_{33}v_3 = 0 \tag{2.22}$$

Let us suppose that all but terminal-1 of the three-terminal network is grounded i.e. $v_2 = v_3 = 0$ and $v_1 \neq 0$, then Eq. (2.22) reduces to

$$Y_{11}v_1 + Y_{21}v_1 + Y_{31}v_1 = (Y_{11} + Y_{21} + Y_{31})v_1 = 0 \tag{2.23}$$

$$Y_{11} + Y_{21} + Y_{31} = 0 \quad (2.24)$$

This proves that the sum of all elements of the first column of a three-terminal floating admittance matrix is zero.

Similarly, if we suppose that all but terminal-2 is grounded i.e. $v_1 = v_3 = 0$ and $v_2 \neq 0$, then Eq. (2.22) reduces to

$$Y_{12}v_2 + Y_{22}v_2 + Y_{32}v_2 = (Y_{12} + Y_{22} + Y_{32})v_2 = 0 \quad (2.25)$$

$$Y_{12} + Y_{22} + Y_{32} = 0 \quad (2.26)$$

Equation (2.26) suggests that the sum of all elements of the second column of the three-by-three matrix is zero.

Lastly, let us suppose that all but terminal-3 are grounded i.e. $v_1 = v_2 = 0$ and $v_3 \neq 0$, then Eq. (2.22) reduces to

$$Y_{13}v_3 + Y_{23}v_3 + Y_{33}v_3 = (Y_{13} + Y_{23} + Y_{33})v_3 = 0 \quad (2.27)$$

Since, $v_3 \neq 0$,

$$Y_{13} + Y_{23} + Y_{33} = 0 \quad (2.28)$$

Equation (2.28) reveals that the sum of all elements of the 3rd column of a 3x3 matrix is zero.

So one by one, it has been proved that *the sum of all elements of any row or any column of any floating admittance matrix becomes zero*.

The coefficient matrix Y_{ij} relating voltages v_1, v_2, …….v_n and currents i_1, i_2, …….i_n in Eq. (2.4) is separated as;

$$\begin{bmatrix} Y_{11} & Y_{12} \ldots . & Y_{1n} \\ & \ldots \ldots & \\ Y_{21} & Y_{22} \ldots . & Y_{2n} \\ & \ldots \ldots & \\ & \ldots \ldots & \\ Y_{n1} & Y_{n2} \ldots . & Y_{nn} \end{bmatrix} \quad (2.29)$$

This coefficient matrix in Eq. (2.29) is also called the *floating admittance matrix* of any n-terminal network because the reference point for the potentials is some arbitrary but unspecified point outside the network. Here coefficient matrix $[Y_{ij}]$ is called the floating admittance matrix (FAM). As stated above, the short circuit initial current I_{oi} results from the independent sources and/ or initial conditions in the interior of the n-port network. For this purpose, we shall consider all independent

sources outside the network, and all initial conditions are set to be zero. Hence, I_{oi} is supposed to be zero, and Eq. (2.5) further simplifies to

$$i_i = Y_{ij} v_i \tag{2.30}$$

Since BJTs, FET, and MOSFETs are 3-terminal active devices, the coefficient matrix can be stated to a 3-terminal devices matrix as;

$$\begin{bmatrix} Y_{11} & Y_{12} & Y_{13} \\ Y_{21} & Y_{22} & Y_{23} \\ Y_{31} & Y_{32} & Y_{33} \end{bmatrix} \tag{2.31}$$

Equation (2.31) represents the floating admittance matrix of any 3-terminal device.

If any of the terminals are made common to the other two, the corresponding row and column are deleted from the floating admittance matrix. For example, say terminal '3' is made common, then the 3rd row and 3rd column of the coefficient matrix are deleted, and the coefficient matrix of Eq. (2.31) reduces to;

$$\begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \tag{2.32}$$

Equation (2.32) is the 2 x 2 matrix reduced from the above Eq. (2.31).

The floating admittance matrix finds extensive use in designing and analysing complicated circuits using active devices such as BJTs, FETs, MOSFETs, and Op. Amp. and complex passive circuits. Since each of these active devices has three terminals, their 3-terminal currents and voltages are denoted as;

Base current and base voltage of the BJT $= i_b, v_b$

Gate current and gate voltage of the FET/ MOSFET $= i_g, v_g$

Collector current and voltage of the BJT$= i_c, v_c$

Drain current and drain voltage of the FET/ MOSFET $= i_d, v_d$

Emitter current and emitter voltage of the BJT $= i_e, v_e$

Source current and the source voltage of the FET/ MOSFET $= i_s, v_s$

As the vacuum tube has become obsolete, except for any special purpose, we take up the more frequently used active devices in electronic circuits such as BJTs, FETs, MOSFETs, and Op. Amps. Usually, these are used as 3-terminal devices, though their variant as four-terminal devices is also available. The four-terminal BJT and MOSFET are used at high frequencies. Even the BJTs and MOSFETs manufactured for low-frequency operations are also represented as a 4-terminal or two-port network by making one of its terminals common to both input and output sides in any of the configurations of BJTs, FETs, MOSFETs, and Op. Amp. We will be analysing these devices throughout our thesis work, assuming BJTs, FETs, MOSFETs, and Op. Amps. as two-port networks. The symbolic representation of typical 3-terminal devices is shown in Fig. 2.10.

These devices can be presented as a two-port network if any one of the terminals is referred to as common to both the input and output sides of the network in Figs. 2.11 and 2.12.

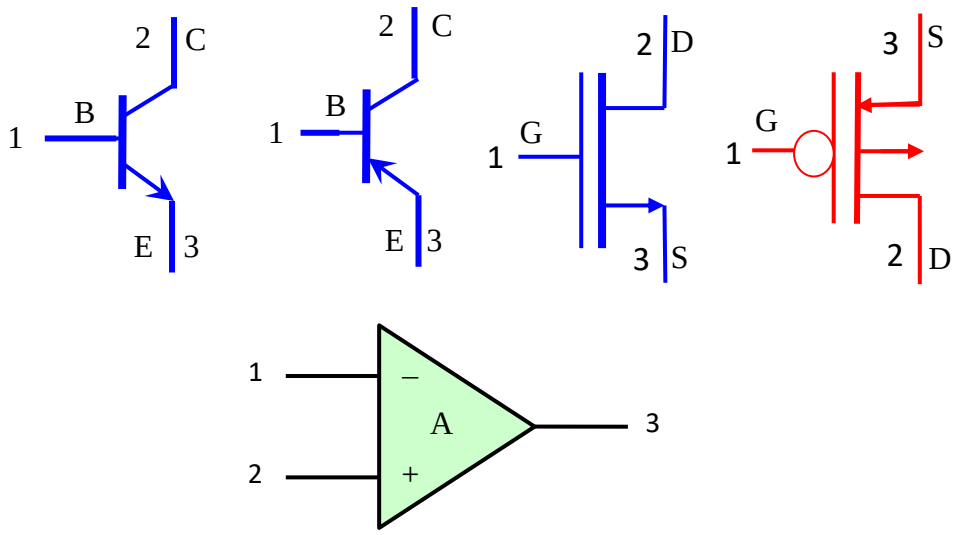


Fig. 2.10 Circuit Symbolic Model of BJT, MOSFET, Op. Amp.

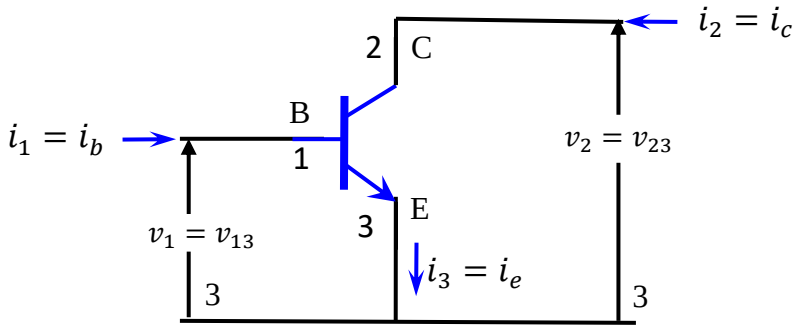


Fig. 2.11 Two-port Circuit Model of the npn Transistor

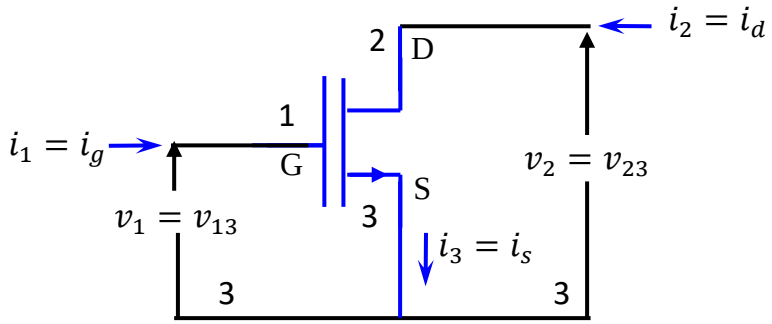


Fig. 2.12 Two-port Circuit Model of n-channel MOSFET

Figure 2.13 is the generalized two-port network. For the analysis of the circuits incorporating electronic devices using FAM, the 3-terminals of these active devices are assigned here numerics instead of their usual terminal symbolic letters such as B→1 for the base, C→2 for the collector, E→3 for the emitter, G→1 for the gate, D→2 for drain, S→3 for source. These numbers have been assigned for generalized description and analysis of the floating admittance matrix of these devices. With their terminal letters and numbers, these devices are shown in Figs. 2.11 and 2.12.

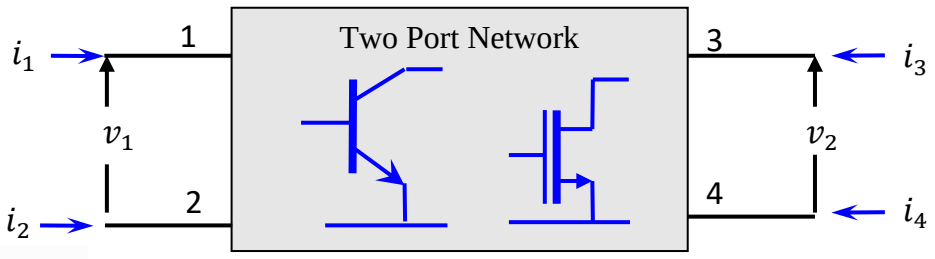


Fig. 2.13 Generalized 2-port network Model

The common base configuration is analogous to the common-gate of the FET, and MOSFET. common emitter configuration is analogous to a common-source and common collector configuration is analogous to a common drain.

Here, current i_1 and voltage v_1 are the generalized representation of the base current and base voltage of the BJT or gate current and the gate voltage of the FET/ MOSFET, i_2 and v_2 are the generalized representation of the collector current and collector voltage of the BJT or drain current and drain voltage of the FET/ MOSFET, i_3 and v_3 represent the emitter current and emitter voltage of the BJT or source current and the source voltage of the FET/ MOSFET. Equation (2.20) represents the generalized floating admittance matrix relationship between voltages and currents of any 2-port network. The generalized form of a 2-port network for BJT in common emitter (CE) configuration and MOSFET in common-source (CS) configuration are shown in Figs. 2.11 and 2.12.

The 3-terminal currents and voltages of the BJT and FET/MOSFET can be expressed [17-32] in the form of a matrix as;

$$\begin{bmatrix} i_1 = i_b/i_g \\ i_2 = i_c/i_d \\ i_3 = i_e/i_s \end{bmatrix} \begin{bmatrix} Y_{11} & Y_{12} & Y_{13} \\ Y_{21} & Y_{22} & Y_{23} \\ Y_{31} & Y_{32} & Y_{33} \end{bmatrix} \begin{bmatrix} v_1 = v_b/v_g \\ v_2 = v_c/v_d \\ v_3 = v_e/v_s \end{bmatrix} \tag{2.33}$$

To demonstrate the beauty of the floating admittance matrix and how the common base, collector, and emitter configurations of the BJTs are easily obtained, we take them up one by one. Eq. (2.33) is easily converted to the common emitter (CE) or common-source (CS) by just deleting the 3rd row and 3rd column of the floating admittance matrix of Eq. (2.33) as;

$$\begin{bmatrix} i_1 = i_b/i_g \\ i_2 = i_c/i_d \\ * \quad = \quad * \end{bmatrix} \begin{bmatrix} Y_{11} & Y_{12} & * \\ Y_{21} & Y_{22} & * \\ * & * & * \end{bmatrix} \begin{bmatrix} v_1 = v_b/v_g \\ v_2 = v_c/v_d \\ * \quad = \quad * \end{bmatrix} \tag{2.34}$$

The simplification of Eq. (2.34) can be done as;

$$\begin{bmatrix} i_1 = i_b/i_g \\ \\ i_2 = i_C/i_D \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{13} \\ \\ Y_{31} & Y_{33} \end{bmatrix} \begin{bmatrix} v_1 = v_b/v_g \\ \\ v_2 = v_C/v_D \end{bmatrix} \tag{2.35}$$

The common collector/ common-source configuration may be represented by deleting the 2nd row and 2nd column of Eq. (2.33) as;

$$\begin{bmatrix} i_1 = i_b/i_g \\ \\ * \quad = \quad * \\ \\ i_3 = i_e/i_s \end{bmatrix} \begin{bmatrix} Y_{11} & * & Y_{13} \\ \\ * & * & * \\ \\ Y_{31} & * & Y_{33} \end{bmatrix} \begin{bmatrix} v_1 = v_b/v_g \\ \\ * \quad = \quad * \\ \\ v_3 = v_e/v_s \end{bmatrix} \tag{2.36}$$

Equation (2.36) is further simplified as;

$$\begin{bmatrix} i_1 = i_b/i_g \\ \\ i_3 = i_e/i_s \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{13} \\ \\ Y_{31} & Y_{33} \end{bmatrix} \begin{bmatrix} v_1 = v_b/v_g \\ \\ v_3 = v_e/v_s \end{bmatrix} \tag{2.37}$$

Finally, the common base/ common-gate configuration can be represented by deleting 1st row and 1st column of the floating admittance matrix of Eq. (2.33) as;

$$\begin{bmatrix} * \quad = \quad * \\ \\ i_2 = i_c/i_d \\ \\ i_3 = i_e/i_s \end{bmatrix} \begin{bmatrix} * & * & * \\ \\ * & Y_{22} & Y_{23} \\ \\ * & Y_{32} & Y_{33} \end{bmatrix} \begin{bmatrix} * \quad = \quad * \\ \\ v_2 = v_c/v_d \\ \\ v_3 = v_e/v_s \end{bmatrix} \tag{2.38}$$

Equation (2.38) further simplifies as;

$$\begin{bmatrix} i_2 = i_c/i_d \\ \\ i_3 = i_e/i_s \end{bmatrix} = \begin{bmatrix} Y_{22} & Y_{23} \\ \\ Y_{32} & Y_{33} \end{bmatrix} \begin{bmatrix} v_2 = v_c/v_d \\ \\ v_3 = v_e/v_s \end{bmatrix} \tag{2.39}$$

The next section covers the mathematical tool that makes the information transformation possible.

2.11 First Order Cofactor of Matrix Model

The sub-matrix of the matrix [Y] is denoted as Y_{ij} and obtained from it by deleting the i^{th} row and j^{th} column.

The first-order cofactor [17-24, 28-32] is denoted by the symbol Y_{ij} of [Y] matrix is defined as;

$$Y_{ij} = (-1)^{i+j} \text{ the determinant of [Y]} \quad (2.40)$$

The main difference between cofactors and minors is the sign. Minors with the sign are called cofactors.

A class of matrix arises in linear systems analysis, known as the Equicofactors because all the first-order cofactors are equal.

As a consequence of the sum of all elements of any row producing zero and the sum of all elements of any column producing zero properties, all the cofactors of the elements of the floating admittance matrix are equal. A square matrix is an Equicofactors Matrix if the SUM of the elements of every row or every column equals zero. If 'Y' is an Equicofactors matrix, then all of its first-order cofactors are equal. Since the FAM of a linear, lumped, and time-invariant multi-terminal network has the property that the sum of elements of every row or every column is equal to zero, it is an Equicofactors Matrix. If Y_{mn} and Y_{ij} are any 2-cofactors of the matrix [Y], then

$$Y_{mn} = Y_{ij} \quad (2.41)$$

2.12. Second Order Cofactors of Matrix Model

If the sub-matrix $Y_{rs,pq}$ is obtained from the floating admittance matrix [Y] by deleting two rows' r' & 's' and two columns 'p' & 'q', the second-order cofactor [17-32] results. The second-order cofactor is denoted by the symbol $Y_{rs,pq}$ of the element Y_{rp} and Y_{sq} of the matrix [Y] and is the scalar quantity defined by the relationship after prefixing the sign,

$$Y_{rs,pq} = sgn(r-s)sgn(p-q)(-1)^{r+s+p+q} dety_{rp,sq} \quad (2.42)$$

$$where\ r \neq s, p \neq q\ and \quad (2.43)$$

$$sgn(x) = 1, if\ x > 0$$

$$sgn(x) = 0, if\ x = 0$$

$$sgn(x) = -1, if\ x < 0$$

It is convenient to define

$$Y_{rs,pq} = 0, \text{ for r = p and s = q} \quad (2.44)$$

This convention will follow throughout the remainder section.

The FAM greatly facilitates the formulation of the driving point or transfer functions between any pair of nodes or from any pair of nodes to any other pair of nodes in the network. The network functions can be expressed as the ratios of the second and/or first-order cofactors of the FAM. Because of its importance and its further applications in this work, it is repeated here.

2.13 Transfer Function Model of 2-Port Network

The network transfer functions [17-32] are important for analysing the active network. Hence, we would like to obtain different types of network functions of two-port networks in a generalized form. For this purpose, Figs. 2.14 and 2.15 are considered here. In Fig. 2.14, terminal 4 is grounded, whereas, in Fig. 2.15, terminal 2 is grounded, but terminal 3 is open-circuited in both of Figs. 2.14 and 2.15 (without load).

Fig. 2.14 Two-Port Network Model with $V_4 = 0$

We would like to derive all types of transfer functions of BJTs, FETs, and MOSFETs, considering them as two-port networks. It is evident from Fig. 2.14 that the output port is open, and the 4th terminal is grounded. The transfer impedance between nodes 3 & 4 and 1 & 2 is defined as the ratio of potential difference measured between nodes 3 & 4 to the current extracted from nodes 1 & 2. It is mathematically written as $\frac{v_{34}}{i_{12}}$ where v_{34} is the voltage across terminals 3 & 4, and the current source i_{12} connected between terminals 1 & 2. The generalized floating admittance matrix of the 4-pole network can be written as the extension 4-terminal network of Eq. (2.4) as;

$$\begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} & Y_{13} & Y_{14} \\ Y_{21} & Y_{22} & Y_{23} & Y_{24} \\ Y_{31} & Y_{32} & Y_{33} & Y_{34} \\ Y_{41} & Y_{42} & Y_{43} & Y_{44} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \end{bmatrix} \tag{2.45}$$

From Fig. 2.14, the terminal variables (voltages and currents) of the 2-port network (without load) can be expressed as;

$$\left.\begin{array}{l} i_{12} = i_1 = -i_2 \\ v_4 = 0, \\ v_{34} = v_3, and \\ i_3 = i_4 = 0 \end{array}\right\} \tag{2.46}$$

Substituting the terminal variable of Fig. 2.14 from Eq. (2.46) in (2.45) yields as;

$$\begin{bmatrix} i_1 \\ -i_2 \\ i_3 = 0 \\ i_4 = 0 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} & Y_{13} & Y_{14} \\ Y_{21} & Y_{22} & Y_{23} & Y_{24} \\ Y_{31} & Y_{32} & Y_{33} & Y_{34} \\ Y_{41} & Y_{42} & Y_{43} & Y_{44} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 = 0 \end{bmatrix} \tag{2.47}$$

Since, $v_4 = 0$, means the 4th terminal is grounded. This condition simplifies Eq. (2.47) after deleting the 4th row and the 4th column as;

$$\begin{bmatrix} i_1 \\ -i_2 \\ i_3 = 0 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} & Y_{13} \\ Y_{21} & Y_{22} & Y_{23} \\ Y_{31} & Y_{32} & Y_{33} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \end{bmatrix} \tag{2.48}$$

Now, Eq. (2.48) is further simplified, substituting terminal variables from Eq. (2.46) as;

$$\begin{bmatrix} i_1 \\ -i_2 \\ i_3 = 0 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} & Y_{13} \\ Y_{21} & Y_{22} & Y_{23} \\ Y_{31} & Y_{32} & Y_{33} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 = v_{34} \end{bmatrix} \quad (2.49)$$

The node voltage $v_3 = v_{34}$ is obtained from Eq. (2.49) using the property of matrix as;

$$\text{Hence, } v_3 = v_{34} = \frac{\begin{vmatrix} Y_{11} & Y_{12} & i_1 \\ Y_{21} & Y_{22} & -i_2 \\ Y_{31} & Y_{32} & 0 \end{vmatrix}}{|Y_4^4|} = \frac{Y_{21}Y_{32} - Y_{22}Y_{31} + Y_{11}Y_{32} - Y_{12}Y_{31}}{|Y_4^4|} i_{12} \quad (2.50)$$

Rearranging floating admittance element in Eq. (2.50) as;

$$v_3 = v_{34} = \frac{(Y_{11}+Y_{21})Y_{32} - (Y_{12}+Y_{22})Y_{31}}{|Y_4^4|} i_{12} \quad (2.51)$$

Applying the zero-sum property for the 1st column in Eq. (2.47) yields as;

$$Y_{11} + Y_{21} = -Y_{31} - Y_{41} = -(Y_{31} + Y_{41}) \quad (2.52)$$

Similarly, applying the zero-sum property for the 2nd column in Eq. (2.47) yields;

$$Y_{12} + Y_{22} = -Y_{32} - Y_{42} = -(Y_{32} + Y_{42}) \quad (2.53)$$

Substituting Eqs. (2.52) and (2.53) in Eq. (2.51) yields;

$$v_{34} = \frac{-(Y_{31}+Y_{41})Y_{32} + (Y_{32}+Y_{42})Y_{31}}{|Y_4^4|} i_{12} = \frac{-Y_{41}Y_{32} + Y_{31}Y_{42}}{|Y_4^4|} i_{12} \quad (2.54)$$

$$v_{34} = \frac{Y_{31}Y_{42} - Y_{32}Y_{41}}{|Y_4^4|} i_{12} = \frac{\begin{vmatrix} Y_{31} & Y_{32} \\ Y_{41} & Y_{42} \end{vmatrix}}{|Y_4^4|} i_{12} \quad (2.55)$$

Rearranging elements of the floating admittance matrix of Eq. (2.55) in the form of the cofactor of matrix yields;

$$v_{34} = \frac{\begin{vmatrix} Y_{31} & Y_{32} \\ Y_{41} & Y_{42} \end{vmatrix}}{|Y_4^4|} i_{12} = \frac{|Y_{34}^{12}|}{|Y_4^4|} i_{12} \quad (2.56)$$

The minor of any element of a matrix is the determinant of the matrix obtained by deleting the row and column that intersect the particular element.

Example

$$[Y] = \begin{bmatrix} Y_{11} & Y_{12} & Y_{13} & Y_{14} \\ Y_{21} & Y_{22} & Y_{23} & Y_{24} \\ Y_{31} & Y_{32} & Y_{33} & Y_{34} \\ Y_{41} & Y_{42} & Y_{43} & Y_{44} \end{bmatrix} \tag{2.57}$$

The minor of the element intersecting 1st row and 3rd column of Eq. (2.57) is expressed as;

$$Minor\ Y_{13} = \begin{vmatrix} Y_{11} & Y_{12} & Y_{13} & Y_{14} \\ Y_{21} & Y_{22} & Y_{23} & Y_{24} \\ Y_{31} & Y_{32} & Y_{33} & Y_{34} \\ Y_{41} & Y_{42} & Y_{43} & Y_{44} \end{vmatrix} = \begin{vmatrix} Y_{21} & Y_{22} & Y_{24} \\ Y_{31} & Y_{32} & Y_{34} \\ Y_{41} & Y_{42} & Y_{44} \end{vmatrix} \tag{2.58}$$

We know that a cofactor is it's minor with the proper sign. The sign of any element of the floating admittance matrix is given as;

$$= (-1)^{i+j}. \tag{2.59}$$

where i =j ≠ 0

Thus, cofactors concerning 2-rows (1 & 2) and 2-columns (3 &4) are expressed as;

Cofactor $|Y_{34}^{12}|$ = Minors of the matrix in Eq. (2.58) after eliminating 1st and 2nd rows and eliminating 3rd and 4th columns with proper signs as;

$$\begin{vmatrix} Y_{31} & Y_{32} \\ Y_{41} & Y_{42} \end{vmatrix} = sgn(1-2)sgn(3-4)(-1)^{1+2+3+4}|Y_{34}^{12}| \tag{2.60}$$

In Eq. (2.60), after deleting the 1st & 2nd rows and 3rd & 4th columns of the 4x4 floating admittance matrix, one of the cofactors is $\begin{vmatrix} Y_{31} & Y_{32} \\ Y_{41} & Y_{42} \end{vmatrix}$. Hence, Eq. (2.56) can now be written as;

$$\frac{v_{34}}{i_{12}} = \frac{\begin{vmatrix} Y_{31} & Y_{32} \\ Y_{41} & Y_{42} \end{vmatrix}}{|Y_4^4|} = sgn(1-2)sgn(3-4)(-1)^{1+2+3+4}\frac{|Y_{34}^{12}|}{|Y_4^4|} \tag{2.61}$$

Equation (2.61) is the transfer impedance between terminal voltage v_3 and terminal current i_1 as;

$$\frac{v_{34}}{i_{12}} = \frac{v_3}{i_1} = Z_{31}. \tag{2.62}$$

2.14. Self-Admittance Model of 2-Port Network

One of the important transfer functions of the two-port networks is the input impedance. The input impedance is also referred to the self-impedance [17-32]. In order to obtain the self-port driving point impedance, let us modify the two-port network of Fig. 2.14 to Fig. 2.15 by grounding the 2nd node and not the 4th as in Fig. 2.14. The self-port driving port impedance is defined as the ratio of the self-port voltage to the self-port current. Mathematically it is expressed between nodes 1 and 2, forming ports 1-2 as;

$$\text{Self-port driving port impedance} = \frac{v_{12}}{i_{12}} \tag{2.63}$$

Fig. 2.15 Two-Port Network Model with $V_2 = 0$

Where, $v_{12} = v_1$ is the potential difference between terminals 1 & 2 of Fig. 2.15, with terminal 2 connected as the reference node and $i_{12} = i_1$. This leads to two-port voltage and current variables of Fig. 2.15 as;

$$\left.\begin{aligned} i_{12} = i_1 = 0 \\ i_2 = 0 \\ v_{12} = v_1, \\ v_2 = 0, and \\ i_3 = 0 \end{aligned}\right\} \tag{2.64}$$

Since terminal 2 is grounded, Eq. (2.47) is further simplified by substituting terminal variables at 2 by shorting 2nd row and 2nd column and substituting conditions written in Eq. (2.64) for Fig. 2.15 as;

$$\begin{bmatrix} i_1 \\ i_2 \\ i_3 = 0 \\ i_4 = 0 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} & Y_{13} & Y_{14} \\ Y_{21} & Y_{22} & Y_{23} & Y_{24} \\ Y_{31} & Y_{32} & Y_{33} & Y_{34} \\ Y_{41} & Y_{42} & Y_{43} & Y_{44} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 = 0 \\ v_3 \\ v_4 \end{bmatrix} \tag{2.65}$$

The floating admittance matrix for Fig. 2.15 with substitution of Eq. (2.65) after deleting the 2nd row and 2nd column (since terminal 2 is grounded) is expressed as;

$$\begin{bmatrix} i_1 \\ i_3 = 0 \\ i_4 = 0 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{13} & Y_{14} \\ Y_{31} & Y_{33} & Y_{34} \\ Y_{41} & Y_{43} & Y_{44} \end{bmatrix} \begin{bmatrix} v_1 \\ v_3 \\ v_4 \end{bmatrix} \tag{2.66}$$

Rearranging port variable $i_{12} = i_1$ of Eq. (2.66) results in;

$$\begin{bmatrix} i_{12} \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{13} & Y_{14} \\ Y_{31} & Y_{33} & Y_{34} \\ Y_{41} & Y_{43} & Y_{44} \end{bmatrix} \begin{bmatrix} v_{12} \\ v_3 \\ v_4 \end{bmatrix} \tag{2.67}$$

The input port voltage is obtained using the property of the matrix as;

$$\text{Now,} \quad v_{12} = \frac{\begin{vmatrix} i_{12} & Y_{13} & Y_{14} \\ 0 & Y_{33} & Y_{34} \\ 0 & Y_{43} & Y_{44} \end{vmatrix}}{|Y_2^2|} = \frac{\begin{vmatrix} Y_{33} & Y_{34} \\ Y_{43} & Y_{44} \end{vmatrix}}{|Y_2^2|} i_{12} \tag{2.68}$$

Since $\begin{vmatrix} Y_{33} & Y_{34} \\ Y_{43} & Y_{44} \end{vmatrix}$ is one of the cofactors deleting 1st & 2nd rows and 1st and 2nd columns of the 4x4 floating admittance matrix of Eq. (2.65) and is expressed as;

$$\begin{vmatrix} Y_{33} & Y_{34} \\ Y_{43} & Y_{44} \end{vmatrix} = sgn(1-2)sgn(1-2)(-1)^{1+2+1+2}|Y_{12}^{12}| \tag{2.69}$$

Now Eq. (2.68) is written as;

$$\frac{v_{12}}{i_{12}} = \frac{\begin{vmatrix} Y_{33} & Y_{34} \\ Y_{43} & Y_{44} \end{vmatrix}}{|Y_2^2|} = Z_{12} = sgn(1-2)sgn(1-2)(-1)^{1+2+1+2}\frac{|Y_{12}^{12}|}{|Y_2^2|} \quad (2.70)$$

Hence, the voltage transfer function $\frac{v_{34}}{v_{12}}$ can be expressed by combining Eqs. (2.70) and (2.61) as;

$$\frac{v_{34}}{i_{12}} / \frac{v_{12}}{i_{12}} = sgn(1-2)sgn(3-4)(-1)^{1+2+3+4}\frac{|Y_{34}^{12}|}{|Y_4^4|} / \frac{|Y_{12}^{12}|}{|Y_2^2|} \quad (2.71)$$

Since terminal 2 is taken as a reference terminal in one case and terminal 4 is taken as the reference for the other case, then $|Y_2^2| = |Y_4^4|$, then Eq. (2.71) simplifies as;

$$\frac{v_{34}}{v_{12}} = sgn(3-4)sgn(1-2)(-1)^{3+4+1+2}\frac{|Y_{34}^{12}|}{|Y_{12}^{12}|} \quad (2.72)$$

Equation (2.72) gives the voltage gain [29-32] between output port voltage v_{34} and input port voltage v_{12}.

From self-port driving point impedance, $i_{12} = i_1 = \frac{|Y_2^2|}{|Y_{12}^{12}|}v_{12}$ (2.73)

From the equation of the voltage transfer function $i_{34} = i_3 = v_{34}G_L$

$$v_{34} = sgn(3-4)sgn(1-2)(-1)^{3+4+1+2}\frac{|Y_{34}^{12}|}{|Y_{12}^{12}|}v_{12}$$

$$i_{34} = i_3 = v_{34}G_L = sgn(3-4)sgn(1-2)(-1)^{3+4+1+2}\frac{|Y_{34}^{12}|}{|Y_{12}^{12}|}v_{12}G_L \quad (2.74)$$

$$v_{12} = \frac{|Y_{12}^{12}|}{|Y_2^2|}i_{12} \quad (2.75)$$

$$i_{34} = v_{34}G_L = sgn(3-4)sgn(1-2)(-1)^{3+4+1+2}\frac{|Y_{34}^{12}|}{|Y_{12}^{12}|}x\frac{|Y_{12}^{12}|}{|Y_2^2|}i_{12}G_L \quad (2.56)$$

Hence, Current gain [29-32] $= \frac{i_{34}}{i_{12}}$

$$\frac{i_{34}}{i_{12}} = sgn(3-4)sgn(1-2)(-1)^{3+4+1+2}\frac{|Y_{34}^{12}|}{|Y_{12}^{12}|}x\frac{|Y_{12}^{12}|}{|Y_2^2|}G_L$$

$$\frac{i_{34}}{i_{12}} = sgn(3-4)sgn(1-2)(-1)^{3+4+1+2}\frac{|Y_{34}^{12}|}{|Y_2^2|}G_L \quad (2.77)$$

The transfer impedance between output port voltage and input port current can now be generalized to n-pole networks as [17-24, 28-32];

$$Z_{mn}^{ij} = \frac{v_{ij}}{i_{mn}} = sgn(i-j)sgn(m-n)(-1)^{i+j+m+n}\frac{\left|Y_{ij}^{mn}\right|}{|Y_n^n|} \tag{2.78}$$

Self-port driving point impedance $Z_{mn} = \frac{v_{mn}}{i_{mn}} = \frac{|Y_{mn}^{mn}|}{|Y_n^n|}$ (2.79)

Voltage Gain $= A_v|_{mn}^{ij} = \frac{v_{ij}}{v_{mn}}$

$$\frac{v_{ij}}{v_{mn}} = sgn(i-j)sgn(m-n)(-1)^{i+j+m+n}\frac{\left|Y_{ij}^{mn}\right|}{|Y_{mn}^{mn}|} \tag{2.80}$$

Current Gain $= A_i|_{mn}^{ij} = \frac{i_{ij}}{i_{mn}}$

$$\frac{i_{ij}}{i_{mn}} = sgn(i-j)sgn(m-n)(-1)^{i+j+m+n}\frac{\left|Y_{ij}^{mn}\right|}{|Y_n^n|}G_L \tag{2.81}$$

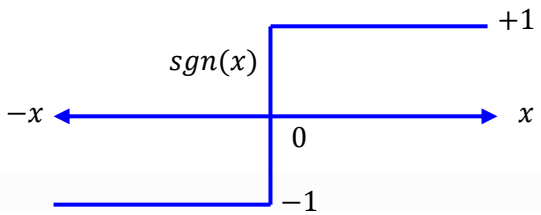
Power Gain $= A_p\big|_{mn}^{ij} = A_v|_{mn}^{ij} x A_i|_{mn}^{ij} = \frac{v_{ij}}{v_{mn}} x \frac{i_{ij}}{i_{mn}}$ (2.82)

$where\ i \neq j, m \neq n\ and$

$sgn(x) = +1\ for\ x > 0$

$sgn(x) = 0\ for\ x = 0$

$sgn(x) = -1\ for\ x < 0$



(2.83)

$$\left|y_{ij}^{mn}\right| = \left|\begin{matrix} determinant\ of\ submatrix\ deleting\ m^{th}, n^{th}\ rows\ and \\ i^{th}, j^{th}\ columns\ of\ |y| \end{matrix}\right|$$

Here, m & n are excitation terminals, and $'i'$&$'j'$ are response terminals.

2.15. Conclusions

Different transfer functions such as voltage gain, current gain, power gain, input impedance, and output impedance of any three-terminal device, amplifiers containing three-terminal devices or circuits can be easily obtained, have been demonstrated here in this chapter. Additionally, how any n-port network can be described using the floating admittance matrix has also been shown. It has been demonstrated that all transfer functions can be obtained in the form of ratios of

cofactors of the floating admittance matrix. This elegant approach is superior to the equivalent circuit approach for analysing the amplifier transfer functions of two-port networks.

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Chapter 3

Modelling of the BJT Amplifiers

3.1 Introduction

The BJT is modelled by the circuit elements such as a current source or voltage source, resistances, and capacitances. The modelling technique [1-17] is much simpler than the graphical analysis procedures of BJT amplifiers. The use of models may result in some loss of accuracy since the representation of a device by a model assumes some degree of approximation. However, the approximations are often very good, resulting in the most accurate circuits. Appropriate approximations are important in most analysis and design procedures for practical devices.

When the signal levels are small, electronic devices can be represented by *linear* models consisting of linear circuit elements like a voltage source, current source, resistance, and capacitances. Such models are applied to many amplifier circuits, except in the case of the power amplifier.

When the signal levels are large, the models assume the nonlinearities of the device. Such models are applied to large-signal amplifiers or digital circuits.

There are many ways to characterise the BJT Amplifiers. One way of categorisation is based on its frequency [4] response i.e.

1. Low frequency
2. Mid-frequency, and
3. High Frequency

Consequently, the low-frequency BJT model [1-26] has two prevalent categories, namely,

- the h-parameter model
- hybrid-π model.
- T-model

For high frequency again, there are two models called

- Hybrid-π model, and
- Y-parameter model

These days hybrid-π or T-model provides a much simpler analysis technique and is normally used to analyse the BJT amplifier.

3.2 Small-Signal Model Development of the BJT

The BJT starts functioning as an amplifier if the base-emitter junction (V_{BE} or V_{EB}) is forward-biased and the collector-base (V_{CB} or V_{BC}) junction is reverse-biased [1-40]. For that, let us consider the circuit of Fig. 3.1.

The relationship between DC voltages and DC current in the circuit [1-26] of Fig. 3.1 is expressed as;

$$I_C = I_S exp\left(\frac{V_{BE}}{\eta V_T}\right) \cong I_S exp\left(\frac{V_{BE}}{V_T}\right);$$

$\eta \to 1$ for the simplification of analysis and $V_{BE} \gg V_T$. (3.1)

$$I_C = \alpha I_E \quad (3.2)$$

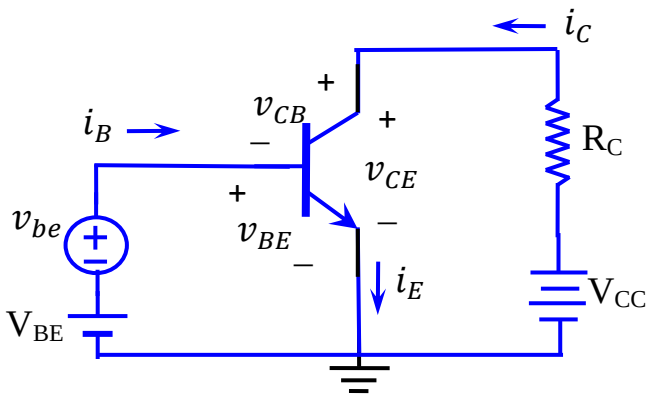

Fig. 3.1 Circuit Model of the BJT amplifier with DC and AC superimposed

$$I_C = \beta I_B \quad (3.3)$$

$$I_E = I_C + I_B \quad (3.4)$$

$$V_{CE} = V_C = V_{CC} - I_C R_C \tag{3.5}$$

Obviously, the voltage at the collector point ($V_C = V_{CE}$) should be larger than the voltage at the base point (V_B) for the npn transistor to operate in the active region. Conversely, V_C should be more negative than V_B in the case of a pnp transistor to remain in the active region.

The circuit of Fig. 3.1 has the pure ac input voltage (v_{be}) and pure DC voltage (V_{BE}) connected in series to set the required biased point taking into consideration of the DC supply voltage V_{CC} and the dc load resistance R_C. Now, the effective base-emitter voltage in Fig. 3.1 is given as;

$$v_{BE} = V_{BE} + v_{be} \tag{3.6}$$

Merging Eq. (3.1) and (3.6) yields the collector current as;

$$i_C = I_S exp\left(\frac{v_{BE}}{V_T}\right) = I_S exp\left(\frac{V_{BE}+v_{be}}{V_T}\right) = I_S exp\left(\frac{V_{BE}}{V_T}\right) exp\left(\frac{v_{be}}{V_T}\right)$$

$$= I_C exp\left(\frac{v_{be}}{V_T}\right) \tag{3.7}$$

Since, $v_{be} \ll V_T$, the exponential function of Eq. (3.7) can be expanded as;

$$i_C = I_C exp\left(\frac{v_{be}}{V_T}\right) = I_C \left\{1 + \frac{1}{1!}\left(\frac{v_{be}}{V_T}\right) + \frac{1}{2!}\left(\frac{v_{be}}{V_T}\right)^2 + \cdots..\right\} \tag{3.8}$$

Again, since, $v_{be} \ll V_T$, the higher-order terms of Eq. (3.8) can be neglected to yield;

$$i_C = I_C \left\{1 + \left(\frac{v_{be}}{V_T}\right)\right\} = I_C + \left(\frac{I_C}{V_T}\right) v_{be} \tag{3.9}$$

The dimensionally $\left(\frac{I_C}{V_T}\right)$ is conductance; more appropriately transfer conductance between the output current (I_C) and the thermal voltage (V_T); which changes the input voltage (V_{BE}). This transfer conductance is given the name mutual conductance, g_m. Hence, Eq. (3.9) simplifies as;

$$i_C = I_C + \left(\frac{I_C}{V_T}\right) v_{be} = I_C + g_m v_{be} = I_C + g_m v_{be} \tag{3.10}$$

Equation (3.10) indicates that the total collector current consists of (a) DC collector current (I_C) and the (b) ac collector current (i_c). So, Eq. (3.10) relates the ac collector current as;

$$i_c = \frac{I_C}{V_T} v_{be} = g_m v_{be} \tag{3.11}$$

$$i_C = I_C + g_m v_{be} = I_C + i_c \tag{3.12}$$

Here, $g_m = \frac{I_C}{V_T}$ (3.13)

We observe from Eq. (3.13) that the transconductance (g_m) of the BJT is directly proportional to the collector bias current (I_C). The value of the transconductance of the BJT is always higher than that of the MOSFET because g_m of the MOSFET depends on the dimension (L & W) of the MOSFET. The small-signal representation of the g_m is approximately equated to the tangent at the Q-point in Fig. 3.2.

Similarly, the base current is defined as;

$$i_B = \frac{i_C}{\beta} = \frac{I_C + g_m v_{be}}{\beta} = \frac{I_C}{\beta} + \frac{1}{\beta}\left(\frac{I_C}{V_T} v_{be}\right) = I_B + i_b \tag{3.14}$$

The total base current in Eq. (3.14) is composed of the dc base current (I_B) and the ac base current (i_b). The swing of the ac input voltage produces the corresponding swing in the collector current as indicated in Fig. 3.2 at the Q-point.

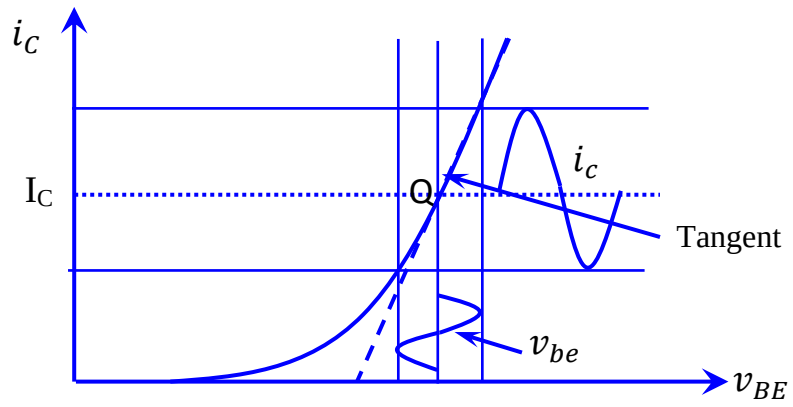

Fig. 3.2 Graphical model representation of I_C vs V_{BE}

3.3 Circuit model of CE for Input resistance

3.4 The base current is the input current that drives the transistor in the conduction region, as in Fig. 3.3 (a).

3.5 The dc base current is written as;

$$I_B = \frac{I_C}{\beta} \text{ and} \tag{3.15}$$

Similarly, the ac base current is expressed as;

$$i_b = \frac{1}{\beta}\left(\frac{I_C}{V_T} v_{be}\right) = \frac{g_m}{\beta} v_{be} \tag{3.16}$$

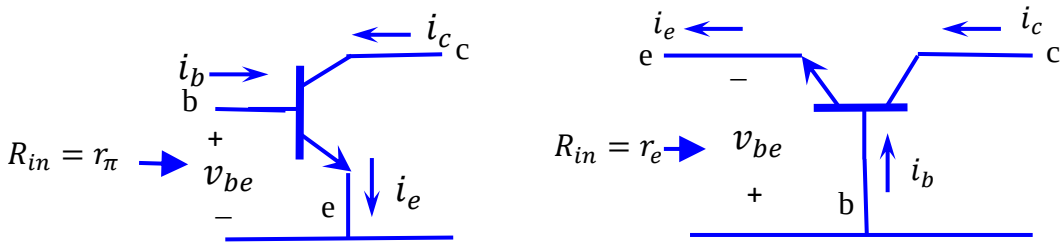

Fig. 3.3 Circuit Symbol model of the BJT (a) CE and (b) CB configurations

The small-signal input resistance looking into the base terminal in the CE configuration of the BJT is shown in Fig. 3.3 (a), given the name r_π, is expressed as;

$$R_{in(CE)} = r_\pi = \frac{v_{be}}{i_b} = \frac{v_{be}}{i_c/\beta} = \beta \frac{v_{be}}{i_c} = \frac{\beta}{g_m} \tag{3.17}$$

Merging Eqs. (3.16) and (3.17) yield;

$$R_{in(CE)} = \frac{v_{be}}{i_b} = \frac{\beta}{g_m} = r_\pi \tag{3.18}$$

Hence, $\beta = g_m r_\pi$ (3.19)

Equation (3.18) indicates [3-16] that the small-signal input resistance of a CE configuration of the BJT is directly proportional to β and Eq. (3.17) indicates that it is inversely proportional to the bias collector current, I_C. Substituting for g_m in Eq. (3.18) from Eq. (3.13) yields;

$$r_\pi = \frac{\beta}{g_m} = \frac{\beta}{\frac{I_C}{V_T}} = \beta \frac{V_T}{I_C} = \frac{V_T}{I_C/\beta} = \frac{V_T}{I_B} \tag{3.20}$$

In the case of the MOSFET, the gate current corresponds to the base current in the BJT. The gate current in MOSFET is zero (0), so input resistance is infinite.

3.4 Circuit model of CB for Input resistance

In the case of a common-base configuration of the BJT, the input drives current is the emitter current, as in Fig. 3.3 (b). To find the input resistance seen at the input (emitter) terminal, we have to represent the base current in terms of the emitter current i.e.

$$i_E = \frac{i_C}{\alpha} = \frac{I_C}{\alpha} + \frac{i_c}{\alpha} = I_E + i_e \tag{3.21}$$

The ac emitter current is now expressed as;

$$i_e = \frac{i_c}{\alpha} \tag{3.22}$$

Substituting for i_c from Eq. (3.11) in Eq. (3.22) yields;

$$i_e = \frac{i_c}{\alpha} = \frac{1}{\alpha} x \frac{I_C}{V_T} v_{be} = \left(\frac{I_C}{\alpha}\right) x \frac{1}{V_T} v_{be} = \frac{I_E}{V_T} v_{be} \tag{3.23}$$

Now, the small-signal input resistance looking into the emitter terminal in the common-base configuration shown in Fig. 3.3 (b) of the BJT, represented by r_e, is defined as;

$$R_{in(CB)} = r_e = \frac{v_{be}}{i_e} = \frac{V_T}{I_E} \tag{3.24}$$

Substituting for $\left(\frac{v_{be}}{i_e}\right)$ from Eq. (3.23) in Eq. (3.24) yields;

$$r_e = \frac{v_{be}}{i_e} = \frac{v_{be}}{\frac{I_E}{V_T} v_{be}} = \frac{V_T}{I_E} \tag{3.25}$$

$$R_{in(CB)} = r_e = \frac{v_{be}}{i_e} = \frac{V_T}{\alpha I_E/\alpha} = \alpha \frac{V_T}{I_C} = \frac{\alpha}{g_m} \tag{3.26}$$

$$\alpha = g_m r_e \tag{3.27}$$

Now, from Eq. (3.17), $v_{be} = r_\pi i_b = r_\pi \frac{i_e}{1+\beta}$

$$\frac{v_{be}}{i_e} = \frac{r_\pi}{1+\beta} = r_e$$

$$r_\pi = (1+\beta) r_e \tag{3.28}$$

Equation (3.28) gives a relationship between input resistances of common-emitter (r_π) and common-base (r_e) configurations of the BJT.

3.5 T-model of the BJT

Although the hybrid--π model of the BJT is simple and suitable for analysing the amplifiers, the other model variant is more convenient in some situations. This variant is called the **T-model,** [4-16] as drawn in Fig. 3.4 (a).

If we just rotate the Fig. 3.4 (b) by 90^0 left and then horizontally, the structure looks like a T and hence its name was given as the T-model small-signal equivalent circuit as in Fig. 3.4 (b). We know that the plot of the collector current versus collector-to-emitter voltage does not remain constant but rather increases very slowly for a large change in the V_{CE} due to the Early effect. Hence, the BJT has a finite output resistance r_o. The small-signal T-model of the BJT including the output resistance r_o is drawn in Figs. 3.4 (c).

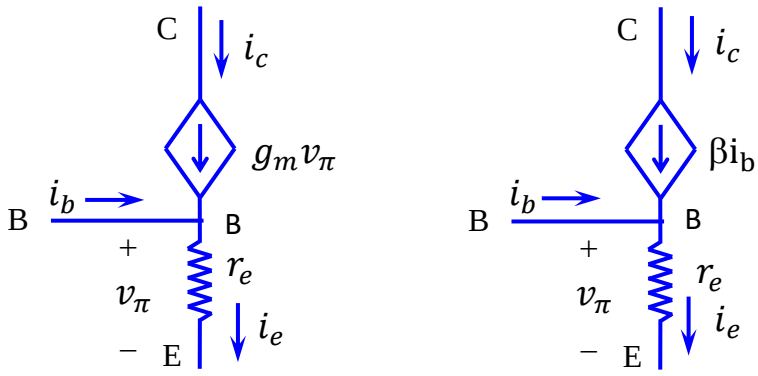

Fig. 3.4 (a) Vertical Circuit T-model of the BJT

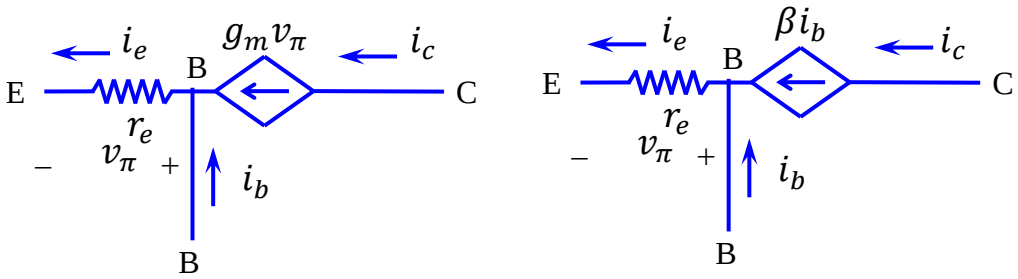

Fig. 3.4 (b) Horizontal Circuit T-model of the BJT

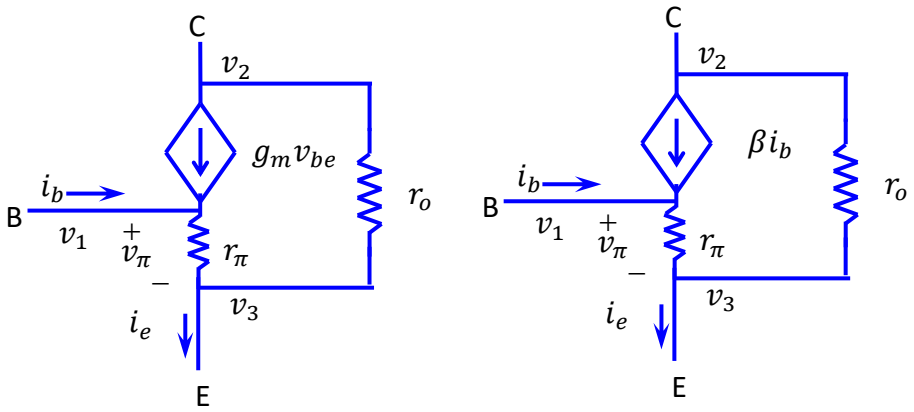

Fig. 3.4 (c) Vertical Circuit T- model of BJT including r_o

3.6 Hybrid-π Circuit model of the BJT

The hybrid-π circuit model of the BJT drawn in Fig. 2.8 (b) is repeated here for deriving the floating admittance matrix of the BJT, assuming r_μ as large as open-circuited and $r_{bb'}$ as small as short-circuited and hence considering these facts the hybrid-π small-signal equivalent circuit model of the BJT is shown in Fig. 3.4 (d).

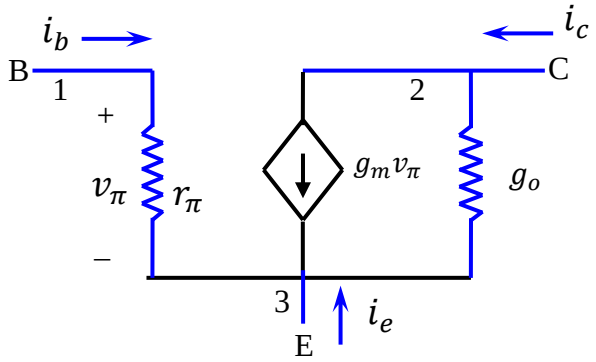

Fig. 3.4 (d) hybrid-π circuit model of the BJT including r_o

The currents and voltages [1-39] are related from Fig. 3.4 (d) as;

$$i_1 = i_b = g_\pi(v_b - v_e) = g_\pi(v_1 - v_3) = g_\pi v_1 + (0)v_2 - g_\pi v_3 \tag{3.29}$$

$$i_2 = i_c = g_o(v_c - v_e) + g_m(v_b - v_e) = g_m v_b + g_o v_c - (g_m + g_o)v_e$$

$$i_2 = i_c = g_m v_b + g_o v_c - (g_m + g_o)v_e \tag{3.30}$$

$$i_3 = i_e = g_\pi(v_e - v_b) + g_o(v_e - v_c) - g_m(v_b - v_e)$$

$$i_3 = i_e = -(g_\pi + g_m)v_b - g_o v_c + (g_\pi + g_m + g_o)v_e \tag{3.31}$$

The above equations (3.29), (3.30), and (3.31) are arranged in the form of a matrix [34-41] as;

$$\begin{bmatrix} i_1 = i_b \\ i_2 = i_c \\ i_3 = i_e \end{bmatrix} = \begin{bmatrix} 1 & 2 & 3 \\ g_\pi & 0 & -g_\pi \\ g_m & g_o & -g_m - g_o \\ -g_\pi - g_m & -g_o & g_\pi + g_m + g_o \end{bmatrix} \begin{bmatrix} v_1 = v_b \\ v_2 = v_c \\ v_3 = v_e \end{bmatrix} \quad (3.32)$$

Where, $g_\pi = 1/r_\pi$, $g_m = \beta/r_\pi$, and $g_o \Rightarrow 0$

The coefficient matrix in Eq. (3.32) is called the *floating admittance matrix* of the BJT as none of its terminals is taken as a reference for the other terminals. This Eq. (3.32) will be used to derive all transfer functions of any configuration BJT amplifier using low-frequency FAM of hybrid-π model.

Now, we would like to demonstrate the use of the floating admittance matrix developed for BJT in the hybrid-π model to obtain its different transfer functions in different configurations.

3.7 Circuit Model of the BJT Phase-Splitter Amplifier

The BJT phase-splitter amplifier [1-33] provides two types of amplified output voltages; one in phase with the input signal at the emitter terminal and the other out of phase of the input signal at the collector terminal. i.e. $v_e = A_e v_s \angle 0^0$ and $v_c = -A_c v_s = A_c v_s \angle 180^0$ as depicted in Figs 3.5. An elementary circuit of the BJT phase-splitter amplifier with two supply voltages V_{CC} and V_{EE} used to bias it is shown in Fig. 3.5. The ac circuit, shorting all capacitors and the dc supply voltages at low frequency, is drawn in Fig. 3.6.

Since the analysis is proposed to be done using the floating admittance matrix, the three terminals of the BJT are denoted as B→1 for the base, C→2 for the collector, and E→3 for the emitter.

The floating admittance matrix of a BJT in hybrid-π model [34-41] of Eq (3.32) is repeated here for ease in further analysis.

$$\begin{bmatrix} i_1 = i_b \\ i_2 = i_c \\ i_3 = i_e \end{bmatrix} = \begin{bmatrix} 1 & 2 & 3 \\ g_\pi & 0 & -g_\pi \\ g_m & g_o & -g_0 - g_m \\ -g_\pi - g_m & -g_o & g_\pi + g_m + g_o \end{bmatrix} \begin{bmatrix} v_1 = v_b \\ v_2 = v_c \\ v_3 = v_e \end{bmatrix} \tag{3.33}$$

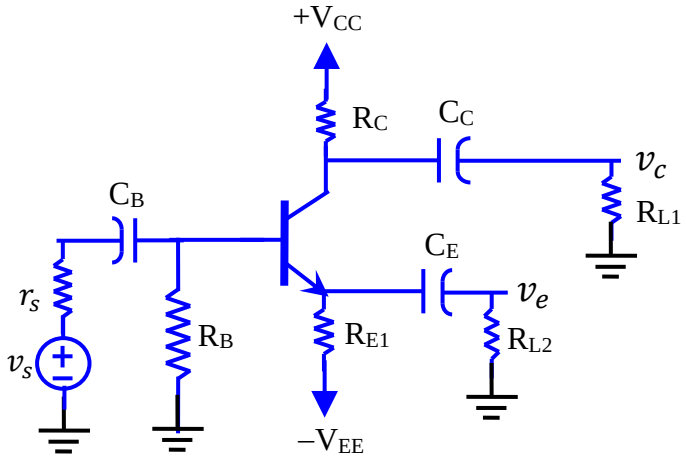

Fig. 3.5 Circuit Model of the BJT Phase-Splitter Amplifier

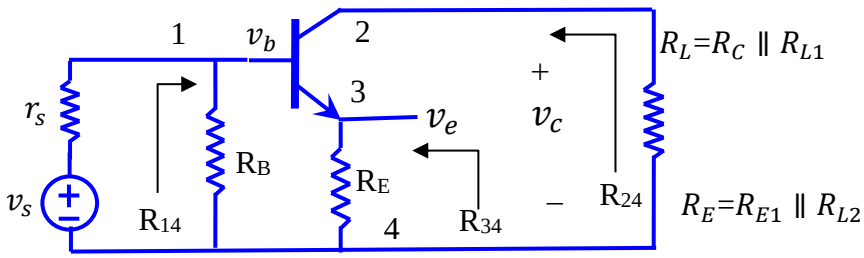

Fig. 3.6 AC circuit model of the BJT Phase-Splitter Amplifier

As the BJT phase-splitter has 4-nodes, the coefficient floating admittance matrix in 3 x 3 of the BJT (active element) in hybrid-π model in Eq. (3.33) is now transformed to 4 x 4 as;

$$\begin{bmatrix} 1 & 2 & 3 & 4 \\ g_\pi & 0 & -g_\pi & 0 \\ g_m & g_o & -g_m - g_o & 0 \\ -g_\pi - g_m & -g_o & g_\pi + g_m + g_o & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} 1 \\ 2 \\ 3 \\ 4 \end{bmatrix} \tag{3.34}$$

Similarly, the 4 x 4 floating admittance matrix of passive elements present in Fig. 3.6 of the BJT phase-splitter amplifier is written as;

$$\begin{matrix} 1 & 2 & 3 & 4 \end{matrix}\begin{bmatrix} g_s + G_B & 0 & 0 & -g_s - G_B \\ 0 & G_L & 0 & -G_L \\ 0 & 0 & G_E & -G_E \\ -g_s - G_B & -G_L & -G_E & g_s + G_B + G_E + G_L \end{bmatrix}\begin{matrix} 1 \\ 2 \\ 3 \\ 4 \end{matrix} \tag{3.35}$$

The overall floating admittance matrix of active and passive elements present in a BJT phase-splitter circuit of Fig. 3.6 can be obtained by merging Eqs. (3.34) and (3.35) as per node specifications that yields;

$$\begin{matrix} 1 & 2 & 3 & 4 \end{matrix}\begin{bmatrix} g_\pi + g_s + G_B & 0 & -g_\pi & -g_s - G_B \\ g_m & g_o + G_L & -g_m - g_o & -G_L \\ -g_\pi - g_m & -g_o & g_\pi + g_m + g_o + G_E & -G_E \\ -g_s - G_B & -G_L & -G_E & g_s + G_B + G_E + G_L \end{bmatrix}\begin{matrix} 1 \\ 2 \\ 3 \\ 4 \end{matrix} \tag{3.36}$$

Eq. (3.36) is the floating admittance matrix of a BJT phase-splitter circuit of Fig. 3.6. Now, we are interested in getting the overall floating admittance matrix of the common-emitter amplifier from the BJT phase-splitter amplifier [34-41] of Fig. 3.6. For that, the 3rd column is added to the 4th column in Eq. (3.36) to yield;

$$\begin{matrix} 1 & 2 & 3 & 4 \end{matrix}\begin{bmatrix} g_\pi + g_s + G_B & 0 & -g_\pi & -g_\pi - g_s - G_B \\ g_m & g_o + G_L & -g_m - g_o & -g_m - g_o - G_L \\ -g_\pi + g_m & -g_o & g_\pi + g_m + g_o + G_E & g_\pi + g_m + g_o + G_E - G_E \\ -g_s - G_B & -G_L & -G_E & -G_E + g_s + G_B + G_E + G_L \end{bmatrix}\begin{matrix} 1 \\ 2 \\ 3 \\ 4 \end{matrix} \tag{3.37}$$

Simplification of Eq. (3.37) yields;

$$\begin{bmatrix} 1 & 2 & 3 & 4 \\ g_\pi + g_s + G_B & 0 & -g_\pi & -g_\pi - g_s - G_B \\ g_m & g_O + G_L & -g_m - g_O & -g_m - g_O - G_L \\ -g_\pi - g_m & -g_O & g_\pi + g_m + g_O + G_E & g_\pi + g_m + g_O \\ -g_s - G_B & -G_L & -G_E & g_s + G_B + G_L \end{bmatrix} \begin{bmatrix} 1 \\ 2 \\ 3 \\ 4 \end{bmatrix} \tag{3.38}$$

Again, adding the 3rd row to the 4th row in Eq. (3.38) yields;

$$\begin{bmatrix} 1 & 2 & 3 & 4 \\ g_\pi + g_s + G_B & 0 & -g_\pi & -g_\pi - g_s - G_B \\ g_m & g_O + G_L & -g_m - g_O & -g_m - g_O - G_L \\ -g_\pi - g_m & -g_O & g_\pi + g_m + g_O + G_E & g_\pi + g_m + g_O \\ -g_\pi - g_m - g_s - G_B & -g_O - G_L & g_\pi + g_m + g_O + G_E - G_E & g_\pi + g_m + g_O + g_s + G_B + G_L \end{bmatrix} \begin{bmatrix} 1 \\ 2 \\ 3 \\ 4 \end{bmatrix} \tag{3.39}$$

Simplifying Eq. (3.39) yields;

$$\begin{bmatrix} 1 & 2 & 3 & 4 \\ g_\pi + g_s + G_B & 0 & -g_\pi & -g_\pi - g_s - G_B \\ g_m & g_O + G_L & -g_m - g_O & -g_m - g_O - G_L \\ -g_\pi - g_m & -g_O & g_\pi + g_m + g_O + G_E & g_\pi + g_m + g_O \\ -g_\pi - g_m - g_s - G_B & -g_O - G_L & g_\pi + g_m + g_O & g_\pi + g_m + g_O + g_s + G_B + G_L \end{bmatrix} \begin{bmatrix} 1 \\ 2 \\ 3 \\ 4 \end{bmatrix} \tag{3.40}$$

Now, deleting the original 3rd row and the 3rd column from Eq. (3.40) yields;

$$\begin{bmatrix} 1 & 2 & \cancel{3} & 4 \\ g_\pi + g_s + G_B & 0 & \cancel{-g_\pi} & -g_\pi - g_s - G_B \\ g_m & g_O + G_L & \cancel{-g_m - g_O} & -g_m - g_O - G_L \\ \cancel{-g_\pi - g_m} & \cancel{-g_O} & \cancel{g_\pi + g_m + g_O + G_E} & \cancel{g_\pi + g_m + g_O} \\ -g_\pi - g_m - g_s - G_B & -g_O - G_L & \cancel{g_\pi + g_m + g_O} & g_\pi + g_m + g_O + g_s + G_B + G_L \end{bmatrix} \begin{bmatrix} 1 \\ 2 \\ 3 \\ 4 \end{bmatrix} \tag{3.41}$$

Simplification of Eq. (3.41) yields;

$$\begin{bmatrix} 1 & 2 & 4 \\ g_\pi + g_s + G_B & 0 & -g_\pi - g_s - G_B \\ g_m & g_O + G_L & -g_m - g_O - G_L \\ -g_\pi - g_m - g_s - G_B & -g_O - G_L & g_\pi + g_m + g_O + g_s + G_B + G_L \end{bmatrix} \begin{bmatrix} 1 \\ 2 \\ 4 \end{bmatrix} \tag{3.42}$$

3.8 Circuit Model of the Common-Emitter Amplifier

Since the 3rd row and the 3rd column have been merged to the 4th row and the 4th column, the 4th row and the 4th column of Eq. (3.42) are now assigned the 3rd row and the 3rd column, and then Eq. (3.42) simplifies to;

$$\begin{bmatrix} 1 & 2 & 3 \\ g_\pi + g_s + G_B & 0 & -g_\pi - g_s - G_B \\ g_m & g_O + G_L & -g_m - g_O - G_L \\ -g_\pi - g_m - g_s - G_B & -g_O - G_L & g_\pi + g_m + g_O + g_s + G_B + G_L \end{bmatrix} \begin{bmatrix} 1 \\ 2 \\ 3 \end{bmatrix} \tag{3.43}$$

This Eq. (3.43) is the floating admittance matrix of a common-emitter amplifier in hybrid-π model. The circuit of a common-emitter amplifier is drawn as in Fig. 3.7 using this Eq. (3.43).

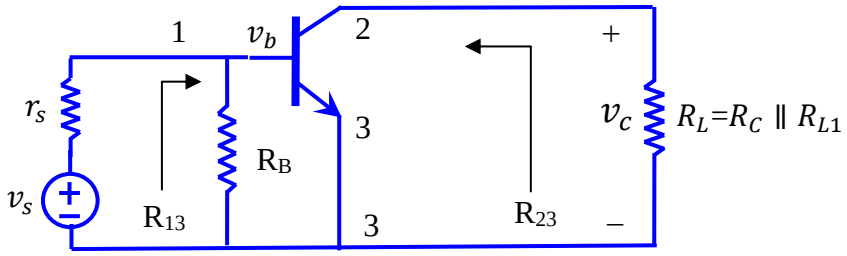

Fig. 3.7 AC Circuit Model of the Common-Emitter Amplifier

The floating admittance matrix for the circuit in Fig. 3.7, including the node currents and node voltages, is written as;

$$\begin{bmatrix} i_1 = i_b \\ i_2 = i_c \\ i_3 = i_e \end{bmatrix} \begin{bmatrix} 1 & 2 & 3 \\ g_\pi + g_s + G_B & 0 & -g_\pi - g_s - G_B \\ g_m & g_O + G_L & -g_m - g_O - G_L \\ -g_\pi - g_m - g_s - G_B & -g_O - G_L & g_\pi + g_m + g_O + g_s + G_B + G_L \end{bmatrix} \begin{bmatrix} v_1 = v_b \\ v_2 = v_c \\ v_3 = v_e \end{bmatrix} \tag{3.44}$$

The voltage gain [34-41] between the output terminals 2 & 3 and the input terminals 1 & 3 of a common-emitter amplifier in Fig. 3.7 using Eq. (3.44) is expressed as;

$$A_v|_{13}^{23} = sgn(2-3)sgn(1-3)(-1)^{2+3+1+3}\frac{|Y_{23}^{13}|}{|Y_{13}^{13}|} = -\frac{|Y_{23}^{13}|}{|Y_{13}^{13}|} \tag{3.45}$$

From Eq. (3.44), $|Y_{23}^{13}| = g_m$, $|Y_{13}^{13}| = g_O + G_L$

$$A_v|_{13}^{23} = -\frac{|Y_{23}^{13}|}{|Y_{13}^{13}|} = -\frac{g_m}{g_O+G_L} = -g_m(r_O||R_L) \cong -g_m R_L \tag{3.46}$$

The input resistance [34-41] between the input terminals 1 & 3 of a common-emitter amplifier in Fig. 3.7 using Eq. (3.44) is expressed as;

$$R_{in(13)} = \frac{|Y_{13}^{13}|}{|Y_3^3|}_{g_s=0} \tag{3.47}$$

$$|Y_{13}^{13}| = g_O + G_L$$

$$|Y_3^3|_{g_s=0} = \begin{vmatrix} g_\pi + g_s + G_B & 0 \\ g_m & g_O + G_L \end{vmatrix}$$

$$= (g_\pi + G_B)(g_O + G_L) = (g_\pi + G_B)(g_O + G_L)$$

$$R_{in(13)} = \frac{|Y_{13}^{13}|}{|Y_3^3|}_{g_s=0} = \frac{g_O+G_L}{(g_\pi+G_B)(g_O+G_L)} = \frac{1}{g_\pi+G_B} = r_\pi \parallel R_B \cong r_\pi \tag{3.48}$$

The output resistance [34-41] between the output terminals 2 & 3 of a common-emitter amplifier in Fig. 3.7 using Eq. (3.44) is expressed as;

$$R_{O(23)} = \frac{|Y_{23}^{23}|}{|Y_3^3|}_{G_L=0} \tag{3.49}$$

$$|Y_{23}^{23}| = g_\pi + g_s + G_B$$

$$|Y_3^3|_{G_L=0} = (g_\pi + g_s + G_B)(g_O + G_L) = (g_\pi + g_s + G_B)g_O$$

$$R_{O(23)} = \frac{|Y_{23}^{23}|}{|Y_3^3|}_{G_L=0} = \frac{g_\pi+g_s+G_B}{(g_\pi+g_s+G_B)g_O} = \frac{1}{g_O} = r_O \tag{3.50}$$

The current gain [34-41] between the output terminals 2 & 3 and the input terminals 1 & 3 of a common-emitter amplifier in Fig. 3.7 using Eq. (3.44) is expressed as;

$$A_i|_{13}^{23} = sgn(2-3)sgn(1-3)(-1)^9 \frac{|Y_{23}^{13}|}{|Y_3^3|} G_L = -\frac{|Y_{23}^{13}|}{|Y_3^3|} G_L \tag{3.51}$$

$$A_i|_{13}^{23} = -\frac{|Y_{23}^{13}|}{|Y_3^3|} G_L = -\frac{g_m}{(g_\pi + g_s + \cancel{G_B})(g_O + G_L)} G_L$$

$$= -\frac{g_m}{(g_\pi + g_s)(\cancel{g_O} + G_L)} G_L = -g_m \frac{r_\pi r_s}{(r_\pi + r_s)} = -g_m (r_\pi \parallel r_s) = -\beta \tag{3.52}$$

The Power gain [34-41] between the output terminals 2 & 3 and the input terminals 1 & 3 of a common-emitter amplifier in Fig. 3.7 is written as;

$$A_P|_{13}^{23} = A_v|_{13}^{23} x A_i|_{13}^{23} = (-g_m R_L)(-\beta) = \beta g_m R_L \tag{3.53}$$

3.9 Circuit Model of the Common-Collector Amplifier

The common-collector amplifier can be analysed using the floating admittance matrix of the BJT phase-splitter amplifier of Eq. (3.36). For that, the 2nd row is added to the 4th row in Eq. (3.36) to yield;

$$\begin{bmatrix} 1 & 2 & 3 & 4 \\ g_\pi + g_s + G_B & 0 & -g_\pi & -g_s - G_B \\ g_m & g_O + G_L & -g_m - g_O & -G_L \\ -g_\pi - g_m & -g_O & g_\pi + g_m + g_O + G_E & -G_E \\ g_m - g_s - G_B & g_O + G_L - G_L & -g_m - g_O - G_E & -G_L + g_s + G_B + G_E + G_L \end{bmatrix} \begin{bmatrix} 1 \\ 2 \\ 3 \\ 4 \end{bmatrix} \tag{3.54}$$

Simplification of Eq. (3.54) yields;

$$\begin{bmatrix} 1 & 2 & 3 & 4 \\ g_\pi + g_s + G_B & 0 & -g_\pi & -g_s - G_B \\ g_m & g_O + G_L & -g_m - g_O & -G_L \\ -g_\pi - g_m & -g_O & g_\pi + g_m + g_O + G_E & -G_E \\ g_m - g_s - G_B & g_O & -g_m - g_O - G_E & g_s + G_B + G_E \end{bmatrix} \begin{bmatrix} 1 \\ 2 \\ 3 \\ 4 \end{bmatrix} \tag{3.55}$$

Now, adding the 2nd column to the 4th column in Eq. (3.55) yields;

$$\begin{bmatrix} 1 & 2 & 3 & 4 \\ g_\pi + g_s + G_B & 0 & -g_\pi & -g_s - G_B \\ g_m & g_O + G_L & -g_m - g_O & g_O + G_L - G_L \\ -g_\pi - g_m & -g_O & g_\pi + g_m + g_O + G_E & -g_O - G_E \\ g_m - g_s - G_B & g_O & -g_m - g_O - G_E & g_O + g_s + G_B + G_E \end{bmatrix} \begin{bmatrix} 1 \\ 2 \\ 3 \\ 4 \end{bmatrix} \quad (3.56)$$

Simplification of Eq. (3.56) yields;

$$\begin{bmatrix} 1 & 2 & 3 & 4 \\ g_\pi + g_s + G_B & 0 & -g_\pi & -g_s - G_B \\ g_m & g_O + G_L & -g_m - g_O & g_O \\ -g_\pi - g_m & -g_O & g_\pi + g_m + g_O + G_E & -g_O - G_E \\ g_m - g_s - G_B & g_O & -g_m - g_O - G_E & g_O + g_s + G_B + G_E \end{bmatrix} \begin{bmatrix} 1 \\ 2 \\ 3 \\ 4 \end{bmatrix} \quad (3.57)$$

Now, deleting the original 2nd row and the 2nd column of Eq. (3.57) yields;

$$\begin{bmatrix} 1 & \cancel{2} & 3 & 4 \\ g_\pi + g_s + G_B & \cancel{0} & -g_\pi & -g_s - G_B \\ \cancel{g_m} & \cancel{g_O + G_L} & \cancel{-g_m - g_O} & \cancel{g_O} \\ -g_\pi - g_m & \cancel{-g_O} & g_\pi + g_m + g_O + G_E & -g_O - G_E \\ g_m - g_s - G_B & \cancel{g_O} & -g_m - g_O - G_E & g_O + g_s + G_B + G_E \end{bmatrix} \begin{bmatrix} 1 \\ 2 \\ 3 \\ 4 \end{bmatrix} \quad (3.58)$$

Equation (3.58) simplifies after assigning the 2nd row and the 2nd column to the 4th row and 4th column that yields;

$$\begin{bmatrix} 1 & 3 & 2 \\ g_\pi + g_s + G_B & -g_\pi & -g_s - G_B \\ -g_\pi - g_m & g_\pi + g_m + g_O + G_E & -g_O - G_E \\ g_m - g_s - G_B & -g_m - g_O - G_E & g_s + g_o + G_B + G_E \end{bmatrix} \begin{bmatrix} 1 \\ 3 \\ 2 \end{bmatrix} \quad (3.59)$$

Equation (3.59) is the floating admittance matrix of the common-collector amplifier derived from Eq. (3.36) of the BJT phase-splitter circuit in Fig. 3.6. The common-collector amplifier circuit is drawn from the floating admittance matrix of the Eq. (3.59) as Fig. 3.8. The conductance G_E may be equal to G_{E1}+G_L.

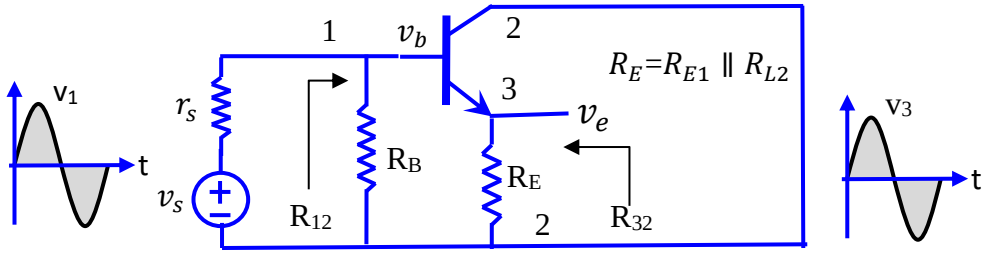

Fig. 3.8 AC Circuit Model the Common-Collector Amplifier

The collector terminal of the BJT is common to both the input and output sides in Fig. 3.8, and hence it is called a common-collector amplifier. The floating admittance matrix for the circuit in Fig. 3.8, along with the currents and voltages, is written as;

$$\begin{bmatrix} i_1 = i_b \\ i_3 = i_e \\ i_2 = i_c \end{bmatrix} \begin{bmatrix} 1 & 3 & 2 \\ g_\pi + g_s + G_B & -g_\pi & -g_s - G_B \\ -g_\pi - g_m & g_\pi + g_m + g_O + G_E & -g_O - G_E \\ g_m - g_s - G_B & -g_m - g_O - G_E & g_O + g_s + G_B + G_E \end{bmatrix} \begin{bmatrix} v_1 = v_b \\ v_3 = v_e \\ v_2 = v_c \end{bmatrix} \tag{3.60}$$

The voltage gain [34-41] between the output terminals 3 & 2 and the input terminals 1 & 2 of a common-collector amplifier in Fig. 3.8 is written as;

$$A_v|_{12}^{32} = sgn(3-2)sgn(1-2)(-1)^8 \frac{|Y_{32}^{12}|}{|Y_{12}^{12}|} = -\frac{|Y_{32}^{12}|}{|Y_{12}^{12}|} \tag{3.61}$$

From Eq. (3.60), $|Y_{32}^{12}| = -g_\pi - g_m$, $|Y_{12}^{12}| = g_\pi + g_m + g_O + G_E$

$$A_v|_{12}^{32} = -\frac{|Y_{32}^{12}|}{|Y_{12}^{12}|} = -\frac{-g_\pi - g_m}{g_\pi + g_m + \cancel{g_O} + G_E} = \frac{g_\pi + g_m}{g_\pi + g_m + G_E} = \frac{(1+\beta)R_E}{r_\pi + (1+\beta)R_E}$$

$$= \frac{R_E}{R_E + \frac{r_\pi}{(1+\beta)}} = \frac{R_E}{R_E + \frac{(1+\beta)r_e}{(1+\beta)}} = \frac{R_E}{R_E + r_e} \cong 1 \text{ (ideal condition of EF)} \tag{3.62}$$

The current gain [34-41] between the output terminals 3 & 2 and the input terminals 1 & 2 of a common-collector amplifier in Fig. 3.8 using Eq. (3.60) is expressed as;

$$A_i|_{12}^{32} = sgn(3-2)sgn(1-2)(-1)^8 \frac{|Y_{32}^{12}|}{|Y_2^2|} G_E = -\frac{|Y_{32}^{12}|}{|Y_2^2|} G_E \tag{3.63}$$

From Eq. (3.60), $|Y_{32}^{12}| = -g_\pi - g_m$

$$|Y_2^2| = \begin{vmatrix} g_\pi + \cancel{g_s + G_B} & -g_\pi \\ -g_\pi - g_m & g_\pi + g_m + \cancel{g_O} + G_E \end{vmatrix}$$

$$= \begin{vmatrix} g_\pi & -g_\pi \\ -g_\pi - g_m & g_\pi + g_m + G_E \end{vmatrix} = \begin{vmatrix} g_\pi & 0 \\ -g_\pi - g_m & G_E \end{vmatrix} = g_\pi G_E$$

$$A_i|_{12}^{32} = -\frac{|Y_{32}^{12}|}{|Y_2^2|} G_E = -\frac{-g_\pi - g_m}{g_\pi G_E} G_E = (1+\beta) \quad \text{(CC current gain)} \tag{3.64}$$

The input resistance [34-41] between terminals 1 & 2 of a common-collector amplifier in Fig. 3.8 using Eq. (3.60) is expressed as;

$$R_{in(12)} = \frac{|Y_{12}^{12}|}{|Y_2^2|}_{g_s=0} \tag{3.65}$$

From Eq. (3.60), $|Y_{12}^{12}| = g_\pi + g_m + g_O + G_E$

$$|Y_2^2|_{g_s=0} = \begin{vmatrix} g_\pi + \cancel{G_B} & -g_\pi \\ -g_\pi - g_m & g_\pi + g_m + g_O + G_E \end{vmatrix} = \begin{vmatrix} g_\pi & 0 \\ -g_\pi - g_m & g_O + G_E \end{vmatrix}$$

$$= g_\pi(g_O + G_E)$$

$$R_{in(12)} = \frac{|Y_{12}^{12}|}{|Y_2^2|}_{g_s=0} = \frac{g_\pi + g_m + \cancel{g_O} + G_E}{g_\pi(\cancel{g_O} + G_E)} = \frac{g_\pi + g_m + G_E}{g_\pi G_E} = r_\pi + (1+\beta)R_E$$

$$= (1+\beta)r_e + (1+\beta)R_E = (1+\beta)(r_e + R_E) \tag{3.66}$$

The output resistance [34-41] between terminals 3 & 2 of a common-collector amplifier in Fig. 3.8 is expressed as;

$$R_{O(32)} = \frac{|Y_{32}^{32}|}{|Y_2^2|}_{G_E=0} \tag{3.67}$$

From Eq. (3.60), $|Y_{32}^{32}| = g_\pi + g_s + G_B$

$$|Y_2^2|_{G_E=0} = \begin{vmatrix} g_\pi + g_s + G_B & -g_\pi \\ -g_\pi - g_m & g_\pi + g_m + \cancel{g_O} + \cancel{G_E} \end{vmatrix}$$

$$= \begin{vmatrix} g_\pi + g_s + \cancel{G_B} & -g_\pi \\ -g_\pi - g_m & (1+\beta)g_\pi \end{vmatrix} = \begin{vmatrix} g_\pi + g_s & g_s \\ -g_\pi - g_m & 0 \end{vmatrix}$$

$$= (g_\pi + g_m)g_s$$

$$R_{O(32)} = \frac{|Y_{32}^{32}|}{|Y_2^2|}_{G_L=0} = \frac{g_\pi + g_s + \cancel{G_B}}{(g_\pi + g_m)g_s} = \frac{g_\pi + g_s}{g_\pi(1+\beta)g_s} = \frac{r_\pi + r_s}{1+\beta} \tag{3.68}$$

The power gain [34-41] between the output terminals 3 & 2 and input terminals 1 & 2 of a common-collector amplifier in Fig. 3.8 is written as;

$$A_P|_{12}^{32} = A_v|_{12}^{32} x A_i|_{12}^{32} = \left(\frac{R_E}{R_E + r_e}\right)(1+\beta) \cong 1+\beta \tag{3.69}$$

3.10 Circuit Model of the Common-Base Amplifier

The floating admittance of the common-base amplifier using the hybrid-π model of the BJT can be obtained using Eq. (3.36) of a BJT phase-splitter amplifier in Fig. 3.6. For that, the 1st row is added to the 4th row in Eq. (3.36) to yield;

$$\begin{bmatrix} 1 & 2 & 3 & 4 \\ g_\pi + g_s + G_B & 0 & -g_\pi & -g_s - G_B \\ g_m & g_o + G_L & -g_m - g_o & -G_L \\ -g_\pi - g_m & -g_o & g_\pi + g_m + g_o + G_E & -G_E \\ g_\pi + g_s + G_B - g_s - G_B & -G_L & -g_\pi - G_E & -g_s - G_B + g_s + G_B + G_E + G_L \end{bmatrix} \begin{bmatrix} 1 \\ 2 \\ 3 \\ 4 \end{bmatrix} \tag{3.70}$$

Simplification of Eq. (3.70) yields;

$$\begin{bmatrix} 1 & 2 & 3 & 4 \\ g_\pi + g_s + G_B & 0 & -g_\pi & -g_s - G_B \\ g_m & g_o + G_L & -g_m - g_o & -G_L \\ -g_\pi - g_m & -g_o & g_\pi + g_m + g_o + G_E & -G_E \\ g_\pi & -G_L & -g_\pi - G_E & G_E + G_L \end{bmatrix} \begin{bmatrix} 1 \\ 2 \\ 3 \\ 4 \end{bmatrix} \tag{3.71}$$

Now, adding the 1st column to the 4th column in Eq. (3.71) yields;

$$\begin{bmatrix} 1 & 2 & 3 & 4 \\ g_\pi + g_s + G_B & 0 & -g_\pi & g_\pi + g_s + G_B - g_s - G_B \\ g_m & g_o + G_L & -g_m - g_o & g_m - G_L \\ -g_\pi - g_m & -g_o & g_\pi + g_m + g_o + G_E & -g_\pi - g_m - G_E \\ g_\pi & -G_L & -g_\pi - G_E & g_\pi + G_E + G_L \end{bmatrix} \begin{bmatrix} 1 \\ 2 \\ 3 \\ 4 \end{bmatrix} \tag{3.72}$$

Simplification of Eq. (3.72) and deleting the original 1st row and the 1st column yields;

$$\begin{bmatrix} \cancel{1} & 2 & 3 & 4 \\ \cancel{g_\pi + g_s + G_B} & \cancel{0} & \cancel{-g_\pi} & \cancel{g_\pi} \\ \cancel{g_m} & g_o + G_L & -g_m - g_o & g_m - G_L \\ \cancel{-g_\pi - g_m} & -g_o & g_\pi + g_m + g_o + G_E & -g_\pi - g_m - G_E \\ \cancel{g_\pi} & -G_L & -g_\pi - G_E & g_\pi + G_E + G_L \end{bmatrix} \begin{bmatrix} 1 \\ 2 \\ 3 \\ 4 \end{bmatrix} \tag{3.73}$$

Eq. (3.73) simplifies as;

$$\begin{bmatrix} 2 & 3 & 4 \\ g_O + G_L & -g_m - g_O & g_m - G_L \\ -g_O & g_\pi + g_m + g_O + G_E & -g_\pi - g_m - G_E \\ -G_L & -g_\pi - G_E & g_\pi + G_E + G_L \end{bmatrix} \begin{bmatrix} 2 \\ 3 \\ 4 \end{bmatrix} \tag{3.74}$$

Since the 1st row and the 1st column were added to the 4th row, and 4th column, the 4th row and 4th column are designated as the 1st row and the 1st column with $G_E = G_E + g_s$ as;

$$\begin{bmatrix} 2 & 3 & 1 \\ g_O + G_L & -g_m - g_O & g_m - G_L \\ -g_O & g_\pi + g_m + g_O + g_s + G_E & -g_\pi - g_m - g_s - G_E \\ -G_L & -g_\pi - g_s - G_E & g_\pi + g_s + G_E + G_L \end{bmatrix} \begin{bmatrix} 2 \\ 3 \\ 1 \end{bmatrix} \tag{3.75}$$

Equation (3.75) is the floating admittance matrix of common-base amplifier in the hybrid-π model. Eq. (3.75) suggests a common-base amplifier's circuit of Fig. 3.9. The base terminal of the BJT is common to both input and output sides in Fig. 3.9, and hence it is called a common-base amplifier.

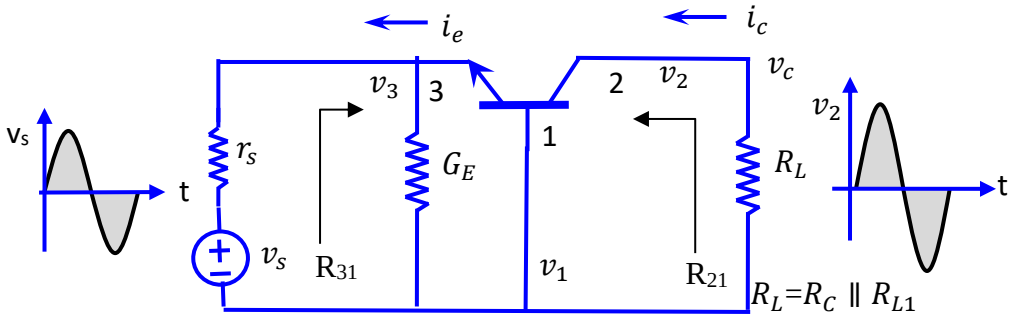

Fig. 3.9 AC Circuit Model of the Common-Base Amplifier

The load resistance could be $R_L = R_C \parallel R_{L1}$.

The voltage gain [34-41] between the output terminals 2 & 1 and the input terminals 3 & 1 of a common-bas amplifier in Fig. 3.9 is written as;

$$A_v|_{31}^{21} = sgn(2-1)sgn(3-1)(-1)^{2+1+3+1}\frac{|Y_{21}^{31}|}{|Y_{31}^{31}|} = -\frac{|Y_{21}^{31}|}{|Y_{31}^{31}|} \tag{3.76}$$

From Eq. (3.75), $|Y_{21}^{31}| = -g_m - g_O$, $|Y_{31}^{31}| = g_O + G_L$

$$A_v|_{31}^{21} = -\frac{|Y_{21}^{31}|}{|Y_{31}^{31}|} = -\frac{-g_m - g_O}{g_O + G_L} = \frac{g_m}{G_L} = g_m R_L \tag{3.77}$$

The current gain [34-41] between the output terminals 2 & 1 and the input terminals 3 & 1 using Eq. (3.75) of a common-bas amplifier in Fig. 3.9 is expressed as;

$$A_i|_{31}^{21} = sgn(2-1)sgn(3-1)(-1)^{2+1+3+1}\frac{|Y_{21}^{31}|}{|Y_1^1|}G_L = -\frac{|Y_{21}^{31}|}{|Y_1^1|}G_L \tag{3.78}$$

From Eq. (3.75), $|Y_1^1| = \begin{vmatrix} g_O + G_L & -g_m - g_O \\ -g_O & g_\pi + g_m + g_O + g_s \end{vmatrix} = (g_\pi + g_m)G_L$

$$A_i|_{31}^{21} = -\frac{|Y_{21}^{31}|}{|Y_1^1|}G_L = -\frac{-g_m - g_O}{(g_\pi + g_m)G_L}G_L = \frac{g_m}{g_\pi + g_m} = \frac{\beta}{\beta+1} = \alpha \tag{3.79}$$

The input resistance [34-41] between the input terminals 3 & 1 of a common-base amplifier in Fig. 3.9 is expressed as;

$$R_i = R_{i(31)} = \frac{|Y_{31}^{31}|}{|Y_1^1|}_{g_s=0} \tag{3.80}$$

From Eq. (3.75), $|Y_{31}^{31}| = g_O + G_L$

$$|Y_1^1|_{g_s=0}\begin{vmatrix} g_O + G_L & -g_m - g_O \\ -g_O & g_\pi + g_m + g_O + g_s + G_E \end{vmatrix} = \{g_\pi + g_m + G_E\}G_L$$

$$= \{r_\pi + (1+\beta)R_E\}G_L g_\pi G_E$$

$$R_i = R_{i(31)} = \frac{|Y_{31}^{31}|}{|Y_1^1|}_{g_s=0} = \frac{g_O + G_L}{\{r_\pi + (1+\beta)R_E\}G_L g_\pi G_E} = \frac{r_\pi R_E}{\{r_\pi + (1+\beta)R_E\}}$$

$$= \frac{r_\pi R_E}{(1+\beta)(r_e + R_E)} = \frac{r_\pi}{(1+\beta)} = \frac{(1+\beta)r_e}{(1+\beta)} = r_e = \frac{1}{g_m} \tag{3.81}$$

The output resistance [34-41] between the output terminals 2 & 1 of a common-base amplifier in Fig. 3.9 is expressed as;

$$R_{O(21)} = \frac{|Y_{21}^{21}|}{|Y_1^1|}_{G_L=0} \tag{3.82}$$

From Eq. (3.75), $|Y_{21}^{21}| = g_\pi + g_m + g_O + g_s + G_E = \{r_\pi + (1+\beta)R_E\}g_\pi G_E$

$$|Y_1^1|_{G_L=0} = \begin{vmatrix} g_O + \cancel{G_L} & -g_m - g_O \\ -g_O & g_\pi + g_m + g_O + \cancel{g_s} + G_E \end{vmatrix}$$

$$= \begin{vmatrix} g_O & -g_m - g_O \\ -g_O & g_\pi + g_m + g_O + G_E \end{vmatrix}$$

$$= \begin{vmatrix} g_O & -g_m - g_O \\ 0 & g_\pi + G_E \end{vmatrix} = g_O(g_\pi + G_E) = g_O(r_\pi + R_E)g_\pi G_E$$

$$R_O = R_{O(21)} = \frac{|Y_{21}^{21}|}{|Y_1^1|}_{G_L=0} = \frac{\{r_\pi+(1+\beta)R_E\}g_\pi G_E}{g_O(r_\pi+R_E)g_\pi G_E} = \frac{\{r_\pi+(1+\beta)R_E\}}{g_O(r_\pi+R_E)}$$

$$= \frac{r_\pi+(1+\beta)R_E}{g_O R_E} = \frac{(1+\beta)R_E}{g_O R_E} = (1+\beta)r_O \tag{3.83}$$

If we look at the output resistance through R_L', then

$$R_{O(21)} = (1+\beta)r_O \parallel R_C \cong R_C \tag{3.84}$$

The power gain [34-41] between the output terminals 2 & 1 and the input terminals 3 & 1 of a common-base amplifier in Fig. 3.9 is written as;

$$A_P|_{31}^{21} = A_v|_{31}^{21} x A_i|_{31}^{21} = (g_m R_L)\left(\frac{\beta}{1+\beta}\right) \cong g_m R_L \tag{3.85}$$

3.11 Circuit Model of the BJT Phase-Splitter Amplifier (Complete Analysis)

Now, we will analyse the BJT phase-splitter amplifier in detail using Fig. 3.5 and the corresponding floating admittance matrix of Eq (3.36). The common-emitter amplifier with an unbypassed emitter resistor (R_E), as shown in Fig. 3.6, is called a phase-splitter circuit. The floating admittance matrix of Eq (3.36) for the BJT phase-splitter amplifier shown in Fig. 3.6 is repeated here for ease in the further analysis.

$$\begin{bmatrix} 1 & 2 & 3 & 4 \\ g_\pi + g_s + G_B & 0 & -g_\pi & -g_s - G_B \\ g_m & g_O + G_L & -g_m - g_O & -G_L \\ -g_\pi - g_m & -g_O & g_\pi + g_m + g_O + G_E & -G_E \\ -g_s - G_B & -G_L & -G_E & g_s + G_B + G_E + G_L \end{bmatrix} \begin{bmatrix} 1 \\ 2 \\ 3 \\ 4 \end{bmatrix} \tag{3.86}$$

The voltage gain [34-41] between the output terminals 2 & 4 and the input terminals 1 & 4 of Fig. 3.6 using Eq. (3.86) is expressed as;

$$A_v|_{14}^{24} = \frac{v_{24}}{v_{14}} = sgn(2-4)sgn(1-4)(-1)^{11}\frac{|Y_{24}^{14}|}{|Y_{14}^{14}|} = -\frac{|Y_{24}^{14}|}{|Y_{14}^{14}|} \tag{3.87}$$

From Eq. (3.86), $|Y_{24}^{14}| = \begin{vmatrix} g_m & -g_m - \cancel{g_o} \\ -g_i - g_m & g_i + g_m + \cancel{g_o} + G_E \end{vmatrix}$

$$= \begin{vmatrix} g_m & -g_m \\ -g_i - g_m & g_i + g_m + G_E \end{vmatrix} = \begin{vmatrix} g_m & 0 \\ -g_\pi - g_m & G_E \end{vmatrix} = g_m G_E$$

$$|Y_{14}^{14}| = \begin{vmatrix} \cancel{g_o} + G_L & -g_m - \cancel{g_o} \\ -\cancel{g_o} & g_\pi + g_m + \cancel{g_o} + G_E \end{vmatrix} = (g_\pi + g_m + G_E)G_L$$

$$A_v|_{14}^{24} = \frac{v_{24}}{v_{14}} = -\frac{g_m G_E}{(g_\pi + g_m + G_E)G_L} = \frac{g_m r_\pi G_E R_E}{(r_\pi + (1+\beta)R_E)G_L} = \frac{\beta}{(r_\pi + (1+\beta)R_E)G_L}$$

$$= \left(-\frac{\beta R_L}{r_\pi + (1+\beta)R_E}\right) = -1 \text{ for } R_E = R_L = 1\ k\Omega \tag{3.88}$$

The input resistance [34-41] between input terminals 1 & 4 of a BJT phase-splitter circuit in Fig. 3.6 is expressed as;

$$R_{in} = R_{14} = \frac{|Y_{14}^{14}|}{|Y_4^4|}_{g_s=0} \tag{3.89}$$

From Eq. (3.86), $|Y_4^4|_{g_s=0} = \begin{vmatrix} g_\pi + \cancel{g_s} + G_B & 0 & -g_i \\ g_m & g_o + G_L & -g_m - g_o \\ -g_\pi - g_m & -g_o & g_\pi + g_m + g_o + G_E \end{vmatrix}$

$$\cong \begin{vmatrix} g_\pi + G_B & 0 & -g_i \\ g_m & G_L & -g_m \\ -g_\pi - g_m & 0 & g_\pi + g_m + G_E \end{vmatrix} \cong \begin{vmatrix} g_\pi & 0 & -g_\pi \\ g_m & G_L & -g_m \\ -g_\pi - g_m & 0 & g_\pi + g_m + G_E \end{vmatrix}$$

$$= \begin{vmatrix} g_\pi & 0 & 0 \\ g_m & G_L & 0 \\ -g_\pi - g_m & 0 & G_E \end{vmatrix} = g_\pi G_L G_E$$

$$R_{in} = R_{14} = \frac{(g_\pi + g_m + G_E)G_L}{g_\pi G_L G_E} = r_\pi + (1+\beta)R_E = (1+\beta)(r_e + R_E) \tag{3.90}$$

The current gain [34-41] between the output terminals 3 & 4 and the input terminals 1 & 4 of a BJT phase-splitter circuit in Fig. 3.6 is expressed as;

$$A_i|_{14}^{24} = \frac{i_2}{i_1} = sgn(2-4)sgn(1-4)(-1)^{11}\frac{|Y_{24}^{14}|}{|Y_4^4|}G_L = -\frac{|Y_{24}^{14}|}{|Y_4^4|}G_L \tag{3.91}$$

From Eq. (3.86), $|Y_4^4| = \begin{vmatrix} g_\pi + g_s + G_B & 0 & -g_\pi \\ g_m & g_o + G_L & -g_m - g_o \\ -g_\pi - g_m & -g_o & g_\pi + g_m + g_o + G_E \end{vmatrix}$

$$\cong \begin{vmatrix} g_\pi + g_s + G_B & 0 & -g_\pi \\ g_m & G_L & -g_m \\ -g_\pi - g_m & 0 & g_\pi + g_m + G_E \end{vmatrix} \cong \begin{vmatrix} g_\pi + \cancel{g_s} + G_B & 0 & \cancel{g_s} + G_B \\ g_m & G_L & 0 \\ -g_\pi - g_m & 0 & G_E \end{vmatrix}$$

$$= \{(g_\pi + \cancel{G_B})G_E + (g_\pi + g_m)\cancel{G_B}\}G_L = g_\pi G_E G_L$$

$$|Y_{24}^{14}| = g_m G_E$$

$$A_i|_{14}^{24} = -\frac{g_m G_E}{g_\pi G_E G_L} G_L = -\frac{g_m}{g_\pi} = -\beta \tag{3.92}$$

To derive the current gain including the source current, the voltage source is converted to the current source as in Fig. 3.10.

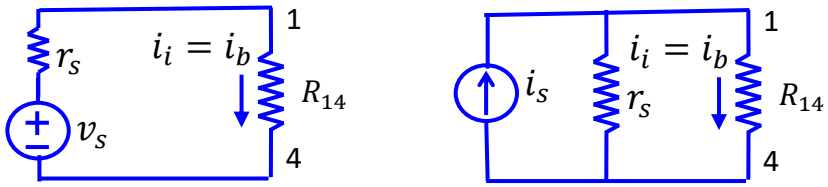

Fig. 3.10 Model of Voltage source converted to Current source

From Fig. 3.4, $i_1 = i_b = i_s \frac{r_s}{r_s + R_i} = i_s \frac{r_s}{r_s + r_\pi + (1+\beta)R_E}$

$$\frac{i_1}{i_s} = \frac{r_s}{r_s + r_\pi + (1+\beta)R_E} \tag{3.93}$$

The current gain [34-41], including source resistance in Fig. 3.10, is written as;

$$A_{is}|_{14}^{24} = \frac{i_2}{i_1} x \frac{i_1}{i_s} = \frac{i_2}{i_s} = (-\beta)\left\{\frac{r_s}{r_s + r_\pi + (1+\beta)R_E}\right\} = -\frac{\beta r_s}{r_s + r_\pi + (1+\beta)R_E} \tag{3.94}$$

$$v_{14} = v_s \frac{R_i}{r_s + R_i} = v_s \frac{r_\pi + (1+\beta)R_E}{r_s + r_\pi + (1+\beta)R_E} = v_s \tag{3.95}$$

The voltage gain, including the source resistance of the signal, is;

$$A_{vs} = \frac{v_o}{v_{14}} x \frac{v_{14}}{v_s} = \left(-\frac{\beta R_L}{r_\pi + (1+\beta)R_E}\right)\left(\frac{r_\pi + (1+\beta)R_E}{r_s + r_\pi + (1+\beta)R_E}\right) = -\frac{\beta R_L}{r_s + r_\pi + (1+\beta)R_E} \tag{3.96}$$

The output resistance [34-41] between the output terminals 2 and 4 of a BJT phase-splitter circuit in Fig. 3.6 is expressed as;

$$R_o = R_{24} = \frac{|Y_{24}^{24}|}{|Y_4^4|}_{G_L=0} \tag{3.97}$$

From Eq. (3.86), $|Y_4^4|_{G_L=0} = \begin{vmatrix} g_\pi + g_s & 0 & -g_\pi \\ g_m & g_o & -g_m - g_o \\ -g_\pi - g_m & -g_o & g_\pi + g_m + g_o + G_E \end{vmatrix}$

$$= \begin{vmatrix} g_\pi + g_s & 0 & -g_\pi \\ g_m & g_o & -g_m - g_o \\ g_s & 0 & G_E \end{vmatrix} = g_o\{(g_\pi + g_s)G_E + g_\pi g_s\}$$

$$|Y_{24}^{24}| = \begin{vmatrix} g_\pi + g_s & -g_\pi \\ -g_\pi - g_m & g_\pi + g_m + g_o + G_E \end{vmatrix} = \begin{vmatrix} g_s & -g_\pi \\ \cancel{g_o} + G_E & g_\pi + g_m + \cancel{g_o} + G_E \end{vmatrix}$$

$$= g_\pi(r_\pi + g_m g_\pi R_E + R_E)g_s G_E + g_\pi G_E = g_\pi\{r_\pi + (1+\beta)R_E\}g_s G_E + g_\pi G_E$$

$$= g_\pi[\{r_\pi + (1+\beta)R_E\} + r_s]g_s G_E$$

$$R_o = R_{24} = \frac{g_\pi[\{r_\pi+(1+\beta)R_E\}+r_s]g_s G_E}{g_o\{g_\pi g_s(r_\pi+r_s)G_E+g_\pi g_s\}} = \frac{g_\pi[\{r_\pi+(1+\beta)R_E\}+r_s]g_s G_E}{g_o\{r_\pi+r_s+R_E\}g_\pi g_s G_E}$$

$$= \frac{\{(r_s+r_\pi)+(1+\beta)R_E\}}{\{r_\pi+r_s+R_E\}} r_o = r_o\left[1 + \frac{\beta R_E}{r_\pi+r_s+R_E}\right] \quad (3.98)$$

The voltage gain [34-41] between the output terminals 3 & 4 and the input terminals 1 & 4 of a BJT phase-splitter circuit in Fig. 3.6 is written as;

$$A_v|_{14}^{34} = \frac{v_{24}}{v_{14}} = sgn(3-4)sgn(1-4)(-1)^{12}\frac{|Y_{34}^{14}|}{|Y_{14}^{14}|} = \frac{|Y_{34}^{14}|}{|Y_{14}^{14}|} \quad (3.99)$$

From Eq. (3.86), $|Y_{34}^{14}| = \begin{vmatrix} g_m & \cancel{g_o} + G_L \\ -g_\pi - g_m & -\cancel{g_o} \end{vmatrix} = (g_\pi + g_m)G_L = (1+\beta)g_\pi G_L$

$$|Y_{14}^{14}| = \begin{vmatrix} \cancel{g_o} + G_L & -g_\pi - g_m \\ -\cancel{g_o} & g_\pi + g_m + \cancel{g_o} + G_E \end{vmatrix} = G_L(g_\pi + g_m + G_E)$$

$$A_v|_{14}^{34} = \frac{v_{24}}{v_{14}} = \frac{(g_\pi+g_m)G_L}{G_L(g_\pi+g_m+G_E)} = \frac{g_\pi+g_m}{g_\pi+g_m+G_E} = \frac{(1+\beta)R_E}{r_\pi+(1+\beta)R_E} \cong 1 \quad (3.100)$$

The current gain [34-41] between the output terminals 3 & 4 and the input terminals 1 & 4 of BJT phase-splitter circuit in Fig. 3.6 is written as;

$$A_i|_{14}^{34} = \frac{i_2}{i_1} = gn(3-4)sgn(1-4)(-1)^{12}\frac{|Y_{34}^{14}|}{|Y_4^4|}G_E = \frac{|Y_{34}^{14}|}{|Y_4^4|}G_E$$

$$= \frac{(1+\beta)g_\pi G_L}{g_\pi G_E G_L}G_E = 1+\beta \quad (3.101)$$

The phase shift between voltages gains at the collector point and emitter point of a BJT phase-splitter circuit in Fig. 3.6 is given as;

$$A_v|_{14}^{34} = -A_v|_{14}^{24} = A_v|_{14}^{24}\angle 180^0.$$

The output resistance [34-41] between the output terminals 3 & 4 of a BJT phase-splitter amplifier in Fig. 3.6 is expressed as;

$$R_o = Z_{34} = \frac{|Y_{34}^{34}|}{|Y_4^4|}_{G_E=0} \quad (3.102)$$

$$|Y_{34}^{34}| = \begin{vmatrix} g_\pi + g_s & 0 \\ g_m & g_o + G_L \end{vmatrix} = (\cancel{g_o} + G_L)(g_\pi + g_s) = G_L(g_\pi + g_s)$$

$$|Y_4^4|_{G_E=0} = \begin{vmatrix} g_\pi + g_s & 0 & -g_\pi \\ g_m & \cancel{g_o} + G_L & -g_m - \cancel{g_o} \\ -g_\pi - g_m & -\cancel{g_o} & g_\pi + g_m + \cancel{g_o} \end{vmatrix} = \begin{vmatrix} g_\pi + g_s & 0 & g_s \\ g_m & G_L & G_L \\ -g_\pi - g_m & 0 & 0 \end{vmatrix}$$

$$= G_L(g_\pi + g_m)g_s$$

$$R_o = R_{34} = \frac{G_L(g_\pi+g_s)}{G_L(g_\pi+g_m)g_s} = \frac{g_\pi g_s(r_\pi+r_s)}{g_\pi(1+\beta)g_s} = \frac{r_\pi+r_s}{1+\beta} \quad (3.103)$$

The LTSpice simulation and Differential Amplifier using varies topologies have been discussed by Ibrahim, Hisham, Soh, Hamzah, Othman, Shilpa and Srilatha [42-43].

3.12 Simulation and Validation of Common Emitter Amplifier

The Common Emitter Amplifier discussed in Fig. 3.7 is constructed in LTSpice shown in Fig. 3.11. The biasing of the BJT with amplification factor β =100 is set to give I_E =2.85 mA. This results in $r_e = \frac{26mV}{2.85\ mA} \cong 9\ \Omega$ and $r_\pi = 919\ \Omega$. Thus the theoretical voltage gain obtained from Eq. (3.46) is

$$A_v = -g_m R_L = -\frac{100}{919}2000 = -217.6$$

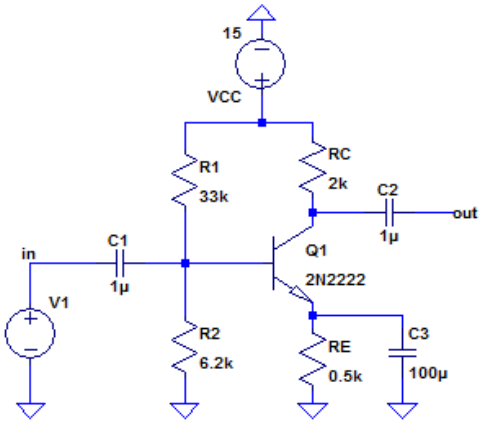

Fig. 3.11 LTSpice Circuit for Common Emitter Amplifier

The LTSpice plot is shown in Fig. 3.12. The $v_{O(pp)} \cong 440\ mV$ for an input voltage of 2 mV is shown in the plot of the LTSpice circuit. So, the practically achieved gain from the plot is

$$A_v = -\frac{440}{2} = -220$$

This value of the gain from the plot of LTSpice is close to the theoretical gain obtained from our Eq. (3.46) derived.

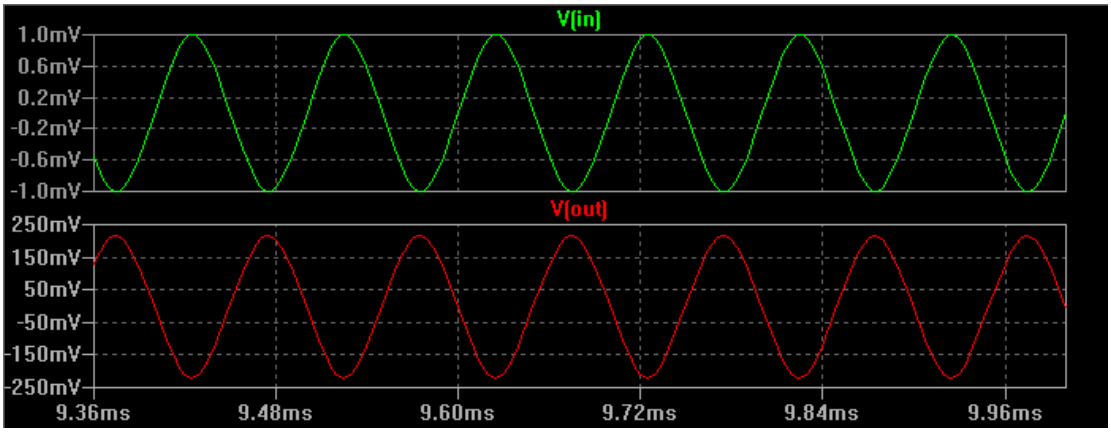

Fig. 3.12 LTSpice Response of the Common-Emitter Amplifier

3.13 Conclusions

All equations of the transfer function and self-port functions of the CE, CC, CB, and the phase-splitter amplifier circuits derived elegantly in this chapter using the floating admittance matrix approach corroborates the equations obtained using the conventional tools of KCL, KVL, and Thevenin's. Norton's etc. The advantage of computers can be taken for the complicated network to obtain the solution easily. Without the knowledge of electronics, even a pure mathematician can obtain the complete solution of any network, provided they know the matrix maneuvering technique. The LTSpice plot of Common Emitter Amplifier very closely results the voltage gain obtained theoretically.

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Chapter 4

Modelling of FET Amplifier

4.1 Introduction:

Before we start dealing with the modelling of the FET amplifier, the parameters that affect the model is discussed here. A simplified cross-section of symmetrical n-channel and p-channel JFETs is shown in Figs. 4.1 and 4.2, respectively [1-18]. In the n-channel between the two p-regions, the majority of carrier electrons flow from the source to the drain terminal. Hence, the JFET is called a ***majority-carrier device.*** It is normally ***ON device***. The two gate terminals shown in Figs. 4.1 and 4.2 are connected together to form a single gate terminal. The gate-to-source i.e. v_{GS} or v_{SG} is always reverse biased that appears across the two p-n junctions from both upper and lower sides. This increases the depletion width and decreases the thickness of the channel opening, reducing the flow of negative or positive charge carriers (electrons/ holes) from the source to the drain. Thus, the drain current, i_D flows in the direction of the flow of the holes and opposite to the flow of electrons.

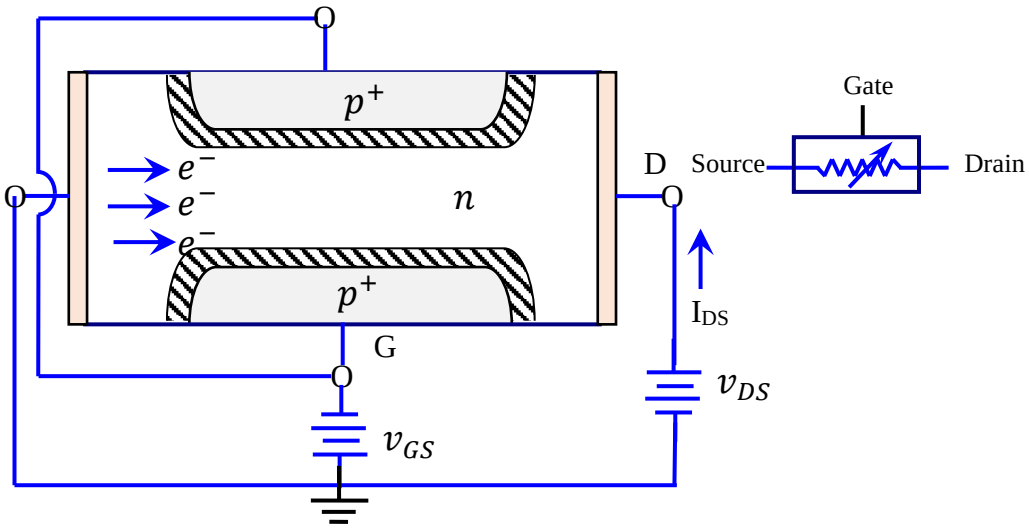


Fig. 4.1 Physical Cross-section of a symmetrical n-channel JFET

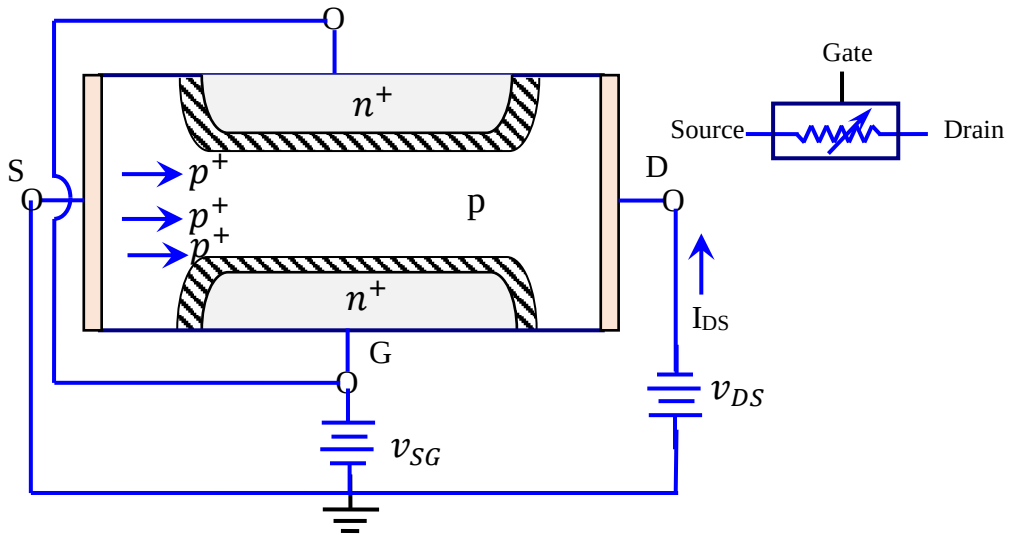
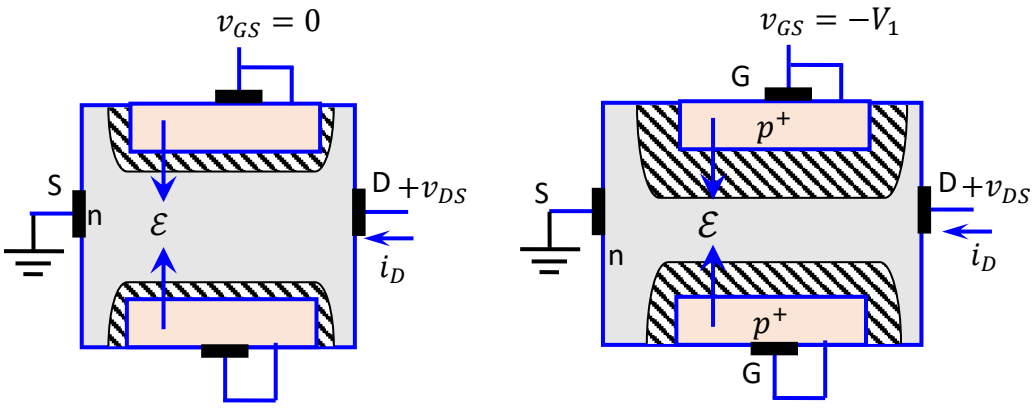


Fig. 4.2 Physical Cross-section of a symmetrical p-channel JFET

The *current direction and voltage polarities in the p-channel JFET are reversed* from those in the n-channel device. Also, the *p-channel JFET* is generally a *lower frequency* device than the n-channel JFET because the hole mobility is approximately two and half times lower than the electron mobility. Thus, the same dimension and external voltages applied across the nJFET produce more drain current than the pJFET.

Figure 4.3 (a) shows an n-channel JFET with zero volts applied to the gate i.e. $v_{GS} = 0$. If the source is at ground potential, and if a small positive drain voltage is applied, a linear drain current i_D is produced between the source and drain terminals. Since the n-channel acts essentially as a resistance, the i_D versus v_{DS} characteristic for small v_{DS} values are approximately linear, as shown in the Fig. 4.3 (a).



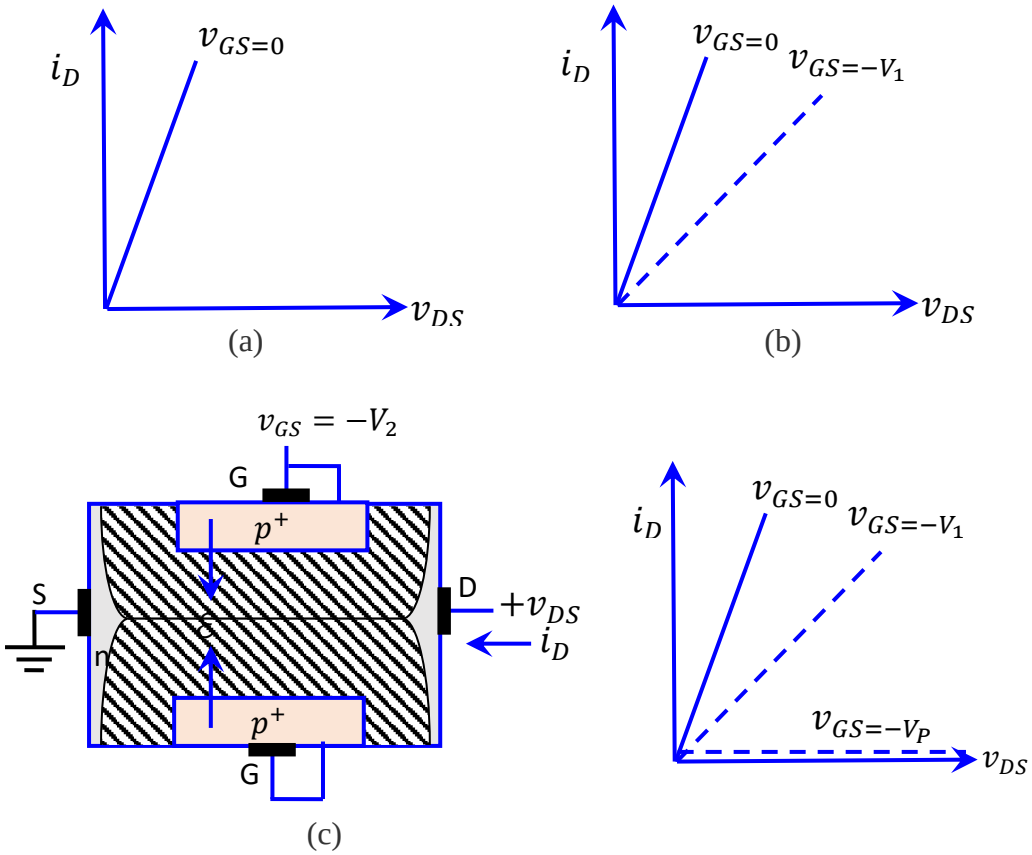


Fig. 4.3 Gate-to-channel space-charge regions and current-voltage characteristics for very small v_{DS} with (a) zero gate voltage, (b) small reverse-biased gate voltage, and (c) a gate voltage that achieves pinch-off.

If a reverse bis voltage ($-V_1$) is applied to the gate of a pn JFET, the channel constriction increases, and the channel conductance changes as in Fig. 4.3 (b). If a further negative gate voltage is applied to the n-channel JFET in Fig. 4.3 (b) and (c), the gate-to-channel pn junction becomes more reverse-biased. The space-charge region widens, the channel region narrows, the resistance of the n-channel increases, and the slope of the i_D versus v_{DS} curve, for small v_{DS}, decreases. These effects are shown in Fig. 4.3 (b) by dotted lines. If a larger negative gate voltage is applied, the condition shown in Fig. 4.3 (c) can be achieved ($-V_p$). The reverse-biased gate-to-channel space-charge region completely fills the channel region. This condition is known as **pinch-off.** Since the depletion region isolates the source and drain terminals, the **drain current** at the physical pinch-off is essentially **zero**. The i_D versus v_{DS} curves are shown by the dotted line in Fig. 4.3 (c). The gate voltage controls the current in the

channel. The control of the current in one part of the device by a voltage in another part of the device is the basic FET transistor action. The pn JFET is a "*normally on," or depletion mode device*; that is, a voltage must be applied to the gate terminal to turn the device OFF.

Consider the situation in which the gate voltage is zero, $v_{GS} = 0$, and the drain voltage change is very small as shown in Fig. 4.4 (a). The channel is maximum open and hence maximum drain current flows [4]. As the reverse bias between gate-to-source is increased ($-V_1$) as in Fig. 4.4 (b), the channel thickness decreases, and the drain current decreases. With increasing reverse bias, a point is reached when the depletion region occupies the complete channel width, and physically no channel exists between the drain and the source and hence no current can flow. This condition is called the **physical pinch-off** and is illustrated in Fig. 4.4 (c). The $V_P = -V_{GS}$ denotes the voltage at which the physical pinch-off occurs.

$$V_{GS} = V_{GS(OFF)}\big|_{I_D=0, V_{DS}=very\ small} \tag{4.1}$$

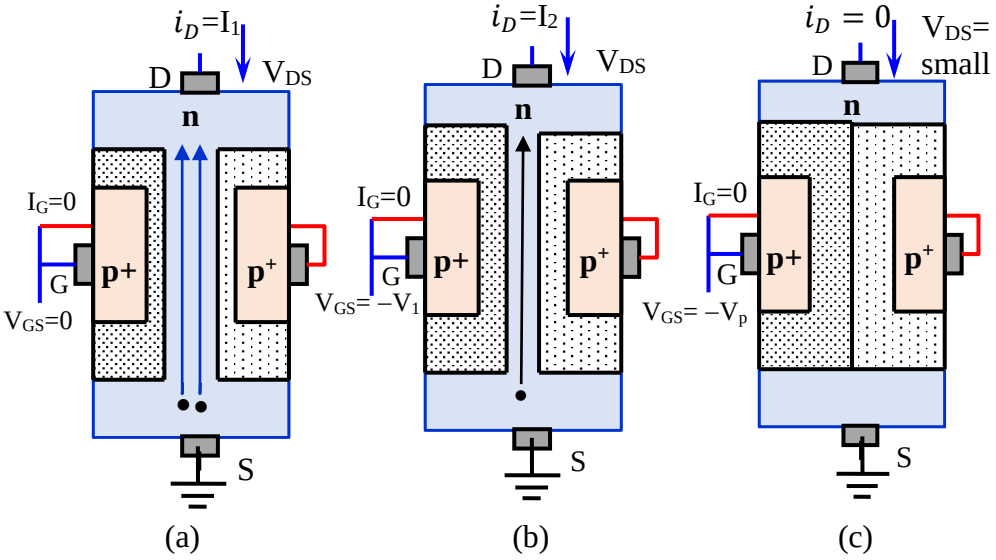


Fig. 4.4 Illustration of physical pinch-off with increasing reverse V_{GS}

When drain to source voltage is very small with $V_{GS} = 0$, the channel is maximum open and i_D versus v_{DS} characteristic is linear as ondicated in Fig. 4.5 (a) [4]. As the drain voltage increases (positive), the gate-to-channel pn junction becomes reverse-biased near the drain terminal, and the space-charge region widens, extending farther into the channel. The channel acts essentially as a variable resistor, and the effective

channel resistance increases as the space-charge region widen; therefore, the slope of the i_D versus v_{DS} characteristic decreases are shown in Fig. 4.5 (b) by dotted lines. The effective channel resistance now varies along the channel length, and, since the channel current must be constant, the voltage drop through the channel becomes dependent on the position.

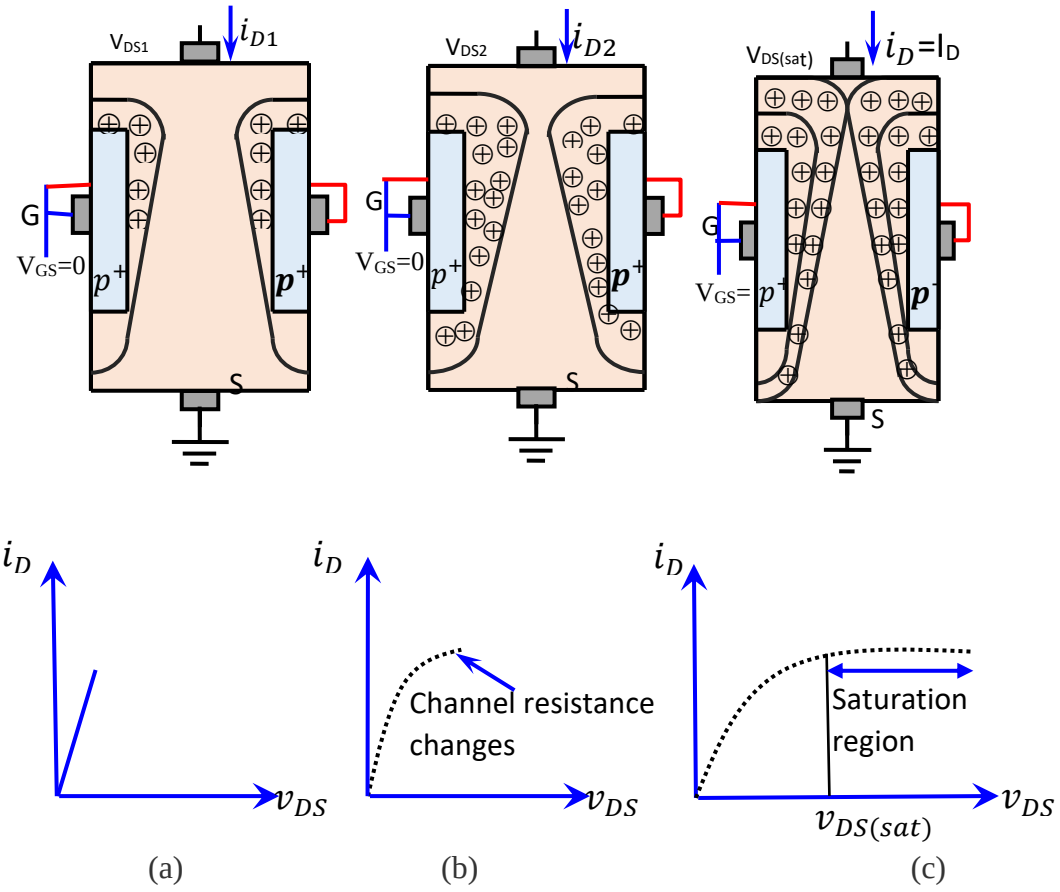


Fig. 4.5 Gate-to-channel space-charge regions and current-voltage characteristics for zero gate voltage with (a) a small drain voltage, (b) a larger drain voltage, and (c) a drain voltage that achieves pinch-off at the drain terminal

If the drain voltage increases further, the condition shown in Fig. 4.5 (c) can result. The channel is *electrically pinched-off* at the drain terminal. Any further increase in drain voltage will not increase the drain current. The i_D-v_{DS} Characteristic for this condition is also shown in the Fig. 4.5 (c). The drain voltage at pinch-off is $v_{DS(sat)}$. Therefore, for $v_{DS} > v_{DS(sat)}$The JFET is biased in the saturation region, and the drain current for this ideal case is independent of v_{DS}.

All books use small-signal equivalent circuit models to analyse and design circuits incorporating FET and MOSFETs. Our approach to the analysis follows a mathematical model of the FET/ MOSFET using its floating admittance matrix. First, we write the expressions of both input and output currents as functions of the voltage of the FET/ MOSFET as in Fig. 4.6.

$$\left.\begin{aligned} I_G &= f_1(V_{GS}) \\ I_D &= f_2(V_{GS}, V_{DS}) \end{aligned}\right\} \tag{4.2}$$

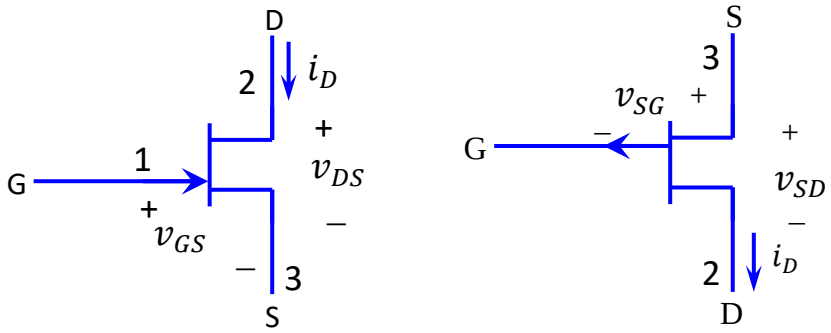


Fig. 4.6 Circuit Symbol Representation of ***three***-terminal FETs

4.2 FET Small-Signal Equivalent Model

The small fluctuation of DC current yields AC current. The small fluctuations in DC current [4] of Eq. (4.2) yield;

$$\Delta I_G = i_g = \frac{\partial I_G}{\partial V_{GS}} \Delta V_{GS} \tag{4.3}$$

$$\frac{\partial I_G}{\partial V_{GS}} = \frac{\Delta I_G}{\Delta V_{GS}} = g_g \tag{4.4}$$

Now, ac gate current as a function of change in the gate to source voltage is expressed as;

$$i_g = \frac{\partial I_G}{\partial V_{GS}} \Delta V_{GS} = g_g v_{gs} \tag{4.5}$$

The total deviation in the drain current due to partial deviation in the gate to source voltage and also partial deviation in the drain to source voltage is expressed as;

$$\Delta I_D = i_d = \frac{\partial I_D}{\partial V_{GS}}\bigg|_{V_{DS}=k} \Delta V_{GS} + \frac{\partial I_D}{\partial V_{DS}}\bigg|_{V_{GS}=k} \Delta V_{DS} \tag{4.6}$$

$$\frac{\partial I_D}{\partial V_{GS}} \cong \frac{\Delta I_D}{\Delta V_{GS}} = g_m \tag{4.7}$$

$$\frac{\partial I_D}{\partial V_{DS}} = \frac{\Delta I_D}{\Delta V_{DS}} = g_d \tag{4.8}$$

Substituting Eqs. (4.7) and (4.8) in Eq. (4.6) yields;

$$i_d = g_m v_{gs} + g_d v_{ds} \tag{4.9}$$

The negligible amount of gate current i_g from Eq. (4.5) that can flow even though the gate-to-source under reverse biased is a function of only the gate-to-source voltage, and hence it can be expressed in the circuit by a conductance g_g across the input terminals, i.e. between the gate to the source.

The drain current from Eq. (4.9) is the sum of two current sources;

- Input voltage-controlled output current source ($g_m v_{gs}$), and
- Output voltage- output current source ($g_d v_{ds}$)

For developing the floating admittance matrix of the FET shown in Fig. 4.7, the small-signal equivalent circuit of FET is drawn as in Fig. 4.7. Thus, the drain current is the algebraic sum of the two current sources, as in Fig. 4.7.

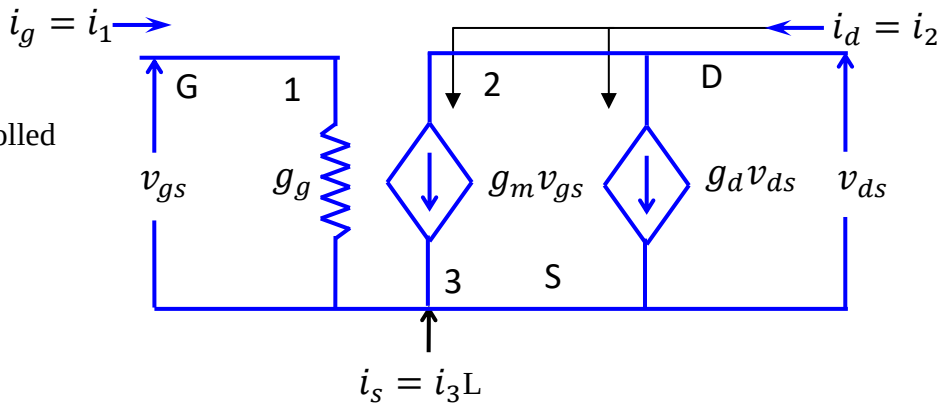


Fig. 4.7 Current Source small-signal model of a 3-terminal FET

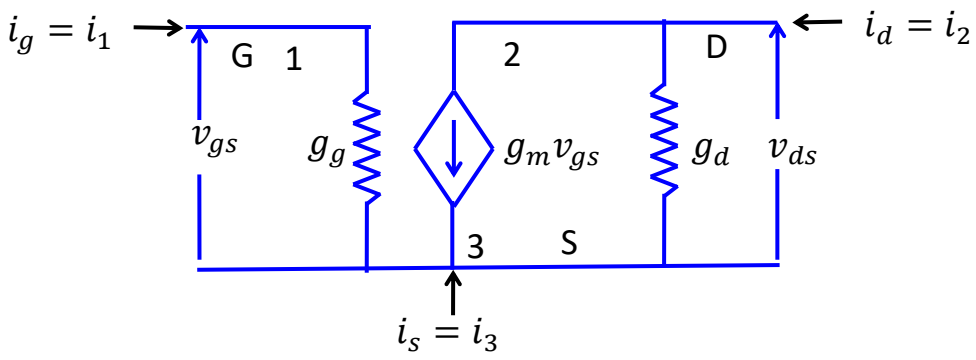


Fig. 4.8 Modified small-signal circuit model of a 3-terminal FET

From Eq. (4.5), a conductance (g_g) is connected between the gate and the source terminals, i.e. across the input terminals. Similarly, from Eq. (4.9), two current sources are connected across the drain and the source terminals as in Fig. 4.7.

Since the current source $g_d v_{ds}$ is across the self-voltage node voltage v_{ds} in Fig. 4.7, it can be reduced in Fig. 4.8 [2-17] by a conductance g_d after dividing the current source $g_d v_{ds}$ by v_{ds} as;

$$\frac{g_d v_{ds}}{v_{ds}} = g_d \tag{4.10}$$

Writing current equations [2-17] at all nodes of Fig. 4.8 yields;

$$i_g = i_1 = g_g(v_g - v_s) = g_g v_1 + (0)v_2 - g_g v_3 \tag{4.11}$$

$$\begin{aligned} i_d = i_2 &= g_d(v_d - v_s) + g_m(v_g - v_s) \\ &= g_m v_1 + g_d v_2 - (g_m + g_d)v_3 \end{aligned} \tag{4.12}$$

$$\begin{aligned} i_s = i_3 &= g_g(v_s - v_g) - g_m(v_g - v_s) + g_d(v_s - v_d) \\ &= -(g_g + g_m)v_1 - g_d v_2 + (g_g + g_m + g_d)v_3 \end{aligned} \tag{4.13}$$

Equations (4.11), (4.12), and (4.13) can be expressed in the form of a matrix [19-26] as;

$$\begin{bmatrix} i_g = i_1 \\ i_d = i_2 \\ i_s = i_3 \end{bmatrix} = \begin{bmatrix} 1 & 2 & 3 \\ g_g & 0 & -g_g \\ g_m & g_d & -g_m - g_d \\ -g_g - g_m & -g_d & g_g + g_m + g_d \end{bmatrix} \begin{bmatrix} v_g = v_1 \\ v_d = v_2 \\ v_s = v_3 \end{bmatrix} \tag{4.14}$$

Since, $r_g \rightarrow$very large, as the gate is always reverse biased, it is approximated to be infinity (∞) and $g_g \rightarrow 0$. Hence, the floating admittance matrix of the FET only can be approximated as;

$$[Y] = \begin{bmatrix} 1 & 2 & 3 \\ \cancel{g_g} & 0 & -\cancel{g_g} \\ g_m & g_d & -g_m - g_d \\ -\cancel{g_g} - g_m & -g_d & \cancel{g_g} + g_m + g_d \end{bmatrix} \cong \begin{bmatrix} 1 & 2 & 3 \\ 0 & 0 & 0 \\ g_m & g_d & -g_m - g_d \\ -g_m & -g_d & g_m + g_d \end{bmatrix} \tag{4.15}$$

Though g_g is negligibly small w.r.t. the g_m and g_d, yet we will carry the same for the analysis of different types of amplifier configurations. Hence, the coefficient matrix from the floating admittance matrix [18-24] of the FET in Eq. (4.14) is written as;

$$[Y_D] = \begin{bmatrix} 1 & 2 & 3 \\ g_g & 0 & -g_g \\ g_m & g_d & -g_m - g_d \\ -g_g - g_m & -g_d & g_g + g_m + g_d \end{bmatrix} \begin{bmatrix} 1 \\ 2 \\ 3 \end{bmatrix} \tag{4.16}$$

Having developed the floating admittance matrix (FAM) model of the FET as an active device in Eq. (4.46), we can use this model in deriving all transfer functions of any amplifier configurations of the FET.

4.3 Circuit Model of FET Common-Source Amplifier

The circuit of a common-source amplifier is shown in Fig. 4.9, where coupling and bypass capacitors have been added along with the signal source and load resistors. These coupling and bypass capacitors do not behave as short circuits at low frequencies. Since, v_s is also used for the voltage at the source terminal of the JFET, the signal voltage will be represented by v_i in the JFET and MOSFET amplifiers.

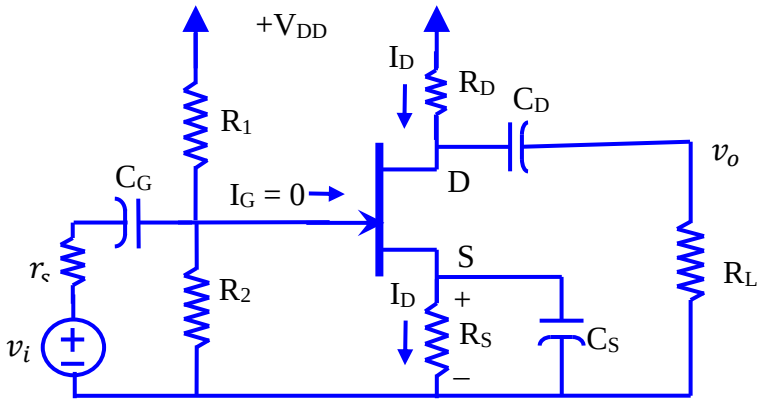


Fig. 4.9 Circuit Model of a Common-Source FET Amplifier

The coupling capacitors C_G and C_D isolate the amplifier dc (V_{DD}) from the signal source and the load. The bypass capacitor provides the low impedance path for the ac signal so that the presence of the source resistor R_S does not reduce the gain of the amplifier. The common-source amplifier (CS) is similar to the common emitter (CE)

amplifier configuration. The common-source amplifier configuration is perhaps the most widely used configuration of the FET amplifier.

For the small-signal analysis of the FET amplifier, the coupling, bypass capacitors, and dc supply V_{DD} are replaced by short circuits. After these replacements, the circuit is called the ac circuit, as shown in Fig. 4.10.

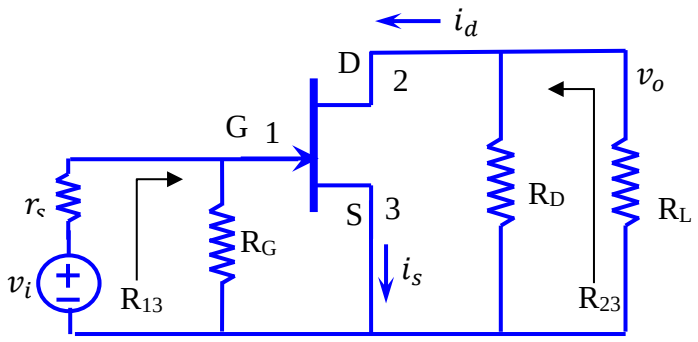


Fig. 4.10 AC Circuit Model of a CS JFET Amplifier

The floating admittance matrix of the JFET only [18-24] used in Fig. 4.10 is rewritten here as;

$$[Y_D] = \begin{bmatrix} 1 & 2 & 2 \\ g_g & 0 & -g_g \\ g_m & g_d & -g_m - g_d \\ -g_g - g_m & -g_d & g_g + g_m + g_d \end{bmatrix} \begin{bmatrix} 1 \\ 2 \\ 3 \end{bmatrix} \tag{4.17}$$

The floating admittance matrix of the passive components used in the CS amplifier in Fig. 4.10 is written as;

$$[Y_{g_s,G_G,G_D,G_L}] = \begin{bmatrix} 1 & 2 & 3 \\ g_s + G_G & 0 & -g_s - G_G \\ 0 & G_D + G_L & -G_D - G_L \\ -g_s - G_G & -G_D - G_L & g_s + G_G + G_D + G_L \end{bmatrix} \begin{bmatrix} 1 \\ 2 \\ 3 \end{bmatrix} \tag{4.18}$$

Now, Eqs (4.17) and (4.18) are merged together as per node specifications to yield the complete floating admittance matrix of the common-source amplifier in Fig. 4.10 as;

$$\begin{bmatrix} 1 & 2 & 3 \\ g_g + g_s + G_G & 0 & -g_g - g_s - G_G \\ g_m & g_d + G_D + G_L & -g_m - g_d - G_D - G_L \\ -g_g - g_m - g_s - G_G & -g_d - G_D - G_L & g_g + g_m + g_d + g_s + G_G + G_D + G_L \end{bmatrix} \begin{bmatrix} 1 \\ 2 \\ 3 \end{bmatrix} \tag{4.19}$$

The voltage gain [18-24] between the output terminals 2 & 3 and the input terminals 1 & 3 of a common-source amplifier in Fig. 4.10 using Eq. (4.19) is expressed as;

$$A_v|_{13}^{23} = sgn(2-3)sgn(1-3)(-1)^9 \frac{|Y_{23}^{13}|}{|Y_{13}^{13}|} = -\frac{|Y_{23}^{13}|}{|Y_{13}^{13}|} \tag{4.20}$$

From Eq. (4.19), $|Y_{13}^{13}| = g_d + G_D + G_L$ and $|Y_{23}^{13}| = g_m$

$$A_v|_{13}^{23} = \frac{v_{23}}{v_{13}} = \frac{v_2}{v_1} = -\frac{g_m}{g_d+G_D+G_L} = -\mathrm{g_m}(\mathrm{r_d} \parallel \mathrm{R_D} \parallel \mathrm{R_L}) \tag{4.21}$$

As $r_d \gg R_D$ & R_L, Eq. (4.21) reduces to

$$A_v|_{13}^{23} = -g_m(R_L) = -g_m(\mathrm{R_D} \parallel \mathrm{R_L}) \tag{4.22}$$

The input resistance [18-24] between the input terminals 1 & 3 of a common-source amplifier in Fig. 4.10 using Eq. (4.18) is expressed as;

$$R_{in} = R_{13} = \frac{|Y_{13}^{13}|}{|Y_3^3|}_{g_s=0} \tag{4.23}$$

From Eq. (4.19), $|Y_{13}^{13}| = g_d + G_D + G_L$

$$|Y_3^3|_{g_s=0} = \begin{vmatrix} g_g + g_s + G_G & 0 \\ g_m & G_D + G_L \end{vmatrix} = (g_g + G_G)(g_d + G_D + G_L)$$

$$R_{in} = R_{13} = \frac{g_d+G_D+G_L}{(g_g+G_G)(g_d+G_D+G_L)} = r_g \parallel R_G \cong R_G \text{ as } R_G \ll r_g \tag{4.24}$$

From Fig. 4.11, $v_{13} = \frac{R_i}{r_s+R_i} v_i = \frac{R_G}{r_s+R_G} v_i = \frac{R_G}{R_G} v_i = v_i$

Since the internal resistance r_s of the input voltage source is very low i.e. $r_s \ll R_G$, above equation simplifies to

$$\frac{v_{13}}{v_i} = 1 \tag{4.25}$$

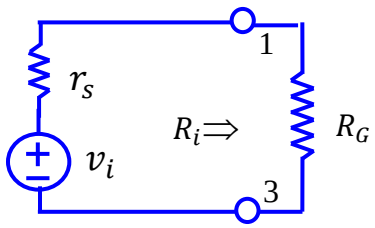


Fig. 4.11 Effective Voltage Gain Model with $R_i = R_{13} = R_G$ for CS Amplifier

$$A_{vs} = \frac{v_{23}}{v_{13}} x \frac{v_{13}}{v_i} = \frac{v_{23}}{v_i} = -g_m(r_d \parallel \mathrm{R_D} \parallel \mathrm{R_L}) \cong -g_m(R_D \parallel R_L) \tag{4.26}$$

The output resistance [18-24] between the output terminals 2 and 3 of a common-source amplifier in Fig. 4.10 using Eq. (4.19) is expressed as;

$$R_o = R_{23} = \frac{|Y_{23}^{23}|}{|Y_3^3|}_{G_L=0} \tag{4.27}$$

From Eq. (4.18), $|Y_{23}^{23}| = g_g + g_s + G_G$

$$|Y_3^3|_{G_L=0} = \begin{vmatrix} g_g + g_s + G_G & 0 \\ g_m & g_d + G_D + \cancel{G_L} \end{vmatrix} = (g_d + G_D)(g_g + g_s + G_G)$$

$$R_o = R_{23} = \frac{g_g+g_s+G_G}{(g_d+G_D)(g_g+g_s+G_G)} = \frac{1}{(g_d+G_D)} = r_d \parallel R_D \tag{4.28}$$

The current gain [18-24] between the output terminals 2 & 3 and the input terminals 1 & 3 of a common-source amplifier in Fig. 4.10 using Eq. (4.19) is expressed as;

$$A_i|_{13}^{23} = sgn(2-3)sgn(1-3)(-1)^9 \frac{|Y_{23}^{13}|}{|Y_3^3|} G_L = -\frac{|Y_{23}^{13}|}{|Y_3^3|} G_L \tag{4.29}$$

From Eq. (4.19), $|Y_{23}^{13}| = g_m$

$$|Y_3^3| = \begin{vmatrix} g_g + g_s + G_G & 0 \\ g_m & g_d + G_D + G_L \end{vmatrix} = (g_d + G_D + G_L)(g_g + g_s + G_G)$$

$$A_i|_{13}^{23} = -\frac{|Y_{23}^{13}|}{|Y_3^3|} G_L = -\frac{g_m G_L}{(g_d+G_D+G_L)(g_g+g_s+\cancel{G_G})} = -\frac{g_m G_L}{G_D+G_L}\left(r_g \parallel r_s \parallel R_G\right)$$

$$= -\frac{g_m R_D}{R_D+R_L} r_s \tag{4.30}$$

The power gain [18-24] between the output terminals 2 & 3 and the input terminals 1 & 3 of the common-source amplifier in Fig. 4.10 is written as;

$$A_P|_{13}^{23} = A_v|_{13}^{23}.A_i|_{13}^{23} = -g_m(R_D \parallel R_L)\left(-\frac{g_m R_D}{R_D+R_L} r_s\right)$$

$$= g_m^2(R_D \parallel \mathrm{R_L})\left(\frac{R_D}{R_D+R_L} r_s\right) \tag{4.31}$$

4.4 Circuit Model of FET Common-Drain Amplifier

The common-drain amplifier is more popularly known as a source follower. It is similar to the emitter follower amplifier circuit as the source terminal follows the voltage at the

gate (input) terminal. The basic circuit of a common-drain amplifier is shown in Fig. 4.12. The ac circuit of the common-drain amplifier is drawn as in Fig. 4.13.

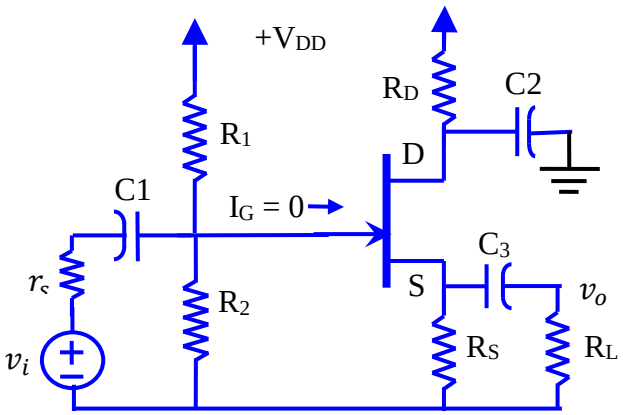


Fig. 4.12 Circuit Model of Source Follower Amplifier

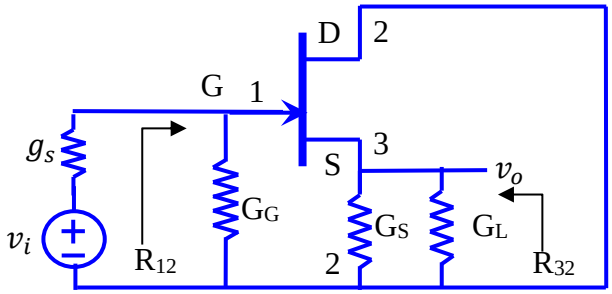


Fig. 4.13 AC circuit Model of a Source Follower Amplifier

The floating admittance matrix of the JFET [18-24] only in Fig. 4.12 is written as;

$$[Y_D] = \begin{bmatrix} 1 & 2 & 3 \\ g_g & 0 & -g_g \\ g_m & g_d & -g_m - g_d \\ -g_g - g_m & -g_d & g_g + g_m + g_d \end{bmatrix} \begin{bmatrix} 1 \\ 2 \\ 3 \end{bmatrix} \tag{4.32}$$

The floating admittance matrix of the passive components in Fig. 4.13 is written as;

$$\left[Y_{g_s,G_G,G_D,G_L}\right] = \begin{bmatrix} 1 & 2 & 3 \\ g_s + G_G & -g_s - G_G & 0 \\ -g_s - G_G & g_s + G_G + G_S + G_L & -G_S - G_L \\ 0 & -G_S - G_L & G_S + G_L \end{bmatrix} \begin{bmatrix} 1 \\ 2 \\ 3 \end{bmatrix} \tag{4.33}$$

Now, Eqs. (4.32) and (4.33) are merged together as per node specifications to yield the overall floating admittance matrix of the common-drain amplifier as;

$$\begin{bmatrix} 1 & 2 & 2 \\ g_g + g_s + G_G & -g_s - G_G & -g_g \\ g_m - g_s - G_G & g_d + g_s + G_G + G_S + G_L & -g_m - g_d - G_S - G_L \\ -g_g - g_m & -g_d - G_S - G_L & g_g + g_m + g_d + G_S + G_L \end{bmatrix} \begin{bmatrix} 1 \\ 2 \\ 3 \end{bmatrix} \tag{4.34}$$

The voltage gain [18-24] between the output terminals 3 & 2 and the input terminals 1 & 2 of the common-drain amplifier in Fig. 4.13 is expressed using Eq. (4.34) as;

$$A_v|_{12}^{32} = sgn(3-2)sgn(1-2)(-1)^8 \frac{|Y_{32}^{12}|}{|Y_{12}^{12}|} = -\frac{|Y_{32}^{12}|}{|Y_{12}^{12}|} \tag{4.35}$$

From Eq. (4.34), $|Y_{32}^{12}| = -\cancel{g_g} - g_m$

$$|Y_{12}^{12}| = \cancel{g_g} + g_m + g_d + G_S + G_L$$

$$A_v|_{12}^{32} = \frac{v_{32}}{v_{12}} = -\frac{-g_m}{g_m + \cancel{g_d} + G_S + G_L} = -\frac{-g_m}{g_m + G_S + G_L} = g_m\left(\frac{1}{g_m} \parallel R_S \parallel R_L\right)$$

$$= g_m(R_S \parallel R_L) \tag{4.36}$$

The input resistance [18-24] between the input terminals 1 & 2 of a common-drain amplifier in Fig. 4.13 using Eq. (4.34) is expressed as;

$$R_{in} = R_{12} = \frac{|Y_{12}^{12}|}{|Y_3^3|}_{g_s=0} \tag{4.37}$$

From Eq. (4.34), $|Y_{12}^{12}| = g_g + g_m + g_d + G_S + G_L$

$$|Y_2^2|_{g_s=0} = \begin{vmatrix} g_g + \cancel{g_s} + G_G & 0 \\ -g_m & g_g + g_d + g_m + G_S + G_L \end{vmatrix}$$

$$= (g_g + g_d + g_m + G_S + G_L)(g_g + G_G)$$

$$R_{in} = R_{12} = \frac{g_g + g_m + g_d + G_S + G_L}{(g_g + g_d + g_m + G_S + G_L)(g_g + G_G)} = r_g \parallel R_G \cong R_G \tag{4.38}$$

The overall voltage gain [18-24] including voltage source resistance r_s can be obtained using Fig. 4.14.

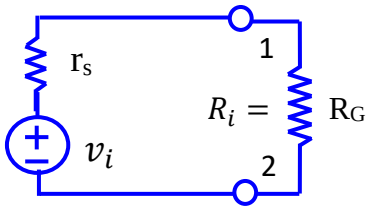


Fig. 4.14 *Effective* Voltage Gain Model with $R_i = R_{12} = R_G$ for CD Amp

$$v_{12} = \frac{R_i}{r_s+R_i} v_i = \frac{R_G}{r_s+R_G} v_i \cong v_i$$

$$\frac{v_{12}}{v_i} = 1$$

$$A_{vs} = \frac{v_{32}}{v_{12}} x \frac{v_{12}}{v_i} = \frac{v_{32}}{v_i} = g_m(\mathrm{R_S} \parallel \mathrm{R_L}) \tag{4.39}$$

The output resistance [18-24] between the output terminals 3 & 2 of a common-drain amplifier in Fig. 4.13 using Eq. (4.34) is expressed as;

$$R_o = R_{32} = \frac{|Y_{32}^{32}|}{|Y_3^3|}_{G_L=0} \tag{4.40}$$

From Eq. (4.34), $|Y_{32}^{32}| = \cancel{g_g} + g_s + G_G$

$$|Y_2^2|_{G_L=0} = \begin{vmatrix} \cancel{g_g} + g_s + G_G & -\cancel{g_g} \\ -\cancel{g_g} - g_m & \cancel{g_g} + g_m + g_d + G_S + \cancel{G_L} \end{vmatrix}$$

$$= (g_m + g_d + G_S)(g_s + G_G) \quad = (g_m + \cancel{g_d} + G_S)(g_s + G_G)$$

$$= (g_m + G_S)(g_s + G_G)$$

$$|Y_2^2|_{G_L=0} = (g_m + G_S)(g_s + G_G)$$

$$R_o = R_{23} = \frac{g_s+G_G}{(g_m+G_S)(g_s+G_G)} = \frac{1}{(g_m+G_S)} = \frac{1}{g_m} \parallel R_S \cong \frac{1}{g_m} \tag{4.41}$$

A Common-source amplifier's output resistance is extremely low.

The current gain [18-24] between the output terminals 3 & 2 and the input terminals 1 & 2 of a common-drain amplifier in Fig. 4.13 using Eq. (4.34) is expressed as;

$$A_i|_{12}^{32} = sgn(3-2)sgn(1-2)(-1)^8 \frac{|Y_{32}^{12}|}{|Y_2^2|} G_L = -\frac{|Y_{32}^{12}|}{|Y_2^2|} G_L \tag{4.42}$$

From Eq. (4.34), $|Y_{32}^{12}| = -\cancel{g_g} - g_m$

$$|Y_2^2| = \begin{vmatrix} \cancel{g_g} + g_s + \cancel{G_G} & 0 \\ -\cancel{g_g} - g_m & \cancel{g_g} + g_m + g_d + G_S + G_L \end{vmatrix}$$

$$= (g_m + g_d + G_S + G_L)g_s$$

$$A_i|_{12}^{32} = -\frac{-g_m}{(g_m+g_d+G_S+G_L)g_s}G_L = \frac{g_m r_s}{g_m+g_d+G_S+G_L}G_L = \frac{g_m r_s}{g_m+G_S+G_L}G_L$$

$$= \frac{g_m R_S r_s}{\{1+g_m(R_S \| R_L)\}(R_S+R_L)} \quad (4.43)$$

The power gain [18-24] between the output terminals 3 & 2 and the input terminals 1 & 2 of a common-drain amplifier in Fig. 4.13 is written as;

$$A_P|_{12}^{32} = A_v|_{12}^{32}.A_i|_{12}^{32} = \{g_m(R_S \parallel R_L)\}\frac{g_m r_S R_S}{\{1+g_m(R_S \| R_L)\}(R_S+R_L)} \quad (4.44)$$

Equation (4.44) indicates that the power of a common-drain amplifier is very low.

4.5 Circuit Model of FET Common-Gate Amplifier

The simple circuit of a common-gate amplifier circuit is shown in Fig. 4.15. This configuration is used to match low input resistance to high output resistance. Its ac circuit is drawn in Fig. 4.16.

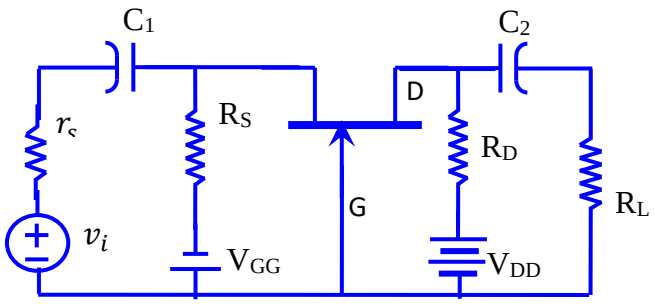


Fig. 4.15 Common-Gate Circuit Model of a FET Amplifier

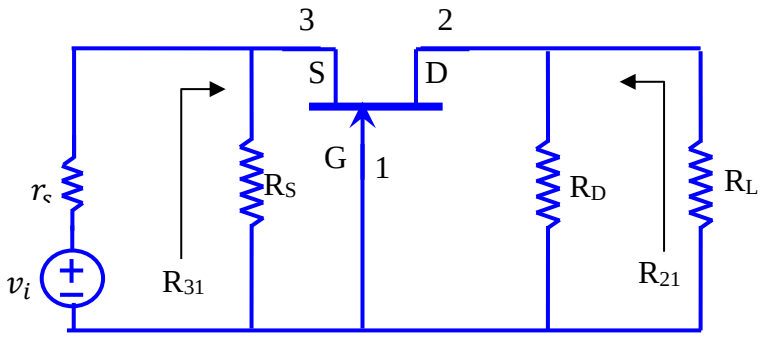


Fig. 4.16 AC circuit model of a FET CG Amplifier

The floating admittance matrix of only the JFET in Fig. 4.16 is once again repeated for ease in the further analysis as;

$$[Y_D] = \begin{bmatrix} 1 & 2 & 3 \\ g_g & 0 & -g_g \\ g_m & g_d & -g_m - g_d \\ g_g + g_m & -g_d & g_g + g_m + g_d \end{bmatrix} \begin{bmatrix} 1 \\ 2 \\ 3 \end{bmatrix} \tag{4.45}$$

The floating admittance matrix [18-24] of the passive circuits used in the amplifier of Fig. 4.14 is once again repeated for ease in the further analysis as;

$$[Y_{g_s,G_S,G_D,G_L}] = \begin{bmatrix} 1 & 2 & 3 \\ g_s + G_S + G_D + G_L & -G_D - G_L & -g_s - G_S \\ -G_D - G_L & G_D + G_L & 0 \\ -g_s - G_S & 0 & g_s + G_S \end{bmatrix} \begin{bmatrix} 1 \\ 2 \\ 3 \end{bmatrix} \tag{4.46}$$

Now, Eqs. (4.45) and (4.46) are merged together to form the overall floating admittance matrix of the common-gate amplifier in Fig. 4.16 as;

$$\begin{bmatrix} 1 & 2 & 3 \\ \cancel{g_g} + g_s + G_S + G_D + G_L & -G_D - G_L & -\cancel{g_g} - g_s - G_S \\ g_m - G_D - G_L & g_d + G_D + G_L & -g_m - g_d \\ -\cancel{g_g} - g_m - g_s - G_S & -g_d & \cancel{g_g} + g_m + g_d + g_s + G_S \end{bmatrix} \begin{bmatrix} 1 \\ 2 \\ 3 \end{bmatrix} \tag{4.47}$$

Assuming $g_g = 1/g_g$ very small, Eq. (4.47) reduces as;

$$\begin{bmatrix} 1 & 2 & 3 \\ g_s + G_S + G_D + G_L & -G_D - G_L & -g_s - G_S \\ g_m - G_D - G_L & g_d + G_D + G_L & -g_m - g_d \\ -g_m - g_s - G_S & -g_d & g_m + g_d + g_s + G_S \end{bmatrix} \begin{bmatrix} 1 \\ 2 \\ 3 \end{bmatrix} \tag{4.48}$$

The voltage gain [18-24] between the output terminals 2 & 1 and the input terminals 3 & 1 of a common-gate amplifier in Fig. 4.16 using Eq. (4.48) is expressed as;

$$A_v|_{31}^{21} = sgn(2-1)sgn(3-1)(-1)^7 \frac{|Y_{21}^{31}|}{|Y_{31}^{31}|} = -\frac{|Y_{21}^{31}|}{|Y_{31}^{31}|} \tag{4.49}$$

From Eq. (4.48), $|Y_{21}^{31}| = -g_m - g_d$

$|Y_{31}^{31}| = g_d + G_D + G_L$

$$A_v|_{31}^{21} = -\frac{|Y_{21}^{31}|}{|Y_{31}^{31}|} = \frac{v_{21}}{v_{31}} = -\frac{-g_m - g_d}{g_d + G_D + G_L} = \frac{g_m}{G_D + G_L} = g_m(R_D \parallel R_L) \tag{4.50}$$

The input resistance [18-24] between the input terminals 3 & 1 of a common-gate amplifier in Fig. 4.16 using Eq. (4.48) is expressed as;

$$R_{in} = R_{31} = \frac{|Y_{31}^{31}|}{|Y_1^1|}_{g_s=0} \tag{4.51}$$

From Eq. (4.48), $|Y_1^1|_{g_s=0} = \begin{vmatrix} g_d + G_D + G_L & -g_m - g_d \\ -g_d & g_m + g_d + \cancel{g_s} + G_S \end{vmatrix}$

$$= \begin{vmatrix} g_d + G_D + G_L & -g_m - g_d \\ -g_d & g_m + g_d + G_S \end{vmatrix} = \begin{vmatrix} G_D + G_L & G_S \\ -\cancel{g_d} & g_m + \cancel{g_d} + G_S \end{vmatrix}$$

$$= \begin{vmatrix} G_D + G_L & G_S \\ 0 & g_m + g_d + G_S \end{vmatrix} = (G_D + G_L)(g_m + G_S)$$

$$R_{in} = R_{31} = \frac{\cancel{g_d} + G_D + G_L}{(G_D + G_L)(g_m + G_S)} = \frac{G_D + G_L}{(G_D + G_L)(g_m + G_S)} = \frac{1}{g_m + G_S} = \frac{1}{g_m} \parallel R_S$$

$$\cong \frac{1}{g_m} \tag{4.52}$$

Equation (4.52) indicates that the output resistance of a common-gate amplifier is very low.

The overall voltage gain, including voltage source resistance r_s can be obtained from Fig. 4.17.

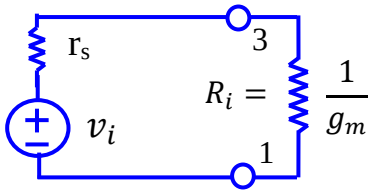


Fig. 4.17 Effective Voltage Gain Model with $R_i = R_{31} = \frac{1}{g_m}$ for CG Amp

From Fig. 4.17, $v_{31} = \frac{R_i}{r_s + R_i} v_i = \frac{\frac{1}{g_m}}{r_s + \frac{1}{g_m}} v_i = v_i$

$$\frac{v_{31}}{v_i} = 1$$

$$A_{vs} = \frac{v_{21}}{v_{31}} x \frac{v_{31}}{v_i} = \frac{v_{21}}{v_i} = g_m(R_D \parallel R_L) \tag{4.53}$$

The output resistance [18-24] between the output terminals 2 & 1 of a common-gate amplifier in Fig. 4.16 using Eq. (4.48) is expressed as;

$$R_o = R_{21} = \frac{|Y_{21}^{21}|}{|Y_1^1|}_{G_L=0} \tag{4.54}$$

From Eq. (4.48), $|Y_1^1|_{G_L=0} = \begin{vmatrix} g_d + G_D + \cancel{G_L} & -g_m - g_d \\ -g_d & g_m + g_d + g_s + G_S \end{vmatrix}$

$= \begin{vmatrix} g_d + G_D & -g_m - g_d \\ G_D & g_s + G_S \end{vmatrix} = \begin{vmatrix} g_d + G_D & -g_m - g_d \\ G_D & g_s + G_S \end{vmatrix}$

$= (G_S + g_s)(g_d + G_D) + G_D(g_m + g_d)$

$|Y_{21}^{21}| = g_m + g_d + g_s + G_S$

$R_o = R_{21} = \frac{g_m+g_d+g_s+G_S}{(G_S+g_s)(g_d+G_D)+G_D(g_m+g_d)} = \frac{g_m+g_s+G_S}{(G_S+g_s)G_D+g_mG_D}$

$= \frac{g_m+g_s+G_S}{\{G_S+g_s+g_m\}G_D} = R_D$ (4.55)

Since the internal resistance of a voltage source is r_s is very small w.r.t. r_d and hence

$R_o = R_{21} = r_d \parallel R_D = R_D$ (4.56)

The current gain [18-24] between the output terminals 2 & 1 and the input terminals 3 & 1 of a common-gate amplifier in Fig. 4.16 using Eq. (4.48) is expressed as;

$A_i|_{31}^{21} = sgn(2-1)sgn(3-1)(-1)^7 \frac{|Y_{21}^{31}|}{|Y_1^1|} G_L = -\frac{|Y_{21}^{31}|}{|Y_1^1|} G_L$ (4.57)

From Eq. (4.48), $|Y_1^1| = \begin{vmatrix} g_d + G_D + G_L & -g_m - g_d \\ -g_d & g_m + g_d + g_s \end{vmatrix}$

$= \begin{vmatrix} G_D + G_L & g_s \\ -g_d & g_m + g_d + g_s \end{vmatrix}$

$= (g_m + \cancel{g_d} + g_s)(G_D + G_L) + \cancel{g_d} g_s = (g_m + g_s)(G_D + G_L)$

$A_i|_{31}^{21} = -\frac{|Y_{21}^{31}|}{|Y_1^1|} G_L = -\frac{-g_m-g_d}{(g_m+g_s)(G_D+G_L)} G_L = \frac{G_L}{(G_D+G_L)} = \frac{R_D}{(R_D+R_L)}$ (4.58)

The power gain [18-24] between the output terminals 2 & 1 and the input terminals 3 & 1 of a common-gate amplifier in Fig. 4.16 is written as;

$A_p\Big|_{31}^{21} = A_v|_{31}^{21}.A_i|_{31}^{21} = g_m(R_D \parallel R_L)\left\{\frac{R_D}{R_D+R_L}\right\}$ (4.59)

The power of the Common-gate amplifier is also very low.

4.6 Circuit Model of FET Phase-splitter amplifier (complete analysis)

A versatile circuit of FET amplifier with resistances connected to all the three terminals (drain, gate, and source) is drawn in Fig. 4.18. The drain resistance R_D, the source

resistance R_S and the gate resistance R_G are connected in Fig. 4.18. We will try to derive all types of transfer functions of the FET amplifiers in all the three configurations, i.e. common-source, common-drain, and common-gate. Fig. 4.19 is the ac circuit derived from Fig. 4.16 after shorting all capacitances C_G and C_D and the DC supply voltages at the frequency of interest. The bypass capacitor C_S is left open to implement this circuit as a FET phase-splitter amplifier. Fig. 4.19 is called a phase-splitter amplifier because the phase of the voltage at terminal-2 is 180^0 out of phase to the voltage at terminal-3.

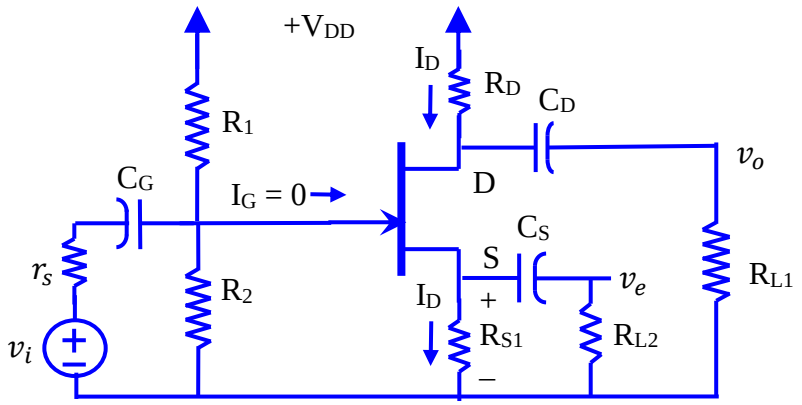


Fig. 4.18 Circuit Model of a FET Phase-Splitter Amplifier

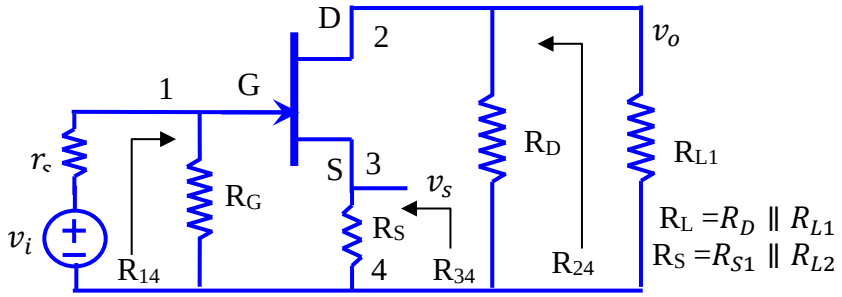


Fig. 4.19 AC Circuit Model of a FET Phase-Splitter Amplifier

Since the phase-splitter amplifier is defined by 4-nodes, the floating admittance matrix [18-24] of the three-node JFET is converted to 4-nodes as;

$$\begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \end{bmatrix} = \begin{bmatrix} \begin{matrix}1\\ g_g\end{matrix} & \begin{matrix}2\\ 0\end{matrix} & \begin{matrix}3\\ -g_g\end{matrix} & \begin{matrix}4\\ 0\end{matrix} \\ g_m & g_d & -g_m - g_d & 0 \\ -g_g - g_m & -g_d & g_g + g_m + g_d & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \end{bmatrix} \tag{4.60}$$

Similarly, the floating admittance matrix of only passive components used in the circuit of the phase-splitter amplifier of Fig. 4.19 is written as;

$$\begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \end{bmatrix} \begin{bmatrix} \begin{matrix}1\\ g_s + G_G\end{matrix} & \begin{matrix}2\\ 0\end{matrix} & \begin{matrix}3\\ 0\end{matrix} & \begin{matrix}4\\ -g_s - G_G\end{matrix} \\ 0 & G_L & 0 & -G_L \\ 0 & 0 & G_S & -G_S \\ -g_s - G_G & -G_L & -G_S & g_s + G_G + G_S + G_L \end{bmatrix} \begin{bmatrix} 1 \\ 2 \\ 3 \\ 4 \end{bmatrix} \tag{4.61}$$

Now, Eqs. (4.60) and (4.61) are merged together as per node specification to form the overall floating admittance matrix of Fig. 4.19 as;

$$\begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \end{bmatrix} \begin{bmatrix} \begin{matrix}1\\ g_g + g_s + G_G\end{matrix} & \begin{matrix}2\\ 0\end{matrix} & \begin{matrix}3\\ -g_g\end{matrix} & \begin{matrix}4\\ -g_s - G_G\end{matrix} \\ g_m & g_d + G_L & -g_m - g_d & -G_L \\ -g_g - g_m & -g_d & g_g + g_m + g_d + G_S & -G_S \\ -g_s - G_G & -G_L & -G_S & g_s + G_G + G_S + G_L \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \end{bmatrix} \tag{4.62}$$

The voltage gain [18-24] between the output terminals 2 & 4 and the input terminals 1 & 4 of a FET phase-splitter circuit in Fig. 4.19 using Eq. (4.62) is expressed as;

$$A_v|_{14}^{24} = sgn(2-4)sgn(1-4)(-1)^{11}\frac{|Y_{24}^{14}|}{|Y_{14}^{14}|} = -\frac{|Y_{24}^{14}|}{|Y_{14}^{14}|} \tag{4.63}$$

From Eq. (4.62), $|Y_{24}^{14}| = \begin{vmatrix} g_m & -g_m - g_d \\ -g_g - g_m & g_g + g_m + g_d + G_S \end{vmatrix} = \begin{vmatrix} g_m & -g_m - g_d \\ -g_g & g_g + G_S \end{vmatrix}$

$$= g_m G_S$$

$$|Y_{14}^{14}| = \begin{vmatrix} g_d + G_L & -g_m - g_d \\ -g_d & \cancel{g_d} + g_m + g_d + G_S \end{vmatrix} = \begin{vmatrix} g_d + G_L & -g_m - g_d \\ G_L & G_S \end{vmatrix}$$

$$= (g_d + G_L)G_S + (g_m + g_d)G_L$$

$$A_v|_{14}^{24} = -\frac{g_m G_S}{(\cancel{g_d}+G_L)G_S+(g_m+\cancel{g_d})G_L} = -\frac{g_m G_S}{(G_S+g_m)G_L} = -\frac{g_m G_S}{G_S G_L} \cong -g_m R_L \qquad (4.64)$$

The current gain [18-24] between the output terminals 2 & 4 and the input terminals 1 & 4 of a FET phase-splitter circuit in Fig. 4.19 using Eq. (4.62) is expressed as;

$$A_i|_{14}^{24} = sgn(2-4)sgn(1-4)(-1)^{11}\frac{|Y_{24}^{14}|}{|Y_4^4|}G_L = -\frac{|Y_{24}^{14}|}{|Y_4^4|}G_L \qquad (4.65)$$

From Eq. (4.62), $|Y_4^4| = \begin{vmatrix} \cancel{g_g} + g_s + G_G & 0 & -\cancel{g_g} \\ g_m & g_d + G_L & -g_m - g_d \\ -\cancel{g_g} - g_m & -g_d & \cancel{g_g} + g_m + g_d + G_S \end{vmatrix}$

$$= \begin{vmatrix} g_s + G_G & 0 & 0 \\ g_m & g_d + G_L & -g_m - g_d \\ -g_m & -g_d & g_m + g_d + G_S \end{vmatrix}$$

$$= (g_s + G_G)\begin{vmatrix} g_d + G_L & -g_m - g_d \\ -g_d & g_m + g_d + G_S \end{vmatrix}$$

$$= (g_s + G_G)\begin{vmatrix} g_d + G_L & -g_m - g_d \\ G_L & G_S \end{vmatrix}$$

$$= (g_s + G_G)\{(g_d + G_L)G_S + G_L(g_m + g_d)\}$$

$$A_i|_{14}^{24} = -\frac{|Y_{24}^{14}|}{|Y_4^4|}G_L = -\frac{g_m G_S G_L}{=(g_s+G_G)\{(\cancel{g_d}+G_L)G_S+G_L(g_m+\cancel{g_d})\}}$$

$$= -\frac{g_m G_S G_L}{(g_s+G_G)G_L\{G_S+g_m\}} = -\frac{g_m r_s}{1+g_m R_S} \cong -g_m r_s \qquad (4.66)$$

The input resistance [18-24] between the input terminals 1 & 4 of a FET phase-splitter circuit in Fig. 4.19 using Eq. (4.62) is expressed as;

$$R_i = R_{14} = \frac{|Y_{14}^{14}|}{|Y_4^4|}_{g_s=0} \qquad (4.67)$$

From Eq. (4.61), $|Y_4^4|_{g_s=0} = \begin{vmatrix} \cancel{g_g} + \cancel{g_s} + G_G & 0 & -\cancel{g_g} \\ g_m & g_d + G_L & -g_m - g_d \\ -\cancel{g_g} - g_m & -g_d & \cancel{g_g} + g_m + g_d + G_S \end{vmatrix}$

$$= \begin{vmatrix} G_G & 0 & 0 \\ g_m & g_d + G_L & -g_m - g_d \\ -g_m & -g_d & g_m + g_d + G_S \end{vmatrix} = G_G \begin{vmatrix} g_d + G_L & -g_m - g_d \\ G_L & G_S \end{vmatrix}$$

$$= G_G\{(g_d + G_L)G_S + G_L(g_m + g_d)\}$$

$$R_i = R_{14} = \frac{(g_d+G_L)G_S+(g_m+g_d)G_L}{G_G\{(g_d+G_L)G_S+(g_m+g_d)G_L\}} = R_G \tag{4.68}$$

The output resistance [18-24] between the output terminals 2 & 4 of a FET phase-splitter circuit in Fig. 4.19 using Eq. (4.62) is expressed as;

$$R_{o2} = R_{24} = \frac{|Y_{24}^{24}|}{|Y_4^4|_{G_L=0}} \tag{4.69}$$

From Eq. (4.62), $|Y_{24}^{24}| = \begin{vmatrix} \cancel{g_g} + g_s + G_G & -\cancel{g_g} \\ -\cancel{g_g} - g_m & \cancel{g_g} + g_m + g_d + G_S \end{vmatrix}$

$$= \begin{vmatrix} g_s + G_G & 0 \\ -g_m & g_m + g_d + G_S \end{vmatrix} = (g_s + G_G)(g_m + g_d + G_S)$$

$$|Y_4^4|_{G_L=0} = \begin{vmatrix} \cancel{g_g} + g_s + G_G & 0 & -\cancel{g_g} \\ g_m & g_d + \cancel{G_L} & -g_m - g_d \\ -\cancel{g_g} - g_m & -g_d & \cancel{g_g} + g_m + g_d + G_S \end{vmatrix}$$

$$= \begin{vmatrix} g_s + G_G & 0 & 0 \\ g_m & g_d & -g_m - g_d \\ -g_m & -g_d & g_m + g_d + G_S \end{vmatrix}$$

$$= (g_s + G_G) \begin{vmatrix} g_d & -g_m - g_d \\ -g_d & g_m + g_d + G_S \end{vmatrix} = (g_s + G_G) \begin{vmatrix} g_d & -g_m - g_d \\ 0 & G_S \end{vmatrix}$$

$$= (g_s + G_G) g_d G_S$$

$$R_o = R_{24} = \frac{(g_s+G_G)(g_m+g_d+G_S)}{(g_s+G_G)g_dG_S} = \frac{(g_m+G_S)}{g_dG_S} = r_d(1+g_mR_S) \tag{4.70}$$

The voltage gain [18-24] between terminals 3 & 4 and 1 & 4 of a FET phase-splitter circuit in Fig. 4.19 using Eq. (4.62) is expressed as;

$$A_v|_{14}^{34} = sgn(3-4)sgn(1-4)(-1)^{12}\frac{|Y_{34}^{14}|}{|Y_{14}^{14}|} = \frac{|Y_{34}^{14}|}{|Y_{14}^{14}|} \tag{4.71}$$

From Eq. (4.62), $|Y_{34}^{14}| = \begin{vmatrix} g_m & g_d+G_L \\ -\cancel{g_g} - g_m & -g_d \end{vmatrix} = \begin{vmatrix} g_m & g_d+G_L \\ -g_m & -g_d \end{vmatrix}$

$$= \begin{vmatrix} 0 & G_L \\ -g_m & -g_d \end{vmatrix} = g_mG_L$$

$$A_v|_{14}^{34} = \frac{g_mG_L}{(\cancel{g_d}+G_L)G_S+(g_m+\cancel{g_d})G_L} = \frac{g_mG_L}{(G_S+g_m)G_L} = \frac{g_mR_S}{(1+g_mR_S)} \cong 1 \tag{4.72}$$

The output resistance [18-24] between its terminals 3 & 4 of a FET phase-splitter circuit in Fig. 4.19 using Eq. (4.62) is expressed as;

$$R_{o3} = R_{34} = \frac{|Y_{34}^{34}|}{|Y_4^4|}_{G_S=0} \tag{4.73}$$

From Eq. (4.62), $|Y_{34}^{34}| = \begin{vmatrix} \cancel{g_g} + g_s + G_G & 0 \\ g_m & g_d+G_L \end{vmatrix} = (g_s+G_G)(g_d+G_L)$

$$|Y_4^4|_{G_S=0} = \begin{vmatrix} \cancel{g_g} + g_s + G_G & 0 & -\cancel{g_g} \\ g_m & g_d+G_L & -g_m-g_d \\ -\cancel{g_g} - g_m & -g_d & \cancel{g_g}+g_m+g_d+\cancel{G_S} \end{vmatrix}$$

$$= \begin{vmatrix} g_s+G_G & 0 & 0 \\ g_m & g_d+G_L & -g_m-g_d \\ -g_m & -g_d & g_m+g_d \end{vmatrix}$$

$$= (g_s+G_G)\begin{vmatrix} g_d+G_L & -g_m-g_d \\ -g_d & g_m+g_d \end{vmatrix}$$

$$= (g_s+G_G)\begin{vmatrix} g_d+G_L & -g_m-g_d \\ G_L & 0 \end{vmatrix} = (g_s+G_G)(g_m+g_d)G_L$$

$$R_{o3} = R_{34} = \frac{(g_s+G_G)(g_d+G_L)}{(g_s+G_G)(g_m+g_d)G_L} = \frac{(\cancel{g_d}+G_L)}{(g_m+\cancel{g_d})G_L} = \frac{G_L}{g_mG_L} = \frac{1}{g_m} \text{ (Very low)} \tag{4.74}$$

The current gain [18-24] between terminals 3 & 4 and 1 & 4 of a FET phase-splitter circuit in Fig. 4.19 using Eq. (4.62) is expressed as;

$$A_i|_{14}^{34} = sgn(3-4)sgn(1-4)(-1)^{12}\frac{|Y_{34}^{14}|}{|Y_4^4|}G_S = \frac{|Y_{34}^{14}|}{|Y_4^4|}G_S \tag{4.75}$$

From Eq. (4.62), $|Y_{34}^{14}| = \begin{vmatrix} g_m & g_d+G_L \\ -g_g-g_m & -g_d \end{vmatrix} = \begin{vmatrix} 0 & G_L \\ -g_m & -g_d \end{vmatrix} = g_m G_L$

$$A_i|_{14}^{34} = \frac{|Y_{34}^{14}|}{|Y_4^4|}G_S = \frac{g_m G_L}{(g_s+G_G)(g_m+g_d)G_L}G_S = \frac{g_m G_L}{(g_s+G_G)g_m G_L}G_S = \frac{G_S}{g_s}$$

$$= \frac{r_S}{R_S} \tag{4.76}$$

The power gain [18-24] between the output terminals 2 & 4 and the input terminals 1 & 4 of a FET phase splitter circuit in Fig. 4.19 using Eq. (4.62) can be expressed as;

$$A_P|_{14}^{24} = A_v|_{14}^{24}.A_i|_{14}^{24} = (-g_m R_L)(-g_m r_s) = g_m^2 r_s R_L \tag{4.77}$$

Power gain [18-24] between the output terminals 3 & 4 and the input terminals 1 & 4 of a FET phase splitter circuit in Fig. 4. 19 using Eq. (4.62) can be written as;

$$A_P|_{14}^{34} = A_v|_{14}^{34}.A_i|_{14}^{34} = \left(\frac{g_m R_S}{(1+g_m R_S)}\right)\left(\frac{r_S}{R_S}\right) = \frac{g_m r_S}{(1+g_m R_S)} \tag{4.78}$$

4.7 Conclusions

The analysis of all configurations FET amplifier to derive all types of transfer functions and self-node functions becomes very simple using the floating admittance matrix approach. All equations derived here corroborate the equations derived using the small-signal equivalent circuits.

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Chapter 5

Four Terminal MOSFET Model and Applications in Amplifiers

5.1 Introduction

In general, the MOS structures are of two-terminal, three-terminal, and four terminal devices. The two-terminal MOS structure has a gate and the substrate terminal only. It does not have the source and drain terminals for the current flow. This structure is often referred to as a MOS *capacitor*. The three terminal MOS structures are similar to the three terminal BJT. The four terminal MOS structure has two gates; the front gate and the back gate. The back gate is nothing but the substrate (body) terminal. The back gate is usually connected to the source terminal and hence it is treated as three terminal devices for general purposes. An IC has numerous numbers of MOSFETs. If the sources of all MOSFETs are connected to the single body (substrate) terminal, the circuit will become useless. Fig. 5.1 has four terminals as V_B (Body), V_S (Source), V_G (Gate), and V_D (Drain). The body and the source terminal are connected to ground and hence it becomes effectively a three-terminal device. Thus, a general purpose MOSFET is basically a three terminal device having the *gate*, the *drain*, and the *source*. The body, in different style, of the MOSFET is the silicon substrate over which drain, gate and source are grown [1-22] as in Fig. 5.1.

No problem exists in the normal functioning of the MOSFET if voltages V_{GS} and V_{DS} are applied with the *body grounded*. If the body is not grounded and V_{GS} is applied, the potential difference exists between source and the body terminals, and the problem will occur. The body is always reverse biased, and the gate is also reverse biased. The body now starts functioning similar to the function of the gate. So, the *body terminal* is called the *second gate terminal* of the MOSFET.

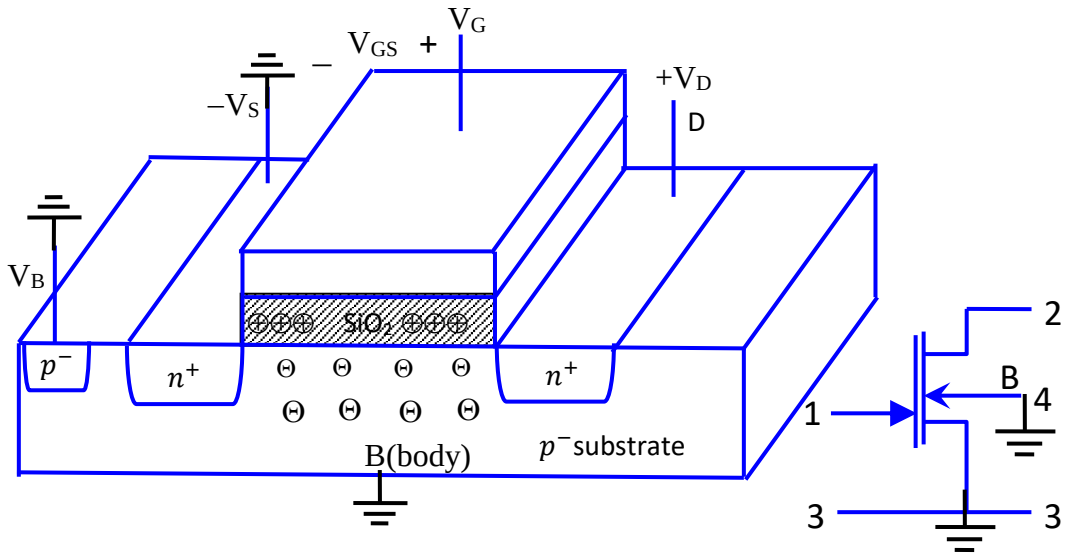

Fig. 5.1 Physical Structural Model of The nMOSFET

Normally, the *body* is kept at the *source potential*. If there exists any potential difference between the source and the body points, the normal functioning of the MOSFET is impaired. The body connection is taken as the 4th terminal of the MOSFET. Body bias is the voltage at which the body terminal (4th terminal of MOS) is connected. Body effect occurs when the body or substrate of the MOSFET is not biased at the same level as that of the source. The body effect is also called the *back-gate effect* [2-22]. Usually, it is grounded but we can bias it to some voltage to adjust V_{th} of the device. The body terminal is called the 2nd gate also. Hence, the different potential at the body (2nd gate) changes the normal input-output functions of the MOSFET.

The derivation of current-voltage characteristics in the linear and saturation mode has been carried out with the underlying assumptions that the substrate potential is equal to the source terminal potential i.e. $V_{SB} = 0$.

5.2 Development of FAM Model for a 4-terminal MOSFET

Figure 5.2 shows the polarities applied across terminal voltages and drain current directions for both nMOS and pMOS devices, including the substrate [8-22] voltage V_{SB}.

We know that the substrate voltage or the *body bias* is the other very important factor which contributes to the drain current. If the body of the MOS device is *not* connected to the source, it works as a *back gate*, and the drain current has some dependency on the body bias voltage V_{SB}. Since the body bias (V_{SB}) functions as a gate terminal, and it is also treated as equivalent to a current source which depends on the body bias voltage in the *small-signal* equivalent circuit. The current source, due to the body bias, is represented as $g_{mb}v_{bs}$.

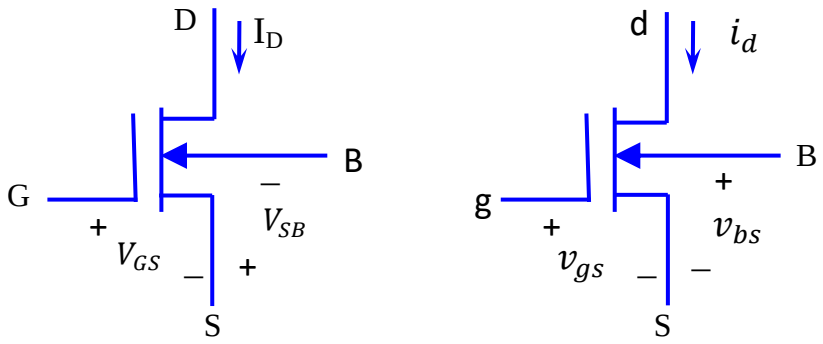

Fig. 5.2 Circuit Symbol Model of a 4-Terminal nMOSFET with (a) DC and (b) AC Voltages

The effect of V_{SB} on the cannel can be represented as a change in the threshold voltage V_t. With increasing reverse substrate bias, the voltage V_{SB} results in an increase in V_{th} according to relaship

$$V_{tn} = V_{th0} + \gamma\left(\sqrt{2\phi_f + v_{SB}} - \sqrt{2\phi_f}\right) \tag{5.8}$$

If there exists an ac component of voltage in the source-to-body (v_{sb}), there will be an ac component of voltage induced in the threshold voltage that causes an ac component in the drain current. Thus, a back-gate transconductance can be defined as;

$$g_{mb} = \frac{\partial I_D}{\partial V_{BS}}\Big|_{V_{GS}=k,V_{DS}=k} = -\frac{\partial I_D}{\partial V_{SB}}\Big|_{V_{GS}=k,V_{DS}=k} \text{ (as } V_{BS} = -V_{SB})$$

$$= -\left(\frac{\partial I_D}{\partial V_{tn}}\right)\left(\frac{\partial V_{tn}}{\partial V_{SB}}\right)\Big|_{V_{GS}=k,V_{DS}=k} \tag{5.9}$$

Using Eq. (5.6), we get

$$g_m = \frac{\partial I_D}{\partial V_{GS}}\Big|_{V_{DS}=k} = 2k_n\{V_{GS} - V_{tn}(V_{SB})\}$$

$$\frac{\partial I_D}{\partial V_{tn}} = 2k_n(V_{GS} - V_{tn})(-1) = -2k_n\{V_{GS} - V_{tn}(V_{SB})\} = -g_m \tag{5.10}$$

Using Eq. (5.8), we get

$$\frac{\partial V_{tn}}{\partial V_{SB}} = -\frac{\gamma}{2\sqrt{2\phi_f + v_{SB}}} = \eta \text{ (A very small fraction)} \tag{5.11}$$

The back-gate transconductance is then given as;

$$g_{mb} = -\left(\frac{\partial I_D}{\partial V_{tn}}\right)\left(\frac{\partial V_{tn}}{\partial V_{SB}}\right)\Big|_{V_{GS}=k, V_{DS}=k} = -(-g_m)(\eta) = \eta g_m \tag{5.12}$$

Thus, we see that due to two gates (the *front gate and the back gate*), we have two transconductances (g_m) and g_{mb}. The value of g_m is much greater than g_{mb}.

The approximate small-signal equivalent circuit of the 4-terminal MOSFET, including the *body effect*, is shown in Fig. 5.3. We should note the direction of the current and polarity of the small-signal source-to-body voltage. If $v_{bs} > 0$, then v_{SB} decreases, V_{tn} decreases, and i_D increases. The current direction and voltage polarity are thus consistent.

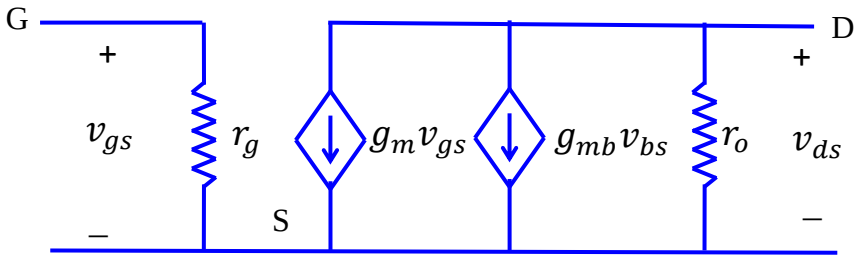

Fig. 5.3 Small-signal Circuit model of the nMOSFET with the body effect.

5.3 Small-signal Model Development of the MOSFET with $V_{SB} \neq 0$

Now, we will develop a more detailed small-signal equivalent model of a 4-terminal nMOSFET. For *non-zero body bias*, there is a voltage between the substrate and the source terminal of the MOSFET. This voltage (V_{SB}) functions as the back gate for the MOSFET. Hence, the input-output performance of the MOSFET will get affected. So its effect has to be included in the small-signal equivalent circuit of the MOSFET to both its input and output sides in the existing small-signal equivalent circuit described in all most all books. Hence, the simplified small-signal equivalent circuit of the MOSFET, including the effect of the V_{SB} is drawn as in Fig. 5.3. We know that the gate conductance g_g is negligibly small. Similarly, the back-gate conductance g_b will also be negligibly small. Let us analyze the most frequently used common source amplifier

circuit, including the effect of non-zero substrate voltage. Fig. 5.4 is the circuit representation of the common source.

The relationship between terminal voltages and currents in Fig. 5.4 are written as;

$$I_G = f_1(V_{GS}) \tag{5.13}$$

$$i_g = i_1 = g_g(v_g - v_s) = g_g(v_1 - v_3) \tag{5.14}$$

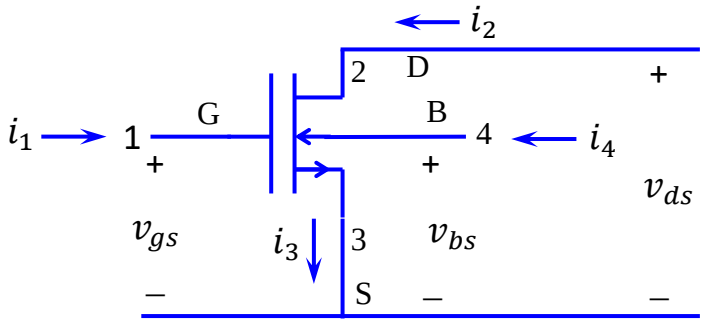

Fig. 5.4 Circuit Model of a 4-terminal Common-Source MOSFET Amplifier

Equation (5.14) is rearranged in terms of 4-terminal voltages v_1, v_2, v_3 and v_4 as;

$$i_1 = g_g v_1 + (0)v_2 - g_g v_3 + (0)v_4 \tag{5.15}$$

Similar to the normal gate, the back-gate current is expressed as;

$$i_b = -g_b(v_s - v_b) = -g_b v_3 + g_b v_4 \tag{5.16}$$

writing $i_b = i_4$; the back-gate current as the 4-terminal current becomes;

$$i_4 = -g_b v_3 + g_b v_4 \tag{5.17}$$

Arranging Eq. (5.17) in terms of 4-terminal voltages v_1, v_2, v_3, and v_4 as;

$$i_4 = -v_{sb}(g_b) = -g_b(v_s - v_b) = (0)v_1 + (0)v_2 - g_b v_3 + g_b v_4 \tag{5.18}$$

The mutual conductance between the output current and the back-gate voltage V_{BS} is defined as;

$$g_{mb} = \frac{\partial I_C}{\partial V_{BS}}\Big|_{V_{GS}\,\&\,V_{DS}=k} = \frac{\partial I_C}{\partial V_4}\Big|_{V_{GS}\,\&\,V_{DS}=k} \tag{5.19}$$

Hence, the total drain current is the combined effect of partial contribution due to changes in V_{GS}, V_{DS}, and V_{BS}.

$$i_g = g_g(v_g - v_s) \tag{5.20}$$

$$i_1 = g_g v_1 + (0)v_1 - g_g v_3 + (0)v_4 \tag{5.21}$$

The mutual conductance between the output current and the back-gate voltage g_{mb} is defined as;

$$g_{mb} = \frac{\partial I_C}{\partial V_{BS}}\Big|_{V_{GS}\,\&\,V_{DS}=k} = \frac{\partial I_C}{\partial V_4}\Big|_{V_{GS}\,\&\,V_{DS}=k} \tag{5.22}$$

Hence, the total drain current is the combined effect of the partial contribution due to a change in V_{GS}, V_{DS}, and V_{BS}. Hence, the total deviation in the drain current is mathematically expressed by a partial differential equation as;

$$\Delta I_D = \frac{\partial I_D}{\partial V_{GS}}\Big|_{V_{DS}\,\&\,V_{GB}=k} + \frac{\partial I_D}{\partial V_{DS}}\Big|_{V_{GS}\,\&\,V_{GB}=k} + \frac{\partial I_D}{\partial V_{BS}}\Big|_{V_{DS}\,\&\,V_{GS}=k} \tag{5.23}$$

$$i_d = g_m(v_g - v_s) + g_o(v_d - v_s) + g_{mb}(v_b - v_s)$$

$$i_d = g_m(v_1 - v_3) + g_o(v_2 - v_3) + g_{mb}(v_4 - v_3)$$

$$i_d = g_m v_1 - g_m v_3 + g_o v_2 - g_o v_3 + g_{mb} v_4 - g_{mb} v_3$$

$$i_2 = i_d = g_m v_1 + g_o v_2 - (g_m + g_o + g_{mb})v_3 + g_{mb} v_4 \tag{5.24}$$

$$i_s = -g_m v_1 - g_o v_2 + (g_m + g_o + g_{mb})v_3 - g_{mb} v_4 - g_g v_1$$

$$+g_g v_3 + g_b v_3 - g_b v_4$$

$$i_3 = i_s = -(g_g + g_m)v_1 - g_o v_2 + \big(g_g + g_m + g_o + g_{mb} + g_b\big)v_3$$

$$-(g_{mb} + g_b)v_4 \tag{5.25}$$

$$i_4 = i_b = -g_b(v_s - v_b) = -g_b v_3 + g_b v_4 \tag{5.26}$$

Writing $i_b = i_4$; the back-gate current in 4-terminal currents as;

$$i_4 = i_b = -v_{sb}(g_b) = -g_b(v_s - v_b) = (0)v_1 + (0)v_2 - g_b v_3 + g_b v_4 \tag{5.27}$$

The terminal voltages and currents of Eqs. (5.21), (5.24), (5.25), and (5.27) can be arranged in the form of floating admittance matrix [23-26] as;

$$\begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \end{bmatrix} = \begin{bmatrix} g_g & 0 & -g_g & 0 \\ g_m & g_o & -g_m - g_{mb} - g_o & g_{mb} \\ -g_g - g_m & -g_o & g_g + g_m + g_o + g_{mb} + g_b & -g_{mb} - g_b \\ 0 & 0 & -g_b & g_b \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \end{bmatrix} \quad (5.28)$$

From Eq. (5.28) is the floating admittance matrix of a 4-terminal MOSFET at low frequency as it does not have the capacitive effect. This Eq. (5.28) will be used to derive all transfer functions of the circuit's incorporating a 4-terminal MOSFET. Eq. (5.28) suggests the small-signal equivalent circuit model of a 4-terminal MOSFET as shown in Fig. 5.5.

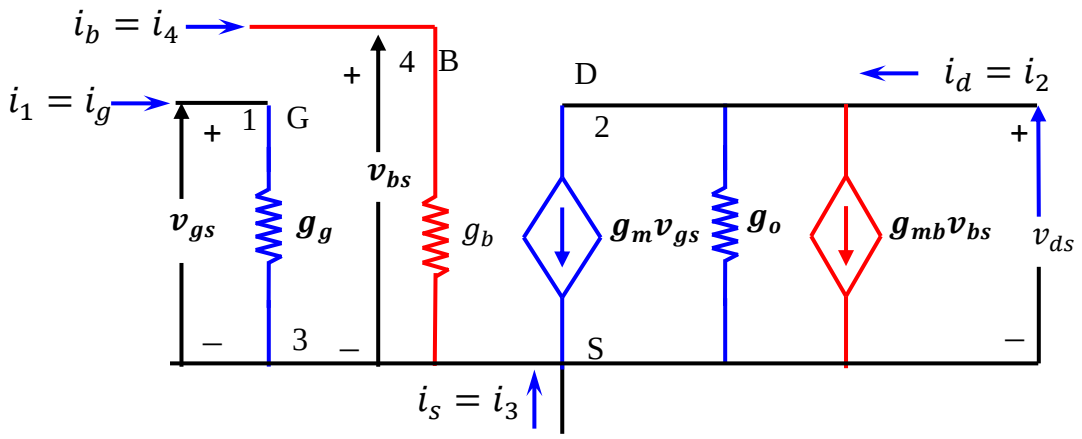

Fig. 5.5 Small-signal Model of a 4-terminal MOSFET with $V_{SB} \neq 0$

Now we will take advantage of the floating admittance matrix of Eq. (5.28) to derive all transfer functions of any circuit containing 4-terminal MOSFET.

5.4 Circuit Model of 4- terminal MOSFET phase-splitter Amplifier

Figs. 5.6 and 5.7 are the simple 4-terminal MOSFET phase-splitter amplifier and its ac circuit, respectively. The phase-splitter amplifier provides two outputs: one at the drain point and the other at the source point. These two outputs are 180^0 apart.

Since, $g_g \rightarrow 1\ pS$, it is neglected w.r.t. the other parameters of the MOSFET $g_o \rightarrow 0.02\ mS$, and $g_m \rightarrow 1\ mS$, $g_{mb} = \eta g_m \rightarrow 0.1\ mS$.

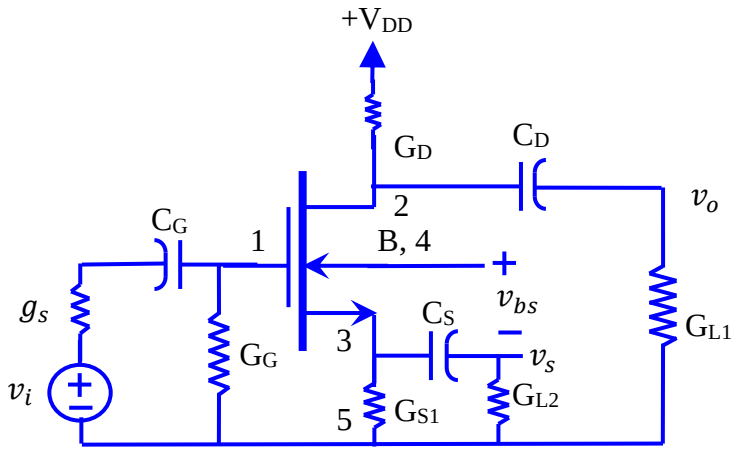

Fig. 5.6 Circuit Model of a 4-terminal MOSFET Phase-Splitter Amplifier

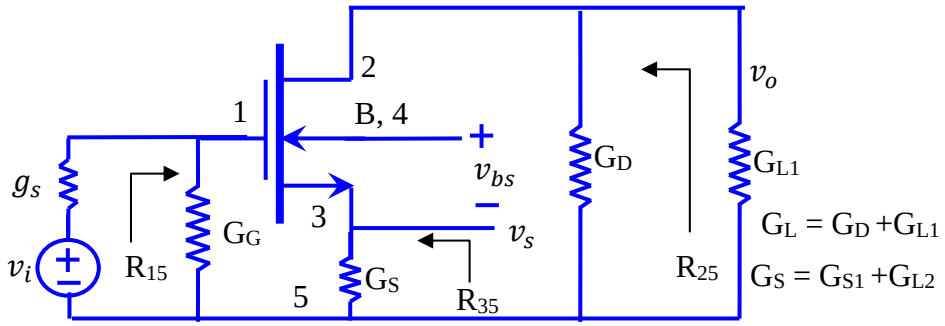

Fig. 5.7 AC circuit model of a 4-terminal MOSFET Phase-Splitter Amplifier

The floating admittance matrix representation of the 4-terminal MOSFET in the 4x4 matrix is repeated here for ease in further analysis.

$$\begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \end{bmatrix} = \begin{bmatrix} 1 & 2 & 3 & 4 \\ g_g & 0 & -g_g & 0 \\ g_m & g_o & g_m - g_o - g_{mb} & g_{mb} \\ -g_g - g_m & -g_o & g_g + g_m + g_{mb} + g_o + g_b & -g_{mb} - g_b \\ 0 & 0 & -g_b & g_b \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \end{bmatrix} \quad (5.29)$$

Ideally, the gate current of FETs/MOSFETs is zero, $g_g \rightarrow 0$. Since the MOSFET phase-splitter amplifier has 5-nodes, then the 4-node floating admittance matrix in Eq. (5.29) is converted to a 5x5 matrix as;

$$\begin{bmatrix} \\ i_1 \\ i_2 \\ i_3 \\ i_4 \\ i_5 \end{bmatrix} = \begin{bmatrix} 1 & 2 & 3 & 4 & 5 \\ 0 & 0 & 0 & 0 & 0 \\ g_m & g_o & g_m - g_o - g_{mb} & g_{mb} & 0 \\ -g_m & -g_o & g_m + g_{mb} + g_o + g_b & -g_{mb} - g_b & 0 \\ 0 & 0 & -g_b & g_b & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} \\ v_1 \\ v_2 \\ v_3 \\ v_4 \\ v_5 \end{bmatrix} \tag{5.30}$$

The floating admittance matrix of the passive components used in the 4-terminal MOSFET phase-splitter amplifier of Fig. 5.7 is;

$$\begin{bmatrix} \\ i_1 \\ i_2 \\ i_3 \\ i_4 \\ i_5 \end{bmatrix} = \begin{bmatrix} 1 & 2 & 3 & 4 & 5 \\ \mathrm{g_s + G_G} & 0 & 0 & 0 & \mathrm{-g_s - G_G} \\ 0 & \mathrm{G_L} & 0 & 0 & \mathrm{-G_L} \\ 0 & 0 & \mathrm{G_S} & 0 & \mathrm{-G_S} \\ 0 & 0 & 0 & 0 & 0 \\ \mathrm{-g_s - G_G} & \mathrm{-G_L} & \mathrm{-G_S} & 0 & \mathrm{g_s + G_G + G_L + G_S} \end{bmatrix} \begin{bmatrix} \\ v_1 \\ v_2 \\ v_3 \\ v_4 \\ v_5 \end{bmatrix} \tag{5.31}$$

Now, Eqs (5.30) and (5.31) are merged together as per the node specifications to yield the overall floating admittance matrix of the 5-node 4-terminal MOSFET phase-splitter amplifier as;

$$\begin{bmatrix} \\ i_1 \\ i_2 \\ i_3 \\ i_4 \\ i_5 \end{bmatrix} = \begin{bmatrix} 1 & 2 & 3 & 4 & 5 \\ \mathrm{g_s + G_G} & 0 & 0 & 0 & \mathrm{-g_s - G_G} \\ g_m & g_o + \mathrm{G_L} & g_m - g_o - g_{mb} & g_{mb} & \mathrm{-G_L} \\ -g_m & -g_o & g_m + g_{mb} + g_o + g_b + \mathrm{G_S} & -g_{mb} - g_b & \mathrm{-G_S} \\ 0 & 0 & -g_b & g_b & 0 \\ \mathrm{-g_s - G_G} & \mathrm{-G_L} & \mathrm{-G_S} & 0 & \mathrm{g_s + G_G + G_L + G_S} \end{bmatrix} \begin{bmatrix} \\ v_1 \\ v_2 \\ v_3 \\ v_4 \\ v_5 \end{bmatrix} \tag{5.32}$$

Now, from this Eq. (5.32), the floating admittance matrix of all the four configurations, i.e. common-source, common-drain, and common-gate 4-terminal MOSFET amplifiers, will be derived easily.

5.5 Circuit Model of a Four Terminal MOSFET C-S Amplifier

We now proceed to derive the floating admittance matrix of a common-source amplifier (CS) using Eq. (5.32) from the 4-terminal phase-splitter MOSFET amplifier. For that, adding the 3rd row to the 5th row and the 3rd column to the 5th column and deleting the original the 3rd row and the 3rd column after assigning the 5th row and the 5th column as the 3rd row and the 3rd column yields as;

$$\begin{bmatrix} 1 & 2 & 4 & 3 \\ g_s + G_G & 0 & 0 & -g_s - G_G \\ g_m & g_o + G_L & g_{mb} & -g_m - g_{mb} - g_o - G_L \\ 0 & 0 & g_b & -g_b \\ -g_m - g_s - G_G & -g_o - G_L & -g_{mb} - g_b & g_m + g_o + g_{mb} + g_b + g_s + G_G + G_L \end{bmatrix} \tag{5.33}$$

Equation (5.33) is the floating admittance matrix of a 4-terminal MOSFET CS amplifier derived from Eq. (5.32) of a 4-terminal MOSFET phase-splitter amplifier circuit in Fig. 5.7. From this Eq. (5.33), the circuit of a MOSFET CS amplifier is drawn as in Fig. 5.8.

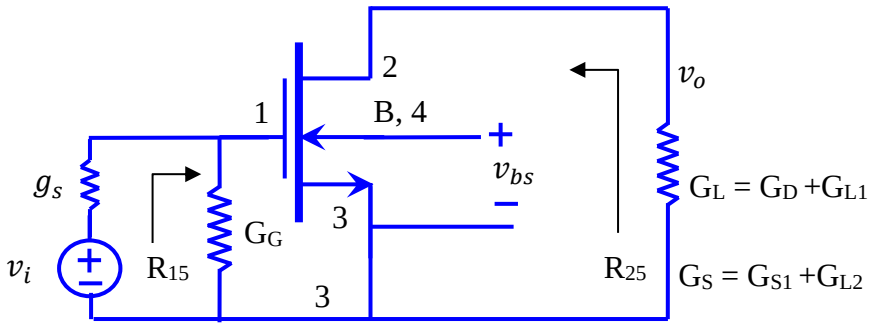

Fig. 5.8 AC Circuit Model of a 4-terminal MOSFET Common-Source Amplifier

The voltage gain [23-26] between the output terminals 2 & 3 and the input terminals 1 & 3 of a 4-terminal MOSFET CS amplifier in Fig. 5.8 using Eq. (5.33) is expressed as;

$$A_v|_{13}^{23} = sgn(2-3)sgn(1-3)(-1)^9 \frac{|Y_{23}^{13}|}{|Y_{13}^{13}|} \tag{5.34}$$

$$|Y_{23}^{13}| = \begin{vmatrix} g_m & g_{mb} \\ 0 & g_b \end{vmatrix} = g_m g_b,$$

$$|Y_{13}^{13}| = \begin{vmatrix} g_o + G_L & g_{mb} \\ 0 & g_b \end{vmatrix} = (g_o + G_L) g_b$$

$$A_v|_{13}^{23} = -\frac{g_m g_b}{(g_o+G_L)g_b} = -\frac{g_m}{(g_o+G_L)} \quad = -g_m(r_o \parallel R_L)$$

$$= -g_m(r_o \parallel R_D \parallel R_L) = g_m(r_o \parallel R_D \parallel R_L)\angle 180^0 \tag{5.35}$$

The current gain [23-26] between the output terminals 2 & 3 and the input terminals 1 & 3 of a 4-terminal MOSFET CS amplifier in Fig. 5.8 using Eq. (5.33) is expressed as follows;

$$\mathrm{A_i}|_{13}^{23} = \mathrm{sgn}(2-3)\mathrm{sgn}(1-3)(-1)^8 \frac{|\mathrm{Y}_{23}^{13}|}{|\mathrm{Y}_3^3|} \mathrm{G_L} \tag{5.36}$$

$$|Y_3^3| = \begin{vmatrix} g_s + G_G & 0 & 0 \\ g_m & g_o + G_L & g_{mb} \\ 0 & 0 & g_b \end{vmatrix} = (g_s + G_G)(g_o + G_L) g_b$$

$$A_i|_{13}^{23} = -\frac{g_m g_b G_L}{(g_s+G_G)(g_o+G_L)g_b} = -\frac{g_m G_L}{(g_s+G_G)(g_o+G_L)}$$

$$= -g_m(r_s)(R_D \parallel R_L)G_L = g_m(r_s)(R_D \parallel R_L)G_L \angle 180^0 \quad (5.37)$$

The input resistance [23-26] between the input terminals 1 & 3 of a 4-terminal MOSFET CS amplifier in Fig. 5.8 using Eq. (5.33) is expressed as;

$$R_{in} = R_{13} = \frac{|Y_{13}^{13}|}{|Y_3^3|}_{g_s=0}$$

$$|Y_3^3|_{g_s=0} = G_G(g_o + G_L)g_b \quad (5.38)$$

$$R_{in} = R_{13} = \frac{(g_o+G_L)g_b}{G_G(g_o+G_L)g_b} = R_G \quad (5.39)$$

Now, the input resistance R_G of the amplifier is connected across the ac input voltage source (v_s) in series with its internal resistance (r_s) as in Fig. 5.9.

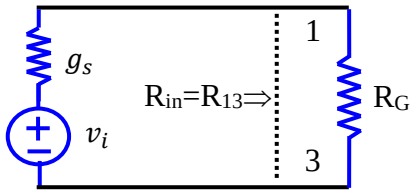

Fig. 5.9 Effective Voltage Gain Model with Source Voltage and Resistance of a 4-terminal MOSFET CS Amplifier

From Fig. 5.9, the effect of source resistance on the overall voltage gain can be estimated as follows;

$$\frac{v_{13}}{v_i} = \frac{R_{in}}{R_{in}+r_s} = \frac{R_G}{R_G+r_s} = 1 \ (R_G >> rs) \quad (5.40)$$

$$A_{vs} = \frac{v_{23}}{v_{13}} x \frac{v_{13}}{v_i} = \frac{v_{23}}{v_i} = \{-g_m(r_o \parallel R_D \parallel R_L)\}\left(\frac{R_G}{R_G+r_s}\right)$$

$$= -g_m(r_o \parallel R_D \parallel R_L) = g_m(r_o \parallel R_D \parallel R_L)\angle 180^0 \quad (5.41)$$

Equation (5.41) reveals that the voltage developed across the actual input terminals 1 and 3 of the MOSFET CS amplifier is the open circuit signal voltage v_s, as $r_s << R_G$. Hence, the overall voltage gain of the amplifier, including the source resistance, is not affected by the source resistance r_s and is expressed as;

$$A_{vs}|_{13}^{23} = \frac{v_{13}}{v_i} x \frac{v_{23}}{v_{13}} = -g_m(r_o \parallel R_D \parallel R_L) \cong g_m(R_D \parallel R_L)\angle 180^0 \quad (5.42)$$

The voltage gain given in Eq. (5.42) of a MOSFET CS amplifier in Fig. 5.7 is available in all standard books [2-13]. This corroborates the correctness of the proposed technique.

The output resistance [23-26] between the output terminals 2 & 3 of the 4-terminal MOSFET CS amplifier in Fig. 5.8 using Eq. (5.33) is expressed as;

$$R_o = R_{23} = \frac{|Y_{23}^{23}|}{|Y_3^3|}_{G_L=0} \quad (5.43)$$

$$|Y_{23}^{23}| = \begin{vmatrix} g_s + G_G & 0 \\ 0 & g_b \end{vmatrix} = (g_s + G_G)g_b$$

$$|Y_3^3|_{G_L=0} = \begin{vmatrix} g_s + G_G & 0 & 0 \\ g_m & g_o + G_D + G_L & g_{mb} \\ 0 & 0 & g_b \end{vmatrix} = (g_s + G_G)(g_o + G_D)g_b$$

$$R_o = R_{23} = \frac{(g_s+G_G)g_b}{(g_s+G_G)(g_o+G_D)g_b} = \frac{1}{g_o+G_D} = r_o \| R_D \quad (5.44)$$

The output resistance seen accros R_D in Fig. 5.8 is the effective output resistance given as;

$$R_o = R_{23} = r_o \parallel R_D \cong R_D \quad (5.45)$$

The power gain [23-26] between the output terminals 2 & 3 and the input terminals 1 & 3 of a 4-terminal MOSFET CS amplifier in Fig. 5.8 using Eq. (5.33) is expressed as ;

$$A_P|_{13}^{23} = A_v|_{13}^{23} x A_i|_{13}^{23} = \{-g_m(R_D \parallel R_L)\}\{-g_m(r_s)(R_D \parallel R_L)G_L\}$$
$$\cong g_m^2(R_D \parallel R_L)^2 r_s G_L \quad (5.46)$$

5.6 Circuit Model of a 4-terminal MOSFET C D Amplifier

The floating admittance matrix of a MOSFET phase-splitter circuit of Eq. (5.32) is again manuevoured by adding the 2nd row and the 2nd column to the 5th row and the 5th column. Then the 5th row and the 5th columns are assigned as the 2nd row and the 2nd column after deleting the original 2nd row and the 2nd column to derive the over all floating admittance matrix of a 4-terminal common-drain (CD) amplifier as in Eq. (5.47).

$$\begin{bmatrix} 1 & 3 & 4 & 2 \\ g_s + G_G & 0 & 0 & -g_s - G_G \\ -g_m & g_m + g_o + g_{mb} + g_b + G_S & -g_{mb} - g_b & -g_o - G_S \\ 0 & -g_b & g_b & 0 \\ g_m - g_s - G_G & -G_S - g_m - g_o - g_{mb} & g_{mb} & g_s + G_G + g_o + G_L \end{bmatrix} \begin{bmatrix} 1 \\ 3 \\ 4 \\ 2 \end{bmatrix} \quad (5.47)$$

The circuit of a common-drain amplifier is drawn in Fig. 5.10 using Eq. (5.47).

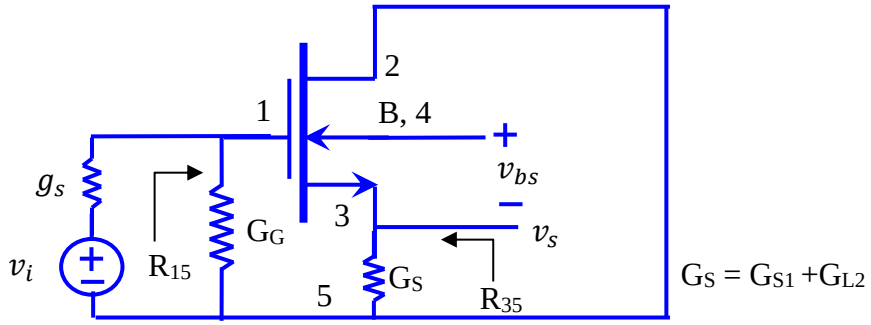

Fig. 5.10 AC circuit model of a 4-terminal CD Amplifier

The voltage gain [23-26] between the output terminals 3 & 2 and the input terminals 1 & 2 of a 4-terminal MOSFET CD amplifier in Fig. 5.10 using Eq. (5.47) is expressed as follows;

$$A_v|_{12}^{32} = sgn(3-2)sgn(1-2)(-1)^8 \frac{|Y_{32}^{12}|}{|Y_{12}^{12}|} \quad (5.48)$$

$$|Y_{32}^{12}| = \begin{vmatrix} -g_m & -g_{mb} - g_b \\ 0 & g_b \end{vmatrix} = -g_m g_b$$

$$|Y_{12}^{12}| = \begin{vmatrix} g_m + g_o + g_{mb} + g_b + G_S & -g_{mb} - g_b \\ -g_b & g_b \end{vmatrix}$$

$$= \begin{vmatrix} g_m + g_o + G_S & -g_{mb} - g_b \\ 0 & g_b \end{vmatrix} = (g_m + g_o + G_S) g_b$$

$$A_v|_{12}^{32} = -\frac{-g_m g_b}{(g_m + g_o + G_S) g_b} = \frac{g_m}{(g_m + g_o + G_S)} = g_m \left(\frac{1}{g_m} \| r_o \| R_S\right)$$

$$\cong g_m \left(\frac{1}{g_m} \| R_S\right) = \left(\frac{R_S}{\frac{1}{g_m} + R_S}\right) = \left(\frac{g_m R_S}{1 + g_m R_S}\right) \quad (5.49)$$

$$\cong 1 \text{ (ideal)} \quad (5.50)$$

The current gain [23-26] between the output terminals 3 & 2 and the input terminals 1 & 2 of a 4-terminal MOSFET CD amplifier in Fig. 5.10 using Eq. (5.47) is expressed as;

$$A_i|_{12}^{32} = sgn(3-2)sgn(1-2)(-1)^8 \frac{|Y_{32}^{12}|}{|Y_2^2|} G_L \tag{5.51}$$

$$|Y_2^2| = \begin{vmatrix} g_s + G_G & 0 & 0 \\ -g_m & g_m + g_o + g_{mb} + g_b + G_S & -g_{mb} - g_b \\ 0 & -g_b & g_b \end{vmatrix}$$

$$= \begin{vmatrix} g_s + G_G & 0 & 0 \\ -g_m & g_m + g_o + G_S & -g_{mb} - g_b \\ 0 & 0 & g_b \end{vmatrix}$$

$$= g_b(g_s + G_G)(g_m + g_o + G_S)$$

$$A_i|_{12}^{32} = -\frac{-g_m g_b G_L}{g_b(g_s+G_G)(g_m+g_o+G_S)} = \frac{g_m G_L(r_s \| R_G)}{(g_m+G_S)} = g_m G_L(r_s \parallel R_G)(\frac{1}{g_m} \| R_S)$$

$$= g_m G_L(r_s \parallel R_G)\left(\frac{1}{g_m}\right) = G_L(r_s \parallel R_G) = \frac{(r_s \| R_G)}{R_L} \tag{5.52}$$

The input resistance [23-26] between the input terminals 1 & 2 of a 4-terminal MOSFET CD amplifier in Fig. 5.10 using Eq. (5.47) is expressed as ;

$$R_{in} = R_{12} = \frac{|Y_{12}^{12}|}{|Y_2^2|}_{g_s=0} \tag{5.53}$$

$$|Y_2^2|_{g_s=0} = g_b G_G(g_m + g_o + G_S)$$

$$R_{in} = R_{12} = \frac{|Y_{12}^{12}|}{|Y_2^2|}_{g_s=0} = \frac{(g_m+g_o+G_S)g_b}{g_b G_G(g_m+g_o+G_S)} = \frac{1}{G_G} = R_G \tag{5.54}$$

The overall voltage gain of the MOSFET CD amplifier including the effect of the signal source resistance is obtained by deriving the actual input voltage appearing at the gate terminal of the amplifier as in Fig. 5.11.

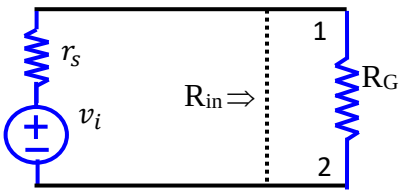

Fig. 5.11 Effective Voltage Gain Model with Source Voltage of a 4-terminal MOSFET CD Amplifier

From Fig. 5.11, $v_{12} = v_i \frac{R_G}{r_s+R_G} \cong v_i$; as $r_s \ll R_G$ (5.55)

Now, $A_{vs} = \frac{v_{32}}{v_{12}} x \frac{v_{12}}{v_i} = A_v|_{12}^{32} x \frac{v_{12}}{v_i} = \left(\frac{R_S}{\frac{1}{g_m}+R_S}\right) x1 = \left(\frac{g_m R_S}{1+g_m R_S}\right) \cong 1$ (5.56)

The output resistance [23-26] between the output terminals 3 & 2 of a 4-terminal MOSFET CD amplifier in Fig. 5.10 using Eq. (5.47) is written as ;

$$R_{out} = R_{32} = \frac{|Y_{32}^{32}|}{|Y_2^2|}_{G_L=0} \quad (5.57)$$

$$|Y_{32}^{32}| = \begin{vmatrix} g_s + G_G & 0 \\ 0 & g_b \end{vmatrix} = (g_s + G_G) g_b$$

$$|Y_2^2|_{G_S=0} = g_b(g_s + G_G)(g_m + g_o)$$

$$R_{out} = R_{32} = \frac{(g_s+G_G)g_b}{(g_s+G_G)(g_m+g_o)g_b} = \frac{1}{(g_m+g_o)} = \frac{1}{g_m} || r_o \cong \frac{1}{g_m} \quad (5.58)$$

The power gain [23-26] between the output terminals 3 & 2 and the input terminals 1 & 2 of a 4-terminal MOSFET CD amplifier in Fig. 5.10 using Eq. (5.47) is written as ;

$$A_P|_{12}^{32} = A_v|_{12}^{32} x A_i|_{12}^{32} = (1) \frac{(r_s || R_G)}{R_L} = \left\{\frac{r_s || R_G}{R_L}\right\} \quad (5.59)$$

5.7 Circuit Model of a 4-terminal MOSFET CG Amplifier

The floating admittance matrix of a MOSFET common-gate (CG) amplifier results from the MOSFET phase-splitter amplifier shown in Fig. 5.7 and its Eq. (5.32) by adding the 1st row and the 1st column to the 5th row and the 5th column and deleting the original 1st row and the 1st column after assigning the 5th row and the 5th column as the 1st row and the 1st column as;

$$\begin{bmatrix} 2 & 3 & 4 & 1 \\ g_o + G_L & -g_m - g_o - g_{mb} & g_{mb} & g_m - G_L \\ -g_o & g_m + g_o + g_{mb} + g_b + g_s & -g_{mb} - g_b & -g_m - g_s \\ 0 & -g_b & g_b & 0 \\ -G_L & -g_s & 0 & G_L + g_s \end{bmatrix} \begin{bmatrix} 2 \\ 3 \\ 4 \\ 1 \end{bmatrix} \quad (5.60)$$

Figure 5.12 is the circuit of the CG amplifier derived from Eq. (5.60) after assigning $G_s + g_s = 1/(R_s \| r_s) = g_s$ to serve as the input source resistance.

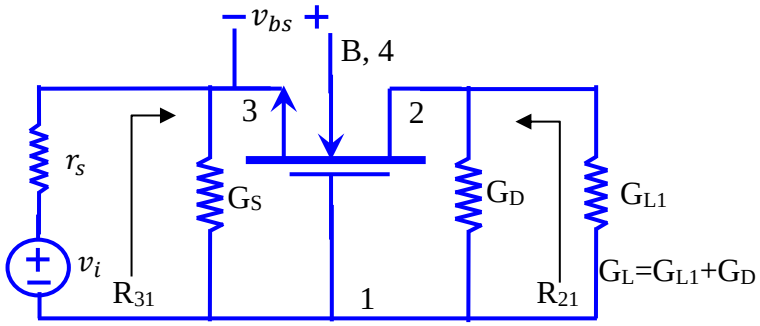

Fig. 5.12 Circuit Model of a 4-terminal CG MOSFET Amplifier

Here, also $G_L=G_{L1} + G_D$

The voltage gain [23-26] between the output terminals 2 & 1 and the input terminals 3 & 1 of a 4-terminal MOSFET CG amplifier in Fig. 5.12 using Eq. (5.60) is expressed as follows;

$$A_v|_{31}^{21} = sgn(2-1)sgn(3-1)(-1)^7 \frac{|Y_{21}^{31}|}{|Y_{31}^{31}|} \quad (5.61)$$

$$|Y_{21}^{31}| = \begin{vmatrix} -g_m - g_{mb} & -g_o & g_{mb} \\ & -g_b & g_b \end{vmatrix} = \begin{vmatrix} -g_m - g_o & g_{mb} \\ 0 & g_b \end{vmatrix} = -(g_m + g_o)g_b$$

$$|Y_{31}^{31}| = \begin{vmatrix} g_o + G_L & g_{mb} \\ 0 & g_b \end{vmatrix} = (g_o + G_L)g_b$$

$$A_v|_{31}^{21} = -\frac{-(g_m+g_o)g_b}{(g_o+G_L)g_b} = \frac{(g_m+\cancel{g_o})}{(g_o+G_L)} = g_m(r_o \parallel R_L) = g_m R_L \quad (5.62)$$

where, $R_L = R_D \parallel R_{L1}$

The current gain [23-26] between the output terminals 2 & 1 and the input terminals 3 & 1 of a 4-terminal MOSFET CG amplifier in Fig.5.12 using Eq. (5.60) is expressed as follows;

$$A_i|_{31}^{21} = sgn(2-1)sgn(3-1)(-1)^7 \frac{|Y_{21}^{31}|}{|Y_1^1|} G_L \tag{5.63}$$

$$|Y_1^1| = \begin{vmatrix} g_o + G_L & -g_m - g_{mb} - g_o & g_{mb} \\ -g_o & g_m + g_{mb} + g_o + +g_b + g_S & -g_{mb} - g_b \\ 0 & -g_b & g_b \end{vmatrix}$$

$$= \begin{vmatrix} g_o + G_L & -g_m - g_o & g_{mb} \\ G_L & g_S & 0 \\ 0 & 0 & g_b \end{vmatrix} = g_b\{(g_o + G_L)g_S + G_L(g_m + g_o)\}$$

$$A_i|_{31}^{21} = \frac{(g_m + \cancel{g_o})g_b}{g_b\{(g_o+G_L)g_S + G_L(g_m + \cancel{g_o})\}} G_L = \frac{g_m G_L}{\{g_S + g_m\}G_L} = g_m \left\{ r_S \| \frac{1}{g_m} \right\} \cong 1 \tag{5.64}$$

The input resistance [23-26] between the input terminals 3 & 1 of a 4-terminal MOSFET CG amplifier in Fig. 5.12 using Eq. (5.60) is expressed as ;

$$R_{in} = R_{31} = \frac{|Y_{31}^{31}|}{|Y_1^1|}_{g_s=0} \tag{5.65}$$

$$|Y_1^1|_{g_s=0} = g_b\{(g_o + G_L)\cancel{g_S} + G_L(g_m + g_o)\} = g_b G_L(g_m + g_o)$$

$$R_{in} = R_{31} = \frac{|Y_{31}^{31}|}{|Y_1^1|}_{g_s=0} = \frac{(\cancel{g_o} + G_L)g_b}{g_b(g_m + \cancel{g_o})G_L} = \frac{(G_L)R_L}{g_m} = \frac{1}{g_m} \tag{5.66}$$

Figure 5.13 gives effective input voltage across the gate and source terminals of the MOSFET CG amplifier in Fig. 5.12.

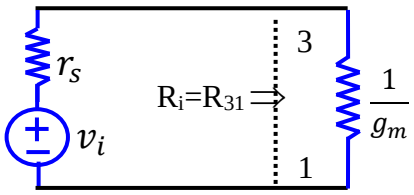

Fig. 5.13 Effective Voltage Gain Model with Source Voltage and Resistance of a 4-terminal MOSFET CG Amplifier

From Fig. 5.13, $\frac{v_{31}}{v_i} = \frac{R_i}{r_s + R_i} = \frac{1/g_m}{r_s + 1/g_m}$

$$A_{vs} = A_v|_{31}^{21} x \frac{v_{31}}{v_i} = [g_m(r_o \parallel R_D \parallel R_L)] \left(\frac{1/g_m}{r_s + 1/g_m} \right)$$

$$= [(r_o \parallel R_D \parallel R_L)] \left(\frac{1}{r_s + 1/g_m} \right) \tag{5.67}$$

The output resistance [23-26] between the output terminals 2 & 1 of a 4-terminal MOSFET CG amplifier in Fig. 5.12 using Eq. (5.60) is expressed as ;

$$R_{out} = R_{21} = \frac{|Y_{21}^{21}|}{|Y_1^1|}_{G_L=0} \tag{5.68}$$

$$|Y_{21}^{21}| = \begin{vmatrix} g_m + g_o + g_{mb} + g_b + g_S & -g_{mb} - g_b \\ -g_b & g_b \end{vmatrix}$$

$$= \begin{vmatrix} g_m + g_o + g_S & -g_{mb} - g_b \\ 0 & g_b \end{vmatrix} = (g_m + g_o + g_S)g_b$$

$$|Y_1^1|_{G_L=0} = g_b\{(g_o + G_D + \cancel{G_L})g_S + (G_D + \cancel{G_L})(g_m + \cancel{g_o})\}$$

$$= G_D g_b\{g_S + g_m\}$$

$$R_{out} = R_{21} = \frac{(g_m+g_o+g_S)g_b}{G_D g_b\{g_S+g_m\}} = \frac{g_m+g_o+g_S}{g_S+g_m} R_D = R_D \tag{5.69}$$

The power gain [23-26] between the output terminals 2 & 1 and the input terminals 3 & 1 of a 4-terminal MOSFET CG amplifier in Fig. 5.12 using Eq. (5.60) is written as;

$$A_P|_{31}^{21} = A_v|_{31}^{21} x\, A_i|_{31}^{21} = \{g_m(r_o \parallel R_D \parallel R_L)\}\{1\} = g_m(r_o \parallel R_D \parallel R_L) \tag{5.70}$$

5.8 Circuit Model of a 4-terminal MOSFET Phase-Splitter Amplifier (complete analysis)

To derive all transfer and self-port functions between output terminals 2 & 5 and input terminals 1 & 5 of the 4-terminal MOSFET phase-splitter amplifier circuit in Fig. 5.7, we take the help of Eq. (5.32).

The voltage gain [23-26] between the output terminals 2 & 5 and the input terminals 1 & 5 of a 4-terminal MOSFET phase-splitter amplifier circuit in Fig. 5.7 using Eq. (5.32) is expressed as;

$$A_v|_{15}^{25} = sgn(2-5)sgn(1-5)(-1)^{13}\frac{|Y_{25}^{15}|}{|Y_{15}^{15}|} \tag{5.71}$$

From Eq. (5.32), $|Y_{25}^{15}| = \begin{vmatrix} g_m & -g_m - g_o - g_{mb} & g_{mb} \\ -g_m & g_m + g_o + g_{mb} + g_b + G_S & -g_{mb} - g_b \\ 0 & -g_b & g_b \end{vmatrix}$

$$= \begin{vmatrix} g_m & -g_o & g_{mb} \\ 0 & G_S & 0 \\ 0 & 0 & g_b \end{vmatrix} = g_b g_m G_S$$

$$|Y_{15}^{15}| = \begin{vmatrix} g_o + G_L & -g_m - g_o - g_{mb} & g_{mb} \\ -g_o & g_m + g_o + g_{mb} + g_b + G_S & -g_{mb} - g_b \\ 0 & -g_b & g_b \end{vmatrix}$$

$$= \begin{vmatrix} g_o + G_L & -g_m - g_o & g_{mb} \\ G_L & G_S & 0 \\ 0 & 0 & g_b \end{vmatrix}$$

$$= g_b\{(g_o + G_L)G_S + (g_m + g_o)G_L\} \quad = g_b\{G_S + g_m\}G_L$$

$$A_v|_{15}^{25} = -\frac{g_b g_m G_S}{g_b\{G_S+g_m\}G_L} = -\frac{g_m R_L}{\{G_S+g_m\}R_S} = -\frac{g_m R_L}{1+g_m R_S} \tag{5.72}$$

$$= -\frac{g_m(\mathrm{R_D}\|\mathrm{R_L})}{1+g_m R_S} \quad \text{(here effective load resistance } = \mathrm{R_D}\|\mathrm{R_L}) \tag{5.73}$$

The voltage gain [23-26] between the output terminals 3 & 5 and the input terminals 1 & 5 of a 4-terminal MOSFET phase-splitter amplifier circuit in Fig. 5.7 using Eq. (5.32) is expressed as;

$$A_v|_{15}^{35} = sgn(3-5)sgn(1-5)(-1)^{14}\frac{|Y_{35}^{15}|}{|Y_{15}^{15}|} \tag{5.74}$$

From Eq. (5.32), $|Y_{35}^{15}| = \begin{vmatrix} g_m & g_o + G_L & g_{mb} \\ -g_m & -g_o & -g_{mb} - g_b \\ 0 & 0 & g_b \end{vmatrix} = \begin{vmatrix} g_m & g_o + G_L & g_{mb} \\ 0 & G_L & 0 \\ 0 & 0 & g_b \end{vmatrix}$

$$= g_b g_m G_L$$

$$A_v|_{15}^{35} = \frac{g_b g_m G_L}{g_b\{G_S+g_m\}G_L} = \frac{g_m R_S}{\{1+g_m R_S\}} \tag{5.75}$$

If we select $G_L = G_S$, then Eqs. (5.72) and (5.75) become exactly equal in magnitude but 180^0 phase apart. For this reason, the circuit is called a phase-splitter amplifier.

The current gain [23-26] between the output terminals 2 & 5 and the input terminals 1 & 5 of a 4-terminal MOSFET phase-splitter amplifier circuit in Fig. 5.7 using Eq. (5.32) is expressed as;

$$A_i|_{15}^{25} = sgn(2-5)sgn(1-5)(-1)^{13}\frac{|Y_{25}^{15}|}{|Y_5^5|}G_L \tag{5.76}$$

From Eq. (5.32),

$$\left|Y_5^5\right| = \begin{vmatrix} g_s + G_G & 0 & 0 & 0 \\ g_m & g_o + G_L & -g_m - g_o - g_{mb} & g_{mb} \\ -g_m & -g_o & g_m + g_o + g_{mb} + g_b + G_S & -g_{mb} - g_b \\ 0 & 0 & -g_b & g_b \end{vmatrix}$$

$$= \begin{vmatrix} g_s + G_G & 0 & 0 & 0 \\ g_m & g_o + G_L & -g_m - g_o & g_{mb} \\ 0 & G_L & G_S & 0 \\ 0 & 0 & 0 & g_b \end{vmatrix}$$

$$= (g_s + G_G) \begin{vmatrix} g_o + G_L & -g_m - g_o & g_{mb} \\ G_L & G_S & 0 \\ 0 & 0 & g_b \end{vmatrix}$$

$$= (-1)^{3+3} g_b (g_s + G_G)\{(\cancel{g_o} + G_L)G_S + G_L(g_m + \cancel{g_o})\}$$

$$= g_b(g_s + G_G)\{G_L G_S + g_m G_L\}$$

$$\left|Y_5^5\right| = g_b(g_s + G_G)G_L(G_S + g_m)$$

$$A_i|_{15}^{25} - \frac{|Y_{25}^{15}|}{|Y_5^5|} G_L = -\frac{g_b g_m G_S}{g_b(g_s+G_G)G_L(G_S+g_m)} G_L = -\frac{g_m G_S}{(g_s+G_G)(G_S+g_m)} = -\frac{g_m(r_s \| R_G)}{(1+g_m R_S)} \quad (5.77)$$

$$= -\frac{g_m r_s}{1+g_m R_S} \quad (5.78)$$

Similarly, the current gain [23-26] between the output terminals 3 & 5 and the input terminals 1 & 5 using Eq. (5.32) of a 4-terminal MOSFET phase-splitter amplifier circuit in Fig. 5.7 is expressed as;

$$A_i|_{15}^{35} = sgn(3-5)sgn(1-5)(-1)^{14} \frac{|Y_{35}^{15}|}{|Y_5^5|} G_S \quad (5.79)$$

$$A_i|_{15}^{25} - \frac{|Y_{25}^{15}|}{|Y_5^5|} G_L = -\frac{g_b g_m G_S}{g_b(g_s+G_G)G_L(G_S+g_m)} G_L = -\frac{g_m G_S}{(g_s+G_G)(G_S+g_m)} = -\frac{g_m(r_s \| R_G)}{(1+g_m R_S)}$$

$$= -\frac{g_m r_s}{1+g_m R_S} \quad (5.80)$$

Equations (5.77) and (5.80) are exactly equal in magnitude but differs in phase by 180^0.

The input resistance [23-26] between the input terminals 1 & 5 of a 4-terminal MOSFET phase-splitter amplifier circuit in Fig. 5.7 using Eq. (5.32) is expressed as ;

$$R_{in} = R_{15} = \frac{|Y_{15}^{15}|}{|Y_5^5|}_{g_s=0} \quad (5.81)$$

$$\left|Y_5^5\right|_{g_s=0} = g_b(\cancel{g_s} + G_G)G_L(G_S + g_m) = g_b G_G G_L(G_S + g_m)$$

$$R_{in} = R_{15} = \frac{g_b\{G_S+g_m\}G_L}{g_b G_G G_L(G_S+g_m)} = \frac{1}{G_G} = R_G$$

The output resistance [14-17] between the output terminals 2 & 5 of a 4-terminal MOSFET phase-splitter amplifier in Fig. 5.7 using Eq. (5.32) is expressed as ;

$$R_{out} = R_{25} = \frac{\left|Y_{25}^{25}\right|}{\left|Y_5^5\right|_{G_L=0}} \tag{5.82}$$

$$\left|Y_5^5\right|_{G_{L1}=0} = g_b(\cancel{g_s} + G_G)(G_D + \cancel{G_{L1}})(G_S + g_m) = g_b G_G G_D(G_S + g_m)$$

$$\left|Y_5^5\right|_{G_S=0} = g_b(g_s + G_G)(G_D + G_{L1})(\cancel{G_S} + g_m) = g_b(g_s + G_G)(G_D + G_{L1})g_m$$

$$\left|Y_5^5\right|_{G_S\neq 0} = g_b(g_s + G_G)(G_D + G_{L1})(G_S + g_m)$$

$$\left|Y_{25}^{25}\right| = \begin{vmatrix} g_s + G_G & 0 & 0 \\ -g_m & g_m + g_o + g_{mb} + g_b + G_S & -g_{mb} - g_b \\ 0 & -g_b & g_b \end{vmatrix}$$

$$= \begin{vmatrix} g_s + G_G & 0 & 0 \\ -g_m & g_m + g_o + G_S & -g_{mb} - g_b \\ 0 & 0 & g_b \end{vmatrix}$$

$$= (g_s + G_G)(g_m + g_o + G_S)g_b$$

$$R_{out} = R_{25} = \frac{\left|Y_{25}^{25}\right|}{\left|Y_5^5\right|_{G_{L1}=0}} = \frac{g_b(g_s+G_G)(g_m+g_o+G_S)}{g_b(g_s+G_G)G_D(G_S+g_m)} = \frac{(g_m+g_o+G_S)}{(G_S+g_m)} R_D$$

$$= \left\{1 + \frac{g_o R_S}{1+g_m R_S}\right\} R_D. \tag{5.83}$$

$$R_{out} = R_{25}\frac{\left|Y_{25}^{25}\right|}{\left|Y_5^5\right|_{G_L\neq 0}} = \frac{(g_m+g_o+G_S)}{G_L(G_S+g_m)} = \frac{g_m+G_S}{G_L(G_S+g_m)} + \frac{g_o}{G_L(G_S+g_m)}$$

$$= R_L + R_L\frac{g_o R_S}{1+g_m R_S} = R_L\left(1 + \frac{g_o R_S}{1+g_m R_S}\right) \tag{5.84}$$

The output resistance [23-26] between the output terminals 3 & 5 of a 4-terminal MOSFET phase-splitter amplifier in Fig. 5.7 using Eq. (5.32) is expressed as ;

$$R_{out} = R_{35} = \frac{\left|Y_{35}^{35}\right|}{\left|Y_1^1\right|_{G_S=0}} \tag{5.85}$$

$$\left|Y_{35}^{35}\right| = \begin{vmatrix} g_s + G_G & 0 & 0 \\ -g_m & g_o + G_L & -g_{mb} - g_b \\ 0 & 0 & g_b \end{vmatrix} = (g_s + G_G)(g_o + G_L)g_b$$

$$R_{out} = R_{35} = \frac{\left|Y_{35}^{35}\right|}{\left|Y_5^5\right|}_{G_S=0} = \frac{(g_s+G_G)(g_o+G_L)g_b}{g_b(g_s+G_G)G_L g_m} = \frac{(g_o+G_L)}{G_L g_m} \cong \frac{G_L}{G_L g_m} = \frac{1}{g_m} \qquad (5.86)$$

$$R_{out} = R_{35} = \frac{\left|Y_{35}^{35}\right|}{\left|Y_5^5\right|}_{G_S\neq 0} = \frac{(g_s + G_G)(g_o + G_L)g_b}{(g_s + G_G)(g_o + G_L)(G_S + g_m)g_b} = \frac{1}{(G_S + g_m)}$$

$$= R_S \parallel \frac{1}{g_m} = \frac{1}{g_m} \qquad (5.87)$$

The power gain [14], [17] between terminals 2 & 5 and 1 & 5 of a MOS phase-splitter amplifier circuit in Fig. 4 is written as ;

$$A_P|_{15}^{25} = A_v|_{15}^{25} x\ A_i|_{15}^{25} = \left(-\frac{g_m R_L}{1+g_m R_S}\right)\left(-\frac{g_m r_s}{1+g_m R_S}\right) \qquad (5.88)$$

The power gain [14], [17] between terminals 3 & 5 and 1 & 5 of a MOS phase-splitter amplifier circuit in Fig. 4 is written as ;

$$A_P|_{15}^{35} = A_v|_{15}^{35} x\ A_i|_{15}^{35} = \left(\frac{g_m R_S}{\{1+g_m R_S\}}\right)\left(\frac{g_m r_s}{1+g_m R_S}\right) \qquad (5.89)$$

The LTSpice simulation of a Voltage-dependent capacitor was presented by Zeltsern and Yaakov[22]. The exhaustive discussion on the Design and comparative analysis of active-loaded differential amplifiers using double-gate MOSFET goes to the credit of Pillay and Srivastava [23].

5.9 Conclusions

The technique proposed is straightforward and purely mathematical. Once the MOSFET parameters are known, even a pure mathematician with the knowledge of matrix manuevouring has little understanding of device operations and can easily obtain all transfer and self-port functions. Additionally, its zero-sum property provides a check at the beginning of writing the FAM of any complicated or straightforward network. This property states that the sum of all elements in any row or in any column should be zero. If not, then some mistakes must have been made somewhere in writing the FAM. In such circumstances, the researchers have to reobserve once again before proceeding further. This provides a clue to saving time and energy. Thus, the analysis and design become easy using the FAM approach. Matrix partitioning method helps to write FAM of complicated circuits as several sub-matrices and then added together, node wise, is

a handy tool. Composite circuits containing both types of devices (BJT and MOS) still further increase the complexity and complicate the problem in arriving at simple solutions using the conventional methods.

On the contrary, the circuit analysis can be done easily using FAM. Some approximations are inherent in the conventional analysis method (complicated small-signal equivalent circuit), but FAM approach does not require any approximation, and the result will be accurate. The solution of lattice network, bridge-T, Twin-T etc., are very cumbersome using the conventional methods and may be solved easily with proposed FAM technique.

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Chapter-6

Conclusions

The conventional method of analysis of any circuit containing the active device(s) is based on the small-signal equivalent circuit of the active device and then use of either KCL, KVL, Thevenin's, or Norton's theorem. The researchers have to decide which conventional tool (either KCL, KVL, Thevenin's, or Norton's theorem) is most suitable for a particular problem to get the solution easily. On the contrary, the proposed technique is unique and can be applied to a simple or to even a complicated circuits using portioning property of the matrix, equally well, to get the solution easily.

We are now more than two decades into the 21st century, and on an ever-accelerating fast track to technological innovation in electronics. The transistors and its progression into the IC, or microchip, lit the fuse leading to the explosion of innovations in electronics that is now taking place. Since the widespread introduction of the microchip in the early 1970s, more medical, mathematical, and scientific breakthroughs have occurred than during any other time, and big breakthroughs are happening more frequently.

In this context, all academicians and professionals are trying hard to simplify and achieve better and better results from any system we think of. Our aim to simplification of the analog circuit combining BJT, FET, MOSFET, and their combinations along with resisters and capacitors lies in using properties of the Floating Admittance Matrix (FAM) technique. The floating admittance matrix approach of the solution of any circuit has the following special features:

1. The zero-sum property provides a self-check of the proposed technique in the very beginning after writing the floating admittance matrix (FAM) of any simple or complicated circuit. This property states that the sum of all elements in any row or in any column should be zero. If, not, then some mistakes must

have been made somewhere in writing the FAM. In such circumstances, the researcher has to observe once again the FAM before proceeding further. This provides a clue to save the time and energy. Hence the analysis and design becomes easy using FAM Approach.

2. The FAM technique of solution of any circuit takes the help of matrix manoeuvring in the form of ratios of co-factors of the FAM only.
3. Matrix partitioning method help to write FAM of complicated circuits in number of sub matrices and then added together node wise, is a handy tool.
4. Cascaded and cascoded circuits with even only one type of the active devices poses too much of problem for finding out different types of transfer or self-port functions of any circuit. Precisely, if we introduce a resistance in-between cascode connection, the solution by conventional method is very cumbersome, if not impossible.
5. Composite circuits containing both types of devices (BJT and FET/MOSFET) still further increases the complexity and complicates the problem in arriving at the solutions. On the contrary, it can be analysed easily using FAM, in the form of sub-matrices.
6. Solving even resistive network having more than two loops becomes tedious task by the conventional tools. As an example, the solution of the bridge T-network or twin-T runs into pages by conventional methods of KCL, KVL, Thevenin's, Norton's theorems.
7. Solving Twin-T Network is very good example of rejecting precisely only one frequency and passing all other frequencies. Its analysis by the conventional method is very difficult, but solved easily using FAM.
8. Similarly, getting the solution of Lattice Network by conventional tool is very cumbersome, but solved easily with FAM technique.
9. Derivation of all types of transfer and self-port functions; such input impedance, output impedance, voltage gain, current gain, power gain by conventional method for even in pure resistive complicated network becomes very lengthy and cumbersome.

10. Some approximation is inherent to the conventional method of analysis, but FAM approach does not require any approximation and results will be more accurate.
11. Mathematical model of any device provides an insight into the complete behaviour of the physical system that reduces the problem to its essential characteristic.
12. Deduction of the value of all the component in the Bridged T-Attenuator in terms of propagation constant and characteristic impedance is very problematic using conventional method, but becomes very simple using FAM technique.
13. The FAM is the only method suitable for non-electrical people with a back ground of matrix, if interested in solving any electrical and electronic circuit, because it is based on only maneuvering of the matrix in the form of cofactors of the FAM only.
14. Once, the FAM of any network is written, it is easy to find out transfer or self-port functions between as many ports as possible.

The technique proposed is straightforward and purely mathematical. Once the BJT/ FET/ MOSFET floating admittance matrix is known, even a pure mathematician with the knowledge of matix maneuvering having little understanding of device operations can also easily obtain all transfer functions and self-port functions. Concluding with the above advantages, the proposed technique provides a clue to the time and energy management. Thus, the analysis and design become easy using FAM approach.

On the contrary, the circuit analysis can be done easily using FAM. Some approximations are inherent in the conventional analysis method (for complicated small-signal equivalent circuit), but FAM approach does not require any approximation, and the result will be accurate. The solution of lattice network, bridge-T, Twin-T etc., are very cumbersome using the conventional methods and may be solved easily with the proposed FAM technique.

If the body of the 4-terminal MOSFET is not connected to the source terminal, a voltage occurs between the body and the source terminal that effects the threshold voltage of the MOSFET and the normal functioning of the MOSFET. The small-signal

model development of the 4-terminal MOSFET gets affected and hence the floating admittance matrix includes the body effect also.

On the other hand, if the source terminal of all the 4-termina MOSFETs in an integrated circuit are connected to only Body (substrate), then the circuit becomes useless. Hence, the body terminal is dealt as a separate terminal and given the name of *back-gate*. Thus all the four terminals of a MOSFET play active role in functioning of the MOSFET.

As stated previously, mathematical modelling is a powerful tool in engineering education that enables its users to minimize time and cost in the design process. Also, mathematical modelling usage facilitates the process of redesigning or concurrent engineering, a relatively new addition to engineering field.

The simulation and Validation of the common emitter amplifier on LTSpice plateform closely corroborates the theoretical results obtained using FAM technique. Also the simulation and validation of three complecated circuit presented in our published paper, indicated on Sr No.-3, 4 and 7 in Anexxure 2 validates theoretically predicted results.

Future Scope of Work

The straight forward answer to the scope is any researcher can prepare a program (s) to maneuver the FAM in the form of ratios of its cofactors to obtain any transfer or self-port function. There are many circuits using many single type of devices i.e. only BJTs or only MSFETs or even the composite of these two types of devices to obtain the solution easily using the FAM technique applying matrix portioning technique. Since, the proposed technique is based on the matrix, the computer or MAT Lab program can very well be used. The wide scope for researchers remain unsolved for the non-linear circuit using piece wise linear model.

Annexure-2

Complete Papers Published List in pdf Formates as downloaded from Publishers source and Indexed in Scopus.

Paper No1-Mathematical modelling of semiconductor devices and circuits-A review

ICICS2020.pdf

Paper No2- Mathematical Modelling of Simple Passive RC Filters Using Floating Admittance Technique.

INOCON2020.pdf

Paper No3- Mathematical Modelling and Simulation of Band Pass Filters using the Floating Admittance Matrix Method.

WSEASTR.pdf

Paper No4- Unique Analysis Approach to Bridge-T Network using Floating Admittance Matrix Method.

IJCSSPBridge-T.pdf

Paper No5- Unique Analysis Technique for 4-Terminal MOSFET Amplifiers using Floating Admittance Matrix Approach.

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Paper No6-An Elegant Method of Analysis for the BJT Amplifiers using Floating Admittance Matrix.

BJTFAM.pdf

Paper No7- Mathematical Modeling of Twin -T Notch Filter using Floating Admittance Matrix.

IJCSSPTwin-T.pdf

Annexure-3

Comperision of Solutions with Convensional and Floating Admittance Method(FAM)

8.8 Darlington configuration (Conventional Method)

We have seen that the input resistance of the emitter follower and BJT phase splitter is high. Still higher input resistance can be achieved using the Darlington pair. This is a very popular interconnection of 2-Bipolar Junction Transistors as a single unit, illustrated in Fig.8.8 (a), is commercially available in the market by the name of Darlington pair. Its main feature is that the 2-BJT works as a single transistor with its current amplification ratio as the product of the current amplification ratios of the 2-independent BJTs. In other words, if β_1 and β_2 are current amplification ratios of the two BJTs (T1 and T2), then the overall current amplification ratio in the form of Darlington connection is;

$$\beta_D = \beta_1\beta_2 \tag{8.99}$$

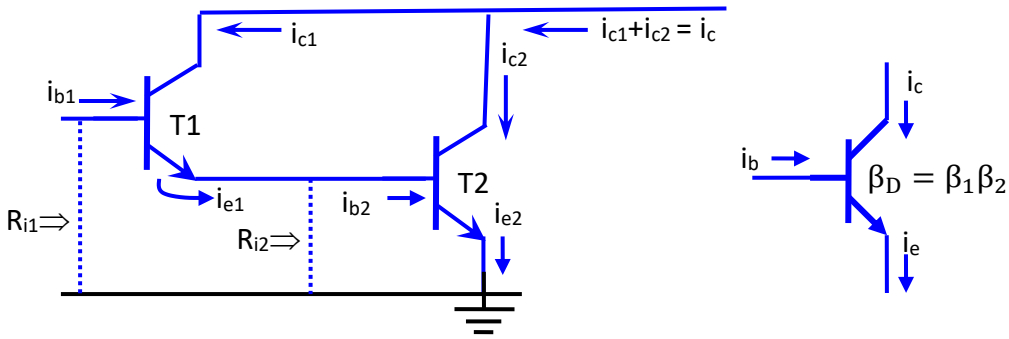

Figure 8.8 (a) Darlington Pair

From Fig.8.8 (a) it is clear that

$$i_{c2} = \beta_2 i_{b2}$$

$$i_{e1} = (1+\beta_1) i_{b1} = i_{b2}$$

$$i_c = i_{c1} + i_{c2} = \beta_1 i_{b1} + \beta_2 i_{b2} = \beta_1 i_{b1} + \beta_2(1+\beta_1) i_{b1}$$

$$= \{\beta_1 + \beta_2(1+\beta_1)\} i_{b1} \tag{8.100}$$

Hence, the overall current amplification ratio is $= \frac{i_c}{i_{b1}} = \frac{\{\beta_1+\beta_2(1+\beta_1)\} i_{b1}}{i_{b1}}$

$$= \beta_1 + \beta_2(1+\beta_1) \tag{8.101}$$

$$r_{\pi 1} = \frac{V_T}{I_{B1}} = \frac{V_T}{I_{E1}/(1+\beta_1)} = \frac{V_T(1+\beta_1)}{I_{E1}} = \frac{V_T}{I_{B2}}(1+\beta_1) = (1+\beta_1) r_{\pi 2}$$

$$r_{\pi 2} = \frac{V_T}{I_{E1}} = \frac{V_T}{(1+\beta_1) I_{B1}} = \frac{V_T/I_{B1}}{(1+\beta_1)} = \frac{r_{\pi 1}}{(1+\beta_1)}$$

Following are the two equivalent circuits in terms of input currents of both transistors. A simple circuit of Darlington amplifier is shown Fig. 8.8 (b). The emitter current of

transistor T1 is equal to the base current of the transistor T2. The ac circuit of the Darlington configuration is shown in Fig. 8.8(c). From the ac circuit of Darlington pair shown in Fig. 8.8 (d), its small signal equivalent circuit looks like the one drawn in Fig. 8.8 (e).

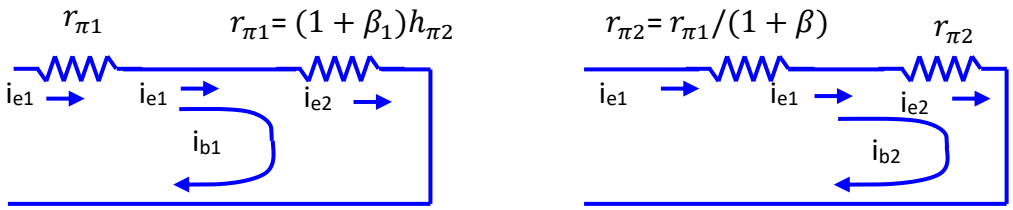

Figure 8.8 (b) Input resistance of Darlington pair

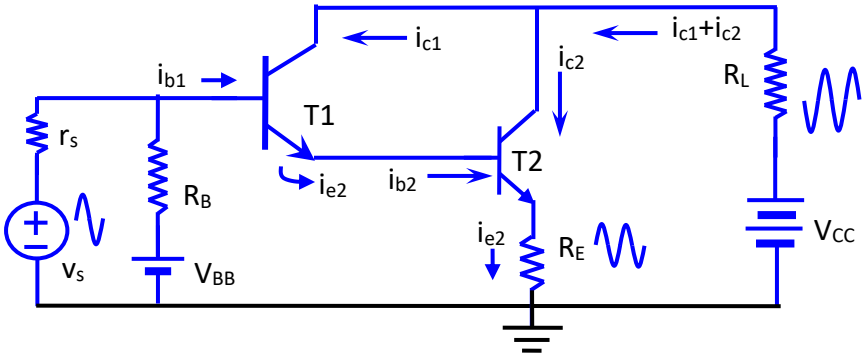

Figure 8.8 (c) Darlington pair amplifier

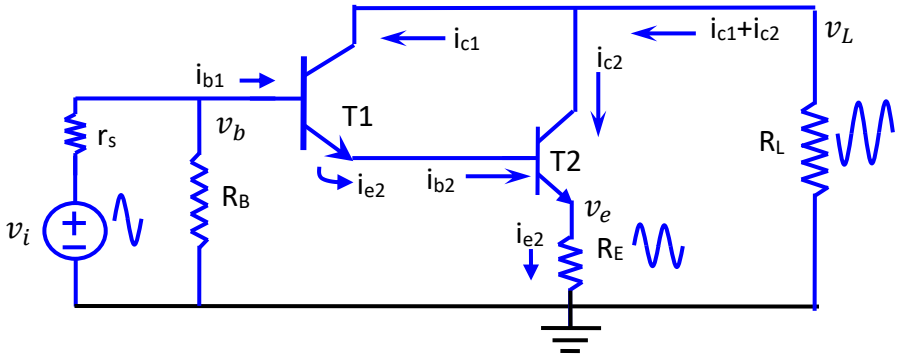

Figure 8.8 (d) ac circuit of Darlington pair amplifier

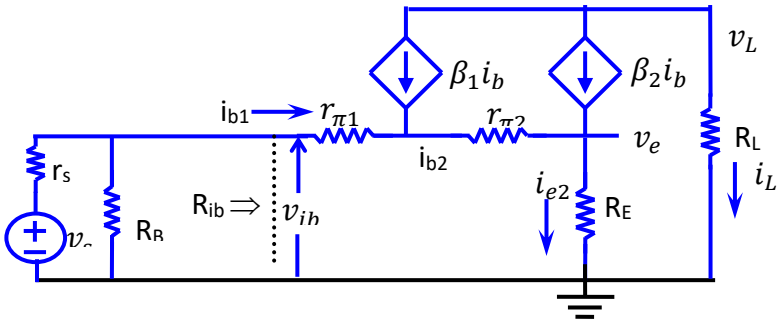

Figure 8.8 (e) Equivalent circuit of Darlington pair amplifier

From Fig.8.8 (e), $i_{b2} = i_{e1} = (1 + \beta_1) i_{b1}$ (8.102)

Writing loop equation in the input circuit

$$\begin{aligned} v_i &= r_{\pi 1} i_{b1} + \{r_{\pi 2} + (1 + \beta_2) R_E\} i_{b2} \\ &= r_{\pi 1} i_{b1} + \{r_{\pi 2} + (1 + \beta_2) R_E\} i_{e1} \\ &= r_{\pi 1} i_{b1} + \{r_{\pi 2} + (1 + \beta_2) R_E\}(1 + \beta_1) i_{b1} \\ &= [r_{\pi 1} + \{r_{\pi 2} + (1 + \beta_2) R_E\}(1 + \beta_1)] i_{b1} \end{aligned} \quad (8.103)$$

Hence, its input resistance $R_{ib} = \frac{v_i}{i_{b1}} = r_{\pi 1} + \{r_{\pi 2} + (1 + \beta_2) R_E\}(1 + \beta_1)$ (8.104)

$$R_{ib} = [r_{e1} + \{r_{\pi 2} + (1 + \beta_2) R_E\}](1 + \beta_1) \quad (8.105)$$

The effective input resistance of the amplifier including the bias resistor R_B is

$$R_{i(eff)} = R_B \parallel R_{ib} \quad 8.106)$$

The upper limit on the value of effective input resistance is limited to the value of R_B. Hence, the Darlington configuration could not help much in enhancing the effective input resistance of the Darlington amplifier. As an example, the circuit of Fig.8.8 (e) reduces to Fig.8.8 (f). The effective input resistance including the bias resistance is;

$$R_{is} = R_i \parallel R_{BB} = 10\ k\Omega \| 10^4\ k\Omega = 10\ k\Omega \quad (8.106)$$

The Darlington configuration is used as the emitter follower, the voltage is supposed to be unity (ideally), but very near to unity in practical cases.

From Fig. 8.8 (e), the voltage developed across the emitter resistance R_E is given as;

$$\begin{aligned} v_{e2} &= i_{e2} R_E = (1 + \beta_2) i_{b2} R_E \\ &= (1 + \beta_2) R_E i_{e1} \\ &= (1 + \beta_2)(1 + \beta_1) R_E i_{b1} \end{aligned} \quad (8.107)$$

$$v_{ib} = R_i i_{b1} = [r_{\pi 1} i_{b1} + (1 + \beta_1) i_{b1} r_{\pi 2} + (1 + \beta_2)(1 + \beta_1) R_E i_{b1}]$$

$$v_{ib} = R_i i_{b1} = [r_{\pi 1} + \{r_{\pi 2} + (1 + \beta_2) R_E\}(1 + \beta_1)] i_{b1} \quad (8.108)$$

The voltage gain between the emitter point and the input (base point) is the ratio of the voltage v_{e2} and v_{ib} and is given as;

$$\frac{v_{e2}}{v_{ib}} = \frac{(1+\beta_2)(1+\beta_1) R_E i_{b1}}{[r_{\pi 1} + \{r_{\pi 2} + (1+\beta_2) R_E\}(1+\beta_1)] i_{b1}} = \frac{(1+\beta_2)(1+\beta_1) R_E}{r_{\pi 1} + \{r_{\pi 2} + (1+\beta_2) R_E\}(1+\beta_1)} \quad (8.109)$$

From Fig. 8.8 (f) $i_s = \frac{v_s}{r_s + R_B \| R_{ib}}$

$$v_{ib} = (R_B \parallel R_{ib}) i_s = (R_B \parallel R_{ib}) \frac{v_s}{r_s + R_B \| R_{ib}}$$

$$v_{ib} = (R_B \parallel R_{ib}) i_s = (R_B \parallel R_{ib}) \frac{v_s}{r_s + R_B \| R_{ib}}$$

$$= \left(\frac{R_B R_{ib}}{R_B + R_{ib}}\right) \frac{v_s}{r_s + \frac{R_B R_{ib}}{R_B + R_{ib}}} = v_s \frac{R_B R_{ib}}{r_s(R_B + R_{ib}) + R_B R_{ib}} \tag{8.110}$$

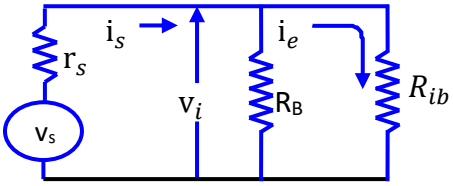

Figure 8.8 (f) Simplified equivalent circuit of Darlington pair amplifier

$$A_v = \frac{v_{ib}}{v_s} = \frac{R_B R_{ib}}{r_s(R_B + R_{ib}) + R_B R_{ib}}$$

Now, the overall voltage gain including the source resistance can be expressed as;

$$A_{vs} = \frac{v_{e2}}{v_{ib}} x \frac{v_{ib}}{v_s} = \frac{v_{e2}}{v_s} = \frac{v_0}{v_s}$$

$$A_{vse} = \frac{v_{e2}=v_o}{v_s} = \left\{\frac{(1+\beta_2)(1+\beta_1)R_E}{r_{\pi 1} + \{r_{\pi 2} + (1+\beta_2)R_E\}(1+\beta_1)}\right\}\left\{\frac{R_{ib}R_B}{r_s(R_{ib}+R_B)+R_{ib}R_B}\right\} \tag{8.111}$$

The output resistance is defined as;

$$R_O = \frac{v_e}{i_o}\Big|_{v_S=0} \tag{8.112}$$

Thus, for obtaining the output resistance, the circuit of Fig.8.8 (e) now reduces to Fig.8.8 (g).

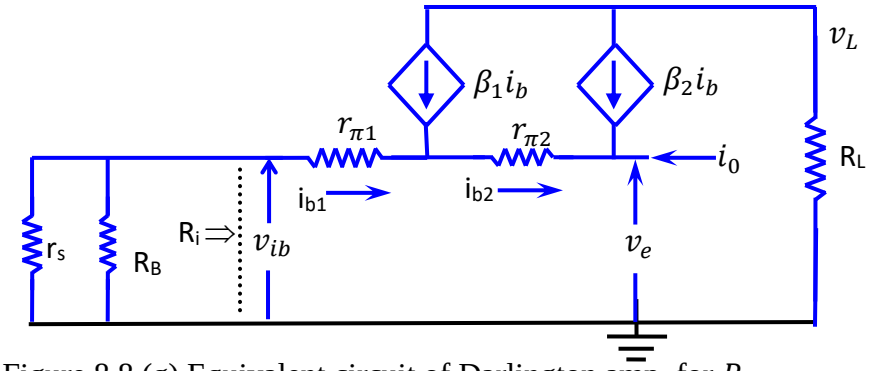

Figure 8.8 (g) Equivalent circuit of Darlington amp. for R_O

From Fig. 8.8 (g),

$$V_e = -r_{\pi 2} i_{b2} - r_{\pi 1} i_{b1} - (r_s \parallel R_{BB}) i_{b1}$$

$$= -r_{\pi 2} i_{b2} - \{r_{\pi 1} + (r_s \parallel R_{BB})\} i_{b1}$$

$$= -r_{\pi 2} i_{b2} - \{r_{\pi 1} + (r_s \parallel R_{BB})\} \frac{i_{e1}}{1+\beta_1}$$

$$= -r_{\pi 2} i_{b2} - \{r_{\pi 1} + (r_s \parallel R_{BB})\} \frac{i_{b2}}{1+\beta_1}$$

$$= -r_{\pi 2} i_{b2} - \frac{\{r_{\pi 1} + (r_s \parallel R_{BB})\}}{1+\beta_1} i_{b2}$$

$$v_e = -\left[r_{\pi 2} i_{b2} - \frac{\{r_{\pi 1} + r_s \| R_{BB}\}}{1+\beta_1}\right] i_{b2} \quad (8.113)$$

$$i_o = -(1+\beta_2) i_{b2},$$

$$i_{b2} = -\frac{i_o}{(1+\beta_2)} \quad (8.114)$$

$$i_{b2} = i_{e1} = -(1+\beta_1) i_{b1} \quad (8.115)$$

Substituting i_{b2} in Eq. (8.113) from Eq, (8.114) yields;

$$v_e = v_O = -\left[r_{\pi 2} i_{b2} + \frac{\{r_{\pi 1} + r_s \| R_{BB}\}}{1+\beta_1}\right]\left(-\frac{i_o}{(1+\beta_2)}\right)$$

$$R_O = \frac{v_O}{i_O} = \frac{r_{\pi 2}}{1+\beta_2} + \frac{r_{\pi 1} + r_s \| R_{BB}}{(1+\beta_1)(1+\beta_2)} \text{ (Very low)} \quad (8.116)$$

The voltage gain between collector and base points is now obtained as;

$$v_c = v_L = -(\beta_1 i_{b1} + \beta_2 i_{b2}) R_L = -(\beta_1 i_{b1} + \beta_2 i_{e1}) R_L$$
$$= -(\beta_1 i_{b1} + \beta_2(\beta_1 + 1) i_{b1}) R_L$$
$$= -\{\beta_1 + (1+\beta_1)\beta_2\} R_L i_{b1} \quad (8.117)$$

$$\frac{v_c = v_L}{v_{ib}} = -\frac{-\{\beta_1 + (1+\beta_1)\beta_2\} R_L i_{b1}}{[r_{\pi 1} + \{r_{\pi 2} + (1+\beta_2) R_E\}(1+\beta_1)] i_{b1}}$$

$$= -\frac{\{\beta_1 + (1+\beta_1)\beta_2\} R_L}{r_{\pi 1} + \{r_{\pi 2} + (1+\beta_2) R_E\}(1+\beta_1)} \quad (8.118)$$

$$A_{vsL} = \frac{V_L}{v_{ib}} x \frac{v_{ib}}{v_s} = \frac{v_L}{v_s} = -\frac{-\{\beta_1 + (1+\beta_1)\beta_2\} R_L}{[r_{\pi 1} + \{r_{\pi 2} + (1+\beta_2) R_E\}(1+\beta_1)]} \left\{\frac{R_{ib} R_B}{r_s(R_{ib} + R_B) + R_{ib} R_B}\right\}$$

$$A_{vsL} = -\frac{-\{\beta_1 + (1+\beta_1)\beta_2\} R_L}{[r_{\pi 1} + \{r_{\pi 2} + (1+\beta_2) R_E\}(1+\beta_1)]} \left\{\frac{R_{ib} R_B}{r_s(R_{ib} + R_B) + R_{ib} R_B}\right\} \quad (8.119)$$

Darlington Configuration(FAM Method)

Analysis using floating admittance matrix technique. The circuit of the Darlington configuration is shown in Fig. 1*(a)*. The ac circuit of the Darlington configuration is shown in Fig. 1*(b)*.

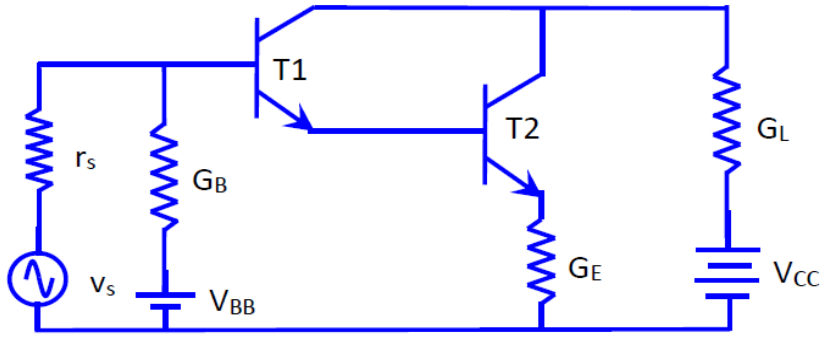

Fig. 1*(a)* Darlington Configuration

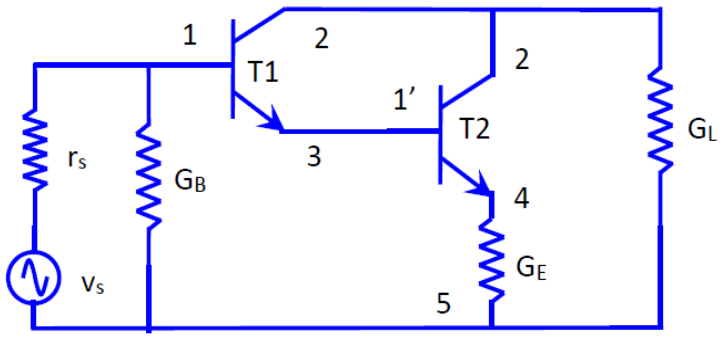

Fig. 1*(b)* Darlington Configuration

The partitioned floating admittance matrix of transistors T1 in Fig. 1(b) is written as;

$$\begin{bmatrix} 1 & 2 & 3 \\ g_{\pi 1} & 0 & -g_{\pi 1} \\ g_{m1} & 0 & -g_{m1} \\ -g_{\pi 1}-g_{m1} & 0 & g_{\pi 1}+g_{m1} \end{bmatrix} \begin{matrix} 1 \\ 2 \\ 3 \end{matrix} \quad (1)$$

Similarly, the partition floating admittance matrix of transistors T2 in Fig. 1(b) is written as;

$$\begin{bmatrix} 3 & 2 & 4 \\ g_{\pi 2} & 0 & -g_{\pi 2} \\ g_{m2} & 0 & -g_{m2} \\ -g_{\pi 2}-g_{m2} & 0 & g_{\pi 2}+g_{m2} \end{bmatrix} \begin{bmatrix} 3 \\ 2 \\ 4 \end{bmatrix} \quad (2)$$

Also, the partition floating admittance matrix of resistors R_B, R_E, and R_L in Fig. 1(b) is written as;

$$\begin{bmatrix} 1 & 2 & 3 & 4 & 5 \\ g_s+G_B & 0 & 0 & 0 & -g_s-G_B \\ 0 & G_L & 0 & 0 & -G_L \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & G_E & -G_E \\ -g_s-G_B & -G_L & 0 & -G_E & g_s+G_B+G_E+G_L \end{bmatrix} \begin{matrix} 1 \\ 2 \\ 3 \\ 4 \\ 5 \end{matrix} \quad (3)$$

The three partition matrices of Eqs. (1), (2), and (3) are combined to form the overall matrix of Fig. 1 (b) as;

$$\begin{bmatrix} 1 & 2 & 3 & 4 & 5 \\ g_{\pi 1}+g_s+G_B & 0 & -g_{\pi 1} & 0 & -g_s-G_B \\ g_{m1} & G_L & -g_{m1}+g_{m2} & -g_{m2} & -G_L \\ -g_{\pi 1}-g_{m1} & 0 & g_{\pi 1}+g_{m1}+g_{\pi 2} & -g_{\pi 2} & 0 \\ 0 & 0 & -g_{\pi 2}-g_{m2} & g_{\pi 2}+g_{m2}+G_E & -G_E \\ -g_s-G_B & -G_L & 0 & -G_E & g_s+G_B+G_E+G_L \end{bmatrix} \begin{matrix} 1 \\ 2 \\ 3 \\ 4 \\ 5 \end{matrix} \quad (4)$$

$$\left|Y_{25}^{15}\right| = \begin{vmatrix} g_{m1} & -g_{m1}+g_{m2} & -g_{m2} \\ -g_{\pi 1}-g_{m1} & g_{\pi 1}+g_{m1}+g_{\pi 2} & -g_{\pi 2} \\ 0 & -g_{\pi 2}-g_{m2} & g_{\pi 2}+g_{m2}+G_E \end{vmatrix}$$

$$= \begin{vmatrix} g_{m1} & -g_{m1}+g_{m2} & 0 \\ -g_{\pi1}-g_{m1} & g_{\pi1}+g_{m1}+g_{\pi2} & 0 \\ 0 & -g_{\pi2}-g_{m2} & G_E \end{vmatrix}$$

$$= \begin{vmatrix} g_{m1} & g_{m2} & 0 \\ -g_{\pi1}-g_{m1} & g_{\pi2} & 0 \\ 0 & -g_{\pi2}-g_{m2} & G_E \end{vmatrix}$$

$$= G_E\{g_{m1}g_{\pi2} + (g_{\pi1}+g_{m1})g_{m2}\} = G_E\{g_{m1}g_{\pi2} + g_{\pi1}(1+\beta_1)g_{m2}\}$$

$$= g_{\pi1}g_{\pi2}\{g_{m1}r_{\pi1} + r_{\pi2}(1+\beta_1)g_{m2}\} = g_{\pi1}g_{\pi2}\{\beta_1 + \beta_2(1+\beta_1)\}$$

$$A_v|_{15}^{25} = sgn(2-5)sgn(1-5)(-1)^{13}\frac{|Y_{25}^{15}|}{|Y_{15}^{15}|} = -\frac{|Y_{25}^{15}|}{|Y_{15}^{15}|} \quad (5)$$

$$A_v|_{15}^{25} = -\frac{|Y_{25}^{15}|}{|Y_{15}^{15}|} = -\frac{g_{\pi1}g_{\pi2}\{\beta_1+\beta_2(1+\beta_1)\}G_E}{G_L g_{\pi1}g_{\pi2}[(1+\beta_1)\{r_{\pi2}+(1+\beta_2)R_E\}+r_{\pi1}]G_E}$$

$$= -\frac{\{\beta_1+\beta_2(1+\beta_1)\}R_L}{[r_{\pi1}+(1+\beta_1)\{r_{\pi2}+(1+\beta_2)R_E\}]} \quad (6)$$

The input resistance between terminals 1 and 5 of the Darlington pair amplifier in Fig. 1 (b) is expressed as;

$$R_{in} = R_{i(15)} = \frac{|Y_{15}^{15}|}{|Y_5^5|}_{g_s=0} \quad (7)$$

$$|Y_{15}^{15}| = \begin{vmatrix} G_L & -g_{m1}+g_{m2} & -g_{m2} \\ 0 & g_{\pi1}+g_{m1}+g_{\pi2} & -g_{\pi2} \\ 0 & -g_{\pi2}-g_{m2} & g_{\pi2}+g_{m2}+G_E \end{vmatrix} =$$

$$\begin{vmatrix} G_L & -g_{m1} & -g_{m2} \\ 0 & g_{\pi1}+g_{m1} & -g_{\pi2} \\ 0 & G_E & g_{\pi2}+g_{m2}+G_E \end{vmatrix}$$

$$= G_L\{(g_{\pi1}+g_{m1})(g_{\pi2}+g_{m2}) + (g_{\pi1}+g_{m1})G_E + g_{\pi2}G_E\}$$

$$= G_L g_{\pi1}g_{\pi2}[(1+\beta_1)\{r_{\pi2}+(1+\beta_2)R_E\}+r_{\pi1}]G_E$$

$$|Y_5^5|_{g_s+G_B=0} = \begin{vmatrix} g_{\pi1} & 0 & -g_{\pi1} & 0 \\ g_{m1} & G_L & -g_{m1}+g_{m2} & -g_{m2} \\ -g_{i1}-g_{m1} & 0 & g_{\pi1}+g_{m1}+g_{\pi2} & -g_{\pi2} \\ 0 & 0 & -g_{\pi2}-g_{m2} & g_{\pi2}+g_{m2}+G_E \end{vmatrix}$$

$$= \begin{vmatrix} g_{\pi1} & 0 & 0 & 0 \\ g_{m1} & G_L & 0 & -g_{m2} \\ -g_{\pi1}-g_{m1} & 0 & 0 & -g_{\pi2} \\ 0 & 0 & G_E & g_{\pi2}+g_{m2}+G_E \end{vmatrix} = g_{\pi1}g_{\pi2}G_L G_E$$

$$R_{in} = R_{i(15)} = \frac{G_L g_{\pi1}g_{\pi2}[(1+\beta_1)\{r_{\pi2}+(1+\beta_2)R_E\}+r_{\pi1}]G_E}{g_{\pi1}g_{\pi2}G_L G_E}$$

$$= r_{\pi1} + (1+\beta_1)\{r_{\pi2}+(1+\beta_2)R_E\} \quad (8)$$

The output resistance between terminals 2 and 5 of the Darlington pair amplifier in Fig. 1 (b) is expressed as;

$$R_{out} = R_{o(25)} = \frac{|Y_{25}^{25}|}{|Y_5^5|}_{G_L=0} \quad (9)$$

$$|Y_{25}^{25}| = \begin{vmatrix} g_{\pi1}+g_s+G_B & -g_{\pi1} & 0 \\ -g_{\pi1}-g_{m1} & g_{\pi1}+g_{m1}+g_{\pi2} & -g_{\pi2} \\ 0 & -g_{\pi2}-g_{m2} & g_{\pi2}+g_{m2}+G_E \end{vmatrix}$$

$$|Y_5^5|_{G_L=0} = \begin{vmatrix} g_{\pi1}+g_s+G_B & 0 & -g_{\pi1} & 0 \\ g_{m1} & \cancel{G_L} & -g_{m1}+g_{m2} & -g_{m2} \\ -g_{\pi1}-g_{m1} & 0 & g_{\pi1}+g_{m1}+g_{\pi2} & -g_{\pi2} \\ 0 & 0 & -g_{\pi2}-g_{m2} & g_{\pi2}+g_{m2}+G_E \end{vmatrix} = 0$$

$$R_{out} = R_{o(25)} = \frac{|Y_{45}^{45}|}{|Y_5^5|}_{G_L=0} = \frac{|Y_{45}^{45}|}{0} = \infty \quad (10)$$

$$R_{out} = R_{o(25)} = \frac{|Y_{45}^{45}|}{|Y_5^5|}_{G_L \neq 0} = \frac{1}{h_{oe}} \parallel R_C \cong R_C \quad (11)$$

Once again output impedance became infinite only because h_{oe} was neglected in the floating admittance matrix representation of BJTs, because its value is negligibly small. If it is considered, then the output resistance will be equal to $\frac{1}{h_{oe}}$.

The output resistance between terminals 4 and 5 of the Darlington pair amplifier in Fig. 1 (b) is expressed as;

$$R_{out} = R_{o(45)} = \frac{|Y_{45}^{45}|}{|Y_5^5|}_{G_E=0} \quad (12)$$

$$|Y_{45}^{45}| = \begin{vmatrix} g_{\pi1}+g_s+G_B & 0 & -g_{\pi1} \\ g_{m1} & G_L & -g_{m1}+g_{m2} \\ -g_{\pi1}-g_{m1} & 0 & g_{\pi1}+g_{m1}+g_{\pi2} \end{vmatrix}$$

$$= \begin{vmatrix} g_s+G_B & 0 & -g_{\pi1} \\ g_{m2} & G_L & -g_{m1}+g_{m2} \\ g_{\pi2} & 0 & g_{\pi1}+g_{m1}+g_{\pi2} \end{vmatrix}$$

$$= G_L\{(g_s+G_B)(g_{\pi1}+g_{m1}+g_{\pi2})+g_{\pi1}g_{\pi2}\}$$

$$= G_L\{(r_s+R_B)\{r_{\pi1}+(1+\beta_1)r_{\pi2}\}+r_sR_B1\}g_{\pi1}g_{\pi2}g_sG_B$$

$$|Y_5^5|_{G_E=0} = \begin{vmatrix} g_{\pi1}+g_s+G_B & 0 & -g_{\pi1} & 0 \\ g_{m1} & G_L & -g_{m1}+g_{m2} & -g_{m2} \\ -g_{\pi1}-g_{m1} & 0 & g_{\pi1}+g_{m1}+g_{\pi2} & -g_{\pi2} \\ 0 & 0 & -g_{\pi2}-g_{m2} & g_{\pi2}+g_{m2}+\cancel{G_E} \end{vmatrix}$$

$$= \begin{vmatrix} g_{\pi1}+g_s+G_B & 0 & g_s+G_B & 0 \\ g_{m1} & G_L & 0 & -g_{m2} \\ -g_{\pi1}-g_{m1} & 0 & 0 & -g_{\pi2} \\ 0 & 0 & 0 & g_{\pi2}+g_{m2} \end{vmatrix}$$

$$= G_L \begin{vmatrix} g_{\pi1}+g_s+G_B & g_s+G_B & 0 \\ -g_{\pi1}-g_{m1} & 0 & -g_{\pi2} \\ 0 & 0 & g_{\pi2}+g_{m2} \end{vmatrix},$$

$$= G_L\{(g_s+G_B)(g_{\pi2}+g_{m2})(g_{\pi1}+g_{m1})\}$$

$$= G_Lg_sG_B(r_s+R_B)g_{\pi1}(1+\beta_2)g_{\pi2}(1+\beta_1)$$

$$R_{out} = R_{o(45)} = \frac{G_L\{(r_s+R_B)\{r_{\pi1}+(1+\beta_1)r_{\pi2}\}+r_sR_B1\}g_{\pi1}g_{\pi2}g_sG_B}{G_Lg_sG_B(r_s+R_B)g_{\pi1}(1+\beta_2)g_{\pi2}(1+\beta_1)}$$

$$R_{out} = R_{o(45)} = \frac{r_{\pi1}}{(1+\beta_2)(1+\beta_1)} + \frac{(1+\beta_1)r_{\pi2}}{(1+\beta_2)(1+\beta_1)} + \frac{\frac{r_sR_B}{r_s+R_B}}{(1+\beta_2)(1+\beta_1)}$$

$$= \frac{r_{e1}}{(1+\beta_2)} + \frac{r_{\pi2}}{(1+\beta_2)} + \frac{r_s \parallel R_B}{(1+\beta_2)(1+\beta_2)} = \frac{r_{e1}}{(1+\beta_2)} + r_{e2} + \frac{r_s \parallel R_B}{(1+\beta_2)(1+\beta_2)} \quad (13)$$

The voltage gain between terminals 4 & 5 and 1 & 5 of a Darlington amplifier in Fig. 1 (b) is expressed as;

$$A_v|_{15}^{45} = sgn(4-5)sgn(1-5)(-1)^{15}\frac{|Y_{45}^{15}|}{|Y_{15}^{15}|} = -\frac{|Y_{45}^{15}|}{|Y_{15}^{15}|} \quad (14)$$

$$|Y_{45}^{15}| = \begin{vmatrix} g_{m1} & G_L & -g_{m1}-g_{m2} \\ -g_{\pi1}-g_{m1} & 0 & g_{\pi1}+g_{m1}+g_{\pi2} \\ 0 & 0 & -g_{\pi2}-g_{m2} \end{vmatrix} = -G_L(g_{\pi1}+g_{m1})(g_{\pi2}+g_{m2})$$
$$= -G_L g_{\pi1} g_{\pi2}(1+\beta_1)(1+\beta_2)$$

$$A_v|_{15}^{45} = -\frac{-G_L g_{\pi1} g_{\pi2}(1+\beta_1)(1+\beta_2)}{G_L g_{\pi1} g_{\pi2}[(1+\beta_1)\{r_{\pi2}+(1+\beta_2)R_E\}+r_{\pi1}]G_E}$$

$$= \frac{(1+\beta_1)(1+\beta_2)\,R_E}{r_{\pi1}+(1+\beta_1)\{r_{\pi2}+(1+\beta_2)R_E\}} \cong \frac{(1+\beta_1)(1+\beta_2)\,R_E}{(1+\beta_1)\{r_{\pi2}+(1+\beta_2)R_E\}} = \frac{(1+\beta_2)\,R_E}{r_{\pi2}+(1+\beta_2)R_E}$$

$$\cong \frac{(1+\beta_2)R_E}{(1+\beta_2)R_E} = 1 \text{ (Emitter follower)} \qquad (15)$$

The current gain between terminals 4 & 5 and 1 & 5 of a Darlington amplifier in Fig. 1 (b) is expressed as;

$$A_i|_{15}^{45} = sgn(4-5)sgn(1-5)(-1)^{15}\frac{|Y_{45}^{15}|}{|Y_5^5|}G_L = -\frac{|Y_{45}^{15}|}{|Y_5^5|}G_E \qquad (16)$$

$$|Y_5^5| = \begin{vmatrix} g_{\pi1} & 0 & -g_{\pi1} & 0 \\ g_{m1} & G_L & -g_{m1}+g_{m2} & -g_{m2} \\ -g_{\pi1}-g_{m1} & 0 & g_{\pi1}+g_{m1}+g_{\pi2} & -g_{\pi2} \\ 0 & 0 & -g_{\pi2}-g_{m2} & g_{\pi2}+g_{m2}+G_E \end{vmatrix}$$

$$= \begin{vmatrix} g_{\pi1} & 0 & 0 & 0 \\ g_{m1} & G_L & 0 & -g_{m2} \\ -g_{\pi1}-g_{m1} & 0 & 0 & -g_{\pi2} \\ 0 & 0 & G_E & g_{\pi2}+g_{m2}+G_E \end{vmatrix} = G_L G_E g_{\pi1} g_{\pi2}$$

$$\text{Current gain} = A_i|_{15}^{45} = -\frac{-G_L g_{\pi1} g_{\pi2}(1+\beta_1)(1+\beta_2)}{G_L G_E g_{\pi1} g_{\pi2}}G_E = (1+\beta_1)(1+\beta_2) \qquad (17)$$

11.14 FET-FET Cascode amplifier (Conventional)

Analysis using conventional method of small-signal equivalent circuit approach.

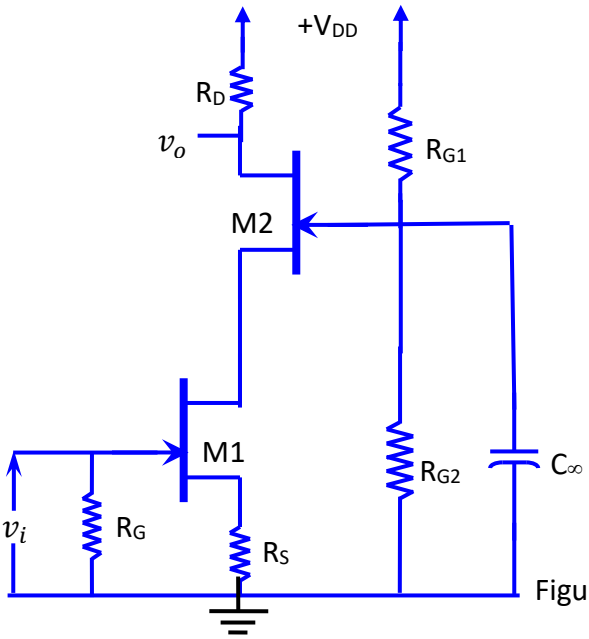

Figure 11.15 (a)

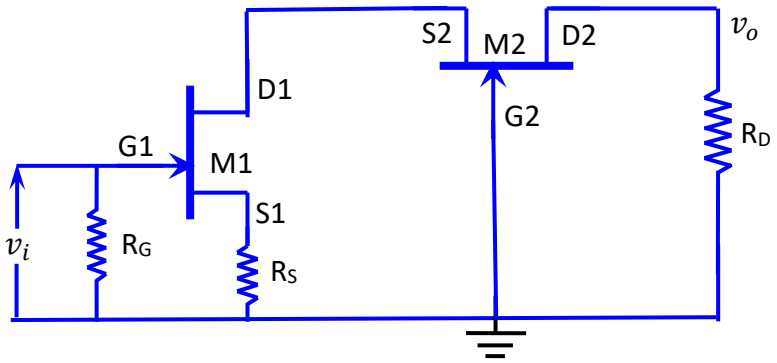

Figure 11.15 (b) ac circuit

The small signal equivalent circuit of the FET-FET cascode is drawn in Fig.

$$v_{gs1} = v_{g1} - v_{s1} = v_i - R_S i_d \tag{11.92}$$

$$v_{gs2} = v_{g2} - v_{s2} = 0 - v_{s2} = -(r_d + R_S)i_d + \mu v_{gs1}$$

$$= -(r_d + R_S)i_d + \mu v_i - \mu R_S i_d$$

$$= -\{r_d + (1+\mu)R_S\}i_d + \mu v_i \tag{11.93}$$

Writing loop equation in Fig. 11.15 (c) yields.

$$(2r_d + R_S + R_D)i_d = \mu v_{gs1} + \mu v_{gs2} \tag{11.94}$$

Substituting v_{gs1} and v_{gs2} from Eqs (11.92) and (11.93) in (11.94) yields;

$$(2r_d + R_S + R_D)i_d = \mu(v_i - i_d R_S) - \mu[\{r_d + (1+\mu)R_S\}i_d] + \mu^2 v_i$$

$$(2+\mu)r_d + (1+\mu)R_S + \mu(1+\mu)R_S + R_D)i_d = \mu v_i + \mu^2 v_i$$

$$(2+\mu)r_d + (1+\mu)^2 R_S + R_D)i_d = \mu v_i + \mu^2 v_i = \mu(1+\mu)v_i$$

$$\therefore i_d = \frac{\mu(1+\mu)v_i}{(2+\mu)r_d + (1+\mu)^2 R_S + R_D)} \tag{11.95}$$

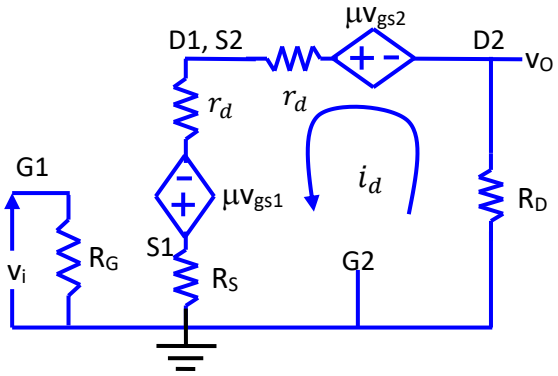

Figure 11.15 (c) Equivalent circuit

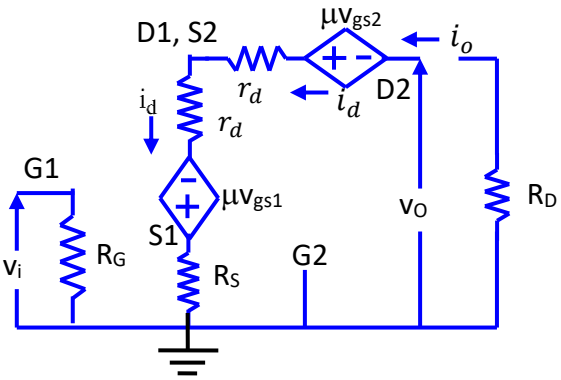

Figure 11.15 (d) Equivalent circuit for R_O

The output resistance and current gain are not derived in the example of the circuit.

FET-FET Cascode(FAM Method)

Analysis using floating admittance matrix technique.

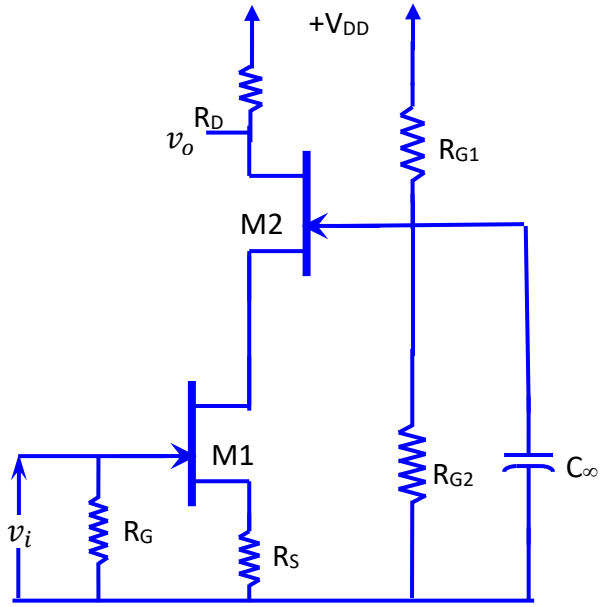

Figure 2(a) FET-FET Casecode

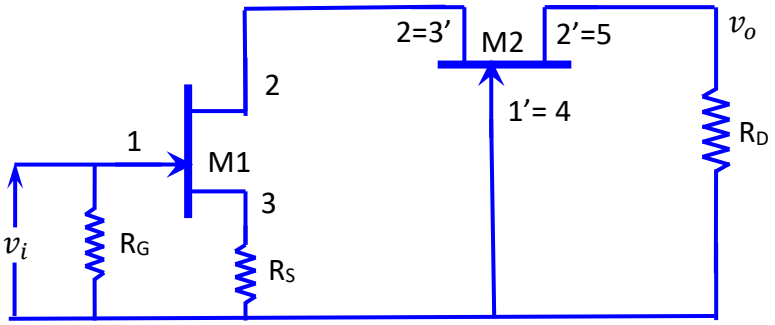

Figure 2(b)AC Circuit FET-FET Casecode

The partitioned floating admittance matrix of each active device M1 of Fig. 2 (b) is and M2 is expressed as;

$$\begin{bmatrix} i_1 = i_g \\ i_2 = i_d \\ i_3 = i_s \end{bmatrix} \begin{bmatrix} 1 & 2 & 3 \\ 0 & 0 & 0 \\ g_m & g_d & -g_m - g_d \\ -g_m & -g_d & g_m + g_d \end{bmatrix} \begin{bmatrix} v_1 = v_g \\ v_2 = v_d \\ v_3 = v_s \end{bmatrix} \begin{bmatrix} 1 \\ 2 \\ 3 \end{bmatrix} \quad (1)$$

The partitioned floating admittance matrix of each active device M2 of Fig. 2 (b) is

$$\begin{bmatrix} i_1 = i_g \\ i_3 = i_d \\ i_2 = i_s \end{bmatrix} \begin{bmatrix} 4 & 5 & 2 \\ 0 & 0 & 0 \\ g_m & g_d & -g_m - g_d \\ -g_m & -g_d & g_m + g_d \end{bmatrix} \begin{bmatrix} v_1 = v_g \\ v_3 = v_d \\ v_2 = v_s \end{bmatrix} \begin{bmatrix} 4 \\ 5 \\ 2 \end{bmatrix} \quad (2)$$

The partitioned floating admittance matrix of all passive resistors R_G, R_S, and R_D of Fig. 2 (b) is

$$\begin{bmatrix} 1 & 2 & 3 & 4 & 5 \\ G_G & 0 & 0 & -G_G & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & G_S & -G_S & 0 \\ -G_G & 0 & -G_S & G_G+G_S+G_D & -G_D \\ 0 & 0 & 0 & -G_D & G_D \end{bmatrix} \begin{bmatrix} 1 \\ 2 \\ 3 \\ 4 \\ 5 \end{bmatrix} \tag{3}$$

The overall floating admittance matrix of the 5x5 Darlington pair amplifier in Fig. 2(b) is;

$$\begin{bmatrix} 1 & 2 & 3 & 4 & 5 \\ G_G & 0 & 0 & -G_G & 0 \\ g_m & 2g_d+g_m & -g_m-g_d & -g_m & -g_d \\ -g_m & -g_d & g_m+g_d+G_S & -G_S & 0 \\ -G_G & 0 & -G_S & G_G+G_S+G_D & -G_D \\ 0 & -g_m-g_d & 0 & g_m-G_D & g_d+G_D \end{bmatrix} \begin{bmatrix} 1 \\ 2 \\ 3 \\ 4 \\ 5 \end{bmatrix} \tag{4}$$

$$|Y_{24}^{24}| = \begin{vmatrix} G_G & 0 & 0 \\ -g_m & g_m+g_d+G_S & 0 \\ 0 & 0 & g_d+G_D \end{vmatrix} = G_G(g_m+g_d+G_S)(g_d+G_D)$$

$$= G_G(\mu R_S + r_d + R_S)g_d G_S(r_d+R_D)g_d G_D$$

$$= G_G\{r_d+(1+\mu)R_S\}g_d G_S(r_d+R_D)g_d G_D$$

$$|Y_{54}^{54}| = \begin{vmatrix} G_G & 0 & 0 \\ g_m & 2g_d+g_m & -g_m-g_d \\ -g_m & -g_d & g_m+g_d+G_S \end{vmatrix} = G_G \begin{vmatrix} 2g_d+g_m & -g_m-g_d \\ -g_d & g_m+g_d+G_S \end{vmatrix}$$

$$= G_G \begin{vmatrix} 2g_d+g_m & -g_m-g_d \\ g_d+g_m & G_S \end{vmatrix} = G_G\{(2g_d+g_m)G_S-(g_m+g_d)(g_d+g_m)\}$$

$$|Y_{54}^{14}| = \begin{vmatrix} g_m & g_m+2g_d & -g_m-g_d \\ -g_m & -g_d & g_m+g_d+G_S \\ 0 & -g_m-g_d & 0 \end{vmatrix} = \begin{vmatrix} 0 & 0 & G_S \\ -g_m & -g_d & g_m+g_d+G_S \\ 0 & -g_m-g_d & 0 \end{vmatrix}$$

$$= G_S g_m(g_m+g_d)$$

$$|Y_{14}^{14}| = \begin{vmatrix} 2g_d+g_m & -g_m-g_d & -g_d \\ -g_d & g_m+g_d+G_S & 0 \\ -g_m-g_d & 0 & g_d+G_D \end{vmatrix}$$

$$= \begin{vmatrix} 0 & G_S & G_D \\ -g_d & g_m+g_d+G_S & 0 \\ -g_m-g_d & 0 & g_d+G_D \end{vmatrix}$$

$$= -G_S g_d(g_d+G_D) + G_D(g_m+g_d)(g_m+g_d+G_S)$$

Voltage gain between output terminals 5 and 4 and input terminals 1 and 4 is expressed as;

$$A_v|_{14}^{54} = sgn(5-4)sgn(1-4)(-1)^{14}\frac{|Y_{54}^{14}|}{|Y_{14}^{14}|} = -\frac{|Y_{54}^{14}|}{|Y_{14}^{14}|} \quad (5)$$

$$A_v|_{14}^{54} = -\frac{|Y_{54}^{14}|}{|Y_{14}^{14}|} = -\frac{G_S g_m(g_m+g_d)}{-G_S g_d(g_d+G_D)+G_D(g_m+g_d)(g_m+g_d+G_S)}$$

$$= -\frac{G_S g_m g_m R_D R_S}{g_d+g_m(g_m R_S+1)} = -\frac{g_m R_D}{(g_m R_S+1)} = -g_m R_D \text{ (for } R_S=0)$$

The input resistance between terminals 1 and 4 of the Darlington pair amplifier in Fig.2(b) from Eq (3) is expressed as;

$$R_{in} = R_{i(14)} = \frac{|Y_{14}^{14}|}{|Y_4^4|}_{g_s=0} \quad (6)$$

$$|Y_4^4| = \begin{vmatrix} G_G & 0 & 0 & -G_G \\ g_m & 2g_d+g_m & -g_m-g_d & -g_m \\ -g_m & -g_d & g_m+g_d+G_S & -G_S \\ 0 & -g_m-g_d & 0 & g_m-G_D \end{vmatrix}$$

$$= \begin{vmatrix} G_G & 0 & 0 & -G_G \\ 0 & 0 & G_S & -G_S-G_D \\ -g_m & -g_d & g_m+g_d+G_S & -G_S \\ 0 & -g_m-g_d & 0 & g_m-G_D \end{vmatrix}$$

$$= \begin{vmatrix} G_G & 0 & 0 & 0 \\ 0 & 0 & G_S & -G_D \\ -g_m & -g_d & g_m+g_d+G_S & 0 \\ 0 & -g_m-g_d & 0 & -g_d-G_D \end{vmatrix}$$

$$= G_G \begin{vmatrix} 0 & G_S & -G_D \\ -g_d & g_m+g_d+G_S & 0 \\ -g_m-g_d & 0 & -g_d-G_D \end{vmatrix}$$

$$= G_G[\{-G_S g_d(g_d+G_D)\} - G_D(g_m+g_d)(g_m+g_d+G_S)]$$

$$= -G_G[\{G_S g_d(g_d+G_D)\} + G_D(g_m+g_d)(g_m+g_d+G_S)]$$

$$|Y_4^4|_{G_D=0} = -G_G G_S g_d g_d$$

$$R_{in} = R_{i(14)} = \frac{-G_S g_d(g_d+G_D)+G_D(g_m+g_d)(g_m+g_d+G_S)}{-G_G[G_S g_d(g_d+G_D)+G_D(g_m+g_d)(g_m+g_d+G_S)]} = R_G \text{ (evident)} \quad (7)$$

The output resistance between terminals 5 and 4 of the Darlington pair amplifier in Fig.1 (b) from Eq (3) is expressed as;

$$R_o = R_{o(54)} = \frac{|Y_{54}^{54}|}{|Y_4^4|}_{G_D=0} \quad (8)$$

$$R_o = R_{o(54)} = \frac{|Y_{54}^{54}|}{|Y_4^4|}_{G_D=0} = \frac{G_G\{(2g_d+g_m)G_S+(g_m+g_d)(g_d+g_m)\}}{G_G[\{G_S g_d g_d\}]}$$

$$= \frac{(2g_d+g_m)G_S}{G_S g_d g_d} + \frac{(g_m+g_d)(g_d+g_m)}{G_S g_d g_d}$$

$$= (2g_d + g_m)r_d r_d + (g_m + g_d)(g_d + g_m)R_S r_d r_d$$

$$= (2 + \mu)r_d + (\mu + 1)(1 + \mu)R_S = (2 + \mu)r_d + (\mu + 1)^2 R_S \quad (9)$$

$$A_v|_{14}^{24} = sgn(2-4)sgn(1-4)(-1)^{11}\frac{|Y_{24}^{14}|}{|Y_{14}^{14}|} = -\frac{|Y_{24}^{14}|}{|Y_{14}^{14}|} \quad (10)$$

$$|Y_{24}^{14}| = \begin{vmatrix} g_m & -g_m - g_d & -g_d \\ -g_m & g_m + g_d + G_S & 0 \\ 0 & 0 & g_d + G_D \end{vmatrix} = \begin{vmatrix} 0 & G_S & G_D \\ -g_m & g_m + g_d + G_S & 0 \\ 0 & 0 & g_d + G_D \end{vmatrix}$$

$$= g_m G_S (g_d + G_D)$$

$$A_v|_{14}^{24} = -\frac{|Y_{24}^{14}|}{|Y_{14}^{14}|} = -\frac{-G_S g_d (g_d+G_D) + G_D (g_m+g_d)(g_m+g_d+G_S)}{g_m G_S (g_d+G_D)}$$

$$= \frac{g_d (g_d+G_D) + G_D (g_m+g_d)(g_m+g_d+G_S)}{g_m (g_d+G_D)}$$

$$= \frac{g_d}{g_m} + \frac{G_D (g_m)(g_m+G_S)}{g_m G_S (G_D)} = \frac{1}{\mu} + \frac{(g_m+G_S)}{G_S} = \frac{1}{\mu} + (1 + g_m R_S) \cong (1 + g_m R_S) \quad (11)$$

11.13 FET-BJT Darlington (Conventional Method)

Obtain voltage gain and the output resistance for the circuit shown in Fig.11.14 (a).

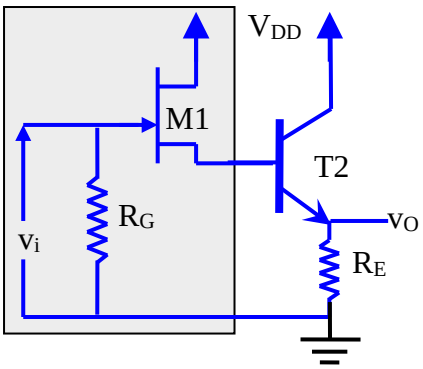

Figure 11.14 (a)

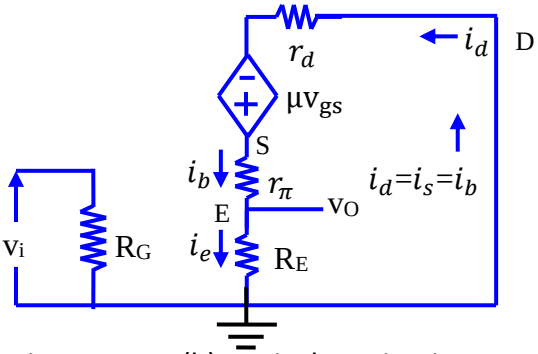

Figure 11.14 (b) Equivalent circuit

From Fig. 11.14 (b),

$$v_s = i_e R_E = (1 + \beta) i_b R_E \quad (11.83)$$

$$v_{gs} = v_g - v_s = v_i - v_s = v_i - \{r_\pi + (1 + \beta)R_E\} i_b$$

$$\mu v_{gs} = r_d i_d + r_\pi i_b + i_e R_E = r_d i_b + r_\pi i_b + (1 + \beta) R_E i_b$$

$$\mu v_i - \mu\{r_\pi + (1 + \beta)R_E\} i_b = r_d i_b + r_\pi i_b + (1 + \beta) R_E i_b$$

$$[r_d + r_\pi + (1 + \beta)R_E + \mu\{r_\pi + (1 + \beta)R_E\}] i_b = \mu v_i$$

$$i_b = \frac{\mu v_i}{r_d + r_\pi + (\mu+1)\{r_\pi + (1+\beta)R_E\}} \quad (11.84)$$

$$v_o = (1 + \beta) i_b R_E = (1 + \beta) \frac{\mu v_i}{r_d + r_\pi + (\mu+1)\{r_\pi + (1+\beta)R_E\}} R_E \quad (11.85)$$

$$\text{Voltage gain} = A_v = \frac{v_o}{v_i} = \frac{\mu(1+\beta)R_E}{r_d + r_\pi + (\mu+1)\{r_\pi + (1+\beta)R_E\}} \quad (11.86)$$

The input resistance is defined as;

$$R_{in} = \frac{v_i}{i_b}\Big|_{v_o=0} = R_G \tag{11.87}$$

Here analysis does not talk about the output resistance and the current gain.

FET-BJT Cascode amplifier (FAM Method)

Analyze the voltage gain and output resistance of the FET cascode amplifier shown in Fig.3(a) and Fig.3(b).

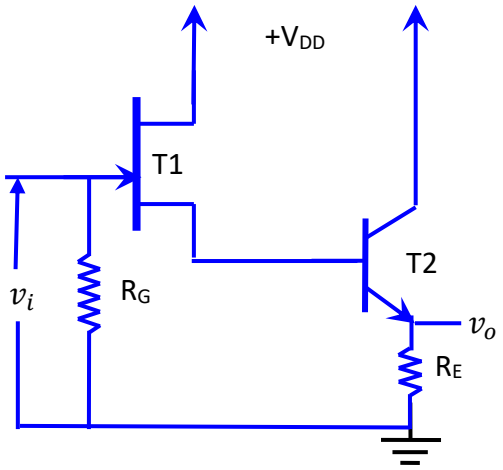

Figure 3(a)

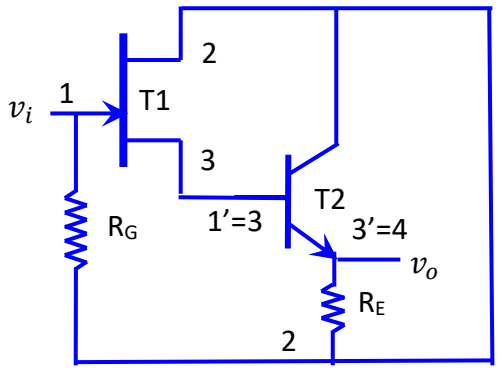

Figure 3(b) ac circuit

The partitioned floating admittance matrices of FET (T1) and BJT (T2) in Fig. 3 (b) are written as;

$$\begin{bmatrix} 1 & 2 & 3 \\ 0 & 0 & 0 \\ g_{m1} & g_d & -g_{m1}-g_d \\ -g_{m1} & -g_d & g_{m1}+g_d \end{bmatrix} \begin{matrix} \\ \\ 1 \\ 2 \\ 3 \end{matrix} \tag{1}$$

$$\begin{bmatrix} 3 & 2 & 4 \\ g_\pi & 0 & -g_\pi \\ g_{m2} & 0 & -g_m \\ -g_\pi - g_{m2} & 0 & g_\pi + g_{m2} \end{bmatrix} \begin{matrix} \\ 3 \\ 2 \\ 4 \end{matrix} \tag{2}$$

The partitioned floating admittance matrices of the passive resistors R_G and R_E are written as;

$$\begin{bmatrix} 1 & 2 & 3 & 4 \\ G_G & -G_G & 0 & 0 \\ -G_G & G_G+G_E & 0 & -G_E \\ 0 & 0 & 0 & 0 \\ 0 & -G_E & 0 & G_E \end{bmatrix} \begin{matrix} \\ 1 \\ 2 \\ 3 \\ 4 \end{matrix} \tag{3}$$

The overall floating admittance matrix of Fig. 3(b) is

$$\begin{bmatrix} 1 & 2 & 3 & 4 \\ G_G & -G_G & 0 & 0 \\ g_{m1}-G_G & g_d+G_G+G_E & -g_{m1}-g_d+g_{m2} & -g_{m2}-G_E \\ -g_{m1} & -g_d & g_{m1}+g_d+g_\pi & -g_\pi \\ 0 & -G_E & -g_\pi-g_{m2} & g_\pi+g_{m2}+G_E \end{bmatrix}\begin{bmatrix} 1 \\ 2 \\ 3 \\ 4 \end{bmatrix} \quad (4)$$

$$|Y_{42}^{12}| = \begin{vmatrix} -g_{m1} & g_{m1}+g_d+g_\pi \\ 0 & -g_\pi-g_{m2} \end{vmatrix} = g_{m1}(g_\pi+g_{m2}) = g_{m1}(1+\beta_2)g_\pi$$

$$|Y_2^2| = \begin{vmatrix} G_G & 0 & 0 \\ -g_{m1} & g_{m1}+g_d+g_\pi & -g_\pi \\ 0 & -g_\pi-g_{m2} & g_\pi+g_{m2}+G_E \end{vmatrix}$$

$$= G_G\begin{vmatrix} g_{m1}+g_d+g_\pi & -g_\pi \\ -g_\pi-g_{m2} & g_\pi+g_{m2}+G_E \end{vmatrix} = G_G\begin{vmatrix} g_{m1}+g_d & -g_\pi \\ G_E & g_\pi+g_{m2}+G_E \end{vmatrix}$$

$$= G_G\{(g_{m1}+g_d)(g_\pi+g_{m2}+G_E)+g_\pi G_E\}$$

$$= G_G[r_d+(1+\mu)\{r_\pi+(1+\beta_2)R_E\}]g_\pi G_E g_d$$

$$|Y_{12}^{12}| = \begin{vmatrix} g_{m1}+g_d+g_\pi & -g_\pi \\ -g_\pi-g_{m2} & g_\pi+g_{m2}+G_E \end{vmatrix} = \begin{vmatrix} g_{m1}+g_d & -g_\pi \\ G_E & g_\pi+g_{m2}+G_E \end{vmatrix}$$

$$= (g_{m1}+g_d)(g_\pi+g_{m2}+G_E)+g_\pi G_E$$

$$= g_d(1+\mu)g_\pi(R_E+g_{m2}r_\pi R_E+r_{\pi 2})G_E+g_\pi G_E$$

$$= [r_d+(1+\mu)\{r_\pi+(1+\beta_2)R_E\}]G_E g_\pi g_d$$

$$|Y_{32}^{12}| = \begin{vmatrix} -g_{m1} & -g_\pi \\ 0 & g_\pi+g_{m2}+G_E \end{vmatrix} = -g_{m1}\{g_\pi+g_{m2}+G_E\}$$

$$= -g_{m1}g_\pi\{R_E+g_{m2}r_\pi R_E+r_\pi\}G_E$$

$$= -g_{m1}g_\pi\{r_\pi+(1+\beta_2)R_E\}G_E$$

$$|Y_{42}^{42}| = \begin{vmatrix} G_G & 0 \\ -g_{m1} & g_{m1}+g_d+g_\pi \end{vmatrix} = G_G(g_{m1}+g_d+g_\pi)$$

$$= G_G(g_{m1}r_\pi r_d+r_d+r_\pi)g_d g_\pi$$

$$= G_G\{r_d+(1+\mu)r_\pi\}g_d g_\pi$$

$$A_v|_{12}^{42} = sgn(4-2)sgn(1-2)(-)^9\frac{|Y_{42}^{12}|}{|Y_{12}^{12}|} = \frac{|Y_{42}^{12}|}{|Y_{12}^{12}|} \quad (5)$$

$$A_v|_{12}^{42} = \frac{|Y_{42}^{12}|}{|Y_{12}^{12}|} = \frac{g_{m1}(1+\beta_2)g_\pi}{[r_d+(1+\mu)\{r_\pi+(1+\beta_2)R_E\}]G_E g_\pi g_d}$$

$$= \frac{g_{m1}(1+\beta_2)R_E r_d}{[r_d+(1+\mu)\{r_\pi+(1+\beta_2)R_E\}]} = \frac{\mu(1+\beta_2)R_E}{[r_d+(1+\mu)\{r_\pi+(1+\beta_2)R_E\}]} \quad (6)$$

$$R_{in} = R_{i(12)} = \frac{|Y_{12}^{12}|}{|Y_2^2|}_{g_s=0} = \frac{[r_d+(1+\mu)\{r_\pi+(1+\beta_2)R_E\}]G_E g_\pi g_d}{G_G[r_d+(1+\mu)\{r_\pi+(1+\beta_2)R_E\}]g_\pi G_E g_d}$$

$$= \frac{1}{G_G} = R_G(evident) \quad (7)$$

$$|Y_2^2|_{G_E=0} = \begin{vmatrix} G_G & G_G & 0 \\ -g_{m1} & g_d & -g_\pi \\ 0 & \cancel{G_E} & g_\pi + g_{m2} \cancel{+ G_E} \end{vmatrix} = \begin{vmatrix} G_G & G_G & 0 \\ -g_{m1} & g_d & -g_\pi \\ 0 & 0 & g_\pi + g_{m2} \end{vmatrix}$$

$$= (g_\pi + g_{m2})G_G(g_d + g_{m1}) = g_\pi(1+\beta_2)G_G g_d(1+\mu)$$

$$R_{out} = R_{i(42)} = \frac{|Y_{42}^{42}|}{|Y_2^2|}_{G_E=0} = \frac{G_G\{r_d+(1+\mu)r_\pi\}g_d g_\pi}{G_G g_d(1+\mu)(1+\beta_2)g_\pi} = \frac{\{r_d+(1+\mu)r_\pi\}}{(1+\mu)(1+\beta_2)}$$

$$= \frac{r_d}{(1+\mu)(1+\beta_2)} + \frac{(1+\mu)r_\pi}{(1+\mu)(1+\beta_2)}$$

$$= \frac{r_d}{\beta_2\mu} + \frac{(1+\mu)r_\pi}{(1+\beta_2)(1+\mu)} = \frac{r_d}{\beta_2\mu} + \frac{r_\pi}{\beta_2} = \frac{r_d}{\beta_2 g_{m1}} + \frac{1}{g_{m2}} \qquad (8)$$

$$A_i|_{12}^{42} = sgn(4-2)sgn(1-2)(-)^9 \frac{|Y_{42}^{12}|}{|Y_2^2|} G_L = \frac{|Y_{42}^{12}|}{|Y_2^2|} G_L \qquad (9)$$

$$A_i|_{12}^{42} = \frac{|Y_{42}^{12}|}{|Y_2^2|} G_L = \frac{g_{m1}(1+\beta_2)g_\pi}{G_G[r_d+(1+\mu)\{r_\pi+(1+\beta_2)R_E\}]g_\pi G_E g_d} G_E$$

$$= \frac{\mu(1+\beta_2)R_G}{[r_d+(1+\mu)\{r_\pi+(1+\beta_2)R_E\}]} = \frac{\mu(1+\beta_2)R_G}{(1+\mu)\{r_\pi+(1+\beta_2)R_E\}} = \frac{(1+\beta_2)R_G}{\{r_\pi+(1+\beta_2)R_E\}}$$

$$= \frac{R_G}{R_E}$$ (Evident as gate current will be negligible and hence ratio is very large).