ENERGY BALANCING AND FAULT-TOLERANT ABILITY OF A CASCADED MULTILEVEL INVERTER FOR SOLAR WATER PUMPING APPLICATIONS

Thesis Submitted for the Award of the Degree of

DOCTOR OF PHILOSOPHY

in

Electrical Engineering

By

M. NARASIMHA RAO

Registration Number: 41800127

Supervised By

Dr. N. KARTHICK (23586)

School of Electronics and Electrical Engineering (Associate Professor)

Lovely Professional University

Co- Supervised By

Dr. A. MADHUKAR RAO (S1152)

Electrical & Electronics Engineering (Assistant Professor)

Kakatiya Institute of Technology and Science, Warangal

LOVELY PROFESSIONAL UNIVERSITY

PUNJAB

2025

DECLARATION

I, hereby declare that the presented work in the thesis entitled **"Energy Balancing and Fault-tolerant Ability of a Cascaded Multilevel Inverter for Solar Water Pumping Applications"** in fulfilment of the degree of **Doctor of Philosophy (Ph.D.)** is the outcome of research work carried out by me under the supervision, **Dr. N. Karthick**, working as **Associate Professor,** in the **School of Electronics and Electrical Engineering,** of Lovely Professional University, Punjab, India and co-supervision of **Dr. A. Madhukar Rao**, working as **Assistant professor**, in the **Department of EEE**, KITS, Warangal, Telangana, India. In keeping with general practice of reporting scientific observations, due acknowledgements have been made whenever work described here has been based on findings of another investigator. This work has not been submitted in part or full to any other University or Institute for the award of any degree.

M. NARASIMHA RAO
Registration No.: 41800127
Department/school: School of Electronics and Electrical Engineering
Lovely Professional University,
Punjab, India

Place: Phagwara
Date: 07-05-2025

CERTIFICATE

This is to certify that the work reported in the Ph. D. thesis entitled "**ENERGY BALANCING AND FAULT-TOLERANT ABILITY OF A CASCADED MULTILEVEL INVERTER FOR SOLAR WATER PUMPING APPLICATIONS**" submitted in fulfillment of the requirement for the award of degree of **Doctor of Philosophy (Ph.D.)** in the **School of Electronics and Electrical Engineering**, is a research work carried out by **M. NARASIMHA RAO**, **41800127**, is a bonafide record of his original work carried out under my supervision and that no part of thesis has been submitted for any other degree, diploma or equivalent course.

Place: Phagwara
Date: 07-05-2025

Dr. N. KARTHICK
Associate Professor
School of Electronics and Electrical Engineering,
Lovely Professional University, Punjab

Dr. A. MADHUKAR RAO
Assistant Professor,
Kakatiya Institute of Technology and Science,
Warangal, Telangana

ABSTRACT

Extensive utilization as well as exploitation of various conventional resources in the 20th century leaves us with no option but to turn to renewable energy resources to build a sustainable future. Irrespective of the geographical limitations, these sources can be implemented as they are easy to install and work on low running cost. Whereas, in remote locations where there is a real time requirement for these renewable sources like Solar and wind energy, operating and troubleshooting proves to be a serious problem.

In order to tackle these issues, research on developing systems with fault tolerant converters proves to be an efficient way. While these essentially increase the reliability of a system, they also tend to provide uninterrupted power supply. In cases like these, we see a consistent combination of fault tolerant systems with multi-level inverters. Multi-level inverters tend to show immense potential as they can have a major impact on the power quality of the system on a whole. Along with that, reduction in the requirement of output filter size and controlled total harmonic distortion constitutes of other advantages. But, addition of multi-level inverters gives rise to increase in the device count and sources of dc power as the number of voltage levels are stepped up.

This increase in the number of variables brings in the issue of Energy Balancing between the sources and also accounts to the switch failures in semiconductor systems. If these issues prove to be evident than the overall reliability of the system gets effected. Energy Balancing issues are not addressed by most of the present topologies of multi-level inverters with photovoltaic sources. Multiple troubles ranging from partial shading to uneven charge states to hotspots affect the associated batteries. Thus, the fault tolerant multi-level inverters must be equipped with a fully functioning Energy Balancing capability which is presented in this thesis in order to avoid faster discharge of PV system risking an inefficient system there by leading a total system shutdown.

NOMENCLATURE

ABBREVIATIONS

RES	:	Renewable Energy Source
SWPS	:	Solar Water Pumping Systems
THD	:	Total Harmonic Distortion
EV	:	Electric Vehicles
PWM	:	Pulse Width Modulation
PD-PWM	:	Phase Disposition Pulse Width Modulation
ESS	:	Energy Storage Systems
SPVS	:	Solar Photovoltaic System
VSI	:	Voltage Source Inverter
SPWM	:	Sinusoidal Pulse Width Modulation
SVM	:	Space Vector Modulation
DCMLI	:	Diode Clamped Multilevel Inverter
FC-MLI	:	Flying Capacitor Multilevel Inverter
CH-MLI	:	Cascaded H-Bridge Multilevel Inverter
NPC	:	Neutral Point Clamped Inverter
PSD	:	Power Semiconductor Device
IGBT	:	Insulated Gate Bipolar Transistor
MOSFET	:	Metal-Oxide-Semiconductor Field-Effect Transistors
RSC-MLI	:	Reduced Switch Count MLIs
OC	:	Open Circuit
SC	:	Short Circuit

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Date: 07-05-2025 **M.Narasimha Rao**

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CHAPTER 1
INTRODUCTION

1.1 Background and Knowledge Gaps

Water is a necessity for sustainability. It is necessary for large-scale water systems, development, and power generation in addition to being needed for drinking and household use. Water plays an important role in the development of any country. Private pride in each beautiful kingdom is based on the amount and nature of that kingdom's accessible water resources. It has been classified that daily survival requires the usual five litres of water per day according to the individual [1]. Although there is a lot of water available in the world, it is not always available in places where it can be fully used directly. This increases the desire to pump water from your equipment to areas where it is popular for several kilometres. For this purpose, the water pump has been used for quite a long time. Solar photovoltaic power was introduced in the late 1980s and grew in importance by the mid-1990s. Previous photovoltaic (PV) cells based entirely on sunlight were very wasteful, with an efficiency of only 5-6 percent, and very expensive [2]. Farmers in a country like India face water challenges ranging from months of combined rainfall in summer to heavy crop-destroying rains in the off-season. This leads to inevitable drought, which leads to several socioeconomic problems that affect the food chain of the entire country. A Solar water pumping system effectively solves this problem because it can store Solar energy and thus strengthen the pumping system.

Many countries currently have a huge vacuum in terms of irrigation and this needs to be filled as the country's population is growing rapidly. Efficient Solar water systems help these desert countries and are part of creating the current sustainable regions through agriculture. Water pumping systems work at different levels of the irrigation process, namely to distribute water between different levels or to improve pressure to meet requirements. Of the available renewable energy sources, using Solar water pumps is more efficient and beneficial, as it is used with low maintenance costs and is generally very reliable. To extract the maximum power from the panel MPPT algorithms are used [3-5].

A technique for mitigating climate change that lowers greenhouse gas (GHG) emissions in agricultural production is solar irrigation. Small-scale farmers are forced to use conventional diesel-powered irrigation pumps because photovoltaic (PV) systems are too expensive for them, despite their promise. This research attempts to examine, from the viewpoint of small-scale farmers in developing nations, the social, economic, and environmental implications of implementing solar irrigation systems [6].

The majority of the land is irrigated by tube wells because water is a valuable resource for agriculture. In order to meet irrigation water needs, diesel engines and electricity-powered pumps are frequently utilized; however, these traditional methods are expensive and ineffective. Selecting a renewable energy source is crucial in light of growing worries about global warming. Taking into account the water requirement, solar resources, tilt degree and orientation, system losses, and performance ratio, SPVWPS has been optimally built in this study [7].

Solar water pumps are vital for farmers, offering substantial energy savings and reducing dependence on conventional fuels. Government subsidies further encourage their adoption, making them a practical option that supports sustainable agriculture. However, the high cost of the necessary solar panels requires optimizing solar water pumping systems (SWPS) for economic feasibility. This study focuses on improving the efficiency and reliability of permanent magnet synchronous motor (PMSM)-driven SWPS in rural areas by employing hybrid maximum power point tracking (MPPT) algorithms and a voltage-to-frequency (V/f) control strategy. The V/f control strategy simplifies the control process while improving performance. Despite system non-idealities and maximum duty cycle constraints, PMSM-based SWPS offer superior efficiency and stability, making them well-suited for off-grid water pumping applications [8].

1.1.1 Operation/Implementation of SPV-WPS based on geographical location

Access to clean drinking water is a major problem in most countries of the world. Only 13% of the world's people live in areas without electricity. Because SPV-WPS has become an outstanding choice in isolated places and non-electrified areas.

This review summarizes the work done on the implementation of SPV-WPS in 28 countries in different geographical locations as shown in figure 1.1

Figure 1.1 Main Solar water pump systems installed in different geographical locations [9]

1.1.2 Financial viability of SPV-WPS:

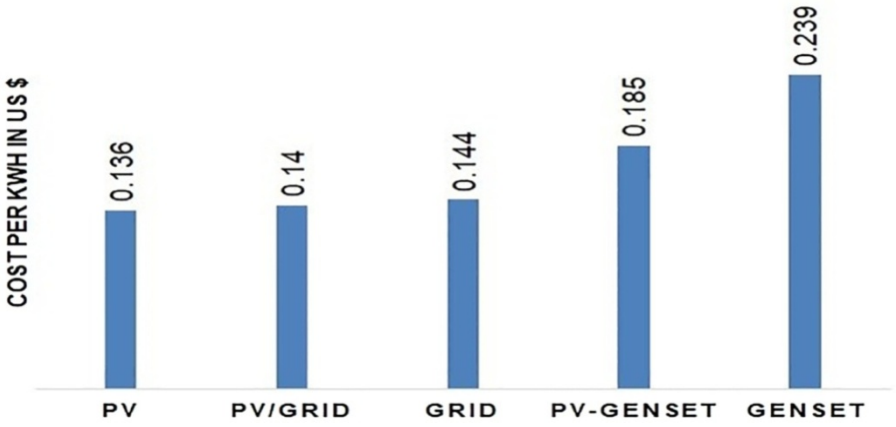


Figure 1.2 Cost comparison of different power sources [10,11]

In Jordan, a cost comparison of four possible power generation options (eg, generator, grid, photovoltaic grid, and PV generator) for large-scale groundwater pumping is done, and its comparison graph in Figure 1.2 shows that Solar is the lowest. electricity generation cost $0.136 per kilowatt-hour. Thus, the use of water pumps using SPVWPS would result in lower costs per kilowatt-hour and carbon emissions with a minimal payback period.

1.2 Sustainable Agricultural Production - A Comprehensive Review of Solar Water Pumping Systems

Agriculture, being the core aspect of human evolution, stands as the center of the world's economy. It is directly responsible for the development of sustainable and economic growth in all aspects [12, 13]. As the world is becoming a global village in the 21st century, agricultural production today is a challenging task in every which way [14]. These challenges can be minimized by sustainable production methods like organic agriculture, hydroponics, agro-farming systems, etc. [15]. One such important and effective practice can be the usage of Solar photovoltaic pumping systems instead of renewable water pumping systems. Irrespective of the geographical location and other real-time constraints, Solar-based systems can be a great power source for water-based irrigation as shown in Figure 1.3 [16]. These Solar-based systems don't just increase the productivity and efficiency of irrigation systems but also help in the decrease in the overall emission of CO_2 [17].

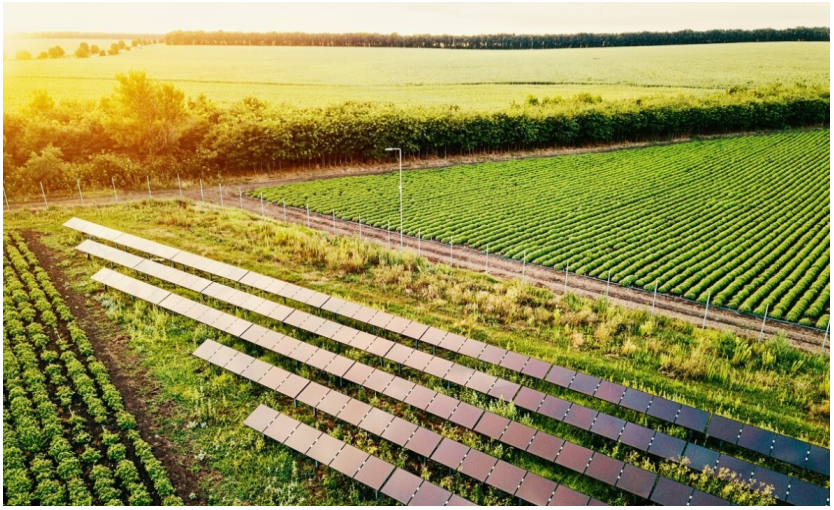


Figure 1.3 Sustainable Agriculture Production [16]

Power can also be utilized in various ways from the unused energy generated from renewable energy sources. Consistent utilization of these systems helped to decrease their costs thereby making it a more convenient and effective solution for both urban and rural areas [18]. Whereas, people in rural areas generally lack knowledge of these new systems and may get anxious based on constraints like high costs, Solar

fluctuations, and other limiting factors [19]. Thus, understanding Solar PV systems as a whole will help make them more suitable for sustainable agricultural production.

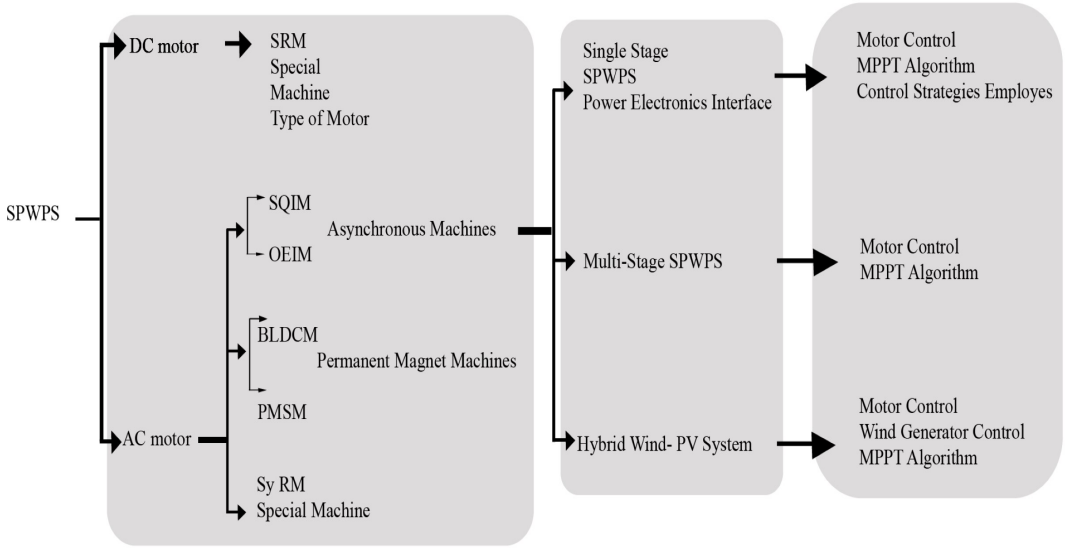


Figure 1.4 Solar PV water pumping system - Classification [20]

Farmers in a country like India are subjected to difficulties concerning water starting from lack of rainfall for months together in the summers to heavy, crop-destroying rains in off-season's results in an inevitable drought leading to several socioeconomic problems that affects the food chain of the whole country. Solar powered water pumping system will effectively terminate this problem with its ability to store Solar power thereby strengthening the pumping system. Among every one of the sustainable sources, sunlight-based photovoltaic energy has immense potential and is liked as an eco - accommodating choice. In India, Solar energy is accessible all over and it tends to be utilized for different applications a ton of studies have been conducted to investigate and comprehend the boundaries like reliability and financial factors of SPVWPS. The classification of SWPS is shown in figure 1.4 whereas the schematic diagram is shown in figure 1.5.

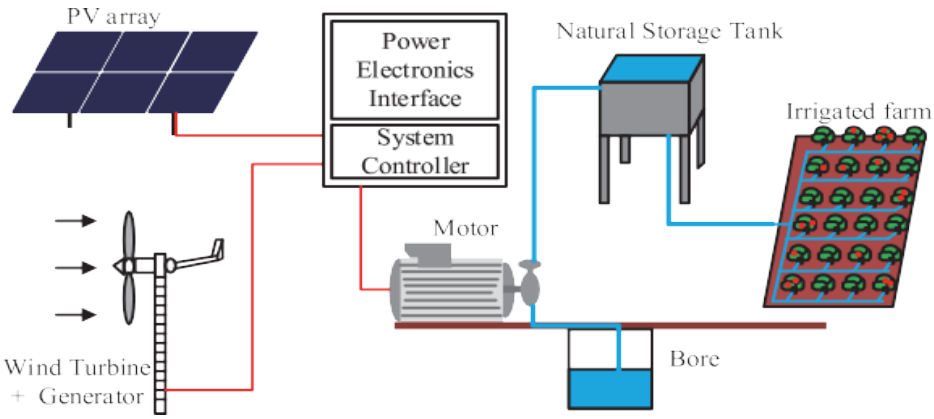


Figure 1.5 A water pumping system based on renewable energy.[20]

Water pumping is a process of imparting kinetic and potential energy to water to transfer it from one place to another. In renewable energy water pumping systems, the renewable energy source is first converted to electric energy for use. A suitable power conditioning circuit with an appropriate control strategy is designed to efficiently deliver the available electric power to load (Motor coupled with centrifugal pump). The centrifugal pump coupled to the motor shaft helps to convert mechanical energy to kinetic and potential energy. Fig.1.5 shows the subsystems of a typical renewable energy based water pumping system.

1.3 Multilevel Converters, Topologies and Modulation Techniques – An Overview

Recently, MLI has been considered a cutting-edge innovation in DC to AC power conversion in age, transmission, distribution, and electrical power capabilities. They have been created as savvy answers for the majority of energy applications, for example, Attractive Reverberation Imaging X-ray and acceptance of warming power supply [21]. Active filters (AFs), ship propulsion, conveyors, mine hoists traction/transport engine motors, dynamic voltage restorers DVR: Unified Power Flow Controllers (UPFC), Static Compensators (STATCOM), High Voltage Direct Current (HVDC) , FACTS, RER .

Because of the blocking voltage limit set by the semiconductor, common two-level inverters can't work in the medium voltage range. Be that as it may, MLIs are fundamental for medium voltage and high power applications. Additionally, compared to two-level inverters of the same power classes, MLIs have the advantage that the

harmonic content of the line voltage supplied to the load is lower compared to the level of their switching frequencies. [22]. The following are the main factors that made MLI a decisive revolution for efficient performance during the industrial age:

a) Simple interface for motor drives where DC is used to facilitate charging.
b) It can operate at higher voltage and current levels and is structurally compatible.
c) To achieve fault tolerance, it takes the input stream with less distortion and uses different control strategies and smaller switching states.
d) As a result of switching at the fundamental frequency, higher efficiency reduces conduction and switching losses.
e) since the power voltage is distributed between the switches at different levels, there are fewer voltage derivatives in power electronic switches.
f) Better electromagnetic compatibility and low harmonic power quality.
g) A reduced common-mode voltage is produced, enabling transformer less operation

1.3.1 Expansion of MLI Topology structures

Progress views of different MLI topologies are described in Figure 1.6. This gives an inside-and-out investigation of that turn of events. CHB was developed first by Baker and Bannister in the 1970s [23]. It was capable of producing a voltage with multiple levels by making use of various DC source voltages [24]. The NPC inverter, first developed by Nabae et al., was the subsequent development in MLI Topology during the 1980s.

In the 1990s, Meynard and Foch [26] and Lavieville et al. [27] developed an FC-type MLI. These three classic MLI-based Topology types have been considered the basis of most modern MLI inverters. The following creation was the secluded multilevel converter (MMC), which was generally utilized in industry [28]. A common MLI called was introduced in 2000. The authors proposed an active neutral Point clamp Topology in [29].

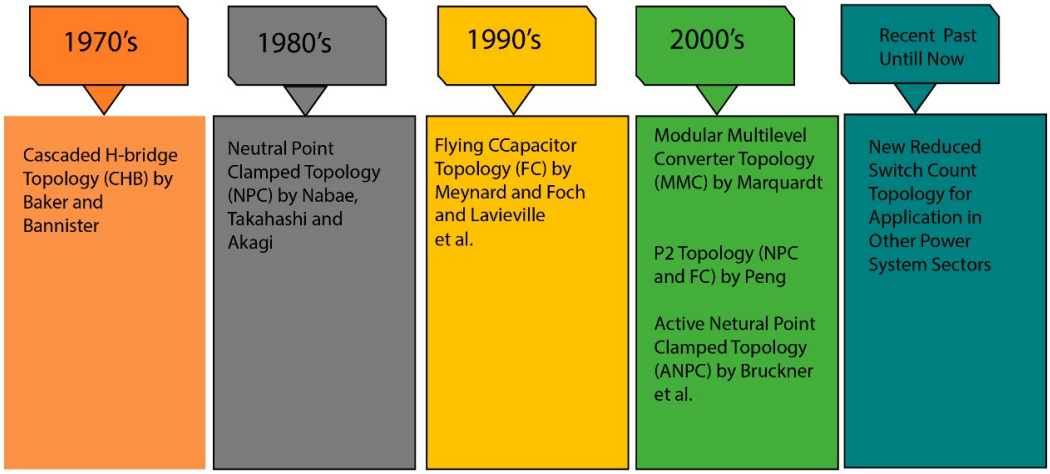


Figure 1.6 Growth of MLI topologies [26-29]

There have already been several additional novel MLI topologies that use application-based methodologies. In a similar way, researchers have concentrated on developing an additional reduced switch count. [30].

MLI can be arranged as

(i) having inborn negative level

(ii) without inborn negative level

(iii) symmetric type in light of the utilization of equivalent DC sources

(iv) asymmetric type in view of the utilization of inconsistent DC sources

(v) regenerative design for activity as both an inverter and a rectifier

(vi) hybrid approach of NPC, FC and CHB

(vii) utilization of capacitors joins with single sources

First proposed in 1975 [23] , the MLI concept was later applied through a work to support different topologies considering the changing design of electrical semiconductor switches and DC power paths. In addition, the study focused on using multiple switch combinations with limited voltage-range DC sources to combine voltage and AC to achieve more significant power.

1.3.1.1 (NPC-MLI) Neutral Point Clamped Multilevel Inverter

A diode-coupled multilevel inverter (DC-MLI), otherwise called NPC-MLI, was proposed by Nabae, Takashi & Akagi in 1981 [25]. Due to their extensive experience with medium voltage, high power, and relatively high efficiency, these inverters have gained widespread acceptance. Assuming that the two diodes pull the changing voltage to half of the Input voltage, the design is three-level. Additionally, it makes sure that the supply voltage is distributed equally between the two halves of the switches held at these points, which have a neutral point in between. The zero point is the name given to the intermediate voltage level. As seen in Figure 1.7, this topology produces multiple DC voltage levels by connecting multiple capacitor banks in series.

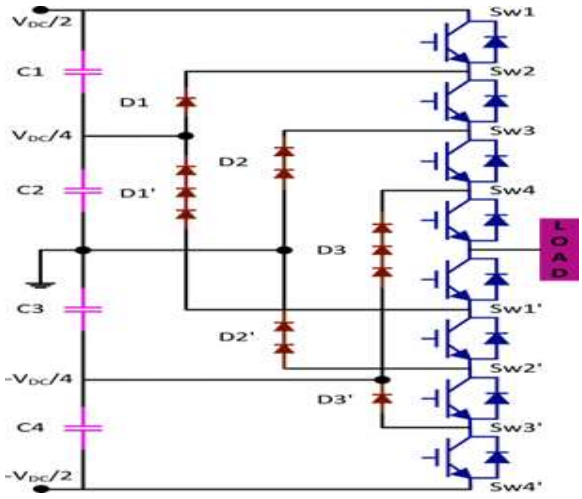


Figure 1.7 Topology of a zero-point clamped multilevel inverter [25-28]

Advantages:

- Excellent efficiency at the basic switching frequency .
- At the appropriate voltage level, the capacitors can be pre-charged collectively.
- With every phase having a shared DC link, the inverter's capacitance requirement is reduced to the minimum.

Disadvantages:

- Because of the quadratically correlated relationship between the number of diodes and the number of levels, packaging for inverters with a high number of levels may present challenges.

- Without the proper control, intermediate DC levels have a tendency to be uneven, which makes real power transmission problematic.
- The diodes required for the converter have uneven ratings.

NPC-MLI tracks down its application in the accompanying ways: voltage AC/DC transmission system [31], variable-speed engine drives, interconnections of high voltage systems and absorption into a high voltage AC and DC transmission system, and static VAR compensation (SVC).

1.3.1.2 (FC-MLI) Flying- Capacitor-Multilevel-Inverter

In 1992, FC-MLI Topology was proposed by Lavieville et al. & Meynard [46] & Foch [45] and to reduce static and dynamic voltage sharing between semiconductor switches in the N-P-C-MLI Topology. The basic architecture of NPC-MLI and FC-MLI is the same. But in this case, as you can see in the Figure 1.8, capacitors are used instead of fixed diodes. We call this Topology FC. Compared to the other capacitors in the whole set, the FC capacitors that replaced the DC-MLI diodes are autonomous (flying). Each capacitor has a different voltage than the capacitor next to it.

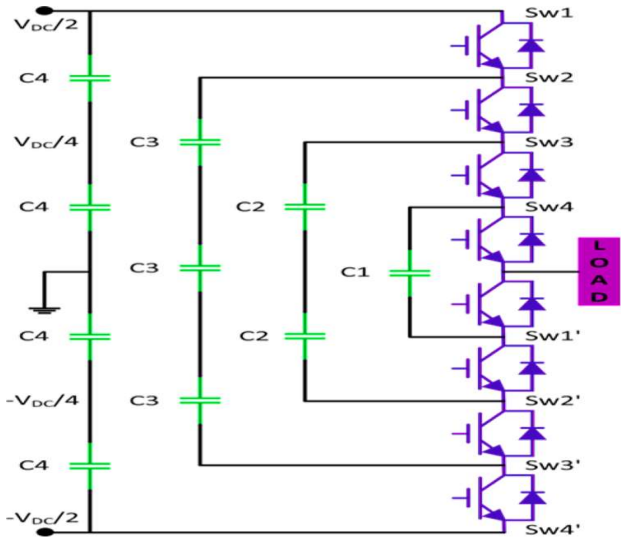


Figure 1.8 Topology of Flying Capacitor Multilevel Inverter [45]

This MLI Topology has several advantages over NPC-MLI, such as:

i. Further developed dependability of the FC is accomplished by the overt repetitiveness of exchanging inside the stage.
ii. Ability to control both the dynamic and reactive power
iii. It has a transformer less working
iv. More adaptable in combining voltage by utilizing capacitors as opposed to clamping diodes.

1.3.1.3 (CHB-MLI) Cascaded H-Bridge Multilevel Inverter

Bannister & Baker [41] suggested the principal patent for this Topology, which likely supplanted beforehand, portrayed topologies because of its essentially lower input power prerequisites. This Topology, known as CHB-MLI, creates a network of connections between individual DC sources and H-bridges. A multi-level stepped waveform is produced by numerous H-bridge structures connected in series. A common H-bridge element can be cascaded to create an arbitrary number of levels in the resulting CHB-MLI.

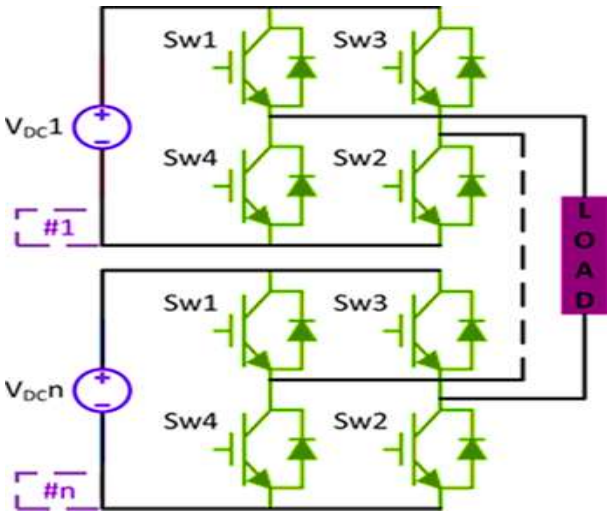


Figure 1.9 Cascade H-Bridge Multilevel Inverter Topology [33]

Modulation is possible with this CHB-MLI function. After settling the activity of huge-power medium voltage, which has now arrived at the modern megawatt level, mechanical advancements have occurred. It is a useful tool against voltage imbalance between NPC and FC nodes due to its modular design. Fuel cells, ultra capacitors Batteries and springs connected to the AC side are examples of isolated DC sources on

the D-C side that power the power conversion elements that make up the CHB [33]. A schematic representation of the CHB topology is displayed in Fig.1.9

Advantages:

- There are more than twice as many possible voltage levels as there are capacitors in a double leg unit (H bridge),
- Thanks to the modularized structure that makes packaging and storage simple.

Disadvantages:

- Every module needs its own capacitor or separate DC sources.
- Because there are more capacitors that need to be balanced, a more sophisticated controller is needed.

1.4 MLI control and modulation systems

Controlling general performance constraints, including switching losses & harmonic reduction, which are utilized to turn on the inverter and regulate the entire system, is the primary function of modulation techniques [34]. In addition, their function is to connect the control signals so that all voltage sources remain regulated. The main target of regulation is to produce a DC voltage signal which is a staircase and a signal for reference which is usually sine form in a normal state [35]. Different multiple / single characteristics of the carrier waveform are usually incorporated in the modulation process along with the modulating waveform. Modulation is also described as the process of modifying the feature of a certain waveform (the carrier wave) using another signal (the reference wave) to control the switching operation. Every MLI group has selected an appropriate modulation plot to improve circuit performance and meet the set objectives. The primary determinants in selecting a specific modulation technique for a given MLI family are as follows: (i) degree of distortion; (ii) exchange frequency; (iii) amount of losses; and (iv) reaction time. (v) the overall quantity of harmonics produced; Prior to usage, MLI modulation techniques must adhere to the following specifications: It should have the following features: (i) modular construction; (ii) no multiple voltage levels can be turned on at the same time; (iii) power supplies should run at the lowest possible frequency; (iv) load sharing between power modules should be consistent; (v)

The verification algorithm must be clear-cut and easy to understand, and (vi) the implementation cost must be minimal (vii) voltage quality must be high;

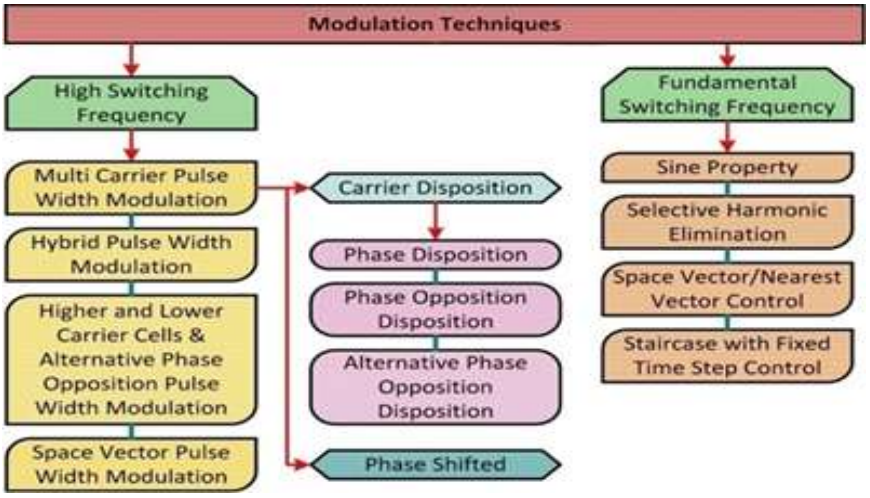


Figure 1.10 Modulation schemes for multilevel inverter [34]

In addition, the module index is crucial for any control system. THD varies depending on the modulation, which also depends on the modulation ratio (under-modulation/ over). Authors recommend different methods in the literature based on whether the switching frequency is fundamental or high frequency. On the other hand, connecting it to the low frequency or fundamental frequency causes small losses. Various MLI control and modulation techniques are shown in Fig. 1.10.

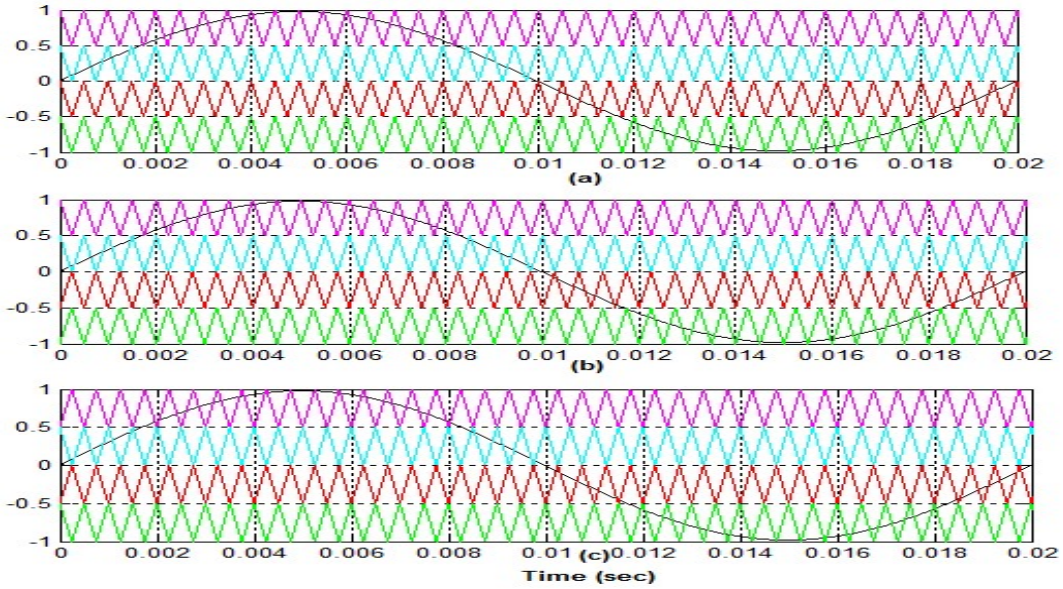


Figure 1.11 Classification of multilevel inverter system different carrier pwm techniques. (a) In phase disposition (b) Phase opposition (c) Alternate phase opposition disposition.

Fig. 1.11 illustrates the three distinct carrier modulation methods used to produce a five-level output voltage. Here, a five-level output voltage across the load is produced by comparing the modulating signal with four triangular carriers.

1.5 Research and treatment methods of IGBT block failures in power electronic converters and Fault Tolerant Multilevel Inverter Topologies comprehensive review

Power electronics, a technology that allows electricity to be efficiently converted from one phase to another, is used in many places to ensure efficiency high and effectiveness. The field of power electronics has grown in recent decades mainly for two reasons: the development of high-speed switches and high-power solid-state switches, and the availability of microcontroller's advancements capable of implementing complex & advanced algorithms.

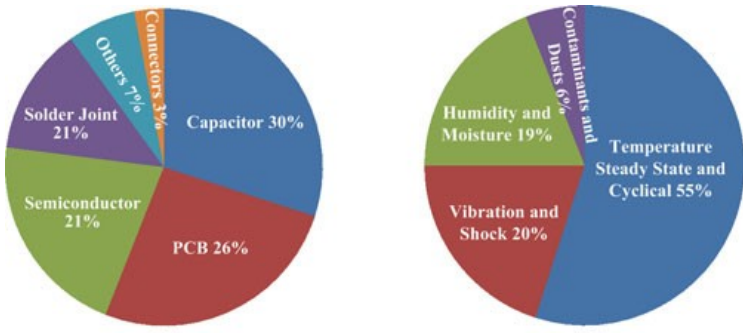


Figure 1.12 Distributed Percentage of failures in (a) power converter (b) sources [41].

These factors led to the development of cost-effective and grid-friendly converters [36]. In addition, solutions with innovation in circuit Topology & control strategy with integration of sensors and systems have also contributed to the development of power electronics [37]. Intensive R&D in these areas has led to significant improvements in the performance of power electronic systems, especially as regards efficiency and energy density.

Due to safety requirements, the reliability limits of power-electronic systems in the automotive & aviation industries are increasingly strict. In addition, the energy & industrial sectors follow the same vogue, trying to improve the dependability of power-electronic systems with sustainable and cost-effective solutions [38]. The following

three areas of research in the field of energy electronics reliability have received a lot of attention. The analysis of the causes and processes for the failure of electronic products is followed by this. The reliability and adequate durability of effective electronic products are also important factors. Reliable field work under specific conditions is ensured by effective condition management and monitoring, as described below. The electrical supply is an extremely vulnerable component of the electronics transformers, [39]. As shown in Figure 1.12(a). Semiconductor and soldering defects in hardware modules are responsible for 34% of transformer system failures. According to a survey based on more than 200 products from more than 80 companies, 31% of respondents chose semiconductor power devices as the most sensitive components [40]. Figure 1.12 (b) shows the sources of stress factors that significantly influence reliability [41]. Temperature stress factors have the greatest influence on the reliability of power electronic components and systems. Other factors such as humidity and vibration are closely related to energy equipment failure.

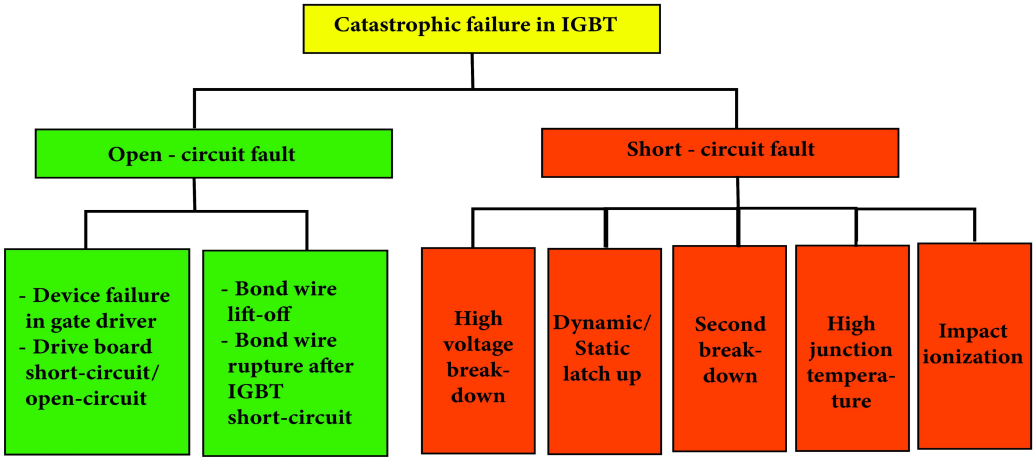


Figure 1.13 Failures in IGBT modules [41]

The dependability of power equipment and the overall power electronic system is closely correlated, as was previously mentioned. Thus, an explanation of power device faults and their release mechanisms in power transformers is required to increase the reliability of power electronic systems. The estimated lifetime of the IGBT module is necessary to design power converters with a certain level of reliability. To find out how long a device module should last under specific operating circumstances, lifetime

prediction models can be employed. As opposed to catastrophic failures, lifetime models are made to account for wear failures brought on by stresses like temperature, voltage, current, vibration, humidity, and cosmic radiation. The models and standard temperature estimation techniques for life prediction are shown in this section. Empirical and more physical models are two categories into which lifespan models can be divided [42].

The different open circuit shortcoming strategies alongside their correlation are introduced in Table-1.

Table 1: Open-Circuit Fault Detection Methods-A comparison

Additional Hardware	**Tuning Effort**	**Diagnosis Time**	**Effectiveness**	**Methods**
Not required	Medium	Within2 fundamental periods	Poor at small current	Current vector shape method [43,44]
Not required	High	Average 2 fundamental periods	Poor at small current	Slope of space vector's trajectory method [48]
Not required	Medium	Within 1.5 Fundamental periods	Poor at small current	Direct average current method [45,46]
Not required	Low	Within 1.5 Fundamental periods	Good	Modified normalized average current method [47]
Required	Tuning Effort	Fast but not defined	Good	Method based on switching function model [47]
Required	Medium	Approximately 2.7 ms	Great however the area of location can't be recognized	Lower-switch voltage estimating strategy [49,50]

1.5.1 Fault Tolerant Multilevel Inverter Topologies:

Numerous researchers have come up with a variety of MLI topologies with fault resiliency, and research is still ongoing to improve power delivery and THD. Here, we look at a few MLI with fault resiliency topologies.

As seen in Fig. 1.14, a fault-tolerant topology is proposed to increase the system's reliability. This topology has the benefit of maintaining the same number of output voltage levels in the event of a fault. By altering the control signal, redundant voltage state states are used to create fault tolerance. To create a fault-tolerant system, nevertheless, more semiconductor devices are needed. For five-level fault tolerant operation, the architecture employs 22 semiconductor devices (standard five-level requires 8 semiconductor devices).

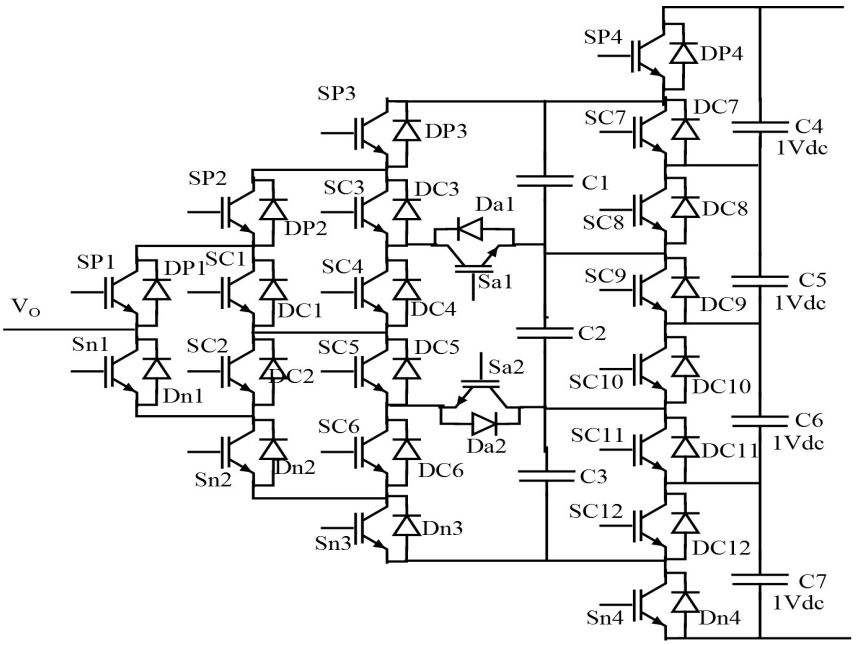


Figure 1.14 Five-level inverter topology with fault tolerant ability [51]

Fig. 1.15 depicts the topology of an A-phase NPC _ve-level inverter. Four capacitors, C1 through C4, and a DC voltage source, Udc, are components of the topological structure. In each phase, where x D a, b, and c, there are also eight power switch tubes (Sx1 _Sx8), eight freewheeling diodes (Dx1 _Dx8), and twelve clamp diodes. Only four power switch tubes are active at any given time; the other four are in the off state. Direction in which the load current flows from the inverter into the load as a positive

direction in which the load current flows from the inverter to the load, and Sa, Sb, and Sc denotes the phase-by-phase switching state.

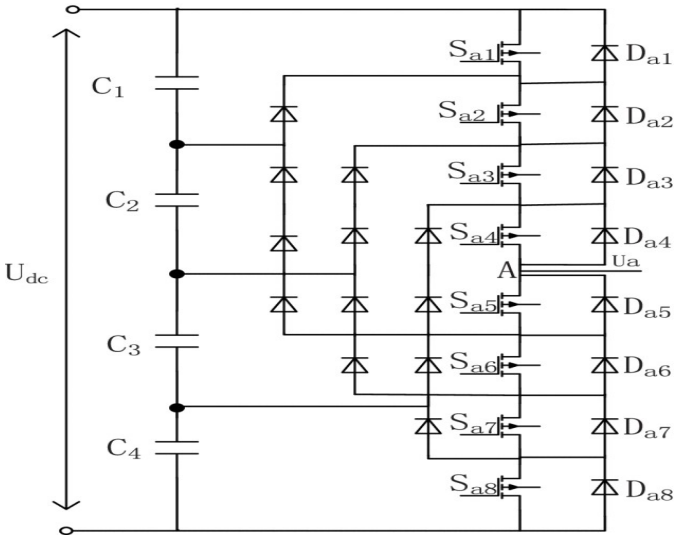


Figure 1.15 Topological structure of A-phase NPC five-level inverter [52]

In order to bring in an efficient and low cost Topology, the usage of DC sources and semiconductor devices has been controlled here. Independent of the load and modulation index, this setup has a self-voltage balance for the capacitor voltage. The cascaded configuration as shown in Fig 1.16 further helps in improving the performance and reducing the complexity. Both 9-level and 17-level inverters have been exploring in this study and relevant prototypes are also developed to test the hardware component [53].

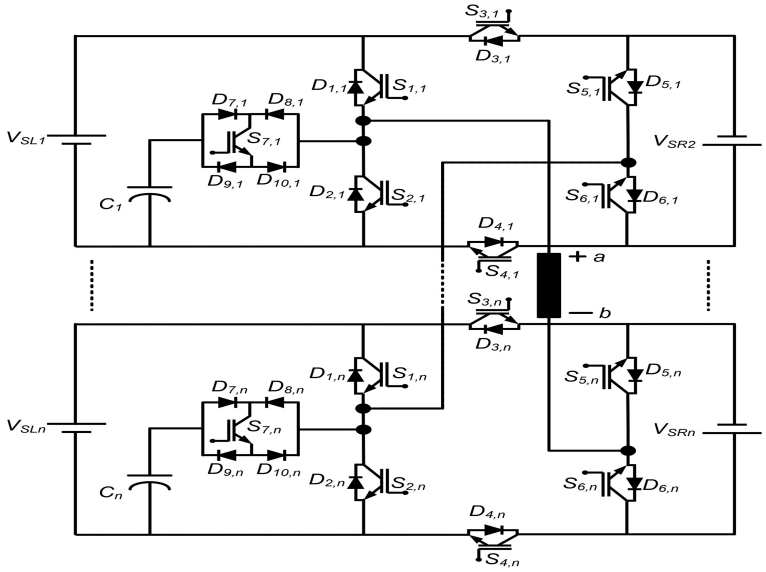


Figure 1.16 Configuration of the proposed fault tolerant Topology [53]

Figure 1.17 shows the schematic structure of the topology. Ten unidirectional switches (one each for bidirectional current flow and bidirectional voltage blocking) and one bidirectional switch (two switches in a common emitter arrangement) with two pairs of dc voltage sources at Vdc and 3 Vdc each make up the components employed. Fault-free topology operation yields 15 output load voltage levels, ranging from 0 to 7 Vdc. When a fault occurs, diodes D1, D2, D3, D4, D5, and D6 are there to counteract the fly back effect [54].

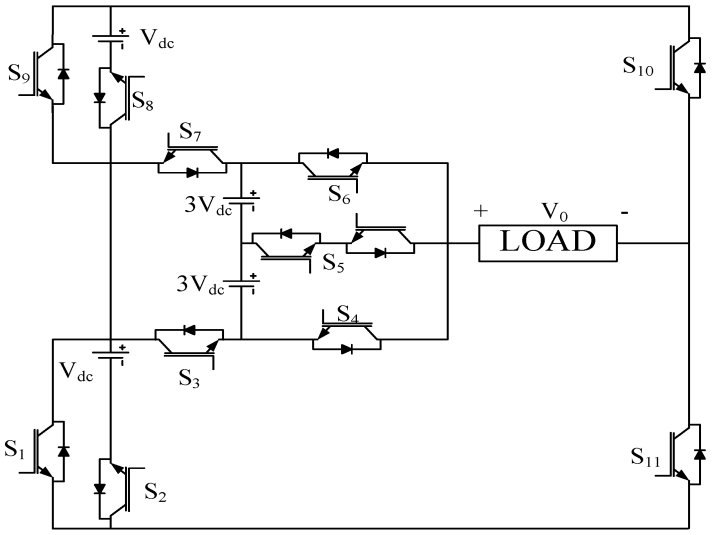


Figure 1.17 Schematic structure of the topology [54]

1.6 Energy Balance Control of a Cascaded Multilevel Inverter for Standalone Solar Photovoltaic Applications.

An MPPT charge regulator, multiple PV arrays, connected batteries, and a multilevel inverter are depicted in the figure as a block diagram. Multilevel inverters are still more common in photovoltaic installations compared to diode, clamp and protruded H-bridge multilevel inverters. Figure 1.18 shows a case study of the 5-level diode clamp inverter with 4 equal power sources in combination. Owing to partial shading of P-V panels and/or switches to produce multi-level voltage, an energy imbalance between the sources may occur. Imagine that every source is an independent PV string that has a backup battery. In case one of the PV strips is not fully shaded, the associated batteries will experience inverse charging and discharging. Under-utilization of healthy components results from a battery with a low state of charge (SOC) that

rapidly drains and shuts down the system. The uneven cargo energy distribution along the sources is another issue with a diode-mounted multilevel inverter.

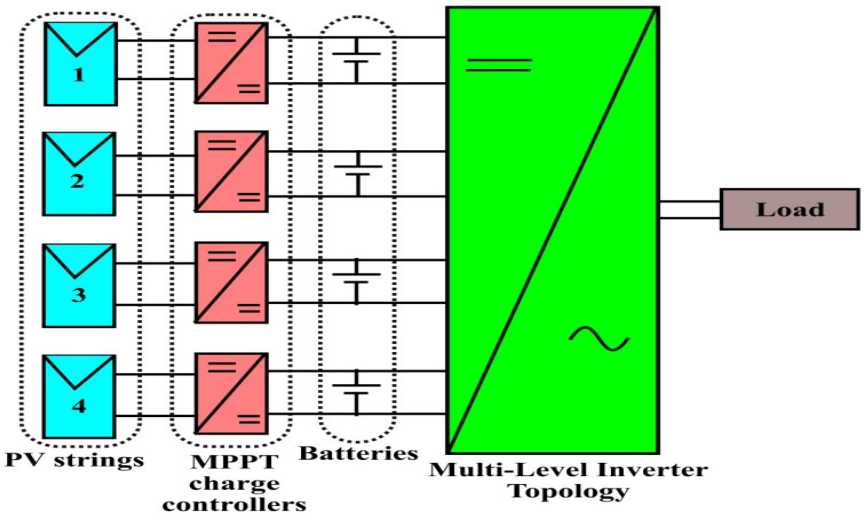


Figure 1.18 Multi-source single-phase inverter system block diagram [52]

1.7 Objectives & Research Methodology

RO-I: To propose a new multi-level inverter Topology that addresses the reliability issues (i.e. fault-tolerant) of the system.

RO-II: To design a multi-level inverter Topology for Energy Balancing issues.

RO-III: The simulation results of the proposed Topology are to be validated by designing a 2kW Cascaded Multilevel inverter for Solar water pumping applications.

1.8 Research Methodology:

To address the current challenges related to faults and uneven energy distribution in inverter systems, a new topology is being introduced. This design specifically targets solar-powered water pumping systems, as illustrated in the Figure.1.19. A fully operational hardware prototype has been created based on this design, which has also been simulated using MATLAB. To resolve fault issues, this setup employs innovative switching techniques to manage both switch open faults and source open faults. The key feature of this switching combination ensures an effective and reliable topology optimizing performance through the most efficient configurations. Additionally, this topology manages battery charging, enabling better energy balance within the system.

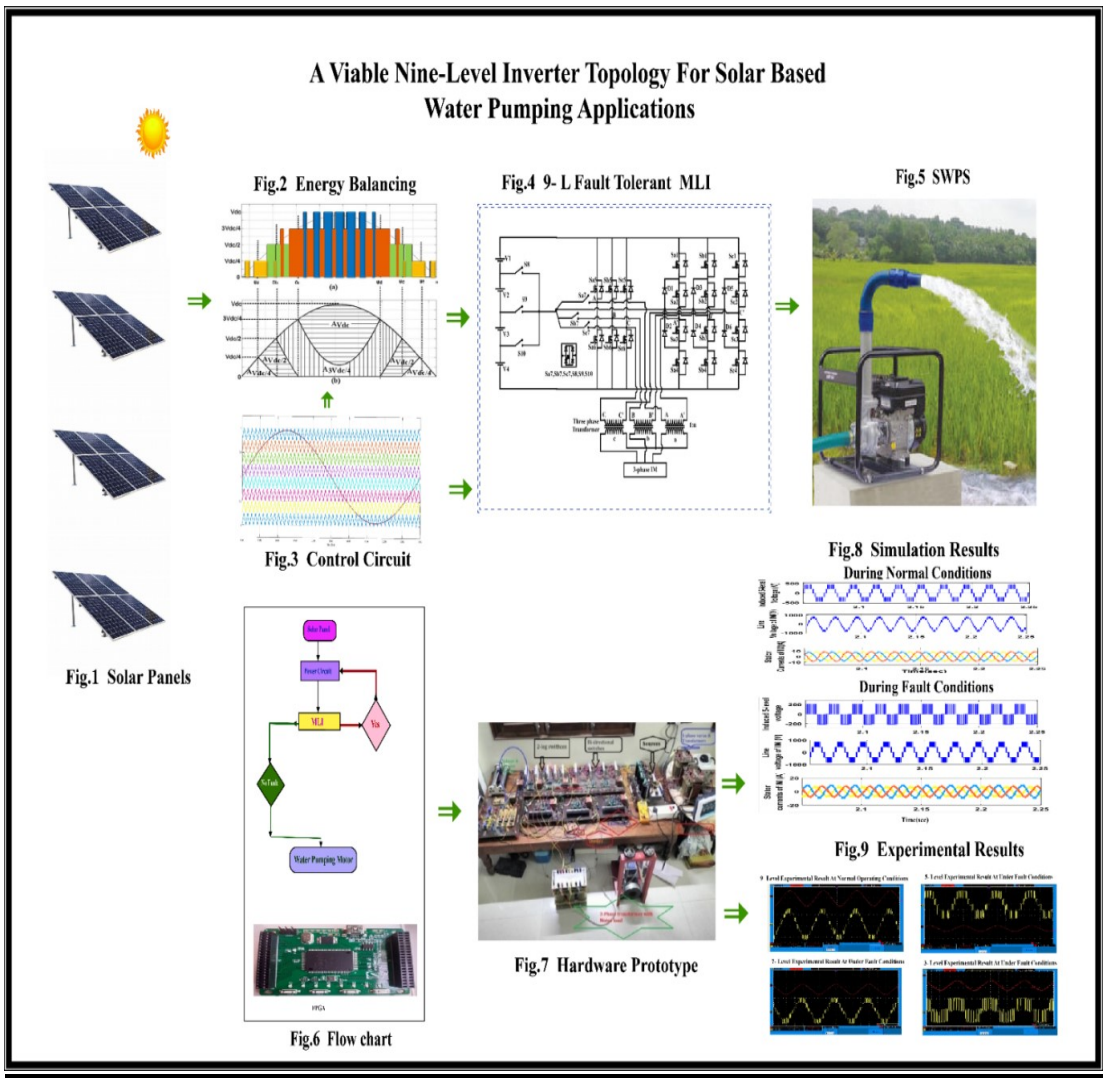


Figure 1.19 Solar Water Pumping System (SWPS) - PV Schematic

1.9 Thesis Structure Outline

This thesis puts forward energy balancing strategies that are provided for Solar P-V water pumping requirements, which can be met with the help of various multilevel inverter topologies that have fault tolerance. Fault tolerance topologies are presented in the literature; however, these topologies are limited by the additional semiconductor devices and the lack of source failure condition discussion. It is necessary to investigate Energy Balancing problems brought on by load sharing- unequally partial, shading of P-V panels, and problems with DC offset minimization.

In the second chapter of the thesis, an improved three phase five level multi-level inverter model that can withstand faults is examined and evaluated in this work. Here, a

precise comparison between the multi-level inverter and the conventional cascade inverter for solar water pumping systems. Compared to previous types of multilevel inverters, the suggested modified multilevel inverter reduces the number of gate drivers and switches. For the suggested system, a level shifted multi carrier PWM approach is employed. The proposed five-level and current five-level inverters are simulated utilizing the MATLAB platform for the thorough study. And naturally, the designed topology performed admirably as compared to the traditional.

In the third chapter of the thesis, a dynamic approach towards developing a three-phase nine level multilevel topology with fault-tolerant capability with respect to photovoltaic systems is carried on. The setup is built by utilizing 3-level and 2-level half-bridge inverters. Four individual PV strings are supported by MPPT-associated batteries and charge controllers help various voltage sources by which the proposed topology is operated. Multiple open circuit sources or switch failures are studied with respect to the current topology. In order to save the critical loads, power at low voltage is supplied when a fault condition occurs with the help of the proposed switching redundancy.

In the fourth chapter of this work, an updated fault tolerant three phase multi-level inverter is built with Energy Balancing capability with open circuit failures. Multiple voltage sources act as the primary sources in a PV application system with multi-level inverters. The state of charge difference is affected by partial shading of the panels thereby resulting in voltage difference between terminal voltages among the sources. Thus, picking the right combination of switching can lead to energy balance for the batteries of panels in every possible condition. This is done by taking into account that a battery with a low state of charge is discharged at a slow pace in order to equate the state of charge of a battery with a high initial SOC. The switching combination and the structure of the inverter give rise to the majority of the load sharing between individual voltage sources which lead to underutilization. This particular issue is tackled by proposing an optimal version of PV module distribution.

A vigorous mathematical model is developed for the efficient sharing of the resources at respective voltage levels. An issue related to Energy Balancing is also worked on here as the complexity of the entire system is diluted with distribution at source strategy. As the voltage sources are divided, Vdc/4 is taken as the magnitude at each source that has 4 isolated voltage sources. Several PV strings help to form these DC voltage sources.

In the fifth chapter the functioning of this proposed, fully realized MLI inverter is carried out at various open circuit switch failures. “MATLAB/SIMULINK” are used to present these topologies and are realized and tested in real-time by hardware prototype.

CHAPTER 2

FAULT TOLERANT ABILITY OF A FIVE LEVEL INVERTER FED THREE-PHASE INDUCTION MOTOR FOR WATER PUMPING APPLICATIONS

2.1 Introduction

Non-renewable resources have been acting as the major sources of production of energy for mankind since the day they were discovered. However, the reliability factor of these sources has significantly dropped down in the past couple of decades as they are bound to be. Both lack of abundance and their adversely inclined effect on the environment. These fossil fuels when subjected to various chemical processes also result in undesirable shortcomings. Thus, the usage of these fossil fuels for mere production of energy at the cost of destroying life on the planet is nothing but a no brainer. Nevertheless, one strong alternative for the mankind to gravitate towards comes in the form of Solar energy and other non-renewable sources of energy. [55] A research by Kishta [56] describes the sustainable nature of the usage of renewable energy sources like Solar, wind, geothermal and biomass energy as a part of the new-age substantial solution for energy production.

Multi-level inverter is designed to be applicable with respect to AC motor drives. Thus, fault tolerant capability of a multilevel inverter is growing to be a primary characteristic [57]. Primary characteristics like reliability, desideratum and prominence of power converters are discussed in [58], [59]. Gate driver failure and semiconductor failures lead to inverter failures in general [60]. Open-circuit and short-circuit fault lead to semiconductor failures. High temperature, wrong gate voltage and over voltage often result in short-circuit fault.

To address the above issues, in this chapter three phase five level inverter is presented for solar water pumping applications. A five-level fault tolerant Topology is showed in the figure 2.1. MPPT charge controller & batteries in association with 2 PV arrays form two dc links are fed to this configuration. The power rating of these DC links are as half as the generalized single PV generation system. As the system is now a

combination of two individual PV arrays, the voltage rating of switches is reduced thus making the system fault tolerant.

2.2 System operation and configuration

A five-level fault tolerant Topology is showed in the figure 2.1. MPPT charge controller & batteries in association with 2 PV arrays form two DC links are fed to this configuration. The power rating of these DC links are as half as the generalized single PV generation system. As the system is now a combination of two individual PV arrays, the voltage rating of switches is reduced thus making the system fault tolerant.

Figure 2.2 describes the power-circuit in which inverter is being provided by two separable equal DC sources, i.e., V1=V2=0.5V_{dc}. The inverter structure is designed by cascading two-level inverter and 3-level diode clamped multi-level inverter. The four quadrant switches are joined between neutral points of two DC sources to each phase of 2-level inverter as shown in Figure 2.2. During faulty conditions, bidirectional switches come into play as they generate intermediate voltage levels. In order to generate five-level voltage, the primary of open-end winding transformer is fed with each phase of neutral point clamped inverter and two-level inverter. Secondary end of the open-end winding transformer is connected with a load. Table 2-1 shows us the switching combination used to generate 5-level voltage of a phase. B & C phases also have the same switching combinations.

Table 2-1 Accurate Switching Composition for Five-Level Operation

Voltage Magnitude	Switches to turn ON
Vdc	S_{a1}-S_{a2}- S_{a7}
Vdc/2	S_{a1}-S_{a2}- S_{a5}
0	S_{a1}-S_{a2}- S_{a6}
-Vdc/2	S_{a3}-S_{a4}- S_{a5}
-Vdc	S_{a6}-S_{a3}- S_{a4}

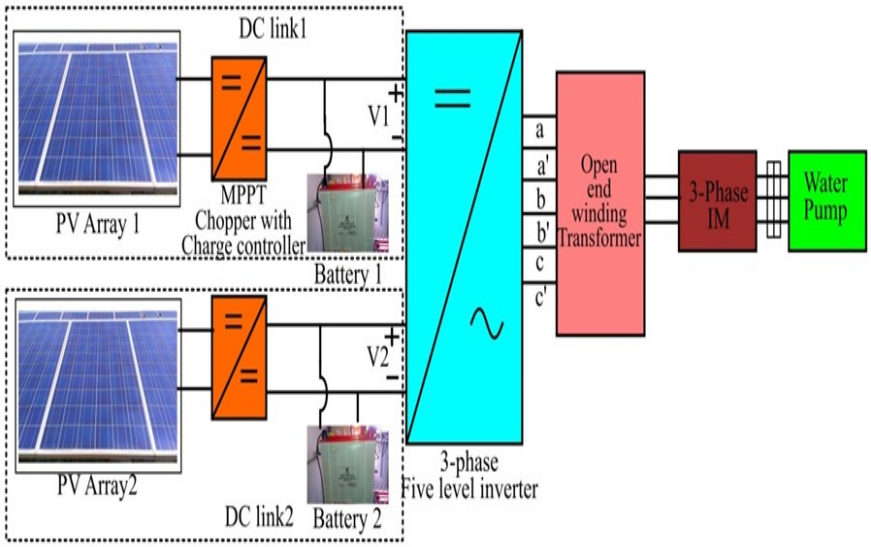


Figure 2.14 The illustration of Multi-level inverter fed water pumping system.

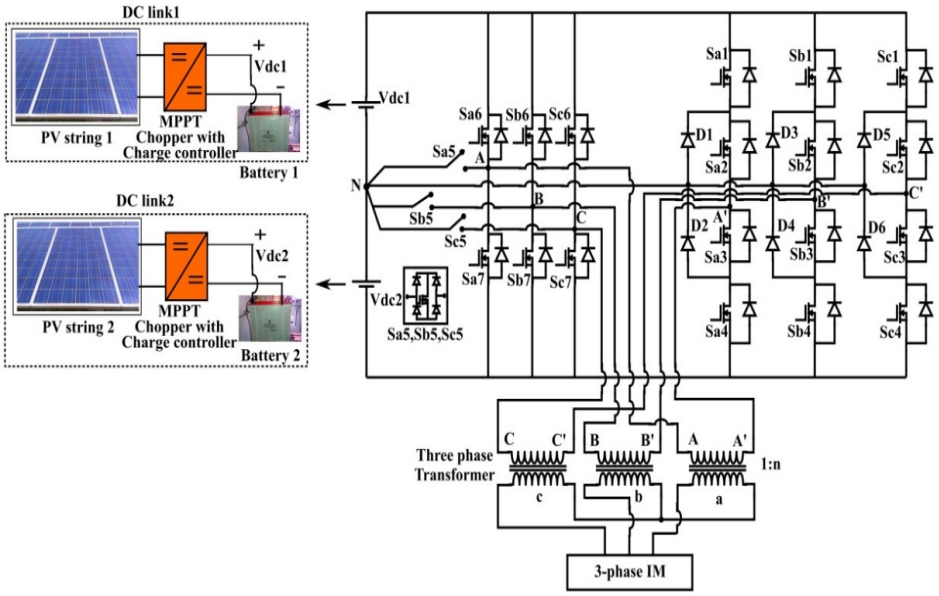


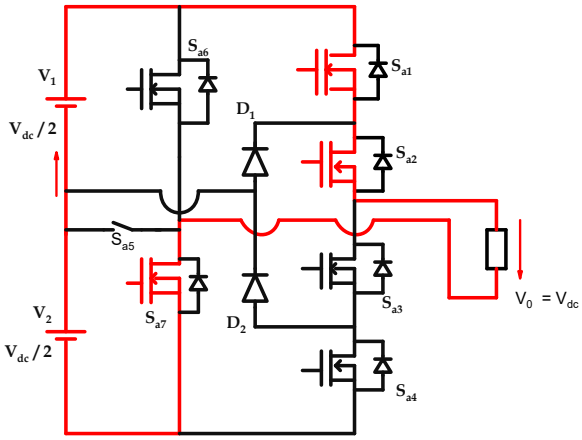
Figure 2.15 Schematic circuit of 3-phase five-level inverter configuration pumping system.

Table 2-2 valid switching composition to produce 3-Level Voltage In Fault Condition

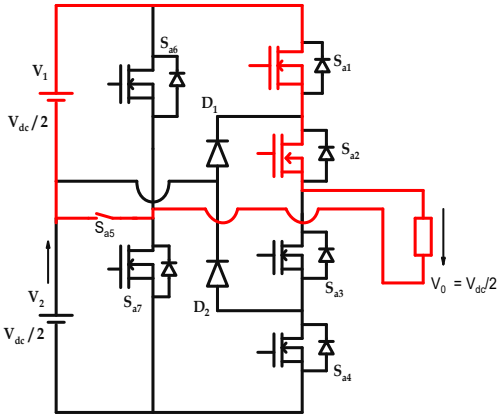
Voltage Magnitude	Direction of Current path and switches to turn ON
Case-A Source V2short-circuit or open fault and/orS_{a4} or/and S_{a7} Switch Open-fault	
Vdc/2	S_{a1}-S_{a2}- S_{a5}
0	S_{a2}-S_{a3}- S_{a6}
-Vdc/2	S_{a6}-S_{a3}- S_{a2}
Case-B Source V1short-circuit or open faultand/orS_{a1} or/and S_{a6} Switch Open-fault	
Vdc/2	S_{a2}-S_{a3}- S_{a7}
0	S_{a2}-S_{a3}- S_{a6}
-Vdc/2	S_{a3}-S_{a4}- S_{a5}
S_{a6} and S_{a7} Switch Open-fault	
Vdc/2	S_{a1}-S_{a2}- S_{a5}
0	S_{a2}-S_{a3-} S_{a5}
-Vdc/2	S_{a3}-S_{a4}- S_{a5}
S_{a5}Switch Open-fault	
Vdc	S_{a1}-S_{a2}- S_{a7}
Vdc/2	S_{a2}-S_{a3}- S_{a7}
0	S_{a2}-S_{a3}- S_{a6}
-Vdc/2	S_{a6}-S_{a3}- S_{a2}
-Vdc	S_{a6}-S_{a3}- S_{a4}

2.2.1 Fault tolerant five-level inverter modes of operation:

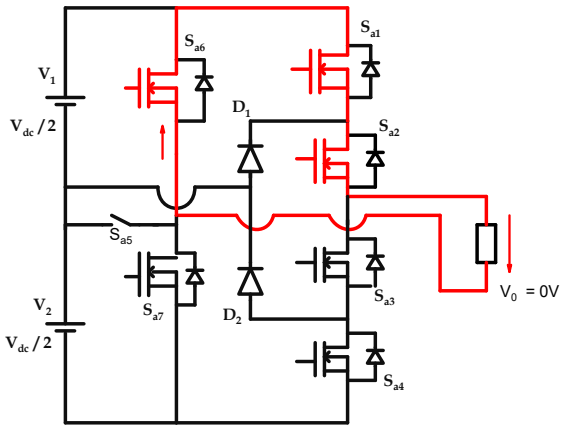
The block diagram of the proposed fault tolerant three phase five-level inverter circuit is shown in Fig.2.2



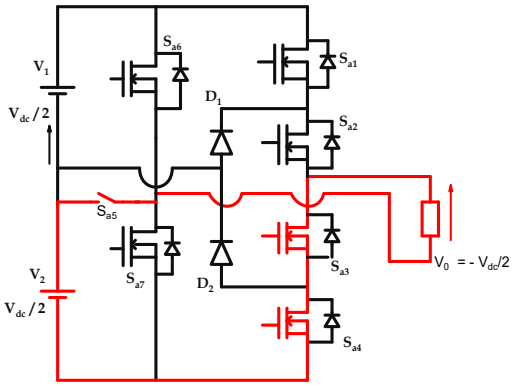
Mode-1 (a)



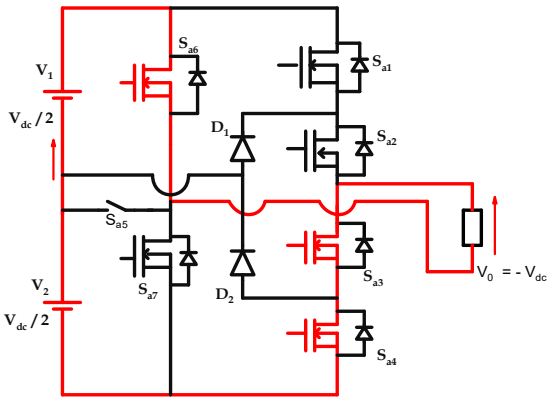
Mode-2 (b)



Mode-3 (c)

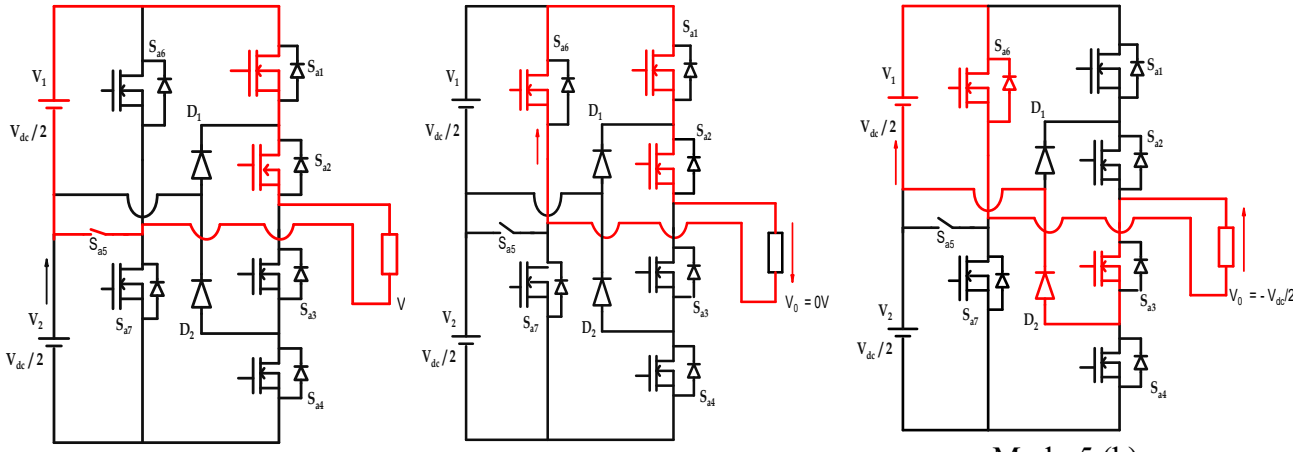


Mode-4 (d)



Mode-5 (e)

Fig. 2.3 (a) Current flow paths working state of five-level inverter each voltage level under normal operation



Mode-6 (f) Mode-7 (g) Mode-5 (h)

Fig. 2.3 (b) Current flow paths working state of five-level inverter each voltage levels under Sa4 switch fault operation

For better understanding, the topology is supplied by two equal dc links Vdc1 and Vdc2, respectively. It is known that a leg of a three-level inverter is capable of generating voltage levels of Vdc1, 0, and − Vdc2; similarly, the two-level half bridge inverter can generate two voltage levels with magnitudes of Vdc1 and − Vdc2. As a result in combining both, the total effective voltage across the load will have a total of five voltage levels with magnitudes of +(Vdc1 + Vdc2), Vdc1, 0, − Vdc2, and − (Vdc1 + Vdc2). If two dc links are balanced to be of equal magnitude Vdc1 = Vdc2 = 0.5Vdc, then it will generate five voltage levels +Vdc, +0.5Vdc, 0, − 0.5Vdc, and − Vdc like the

conventional multilevel inverter. The switching combination for five-level voltage generation and direction of current during each voltage level under normal operation is given in Table 2.1 and illustrated in Fig. 2.3(a) (a)–(e). Whereas Fig. 2.3(b) from (a)–(h) under Sa4 switch fault operation. The switch Sa5 provides switching redundancy for voltage levels 0.5Vdc , 0, and − 0.5 Vdc which can help in the energy sharing between two sources due to partial shading on one side of the PV panels which is discussed in next chapter. The inverter structure is formed by combining three phase two-level inverter, three-level neutral point clamped inverter and bidirectional switches. The inverter is fed with two individual DC links which consists of PV strings with MPPT charge controller and associated batteries. The total rated power is divided into halve among two PV strings. The configuration has a common connection point 'N' between sources Vdc1 and Vdc2. The bidirectional switches are connected between common connection point and two-level inverter as depicted in Fig.2.1. Phase A of two-level inverter and A' of diode clamped inverter are connected to three phase transformer winding A-A' to generate five-level voltage as shown in Fig.2.2. Similarly other phases are connected between B-B' and C-C'. The secondary side of transformer is connected in star to supply three phase or single phase loads.

The additional advantage of bidirectional switch Sa5 is to continue the operation of the inverter as three level in case of switch or source failure, which is discussed in detail at the later part of this section. From the proposed converter, it can be observed that the maximum voltage rating of the switching devices Sa1–Sa7 is 0.5Vdc, and for Sa5 is Vdc. In Table 2.1, if Sax = 1 switch is on, Sax = 0 switch is off, where x = 1, 2. . . 7., x refers to a, b, c phases.

Driver circuit failure, semiconductor device open and short circuit faults and source failure are generally the causes for inverter failures. Here, focus on source failure & switch open-circuit faults are discussed. An open circuit fault in a semiconductor switch occurs due to cracking and lifting of wires. Cracking and lifting of bonds in semiconductor devices refer to physical damage that affects the electrical interconnections within the device, typically caused by mechanical stress, thermal cycling, or material fatigue. In most cases, cracking and lifting of bonds lead to open

circuit failures because the broken or lifted bond interrupts the flow of current through the intended paths in the semiconductor device.

Table 2-2 gives us the types of failure combinations & 3-level generation on the major side of transformer. In analogy with Table 2-1, the b & c phases under switch open-circuit fault are also similar in Table 2-2. The given system is compared with conventional multilevel inverters is presented in Table 2-3. The proposed system is advantageous with respect to the quantity of components, capacitor balancing issues and fault tolerance compared to conventional topologies.

Table 2-3 Comparison of Proposed system Configuration

Inverter Type	NPC	FC	H-bridge	Proposed system
Semiconductor devices	24	24	24	21
Diodes	18	0	0	12
DC capacitors/ Isolated power supplies	4	4	6	2
Capacitors	0	18	0	0
Fault tolerant	No	No	Not fully tolerant	Yes

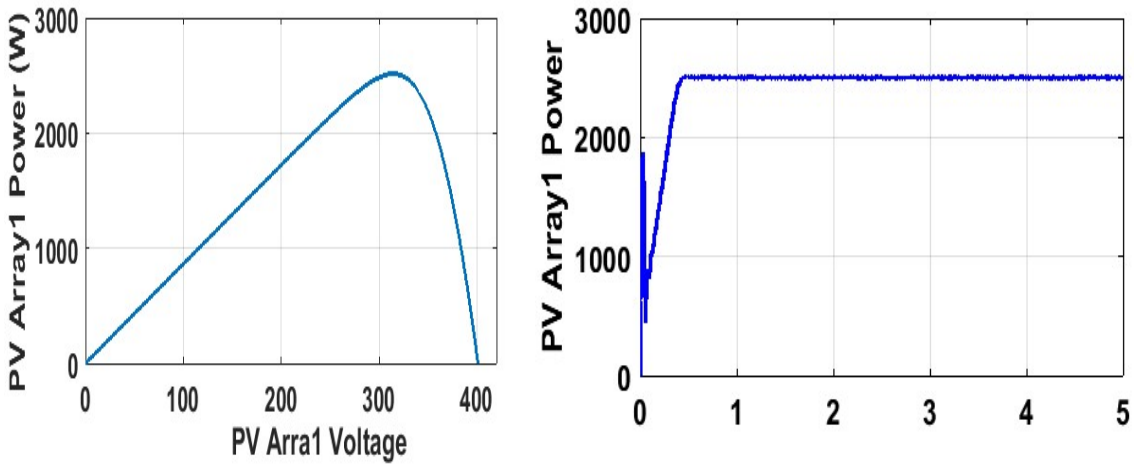
2.3 Simulation Results and Analysis

MATLAB is the software that is used to simulate the proposed 3-phase five-level inverter Topology. Table 2-4 shows us the parameters considered for simulation. The modelling of PV array and perturb and observe maximum power point algorithm is executed using [61]. For controlling the inverter the technique of Phase disposition pulse width modulation (PDPWM) is used. The comparison between modulating signal and 4-carrier signal to generate five-level output voltage using switching combinations is shown in Table 2-1. In the event of failure of semiconductor device or source the signal used to modulate will be attached with two carriers in order to produce three-level voltage.

Table 2-4 Parameters for Simulation

PV Arra1 & 2 Maximum power	2.5KW
Irradiation	1000W/m^2
Temperature	25^0C
Rated DC voltage	Vdc1=Vdc2=215V
Frequency of Modulating signal	f_m=50Hz
Frequency of Carrier Signal	f_s=2KHz
Modulation-index	m_a=0.98
Type of Load	3-Phase Induction Motor, 415V,1480 rpm

The whole systems modelled in Matlab Simulink and perturb and observe process is used to track the maximum power. The power versus voltage characteristic and maximum power output is shown in Figure 2.4. It is similar for PV array2.



(a) (b)

Figure 2.4 (a) P vs V Characteristic of PV Array1 (X axis:100v/div, Y:1000W/div) (b) Maximum power of PV Array1 (X axis:1 sec /div, Y:1000W/div)

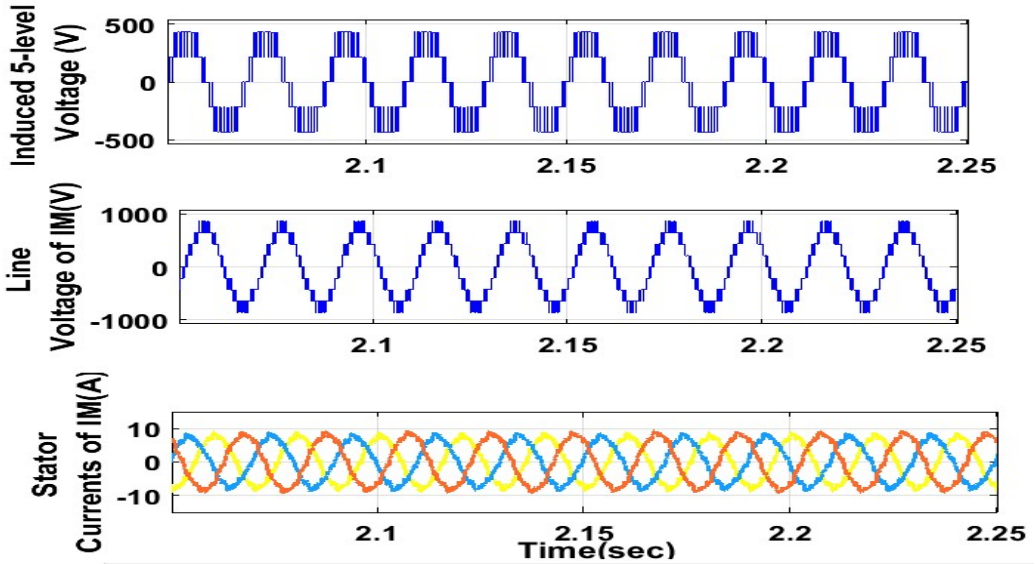


Figure 2.5 From Top: The five-level voltage of primary side, line voltage of IM and stator currents of IM (Y axis:10A/div, 1000V/div,500V/div X:0.05sec/div)

The 5-level potential difference induced across the winding that is primary to the transformer, induction motor line voltage & stator currents are displayed in Figure 2.5. The speed and torque of induction motor are shown in Figure 2.6 during normal operation. The three-level voltage of primary side winding of transformer, the induction motor stator voltage and currents are shown in Figure 2.7 during open-circuit fault occurred in Sa4. The output voltage is maintained constant during fault by reducing the number of turns of transformer to halve. The unaltered speed and torque are presented in Figure 2.8 during switch Sa4 failure.

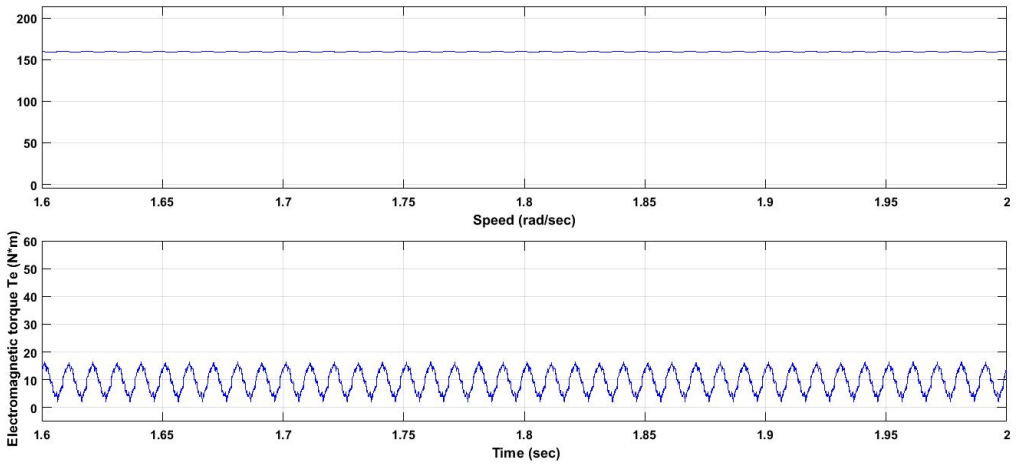


Figure 2.6 From Top: The Speed and Torque of IM under normal conditions (Y axis: 1000rpm/div, 100N-m/div X:1sec/div)

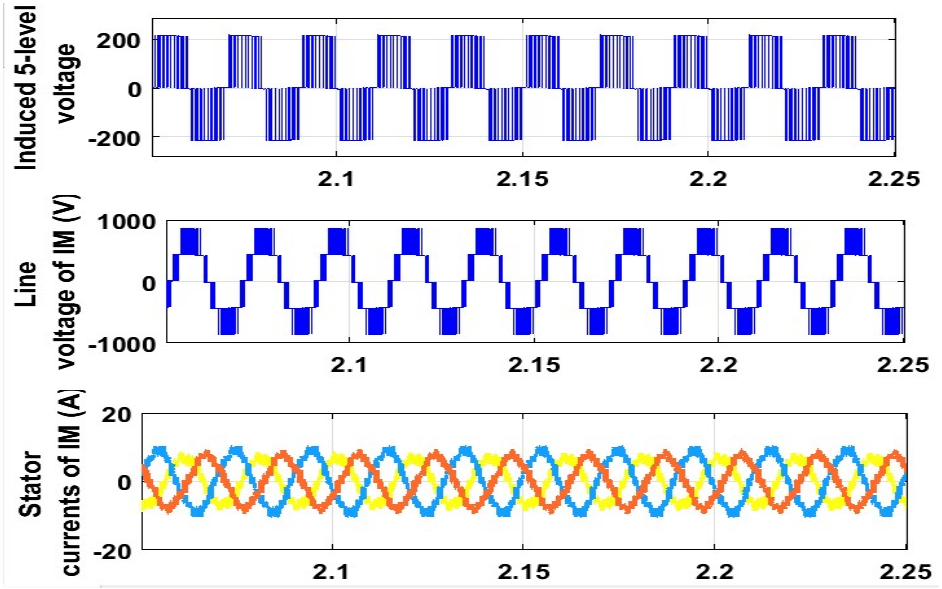


Figure 2.7 From Top: The 3-level voltage across primary winding, line voltage of IM and stator currents of IM during fault (Y axis:20A/div, 1000V/div,200V/div X:0.05sec/div)

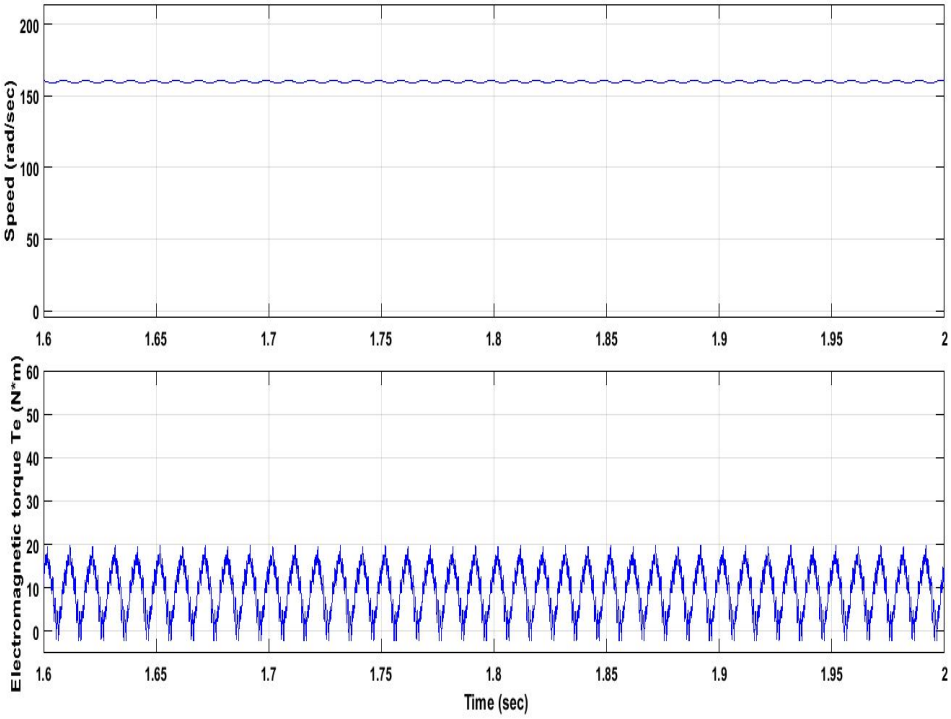


Figure 2.8 From Top: The Speed and Torque of IM under fault conditions (Y axis: 1000rpm/div, 50N-m/div X:1sec/div)

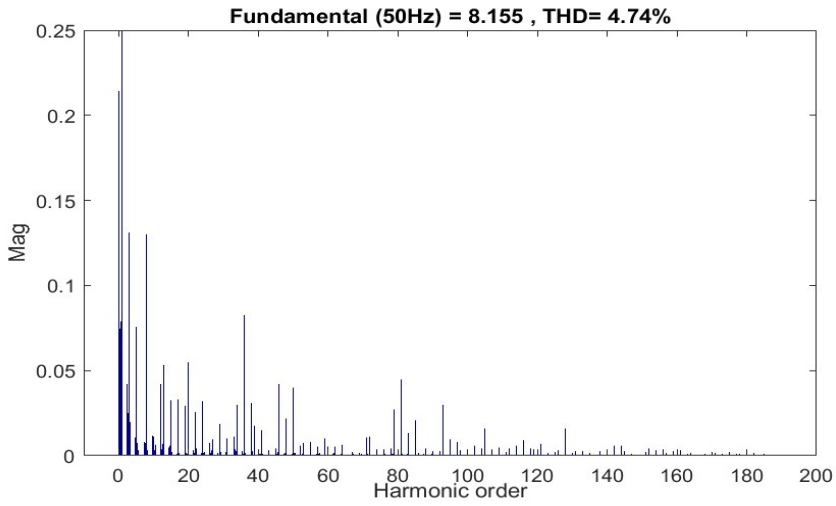


Figure 2.9 Total Harmonic Distribution of 5-Level inverter

Using the PD-PWM technique, Figure 2.9 displays the Total Harmonic Distortion (THD) of 5-Level inverter for phase (a) of the inverter current. It is evident that the THD for the inverter current is 4.74%, which is below the IEEE standards' allowable THD limits for water pumping applications of 5%.The circuit connection and output of the simulation are displayed in Figures 2.6, 2.7, 2.8, and 2.9, respectively. Therefore, in order to obtain a perfect sinusoidal wave while using these MLI topologies for water pumping applications, we must connect a filter with the proper design at the MLI's output

2.4 Comparison of Five-level and Nine-level fault-tolerant inverters

(a) Tolerance for faults

Five-level fault-tolerant inverters are capable of managing a single switch or H-bridge leg failure. When a single-switch open circuit fault occurs, 9-level fault tolerant inverters can produce three or five levels.

(b) Paths those are redundant

In the event that a switch fails, 5-level fault tolerant inverters can help the circuit achieve the necessary voltage by adding redundant routes to each output voltage level.

(c) Device switching

Compared to traditional T-type multilevel inverters, 5-level fault tolerant inverters may contain fewer switching devices. There can be fewer switches in 9-level fault-tolerant inverters.

(d) Efficiency

Up to 97% efficiency can be achieved using 5-level fault-tolerant inverters.

(e) Voltage output

Nine levels can be created in the output of 9-level fault-tolerant inverters.

Due to their benefits, which include lower overall harmonic distortion, fewer losses, and lower voltage transients, multilevel inverters are frequently utilized in industry. On the other hand, adding more power switching devices may make faults more likely and lower system dependability.

2.5 Summary

In this chapter, a 5-level MLI fault-tolerant topology is proposed for solar water pump applications. The notable achievements of the proposed topology are the adaptation to the failure of semiconductor switches. The correlation between the modified inverter and the traditional multi-level inverter is demonstrated effectively. The MATLAB software was used to simulate a cascaded H-bridge MLI with equal voltage sources. This study shows where the proposed inverter is a better decision for solar water pump applications. The fault tolerance of the Topology is confirmed by simulation results.

The fault tolerant multilevel inverters are focused on the development of reduced switch count and fault tolerant capabilities. In the following chapter proposes a new fault-tolerance 9-leve MLI. The proposed FT topology can with stand both single and multiple switch failures.

CHAPTER 3
FAULT TOLERANT NINE-LEVEL INVERTER TOPOLOGY FOR SOLAR WATER PUMPING APPLICATIONS

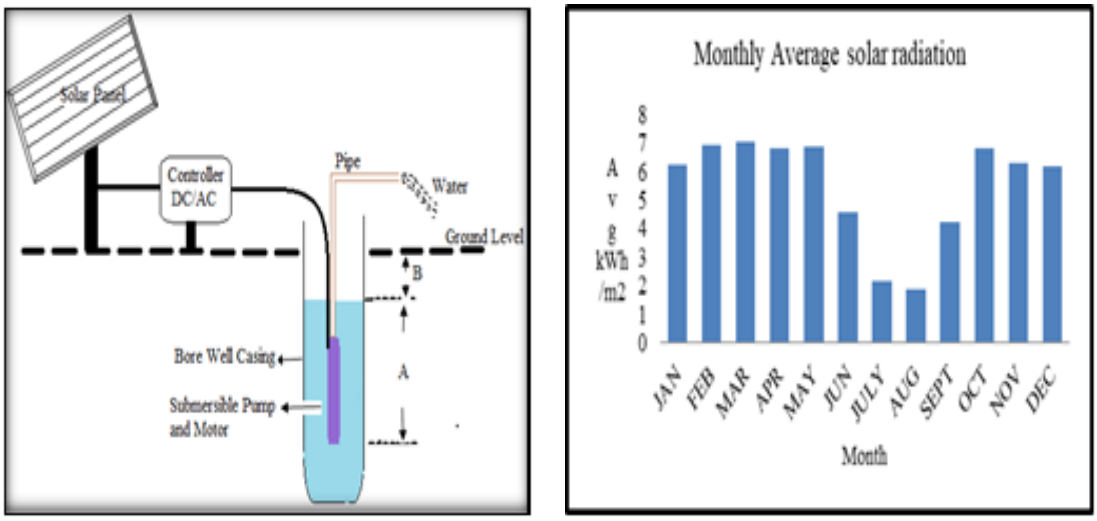
3.1 Introduction

A multi-level inverter (MLI) is the acts as the source for powering a 3-Φ induction motor that is utilized in agricultural works. Any failure of MLI leads to a total shutdown of the system. Thus, addressing the failure of a MLI leads in effective working and makes the system less prone to shutdowns. The proposed fault-tolerant ability provides uninterrupted, quality power supply with less total harmonic distortion (THD) and helps in the functioning of the induction motor used. Nowadays, there are advanced progress in applying computing technologies [62-68] that have significant progress in different techniques.

To address the above issues a 9-level inverter is employed to feed power to an induction motor for pumping applications. The proposed nine-level fault tolerant ability is a new contribution. To address the mentioned issues a new nine-level inverter is modelled to incorporate the fault tolerant ability. As per the literature survey there are no solutions for dealing with the faults occurring in the functioning of a MLI fed induction motor drives for water-pumping application.

The particular Topology has the benefits in terms of switch and sources failures, requires less components and not having neutral point and capacitor voltage balancing issues compared to conventional multilevel inverters. Average operating modulation index and equivalent load demand are the factors on which PV modules are divided. For better source utilization, the ratings of the battery are confirmed with respect to the newer source ratings. Phase disposition pulse width modulation (PDPWM) is used to produce the control signals for the switches to generate nine level voltages. The total system is simulated using MATLAB.

3.2 Conventional Solar Water Pumping System Configuration



(a) (b)

Figure 3.1 (a) PV water pumping system, (b) Average Solar radiation intensity (Monthly)

The system operates on power generated using solar PV (photovoltaic) system. The photovoltaic array converts the solar energy into electricity, which is used for running the motor pump set. The pumping system draws water from the open well, bore well, stream, pond, canal etc. The system requires a shadow-free area for installation of the Solar panel. The block diagram of existing photovoltaic based three phase induction motor-pump system for irrigation system and monthly average solar radiation is shown in Figure 3.1 (a) & (b).

3.3 Solar Water Pumping System Configuration with Fault Tolerant Ability

The overview of the fault tolerant nine-level inverter is shown in Figure 3.2.The system is fed with four separate direct current links which are formed by four separate PV arrays, equipped with batteries and Maximum Power Point Tracking charge controller. The direct current links are rated at $1/4^{th}$ of the total power rating with respect to single centralized PV generation system. The benefit of having four separate PV arrays is that it decreases voltage rating of switches and becomes fault resilient in case of any one of the array failures which is discussed in later part of this section.

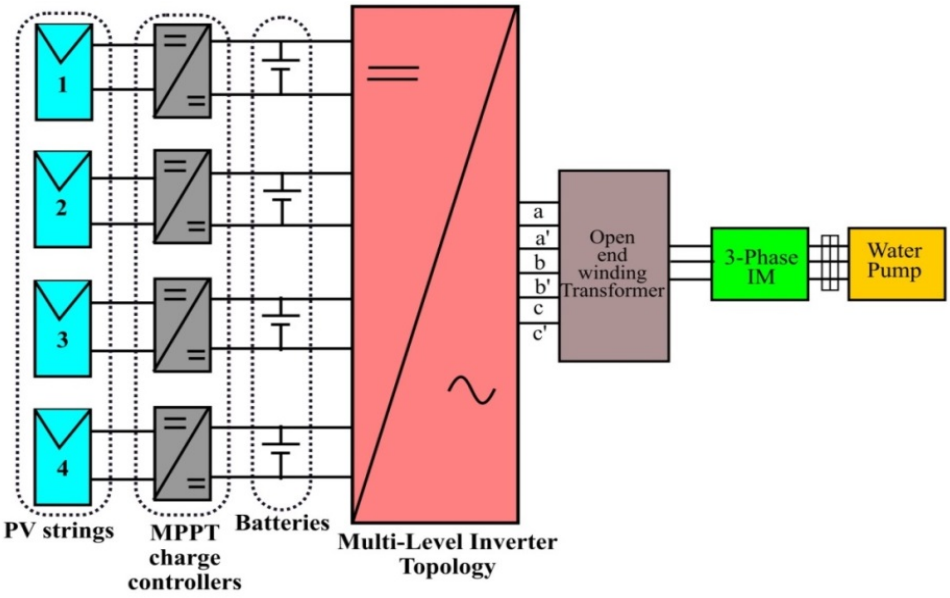


Figure 3.2 Schematic diagram of Multi-level inverter fed water pumping system

Figure 3.3 shows the power circuit in which the inverter is being supplied by four separate equal DC sources, i.e., V1=V2=V3=V4=0.25Vdc. The system is achieved by cascading 2-level inverter and 3-level neutral point clamped multilevel inverter. The four quadrant switches are connected between neutral point of four direct current links to each phase of two-level inverter as shown in Figure 3.3

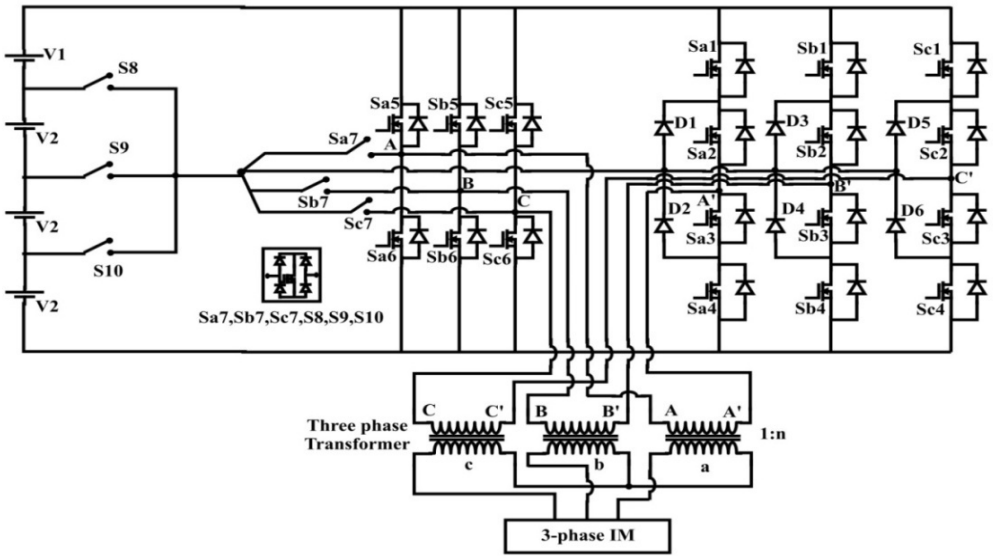


Figure 3.3 Power circuit of 3-phase nine-level inverter configuration

In Figure 3.3 the four quadrant switches are utilized used to generate intermediate voltage levels for the duration of normal and fault circumstance. Each phase of two-level inverter and neutral factor clamped inverter are given to number one of open end winding transformer to generate 9-level voltage. The induction motor is connected to the secondary aspect of open end winding transformer. The switching combination to produce nine-level voltage for a-phase is given in Table 3-1. The switching is same for b and c phases.

Table 3-1 Switching Combination For Nine-Level Operation

Voltage Magnitude	Switches to turn ON
Vdc	Sa1-Sa2- Sa6
3Vdc/4	Sa1-Sa2- Sa7- S10
Vdc/2	Sa2-Sa1- Sa7- S9
Vdc/4	Sa1-Sa2- Sa7- S8
0	Sa1-Sa2- Sa5
-Vdc/4	S10-Sa7- Sa3- Sa4
-Vdc/2	S9-Sa7- Sa3- Sa
-3Vdc/4	S8-Sa7- Sa3- Sa4
-Vdc	Sa5-Sa3- Sa4

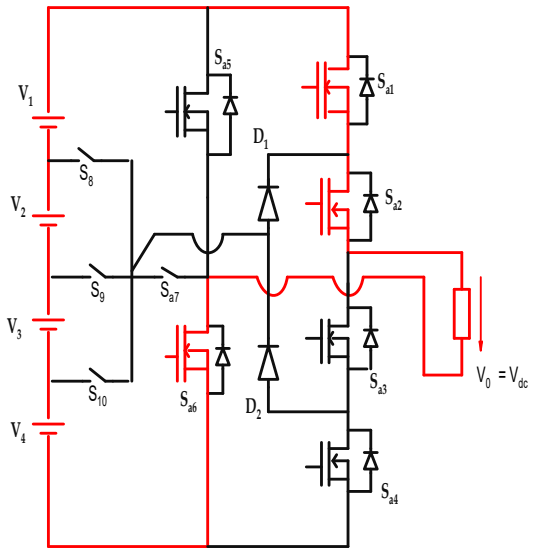
Basically, inverter failures tend to occur because of source failure, semiconductor device short and open circuit failure, and drive circuit failure. Here, both open circuit fault and source failure are discussed. Because of lifting & cracking of bonding wires in semiconductor switches reasons the open circuit fault. The unique type of failure mixtures and 3-stage voltage technology on primary side of open quit winding transformer using suitable switching for a-phase is given in Table 3-2. The switching pattern given in Table 3-2 is comparable for b and c phases under transfer open circuit fault.

Table 3-2 Switching Combination To Generate Voltage During Fault

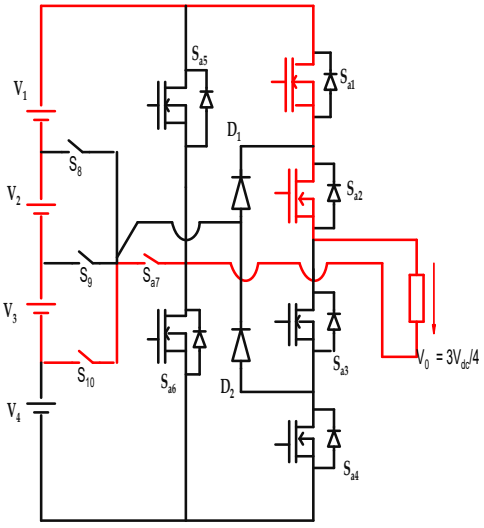
Voltage Magnitude	Direction of Current path and switches to turn on
Source V4 open or short circuit fault and/or Sa4 or/& Sa6 Switch Open fault	
3Vdc/4	Sa1-Sa2- Sa7- S10
Vdc/2	Sa2-Sa1- Sa7- S9
Vdc/4	Sa1-Sa2- Sa7- S8
0	Sa1-Sa2- Sa5
-Vdc/4	Sa5-Sa2-Sa3-Sa7-S8
- Vdc/2	Sa5-Sa2-Sa3-Sa7-S9
-3Vdc/4	Sa5-Sa2-Sa3-Sa7-S10
Source V1 open or short circuit fault and/orSa1 or/ & Sa5 Switch Open fault	
3Vdc/4	S8-Sa2- Sa3- Sa6
Vdc/2	S9-Sa2- Sa3- Sa6
Vdc/4	S10-Sa2- Sa3- Sa6
0	Sa3-Sa4- Sa6
-Vdc/4	S10-Sa7- Sa3- Sa4
- Vdc/2	S9-Sa7- Sa3- Sa4
-3Vdc/4	S8-Sa7- Sa3- Sa4
Sa5 & Sa6 Switch Open fault	
3Vdc/4	Sa1-Sa2- Sa7- S10
Vdc/2	Sa2-Sa1- Sa7- S9
Vdc/4	Sa1-Sa2- Sa7- S8
0	Sa2-Sa3- Sa7
-Vdc/4	S10-Sa7- Sa3- Sa4
- Vdc/2	S9-Sa7- Sa3- Sa4
-3Vdc/4	S8-Sa7- Sa3- Sa4

3.3.1 Fault tolerant nine-level inverter modes of operation:

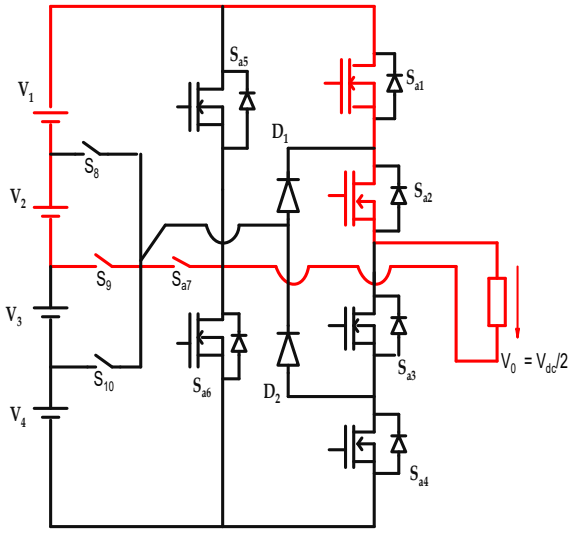
The block diagram of the proposed fault tolerant three phase nine-level inverter circuit is shown in Fig.3.3



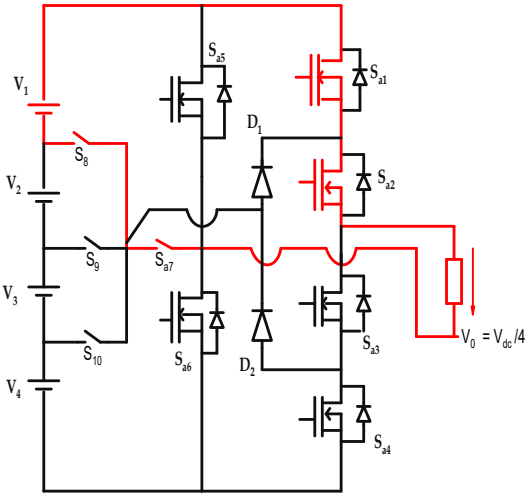
Mode-1 (a)



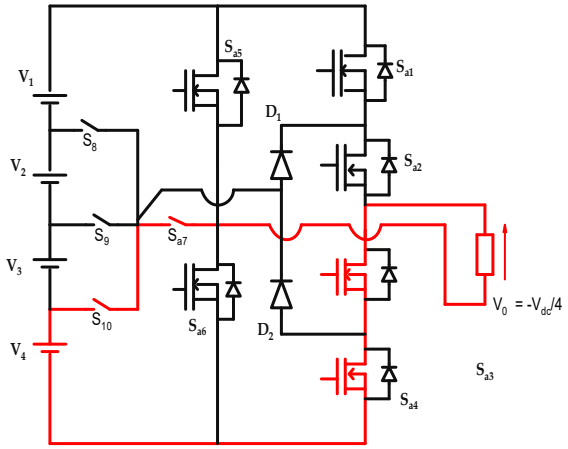
Mode-2 (b)



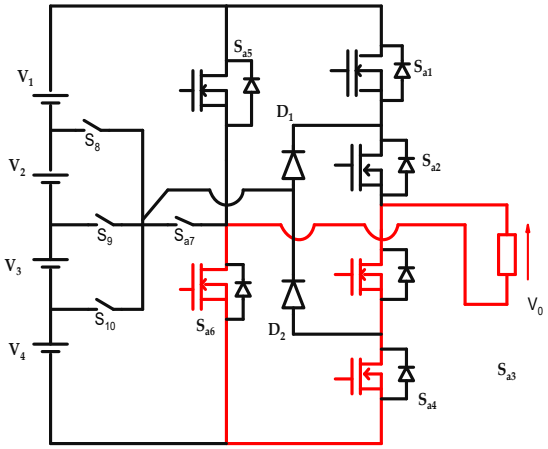
Mode-3 (c)



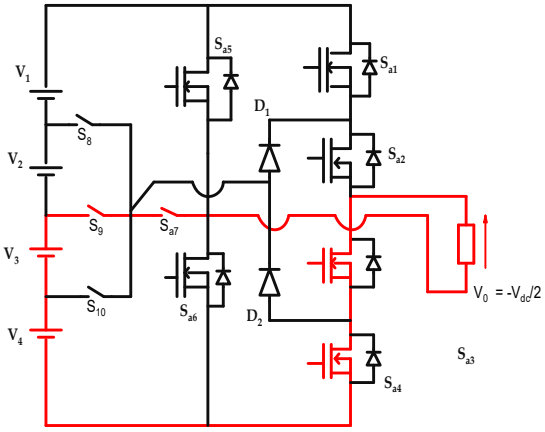
Mode-4(d)



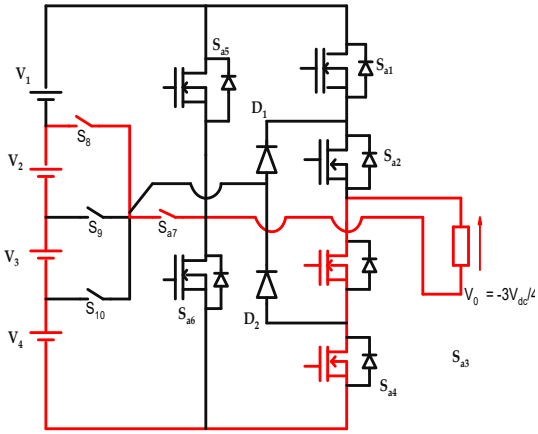
Mode-5 (e)



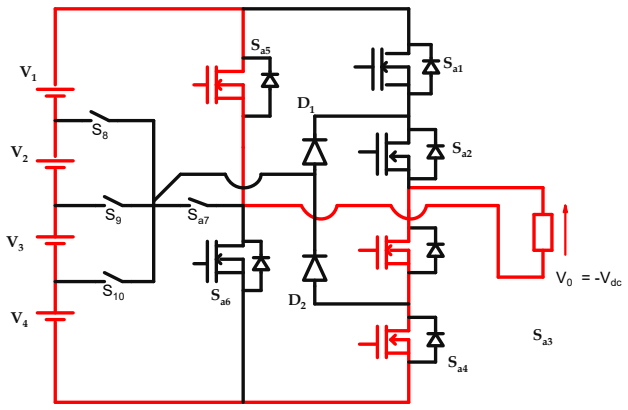
Mode-6 (f)



Mode-7 (g)

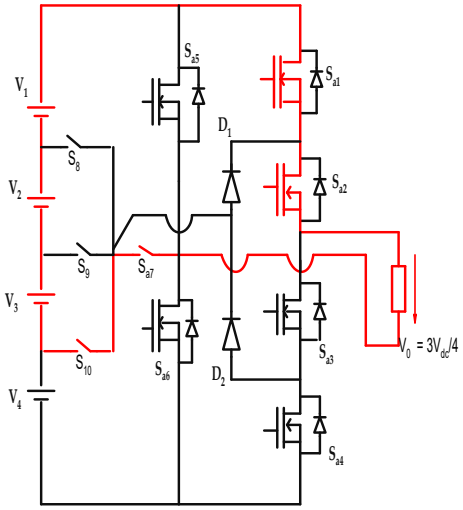


Mode-8 (h)

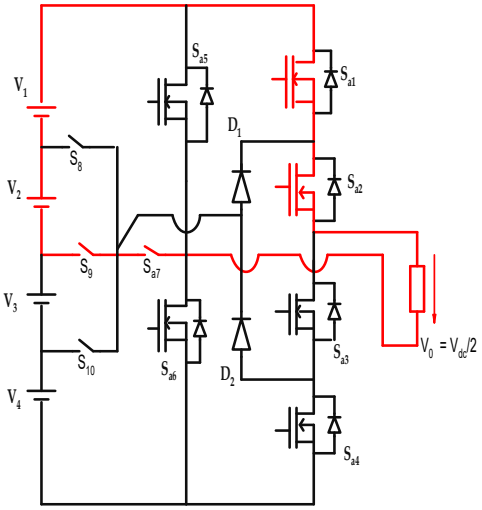


Mode-9 (i)

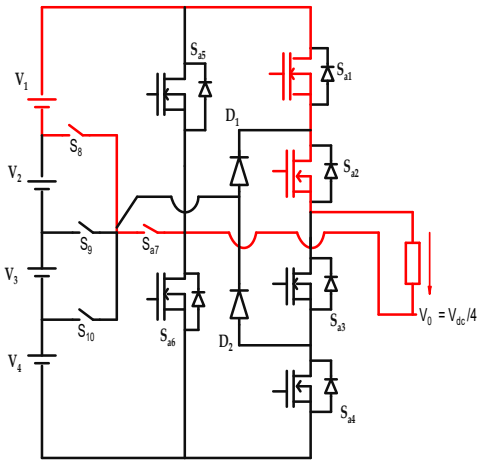
Figure. 3.4 (a) Current flow paths and working state of nine level inverter per phase circuit diagram under normal operating conditions



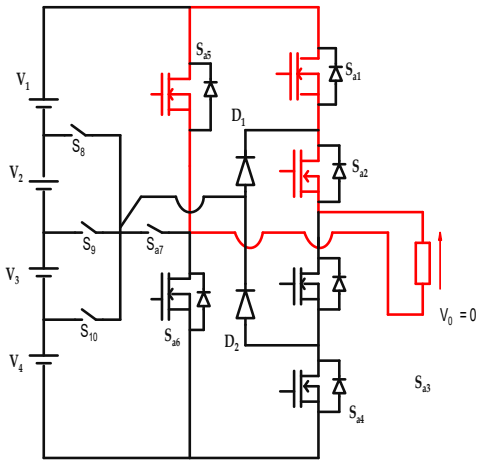
Mode-1 (j)



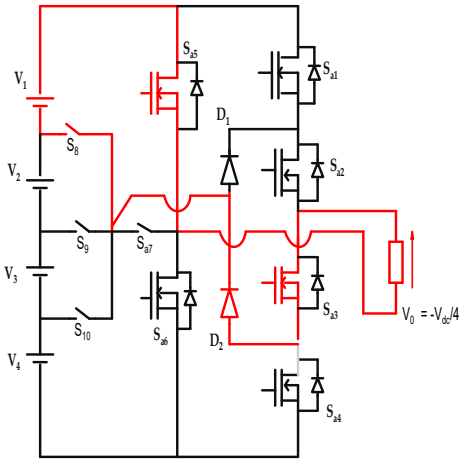
Mode-2 (k)



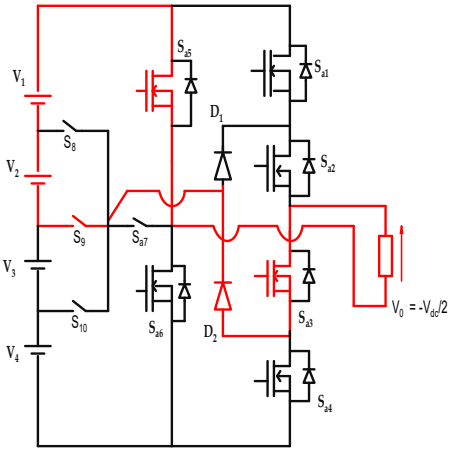
Mode-3 (l)



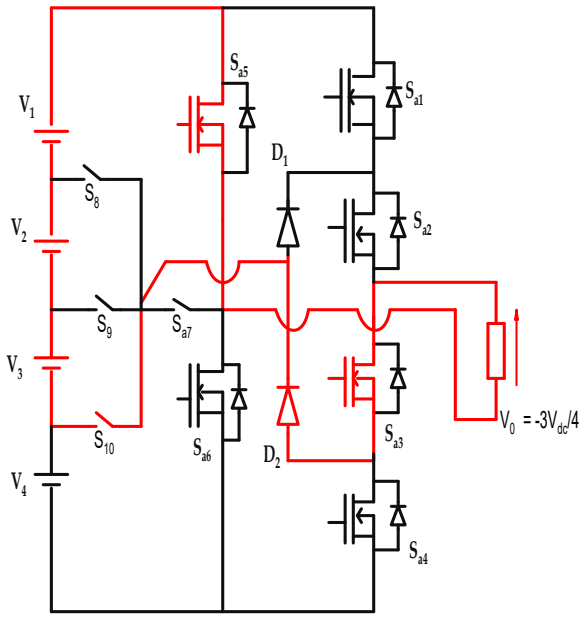
Mode-4 (m)



Mode-5 (n)



Mode-6 (o)



Mode-7 (p)

Figure. 3.4(b) Current flow paths and working state of nine level inverter per phase circuit diagram under Sa4 fault operating conditions

The suggested inverter's modes of operation The main functions of the suggested new 3-phase, 9-level inverter are described in Fig 3.4 (a) & (b) a variety of modes that generate nine different voltage levels and indicate which way current flows from the source to the load. Table 3-1 shows the switching configuration for producing nine-level output voltages while operating normally, or without fault. The nine operational modes include.

Mode 1: A load voltage of Vdc volts is produced by the combination of the Sa1-Sa2-Sa6 switches after the other switches have been inactivated and enabled to activate. When all four voltage source modules are added together, the maximum voltage across the load is produced. An active circuit's operation with the direction of current flow is depicted in Figure 3.4(a).

Mode 2: A load voltage of 3Vdc/4 volts is produced by the combination of the Sa1-Sa2-Sa7-S10 switches after the other switches have been inactivated and enabled to activate. When three voltage sources are added, the voltage across the load has a middle

magnitude. An active circuit's operation with the direction of current flow is depicted in Figure 3.4(b).

Mode 3: A load voltage of Vdc/2 volts is produced by the combination of the Sa2-Sa1-Sa7-S9 switches after the other switches have been inactivated and enabled to activate. Two voltage sources are present, which results in a low magnitude of voltage across the load. An active circuit is operation with the direction of current flow is depicted in Figure 3.4 (c).

Mode 4: A load voltage of Vdc/4 volts is produced by the combination of the Sa1-Sa2-Sa7-S8 switches after the other switches have been inactivated and enabled to activate. An active circuit is operation with the direction of current flow is depicted in Figure 3.4(d).

Mode 5: The action of all the switches combined produces a load voltage of zero volts when the remaining switches are inactivated and the Sa1-Sa2-Sa5 switches are enabled to activate. All of the switches short out with respect to the load, resulting in zero voltage across the load. An active circuit is operation with the direction of current flow is depicted in Figure 3.4 (e).

Mode 6: Following the inactivation of the remaining switches and the activation of the S10, Sa7, Sa3, and Sa4 switches, the combination of the switches produces the load voltage, which is equal to -Vdc/4 volts. Because there are two voltage sources present, a low magnitude of voltage is produced across the load with negative polarity. An active circuit is operation with the direction of current flow is depicted in Figure 3.4 (f).

Mode 7: The load voltage, which is equivalent to -Vdc/2 volts, is produced by the combined action of the S3, S4, S5, and S7 switches after the other switches have been inactivated and allowed to function. A medium-sized voltage is produced across the negatively polarized load when two voltage sources are included. An active circuit is operation with the direction of current flow is depicted in Figure 3.4 (g).

Mode 8: A load voltage of -3Vdc/4 volts is produced by the combination of the S9, Sa7, Sa3, and Sa4 switches after the other switches have been inactivated and enabled

to activate. Because all three voltage source modules are included, the load with negative polarity generates the highest voltage magnitude. An active circuit is operation with the direction of current flow is depicted in Figure 3.4 (h).

Mode 9: Following the inactivation of the remaining switches and the activation of the Sa5, Sa3, and Sa4 switches, the combination of the switches produces the load voltage, which is equal to -Vdc volts. Because all four voltage source modules are included, the load with negative polarity generates the highest voltage magnitude. An active circuit is operation in relation to the direction of current flow is depicted in Figure 3.4(i). Mode-1 (j) - Mode-1 (p) the flow of current paths under Sa4 switch open circuit conditions.

Bidirectional switch Sx7 has the added benefit of allowing the inverter to continue operating at three levels in the event of a switch or source failure; It is evident from the suggested converter that the switching devices Sa1–Sa6 have a maximum voltage rating of 0.5Vdc, whereas Sa7 and Sa8 have a maximum voltage rating of Vdc. In Table 3.2, where a = 1, 2... 7., x denotes a, b, and c phases, if Sxa = 1 switch is on, Sxa = 0 switch is off.

Table 3-3 Comparison of proposed Topology

Inverter Type	NPC	Flying capacitor	H-bridge	Proposed system
Switches	48	48	48	24
Diodes	144	0	0	24
DC capacitors/ Isolated power supplies	8	8	12	4
Capacitors	0	72	0	0
Fault tolerant	No	No	Not fully tolerant	Yes

The given system is compared with conventional multilevel inverters is presented in Table 3-3. The proposed system is advantageous in terms of number of components, capacitor balancing issues and fault tolerance compared to conventional topologies.

3.4 Simulation Results and Analysis

The three phase nine-level inverter Topology presented here is simulated using MATLAB Simulink. The parameters for simulation are given in Table 3-4. Phase disposition pulse width modulation (PDPWM) is used to control the inverter. In PDPWM the modulating signal is compared with 8-carrier signal depicted in Figure.3.5 to generate nine-level output voltage using switching combination given in Table 3-4. The logic to generate nine level voltages can be observed from Table 3-5. In case of fault the seven level voltages can be generated by changing the modulation index to 0.75 and can be compared with middle six carrier signals and Table 3-2 can be used for seven level voltage generation.

Table 3-4 Parameters for Simulation

PV Arra1,2,3 and 4 Maximum power	2.5KW
Irradiation	1000W/m^2
Temperature	25^0C
Rated Lead acid battery voltage	Vdc_1=Vdc_2=Vdc_3 = Vdc_4=96V
Modulating wave frequency	f_m=50Hz
Switching frequency	f_s = 2kHz
Modulation index	m_a=0.98
Load	3-Phase Induction Motor, 415V,1480 rpm

The whole systems modeled in Matlab Simulink and perturb and observe algorithm is used to track the maximum power [61]. The power versus voltage characteristic of PV array1 and maximum power output is shown in Figure 3.6. The induced nine-level voltage is shown in Figure 3.7.

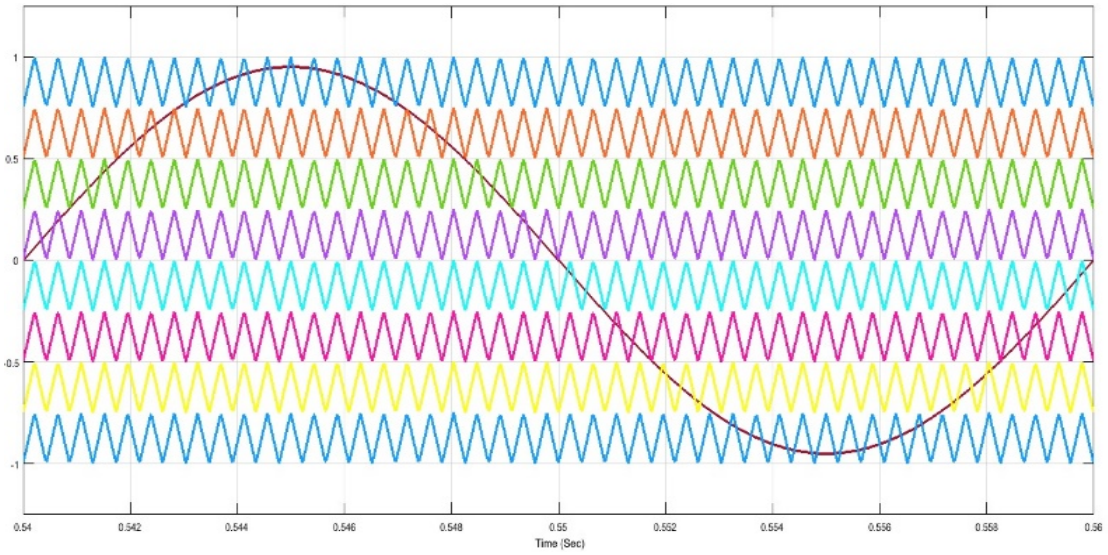
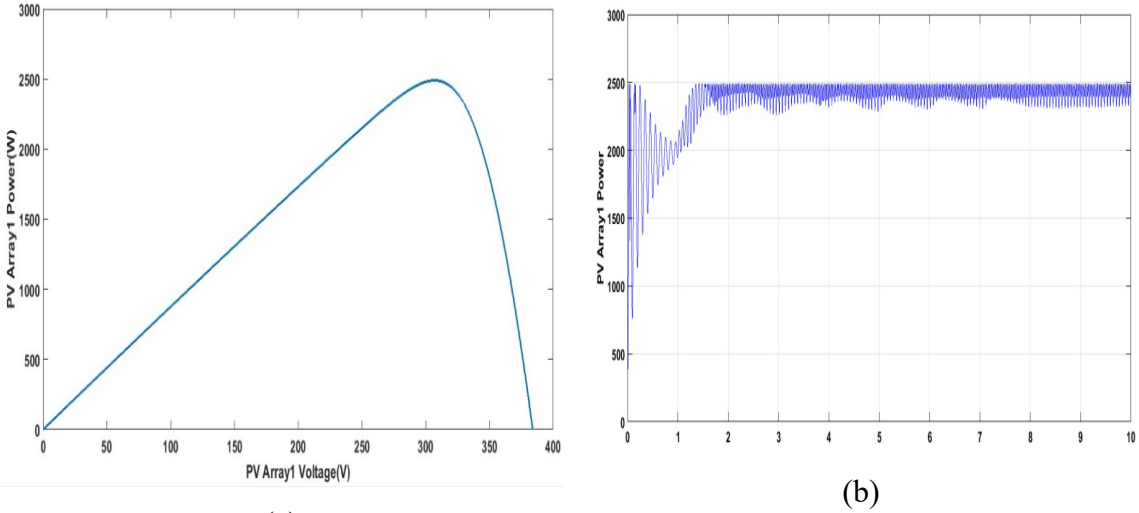


Figure 3.5 9-level phase disposition carrier pulse width modulation technique

Table 3-5 Logic for Nine level voltages Generation

Step 1	ma > Vcr1	Vdc
Step 2	Vcr1 < ma > Vcr2	3Vdc/4
Step 3	Vcr2 < ma > Vcr3	Vdc/2
Step 4	Vcr3 < ma > Vcr4	Vdc/4
Step 5	Vcr4 < ma > Vcr5	0
Step 6	Vcr5 < ma > Vcr6	-Vdc/4
Step 7	Vcr6< ma > Vcr7	-Vdc/2
Step 8	Vcr7 < ma > Vcr8	-3Vdc/4
Step 9	Vcr8< ma	-Vdc



(a) (b)

Figure 3.6 (a) P vs V Characteristic of PV Array1 (X xais:50v/div, Y:500W/div) (b) Maximum power of PV Array1 (X axis:1 sec /div, Y:500W/div)

The induced nine-level voltage across primary side of transformer induction motor is shown in Figure 3.7

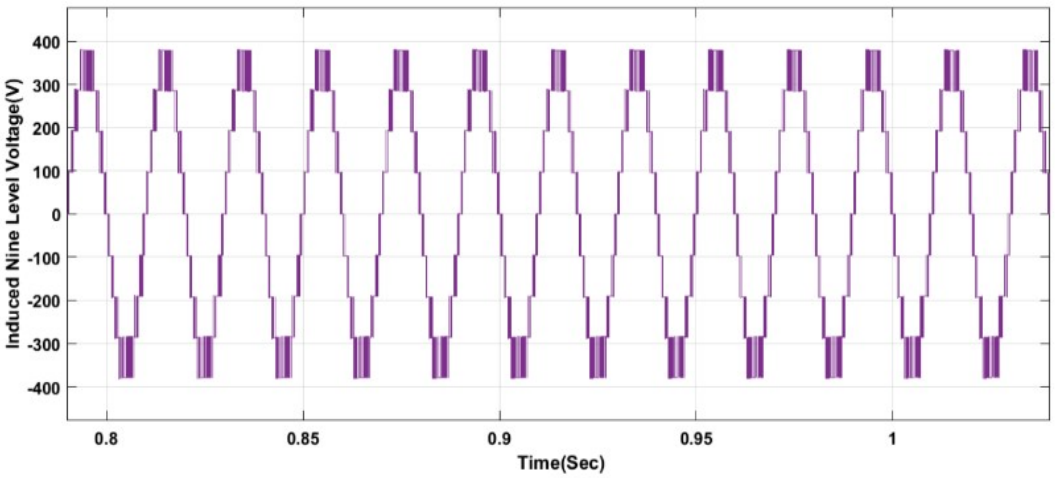


Figure 3.7 The Nine level voltage across primary side (Yaxis:10A/div, 1000V/div,500V/div X:0.05sec/div)

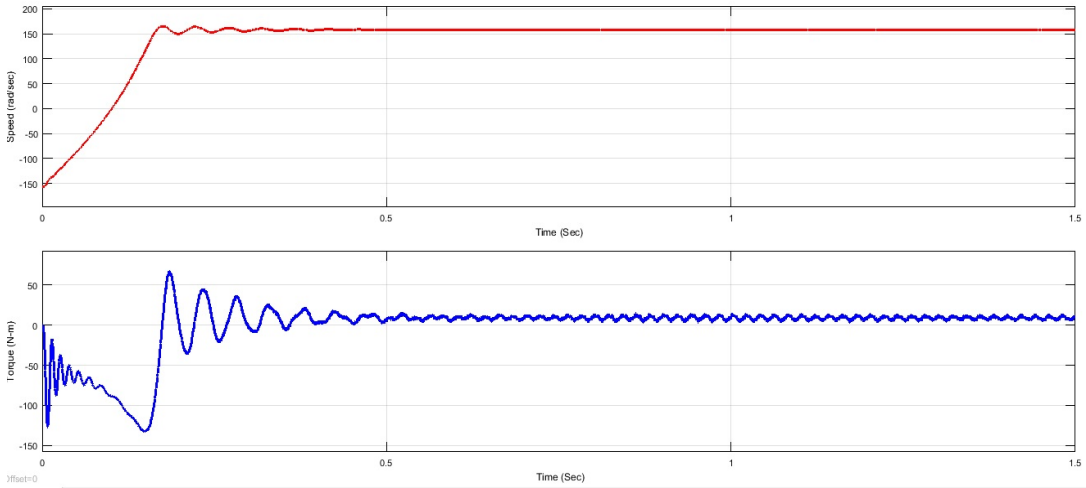


Figure 3.8 The Speed (Upper) and Torque (Lower) of IM under normal conditions (Y axis: 1000rpm/div, 50N-m/div X: 0.1sec/div)

The speed and torque of the induction motor are shown in the Figure 3.8 during normal operation. The seven-level voltage across primary side of transformer, the induction motor stator voltage and currents are shown in Figure 3.9 during normal and open circuit fault clearance conditions during switch Sa4 & Sa6 failure. The output voltage is maintained constant during fault by changing the tapings of transformer on primary side. The unaltered speed and torque are shown in Figure 3.10

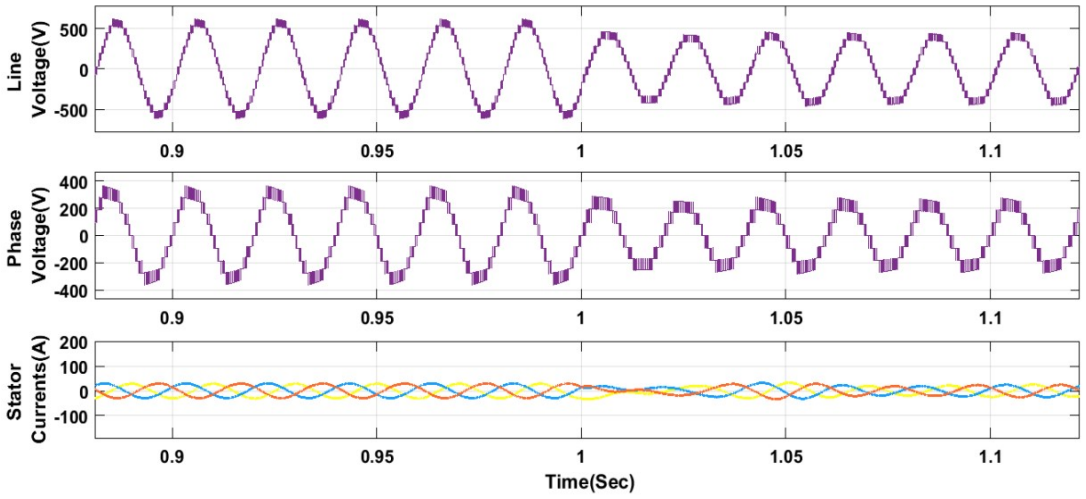


Figure 3.9 From Top: The nine- level voltage across primary side, line voltage of IM and stator currents of IM under normal and fault clearance conditions (Y axis: 10A/div, 1000V/div, 500V/div X: 0.05sec/div)

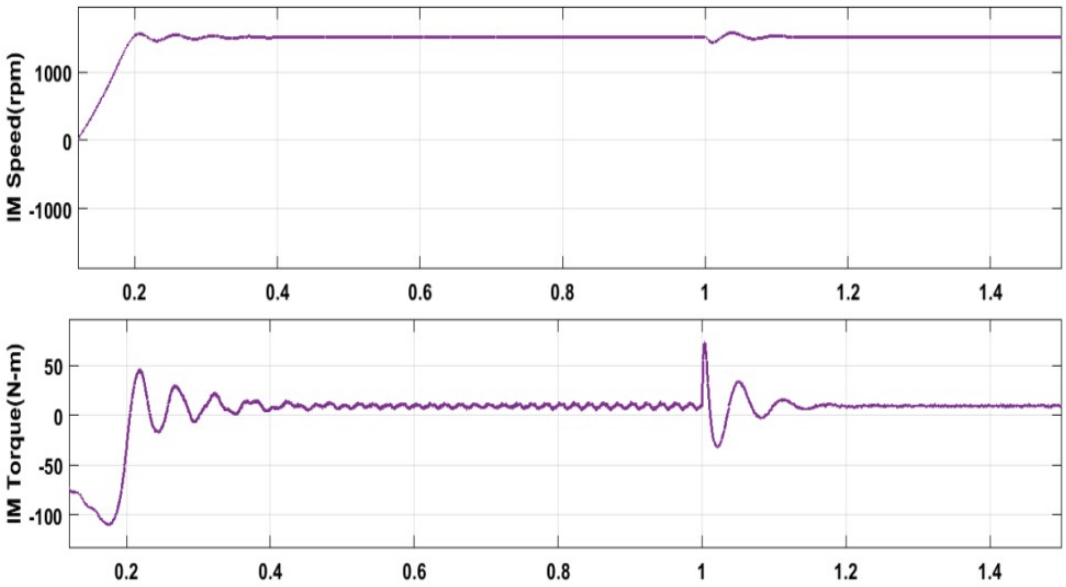


Figure 3.10 From Top: The Speed and Torque of IM under normal and fault clearance conditions (Y axis: 1000rpm/div, 50N-m/div X: 0.1sec/div)

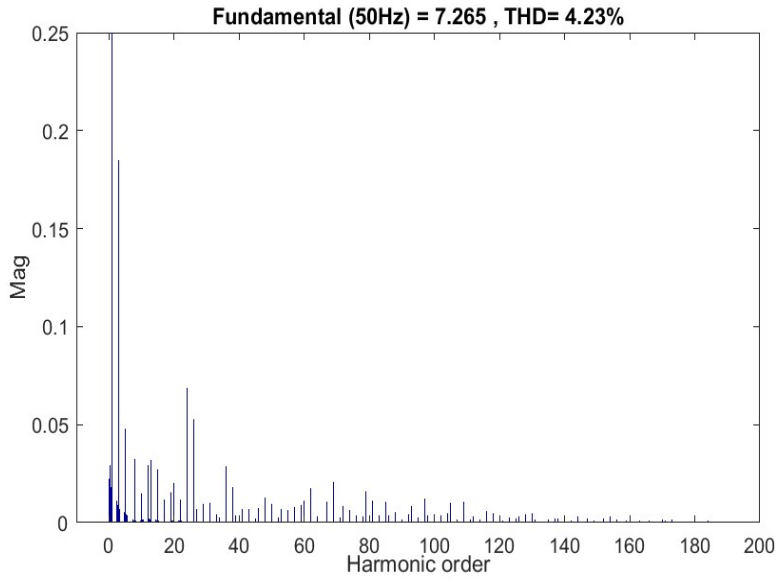


Figure 3.11 Total Harmonic Distribution of 9-Level inverter

Using the PD-PWM method, Figure 3.11 displays the Total Harmonic Distortion (THD) of a 9-Level inverter for phase (a) of the inverter current. As may be observed, the inverter current's THD is 4.23%.

3.5 Summary

In this chapter a new fault tolerant Topology of a nine-level MLI for Solar water pumping applications is proposed. The major attainments of the proposed Topology are fault tolerance to semiconductor switch failures and require less number of components. A comprehensive comparison is done with respect to the modified inverter with the conventional multilevel inverter. The switching technique used in the new Topology is Phase Disposition Pulse Width Modulation Technique (PD-PWM). This comparison leads to a conclusion where the proposed multilevel inverter is a better choice for water pumping applications. The fault tolerant ability of the Topology has been validated by Matlab/Simulation results. The enhanced inverter with the ability of switching redundancy at the time of open circuit switch failure works to supply energy by working on the voltage levels. The results reveal the capability of the Topology working under single & multiple switch failures. The working of the motor-drive system is found efficient during starting, steady-state, transient conditions and switch failures.

CHAPTER 4

FAULT TOLERANT ABILITY AND ENERGY BALANCING CAPABILITY OF MULTI-LEVEL INVERTER FED 3-PHASE INDUCTION MOTOR FOR SOLAR WATER PUMPING APPLICATIONS

4.1 Introduction

The redundancy in switching states, crucial for creating various voltage levels, significantly integrates fault-tolerant capabilities into multilevel inverters. However, this redundancy increases the device count, which increases the vulnerability of semiconductor devices and reduces overall reliability. Addressing these concerns, the current study introduces a novel fault-tolerant topology designed to generate an output voltage. This topology is equipped to handle open-circuit failures in single and multiple switches through an innovative redundant leg architecture, while short-circuit conditions are managed using fast fuses [69].

Applications that are safety-critical mainly depend on multilevel inverters. A single and many power switches experienced an open switch fault that prevented the multilevel inverter from operating continuously. In order to achieve a high-quality voltage waveform, the number of power semiconductor devices employed in dc-ac converters increased, making them more susceptible to failure. Therefore, one of the main obstacles to using multilayer inverters (MLIs) in many industrial applications is reliability [70].

In the context of cascaded multilevel inverters used in energy storage systems, such as batteries, achieving a state of charge (SoC) balancing among the storage cells poses a notable challenge. The technical literature has investigated and documented various methods to address SoC balancing. However, achieving effective and reliable SoC balancing remains challenging in practical applications [71].

Peculiar features like sustainability and efficiency makes batteries the most desirable energy storage systems. [72] Among all the combinations Li-ion, NI-Cd, lead-acid are the leading ones. Characteristics like high power density, low self-discharge rate; working cell voltage gives batteries a upper hand than other sources. Certain applications including hybrid electrical vehicles and portable utilities always benefit with the usage of batteries. One of the most important parameters to consider while

executing the control strategy is the SOC of batteries [70]. SOC determines the battery performance by reflecting upon the remaining capacity of the battery [71]. Thus, understanding SOC helps in protecting the battery and avoids the problem of over discharge and above all gives room to apply control strategies in order to save energy [72].

The off-grid photovoltaic framework utilizes two-stage power change to accomplish the necessary AC power from the accessible DC power [73, 74]. In Off-grid PV systems, power is produced with the assistance of various PV sources which improves the dependability yet there might be a shot at uneven charging of batteries due to the neighbourhood areas of interest and partial shading of PV panel boards. [75] There is a sharp affect on the state of charge levels of the battery because of the uneven charging and this can lead to complete shutdown of the system. This particular problem is partially solved in [76] single stage five-level inverter fed with two sources, where the researchers haven't introduced the Energy Balancing examination for the inverter with various sources.

In order to address the Energy Balancing among sources and larger count of devices issues of MLIs, A multi-source Energy Balancing capability MLI is presented in this paper, which is skilled to produce 9 levels in the yield with 4 symmetric sources separately. Here the numerous DC sources can be investigated effectively with various PV sources [77-79].

4.2 Proposed System Description

A. Normal Operation of Nine-Level Inverter

The topology mentioned in the chapter 3 is having some real time implementation problems with regard to short circuit switch faults and also problems related energy balancing issues. To address the above issues, in this chapter a three phase nine level inverter is presented for solar water pumping applications. The power circuit is used in chapter 3 is modified and with suitable switching connections. The newly introduced fault-tolerant capability at nine levels represents a novel advancement. This proposed nine-level inverter topology in this chapter addresses the aforementioned challenges by integrating fault tolerance. Its specific topology offers advantages over conventional multilevel inverters, including fewer components, the absence of a neutral point, and

mitigation of capacitor voltage balancing issues, especially concerning switch and source failures.

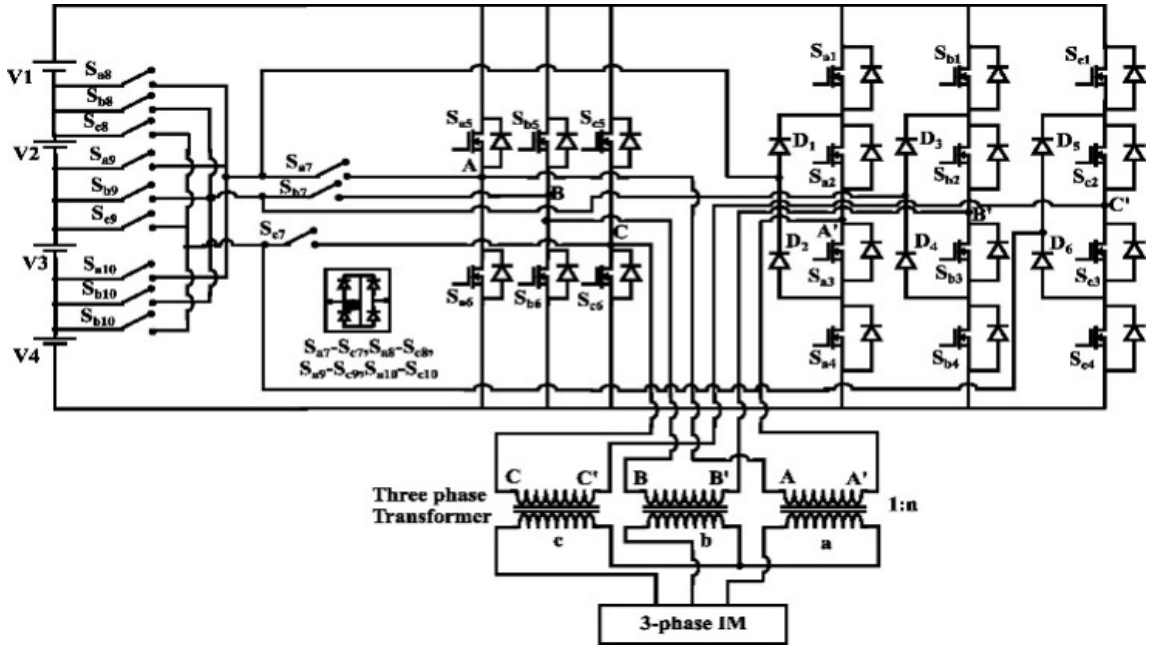


Figure 4.1 Modified 3-Φ 9-Level inverter configuration (Power circuit)

The proposed MLI can generate the nine-stage voltage the use of the switching combinations listed in Table 4-1 if its 4 resources are symmetrical in magnitude (this is, have equal strength and voltage ratings) (V1 = V2 = V3 = V4 = Vdc/4). The power circuit of nine-level inverter topology is shown in Fig.4.1.The Schematic of the proposed inverter functionality of semiconductor switches with Vdc/2 for S_{a1}-S_{a4}, Vdc for S_{a5}-S_{a6} and Vdc/4 for S_{a7}-S_{c7}, S_{a8}-S_{c8} S_{a9}-S_{c9}, S_{a10}-S_{c10}. For each regular and fault-tolerant operation of the inverter, the switches S_{a8}-S_{c8}, S_{a9}-S_{c9}, S_{a10}-S_{c10} and S_{a7}-S_{c7}, make contributions to growing the range of voltage levels and redundant switching combinations. According to Table 4-1, there are at least alternative switching states for each voltage level of the suggested MLI, which increases system reliability. All the possible voltage levels with corresponding switching combinations are indexed in Table 4-1. The switching combination is similar for b and c phases.

Table 4-1

Switching Pattern for 9- Level Normal Operation

Voltage Level [V]	HVL-MLV-LVL	Switches to turn ON
V1 = +Vdc	Higher Voltage Level [HVL]	S_{a1}-S_{a2}- S_{a6}
V2 = +0.75Vdc	Middle Voltage Level [MVL]	S_{a1}-S_{a2}-S_{a7}-S_{a10}
V3 = +0.5Vdc	Middle Voltage Level [MVL]	S_{a2}-S_{a1}-S_{a7}-S_{a9}
V4 = +0.25Vdc	Lower Voltage Level [MVL]	S_{a1}-S_{a2}-Sa_{7}-Sa_{8}
V5 = 0	Zero Level	S_{a1}-S_{a2}- S_{a5}
V6 = -0.25Vdc	Lower Voltage Level [MVL]	S_{a10}-S_{a7}-S_{a3}- S_{a4}
V7 = -0.5Vdc	Middle Voltage Level [MVL]	S_{a9}-S_{a7}-S_{a3}- S_{a4}
V8 = -0.75Vdc	Middle Voltage Level [MVL]	S_{a8}-S_{a7}-S_{a3}- S_{a4}
V9 = -Vdc	Higher Voltage Level [HVL]	S_{a5}-S_{a3}- S_{a4}

B. Fault Tolerant Operation of Nine-Level Inverter

(i) Open Circuit fault operation

Basically, inverter failures tend to occur because of source failure, semiconductor device short and open circuit failure, and drive circuit failure. As a result of lifting and breaking of holding semiconductor devices reasons the OC deficiencies. The source failure and open-circuit fault are addressed using redundant switching combinations. The possible switching pattern for bypassing the a-phase switch and source failures are given in Table 4-2. The Table 4-2 is similar for other phases failure.

(ii) Short Circuit fault operation

The SC failure is addressed by using Fuses on each leg. The faulty switch is isolated by using fuses and the short circuit path is bypassed by using redundant switching combinations given in Table 4-2. For instance, a SC failure on switches S_{a4} and S_{a6} in Fig.4.1 could cause the voltage supply to short circuit while the intermediate voltage level is being formed. Therefore, in order to completely isolate the arm two fuses are used at the end of each leg.

Table 4-2

Fault Operation Switching Pattern Generation of Voltage Levels

Levels (V)	Current Direction of Switches	Nature of fault
0.75Vdc	S_{a1}-S_{a2}-S_{a7}-S_{a10}	Source V4 Open/short Circuit Fault and/or S_{a4}, S_{a6} switch Open Fault
0.5Vdc	S_{a2}-S_{a1}-S_{a7}-S_{a9}	
0.25Vdc	S_{a1}-S_{a2}-S_{a7}-S_{a8}	
0	S_{a1}-S_{a2}- S_{a5}	
- 0.25Vdc	S_{a5}-S_{a2}-S_{a3}-S_{a8}	
- 0.5Vdc	S_{a5}-S_{a2}-S_{a3}-S_{a9}	
- 0.75Vdc	S_{a5}-S_{a2}-S_{a3}-S_{a10}	
0.75Vdc	S_{a2}- S_{a3}- S_{a8}	Source V1 Open/Short Circuit fault and/or S_{a1}, S_{a5} switch Open Fault
0.5Vdc	S_{a2}- S_{a3}- S_{a9}	
0.25Vdc	S_{a2}- S_{a3}- S_{a10}	
0	S_{a3}-S_{a4}- S_{a6}	
- 0.25Vdc	S_{a10}-S_{a7}- S_{a3}- S_{a4}	
- 0.5Vdc	S_{a9}-S_{a7}- S_{a3}- S_{a4}	
- 0.75Vdc	S_{a8}-S_{a7}- S_{a3}- S_{a4}	
0.75Vdc	S_{a1}-S_{a2}- S_{a7}-S_{a10}	S_{a5}, S_{a6} Switch Open Fault
0.5Vdc	S_{a2}-S_{a1}- S_{a7}-S_{a9}	
0.25Vdc	S_{a1}-S_{a2}- S_{a7}-S_{a8}	
0	S_{a2}-S_{a3}- S_{a7}	
- 0.25Vdc	S_{a10}-S_{a7}- S_{a3}- S_{a4}	
- 0.5Vdc	S_{a9}-S_{a7}- S_{a3}- S_{a4}	
- 0.75Vdc	S_{a8}-S_{a7}- S_{a3}- S_{a4}	

4.3 Analysis of Energy- Balancing Issue for Suggested MLI Arrangement

For certain applications involving SWPS the proposed topology shown in Figure 4.2 This particular pumping system consists of PV strings that are separate from each other and can operate at one fourth of their power when contrasted with an inverter (PV). A unique methodology of balance of energy takes place with the help of the combination of switches at the mid-levels of voltage shown in Figure 3.3(mentioned in chapter 3). Therefore, the mathematical understandings of this energy division at each level are noted.

Incomplete shading or nearby obstructions on any of the PV strings can lead to uneven charging or discharging of batteries, affecting their state of charge (SOC). As a result, a battery with a lower SOC will discharge faster compared to one with a higher SOC, potentially leading to the premature shutdown or abnormal behaviour of the entire system. To prevent this, batteries with higher SOC levels should be discharged more quickly. This can be achieved by applying the Energy Balancing technique using various gating pulses. A case study to calculate the energy transferred to load during each voltage-level of nine-level inverter with four individual sources is presented.

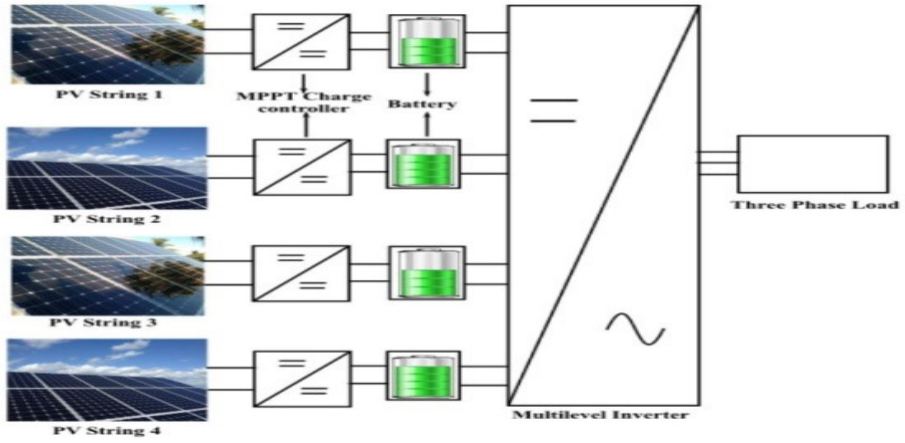


Figure 4.2 Multi-source single phase inverter system block diagram

To achieve every voltage level, the combinations at the source are shown in Table 4-3. The takeaway from this particular table is the load should be getting its power from Vdc1 to produce ±Vdc, 3Vdc/4, Vdc/2, Vdc/4. This results is the charge of Vdc1 draining out first when opposed to the others. Thus, to compensate this particular drain a system with balanced energy setup is proposed here. The balance is achieved by utilizing various combinations of sources which are redundant. The equations determine the transfer of energy at the respective voltage-level. The Figure 4.3 (a) and (b) gives a clear picture of the concept on a graphical front. Both the graphs combined gives us the half cycle (positive) and the areas of the voltage levels.

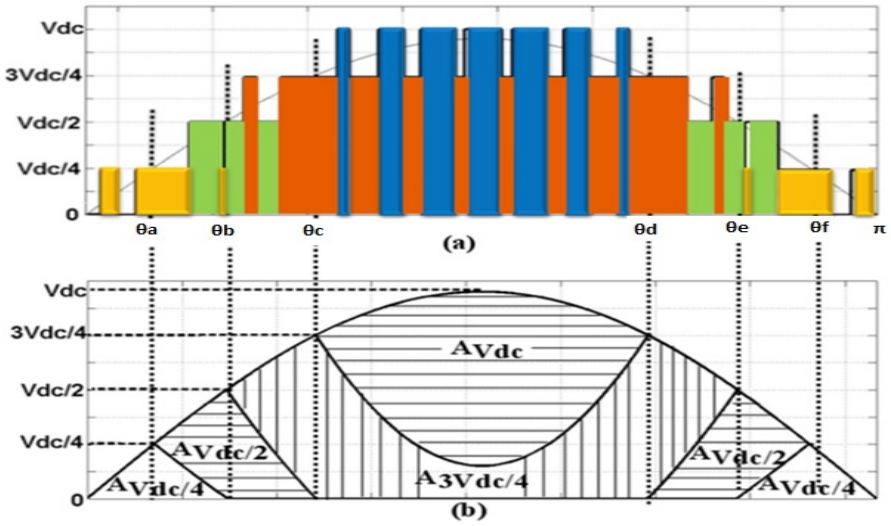


Figure 4.3 (a) Half cycle of 9-level voltage waveform (0 - Π) (b) Region referred to respective voltage gradient.

The fundamental voltage (Instantaneous) waveform from o to π given as:

$$V_{FUNDA} = V_P \sin(\omega t) \tag{4.1}$$

Vdc, ¾ Vdc, ½ Vdc, ¼ Vdc are the voltage levels indicated as V_A, V_B, V_C, V_D.

In the region θc to θd given VA indicates Vdc voltage level and given as:

$$V_A = 4\left\{V_P \sin(\omega t) - \left(\frac{3Vdc}{4}\right)\right\} \tag{4.2}$$

In the region θb to θe given V_B indicates ¾ Vdc voltage level and given as:

The ¾ Vdc voltage gradient in the area θc to θd

$$V_m = \left(V_{FUNDA} - V_A\right) \tag{4.3}$$

The ¾ Vdc voltage gradient in the area θb to θc

$$V_n = 3\left(V_{FUNDA} - \left(\frac{V_{dc}}{2}\right)\right) \tag{4.4}$$

$$V_B = \left(V_m + 2V_n\right)$$

V_C indicates ½ Vdc voltage gradient in the area θa to θf given as:

The ½ Vdc voltage gradient in the area θb to θc

$$V_o = \left(V_{FUNDA} - V_n\right) \tag{4.5}$$

The ½ Vdc voltage gradient in the area θa to θb

$$V_p = 2\left(V_{FUNDA} - \left(\frac{V_{dc}}{4}\right)\right) \tag{4.6}$$

$$V_C = \left(2V_o + 2V_p\right) \tag{4.7}$$

V_D indicates ¼ Vdc voltage gradient in the area 0 to θb and θf to π given as:

The ¼ Vdc voltage gradient in the area θa to θb

$$V_q = \left(V_{FUNDA} - V_p\right) \tag{4.8}$$

The ¼ Vdc voltage gradient in the area 0 to θa

$$V_r = V_{FUNDA} \tag{4.9}$$

$$V_D = \left(2V_r + 2V_q\right) \tag{4.10}$$

are the corresponding energies to Vdc, ¾ Vdc, ½ Vdc, ¼ Vdc voltage levels.

$$i = I_m \sin(wt - \phi), \tag{4.11}$$

where ϕ is power factor angle of load current.

The angle θa to θf calculation is based on depends on modulation index (m_i) and calculated as

$$\left(m_i * V_{dc} * \sin\theta\mathrm{a}\right) = \frac{V_{dc}}{4} \tag{4.12}$$

$$\begin{aligned}
\theta\mathrm{a} &= \sin^{-1}\left(\frac{1}{4m_i}\right) \\
\theta\mathrm{b} &= \sin^{-1}\left(\frac{1}{2m_i}\right) \\
\theta\mathrm{c} &= \sin^{-1}\left(\frac{3}{4m_i}\right) \\
\theta\mathrm{d} &= \pi - \sin^{-1}\left(\frac{3}{4m_i}\right) = \pi - \theta c \\
\theta\mathrm{e} &= \pi - \sin^{-1}\left(\frac{1}{2m_i}\right) = \pi - \theta b
\end{aligned} \tag{4.13}$$

$$\theta \mathrm{f} = \pi - \sin^{-1}\left(\frac{1}{4m_i}\right) = \pi - \theta a$$

During voltage gradient the energy transferred is given as:

$$E_{VA} = \int_{\theta c}^{\pi-\theta c} V_1 I_m \sin(wt-\phi) d\omega t \tag{4.14}$$

$$E_{V_A} = \left\{ \begin{array}{l} \left(2V_m I_m\right) * \left\{ \left(\pi - 2\theta \mathrm{c}\right) * \cos\left(\phi\right) + \dfrac{\sin\left(2\theta c + \phi\right)}{2} + \dfrac{\sin\left(2\theta c - \phi\right)}{2} \right\} - \\ \left\{ 3V_{dc} I_m \left[\cos\left(\theta c + \phi\right) + \cos\left(\theta c - \phi\right) \right] \right\} \end{array} \right\} \tag{4.15}$$

During V_2 voltage level the energy transferred is given as:

$$E_{VB} = \left\{ \int_{\theta b}^{\theta c} V_n id\omega t + \int_{\pi-\theta c}^{\pi-\theta b} V_n id\omega t + \int_{\theta c}^{\pi-\theta c} V_m id\omega t \right\} \tag{4.16}$$

$$E_{VB} = \left\{ \begin{array}{l} \left(1.5V_m * I_m\right) \times \left\{ \left(\theta \mathrm{c} - \theta \mathrm{b}\right) \cos\left(\phi\right) - \dfrac{\sin\left(2\theta c - \phi\right)}{2} + \dfrac{\sin\left(2\theta c + \phi\right)}{2} \right\} + \\ \left\{ 1.5V_{dc} * I_m \left[\cos\left(\theta c - \phi\right) - \cos\left(2\theta b - \phi\right) \right] \right\} + \\ \left(1.5V_m * I_m\right) \times \left\{ \left(\theta c - \theta \mathrm{b}\right) \cos\left(\phi\right) + \dfrac{\sin\left(2\theta b + \phi\right)}{2} - \dfrac{\sin\left(2\theta c + \phi\right)}{2} \right\} + \\ \left\{ 1.5V_{dc} * I_m \left[\cos\left(\theta c + \phi\right) - \cos\left(\theta b + \phi\right) \right] \right\} + \\ \left(1.5V_m * I_m\right) \times \left\{ \left(\pi - 2\theta \mathrm{c}\right) \cos\left(\phi\right) + \dfrac{\sin\left(2\theta c + \phi\right)}{2} + \dfrac{\sin\left(2\theta c - \phi\right)}{2} \right\} - E_{V_k} \end{array} \right\} \tag{4.17}$$

During V_3 voltage gradient the energy transferred is given as:

$$E_{VC} = \left\{ \int_{\theta a}^{\theta b} V_p id\omega t + \int_{\pi-\theta b}^{\pi-\theta a} V_p id\omega t + \int_{\theta b}^{\theta c} V_o id\omega t + \int_{\pi-\theta c}^{\pi-\theta b} V_o id\omega t \right\} \tag{4.18}$$

$$E_{VC} = \left\{ \begin{array}{l} \left(V_m * I_m\right) \times \left\{ \left(\theta b - \theta \mathrm{a}\right) \cos\left(\phi\right) - \dfrac{\sin\left(2\theta b - \phi\right)}{2} + \dfrac{\sin\left(2\theta a - \phi\right)}{2} \right\} + \\ \left\{ 1.5V_{dc} * I_m \left[\cos\left(\theta b - \phi\right) - \cos\left(\theta a - \phi\right) \right] \right\} + \\ \left(V_m * I_m\right) \times \left\{ \left(\theta b - \theta \mathrm{a}\right) \cos\left(\phi\right) + \dfrac{\sin\left(2\theta a + \phi\right)}{2} - \dfrac{\sin\left(2\theta b + \phi\right)}{2} \right\} + \\ \left\{ 0.5V_{dc} * I_m \left[\cos\left(\theta b + \phi\right) - \cos\left(\theta a + \phi\right) \right] \right\} - \\ \left(V_m * I_m\right) \times \left\{ \left(\theta c - \theta \mathrm{b}\right) \cos\left(\phi\right) + \dfrac{\sin\left(2\theta c - \phi\right)}{2} + \dfrac{\sin\left(2\theta b - \phi\right)}{2} \right\} - \\ \left\{ 0.5V_{dc} * I_m \left[\cos\left(\theta c - \phi\right) - \cos\left(\theta b - \phi\right) \right] \right\} - \\ \left(V_m * I_m\right) \times \left\{ \left(\theta c - \theta \mathrm{b}\right) \cos\left(\phi\right) - \dfrac{\sin\left(2\theta b + \phi\right)}{2} - \dfrac{\sin\left(2\theta c + \phi\right)}{2} \right\} - \\ \left\{ 0.5V_{dc} I_m \left[\cos\left(\theta c + \phi\right) - \cos\left(\theta b + \phi\right) \right] \right\} \end{array} \right\} \tag{4.19}$$

During V_4 voltage gradient the energy transferred is given as:

$$E_{VD} = \left\{ \int_{0}^{\theta a} V_f id\omega t + \int_{\pi-\theta a}^{\pi} V_f id\omega t + \int_{\theta a}^{\theta b} V_e id\omega t + \int_{\pi-\theta b}^{\pi-\theta a} V_e id\omega t \right\} \tag{4.20}$$

$$E_{VD} = \left\{ \begin{array}{l} (0.5V_m * I_m) \times \left\{ \theta \mathrm{a}\cos(\phi) - \frac{\sin(2\theta a - \phi)}{2} - \frac{\sin(\phi)}{2} \right\} + \\ (0.5V_m * I_m) \times \left\{ \theta \mathrm{a}\cos(\phi) + \frac{\sin(2\theta a + \phi)}{2} + \frac{\sin(\phi)}{2} \right\} - \\ (0.5V_m * I_m) \times \left\{ (\theta b - \theta \mathrm{a})\cos(\phi) - \frac{\sin(2\theta b - \phi)}{2} + \frac{\sin(2\theta a - \phi)}{2} \right\} - \\ \left\{ 0.5V_{dc} * I_m \left[\cos(\theta b - \phi) - \cos(\theta a - \phi) \right] \right\} - \\ (0.5V_m * I_m) \times \left\{ (\theta b - \theta \mathrm{a})\cos(\phi) - \frac{\sin(2\theta b + \phi)}{2} + \frac{\sin(2\theta a + \phi)}{2} \right\} - \\ \left\{ 0.5V_{dc} * I_m \left[\cos(\theta b + \phi) - \cos(\theta a + \phi) \right] \right\} \end{array} \right\} \tag{4.21}$$

During positive half cycle the total energy transferred to load given as:

$$E = E_{VA} + E_{V_B} + E_{VC} + E_{VD} \tag{4.22}$$

$$\%E_{V\max} = \left[E_{V_s} / (\sum_{i=1}^{4} E_{V_i}) \right] * 100 \tag{4.23}$$

Where s=1, 2, 3, 4

For b, c phases it is phase shifted by 120^0, 240^0 respectively.

With the help of equations [80], we can obtain the change in the percentage with respect to energy transfer at various voltage levels. This analysis gives us a clear idea about the working of batteries as each ambiguous drain in terms of charging will inevitably influence the working of the system on a whole.

4.3.1 Control Scheme

To regulate the battery charge balance and select the switching combination in the event of source or switch failure, as depicted in flowchart Fig.4.4. V1, V2, V3, and V4. are four DC source voltages and Sf is the fault signal from the driver circuit or charge regulator. According to the flowchart, the system will check the difference in the state of charge of the batteries if there is no fault; if it is within specified limits, nine-level voltages will be generated using Table 4-1. Using groups, I&III and groups II&IV (shown in the split column) in Table 4-3, the appropriate switching combination is chosen if the difference in SOC is greater or less than the limit. Assuming the fault signal is high (switches or sources failure) then the proper switching combination is chosen with respect the switch or source fault utilizing Table 4-2. Using phase disposition carrier pulse width modulation, the gating pulses are produced in this paper

to generate a nine-level voltage. Carrier phase disposition pulse-width modulation generates the gate pulses shown in fig 4.5 that enable the proposed multilevel inverter (MLI) to produce a nine-level output voltage. The modulation signal (Vm) is compared with corresponding carrier signals (Tri1 to Tri8) and the related pulses are applied to switches to generate a nine- level voltage. During fault condition the the magnitude of modulation signal is reduced to generate lower voltage levels.

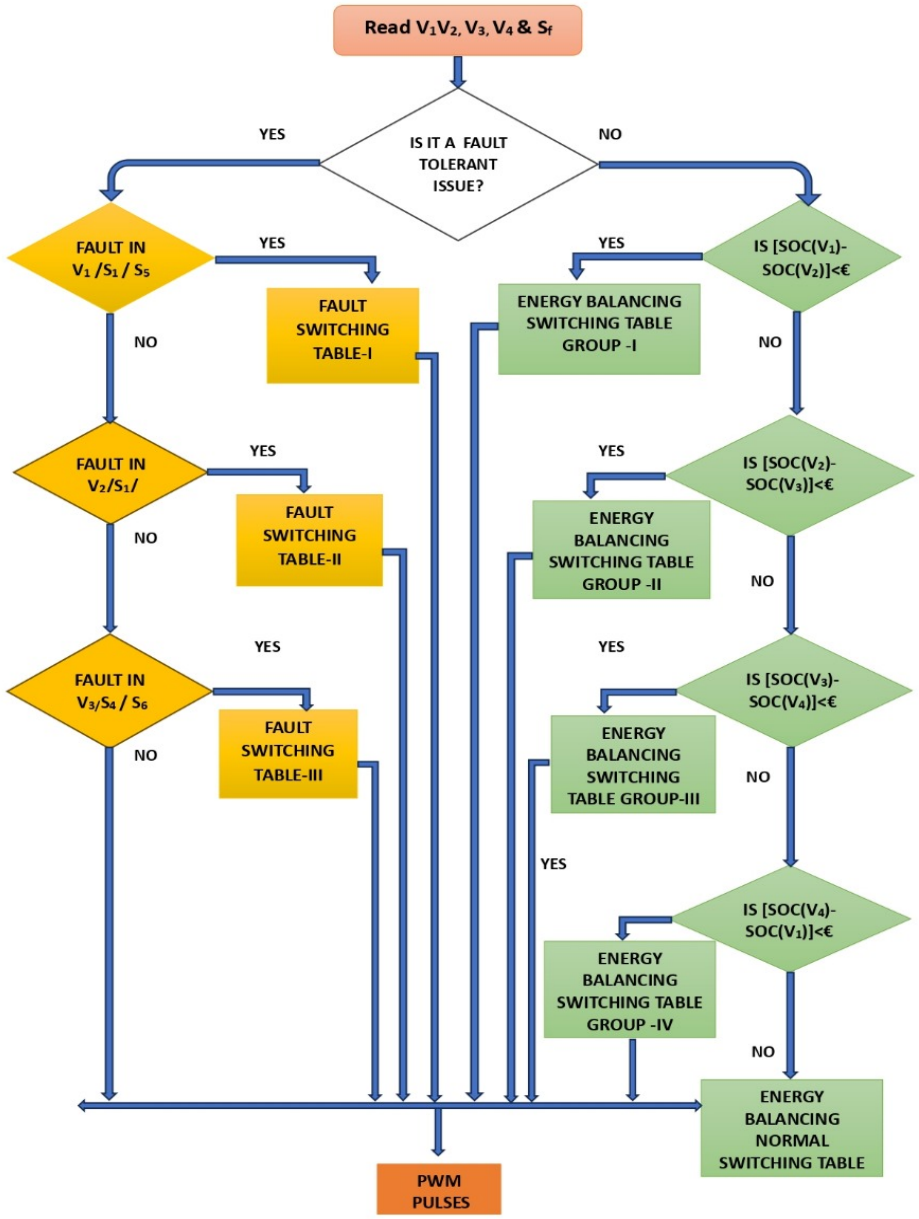


Figure.4.4 Flowchart of 9-Level MLI topology for the implementation of switching schemes under Healthy, faulty, and Energy balancing operations

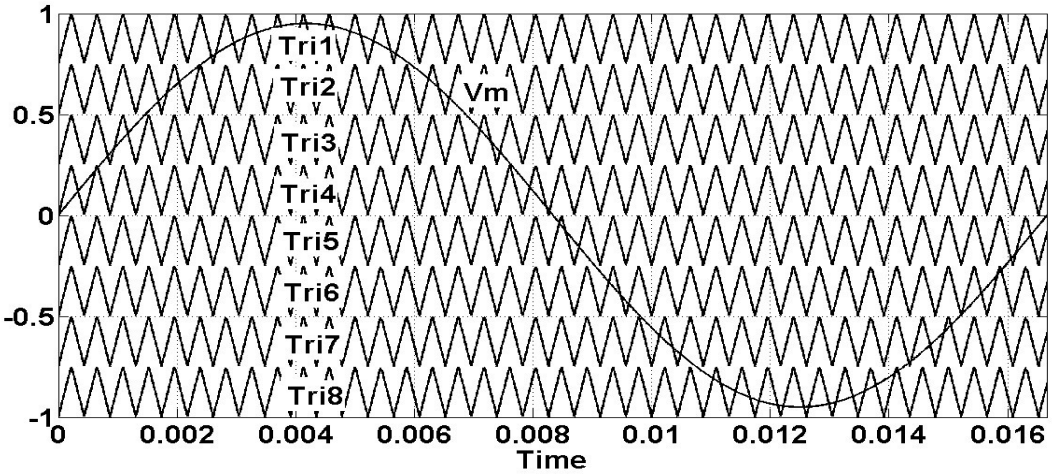


Figure 4.5 9-level voltage operation of the proposed MLI- Carrier pulse width modulation

Table 4-3 Switching pattern – possible source combinations

Levels	Switches	Sources	Possible source combination	
			GROUP I &III	GROUP II &IV
V_{dc}	Sa_1-Sa_2- Sa_6	V_1, V_2, V_3,V_4	√	√
$3V_{dc}/4$	Sa_1-Sa_2- Sa_7- S_{10}	V_1, V_2, V_3	√	--
	S_8-Sa_2- Sa_3- Sa6	V_2, V_3, V_4	--	√
$V_{dc}/2$	Sa_2-Sa_1- Sa_7- S_9	V_1, V_2	√	---
	S_9- Sa_2- Sa_3- Sa_6	V_3, V_4	---	√
$V_{dc}/4$	Sa_1-Sa_2- Sa_7- S_8	V_1	√	---
	S_{10}- Sa_2- Sa_3- Sa_6	V_4	---	√
0	Sa_3-Sa_4-Sa_6 (or) Sa_1-Sa_2- Sa_5(or) Sa_2-Sa_3- Sa_7	---	---	---
$-V_{dc}/4$	Sa_5-Sa_2-Sa_3-Sa_7-S_8	V_1	---	√
	S_{10}-Sa_7- Sa_3- Sa_4	V_4	√	
$-V_{dc}/2$	Sa_5-Sa_2-Sa_3-Sa_7-S_9	V_1, V_2	---	√
	S_9- Sa_7- Sa_3- Sa4	V_3, V_4	√	---
$-3V_{dc}/4$	Sa_5-Sa_2-Sa_3-S_{10}	V_1, V_2, V_3	---	√
	S_8- Sa_7- Sa_3- Sa_4	V_2, V_3, V_4	√	---
$-V_{dc}$	Sa_5-Sa_3- Sa_4	V_1, V_2, V_3, V_4	√	---

Figure 4.6 (a) illustrates the energy transferred to different voltage levels for various modulation index values using the equations above. It can be observed that the energy transferred to each voltage level varies due to the batteries' irregular discharging and charging.

Figure 4.6 (b) depicts the energy shared by various sources for various modulation indexes and the energy balance achieved by the redundant switching combinations shown in Table 4-2. From this figure, it tends to be seen that at a modulation index of 0.62 for all voltage sources share equivalent burden energy. For this situation, the level of energy shared to load by various sources is practically consistent after the 0.85 modulation index.

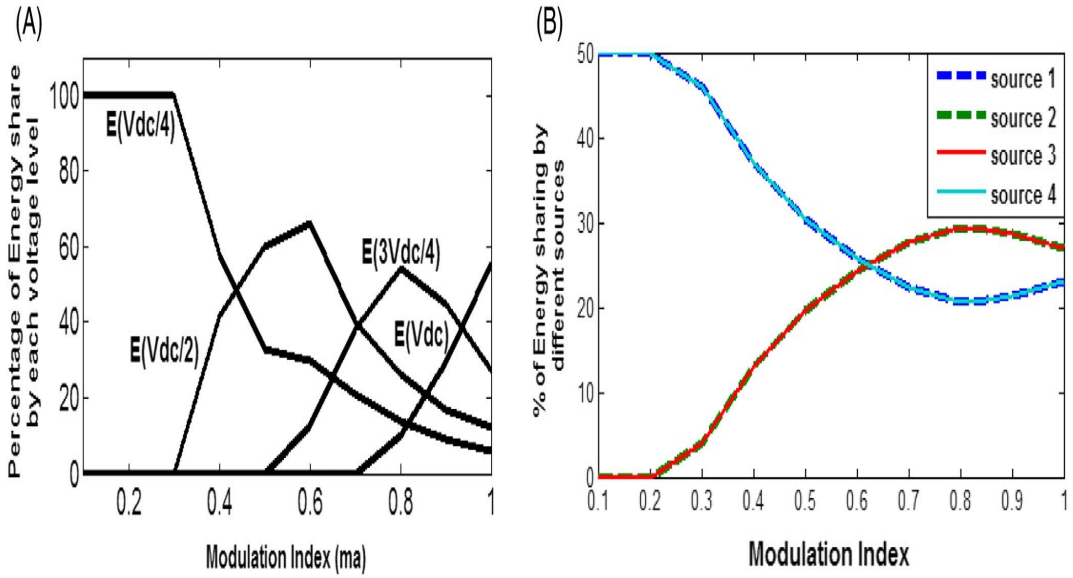


Figure 4.6 (a) For the positive half cycle, the energy share at each voltage level is expressed as a percentage with different modulation indices and Percentage of energy share by each voltage level (b) Percentage of energy transferred to load by each source

4.4 Simulation Results

The suggested topology's viability and resilience are tested in a MATLAB Simulink environment and confirmed by the acquired experimental outcomes. The topology is also examined in both healthy and fault-prone environments. Two failure scenarios under both OC and SC failure are examined. A single switch is deemed defective in the fault scenario, and then another single switch fails. The single switch failure tolerance of the suggested topology is covered in this thesis. On a given switch, the removal of

gate pulses simulates an OC failure operation, whereas the continuous application of gate pulses simulates a SC failure operation.

Only the fault tolerance capability and energy balancing problem caused by the proposed MLI topology's unequal battery charge and the switching scheme reconfiguration under defective situations is the subject of this chapter. Therefore, it is believed that in the event of a short circuit failure, if high magnitude current flows for a long enough period of time, the fuse associated with the malfunctioning switch will blow open. An SC failure becomes an OC failure as a result. Fig.4.7 shows the nine-level phase voltage (upper trace), line voltage (middle trace) and three phase motor currents (lower trace) during normal operation. The induction motor speed (upper trace) and torque (lower trace) are given in Fig.4.8

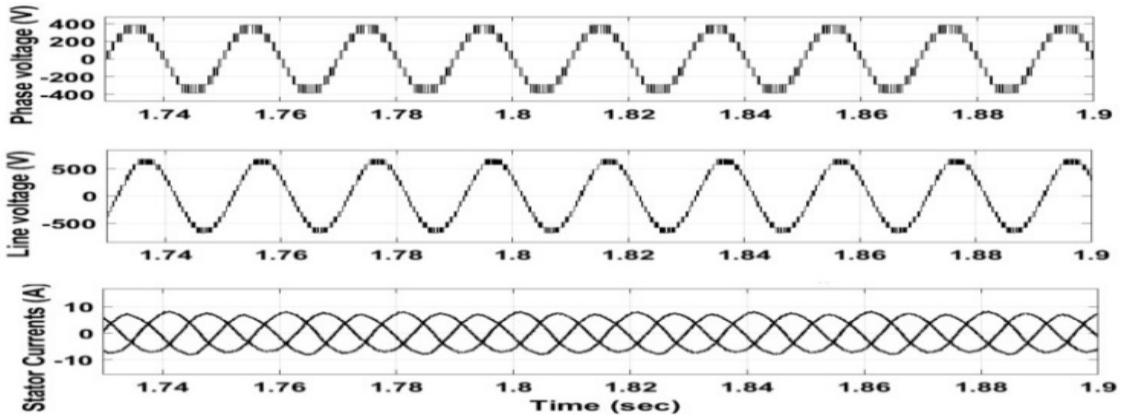


Fig.4.7: The 9-L voltage across the primary side, line voltage of IM, and stator currents of IM

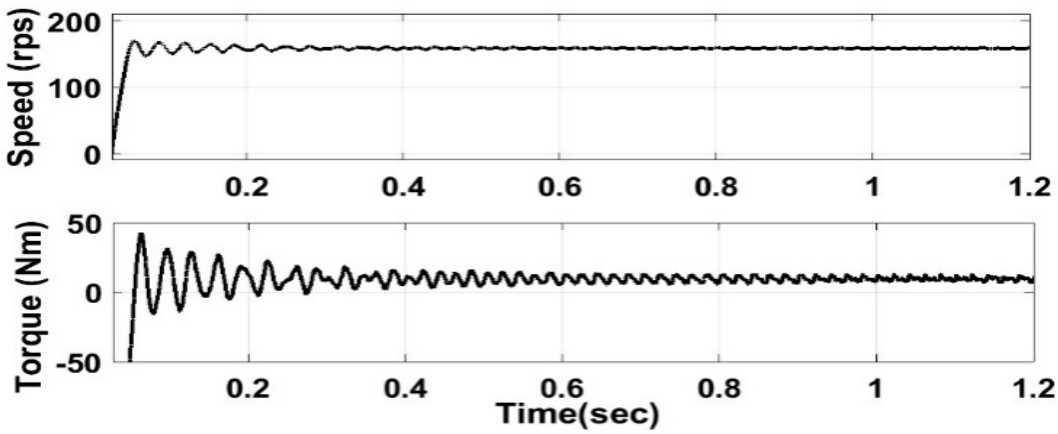


Fig 4.8: Speed (N) &Torque (Te) plot of Induction-Motor under steady-state operations. Top Trace: Speed [X-Scale: 0.1s /div]-[Y-Scale- 1500rpm/div] Bottom Trace: Torque [X-Scale: 0.1s/div]-[Y-Scale-5N-m/div]

A. Simulation Results under Open Circuit (OC) Fault (*OC on Switch S4, Followed by Switch S6)*

The voltage levels "V1" and "V9" are produced using Vm> Vcar1 and Vcar8<Vm, respectively, in all healthy situations. The fundamental cycle's positive and negative phases are produced by the switching sequences Vm> Vcar1 and Vcar8<Vm, respectively. A detailed analysis of Table 4-2 reveals that the absence of the "V1" voltage level generation is caused by an Open-Circuit (OC) failure involving switch S4. The present path is closed when the bidirectional switch Sa10 is activated via the Sa1-Sa2-Sa7-Sa10.

The topology returns to its pre-fault behaviour at the point (which happens at t = 1.75 seconds) shown in Figure.4.9, when the ability to create the "V1" voltage level is restored. At t = 1.6 seconds, switch S6 then experiences an Open-Circuit (OC) failure. Both the "V2" and "V1" voltage levels cannot be produced after the inverter's OC failure. As a result, the load current decreases, which eventually results in a drop in torque. The "V2" voltage level generation capability is restored when Switch Sa_{10} is activated during the (t = 1.7 seconds). The topology may still provide the load with the pre-fault output voltage rating even if it is now operating as a seven level inverter. A failure of the OC is shown in Fig. 4.9; a failure of the switching scheme to activate the proper bidirectional switches is shown under fault conditions in the results obtained.

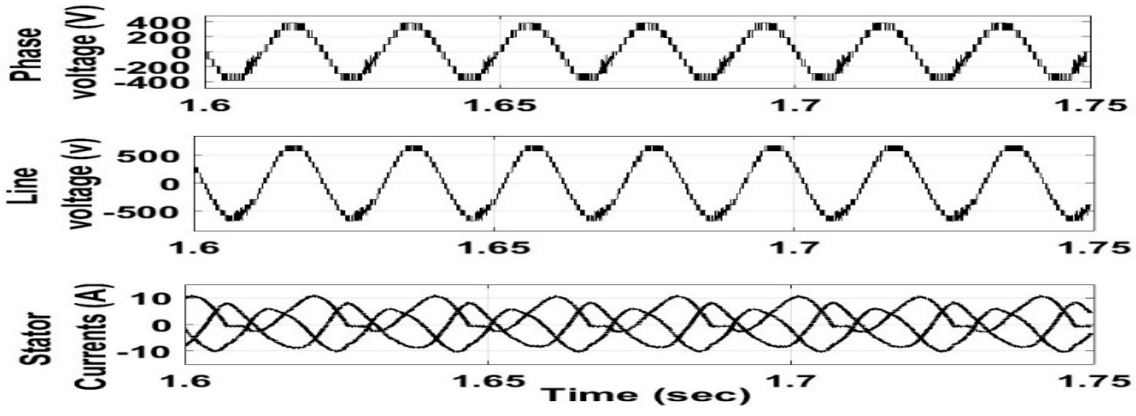


Fig.4.9 The 9-L voltage across the primary side, line voltage of IM, and stator currents of IM under open circuit fault conditions Top Trace1: P-V Plot of P-V Array [X-Scale: 0.05s/div]-[Y-Scale-1000v/div] Middle Trace: [X-Scale: 0.05s/div]-[Y-Scale- 500v/div] Bottom Trace: [X-Scale: 0.05s/div]-[Y-Scale-10amp/div]

Fig.4.8 depicts an induction motor's speed and torque during normal operation. The voltage and currents across the induction motor stator's seven levels, as well as the transformer's primary side voltage, are depicted in Fig.4.9 an open circuit fault occurred in Sa4 and Sa6. By altering the transformer's primary side tapings, the output voltage is kept constant while there is a fault. Fig.4.10 depicts the unaltered speed and torque.

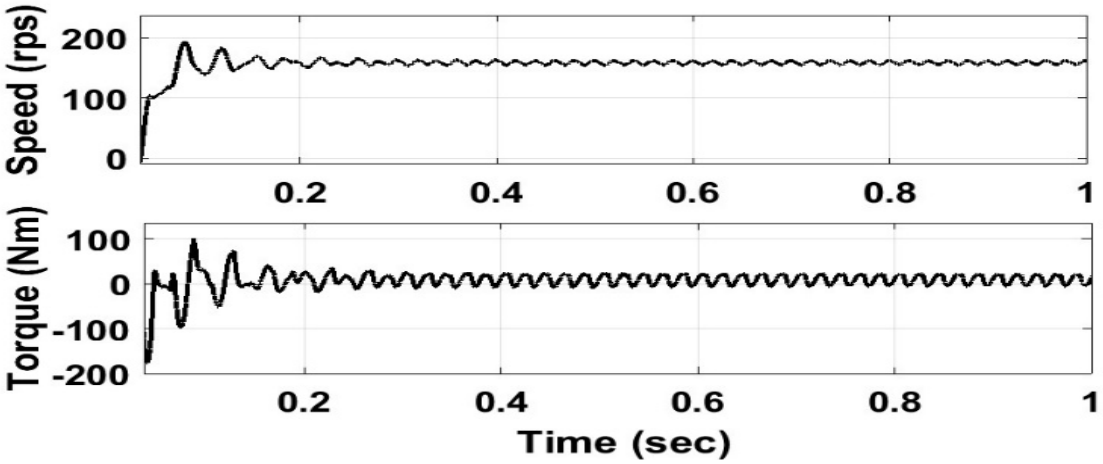


Fig.4.10 Speed (N) & Torque (Te) Plot of Induction-Motor under open circuit fault conditions. Top Trace: Speed [X-Scale: 0.1s /div]-[Y-Scale- 1000rpm/div] Bottom Trace: Torque [X-Scale: 0.1s/div]-[Y-Scale- 5N-m/div]

B. Simulation Results under Short Circuit (SC) Faults ***(SC on Switch S4, Followed by SC on Switch S6)***

Unlike an OC failure, a SC failure does not cause the current to stop passing through the malfunctioning switch. If the SC on any switch fails, activating the complementary switch may result in a short circuit path. For example, the voltage supply may short circuit while the middle voltage level is being created due to a SC failure on switches Sa4 and Sa6 shown in Figure.4.11. Fuse F1–F6 are then added to each arm of the inverter architecture to ensure complete isolation of the faulty arm, which may then be viewed as an OC failure.

Under the healthy condition, nine level voltages are generated. At the instance of SC failure on switches Sa4 (in Figure.4.11 the corresponding fuse ‘F6’ is considered to blow open. This converts the SC failure into an OC one. Thus, an output voltage waveform comprising of seven levels immediately starts generating. Nine level inverter voltages and current after fault conditions is also presented in Figure. 4.12. And under these conditions the speed and torque characteristics of induction motor are also

investigated (shown in Figure: 4.13). There is lot of distortion in the output voltages and high surges in the currents and also in speed and toques ripples observed.

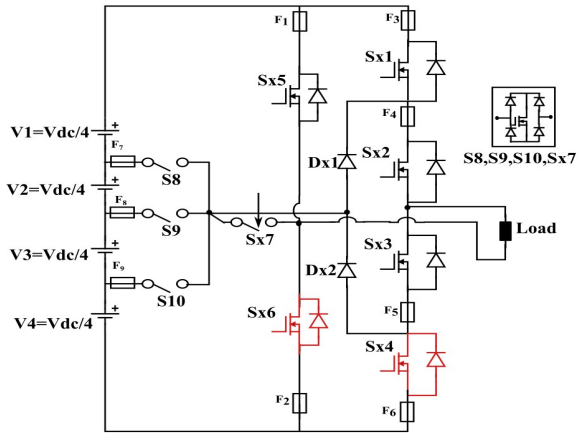


Figure 4.11 Nine-Level Short circuit with Fuses -Short circuit failure on switch S4

An SC failure does not stop the current flowing through the malfunctioning switch, in contrast to an OC failure. Turning on the complementary switch could result in a short circuit path if the SC on any switch fails. For instance, a SC failure on switches S5 and S6 could cause the voltage supply to short circuit while the "V2" voltage level is being generated. As a result, fuses F1–F4 are added to each arm of the main inverter architecture to guarantee total isolation of the problematic arm, which can then be regarded as an OC failure. The fuse is deemed to blow open under the following short circuit failure scenarios, and concurrent modifications to the switching method are made.

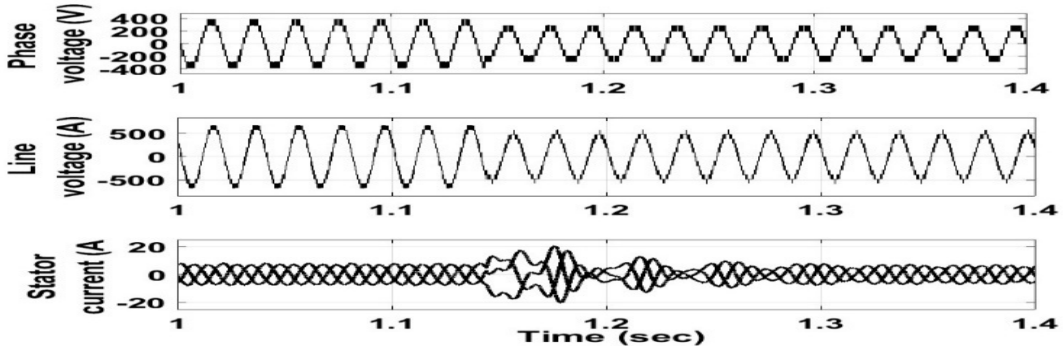


Fig.4.12 The 9-L voltage across the primary side, line voltage of IM, and stator currents of IM under normal and after short circuit fault clearance conditions

In a healthy state, Vcar4 <Vm> Vcar5 is used to generate the voltage level "V5". When switch S4 experiences a SC failure (t = 1.1 sec in Fig. 4.12), malfunctioning switches Sa1-Sa2-Sa5, which are activated for the formation of the "V5" voltage level.

Consequently, the medium voltage level generation is no longer available. According to Figure 4.12, the matching fuse "F2" is said to blow open at t = 1.15 seconds.

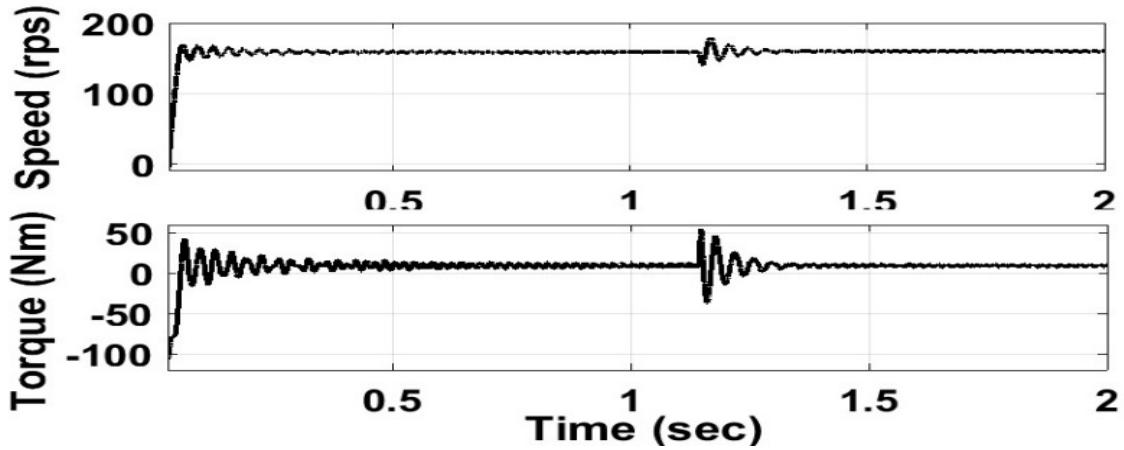


Fig.4.13 Nine level inverter speed and torque under normal and after short circuit fault clear

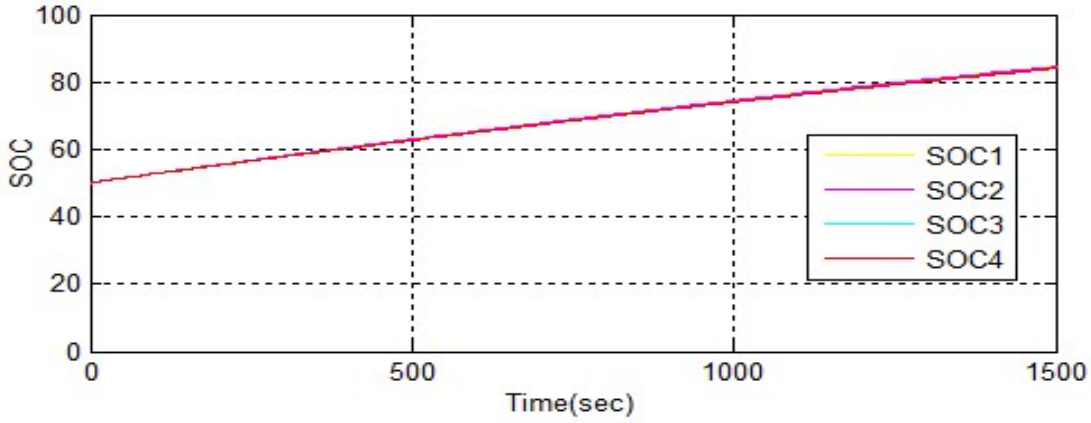
As discussed in the preceding section, this changes the SC failure into an OC one. When switch "Sa8" is activated, a voltage level known as "V1" is produced. As a result, a seven-level output voltage waveform begins to generate instantly. At time t = 1.6 seconds, a subsequent SC failure on switch S6 is taken into consideration. When switch S6 experiences a SC failure, S6 is shorted out once more. The matching fuse, "F6," is thought to blow open at t = 1.6 seconds in Figure 4.12. As discussed in the preceding section, this again turns the short circuit into an open circuit failure scenario. The speed and torque under normal and after short circuit fault clear is shown in Figure.4.13. In contrast to the pre-fault one, the five-level output voltage production that occurs when switch Sa9 is activated has the same peak-to-peak voltage magnitude.

C. Simulation Results under Energy Balancing Operation

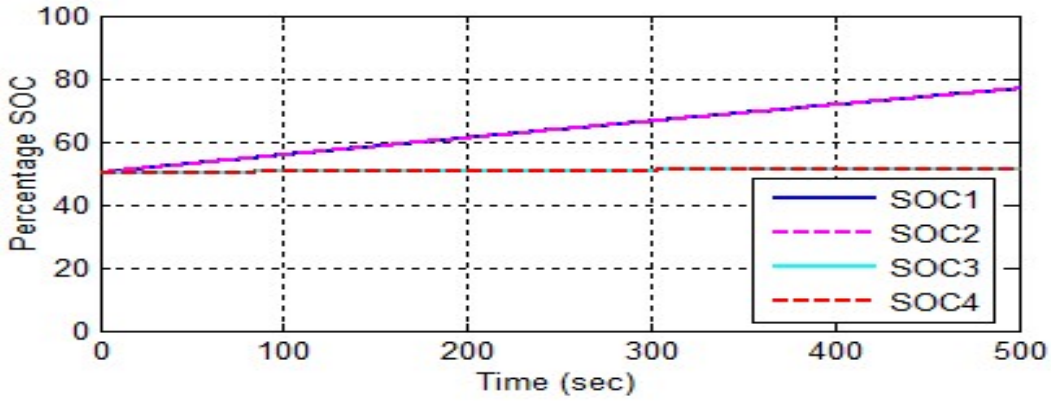
All of the batteries have been charged to unequal SOC levels in order to assess the suggested topology's energy balancing capacity (for example, the first battery connected to Vdc1 is kept at 60%, the second battery is at 80%, and so on.).As was said in the preceding section, Figs. 4.14 (a) & (b) show that the suggested energy balancing control technique is employed to minimize the difference in the SOCs of the four batteries. The modulation index affects how much energy is transmitted to the load at each voltage level. For a modulation index of 0.98 at a higher voltage level (Vdc), roughly 52% of the total energy is transmitted to the load. In contrast, it makes up 28%

of the total energy at the medium voltage level (0.75 Vdc), 14% at the medium voltage level (0.5 Vdc), and 6% at the lower frequency level (0.25 Vdc). The possible source choices for every voltage level are listed in Table 4-3.

The derivations shown in the previous section are supported by these percentages [80]. It shows that the source V1 must supply power to the load in order to produce voltage levels of Vdc, 3Vdc/4, Vdc/2, and Vdc/4. V1 thus releases its energy more quickly than the other sources. As shown in Table 4-3, the study recommends utilizing many redundant source combinations for each voltage level in order to balance energy across all four sources. During 3Vdc/4 and Vdc/2 voltage levels, the source combination (V2, V3, V4) and (V3, V4) can be employed to prevent the quicker discharge of source V1. This method can be used to control SoC imbalance at different voltage levels.



(a)



(b)

Fig.4.14 (a) & (b) Difference in SOC of batteries1, 2, 3&4 [Y-axis Difference in SOC of batteries; X-axis 100sec/div]

4.5 Summary

A nine-level inverter topology with single, multiple switch fault tolerant capability and energy-balancing between sources for solar water pumping applications is presented in this chapter. With the increase in the global effect of natural resources, various methods to pump water are the need of the hour. The Solar pumping market proves to be the way for the future. Energy concerning each level of voltage is presented in the form of equations in this chapter. Based on the redundant switching patterns of middle voltage levels, energy calculations for individual sources for various topologies can be obtained. According to the theoretical analysis, the simulation results are observed and the Energy Balancing issue is resolved. For multi-source SWPS applications, a three-phase MLI Topology is presented in this paper. With the help of 4 individual PV sources, the proposed MLI gives the motor load a 9-level voltage. This specific geography gives an arrangement to energy dividing among the sources at the hour of partial- shading causing batteries with uneven charging. Both the results of normal and energy-unbalancing conditions are discussed in this chapter. The numerical examination for energy supplied in the course of every voltage stage and restriction conditions is delivered in this chapter. Using “MATLAB/SIMULINK” the simulation results are validated.

CHAPTER 5
HARDWARE RESULTS AND DISCUSSIONS

5.1 Introduction

In this chapter, A Nine level Fault tolerant based multi-level inverter (9-LMLI) using phase disposition pulse width modulation (PD-PWM) strategy with an experimental prototype to verify the performance of proposed inverter described in Chapter 4. The design of each component is elucidated with essential circuit schematics with a pictorial view. The dawn of the 20th century marked the inception of the effective usage of renewable energy sources for applications across a plethora of fields. Agriculture being at the centre has seen drastic changes over the decades in how technological advancements lead to efficient working systems. One such new age topology is presented, where an advanced fault-tolerant multi-level is designed for a Solar-based Water Pumping System. The topology is also equipped with Energy Balancing capabilities thereby functioning as a reliable source of application. The control of the inverter Topology is done by using the PD-PWM technique and the necessary algorithm is implemented using the FPGA controller. Both fault tolerant and Energy Balancing capability is analysed using "MATLAB/SIMULINK" and a working hardware prototype is built for the same.

The real-time operation of proposed Topology with experimental setup is validated using field programmable gate array (FPGA) controller. The responses are realized in the subsequent sections using a digital signal processor (DSO).

5.2 Experimental Setup

In this part, we will demonstrate the complete creation of a physical model of the 9-level MLI supplied with a 3-IM drive, showcasing its capacity to balance energy and tolerate faults during water pumping operations. FPGA controllers are utilized in an open-loop system for control purposes, particularly in PWM communication and synchronization, modulation of the system, and generating regulated output waveforms. To generate the switching signals, a digital controller was developed utilizing VHDL and a PD-PWM strategy. The PD-PWM technique, which is a shortened form of PWM, was utilized. A set of experimental outcomes that cover both pre- and post-fault operation are presented.

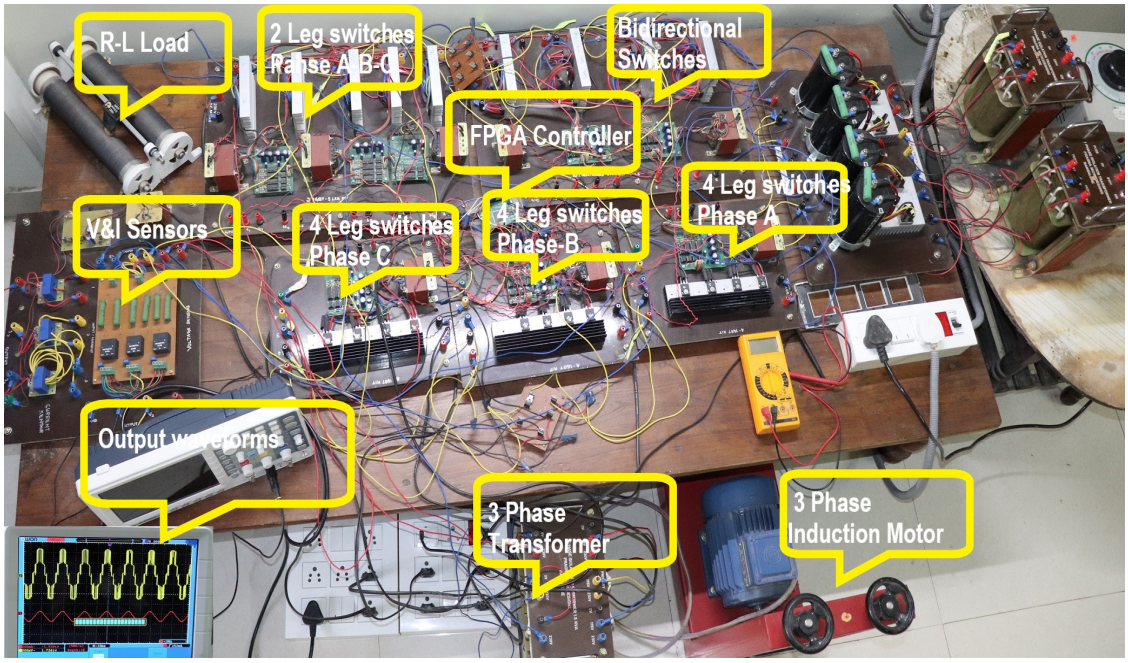


Figure 5.1 Hardware Prototype of Nine level Inverter with fault tolerant ability

5.3 Full-scale low-voltage hardware prototype Implementation-Experimental Results

A nine-level Multilevel Inverter with Energy Balancing and fault handling was created as a fully functional, small-scale model. The 3-phase induction motor that will be used in this model's water pumping applications will be powered by it. A representation of the working prototype is shown in Figure 5.1. Utilizing a Spartan-6 XC6SLX9 FPGA from Xilinx, the validated and synthesized controller is implemented in this section. The nine-level inverter of the low-power prototype was scaled down in the lab and evaluated, as shown in Figure 5.1. The system includes a Xilinx FPGA: Spartan-6 XC6SLX9 board that generates the gating signals for the inverters and performs all necessary computations in accordance with the control scheme shown in the Table and provides for the gating signals of inverters. With reference to pre &post-fault for Energy Balancing and fault tolerant ability of 9-L MLI fed 3- IM drive for water pumping applications operating conditions, an entire set of open-loop (Fig. 5.1) experimental results using phase disposition modulation techniques are presented in this section. This is done based on the simulation results provided in previous chapters.

Figures 5.2, 5.3, and figure 5.4, respectively, show how the suggested inverter performs under typical conditions with the motor load. The bottom image displays the load voltage waveform, and the top figure depicts the load current waveform. The 8 volts per division scale used in Figure 5.1 is used. It can be seen from Figure 5.2 that the load voltage has nine levels, including 4V, 8V, 16V, 24V, and 0V.

System experimental specification:

Each voltage source = 24V and Total voltage = 96V (24Vper source and 4 sources overall) for the prototype testing with necessary precautions. Reference signal frequency (fref)=50Hz, carrier signal frequency (fs)=4000Hz, Dc link capacitor=4700μF, Modulation Index =0.98 for normal operation, 0.66 for single switch, 0.3 for multi switch fault operation, 3-Phase Induction Motor, 415V, 1480rpm.

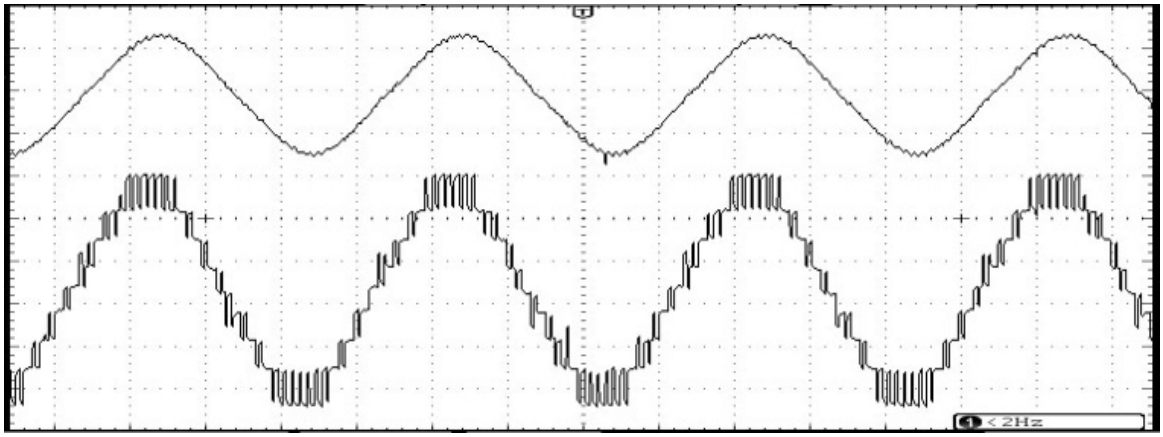


Figure 5.2: Phase Voltage & Current: Va & Ia for 9-level operation under normal condition

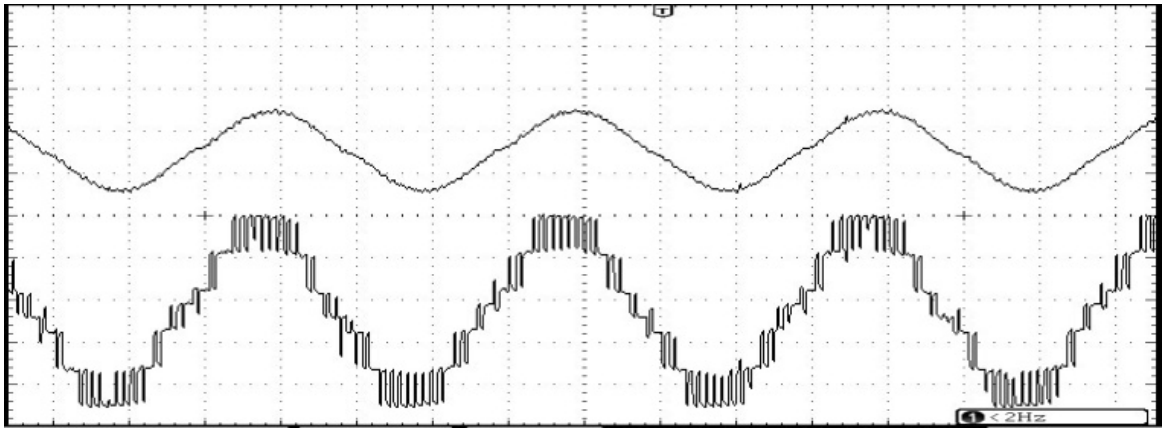


Figure 5.3: Phase Voltage & Current: Va & Ia for 7-Level under fault condition.

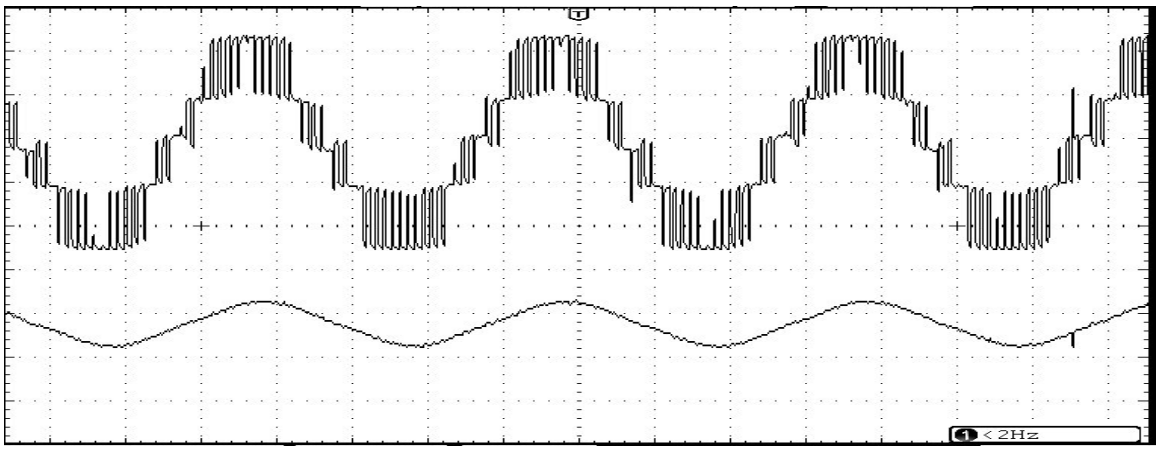


Figure5.4: Phase Voltage & Current: Va & Ia for 5-Level under fault condition

5.3.1 Power Semiconductor Devices (PSD):

In general, the insulated-gate bipolar transistor (IGBT) is having more demand for choosing as a PSD for assembling medium-frequency inverter with low cost. Due to some key features the IGBTs are more suitable for grid connected inverter applications as compared to metal-oxide-semiconductor field-effect transistors (MOSFETs).

5.3.2 IGBT selection:

The selection IGBT is mainly depends upon the following ratings.

a) Voltage rating
b) Current rating
c) Temperature of Junction

Voltage rating: The device is typically rated to ensure the applied maximum peak collector-emitter voltage is approximately 20% lower than its actual. It promises that durin the transient operation is sufficient margin is available.

Current rating: The safe operating area (SOA) curve shows that the maximum current a device can withstand is limited by the bond wire current capacity. It is advised to keep the device's current level 20% below this figure at all circumstances.

Junction temperature: It is advised to make sure the device junction temperature is no more than 25°C lower than the maximum rating of 150°C or 175°C when running under normal conditions. According to this constraint, the heat-sink construction and cooling mechanism is employed.

5.4 Comparison with recent fault-tolerant topologies

An appropriate comparison with traditional and recently published MLIs is made in order to demonstrate the advantages of the proposed FT-MLI. The stated comparison is summarized in Table 5. The comparison demonstrates that the experimental setup with fewer components is required for the proposed FT structure's reliable operation [81]. The conventional topologies NPC, FC, and CHB do not have FT operation, despite the fact that the structure in [82] and NPC contain additional circuitry such as clamping diodes, which increase the number of components. In addition to having a low switch count, the proposed FT-MLI is highly capable of CHB. In the event of a single OSF, the structures in [53] have higher switch counts and FT capability, but they are unable to produce output voltage in the event of multiple switch failures. The FT-MLI [83] is highly capable of presenting FT-MLI in the event of a multi-switch failure and requires additional switches.

- The major attainments of the proposed Topology are fault tolerance to semiconductor switch failures.
- This comparison leads to a conclusion where the proposed multilevel inverter is a better choice for water pumping applications. The fault tolerant ability of the Topology has been validated by MATLAB/SIMULATION results. An optimized source distribution scheme for a nine-level inverter fed with four PV sources is presented.
- The results 9-L, 7-L, 5-L & 3-L show the ability of proposed Topology working under single and multiple switch failures.
- The performance of new 9-Level MLI Topology for Solar Water Pumping Application is simulated using MATLAB and implemented using hardware setup with FPGA controller and found satisfactory during switch failures and Energy Balancing issue.

Table 5: Performance comparison of nine-level voltage inverters

Components		In conventional topologies			Recent multi-level topologies proposed in the literature				Proposed Topology
		NPC	FC	CHB	[84]	[85]	[53]	[86]	
Main Switches		48	48	48	57	21	27	42	24
Clamping Diodes		144	0	0	0	0	0	0	30
Sources		8	8	12	14	3	2	4	4
Flying Capacitors		0	72	0	0	6	6	6	0
Energy Balancing capabilities		No	No	No	No	No	No	Partially Yes	Yes
Reliability for various faults	Switches	No	No	No	Yes	Yes	Partially Yes	No	Yes
	Source	No	No	No	No	No	No	No	Yes

5.5 Summary

This chapter presents an optimized source distribution scheme fed by four photovoltaic sources into a nine-level inverter. The average operating modulation index and equivalent load demand are used to divide the PV modules. In a similar vein, the modified rating of the sources is used to determine battery ratings, ensuring optimal source utilization. For the nine-level inverter, a thorough mathematical analysis has been conducted to determine how well each source can be loaded. Two additional switches are added to the traditional cascaded T-type 9-level inverter in order to increase its fault tolerance capacity. In the event of an open circuit switch failure, the modified inverter's switching redundancy helps to provide power either with/without adjusting the voltage-levels. The outcomes demonstrate the suggested Topology's functionality in both fault and normal scenarios. The suggested plan has been simulated using MATLAB Simulink. A laboratory prototype has been used to aid in the experimental validation process.

6. CONCLUSIONS AND FUTURE SCOPE

6.1 General

This chapter outlines the thesis, discusses its importance, enumerates the advantages of the current work, and imparts directions for future research. Based on the observation, a few conclusions and scope for future work are listed

6.2 Conclusion

With the increase in the global exploitation of natural resources, effective methods to pump water are the need of the hour. Solar-based water pumping systems prove to be the way forward moving towards the future. The multi-level inverter Topology equipped with this Solar-based system is studied and an enhanced version is presented in this thesis. Energy with respect to each level of voltage is presented in the form of equations. Based on the switching patterns, energy calculations for individual sources for various topologies can be obtained using these equations. According to the theoretical analysis, the simulation results are also observed. For multi-source SWPS applications, a three-phase MLI Topology is presented in this thesis. With the help of 4 individual PV sources, the proposed MLI gives the motor load a 9-level voltage. This specific geography gives an arrangement to energy dividing among the sources at the hour of partial- shading causing batteries with uneven charging. Thereafter, a fault-tolerant Topology of a 5-level MLI for Solar water pumping applications is proposed. The significant achievement of the proposed Topology is adaptation to the failure to semiconductor switches. A complete correlation is done regarding the modified inverter with the traditional multilevel inverter. This examination prompts, where the proposed inverter is a superior decision for solar water pumping applications. The fault-tolerant ability of the Topology has been validated by simulation results.

After this, a nine-level MLI with Energy Balancing and fault-tolerant capabilities for solar-based is presented. A thorough examination is finished concerning the altered inverter with the customary multilevel inverter. The modulation procedure utilized in the new topology is the pulse width modulation technique with phase disposition standard. The tolerance for fault capability of the given idea is verified by MATLAB

results. The more desirable inverter with the ability to switch redundancy at the time of open circuit and short circuit switch failures work to deliver energy by operating on the voltage ranges. The consequences show us the capability of the Topology to work under single and multiple of switch failures. The running of the motor-drive combination is proved efficient at the point of starting, steady state, transient conditions, and switch failures. These results prove that the proposed multilevel inverter can be a better selection for applications related to Solar-based water pumping systems. A real-time hardware prototype is built and tested to prove the fault-tolerant and energy-balancing capabilities of the proposed multi-level Topology.

6.3 Future Scope:

The exploration of fault-tolerant multilevel inverter topologies for solar water pumping systems presents a robust system for enhancing reliability in renewable energy applications. By examining switch open circuit faults and expanding this analysis to encompass short circuit scenarios and grid integration, we lay the groundwork for more resilient inverter designs.

The implications of these findings extend beyond solar pumping, indicating potential adaptations for diverse applications such as induction motors and electric vehicles. Notably, the distinct requirements of solar pumping systems, such as variable load conditions and energy efficiency, demand tailored approaches that differ from traditional loads.

Future research should delve into the specific impacts of different load types on inverter performance, while also considering the broader applications of these systems in both grid-connected and off-grid scenarios, as well as their integration into micro grids. This comprehensive approach not only enhances the viability of solar water pumping but also paves the way for innovative solutions across various sectors in the renewable energy landscape, including electric vehicles and ship propulsion systems, further expanding the horizon for sustainable technologies.

APPENDIX-A

System simulation specification:

Input single DC voltage=100 V, Reference signal frequency (fref)=50Hz, carrier signal frequency (fs) = 2kHz, Modulation Index =0.98 for normal operation, 0.66 for single switch, 0.3 for multi switch fault operation, on-state voltage drop of IGBT (Von) = 0.0054V, On-state Resistance (Ron)=0.8Ω, Energy losses when the IGBT switch is on (Eon-s) =1.21W,. 3-Phase Induction Motor, 415V,1480rpm

APPENDIX-B

System experimental specification:

Input each DC voltage=24V, Reference signal frequency (fref)=50Hz, carrier signal frequency (fs) = 2000Hz, Dc link capacitor=4700μF, Modulation Index =0.98 for normal operation, 0.66 for single switch, 0.3 for multi switch fault operation 3-Phase Induction Motor, 415V,1480rpm

APPENDIX-C

VHDL Program for Implemention

FPGA Programme:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
use IEEE.NUMERIC_STD.ALL;
-- Uncomment the following library declaration if instantiating
-- any Xilinx primitives in this code.
--library UNISIM;
```

```
--use UNISIM.VComponents.all;
entity threephaseninelevel is
port (clk :in  std_logic;
      pwm1 : out std_logic;
      pwm2 : out std_logic;
      pwm3 : out std_logic;
      pwm4 : out std_logic;
      pwm5 : out std_logic;
      pwm6 : out std_logic;
      pwm7 : out std_logic;
      pwm8 : out std_logic;
      pwm9 : out std_logic;
      pwm10 : out std_logic;
      pwm11 : out std_logic;
      pwm12 : out std_logic;
      pwm13 : out std_logic;
      pwm14 : out std_logic;
      pwm15 : out std_logic;
      pwm16 : out std_logic;
      pwm17 : out std_logic;
      pwm18 : out std_logic;
      pwm19 : out std_logic;
      pwm20 : out std_logic;
      pwm21 : out std_logic
      );
end three phase nine level;
architecture Behavioral of three phase nine level is
signal a1 : integer range 0 to 3600:=0;
signal a2 : integer range 0 to 3600:=1200;
signal a3 : integer range 0 to 3600:=2400;
signal sine1 : integer range -2047 to 2047:=0;
signal sine2 : integer range -2047 to 2047:=0;
```

```
signal sine3 : integer range -2047 to 2047:=0;
signal tri1 : integer :=0;
signal tri2 : integer :=0;
signal tri3 : integer :=0;
signal tri4 : integer :=0;
signal tri5 : integer :=0;
signal tri6 : integer :=0;
signal tri7 : integer :=0;
signal tri8 : integer :=0;
signal z4 :integer :=0;
begin
-- Setting frequency
process (clk)
begin
if (rising_edge(clk)) then
if (count= 139)then
clk_out<= not (clk_out);
count <= 0;
else
count <= count+1;
end if;
if (count1= 34)then
clk_out1 <= not (clk_out1);
count1 <= 0;
else
count1 <= count1+1;
end if;
end if;
end process;
-- Generation of triangular Signal
process(clk)
begin
```

```
if(rising_edge(clk_out1)) then
z4 <= z4+1;
if (z4 <= 540) then
tri1 <= (z4+1620);
tri2 <= (z4+1080);
tri3 <= (z4+540);
tri4 <= z4;
tri5 <= (z4-540);
tri6 <= (z4-1080);
tri7 <= (z4-1620);
tri8 <= (z4-2160);
elsif ((z4 >= 540) and (z4<=1080)) then
tri1 <= (2700-z4);
tri2 <= (2160-z4);
tri3 <= (1620-z4);
tri4 <= (1080-z4);
tri5 <= (540-z4);
tri6 <= (-z4);
tri7 <= (-z4-540);
tri8 <= (-z4-1080);
elsif (z4>=1080) then
z4<=0;
end if;
end if;
end process;
-- Generation of sine wave modulating signal for A-phase
process(clk)
begin
if(rising edge(clk_out)) then
sine1 <= 2*sine(a1);
a1 <= a1+ 1;
if(a1 = 3600) then
```

```
a1 <= 0;
end if;
end if;
if(rising edge(clk_out)) then
sine2 <= 2*sine(a2);
a2 <= a2+1;
if(a2 = 3600) then
a2 <= 0;
end if;
end if;
if(rising edge(clk_out)) then
sine3 <= 2*sine(a3);
a3 <= a3+1;
if(a3 = 3600) then
a3 <= 0;
end if;
end if;
end process;
process(clk)
begin
```
PWM logic for switch S1
```
if(rising edge(clk)) then
if((sine1>=tri1)or((sine1>=tri2)and(sine1<=tri1))or((sine1>=tri3)and(sine1<=tri2))or((s
ine1>=tri4)and(sine1<=tri3))or((sine1>=tri5)and(sine1<=tri4))) then
                dpwma1<='1';
        else
                dpwma1<='0';
end if;
end if;
```

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LIST OF PUBLICATIONS

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1. Mucherla, Narasimha Rao, Nagaraj Karthick, and Airineni Madhukar Rao. "Fault tolerant nine-level inverter topology for solar water pumping applications." International Journal of Electrical and Computer Engineering (IJECE) 12.4 (2022): 3485-3493.

Journals under review:

1. Fault Tolerant Ability and Energy Balancing Capability of Multi-Level Inverter Fed 3-Phase Induction Motor for Solar Water Pumping Applications to IEEE Journal of Emerging and Selected Topics in Power Electronics.

Conference papers:

1. M. N. Rao, N. Karthick and A. M. Rao, “Fault Tolerant Ability of A Multi Level Inverter Fed Three Phase Induction Motor for Water Pumping Application,” 2021 7th International Conference on Electrical Energy Systems (ICEES), Chennai, India, 2021, pp. 212-216, doi: 10.1109/ICEES51510.2021.9383689.
2. M. N. Rao, N. Karthick and A. M. Rao, “Energy Balancing Capability of a Three Phase Nine-Level Inverter for Solar Water Pumping Applications,”2022 2nd International Conference on Power Electronics & IoT Applications in Renewable Energy and its Control (PARC), Mathura, India, 2022, pp. 1-6, doi: 10.1109/PARC52418.2022.9726255.