DESIGN AND PERFORMANCE OPTIMIZATION OF MODIFIED TUNNEL FIELD EFFECT TRANSISTOR (TFET) FOR HIGHLY EFFICIENT, LOW POWER, DIGITAL VLSI CIRCUIT APPLICATIONS

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By

Sabitabrata Bhattacharya

Registration Number: 41900709

Supervised By

Dr. Suman Lata Tripathi (21067)

School of Electronics and Electrical Engineering (Professor)

Lovely Professional University

LOVELY PROFESSIONAL UNIVERSITY, PUNJAB

2024

DECLARATION

I, hereby declared that the presented work in the thesis entitled "**Design and Performance Optimization of Modified Tunnel Field Effect Transistor (TFET) for Highly Efficient, Low Power, Digital VLSI Circuit Applications**" in fulfilment of degree of **Doctor of Philosophy (Ph. D.)** is outcome of research work carried out by me under the supervision of **Dr. Suman Lata Tripathi**, working as **Professor**, in the **School of Electronics and Electrical Engineering** of Lovely Professional University, Punjab, India. In keeping with general practice of reporting scientific observations, due acknowledgements have been made whenever work described here has been based on findings of other investigator. This work has not been submitted in part or full to any other University or Institute for the award of any degree.

(Signature of Scholar)

Name of the scholar: **SABITABRATA BHATTACHARYA**

Registration No.: **41900709**

Department/school: **Electronics & Communication Engineering**

Lovely Professional University,

Punjab, India

CERTIFICATE

This is to certify that the work reported in the Ph. D. thesis entitled "**Design and Performance Optimization of Modified Tunnel Field Effect Transistor (TFET) for Highly Efficient, Low Power, Digital VLSI Circuit Applications**" submitted in fulfillment of the requirement for the award of degree of **Doctor of Philosophy (Ph.D.)** in the **Electronics & Communication Engineering Department**, is a research work carried out by **Sabitabrata Bhattacharya**, **(41900709)**, is bonafide record of his original work carried out under my supervision and that no part of thesis has been submitted for any other degree, diploma or equivalent course.

(Signature of Supervisor)

Name of supervisor: **Dr. Suman Lata Tripathi**

Designation: **Professor**

Department/school: **School of Electronics and Electrical Engineering**

University: **Lovely Professional University, Punjab, India**

ABSTRACT

In today's scenario VLSI Technology is growing by shrinking its unit modules or the transistors. MOSFETs which has ruled the VLSI market for almost three decades is now becoming unable to follow the Moore's law pattern due to its thermionic limitation of subthreshold slope and rapidly increasing short channel effects (SCEs) in the nanometre regime. A new device at least as much efficient as the MOSFET but prone to it's scaling limitation is the need of the hour. TFET is one such candidate. It is structuring very similar to MOS but it's operating principle is entirely different. But it has certain other limitations like poor ON current and ambipolarity. The present research focuses on fighting these limitations of TFET by performing structural, geometrical and material modifications in it. Firstly, the research introduces the VLSI domain, it's advent and evolution to it's present state. Then the motivation behind taking up the Tunnel FET device is illustrated. Next the conventional structure of the TFET and it's structural similarities and differences with MOSFET is explained. After that all the digital and analog/RF performance parameters for estimating the efficiency of a TFET structure are introduced in detail. Two Simulation tools, viz Cogenda Visual TCAD and Silvaco Atlas are extensively used throughout the research. A brief introduction to both the tools are given. A detailed literature survey is done on almost all the variations of TFET device proposed by researchers from time to time until the present day. Some researchers have proposed Double Gate structure for better control over the channel current. Much research is done on engineering the gate dielectric to high-k and low -k combination in place of a single oxide layer. Heterogenous metal combination for the gate contact is also used by some researchers to have a variation of metal work functions to bring about better performance. Junctionless or dopingless techniques are also employed, like charge plasma to form a n electrically induced junction in place of a permanent on to avoid leakages. To increase the tunnelling phenomenon lower bandbap materials are also utilised.Some researchers applied vertical channel to have transverse tunnelling along with the lateral counterpart so as to increase the overall drive current. Many application orientated research is also done to use the TFET device for Bio-molecule sensors etc. We firstly developed a novel device called n channel JL DG TFET with a SiGe p+ pocket towards the source and optimised it with respect to 4 metrics, viz channel length, gate metal -oxide combination, mole fraction of Ge in the pocket and temperature and designed the optimum structure and verified it for efficiency with rigorous simulations. Next, we developed p-JL DG TFET with similar procedure and with the combination of both designed an inverter circuit and verified its

performance. Next, we designed two transmission gate (TG) circuits using our constructed and optimised complementary JL DG TFET and JL SG TFET with SiGe source pockets. The device performed well above expectations. Finally, we concluded our research with the development of yet another well-established circuit the 2x1 Multiplexer (MUX) using the complementary JL DG TFET and the TG made using it.

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First and foremost, I am thankful to the almighty for making things possible at the right time. I owe my success to my supervisor and would like to sincerely thank Dr. Suman Lata Tripathi for her guidance. I greatly appreciate her support, positive attitude, and her vast knowledge in a wide range of topics. Her guidance not only in terms of giving ideas and solving research problems, but also in terms of giving freedom to do research in my own ways has proved to be useful and invaluable. I am deeply influenced by my supervisor's way of guidance and sincerely thankful for standing by my side in tough times. I would like to thank my wife Raka Chatterjee, for her unconditional love, support, and encouragement. Last but not least, I would like to thank my family (especially my mother and son) and my friends for their continuous love and support. Finally, a special thanks to all the people who helped me in direct and indirect ways to accomplish this work.

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CHAPTER 1

INTRODUCTION

1.1 Brief History of VLSI Design

First solid-state transistor was invented in 1947 at Bell Labs. First integrated circuit was developed by Jack Kilby at Texas Instruments. Intel launched its Itanium processor in 2008 which consists of 2 billion transistors. The above growth rate corresponds to about 53% in about 50 years. This unprecedented growth has not been shown by any other industry for such a long span of time and it is continuing till this day. This great advancement in the field of VLSI and electronics at large emerged from steady scaling down of transistors and huge improvisations in the fabrication steps. Generally, there is always a trade-off between cost, power consumption and efficiency in most of the engineering industries, but for the case of VLSI the converse became true as when transistors were scaled down their speed increased, power consumption became much lesser, and cost decreased manifolds. This converse nature of the VLSI industry helmed the great progress of electronics and society as well. A teenager's iPod now contains the memory required for an entire company's accounting system.

Integrated circuit advancements have changed the face of warfare, made space travel possible, improved the safety and fuel economy of cars, added a great deal of human knowledge to Web browsers, and flattened the planet. About 6 quintillion (6×10^{18}) transistors, or almost a billion for each person on the earth, were produced by the industry in 2007. Numerous engineers have achieved financial success in this domain. Those with creative ideas and the ability to make them a reality are going to reap new rewards. Electronic circuits in the early half of the 20th century used bulky, pricy, power-hungry, and unstable vacuum tubes. At Bell Laboratories, John Bardeen and Walter Brattain constructed the first operational point contact transistor in 1947. Although Bell Labs almost declared it a military secret, the gadget was unveiled to the public the next year. A decade later, Jack Kilby from Texas Instruments recognised the possibility of miniaturisation provided more than one transistor could be constructed on a single silicon piece. His initial integrated circuit prototype was made with gold wires and a slice of germanium. Bardeen, Brattain, and William Shockley, their mentor, were awarded the 1956 Nobel Prize in Physics for creating the transistor. Kilby's development of the integrated circuit earned him the 2000 Nobel Prize in Physics.

Consider transistors as electrically operated switches that have two extra terminals which are either detached or connected based upon the current or voltage applied at the

controlling terminal. Transistors have a controlling terminal called control. Bell Laboratories created the BJT or bipolar junction transistor not long after the invention of point contact transistors. In terms of dependability, noise level, and power efficiency, bipolar transistors were superior. Primarily, bipolar transistors or BJTs were only employed in early integrated circuits (ICs). To switch much greater currents between the other 2 terminals (the collector & emitter terminals), BJTs or bipolar junction transistors need to supply a very tiny amount of current through the base or the control terminal. It is not possible to integrate more transistors onto a single die than this due to the quiescent amount of power dissipated by the base currents, which flows even when the circuit is not undergoing switching.

Metal Oxide Semiconductor Field Effect Transistors, or MOSFETs, started to be produced by the 1960s. The main advantage of MOSFETs is that, when they are idle, they consume negligible control current. MOS devices are available in 2 flavours: n channel MOS & p channel MOS, which utilizes silicon that is n type or p type, respectively. FETs or Field Effect Transistors were first conceptualised in the year 1925 by the German physicist Julius Lilienfield. In the year 1935, Oskar Heil proposed a device that was similar to the MOSFET. However, early attempts to make working devices were thwarted by issues with the materials. The early MOSFET based logic circuits were described in the year 1963 by Frank Wanlass of Fairchild[1]. Fairchild's gates gave rise to the term complementary metal oxide semiconductor, or CMOS, because they incorporated both nMOS and pMOS transistors. Despite using discrete transistors, the circuits' power consumption was just nanowatts, which is almost five orders of value lesser than that of their bipolar equivalents. MOSFET based ICs or integrated circuits gained popularity as a result of their very low cost and simpler fabrication method, which resulted from the development of the silicon planar process and smaller area required for each transistor[2]. Early commercial processes had low yield, reliability, and performance since they solely employed pMOS transistors.

In the 1970s, nMOS transistor processes became widespread[3]. With its 4004 4-bit CPU and 1101 256-bit static RAM, Intel was the first company to proceed further with the nMOS technology. Despite being less expensive to produce than CMOS, nMOS logic gates still required much more power to operate. With the integration millions of transistors into a unit chip in the 1980s, power consumption emerged as a significant concern. Almost, for all digital logic applications, CMOS techniques have largely taken the place of nMOS and bipolar processes due to their widespread adoption.

1.2 Moore’s Law and its continued significance

Plotting the number of transistors that may be produced on a chip most profitably results in an uninterrupted line on a semilogarithmic scale, as Gordon Moore noted in 1965 [4]. He discovered that the transistor count doubled every 18 months at the time. Moore's Law is the name given to this insight, which has come to pass as a self-fulfilling prophecy. Since the 4004's inception, the total quantity of transistors in the processors manufactured by Intel has doubled every 26 months. Building bigger chips and, to a lesser degree, shrinking transistor size are the main forces behind Moore's Law. Fig.1.1 depicts the plot of Moore’s Law in its present form.

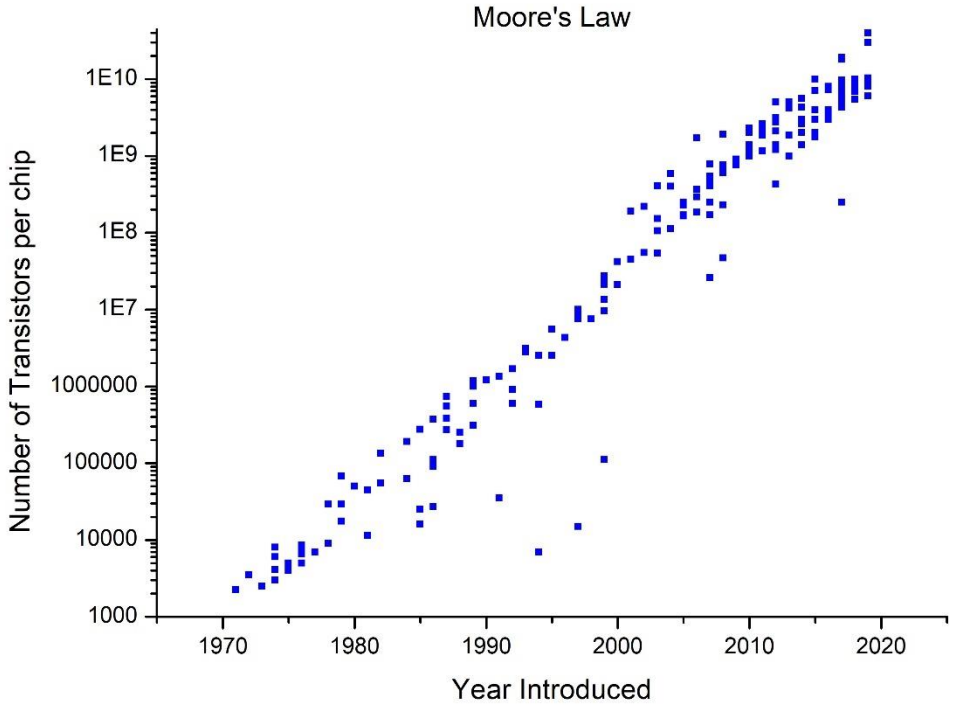


Fig1.1 Moore’s Law

Chip integration has been divided into four categories: small-, medium-, large-, and very large-scale. Circuits that use small-scale integration (SSI), like the 7404 inverter, have less than ten gates and about six transistors per gate. Circuits classified as medium-scale integration (MSI) include the 74161 counter, which has up to 1000 gates. Up to 10,000 gates can be found in (LSI) large-scale integration circuits, which include basic microprocessors of 8-bits. Once it was realised that if this naming trend persisted, newer names would need to be coined every 5

years, most integrated circuits built after the 1980s is referred to as very large-scale integration, or VLSI.

Dennard's Scaling Law[5] is a corollary to Moore's law, which states that transistors get faster, use less power, and are less expensive to produce as they get smaller. The clock frequency of Intel microprocessors has doubled approximately every 34 months. Around 2004, this frequency scaling reached its limit, and clock frequencies levelled out at 3 GHz. Even more sophisticated than raw clock speed is computer performance, as measured by the amount of time it takes to run an application. These days, a chip's number of cores determines performance rather than its clock speed.

Despite the fact that a single CMOS FET consumes very less energy when it switches, a massive number of transistors flipping at extremely fast speeds has once again made power consumption a crucial design factor. Furthermore, because transistors are now so tiny, they can no longer turn off entirely. When multiplied by a billion or more of transistors on a single chip, little current leaks via each transistor suddenly result in a large power usage. The smallest diameter of a transistor that can be produced with reliability is referred to as the feature size in a CMOS FET manufacturing flow process. In 1971, the 4004's feature size was 10 μm. In 2008, the Core 2 Duo's feature size was 45 nm. Every two to three years, manufacturers release a brand new process generation, which is also known as a technology node, that packs two times as many transistors in a similar area but has a 30% reduced feature size. Lower feature sizes are represented in nanometres (10^{-9} m), while feature sizes of the range of 0.25 μm are frequently expressed in microns (10^{-6} m). Effects including wire resistance, transistor leakage, and differences in the properties of neighbouring transistors, which were comparatively insignificant in micron processes, have a significant impact in nanoscale processes.

Due to the need for every business to stay ahead of its rivals, Moore's Law has continued to be a reality till date. Transistors obviously cannot be any smaller than atoms, hence this scaling cannot continue indefinitely. Dennard scaling has started to decelerate already. Designers are forced to choose between increasing power and decreasing delay by the 45 nm generation[6]. Cutting-edge techniques are limited to IC chips which will trade in large numbers or that have requirements of performance that are at the forefront of the industry, even though the expense of printing individual transistors is decreasing due to the exponential rise in one-time design expenses. Still, several fundamental constraints to scaling forecasts have already shown out to be incorrect. Getting ahead of the competition can provide billions of

dollars to creative engineers and material scientists. Experts predicted that scaling would go on for at least ten years in the early 1990s, but after that the future was uncertain. We continue to think that Moore's Law will hold true for at least ten more years in 2024.

1.3 Motivation behind selection of TFET for the present research

The trend of scaling electronic devices, which was initiated over 50 years ago by Gordon Moore's law, is still going strong. However, the thermionic limitation (60 mV/dec) on the subthreshold swing at ambient temperature has created a bottleneck for scaling using standard MOS devices[7]. Other drawbacks of scaling down MOS devices include higher junction and gate-oxide leakage [8], short channel effects such as Drain Induced Barrier Lowering (DIBL) and V_T lowering[9], among others. Researchers have occasionally suggested several devices to address the scaling down issues caused by MOS devices. The tunnel field effect transistor, or TFET, is one of the main candidates to replace MOS transistors in contemporary low power CMOS comparable circuits. The TFET, which has a highly doped p+ type material for the source, a highly doped n+ type material for the drain, and an intrinsic or minimally doped region for the channel, is essentially a reverse biassed P-I-N structure[10]. To provide very high input impedance, the gate is constructed over the intrinsic channel with a thin dielectric layer electrically shielding it from the channel. With the exception of the reverse doping at the source and drain regions, the structure of TFET and MOSFET are identical. Because of their similar structures, TFETs can easily replace MOSFETs in circuits that are compatible with CMOS technology [11]. However, in terms of functionality, TFET and MOSFET are completely different from one another since, in contrast to MOS devices, which primarily rely on thermionic emissions, TFETs generate the ON state current using the Band-to-Band Tunnelling mechanism (BTBT). To regulate the conduction of the reverse biassed PIN diode, the TFET gate essentially modifies the tunnelling current across it. Using them, subthreshold slopes significantly lower than 60mV/dec can be achieved because the thermionic emission is not included in the conduction of TFET[11], [12]. In comparison to MOS devices, TFETs have significantly lower dynamic power dissipation, or the power needed or lost when a state changes from high to low or vice versa[11], [13]. Because the TFET devices do not rely on thermionic emissions in any way for conduction, they have the characteristic of having very low OFF state current. They are highly effective in the construction of low power consumption SRAM cells and associative memory (AM) based on cellular neural networks (CNNs) because of their very low off state current & steep SS or subthreshold slope[14], [15]. Since there is a significant fluctuation in channel conduction due to variations in the gate material's dielectric

constant, dielectric engineering for the gate insulator is also used to boost the efficiency of the TFET. Applications for biomolecule sensors make use of the TFET current's exceptional sensitivity to changes in the gate oxide's dielectric constant[16], [17]. In addition, TFET-based devices are very helpful in low-power IoT, ML, and AI applications nowadays[15], [18], [19].

A few disadvantages of TFET devices are also present; the two main ones are very tiny ON state current value and ambipolar conduction, or conduction in the opposite direction when switched OFF. Researchers have suggested a number of altered topologies for the traditional TFET devices to lessen these shortcomings. Using numerous gates and gate-all-around structures is one practical strategy for improving ON current and improving channel conduction control [20], [21].The second method used to improve performance is dielectric engineering of the gate oxide, which involves utilising numerous dielectrics at the gate with different diameters and k values[22], [23]. In order to boost the overall ON current, the TFET can also be built vertically, resulting in lateral BTBT and vertical tunnelling [24]–[26] Asymmetric gates and changes to the channel's gate overlap/underlap can also be used to increase the ON current[27], [28].

1.4 Basic Structure of Tunnel FET

Now let's look at the fundamental design of a tunnel FET. The functioning concept of TFET is predicated on this fundamental configuration of regions, terminals and doping [29]; we shall go into numerous modifications of this structure in the literature review chapter. An n-channel TFET's fundamental construction is depicted in Figure 1.2(a). The source, channel, and drain are the three regions of the apparatus. When the architecture of an n-channel MOSFET and n-channel TFET is compared (Figure 1.2(c)), it can be observed that the MOSFET's source doping is n-type, while the TFET's is p-type. The sole significant distinction between a MOSFET and a TFET is this. Typically, the TFET's channel area is either intrinsic or very mildly doped. Figure 1.2(b) illustrates a p-channel TFET.

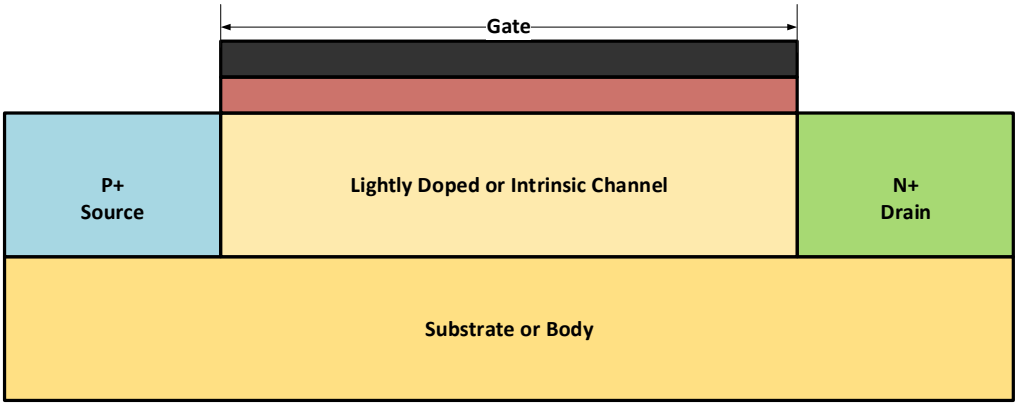


Fig1.2(a) Fundamental Architecture of n-TFET

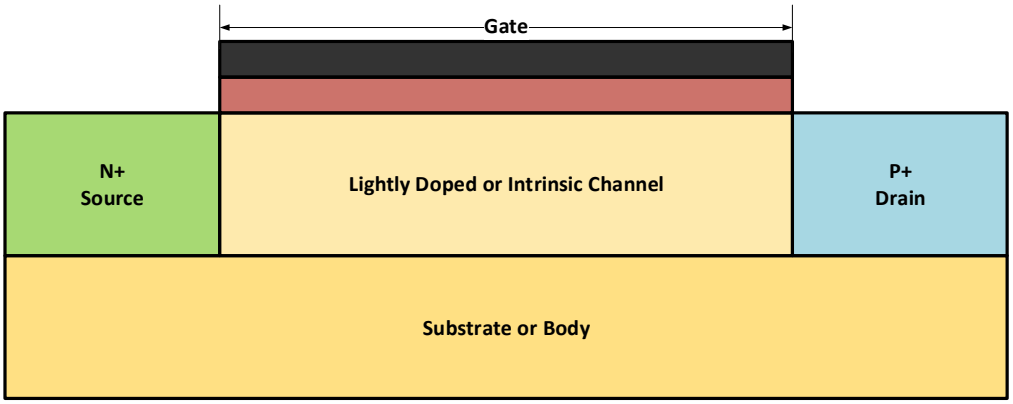


Fig1.2(b) Fundamental Architecture of p-TFET

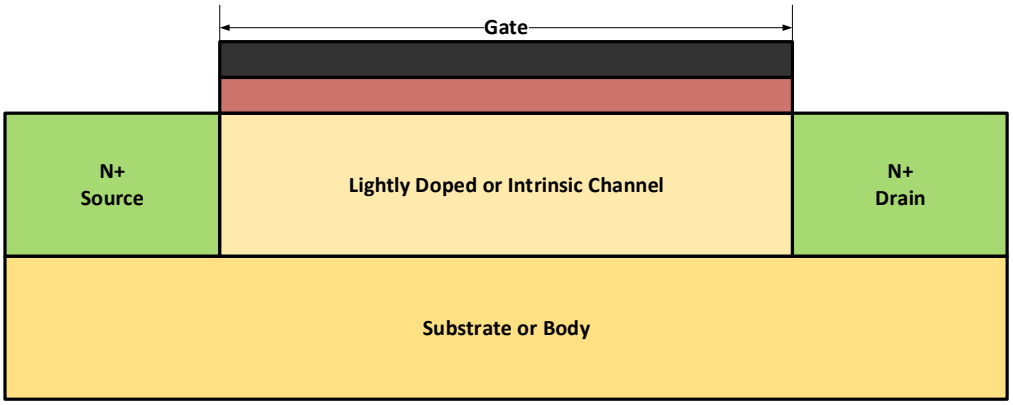


Fig1.2(c) Fundamental Architecture of n-MOSFET

1.5 Performance Parameters of Tunnel FET

In this section we will go through the major performance parameters of TFET viz. threshold voltage (V_T), subthreshold slope (SS), I_{ON}, I_{OFF}, drain induced barrier lowering (DIBL)**.** These are some of the major parameters on the basis of which we are going to compare the different structurally and geometrically modified versions of the basic TFET structure in the upcoming chapters.

1.5.1 Threshold Voltage

The lowest gate to source voltage necessary to start current conduction via a FET's channel is known as V_T or the threshold voltage. In the context of traditional MOS, it refers to the potential necessary at gate terminal for creation of inversion region in the channel, thus creating a conduit for the movement of charge carriers among the drain and source. However, in the context of TFETs, it can be seen as the lowest gate source voltage necessary to bring the channel's conduction band and source's valence band into alignment so that band to band (BTB) tunnelling among them can begin. The threshold voltage for a TFET is temperature independent.

1.5.2 Subthreshold Slope

The quantity of gate potential needed to cause a one decade variation in the drain current in the area below the threshold is known as the subthreshold slope[30]. It can be expressed mathematically as ratio of the variation in the gate's voltage to the variation in the logarithm of current at the drain, given as

$$S = \frac{dV_g}{d(\log I_d)} \text{ mV/dec} \tag{1.1}$$

The sub-threshold slope for standard MOS devices is determined to be entirely free of the gate to source potential & is provided as[31]

$$S_{MOSFET} = \frac{kT}{q} \ln 10 \left(1 + \frac{C_D}{C_{ox}}\right) \tag{1.2}$$

where kT⁄q is the thermal limitation of MOSFET devices, preventing them from having a minimum SS of 60mV/dec at T=300K (ambient temperature). C_D and C_{ox} are the device's

depletion and oxide capacitances. TFET devices, however, rely on the barrier of tunnelling near the junction of source & channel rather than temperature barrier. For a TFET, the subthreshold slope is provided below [32]

$$S_{TFET} = \frac{V_{GS}^2}{2V_{GS} + B_{kane} W_g^{3/2} / D} \tag{1.3}$$

Consequently, in contrast to MOSFETs, TFETs have a subthreshold slope that is mostly influenced by the gate voltage and very somewhat by the bandgap at the source-channel junction (tunnelling junction). So, it is evident that utilising low V_{GS} can result in a TFET with a sub 60mV/dec S value.

1.5.3 ON State Current

The ON state current (I_{ON}) of a TFET is a critical performance evaluation parameter that needs to be as large as feasible for optimal performance. This is nothing but the drain - source current (I_{DS}) that passes via the apparatus when the voltage between the gate and the source is higher than V_T. More concisely, it's the drain-source current, while the device is turned ON. At the source-channel junction, BTBT or Band-to-Band-Tunnelling of the electrons is the main reason for I_{ON}.

1.5.4 OFF State Current

I_{OFF} is used to represent it. It can be described as the amount of current that flows between the source and drain when the device is deemed off or when the gate to source voltage is less than the threshold voltage. I_{OFF} should ideally be moving towards zero, but in reality, because of a small subthreshold slope, it has a non-zero value. Because of several leakage processes and the ambipolar behaviour of TFETs, I_{OFF} has a small value, however it needs to be kept as little as possible for optimal performance.

Another crucial performance metric is the ratio of ON current to the OFF current. I_{ON}/I_{OFF} ought to be as large as feasible for the TFET to operate as efficiently as possible.

1.5.5 Drain Induced Barrier Lowering (DIBL)

The reduction in the V_{Th} or threshold voltage with elevated drain biases is caused by a sort of short channel effect called DIBL or Drain Induced Barrier Lowering. For the TFET to function as well as feasible, it must be as tiny as possible. The ON current depends heavily on the drain

voltage instead of gate voltage due to the high value of DIBL. It renders the device unusable and destroys its gate controllability. Its mathematical definition is the ratio of the difference between the highest and lowest drain voltages and the difference between the threshold voltages recorded at those values[33], and is represented as shown below,

$$DIBL = -\frac{V_{Th}^{high} - V_{Th}^{low}}{V_D^{high} - V_D^{low}} \tag{1.4}$$

The negative sign before the formula ensures that the value of the DIBL is always positive since the threshold voltage, V_T recorded at higher drain voltage is invariably lesser than that recorded at lower drain voltage. Drain Induced Barrier Lowering or DIBL is measured in mV/V, & it must be, as minimal as feasible.

1.6 Analog or RF performance metrics of TFET

For very low power transistors to work with today's high-speed CPUs, they need to have fast switching rates. TFET efficiency is determined by several key high-frequency performance factors, including transconductance (g_m), cut-off frequency (f_T), gain bandwidth product (GBP), and transit time(τ)[34].

1.6.1 Transconductance

Assuming the drain to source voltage remains constant, the transconductance (gm) of a TFET is determined by the rate at which the drain current changes to change the gate to source voltage. It is provided mathematically as,

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}}\Big|_{V_{DS}=constant} \tag{1.5}$$

It is graphically represented as the TFET's slope of transfer characteristic.

1.6.2 Cut-off Frequency

For analog/RF operations, one of the most significant performance characteristics is the cut-off frequency (f_T). It is described to be the frequency for which the short circuit current gain for small signals decreases to unity value.[34]. It is expressed as

$$f_T = \frac{g_m}{2\pi(C_{gs}+C_{gd})} \quad (1.6)$$

where the gate to drain capacitance is denoted by C_{gd} and the gate to source capacitance by C_{gs}. For optimal performance, the value cut-off frequency must be high.

1.6.3 GBP or the Gain Bandwidth Product

The next crucial RF performance characteristic is GBP, which is the trade-off between the device's gain & bandwidth. It oversees figuring out a circuit's selectivity. Typically, GBP or Gain Bandwidth Product is used to assess the device's efficiency at a DC gain value of 10[35] and is expressed mathematically as,

$$GBP = \frac{g_m}{20\pi C_{gd}} \quad (1.7)$$

1.6.4 Transit Time

The transit time, represented by τ, is another crucial factor that impacts the RF/ analog performance of TFET device. The transit time indicates how long it takes for the charge carriers to go from the device's source to the drain [34]. It serves as a gauge for the device's speed. It can be expressed mathematically as proportional to the reciprocal of the cut-off frequency,

$$\tau = \frac{1}{2\pi f_T} \quad (1.8)$$

1.7 TCAD Simulation Tools used in this research

TCAD or Technology Computer Aided Design, is a useful technique for cutting plan costs, improving the effectiveness of device design, and creating innovative and improved device designs. In this research two very efficient and widely used TCAD tools are utilized, viz Cogenda Visual TCAD tool and Silvaco ATLAS TCAD tool.

1.7.1 Cogenda Visual TCAD tool

Cogenda Visual TCAD tool is a comprehensive software solution designed to streamline the process of Technology Computer-Aided Design (TCAD) in semiconductor industries. Offering a user-friendly interface and powerful simulation capabilities, Cogenda Visual TCAD facilitates precise modelling and analysis of semiconductor devices and processes. Its intuitive visualizations enable engineers to efficiently explore device behaviour, predict performance, and optimize designs, ultimately accelerating product development cycles and enhancing overall efficiency in semiconductor research and development. The upcoming chapters will elaborate more on how the tool has been fully utilised for the present research.

1.7.2 Silvaco ATLAS TCAD tool

Silvaco's ATLAS TCAD tool is a cutting-edge software solution revolutionizing semiconductor device simulation. Renowned for its versatility and accuracy, ATLAS empowers semiconductor engineers to delve into the intricate physics governing device behavior with unparalleled depth. Its comprehensive suite of features enables precise modeling and analysis of various semiconductor devices, from transistors to solar cells, facilitating exploration across a broad spectrum of applications. ATLAS's robust simulation engine, coupled with its user-friendly interface, empowers researchers and engineers to predict device performance, optimize designs, and accelerate innovation cycles in semiconductor technology. By providing a powerful platform for in-depth analysis and exploration, Silvaco's ATLAS TCAD tool continues to drive advancements at the forefront of semiconductor research and development. This tool is also used extensively in our research as will be clarified in the upcoming chapters.

1.8 Outline of the Thesis

This section describes the outline of the thesis in detail. The present Thesis work is an illustration of the research carried out for designing and optimizing a modified Tunnel Field Effect Transistor for use in low power VLSI circuits. The thesis is divided into seven chapters. The chapter-1 is the Introduction, which firstly introduces VLSI technology as an engineering stream and its advent and evolution since the discovery of transistor in 1947. It also explains the motivation behind opting for TFET as our device for research. Then it demonstrates the different performance parameters of TFET on the basis of which the optimization of our proposed research is done. Finally, It introduces the two most important EDA tools Cogenda Visual TCAD and Silvaco ATLAS used extensively in the research. Next chapter-2 is Literature Survey, which illustrates most of the contemporary TFET architectures introduced by researchers till date, their detailed structures, dimensions etc. It also compares the structures for the merits and shortcomings through a tabular representation. The chapter-3 is illustration of our first major breakthrough, the design and optimization of a device called n channel JL DG TFET with p+ type SiGe pocket near the source region of channel. It demonstrates how the device is having much superior performance compared to the existing devices of similar dimensions. Next chapter-4 is on the design of an inverter circuit using both n-JL DG TFET and p-JL DG TFET. It explains the implementation of p JL DG TFET along with the fabrication steps. Finally, it compares and plots the performance of the implemented inverter which proves to be a worthy replacement for CMOS inverters for very low power circuits. Next chapter-5 illustrates our new novel design, Asymmetric double gate P-I-N Tunnel FET. It describes the dimensions and structure of Asymmetric double gate P-I-N TFET. Then it summarises the device characteristics and interprets the findings. Chapter-6 focuses on the application perspectives of the proposed JL DG TFET and illustrates the implementation of two major digital circuits using the JL DG TFET, viz. the transmission gate and the 2:1 Multiplexer (MUX). Finally, Chapter-7 concludes our research with the summary of major findings and future scopes of further research.

CHAPTER 2
LITERATURE REVIEW

Although TFET devices have a lot of merits to be utilised as worthy replacement of MOSFETs from low power VLSI circuits, they have a few disadvantages as well, the two main ones are very modest ON state current value and ambipolar conduction, or conduction in the reverse direction when switched OFF. To lessen these shortcomings, researchers have suggested a number of altered topologies for the traditional TFET devices. In this section we will illustrate a few of the major strategies found in the literature for generation of highly efficient TFET circuits and devices.

2.1 Gate-Drain Overlap Hetero-Dielectric Gate-All-Around TFET (GDO HD GAA TFET)

When building and modifying the fundamental Tunnel FET structure, researchers concentrated on different structural and geometrical adjustments as well as the application of more recent and cutting-edge materials. Here, several of these structures are categorised and their dimensional characteristics are briefly explained. A small number of them concentrated on using low band gap material as the source and a heterogenous dielectric structures for the gate dielectrics that combined low and high k materials. Madan & Chaujar [27] proposed GDO HD GAA TFET, a TFET having gate to drain overlapping, gate dielectric of heterogenous materials, and gate wrapped all-round the channel structure (Fig. 2.1). While the hetero material used for the gate dielectric improves the I_{ON}, the gate-drain overlap inhibits the ambipolar nature of current. Additionally, the gate's surrounding structure enhances its ability to control the tunnel current. Dimensions of the device being given as channel length, L_g=50nm, R=10nm, T_{ox}=2nm, Gate metal Φ=4.3eV, ε_2=21(HfO_2, High k), ε_1=3.9(SiO_2, Lower-k), high-k dielectric length $L_{high\text{-}k}$=10nm & Source of type p+, Channel of type p-, Drain of type n+ doping of 1x $10^{20}cm^{-3}$, 1x $10^{16}cm^{-3}$, 1x $10^{18}cm^{-3}$ respectively.

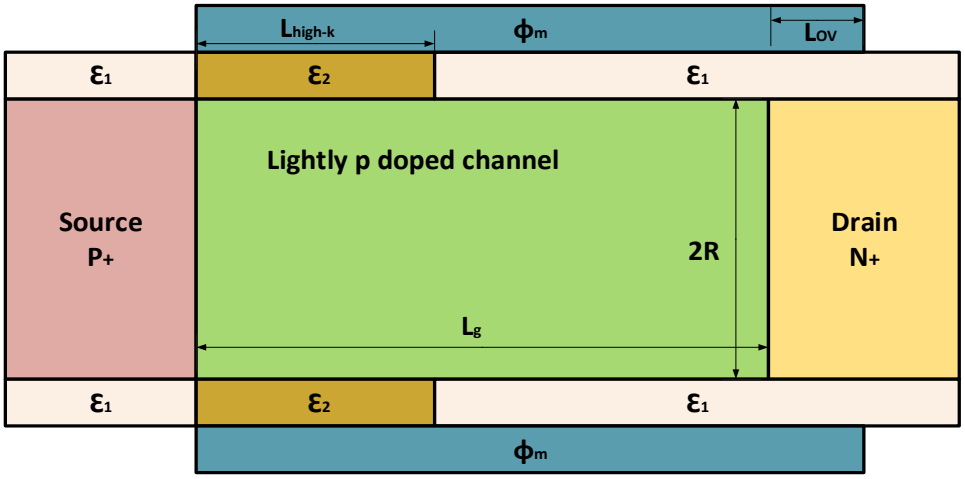


Fig.2.1 Cross-section of GDO HD GAA TFET

2.2 Low Doping Heterogenous Gate Dielectric TFET (LD-HTFET)

Wang et al. [22] paper proposed the LD-HTFET (Fig. 2.2), a Carbon Nano Tube-based TFET with heterogeneous gate dielectric and low doping. The authors also compared the LD-HTFET's performance to that of the HK-TFET, a CNT or Carbon Nano Tube based TFET having high k material for the dielectric at gate, & the HTFET, which is the only TFET with heterogeneous gate dielectric. When light doping and gate dielectric modulation are present, the device-level study of switching behaviours and HF figure of performance is conducted using the quantum kinetic model. It is discovered that the LD-HTFET has superior HF and switching figures. HSPICE circuit simulations revealed significant gains in the power delay product, delay energy, and static noise margin. The LD-HTFET has the following device dimensions: a 20 nm gate length, a 2 nm gate oxide thickness, a 20 nm source/drain expansion length, and a gate oxide with ε values of 16 and 3.9 for high and low k, respectively.

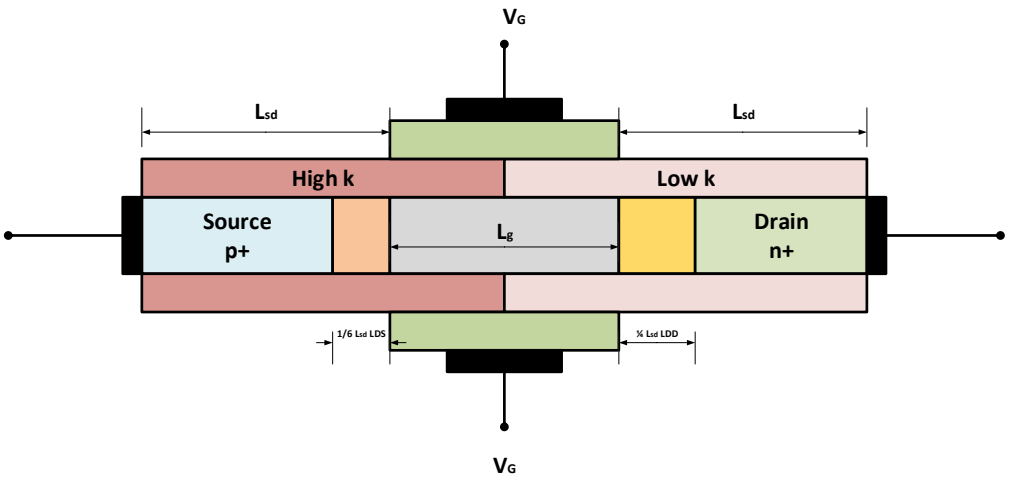


Fig.2.2 Cross-section of LD HTFET

2.3 Hetero Gate Dielectric, Nano Wire TFET with SiGe Source (SiGe S NW TFET)

In order to build analog circuits such as operational amplifiers, Patel et al.[34] presented the SiGe S NW TFET (Fig.2.3) with a hetero gate dielectric & source built of lower bandgap SiGe material. They also assessed the SiGe S NW TFET's performance in comparison to the conventional Si nanowire TFET. The constructed source's narrow bandgap SiGe and the usage of HfO_2 (with a higher value for k) as the gate-oxide near source to channel junction resulted in a SS of 6.54 mV/dec, which is much low compared to that of the traditional device's 36.24 mV/dec. An increase in transconductance brought about by an improvement in ON current(640 times than conventional TFET) led to improved RF/analog performance. While the device's diameter changes, the channel length varies very little and has little effect on SS. The device measures 20 nm in length, 20 nm in diameter for the nanowire, 2 nm for t_{ox}, 1 x 10^{17} cm^{-3} for substrate doping, 1 x 10^{18} cm^{-3} for drain doping, and 1 x 10^{20} cm^{-3} for source doping.

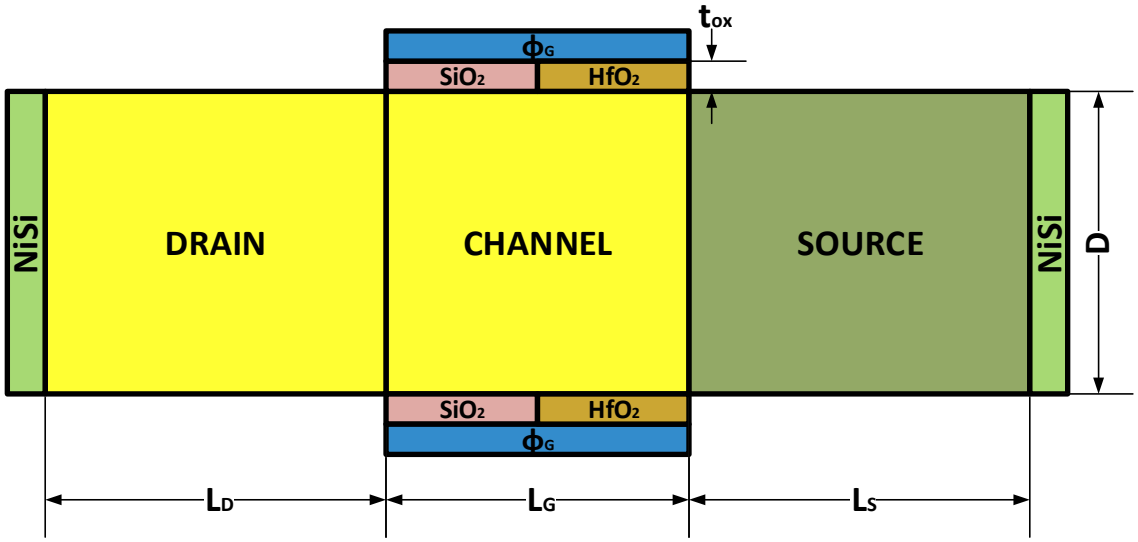


Fig2.3 Cross-section of SiGe S NW TFET

2.4 Heterogenous Gate Dielectric Double-Gate-Metal Work-Function TFET (HGDDW TFET)

Few engineers combined several gate metal combinations with different work functions. For instance, a heterogenous gate-dielectric based double-gate-metal work function transistor (HGDDW TFET) that reduces ambipolar-behaviour & improves RF performance figure was proposed by Raad et al.[36]. Three gate metals with distinct work functions, $\Phi_1=\Phi_3=4.0eV$ and $\Phi_2=4.6eV$ are present in its structure (Fig. 2.4). On the drain side, low Φ increases ON current and decreases ambipolarity. High k(HfO_2) towards the source end aids in improving drive/ON current by decreasing the width of tunnelling at source-channel interface, lower k SiO_2 is

employed at the drain end to decrease the ambipolar leakage & improve RF figure of performance. L_D=L_S=100nm, L_G=50nm are the device dimensions that is used. It comprises a high-density layer with t_h=2nm, t_{ox}=2nm, t_{Si}=10nm, lengths of Φ_1 and Φ_3=10nm, and drain/source doping of $1x10^{20}cm^{-3}$.

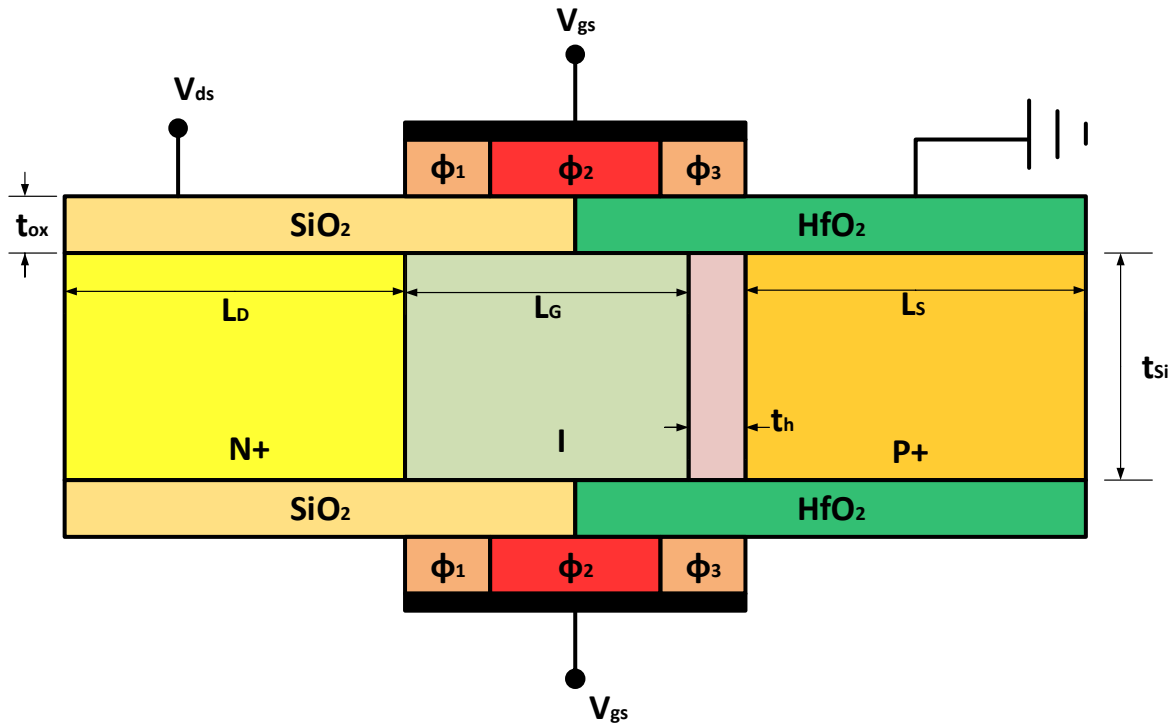


Fig.2.4 Cross section of HGD DW TFET

2.5 Triple-Metal Gate-All-Around TFET (TMGAA TFET)

A Si nano wire-based Triple-Metal-Gate-All-Around TFET (TM GAA TFET) was proposed by Bagga & Dasgupta [37] (Fig. 2.5). The gate, which is wrapped around the structure and made of three different metals, bends the energy band close to the source to boost driving current and helps to form a barrier to prevent backward tunnelling current from draining. Kane's model and Poisson's equation dependent analytical approach are used to verify the device. Poisson's Equation in cylindrical coordinates can be expressed as follows:

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial\varphi(r,z)}{\partial r}\right)+\frac{\partial^2\varphi(r,z)}{\partial z^2}=\frac{-qN_C}{\varepsilon_{Si}} \quad \text{for } (0\le z\le L,\ 0\le r\le R) \tag{2.1}$$

The device's dimensions are as follows: the channel's length, L=L1+L2+L3=60 nm; the metal M1 and M2 lengths, L1=10nm and L2=30 nm, M3 length L3 is 20; the work-functions, Φ_{M1}=4.4 eV, Φ_{M2}=4.8 eV, Φ_{M3}=4.6 eV; the gate-oxide thickness, t_{ox} is 2 , & the Silicon nano-wire radius, R is 10 nm.

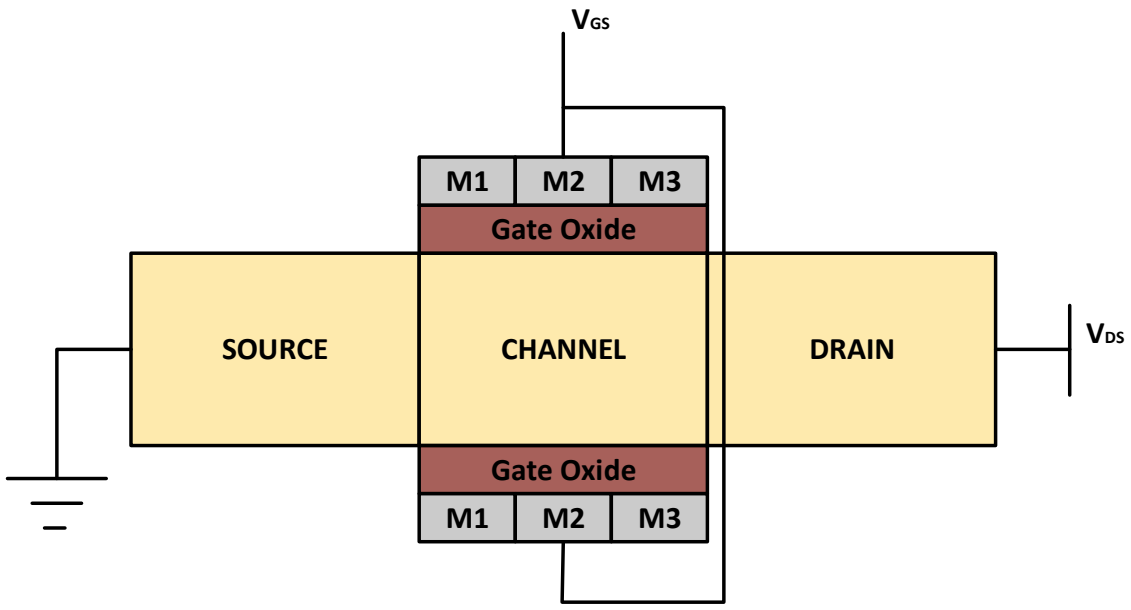


Fig.2.5 Cross-section of Si nanowire TM GAA TFET

2.6 U-Gate Hetero-Junction Vertical Tunnelling FET (U HJ VTFET)

Much effort is put into changing the channel's geometry to make it stand vertically so that point and line tunnelling can be used. A U shaped Gate Hetero-Junction (InGaAs-GaAsSb) Vertical Tunnel FET (UHJ V-TFET) was proposed by Shih et al.[38] (Fig. 2.6). The ON current is improved by the device's band to band tunnelling normal to the surface of the gate. By inserting a spacer material layer at the channel-drain interface, this device allows for the independent & separate regulation of ON & OFF currents. The (InGaAs/GaAsSb) hetero-junction has a narrow band-gap of 0.02 eV. In terms of performance, the structure can attain a driving current of 520 μA/μm and an I_{ON}/I_{OFF} ratio of 10^7. The structure's measurements are L_g = 100 nm, L_d = 50 nm on either sides of the gate, 2 nm of the gate oxide (HfO_2) thickness, 4.7 eV of the gate metal work function, 3×10^{19} cm^{-3} of the source (GaAsSb)-p+ doping, and 2×10^{18} cm^{-3} of the drain (InGaAs)–n+ doping. The device is compatible with VLSI technology and doesn't require any complicated fabrication methods.

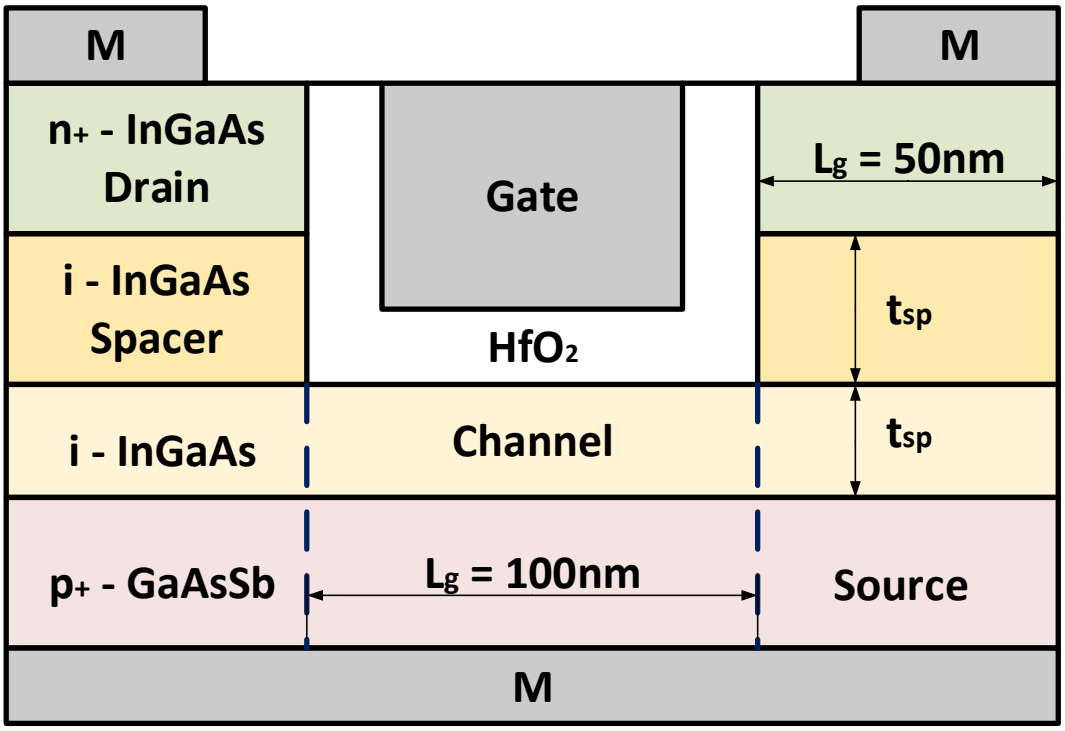


Fig. 2.6 Cross section view of U HJ VTFET

2.7 Double-Gate Vertical-Structure TFET (VS-TFET)

A TFET known as the VS-TFET was proposed by Kim et al.[39]. It has a vertical construction with a source, drain, and channel stack, two gates on each side, and weakly doped Silicon to encircle the stack at both the sides (Fig. 2.7). The device's vertical-channel gives it excellent control over the tunnelling current and BTBT perpendicular to the gate field. The device is treated with NH_3 plasma to improve the quality of the gate dielectric, and it has a progressive doping profile to suppress ambipolar conduction. The device yields a high $I_{ON}/I_{OFF}=10^4$ and a very low SS of 17 mV/dec. Additionally, it is proposed that, the device may be improved for better working by building the tunnelling-junction using materials with low band gaps, such as SiGe or Ge. Source of height 100 nm with p doping of 5 x 10^{19} /cm^3, channel of height 175 nm with p doping of 1 x 10^{17} /cm^3 and drain height of 50 nm with n doping of 1 x 10^{20} cm^{-3} are the dimensions of the device.

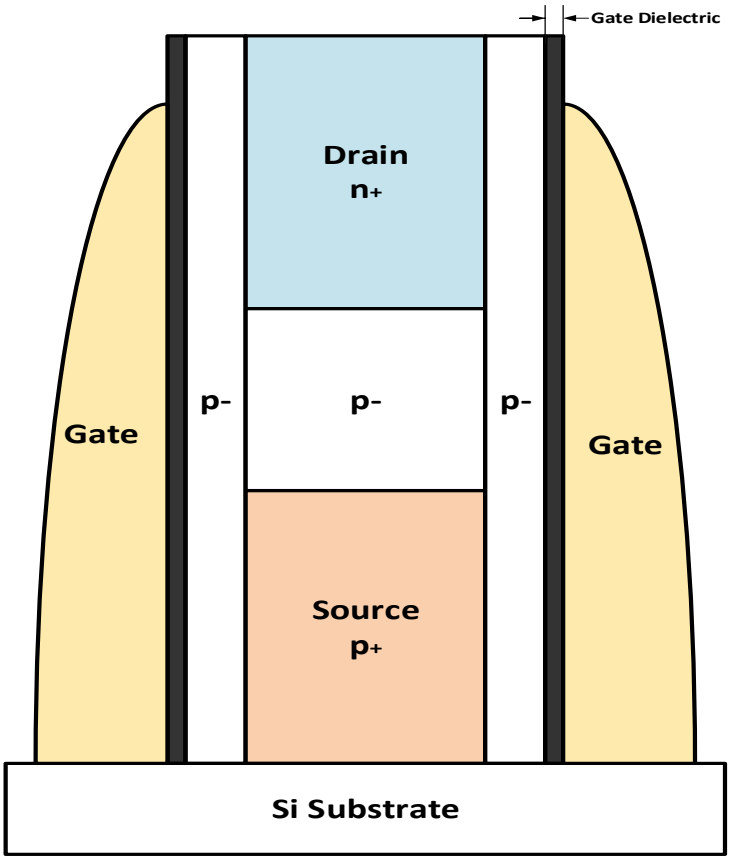


Fig.2.7 Cross-section of Double-Gate Vertical-Structure TFET (VS-TFET)

2.8 T-Channel Drain-Engineered Quad-Gate TFET(DE-QG-TFET)

A drain engineered TFET with 4 gates & a T shaped channel, known as the DE QG TFET, as shown in Fig. 2.8, is proposed by Uddin Shaikh & Loan[40]. The device features a unique design with two lateral sources and a vertically extended drain above the T-shaped channel that is managed by four gates. The distinct design effectively reduces ambipolar leakage in comparison to lateral double gate transistors. The device boasts an I_{ON}/I_{OFF} ratio five orders higher and twice the ON state current of a typical DG-TFET. Additionally, there is a significant improvement in the analog/RF figure of merits. The device dimensions are as follows: t_{Si}=10nm, gate oxide SiO_2 thickness of 3nm, gate metal work function = 4.5eV, p type source doping = $1x10^{20}$ cm^{-1}, n type channel doping = $1x10^{17}$ cm^{-1}, and n type drain doping = $5x10^{18}$ cm^{-1}.

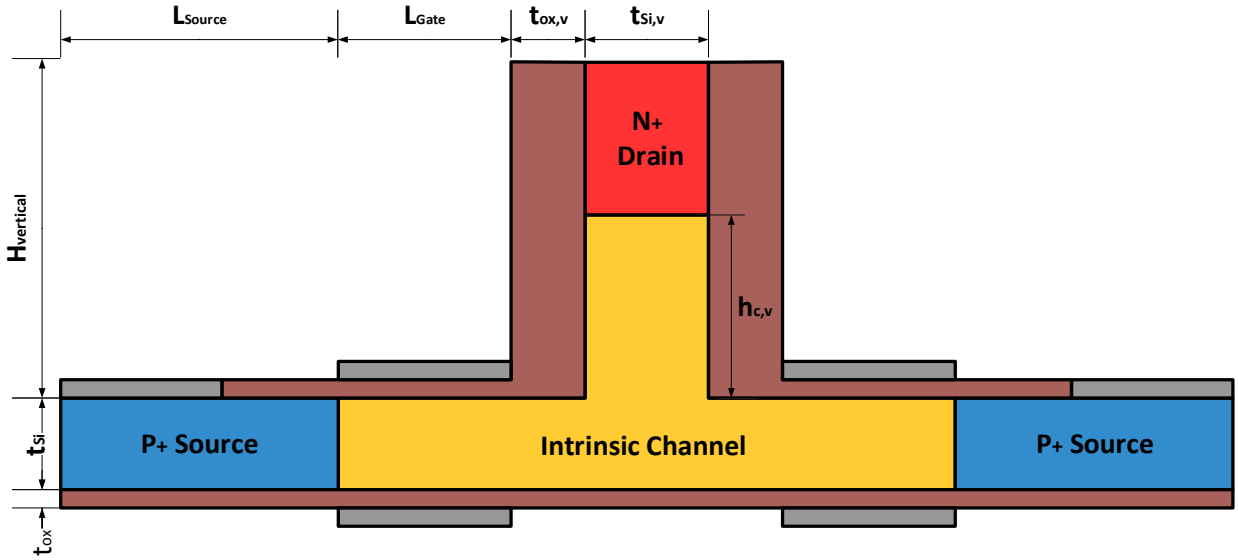


Fig. 2.8 Cross- Section of T-Channel DE-QG-TFET

2.9 Core and Shell Gate Si nanotube TFET

A silicon nanotube-based transistor field-effect transistor (TFET) with two gates—one encircling the channel as a shell and the other as a core—is suggested by Kumar et al. [41] (Fig. 2.9). Much more control on the channel & increased drive capability are provided by the device that combines an outer shell-based wrapped all-around gate with an inner core gate. For analog and RF performance, when compared, with traditional nanowire based TFET, it is found to be significantly better. It has a vertical device structure which greatly aids in increasing the ON current. The channel thickness is 50 nm, the t_{ox} is 1 nm, the radius is 5 nm, the source doping is 1 x 10^{20} cm^{-3}, the drain doping is 5 x 10^{18} cm^{-3}, the channel doping is 1 x 10^{17} cm^{-3}, and the gate work function is 4.4 eV.

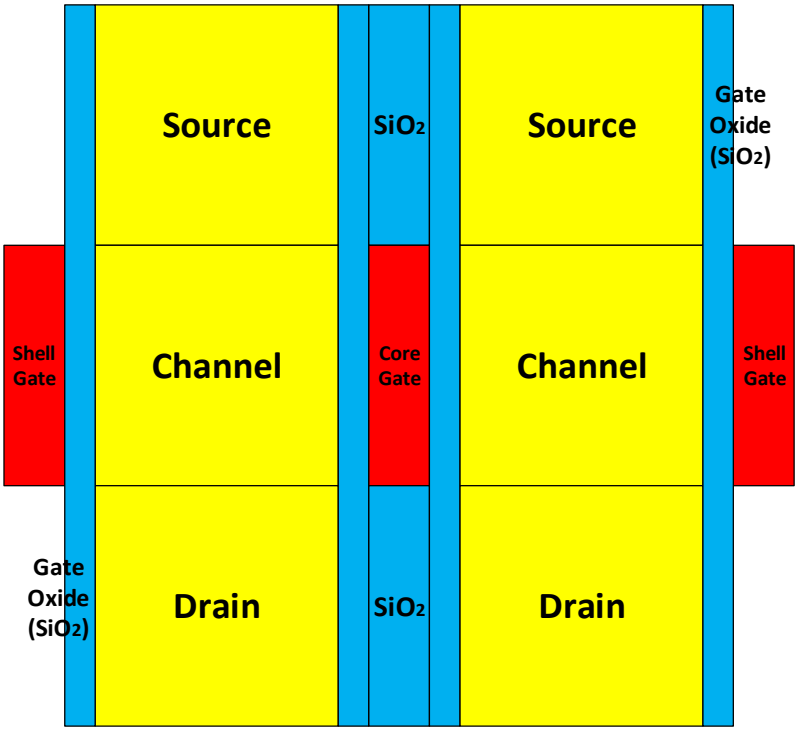


Fig. 2.9 Cross- Section of the Core & Shell-Gate in Si based nanotube-TFET

2.10 Dual-Metal Control-Gate Charge-Plasma TFET (DMCG CP TFET)

Research is conducted to incorporate charge-plasma dependent junction-less technology in order to decrease fabrication complexity & expense, as well as reduce various leakages. A TFET utilising charge plasma technology with a dual metal control gate, known as the DMCG-CPTFET (Fig. 2.10), was created by Nigam et al.[42]. In order to simplify fabrication, the device is made junction less & relies on electrical doping dependent on charge plasma. Platinum (Φ = 5.93 eV) is deposited over Si to generate the p+ source, while Hafnium (Φ = 3.9 eV) is deposited to form the n+ drain. Three metals, each with a distinct work function, are used to construct the gate. Metal $M_1(\Phi_1)$ is referred to as the tunnelling gate on the source side, $M_3(\Phi_3)$ as the auxiliary gate on the drain side, and $M_2(\Phi_2)$ as the control gate at the centre. Taking $\varphi 1 = \varphi 3 < \varphi 2$ yields the best results. While the auxiliary gate inhibits ambipolarity, the tunnelling gate enhances ON state performance. The dimensions of the device are as follows: tunnelling gate length L_1 = 10 nm, control gate length L_2 = 25 nm, auxiliary gate length L_3 = 15 nm, silicon layer thickness t_{Si} = 10 nm, oxide layer thickness t_{ox} = 1 nm, and gate length L_g = 50 nm.

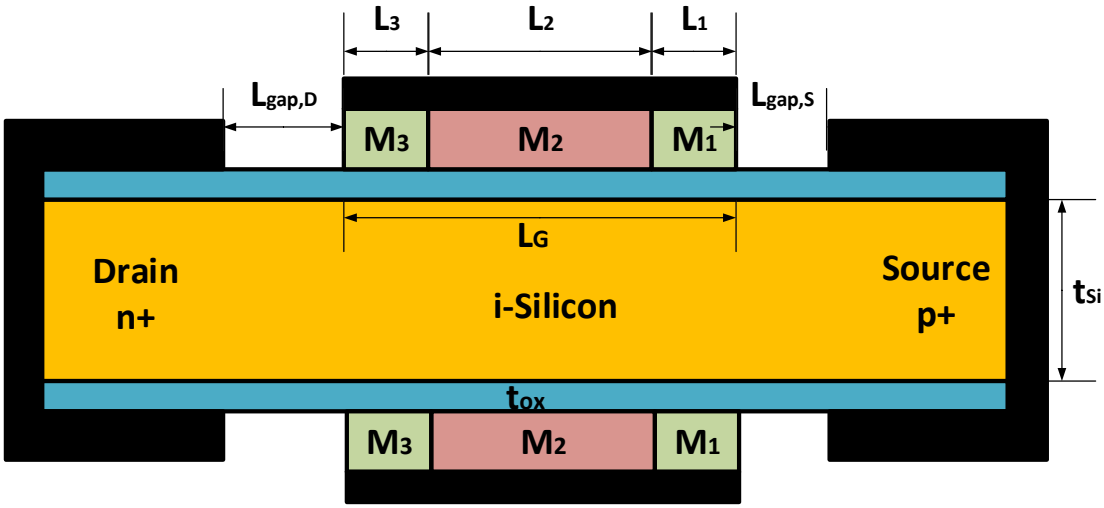


Fig. 2.10 Cross-section of DMCG CP TFET

2.11 Hetero-Gate-Dielectric Drain-Engineered Dual-Metal-Gate Doping-Less TFET (HGD DE DMG DL TFET)

HGD DE DMG DL TFET (Fig. 2.11) is a doping less Tunnel FET with hetero-geneous gate dielectric & work-function engineered at both the gate & drain that was proposed by D. S. Yadav et al.[35]. Because of the charge plasma technology's great simplicity of manufacture, the device requires less doping. Here, the dual work function is employed twice: once at the gate terminal to increase the ON-state current, and once at the drain to decrease ambipolarity. Once more, there is a hetero gate dielectric, which when paired with work function modulation at the drain and gate, reduces the subthreshold slope, raises the threshold-voltage, & enhances the high frequency responses. The measurements of the device are as follows: length of the metal at drain (L_D) is 40 nm having Φ of 3.9 eV; the length of the drain metal extension (L_B) is 10 nm having Φ of 4.3 eV; the length of the metal at the gate (L_G) is 40 nm having Φ of 4.6 eV; the extended portion of the gate metal length (L_C) is 10 nm having Φ of 4.0 eV; the length of source-metal (L_S) is 50 nm having Φ of 5.93 eV, the thick-ness of the silicon based body (t_{Si}) is 10 nm & the thick-ness of the layer of oxide (t_{ox}) is 1 nm.

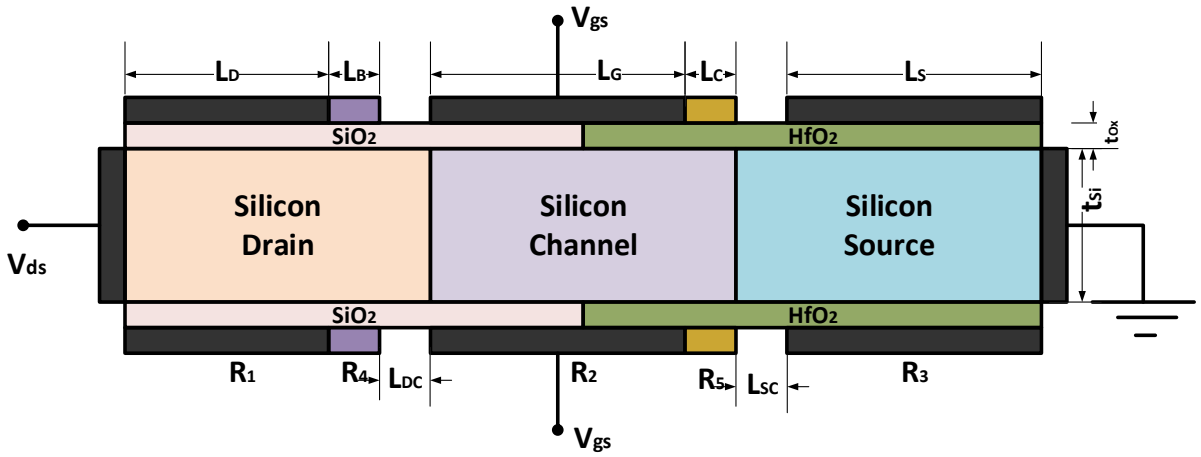


Fig. 2.11 Cross Section of HGD DE DMG DL TFET

2.12 Hetero-Material Gate-Underlap Electrically Doped TFET (HM GUL ED TFET)

A Tunnel FET with electrical-doping, underlapping of gate, & a hetero-geneous body having low band-gap SiGe material at the source end and Silicon at the drain & channel was proposed by S. Yadav et al. [43]. Figure 2.12 depicts the HM-GUL-ED-TFET device. Ambipolarity and gate leakage current (I_g) are suppressed in part by the gate under-lap. The small bandgap of the $Si_{0.5}Ge$ material at the source contributes to an improvement in the RF & DC figures of performence. Additionally, the system employs electrical doping dependent on charge plasma, that greatly simplifies manufacture. The dimensions of the device consist of an electrical drain/source length of L_{ED}=L_{ES}=50nm with a work function of 4.5eV, substrate doping of $1x10^{15}$ cm^{-3}, control gate length L_{CG}=30nm, gate underlap L_{GUL}=20nm, and t_{Si}=10nm, t_{ox}=1.5nm.

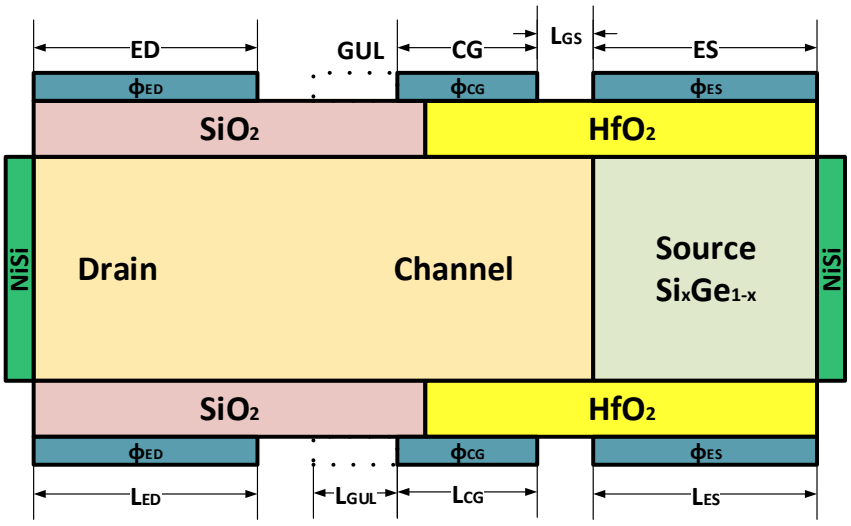


Fig2.12 Cross section of HM GUL ED TFET

2.13 Junction-Less TFET(JL-TFET) with SiGe n+ pocket

The JL-TFET (Fig.2.13), a junction-less Tunnel FET with SiGe based n+ pocket doping region near the source, is proposed by Devi & Bhowmick [44] and can be used to build effective inverter circuits. Two metal gates, one fixed and the other control, with distinct purposes, are part of the apparatus. It employs junction-less technology, which uses appropriate voltage fluctuations at the two gates to transform the N+-N+-N+ structure into a PIN. By utilising a SiGe N+ pocket close to the source end, the ON state current is significantly increased to around 5.7×10^{-4} A. This creates a conduit for tunnelling-current, which is transverse to gate-oxide along with the typical lateral way. It is possible to get close to about 43.6 mV/dec of subthreshold-swing value by adjusting the fixed-gate & control-gate work-functions values at 5 & 4.5eV, respectively. Additionally, RF study demonstrates better performance when compared to traditional JL-TFET. The device's dimensions are $1x10^{17}$ cm^{-3} for source, channel, and drain doping, 2 nm for gate oxide thickness, 35 nm for channel length, 30 nm for Si thickness, 20 nm for pocket length, and 10 nm for thickness.

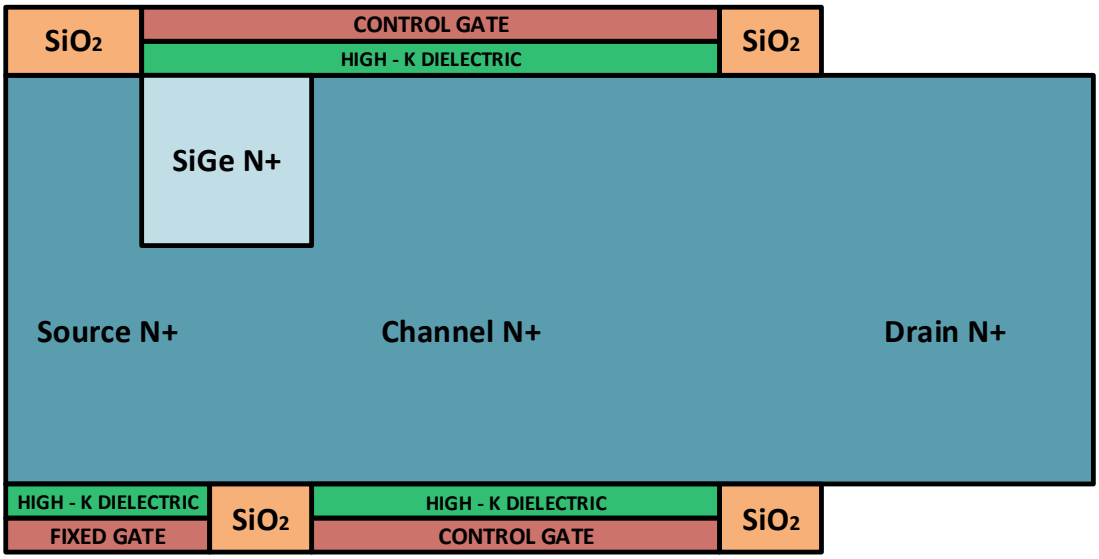


Fig.2.13 Cross-section of JL-TFET with SiGe n+ pocket

2.14 SiGe source pocket Junction-Less Single Gate TFET (JL SG TFET)

JL SG TFET (Fig. 2.14), a junction less Tunnel FET with a single-gate & an SiGe based pocket towards the source, was proposed by Tripathi et al.[45]. For ease of fabrication, junction-less technology is used in the device. The device's switching capacitance is decreased by the small band-gap SiGe pocket between the source & the channel. Utilising Ge mole fraction x=0.3

enhances a number of electrical characteristics, including junction capacitance, leakage-current, and transconductance. At 300 K, the proposed device achieves a steeper SS or subthreshold slope of 52.3 $mVdec^{-1}$, an I_{ON}/I_{OFF} ratio of $2x10^8$, and a DIBL of 2.1 mV/V. Additionally, the device properties are examined over a broad temperature range of 250 to 400 K, and it is discovered that the fluctuations are quite small, making it perfect for digital applications requiring sub-20nm ultra-low power. The dimensions of the device are as follows: source/drain doping of $1x10^{20}$ cm^{-3}, drain/source height of 20 nm, channel length of 15 nm, gate length L_g=15 nanometres, and SiGe pocket of length 5 nm.

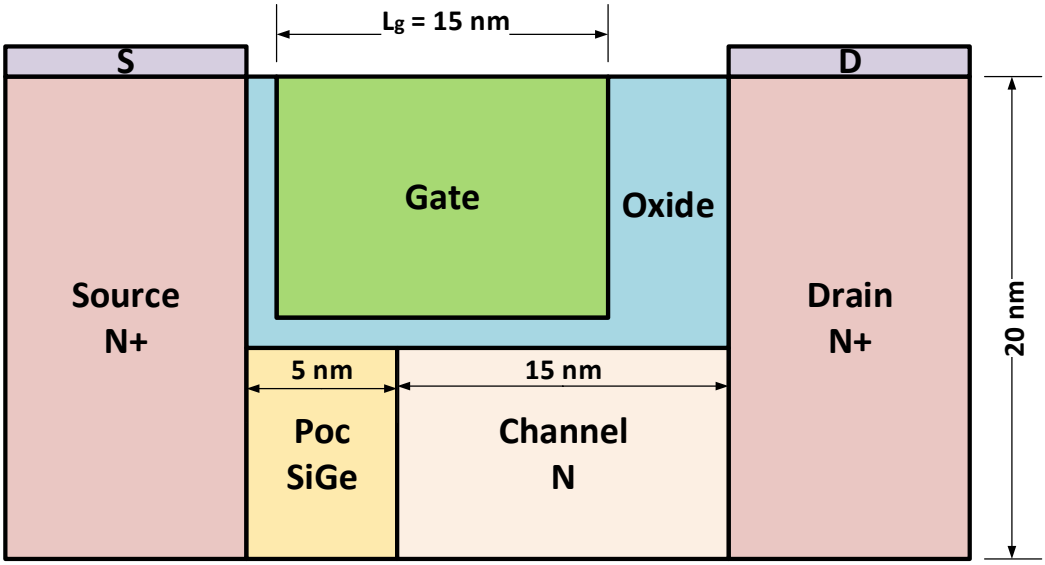


Fig. 2.14 Cross sectional of SiGe source pocket JL SG TFET

2.15 Doping Less Si Nanowire Vertical TFET

Using cylindrical Si nanowire, Kumar & Raman[46]presented a charge plasma-based TFET. To induce the vertical PIN structure, it utilises source, drain & gate terminals with distinct work-functions wrapped-all-around the nanowire of intrinsic Si. Fig. 2.15 displays the proposed structure in two dimensions. The effects of ITC or interface trap charges at the dielectric-channel interface are examined in this device, and the noise behaviour that results is also examined. It is discovered that while positive ITCs enhance drive current and noise behaviour, ITCs of all polarities deteriorate the I_{ON}/I_{OFF} ratio. The device measures 100 nm for the drain/source length, 50 nm for the channel-length, 5 nm for the radius of the NW, 2 nm for the T_{OX}, and 4.5, 5.93, and 3.9 eV for the gate, source, and drain work functions, respectively.

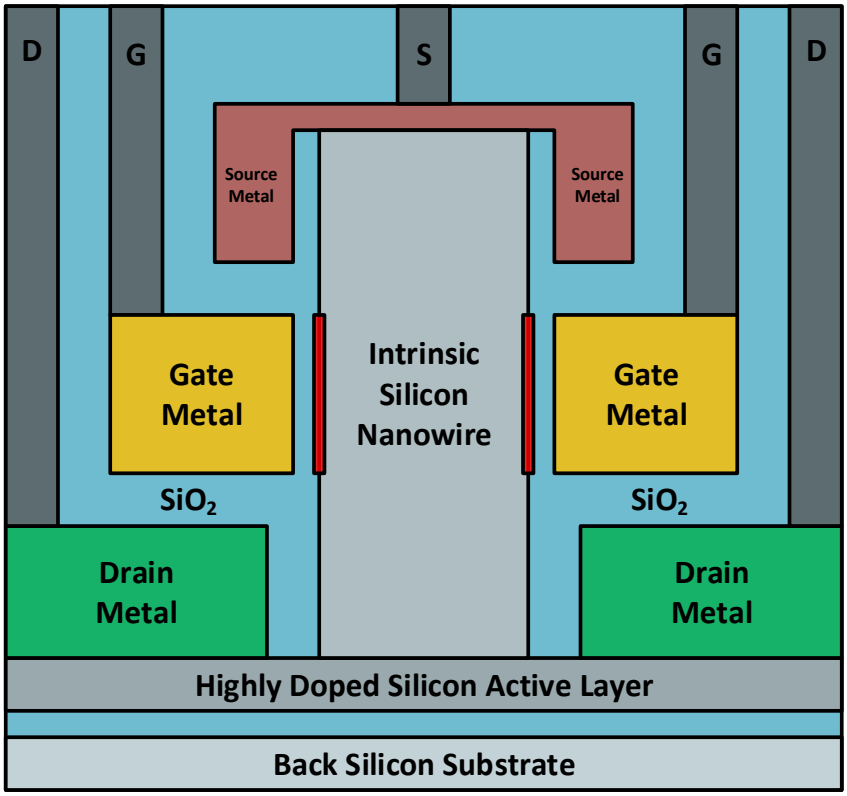


Fig. 2.15 Cross-section of doping less vertical TFET

2.16 Split-Drain Single-Gate TFET (SD SG TFET)

A few studies have used the technologies of BOX or buried oxide and SELBOX or selective buried oxide to improve the performance of TFETs. As seen in Fig. 2.16, Bhattacharjee et al.[47] suggested the SD-SG TFET, a novel TFET with a single gate and a split or fractured drain. Drain doping engineering is utilised in the device to produce a split or separated drain, with one part heavily doped and the other lightly doped. The doping is arranged in descending order. Ambipolar conduction is significantly reduced by the divided drain arrangement. The performance of four devices with varying split drain (SD) relative location is evaluated and assessed. While the other devices have either splitted Drain or SD at top termed TSD-SG, Splitted Drain or SD at the bottom of the device called BSD-SG, or Splitted Drain/SD in the centre called MSD-SG Tunnel FET, the first has the full drain split into low & high doping. Out of all the structures, the BSD-SG TFET has the highest I_{ON}/I_{OFF} ratio. When compared to traditional TFETs, all of the structures performed better. Drain doping $N_{D1}=5x10^{18}cm^{-3}$ and $N_{D2}=1x10^{17}cm^{-3}$, source doping $N_S=1x10^{20}cm^{-3}$, channel doping $N_{ch}=1x10^{17}cm^{-3}$, drain length $X_d=100nm$, source width $Y_s=60nm$, channel width $W=60nm$, $T_{si}=60nm$, and $T_{ox}=1nm$ are among the dimensions.

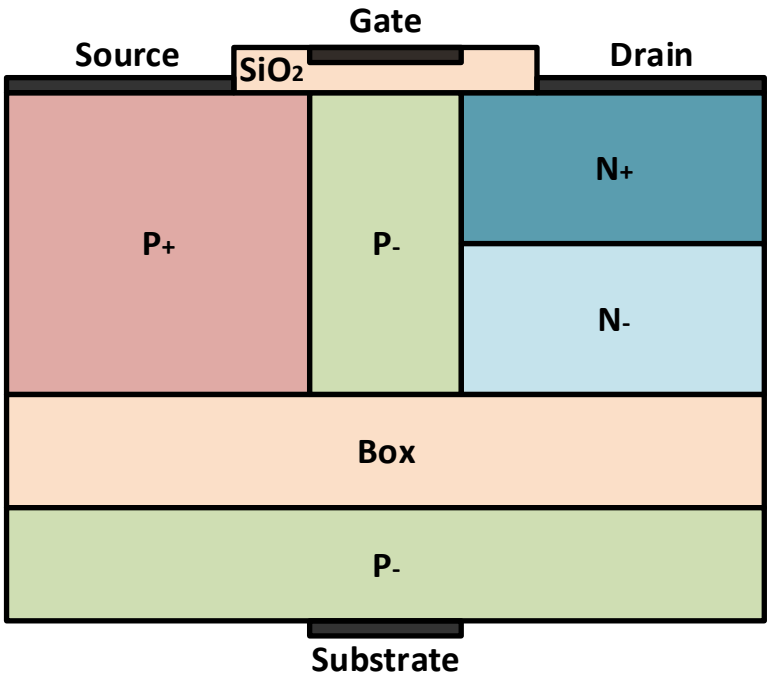


Fig. 2.16 Cross-Section of SD-SG TFET

2.17 Gate-on-Source Channel TFET (GOSC TFET) with BOX Layer

In order to compare the performance of the buried oxide (BOX) based TFET with traditional FG-SOI Tunnel FET & GOS-SOI Tunnel FET when there are traps present at all the Silicon to Oxide interfaces, Mitra & Bhowmick[33]constructed the GOSC TFET (Fig. 2.17) with a gate over some regions of both the channel and the source. For each of the three devices, the influences of the trap charges at interface between gates oxide & Silicon & BOX and Silicon are assessed with regard to subthreshold swing, drive current, ambipolarity, C_g, and f_T. The effect of the former is found to be significantly more severe. Trap charges at the interface of Silicon to gate oxide diminish ON current, whereas traps at the interface of BOX to Si increase ambipolar conduction. It is discovered that the most resistant to the negative consequences of interface traps is GOS SOI TFET. The GOS TFET exhibits significantly improved performance, with Subthreshold Slope (SS) of 61.5 mVV^{-1}, V_T of 0.6V, & I_{ON} of 37.5 µA/µm. Drain/source length = 30 nm, source p+ (10^{21} cm^{-3}), p channel (10^{16} cm^{-3}), drain n+ (5×10^{19} cm^{-3}), Gate work function of 4.2 eV, T_{ox} = 2 nm, Gate to channel overlap L of 10 nm, & L_{UN} = 30 nm are the dimensions of the device.

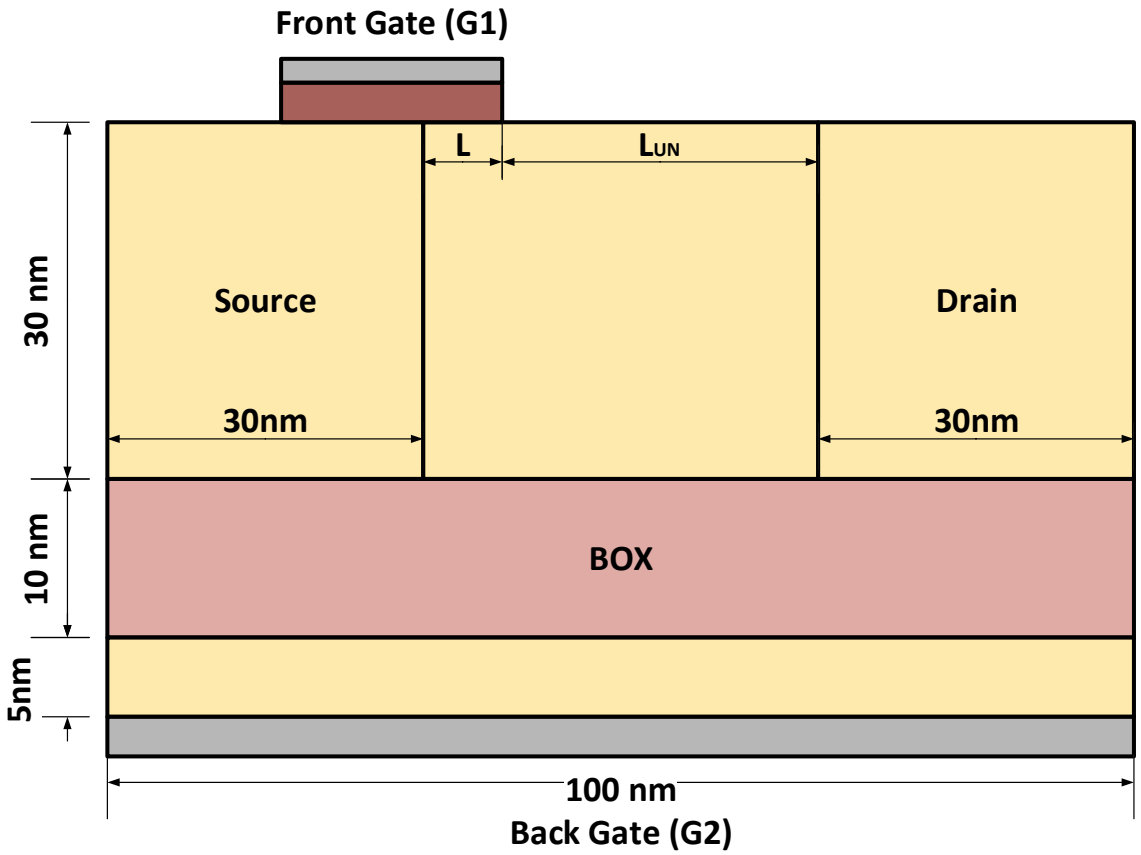


Fig. 2.17 GOSC TFET with BOX layer

2.18 L shaped BOX Ge Source Vertical TFET

A Tunnel FET having an L shaped BOX or buried oxide layer and a highly thin δ doped layer inside the Ge source region was proposed by Vanlalawpuia & Bhowmick [48] (Fig. 2.18). The drive current is increased when low bandgap Ge material is used as the source, while ambipolarity and OFF state leakage are decreased when δ-doped layer is used. Additionally, because the source is placed vertically at the bottom of the gate channel stack, tunnelling current in the vertical direction—also known as Band-to-Band-Tunnelling or BTBT—is produced that is at right angles to the gate-oxide and produces a large ON state current. Each region's sizes & dimensions are decided following optimisation with software simulation. In terms of measurements, the δ layer is 1 nm thick, the L_{UC} is 15 nm thick, the Ge source is 16 nm thick, the t_{OX} is 2 nm thick, the source is 15 nm long, the drain is 10 nm long, and the gate is 30 nm long. 1×10^{20} cm^{-3}, 1×10^{16} cm^{-3}, 5×10^{18} cm^{-3}, and 5×10^{16} cm^{-3} correspond to the source, the channel, the drain, & the δ layer doping, respectively.

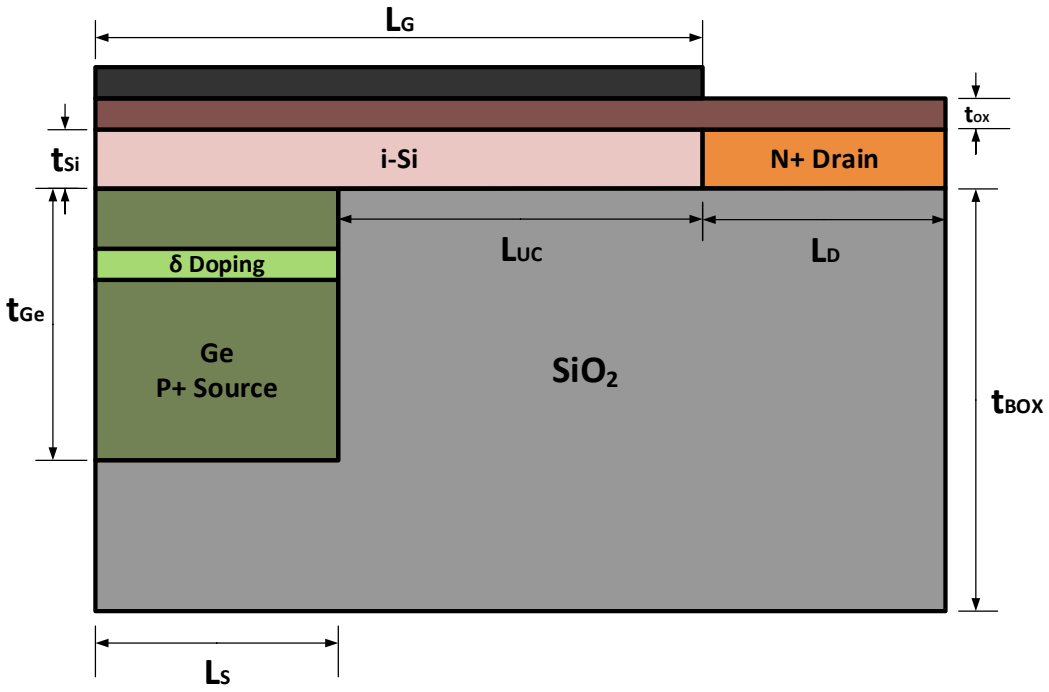


Fig. 2.18 Cross section of L shaped BOX Ge Source Vertical TFET

2.19 W/ZrO_2/Al_2O_3 gate stack Zn diffused source InGaAs planer TFET

An InGaAs based planar TFET device with a W/ZrO_2/Al_2O_3 gate stack and a diffused Zn source was proposed by Ahn et al. [23] (Fig 2.19). In order to increase BTBT and therefore the ON current, the channel is made of direct & narrow bandgap, group III–V InGaAs components. In order to create a quantum-well or QW that suppresses OFF current and simultaneously maintains high I_{ON}, the mole-fraction value for Indium is optimised. To generate an abrupt doping profile for high BTBT, Zn is dispersed in the source region. In order to maintain low equivalent oxide thickness (EOT) and maximise gate control over the tunnelling current, the ZrO_2/Al_2O_3 gate stack is utilised. The device's dimensions are designed to maximise performance in digital circuits with low power consumption.

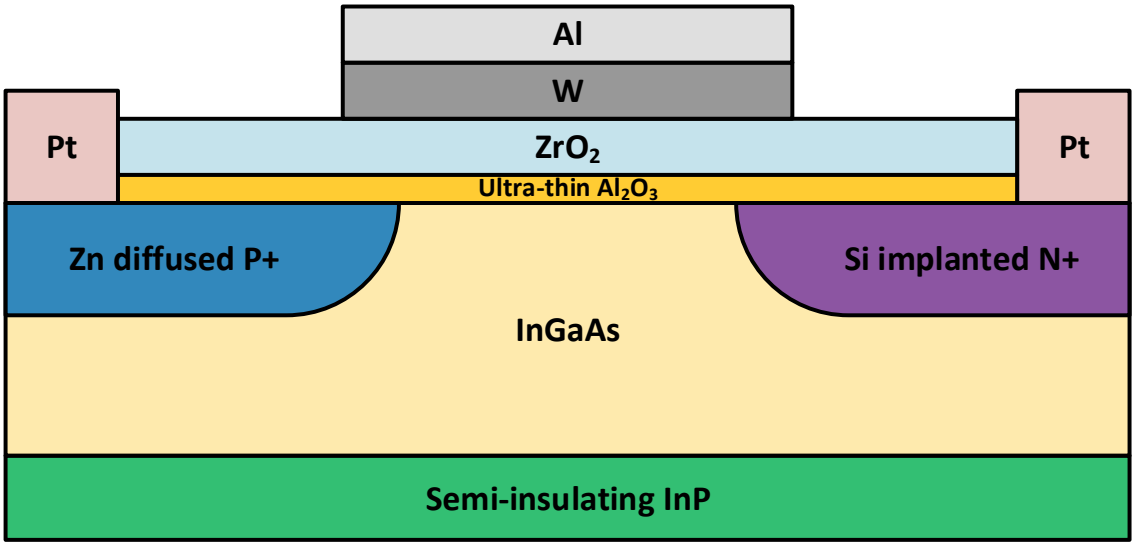


Fig. 2.19 Cross- section of W/ZrO_2/Al_2O_3 gate stack Zn diffused source InGaAs planer TFET

2.20 p+ SiGe layer SELBOX TFET

According to Ghosh and Bhowmick's[49] proposal, a TFET device with a heterogeneous junction and a thin layer of δp+ SiGe near the source-channel interface would be installed atop a selective buried oxide (SELBOX) (Fig. 2.20). As a result of both uniform and gaussian trap distributions, which are a major source of concern for almost all TFET devices, the structure is studied with optimistic results regarding the effect of flicker-noise. Because of its ability to lower OFF current, the structure substitutes SELBOX or selective BOX with a gap for FD or fully depleted BOX. BTBT is improved by using a narrow bandgap δ layer of SiGe, and I_{ON} is improved by using a high k gate dielectric. Through simulations, the mole-fraction of the δ layer, its position, and the position of the selective buried oxide or SELBOX gap are all optimised. The measurements of the device consist of a 30 nm channel length, a 3 nm of δ layer thickness, a 35 nm drain/source length, and a 10 nm of SELBOX thickness with a 2 nm of gap length. The doping of $1\times10^{20}cm^{-3}$, $1\times10^{16}cm^{-3}$, $5\times10^{18}cm^{-3}$, and $1\times10^{18}cm^{-3}$ for the source, channel, drain, and δp+ layer, respectively.

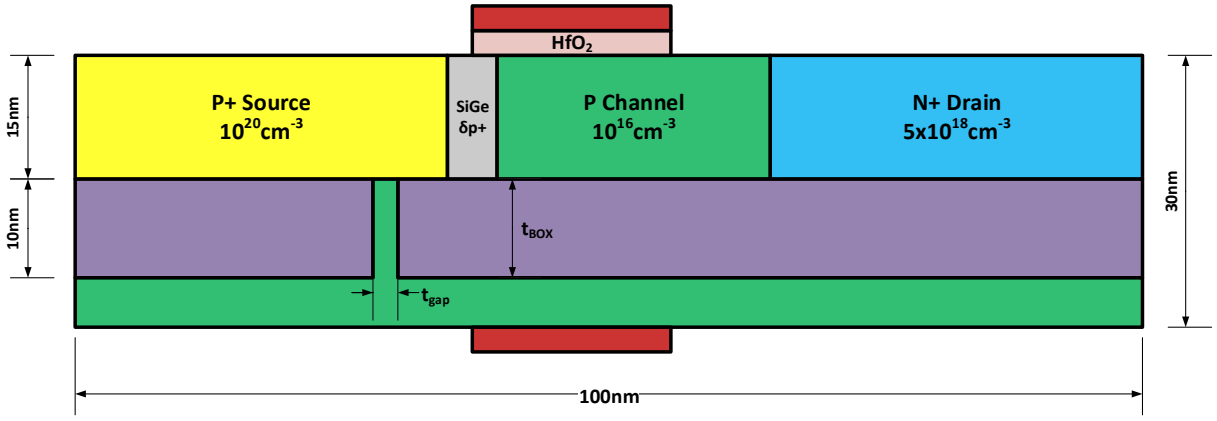


Fig. 2.20 Cross Section of p+ SiGe layer SELBOX TFET

2.21 Partial-Ground-Plane (PGP) Based TFET on SELBOX (GSHJ-PGP-STFET)

The GSHJ-PGP-STFET, as proposed by Singh et al. [50], is a Tunnel FET on Selective BOX layer with a partial-ground-plane or PGP that uses low bandgap Ge as the source material and a gate dielectric stack of HfO_2 over SiO_2. To improve BTB tunnelling, the apparatus uses narrow bandgap Ge material as the source. When paired with a Ge source, the HfO_2/SiO_2 stack optimises gate control of the tunnelling phenomenon and increases ON-state current. A favourable I_{ON}/I_{OFF} ratio is maintained, and OFF state leakage is suppressed by the SELBOX structure with PGP. The device's average SS, I_{ON}, and I_{ON}/I_{OFF} ratio are found to be significantly higher than those of the traditional SELBOX TFET and FD BOX TFET. The device's measurements are as follows: the channel is 40 nm long, the source and drain are 30 nm long, the SELBOX is 10 nm thick with a 4 nm gap width, and the low & high k gate-oxide thicknesses are 1 & 2 nanometres, respectively. Source, channel, drain, and PGP area doping concentrations are 10^{20}, 10^{16}, 5×10^{18}, and 5×10^{18} cm^{-3}, in that order.

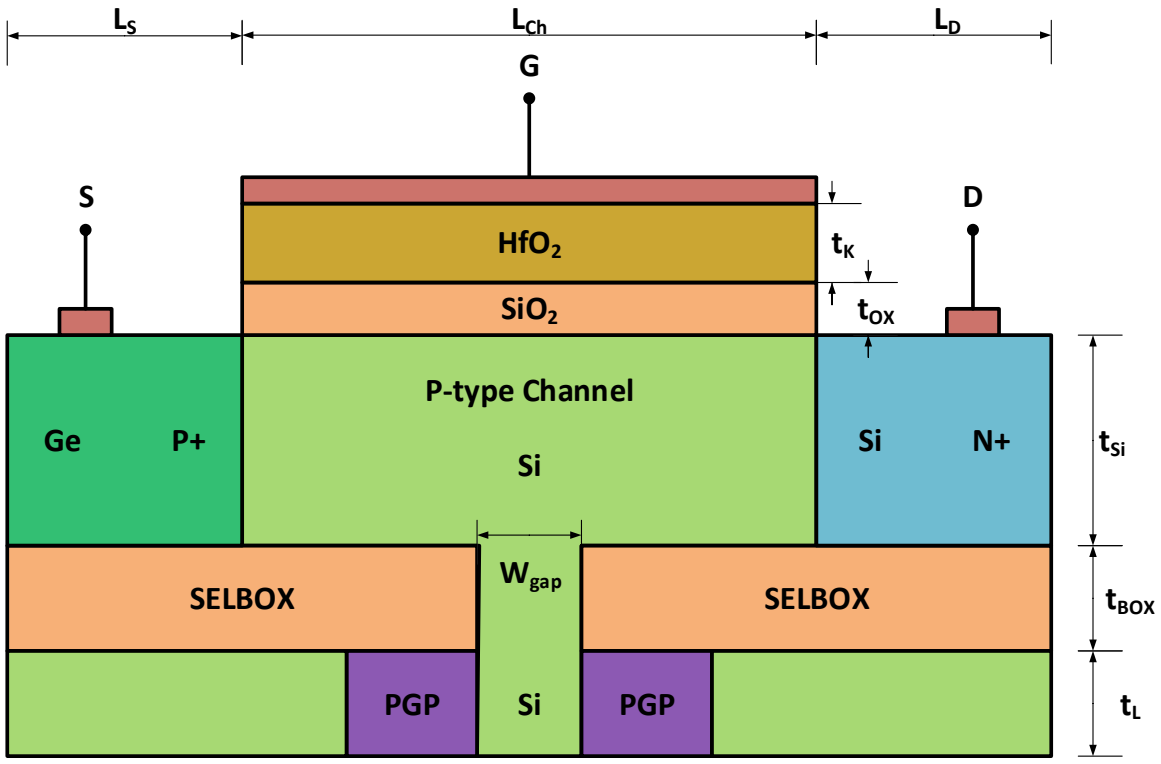


Fig 2.21 Cross-section of GSHJ-PGP-STFET

2.22 Vertical Dielectric Modulated TFET (V DM TFET) for biomolecule sensing

Studies are conducted to utilise TFET features to the development of biosensors. Regarding this, Verma et al. [24] suggested a label free biomolecule sensor based on TFETs that makes use of vertical dielectric modulation, or V DMTFET (Fig. 2.22). Performance comparison is made with the previously established lateral DMTFET (L-DMTFET). In order to achieve both lateral and vertical tunnelling, a strongly doped n+ pocket is added to the device. This significantly boosts the ON current & lowers the SS or subthreshold swing. Additionally, a source-to-gate overlap is present to increase sensitivity. The device has two nanocavities: a bigger one for biomolecule sensing, L_{c2}=15 nm below the front gate, and a smaller one, L_{c1}=10 nm below the rear gate. Higher sensitivity results from filled cavities; to increase the sensitivities, gate metals M1(Φ_{M1} = 4.3 eV) is used near the drain end & M2 (Φ_{M2} = 3.8 eV) is utilised near the source end. The dimensions of the device are: channel length (L_{ch} = 42 nm), source and drain lengths (L_s = L_d = 20 nanometres), body-thickness (t_{Si} = 10 nm), oxide-thickness (t_{ox} = 6 nm), & cavity thickness (t_{cavity} = 5 nm). n+ pocket doping is 5×10^{19} cm^{-3}, and source, channel, and drain doping are, respectively, 5×10^{19}, 1×10^{12}, and 5×10^{18} cm^{-3}.

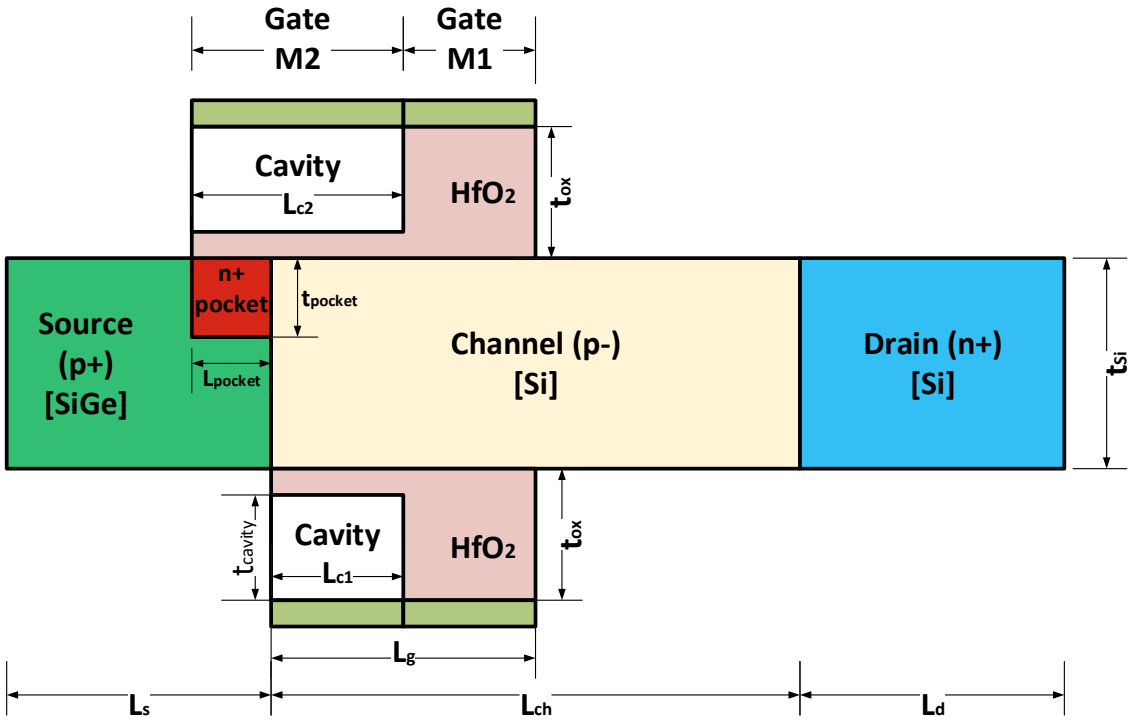


Fig2.22 Cross section of V DMTFET for bio-sensing

Table 2.1: Literature review

Detail of the Journal/ Book / Book chapter/ website link	**Year of Publication**	**Indexing of Journal (Scopus/ SCI index etc.)**	**Main findings or conclusion relevant to proposed research work**	**Remarks**
Dielectric and work function engineered TFET for ambipolar suppression and RF performance enhancement. *Electronics Letters*	2016	Scopus & SCI	A dual-gate-metal work-function transistor (HGDDW Tunnel FET) with a hetero gate dielectric base that minimises ambipolar behaviours and improves RF figure of merits has been proposed.	The device is having channel length of 50nm. Dielectric combination of SiO_2-HfO_2 is used.
Gate drain-overlapped-asymmetric gate dielectric-GAA-TFET: a solution for suppressed	2016	Scopus	Created the GDO HDGAA Tunnel FET, a TFET with drain to gate overlap, heterogeneous gate -	The device uses Gate to Drain overlap.

ambipolarity and enhanced ON state behaviour. *Applied Physics A*			dielectric, and gate wrapped all-around the channel structure. While the hetero material used for the gate dielectric improves the ION, the Gate Drain overlapping inhibits the ambipolar current. Additionally, the gate's surrounding structure enhances its ability to control the tunnelling current.	Gate all around the channel structure is used.
A Barrier Controlled Charge Plasma-Based TFET with Gate Engineering for Ambipolar Suppression and RF/Linearity Performance Improvement. *IEEE Transactions on Electron Devices*	2017	Scopus & SCI	created the DMCG-CPTFET, a TFET with a dual-metal control gate that utilises charge plasma technology. Three metals, each with a distinct purpose, are used to construct the gate. Auxiliary gate on the drain side, tunnelling gate on the source side, and control gate in the middle. Whilst the auxiliary gate inhibits ambipolarity, the tunnelling gate enhances ON state performance.	The device uses charge plasma technology on TFET. It has triple gate with different work function metals.
Performance Assessment of a Novel Vertical Dielectrically Modulated TFET-Based Biosensor. *IEEE Transactions on Electron Devices*	2017	Scopus & SCI	TFET-based label-free biomolecule sensor proposal Additionally, a gate to source overlapping is present to increase sensitivity. The biomolecule sensing	Vertical dielectric modulation is used by the apparatus. In order to achieve both lateral and vertical tunnelling, a strongly doped n+

			device consists of two nano cavities.	pocket is added to the device. This significantly boosts the ON condition current and lowers subthreshold swing.
A novel heteromaterial gate-underlap electrically doped TFET for improving DC/RF and ambipolar behaviour *Superlattices and Microstructures*	2018	Scopus & SCI	Suggested a TFET with a heterogeneous body, low band gap SiGe near the source and Silicon at the channel & drain, electrical doping, and gate underlapping. The device in question is known as HM-GUL-EDTFET.	The device uses charge plasma technology on TFET. The device uses a source region made of SiGe. The concept of Gate underlap is used.
Design and performance analysis of Dual Gate All around Core-Shell Nanotube TFET *Superlattices and Microstructures*	2019	Scopus & SCI	Constructed a TFET based on Si nanotubes with two gates: a core that runs through the middle of the channel and a shell that wraps around the outside of the channel. Its vertical device shape significantly contributes to the ON state current enhancement.	The device uses Si nanotube. Two gates are used one in the core and other as an outer wrapper all around the channel for better control and enhancement of channel current.
Optimization of pocket doped junction less TFET and its application in digital inverter. *Micro & Nano Letters*	2018	Scopus & SCI	Developed the JL-TFET, a junction-less TFET having SiGe n+ pocket of doping near the source region that can be used to build effective inverter circuits. Two metal	The device utilises junction less TFET design. It has n+ SiGe pocket doping near the source end.

			gates, one fixed and the other control, with distinct purposes, are part of the apparatus.	A pair of metal gates that have distinct work functons.
Analytical modelling and simulation of drain doping engineered splitted drain structured TFET and its improved performance in subduing ambipolar effect. *IET Circuits, Devices and Systems*	2019	Scopus & SCI	Constructed the SD-SG TFET, a novel type of TFET with a single gate and a split or fractured drain. Drain doping engineering is utilised in the device to produce a split or separated drain, with one part heavily doped and the other one lightly doped. The doping is arranged in descending order. Ambipolar conduction is significantly reduced by the divided drain arrangement.	The performance of four devices with varying splitted drain (SD) relative location is evaluated and assessed. In terms of performance, all the architectures outperformed traditional TFETs.
Performance improvement of nano wire TFET by hetero-dielectric and hetero-material: At device and circuit level. *Microelectronics Journal*	2019	Scopus & SCI	Suggested the SiGe S NW TFET, a nanowire based TFET with a heterogeneous gate - dielectric & a source composed of lower band gap SiGe substance. Its performance was assessed for use in the construction of analog circuits such as operational amplifiers.	Low band gap SiGe used for source. Dielectric combination of SiO_2-HfO_2 is used for gate oxide.
Surface Potential and Drain Current Analytical Model of Gate All Around Triple Metal TFET	2017	Scopus & SCI	Built a Triple-Metal Gate-All-Around Tunnel FET (TMGAA Tunnel FET) based on Si nanowire. The gate,	Triple metal gate, each having distinct work-function is used.

IEEE Transactions on Electron Devices			which is wrapped round the structure and made of three different metals, bends the energy band close to the source to boost driving current and helps to form a barrier to prevent reverse tunnelling current from draining.	Gate wrapped all around structure is implemented better control over channel conduction.
Architecture- and Gate-Oxide-Level Optimization of a Si-Based Asymmetric U-TFET for Low Power Operation: a Real-Time Gate/Drain Electrostatic Based Leakage Perspective. *Silicon*	2022	Scopus & SCI	A low power application-friendly optimised asymmetric U-shaped TFET has been suggested. The Al_2O_3 asymmetric oxide arm of the suggested TFET device is 5 nm in size. It is discovered to be the gadget best suited for minimal power usage.	Device for two-level optimisation for the suggested device, work has been done at the architectural and gate-oxide levels.
Interfacial charge analysis & temperature sensitivity of Ge source vertical tunnel FET with delta-doped layer. *Microelectronics Reliability*	2022	Scopus & SCI	A vertical TFET having low band gap Ge material with delta-doped layer is implemented.	Investigated is the relationship between interface trap charges (ITCs) and the Ge source vertical tunnelling field effect transistor's dependability with a delta-doped layer.
Noise behaviour and reliability analysis of non-uniform body tunnel FET with dual material source. *Microelectronics Reliability*	2022	Scopus & SCI	The noise analysis of the Non-Uniform Body TFET having Dual Materials Source is carried out by taking into account both the existence and	The analysis of the device is done by varying the source material to different low band gap materials.

			absence of distinct trap charge types when the device is subjected to temperature fluctuations (200 K–400 K) and variations in the source material (Si, Ge, and both Si + Ge).	The effect of different interface trap charges is considered.

2.23 A Comparative Study of Recent TFET Architectures

Table 2.2, presents a thorough parametric analysis of interesting TFET designs. Because of its splitted drain architecture and drain doping engineering, the SD SG Tunnel FET[47] exhibits the highest value of ON current. It has a drain made up of a stack of heavily doped regions stacked on top of lightly doped regions. This boosts the drive current, decreases ambipolar leakage, and widens the tunnelling-width of the channel-drain interface. Additionally, when splitted drain's relative position is changed for the channel's maximum ON-current, the I_{ON}/I_{OFF} ratio is discovered while it is at the lowest position. The VS TFET[39] has a very high feature size that will reduce packing density, despite its promise to display a minimal sub-threshold slope or SS of 17 $mVdec^{-1}$. Its vertical structure lowers the SS by having a channel over & on either side of source, as well as a double-gate that regulates transverse and lateral tunnelling. However, the structure has the disadvantage of having the lowest I_{ON}/I_{OFF} ratio. At the 30nm technology node, the HMGULED Tunnel FET[43] has a subthreshold slope or SS of 19.13 $mVdec^{-1}$ and an I_{ON}/I_{OFF} ratio = 2.73×10^{11}. One of the most in-demand and efficient options for very low power portable devices for RF/analog applications has been determined. The device suppresses gate leakage, ambipolar leakage, & low-bandgap material for the source, that improves BTBT and consequently ON state current, by using gate underlap towards the drain side. As a result, the SS is made steeper and the I_{ON}/I_{OFF} ratio is increased. Additionally, the device employs electrical doping based on charge plasma, which lowers fabrication complexity and junction leakage. As a TFET-based label-free biomolecule sensor, the V-DMTFET [24] performs well. It detects particular biomolecules by measuring the relative change in the detecting cavities' dielectric constant caused by the presence of target bio-molecules (with known dielectric-constants). It displays a good I_{ON}/I_{OFF} ratio and SS of 47 mV/dec. At the 15nm technology node, the JL SG-Tunnel FET[45] has the lowest DIBL or

drain induced barrier lowering value at just 2.1mV/V & good other performance characteristics including SS, I_{ON}, & I_{ON}/I_{OFF}. The performance parameters are significantly improved by using junction less technology with a p+ $Si_{0.7}Ge_{0.3}$ pocket between the n-channel and n+ source.

Table-2.2 Comparison of TFET designs' performances for DC parameters

*Device	I_{ON} (A/µm)	I_{OFF} (A/µm)	I_{ON}/I_{OFF}	SS (mV/dec)	DIBL (mV/V)	Channel length (nm)
HGD DW TFET[36]	1.21×10^{-4}	1.23×10^{-16}	9.83×10^{11}	_	_	50
U HJ VTFET[38]	5.2×10^{-4}	5.2×10^{-11}	1×10^{7}	_	_	100
DMCG-CPTFET[42]	6×10^{-5}	1×10^{-17}	6×10^{12}	_	_	50
V-DMTFET[24]	2.71×10^{-6}	2.71×10^{-14}	1×10^{8}	47	_	42
HGD DE DMG DL TFET[35]	1×10^{-6}	1×10^{-17}	1×10^{11}	_	_	50
HM-GUL-ED-TFET[43]	8.40×10^{-6}	3.07×10^{-17}	2.73×10^{11}	19.13	_	30
D GAA CS NT TFET[41]	_	_	_	58.3	175.29	50
JL-TFET[44]	5.71×10^{-4}	1.32×10^{-10}	4.32×10^{6}	43.6	_	35
SD-SG TFET[47]	1×10^{-3}	1×10^{-17}	1×10^{14}	_	_	50
SiGe-S-NW-TFET[34]	1.16×10^{-5}	8.63×10^{-17}	1.35×10^{11}	23.75	_	20
VS-TFET[39]	_	_	1×10^{4}	17	_	175
GOSC TFET[33]	3.75×10^{-5}	_	_	61.5	_	40
JLSGTFET[45]	9.91×10^{-4}	2.80×10^{-13}	2×10^{8}	52.3	2.1	15

Table 2.3 compares the RF/analog performance metrics of some of the very effective devices.

The SiGe-S-NW-TFET[34] exhibits the greatest GBP of 549 GHz and the largest cut off frequency of 950 GHz. To boost performance, it employs hetero-gate-dielectric having high k HfO_2 near the source and narrow bandgap SiGe material for the source in Si nanowire technology. At 0.9 ps, it also shows the shortest transit time. The maximum transconductance of 0.53 mS is found in the GDOHDGAA Tunnel FET [27] with a drain-gate overlap, a heterogeneous gate-dielectric, & a cylindrical gate throughout the structure. The device's low

cut off frequency and slow transit-time response are offset by its strong ON current, good gate control, and decreased ambipolarity.

Table-2.3 Analog/RF performance parameters comparison of TFET designs

*Device	Transconductance (gm) (mS)	Cut off frequency (f_T)(GHz)	Gain Bandwidth Product (GBP)(GHz)	Transit Time (τ) (ps)
HGD DW TFET [36]	0.29	59.6	9.97	2.67
GDO– HD–GAA-TFET [27]	0.53	38	_	20
DMCG-CPTFET [42]	_	28	_	_
HGD DE DMG DL Tunnel FET [35]	0.0052	0.22	0.069	_
HM-GUL-ED-Tunnel FET [43]	0.0554	100.6	10.8	_
D GAA CS NT Tunnel FET [41]	0.0111	130	_	_
JL-Tunnel FET [44]	0.1	100	_	_
SiGe-S-NW-Tunnel FET[34]	0.045	950	549	0.9
DE-QG-Tunnel FET [40]	0.261	34	3.9	_
JLSG Tunnel FET [45]	0.016	_	_	_
GSHJ-PGP-S TunnelFET [50]	0.029	4.7	_	_

With low bandgap SiGe pocket near source and junction less technology, the JL-TFET [44] displays moderate transconductance of 0.1mS and f_T of 100GHz. With its cylindrical core to shell dual gate all around geometry, the D GAA CS NT TFET [41] achieves a cut frequency of 130 GHz; nonetheless, its transconductance is below expectations, and the complexity of its construction and structure do not outweigh the performance gain. Additionally, the HM-GUL-ED-TFET[43] exhibits a moderate gain-bandwidth product and good f_T. It makes use of electrical doping based on charge plasma, which facilitates fabrication and lowers leakage.

2.24 Problem Formulation

The problem addressed in this thesis revolves around the design and performance optimization of a modified Tunnel Field Effect Transistor (TFET) for highly efficient, low-power, digital Very-Large-Scale Integration (VLSI) circuit applications. TFETs have emerged as a promising

alternative to conventional Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) due to their lower subthreshold swing, enhanced power efficiency, and reduced leakage currents, making them suitable for low-power, high-performance digital circuits. However, while TFETs hold potential, several challenges exist in optimizing their performance for practical VLSI applications.

The core research problem can be broken down into the following key aspects:

Design of Modified TFETs for Low-Power Operation: Current TFET designs exhibit limitations in terms of drive current and scalability, which affect their performance in digital VLSI applications. There is a need for modifications in TFET design to improve key parameters such as threshold voltage, subthreshold slope, on-state current, and off-state leakage. The challenge lies in tailoring the TFET's material, geometry, and doping profiles to meet the strict power consumption and performance requirements of modern VLSI circuits.

Performance Optimization for High-Speed Digital Circuitry: Despite TFETs showing promise for low-power operation, they often suffer from limited current drive and slower switching speeds compared to MOSFETs, especially in high-performance digital circuits. This research will explore strategies to enhance the speed and efficiency of TFETs, addressing performance bottlenecks that hinder their application in high-speed digital VLSI circuits.

Integration with VLSI Circuit Design: While TFETs may offer lower power consumption, their integration into VLSI circuits presents challenges related to compatibility with existing CMOS technologies, device scaling, and fabrication limitations. A key part of this problem is designing modified TFET structures that can seamlessly integrate into current VLSI processes without significant compromises in yield or manufacturability.

Device and Circuit-Level Performance Trade-offs: Achieving the optimal balance between low power consumption, high-speed operation, and reliable circuit performance is crucial in the context of VLSI design. The problem formulation includes evaluating various TFET modifications at both the device and circuit levels to determine trade-offs between energy efficiency, delay, and reliability for specific VLSI applications, such as logic gates, memory cells, and processor units.

Exploration of Novel Device Structures and Materials: The investigation will also consider novel materials and device structures (e.g., heterostructure TFETs, strained channels, and 2D materials) to further improve TFET performance. This involves exploring the impact of these

materials on the tunnelling mechanism and electrical characteristics of the device, as well as their compatibility with standard semiconductor processes.

2.25 Research Objectives

The primary objective of this thesis is to design and optimize modified TFET structures that achieve superior performance for low-power, high-efficiency digital VLSI circuits. The research will focus on developing new TFET architectures, improving device parameters, and addressing integration challenges to enable the use of TFETs in scalable, high-performance, and low-power VLSI systems.

Research Goals:

1. To explore and implement modifications in TFET design for enhanced performance in digital VLSI applications.
2. To identify optimal device parameters that ensure low-power, high-speed operation of TFETs in VLSI circuits.
3. To analyse the impact of material and geometric modifications on the TFET's electrical performance and scalability for VLSI applications.
4. To demonstrate the feasibility of modified TFETs in real-world digital circuit applications through simulation and experimental validation.

By addressing these research challenges, the thesis aims to advance the understanding of TFET technology and contribute to the development of next-generation low-power, high-performance digital VLSI systems.

Table-2.4 enlists all the Device* abbreviations used Table-2.2 & 2.4 as well as in the present text with their full forms.

Table-2.4 Device Abbreviations Chart

Abbreviations	Full forms
GOSC TFET[33]	Gate On Source Channel Tunnel Field Effect Transistor
SiGe-S-NW-TFET[34]	SiGe Source Nano Wire Tunnel Field Effect Transistor
HGD DE DMG DL TFET[35]	Hetero Gate Dielectric Drain Engineered Dual Metal Gate Tunnel Field Effect Transistor
HGD DW TFET[36]	Hetero Gate Dielectric Dual gate-metal Work function Tunnel Field Effect Transistor
GDO– HD–GAA-TFET [27]	Gate Drain Overlapped Hetero Gate Dielectric Gate All Around Tunnel Field Effect Transistor
U HJ VTFET[38]	U-shaped Gate Hetero Junction Vertical Tunnel Field Effect Transistor
DMCG-CPTFET[42]	Dual Metal Control Gate Charge Plasma Tunnel Field Effect Transistor
V-DMTFET[24]	Vertical Dielectric Modulated Tunnel Field Effect Transistor
HM-GUL-ED-TFET[43]	Hetero Material Gate Underlapped Electrically Doped Tunnel Field Effect Transistor
D GAA CS NT TFET[41]	Dual Gate All Around Core Shell Nano Tube Tunnel Field Effect Transistor
JL-TFET[44]	Junction Less Tunnel Field Effect Transistor
SD-SG TFET[47]	Splitted Drain Single Gate Tunnel Field Effect Transistor
VS-TFET[39]	Vertical Sandwiched channel Tunnel Field Effect Transistor
DE-QG-TFET [40]	Drain Engineered Quadruple Gate Tunnel Field Effect Transistor
JLSGTFET[45]	Junction Less Single Gate Tunnel Field Effect Transistor
GSHJ-PGP-STFET [50]	Ge Source Hetero Junction Partial Ground Plane base SELBOX (Selective Buried Oxide) Tunnel Field Effect Transistor

CHAPTER 3

Dual Gate Tunnel FET with SiGe Pocket with 18nm technology node

A new Junction-less Double-Gate Tunnel FET is suggested, with a small (5 nm) $Si_{1-x}Ge_x$ P+ pocket located at the channel's source end. The thin pocket causes enhanced tunnelling, which is why it displays a high I_{ON}/I_{OFF} ratio. The SiGe pocket lowers OFF state leakage while the junction less behaviour raises ON state current. Better control over the drain current is ensured by the double gate construction with front and rear gates. The high value of its work function, combined with a high-k gate dielectric, further boosts the ON current. An 18 nm gate length yields an ION/IOFF ratio as high as 1011. Because of the high k oxide at the gate, which allows for better control of channel conduction by the gate, the high-k dielectric, HfO2, lowers the subthreshold slope of the ID-VGS characteristics and makes the characteristics steeper as ON current increases and OFF current decreases[51]. The threshold voltage is lowered to an extremely low value and the subthreshold slope is steepened when high work function gate metals, such as Pt, are used [52]. Therefore, lower threshold voltage and a smaller subthreshold slope result from using Pt/HfO_2 in conjunction as the gate metal-dielectric interface. Using a low band gap material can greatly improve the TFET's low ON current restriction. [53]. And as SiGe is a material with a lower band-gap its introduction [54] towards the source end of channel greatly improves the ON current of the device. In order to suggest that Pt/HfO2 provides the optimal performance, a comparative analysis of several gate metal and dielectric combinations is also conducted. Additionally, it compares various combinations of mole fraction (x) for the $Si_{1-x}Ge_x$ and demonstrates that x=3 exhibits the lowest value of OFF state current. In order to determine the suggested device's efficiency at temperatures between 200 and 400K, additional temperature analysis is carried out.

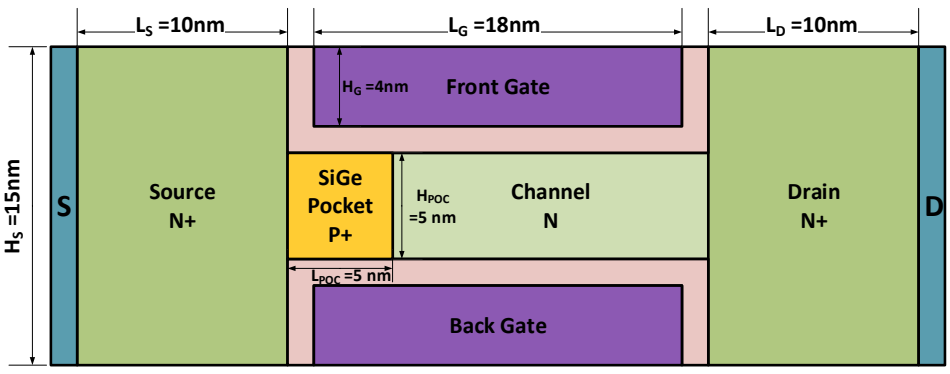


Fig.3.1 Cross-section of DGTFET with P+ SiGe pocket

3.1 Structure and dimensions of the JL DG TFET

Using the Cogenda Visual TCAD device simulator, a unique Junction-less Double-Gate Tunnel FET (JL DGTFET) is implemented. Fig.3.1 shows the two-dimensional structure of the JL DGTFET with a 5 nm SiGe P+ pocket region close to the channel's drain end. An L_g=18nm dual gate is employed to improve channel conduction control. To increase the ON current, high-k HfO_2 (25) is employed as the gate dielectric and high work function Pt (5.7eV) as the gate metal. The $Si_{1-x}Ge_x$ pocket, which was discovered to generate the least OFF state current, is taken into consideration when calculating the mole fraction value of x=0.3. A consistent doping concentration of 1e+20 cm^{-3} is applied to the source and drain areas, and a measurement of 10 nm is made. A 20 nm channel length and homogeneous 1e+16 cm^{-3} doping are employed, with the P+ SiGe pocket extending 5 nm in the direction of the source end. The proposed device's precise dimensions are shown in Table 3.1.

Table 3.1 Measurements of the n-JL DG TFET

Notation	Factor	Measure
$N_{Channel}$	Doping of Channel	1e+16 cm^{-3}
$L_{Channel}$	Length of Channel	20nm
H_{POC}	Height of Pocket	5nm
L_{POC}	Length of Pocket	5nm
L_G	Length of Gate	18nm
H_G	Height of Gate	4nm
N_D and N_S	Drain and Source Doping	1e+20 cm^{-3}
H_D and H_S	Height of Drain and Source	15nm
L_D and L_S	Length of Drain and Source	10nm

3.2 Detailed Analysis of the JL DGTFET

The suggested Junction-less DGTFET is visually simulated using TCAD for both linear (V_{DS}=0.1V) and saturation (V_{DS}=1V) regions. The transfer properties (I_D vs. V_{GS}) of the JL DGTFET with various oxide materials, gate contacts, and tight band gap pockets are displayed in Fig. 3.2. The device, when comparing Al/SiO_2 to Pt/HfO_2 gate contact/oxide combination with SiGe pocket, exhibits a very substantial improvement in the I_{ON}/I_{OFF} ratio, on the order of 10^{11}. The P+ pocket, which suppresses the OFF current, and junction lessness, which enhances the ON current, are responsible for this significant rise in the I_{ON}/I_{OFF} ratio. The suggested JL

DGTFET has extremely acute subthreshold features, which result in a subthreshold slope of roughly 63.5 mV/dec, which approaches the ideal value and surpasses the thermal budget's limitations. The JL DGTFET is compared in the linear (V_{DS}=0.1V) and saturation (V_{DS}=1V) regions in Fig. 3.3 for a range of gate contact/oxide combinations and pocket material combinations. For every case, a perfect behaviour is discovered.

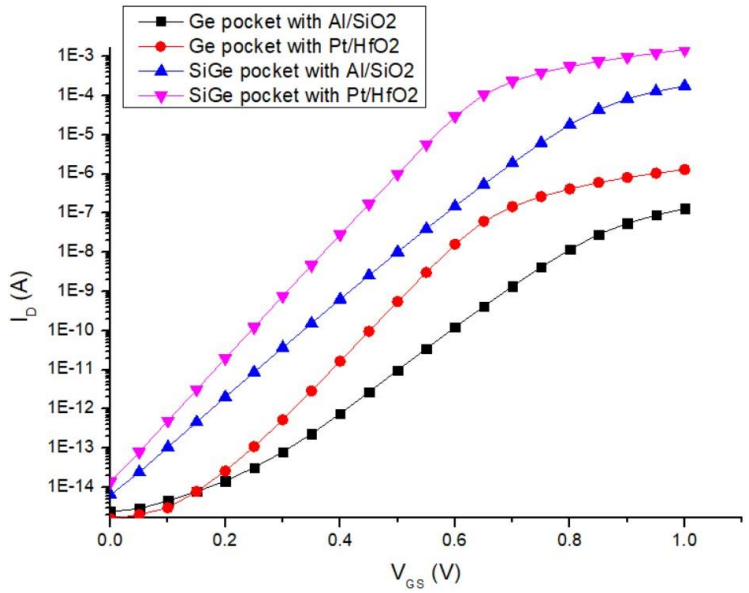


Fig.3.2 Transfer Curve of n-JL DG TFET with various gate contact, pocket and oxide

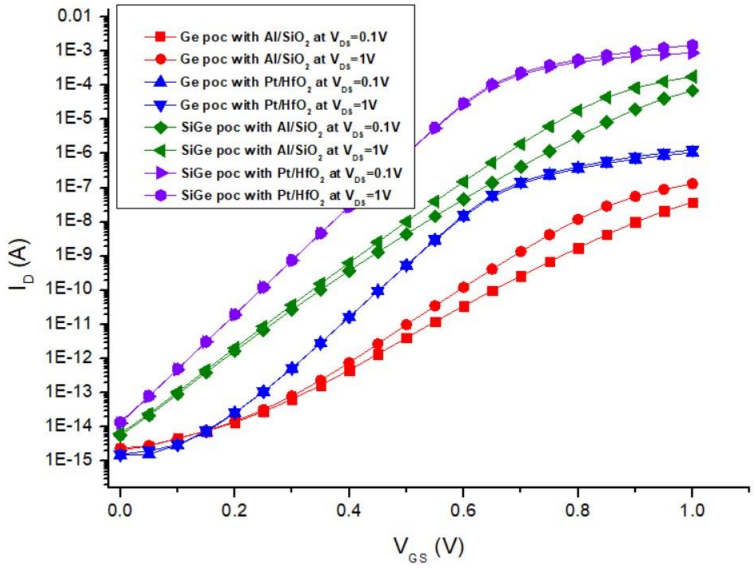


Fig. 3.3 Transfer Curve (I_D vs V_{GS}) of n-JL DG TFET in linear & saturation regions

The drain curves (V_{DS} vs. I_D) of the suggested device having the HfO_2/Pt oxide/ gate contact combination & SiGe n+ pocket is shown in Fig. 3.4. It demonstrates that the drain current becomes constant w.r.t variations in V_{DS} & increases solely with increases in V_{GS} over a certain

threshold voltage. Therefore, in accordance with the specifications, the suggested device operates in cut-off, linear and saturation modes.

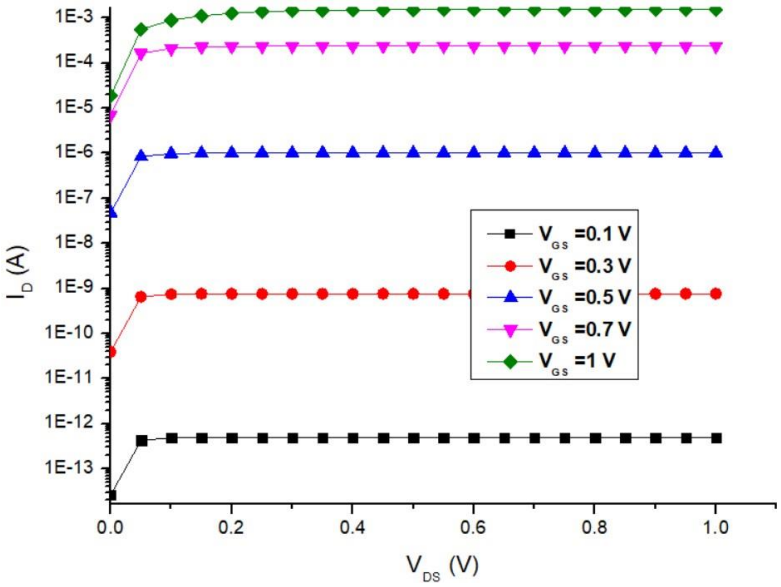


Fig. 3.4 Output Curve (I_D vs V_{DS}) of JL DG TFET

The effect of changing the gate length L_G on the device's transfer curve is seen in Fig. 3.5. The optimal transfer curve & the maximum magnitude of the I_{ON} to I_{OFF} ratio, of the order 10^{11}, have been found with 18 nm of gate length.

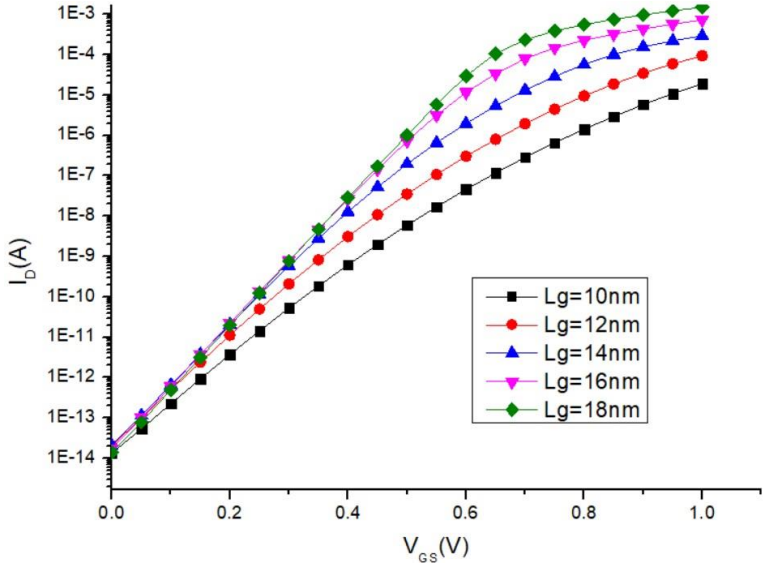


Fig. 3.5 Transfer Curves of n-JL DG TFET with varying gate lengths

The effect of changing the mole fraction x of Ge in the $Si_{1-x}Ge_x$ pocket of the suggested device is shown in Fig. 3.6. It is discovered that there is very little change in the ON state current but a significant change in the OFF state current when the magnitude of x is varied from 0.1 upto

0.9. In the range of x=0.2 to 0.3, the lowest value of OFF current is detected. Thus, the device considers x=0.3.

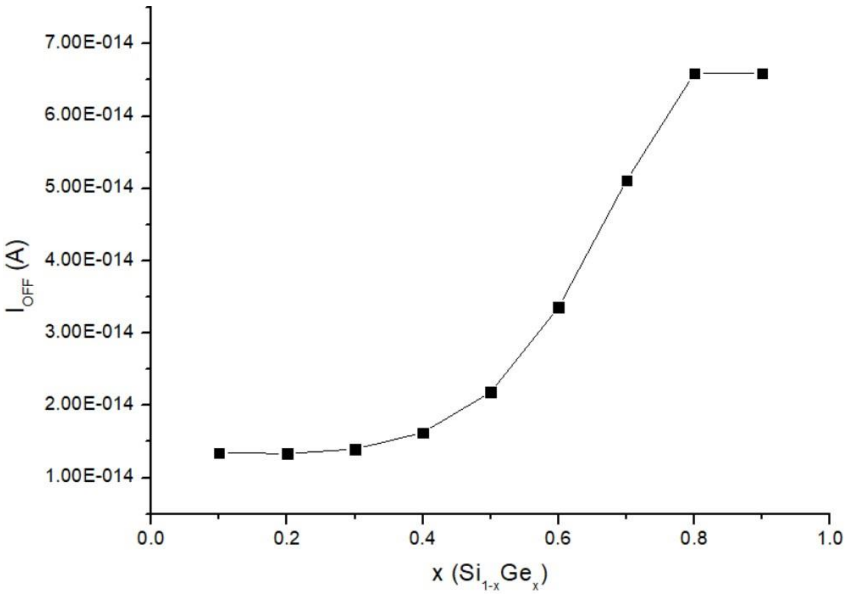


Fig. 3.6 Plot of varying mole fraction of Germanium used in SiGe

The effect of temperature change on the suggested device's transfer properties is seen in Fig. 3.7. It is discovered that a temperature change from 200K upto 400K has a negligible impact on the ON state current but a significant impact on the OFF state current. It is not practicable to operate the device at 200K, yet at that point the subthreshold slope and the IOFF are at their lowest and optimal. However, room temperature operation is also yielding encouraging outcomes.

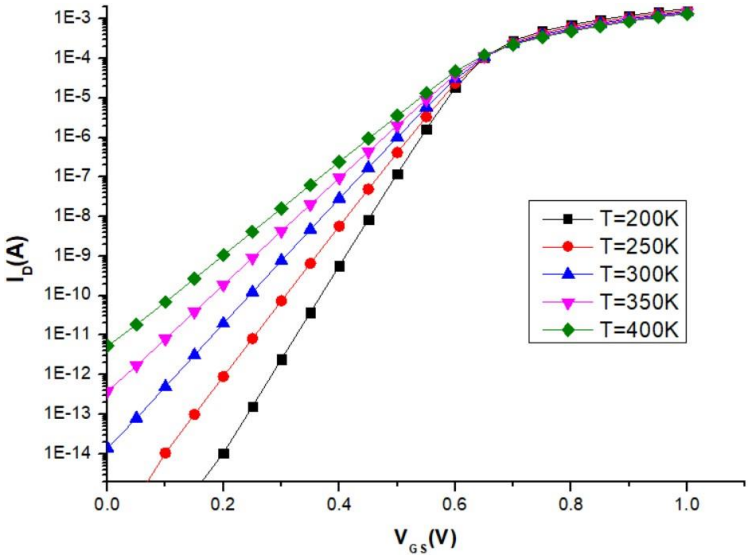


Fig.3.7 Transfer Curve (I_D vs V_{GS}) plotted for T=200 to 400K.

Table 3.2 compares the various performance parameters of junction-less DGTFETs with varying oxide and gate contact materials, all while maintaining a gate length of 18 nm. With I_{ON}/I_{OFF}=1.09E+11, a subthreshold slope of 63.5 mV/dec, which is extremely close to the optimal response, the results we got in the instance of n-JL DG TFET with Pt/HfO_2 show the best conceivable response. Additionally, a very low DIBL value of 22.2 mV/V is shown. The performance comparisons of the suggested n-JL DG TFET with various gate-lengths is shown in Table 3.3, and it was discovered that L_G=18nm once more yielded the best results in terms of SS, DIBL, and I_{ON}/I_{OFF}.

Table 3.2 Performance comparison for varying gate contacts and oxide materials

JL DG TFET	DIBL (mV/V)	SS (mV/dec)	I_{OFF} (A)	I_{ON} (A)	I_{ON}/I_{OFF}
With Al/SiO_2	122.2	80.2	6.42E-15	1.79E-04	2.79E+10
With Al/HfO_2	111.1	178.6	4.71E-09	0.0036881	7.83E+05
With Pt/SiO_2	55.5	80.1	9.38E-16	5.47E-07	5.83E+08
With Pt/HfO_2	22.2	63.5	1.39E-14	0.00152	1.09E+11

Table 3.3 Performance matrix for varying lengths of gate

Gate Length, L_G	DIBL (mV/V)	SS (mV/dec)	IOFF (A)	ION (A)	ION/IOFF
18nm	22.2	63.5	1.39E-14	0.00152	1.09E+11
16nm	24.2	68.6	1.73E-14	7.37E-04	4.26E+10
14nm	11.3	79.6	2.06E-14	2.97E-04	1.44E+10
12nm	31.1	90	2.06E-14	9.51E-05	4.63E+09
10nm	55.5	97.4	1.34E-14	1.93E-05	1.44E+09

The suggested JL DGTFET's Subthreshold Slope dependence on gate length is shown in Table 3.4 over a temperature range of 200K upto 400K. Once more, the lowest possible SS was determined to be provided by LG = 18nm. The device was discovered to operate at its peak efficiency at 200K, an unfeasible temperature. However, it was also discovered that the performance of the device at 300K or ambient temperature is satisfactory. The performance comparison between the suggested JL DG TFET and current devices is shown in Table 3.5[55] and [56]. It is discovered that, the suggested device provides a significantly high I_{ON}/I_{OFF} ratio than the current JL TFET devices.

Table 3.4 Comparison matrix of SS for varying L_G & T

Gate Length, L_G	Subthreshold Slope (mV/dec)				
	T=400	T=350K	T=300K	T=250K	T=200K
18nm	85.29	74.59	63.87	53.15	42.46
16nm	96.32	84.15	72.07	60.06	48.12
14nm	113.9	99.33	84.95	70.76	56.73
12nm	126.6	110.62	94.78	79.06	63.41
10nm	133.84	116.69	99.8	83.11	66.63

Table 3.5 Comparison matrix of JL DG TFET with contemporary TFETs

Device type	Length of Gate (nm)	I_{ON} to I_{OFF} ratio
TDJLT[56]	10nm	1.00E+02
	20nm	1.00E+07
JL SGTFET [55]	10nm	2.00E+06
SG SOI TFET[57]	18nm	1.00E+09
JL DG TFET (proposed structure)	18nm	1.09E+11

3.3 Summary

The proposed TFET structure is new and distinct. It is the first-ever double gate device with a SiGe material pocket near the source. It is thoroughly examined, along with comparisons for various combinations of gate metal and dielectric, changes in the mole fraction of SiGe, and temperature analyses is also performed for a functioning range of 200 upto 400K. The JL DGTFET device that has been suggested has the optimum performance when the gate length (L_G) is maintained at 18 nm and the oxide area of HfO_2 and Pt have gate contacts.

The magnitude of I_{ON} to I_{OFF} ratio of the structure is much larger, of the order of 10^{11} when compared to 10^6 for JL SGTFET,10^7 for TDJLT and 10^9 for SG SOI TFET for devices with alike dimensions. Thus, the proposed design illustrates approximately 10^2 to 10^5 order improvement in I_{ON} to I_{OFF} ratio with respect to the contemporary devices. Optimum results in terms of Subthreshold Slope & DIBL are also provided by the suggested device for a wide range of temperature fluctuations. Therefore, the suggested device complies well with criteria for low power, low leakage, and low subthreshold slope. In addition, it is staying within the

thermal budget restrictions when the apparatus scales in the future. equivalent to the constructed n-JL DG TFET, we may also create and optimize p-JL DG TFET in terms of materials, dimensions, and doping modifications to produce equivalent device performance and properties. Additionally, complementary JL DG TFET circuit can be constructed, fully compatible with CMOS based circuits but having significantly low power consumption by combining nJL and pJL DG TFETs.

CHAPTER 4

Low Power Inverter with SiGe Pocket N & P Channel JL DG TFETs

This chapter builds on our earlier study of JL DGTFETs (Junction Less Double Gate TFETs) featuring a 5nm $Si_{1-x}Ge_x$ P+ material pocket close to the device's source terminal[20]. First, we have summarised our device, JL DG TET, whose construction is shown in Fig. 4.1, in this study. The n-channel JL DGTFET's structure has been described. Next, its fabrication processes and dimensional data are described. Afterwards, the device is optimised concerning the selection of gate metal and gate oxide, gate length, and the mole fraction of Germanium material in the SiGe pocket near the source. Subsequently, the entire analysis of temperature is performed over a broad range of 200 upto 400K. Additionally, we implemented JL DG TFET for the p type channel as well; Fig. 4.10 illustrates this. The n-JL DG TFET and p-JL DG TFET mapping over the same plot, as well as the device properties of the p-channel, are shown in the following section. The Complementary JL DG TFET, or CJL DG TFET, is a type of n-JL & p-JL DG TFET combination that is compatible with the CMOS structures. It is used in the construction of an inverter in the chapter's final part. Using the Cogenda tool called Visual TCAD device simulator programme, the inverter is developed and simulated. It was discovered that the inverter functions flawlessly as a MOSFET inverter substitute in circuits concerning low power.

4.1 Geometry and Measurements for n channel JL DG TFET

Fig. 4.1 depicts the 2D architecture of the n-type Junction Less Dual Gate Tunnel FET (n JL DG TFET). Cogenda Visual TCAD is the device simulator tool utilised in the proposed device's implementation. In the channel near the source region, there is a heavily doped P+ type, pocket of 5 nm composed of low band gap (E_G) SiGe material. The device uses 18nm long twin gates (front as well as back) made of Pt metal with a big work function value of 5.7eV to better control current conduction in the channel. To increase the ION value, the gate oxide for both gates is large-k dielectric HfO_2(25), which replaces the widely used SiO_2.

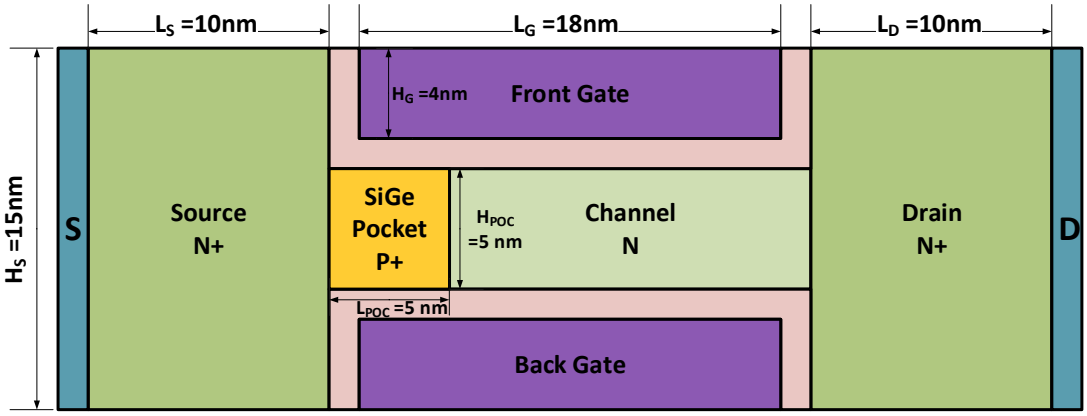


Fig. 4.1 p+ SiGe pocket nJL DG TFET

The mole fraction (x) of Germanium in the SiGe pocket is assumed to be 0.3 in order to lower the I_{OFF}. The source & drain dimensions are assumed to be of 10 nm with homogeneous large doping (1e+20 /cm^3). The moderately doped channel (1e+16 /cm^3) has a length of 20 nm, with the densely doped p+ pocket of SiGe material towards the source covering 1/4 of it. Table 4.1 provides information about the device's precise dimensions.

Table 4.1 Detailed dimensions p+ SiGe pocket nJL DG TFET

Notations	Properties	Magnitudes
N_D and N_S	Doping in the Drain and Source	1e+20 /cm^3
N_{CH}	Doping in the Channel	1e+16 /cm^3
H_D & H_S	Altitude of the Drain and Source	15nm
H_G	Gate Altitude	4nm
H_{POC}	Pocket Altitude	5nm
L_D and L_S	Dimension of the Drain and Source	10nm
L_{CH}	Dimension of the Channel	20nm
L_G	Dimension of the Gate	18nm
L_{POC}	Pocket Dimension	5nm

4.2 Process for Fabricating of the nJL DG TFET

Fig. 4.2 shows the potential process flow for fabricating the n channel JL DGTFET [58][59]. The procedure starts with a 15 x 40 nm, slightly doped n-type substrate, as seen in Fig. 4.2(a). As shown in the Fig. 4.2(b), a mask is placed to the substrate in the centre on both the front and the back to construct a 20 nm long channel. Ion implantation then forms the highly doped n+ source and drain regions at the two ends of the channel, each with a length of 10 nm. Subsequently, the mask is extracted from the channel, and the top and bottom of the channel are etched off to a depth of 5 nm, as shown in Fig.4.2(c). Subsequently, as illustrated in

Fig.4.2(d), a resist mask measuring 15 nm is once more placed to the channel's drain end on both the top and bottom, leaving only 5 nm of the channel exposed. This is followed by controlled ion implantation, which forms the SiGe p+ pocket. The next step involves the growth of high-k (HfO_2) gate oxide with a thickness of 1 nm on both channel sides using either plasma enhanced chemical vapour deposition (PECVD) or atomic layer deposition (ALD) [60] as illustrated in Fig.4.2(e). As shown in Fig.4.2(f), the metallization phase is then completed to create the Al source and drain electrodes, Pt front and back gates, and other structures.

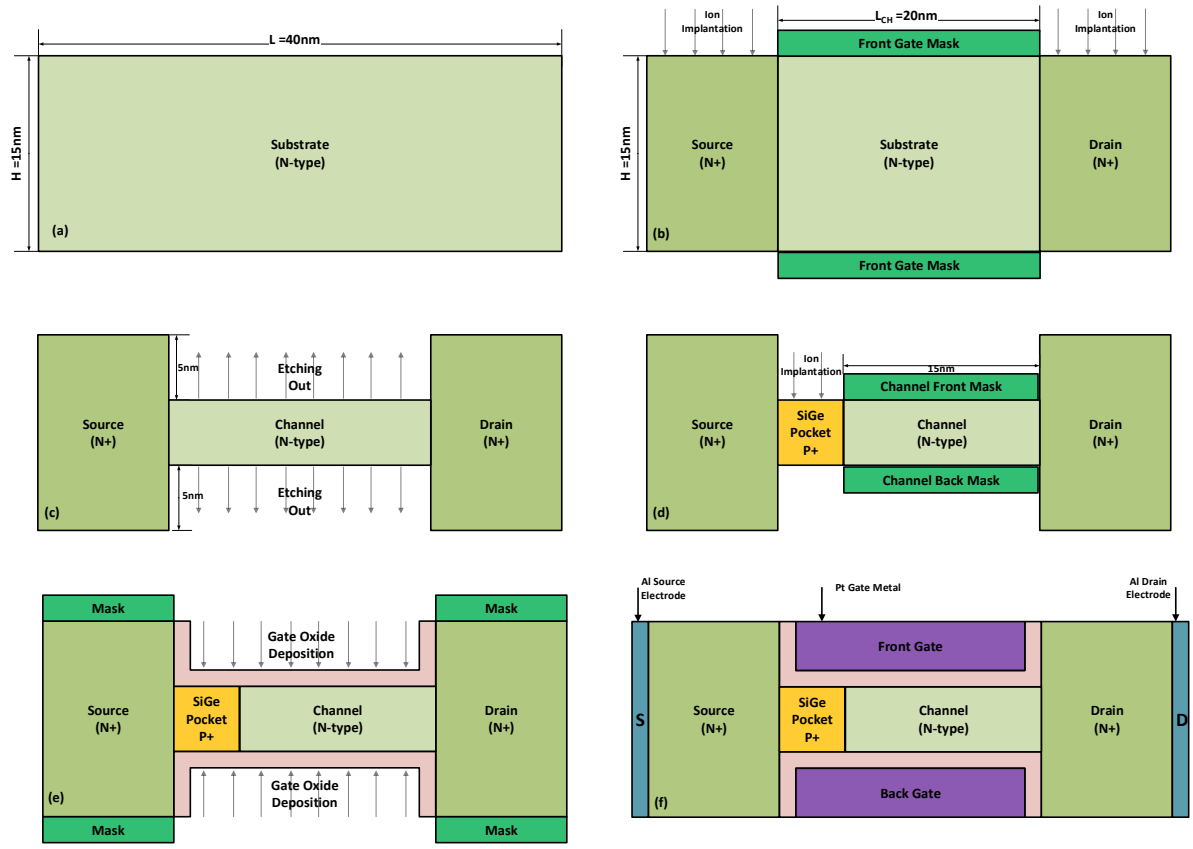


Fig.4.2 Fabrication steps for the n-JL DG TFET

4.3 Characteristic curves of the nJL DG TFET

The drain characteristics curves (I_D vs. V_{DS}) of the proposed n-JL DG TFET, which has a small band gap SiGe pocket in the channel and Pt metal gate contact having a high work function and gate dielectric of high k HfO_2, are shown in Fig. 4.3. The plot makes it very evident that only the current through drain, I_D is dependent on V_{DS} until it is increased to a little pinch-off voltage; beyond that, it only varies in response to variations in the gate to source voltage. Consequently, the apparatus amply illustrates proper function in the linear, cut-off and saturation regions in accordance with the requirements of a VCCS.

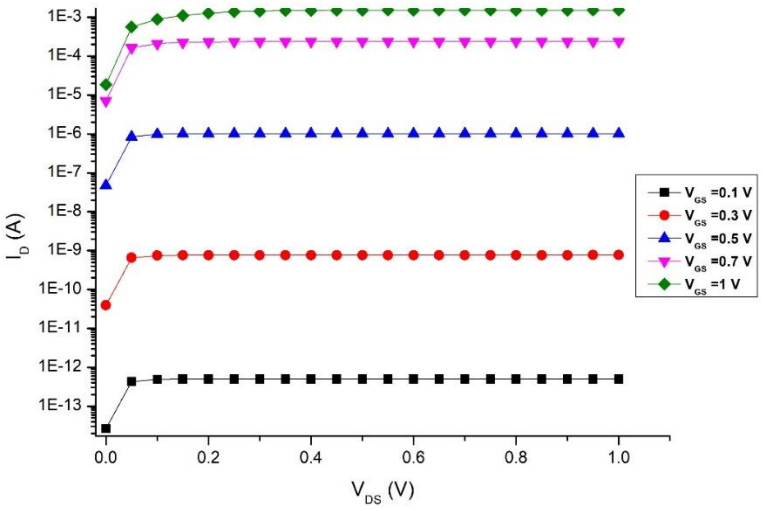


Fig. 4.3 I_D vs V_{DS} curve / Drain Characteristics of n -JL DG TFET

With Pt serving as the gate metal with high work function and HfO_2 serving as the large k gate dielectric with channel pocket of SiGe, the proposed n-JL DGTFET's transfer characteristics (I_D vs. V_{GS}) with variations in V_{DS} are shown in Fig. 4.4. It also makes clear that I_D, or the driving current, is completely independent of the output voltage V_{DS} and dependent only on V_{GS}, as would be anticipated from an efficient Voltage Dependant Current Source (VDCS). As a result, the suggested device satisfies all criteria for a quality VDCS.

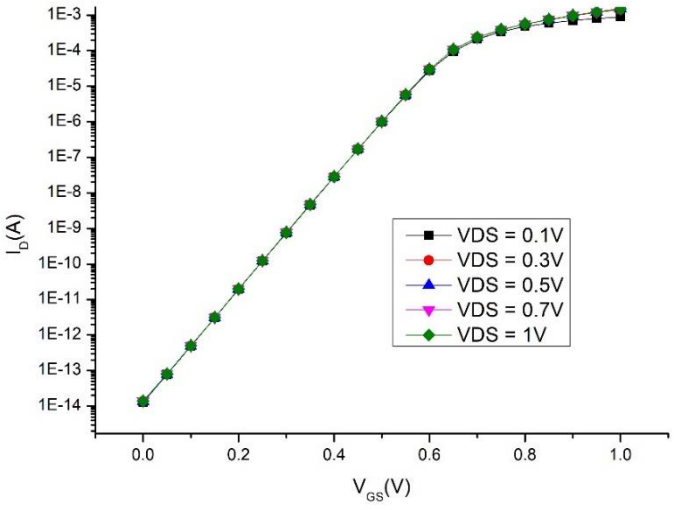


Fig. 4.4 Transfer Curve of n channel JL DG TFET

4.4 Optimisation of the nJL DG TFET

In addition, four elements of the suggested n-JL DGTFET are optimised. It is optimised in terms of the length of the gate selected, the mole fraction of Germanium in the pocket of SiGe, the gate metal, and the gate oxide. Additionally, it is designed to function well in a broad temperature spectrum. Let's examine each of the device's optimisations individually.

4.4.1 Optimisation of the Metal Contact & Oxide layer

The transfer curve (I_D vs. V_{GS}) of the n-JL DG TFET is shown in Fig. 4.5 by repeatedly changing the channel pockets' materials, gate contact metals, and gate oxide dielectric. In comparison to other material combinations, the best performance is achieved when Platinum metal is used to make the gate contacts, HfO_2 is used to make the gate oxide, and there is a SiGe pocket in the channel. The ratio of ON-state to OFF-state current for the aforementioned combination is as high as 10^{11}. The device's junction-less design is primarily responsible for the improvement of the ON current, while the presence of a P+, SiGe pocket close to the channel's source end is responsible for the reduction of the OFF-state current. Taken together, these factors result in the enormous increase in I_{ON}/I_{OFF} that was previously mentioned. The suggested device's subthreshold slope is nearly 63.5 mV/dec, which is marginally higher than MOSFETs' 60 mV/dec limit. Therefore, the suggested device is not really surpassing the MOS device subthreshold limit; nonetheless, it can be further decreased with additional research.

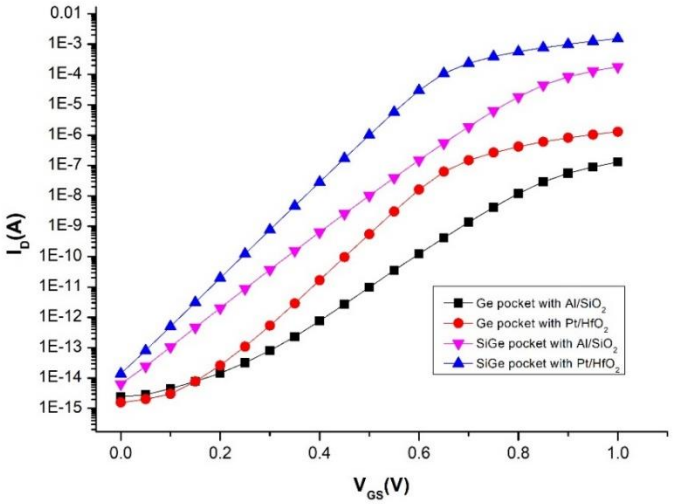


Fig.4.5 I_D vs V_{GS} for n-JL DG TFET for different pocket, metal &oxides

The diverse performance matrix of the n channel JL DG TFET employing multiple contact metals for the gate and different dielectrics as the oxide layer, while maintaining gate dimension, L_G=18nm, which is optimized in the section below, has been listed in Table 4.2. With an ON to OFF state current ratio of order 10^{11}, an SS value of roughly 63 mV/dec, and an excellent Drain Induced Barrier Lowering (DIBL) value of only 22.2 mV/V, the device configuration using Pt metal as the gate contact and high-k dielectric HfO_2 as the gate oxide exhibits the most promising results.

Table 4.2 Performance Matrix of n-JL DG TFET

Gate Metal & Oxide	**DIBL (mV/V)**	**SS (mV/dec)**	**I_{OFF} (A)**	**I_{ON} (A)**	**I_{ON}/I_{OFF}**
Al & SiO_2	122.2	80.2	6.42e-15	1.79e-4	2.79e+10
Al & HfO_2	111.1	178.6	4.71e-9	0.0036881	7.83e+5
Pt & SiO_2	55.5	80.1	9.38e-16	5.47e-7	5.83e+8
Pt & HfO_2	22.2	63.5	1.39e-14	0.00152	1.09e+11

4.4.2 Optimisation of the Length of the Gate

By changing the length of the gate L_G in each scenario, the transfer curve, of I_D and V_{GS}, is presented for the suggested device in Fig. 4.6. The plot makes it evident that an 18 nm of gate length yields the best results and a large (about 10^{11}) value of I_{ON}/I_{OFF}.

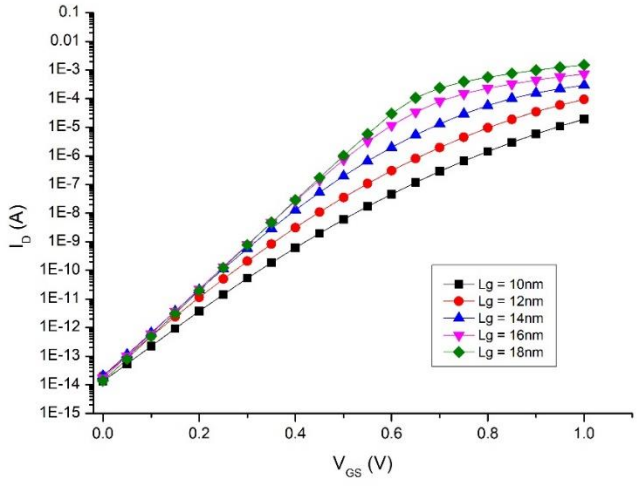


Fig.4.6 Transfer curve of the device with changing L_G

Table 4.3 shows the n channel JL DG TFET's performance matrix for a range of L_G values. Additionally, in this matrix, the most efficient gate length—in terms of performance metrics like SS, DIBL, and I_{ON}/I_{OFF}—is determined to be 18 nm.

Table 4.3 Performance Matrix of n-JL DG TFET with varying L

Length of Gate L_G	I_{OFF} (A)	DIBL (mV/V)	SS (mV/dec)	I_{ON}/I_{OFF}	I_{ON} (A)
18nm	1.39e-14	22.2	63.5	1.09e+11	0.00152
12nm	2.06E-14	31.1	90	4.63e+9	9.51e-5
10nm	1.34E-14	55.5	97.4	1.44e+9	1.93e-5
16nm	1.73e-14	24.2	68.6	4.26e+10	7.37e-4
14nm	2.06e-14	11.3	79.6	1.44e+10	2.97e-4

4.4.3 SiGe pocket mole fraction optimization

The OFF current of n-JL DG TFET in the $Si_{1-x}Ge_x$ pocket region of the device is displayed versus the mole fraction(x) value of Ge in Fig. 4.7. Since it was shown that there is very little influence of fluctuation of Germanium mole fraction on I_{ON}, the impact on I_{OFF} is only shown in the plot. The material $Si_{0.7}Ge_{0.3}$ is used for the pocket, and the value of 0.3 is taken into consideration for the design. The Mole percentage of Germanium in the small band gap SiGe pocket portion varies from 0.1 upto 0.9, & the least feasible OFF current is attained around 0.1 to 0.3.

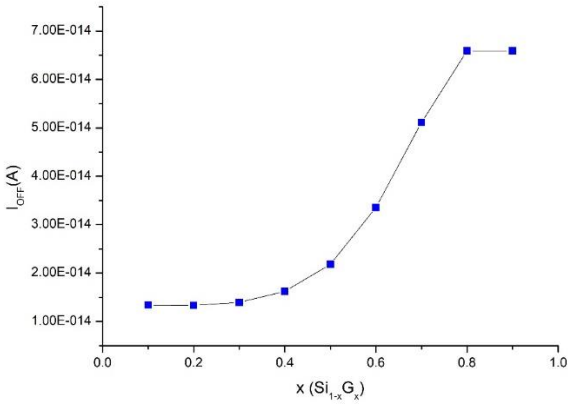


Fig.4.7 Plot of Mole fraction of Ge & OFF state Current

4.4.4 Optimisation with Temperature

The transfer curve, or I_D vs. V_{GS}, for n JL DG TFET are plotted in Fig. 4.8 by changing the temperature from 250K to 400K. Plot analysis makes it abundantly evident that while

temperature change has little to no effect on the I_{ON}, it causes an increase in I_{OFF}. The I_{OFF} value should be as low as possible to ensure optimal device operation, it also lowers the SS. While the magnitude at ambient temperature is likewise noteworthy, the optimal value for I_{OFF} is obtained at 250K.

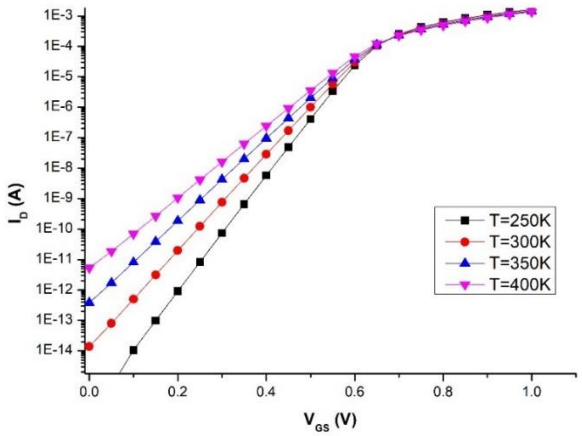


Fig. 4.8 Transfer Curve of n-JL DG TFET for T=250 to 400K

The output or drain characteristics, or I_D vs. V_{DS} plot, for the suggested device with a temperature change of 200 to 400K are shown in Fig. 4.9. The plot unequivocally demonstrates how temperature affects the saturation ON state current, which rises as temperature falls. As anticipated, T=200K yields the maximum I_{ONsat}, or saturation ON current, but the value at room temperature is also noteworthy.

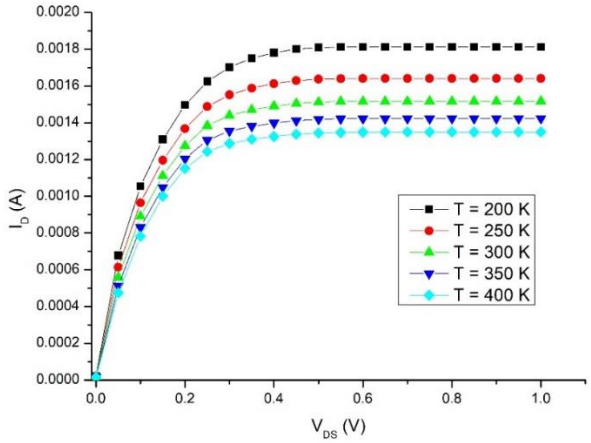


Fig.4.9 Drain Curve of n-JL DGTFET for T=200 to 400K

A matrix comparing the subthreshold slope to variations in temperature and gate length is shown in Table 4.4. It shows how, in the case of the planned n-JL DGTFET, the SS depends on the L_G and T. The table provides more evidence that the device attains the lowest SS with a gate length of 18 nm. The temperature at 200K yields the lowest SS value, as would be predicted, but the value at 300K is also within acceptable bounds.

Table4.4 Comparison of SS for different L_G & T

Gate Length, L_G (nm)	SS (mV/dec)				
	T=350 K	T=400 K	T=200 K	T=250 K	T=300 K
18	74.59	85.29	42.46	53.15	63.87
12	110.62	126.6	63.41	79.06	94.78
10	116.69	133.84	66.63	83.11	99.8
16	84.15	96.32	48.12	60.06	72.07
14	99.33	113.9	56.73	70.76	84.95

4.5 Construction of p-JL DG TFET

Following alike fabrication methods as shown in Fig. 4.2 for n-JL DG TFET, the P-channel counter portion of the JL DGTFET is similarly designed and simulated using the device simulator tool named Visual TCAD from Cogenda. The p-JL DGTFET and the n-JL DGTFET are identical in terms of dimensions. The p-JL DGTFET's detailed construction is shown in Fig. 4.10. In this case, P+ impurities are present in the highly doped (1e+20 cm^{-3}) source and drain Si regions. The channel area has a moderate 1e+16 cm^{-3} p-type doping. A highly doped 5 nm N+ SiGe pocket is introduced close to the channel's source end. Consideration is given to the previously optimised gate metal Pt and gate oxide HfO_2. In this design, the optimal gate length of 18 nm is taken into account. Additionally, only 0.3 is used as the mole fraction of Ge in the SiGe pocket because it was previously tuned for the lowest I_{OFF}.

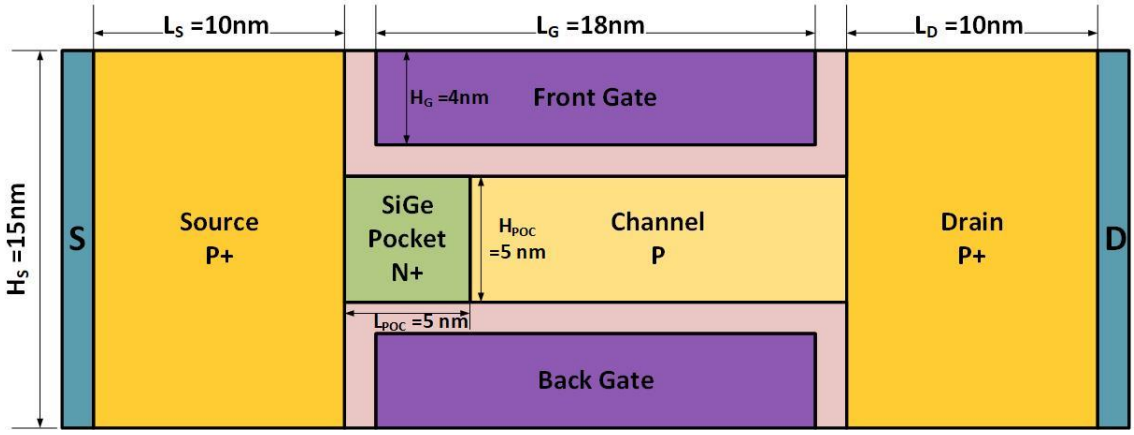


Fig.4.10 N+ SiGe pocket p-JL DG TFET

4.5.1 Characteristics of p-JL DG TFET

With Pt metal as the gate terminal contact and HfO_2 as the gate dielectric & pocket material close to the SiGe channel's source end, the drain characteristics (I_D vs. V_{DS}) of the p-JL DG TFET are shown in Fig. 4.11. The plot makes it abundantly evident that I_D depends exclusively on V_{GS} and becomes completely independent of the Drain to Source voltage at a small value of V_{DS}, commonly known as the pinch-off voltage. As would be expected from a p channel device, the saturation drain current increases when V_{GS} is raised in the opposite direction. As a result, the device also operates satisfactorily for the p channel.

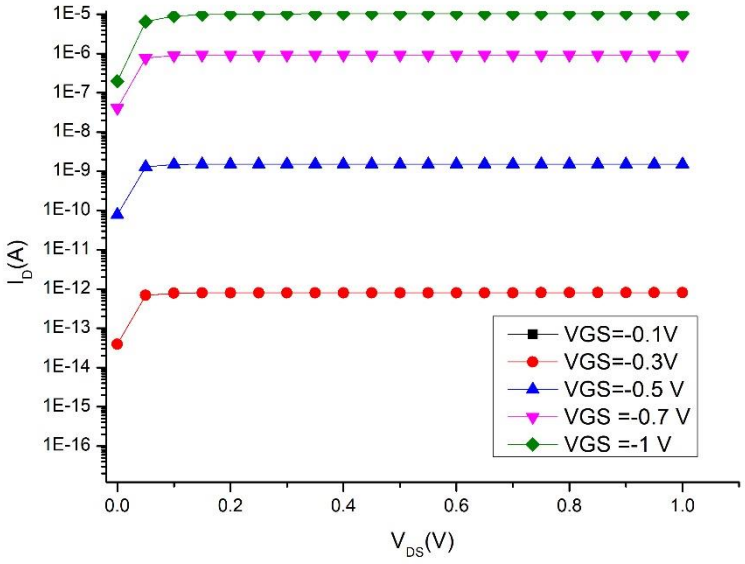


Fig.4.11 I_D vs V_{DS} for p-JL DG TFET

The transfer characteristics (I_D vs. V_{GS}) with variations in V_{DS} for the p-JL DG TFET with a pocket of SiGe material and a gate terminal contact of Pt metal and a gate dielectric of HfO_2 are shown in Fig. 4.12. The plot makes it very evident that I_D, or the drive current, is completely independent of the output voltage V_{DS} and solely dependent on V_{GS}, as would be expected from a good Voltage Controlled Current Source (VCCS). As a result, the suggested device satisfies all of the criteria for a high-quality VCCS for p-channel.

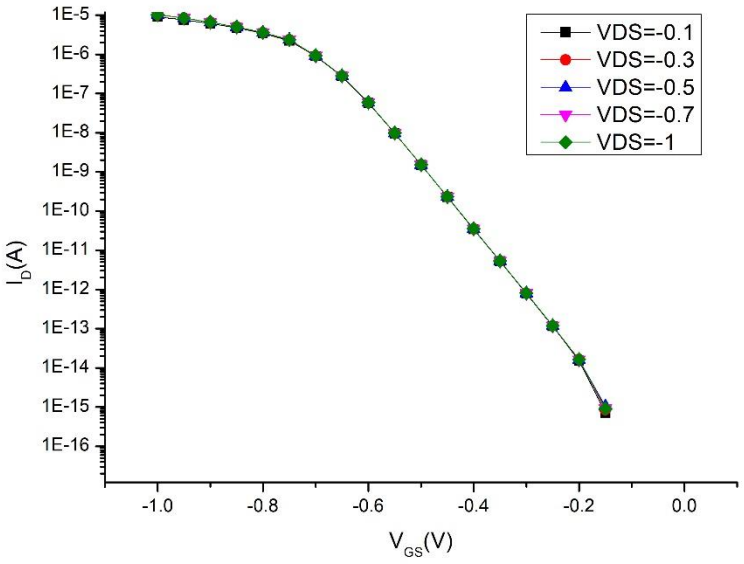


Fig.4.12 I_D vs V_{GS} for p-JL DG TFET

The transfer characteristics (I_D vs. V_{GS}) of the n and p-JL DGTFETs are represented and plotted together on the same figure in Figure 4.13. It demonstrates that they are nearly identical in threshold voltage and perfectly complimentary to one another in terms of both structure and functionality.

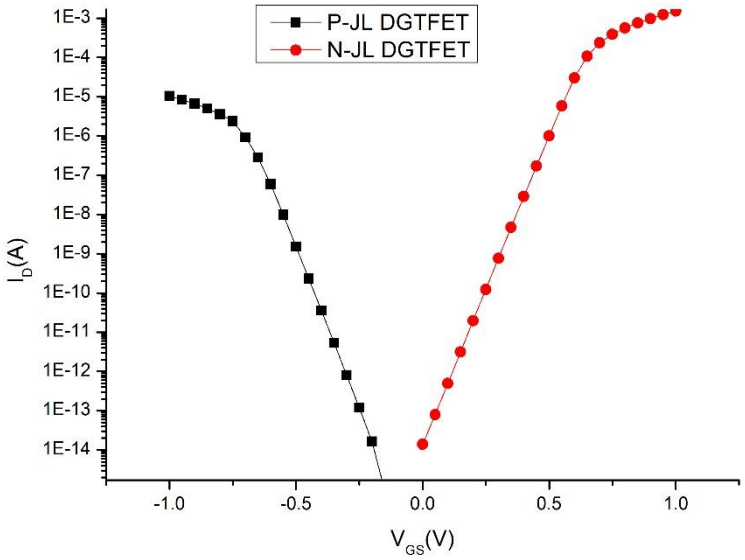


Fig.4.13 I_D vs V_{GS} for n and p-JL DG TFET together on the same plot

4.6 Construction of Inverter using n & p JL DG TFET

The inverter developed with the suggested n-channel and p-channel JL DG TFET is shown in Figure 4.14. The device receives its input via the gate contact of both the n-JL and p-JL DG TFETs. The input terminal of the inverter is made up of the four gates—the front and back gates of the n-channel device and the front and back gates of the p-channel device—that are connected to one another. The device's output terminal is created by joining the drains 1 (of the p-JL DGTFET) and 2 (of the n-JL DGTFET) together. The device exhibits the expected behaviour of an inverter when the applied voltage to the input terminal is high, and the output is low when the applied voltage to the input is low. There is a connection between the two drains. V_{DD} is connected to source 1, and GND is connected to source 2. Figure 4.15 displays the output that the inverter produced. The output obtained is 0 when the input is 1, and vice versa. The behaviour of the inverter output is nearly perfect. This demonstrates the great response and compatibility of the proposed JL DG TFET with CMOS technology.

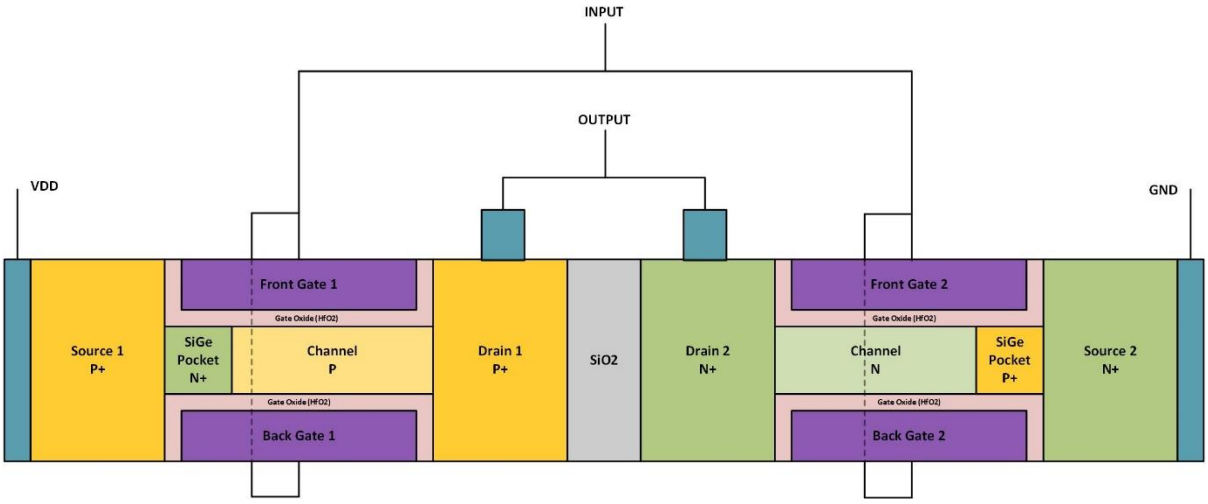


Fig. 4.14 Inverter using n & p- JL DG TFET

4.7 Summary

The Junction-less Dual Gate Tunnel FET (JL DGTFET) is a novel device that features a SiGe material pocket near the source area within the channel. First, the device's Drain and Transfer characteristics are ascertained, and it is built for n channel, or n-JL DG TFET. After that, it is optimised in four different ways. In terms of choosing the gate metal, gate oxide, Ge mole fraction inside the SiGe material pocket in the channel, and gate length, it is optimised. It is also designed to function well in a broad temperature range. It was discovered that the device

operated most efficiently when the gate electrode was constructed of Pt metal, the gate dielectric was built of HfO_2, and the gate length was fixed at 18 nm.

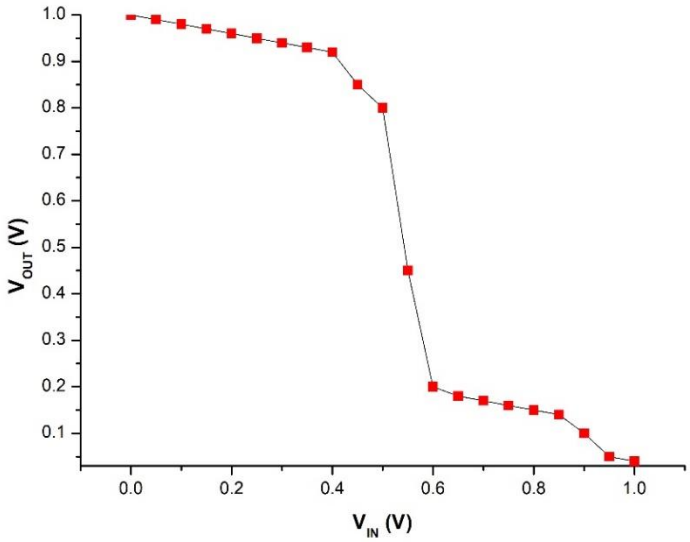


Figure 4.15 V_{OUT} v/s V_{IN} plot of the inverter made with c-JL DG TFET

For the device, an extremely high value of around 10^{11} for the ON state to OFF state current ratio is obtained. The device achieves a subthreshold slope of 63.5mV/dec and a drain induced barrier lowering (DIBL) of 22.2mV/V. The apparatus exhibits satisfactory performance even when exposed to a broad temperature range of 200K to 400K.Then, using the same design approach and manufacturing processes, p-type junction-less DG TFETs are likewise implemented and optimised, with consideration for the n-channel device's size, materials, and doping limitations. Lastly, to demonstrate their complementary nature, the combination of n channel JL DG TFET and p channel JL DG TFET are matched with each other on the same transfer characteristic curve. Afterwards, an inverter circuit with excellent, nearly ideal response was implemented using the complementary JL DG TFET that was thus produced. This inverter required significantly less power than a CMOS inverter of comparable dimensions. Additionally, it is discovered that the device is CMOS compatible, making it simple to integrate into existing circuits.

CHAPTER 5

Asymmetric double gate P-I-N Tunnel FET

With just minor structural changes, a modified TFET design has been developed, which is an altered version of our prior device[20]. The goal of present research is to find a suitable MOSFET substitute that can be used in nanoscale, ultra-low power VLSI circuits while still working with current CMOS circuits. The device's fundamental TFET structure is created by a lightly doped n-type/intrinsic channel formed on silicon material, a highly doped N+ region serving as the drain, and a highly doped P+ region serving as the source. To improve control over the channel conduction, the device incorporates two gates. To increase the ON state tunnelling current, a highly doped, low band-gap p+ type SiGe pocket is positioned close to the device's source. To improve the efficiency, the gate oxide is subjected to dielectric engineering. The gate oxide is composed of low-K SiO_2 at the drain end and high-K HfO_2 towards the source area. In addition, the device has an asymmetric gate structure[28], [61]–[64], with the front gate overlapping the source by 1 nm and the drain by the same amount of underlap. In this way, a reverse underlap-overlap combination is applied to the back gate. More channel conduction and improved gate control are provided by the suggested asymmetry. Fig. 5.1 shows the proposed device's structure. The suggested device has low DIBL and SS, a high I_{ON}/I_{OFF} ratio, and an extremely high ON current. However, it is still difficult to verify the ambipolar conduction to a significant degree, necessitating a little more material and dimension investigation.

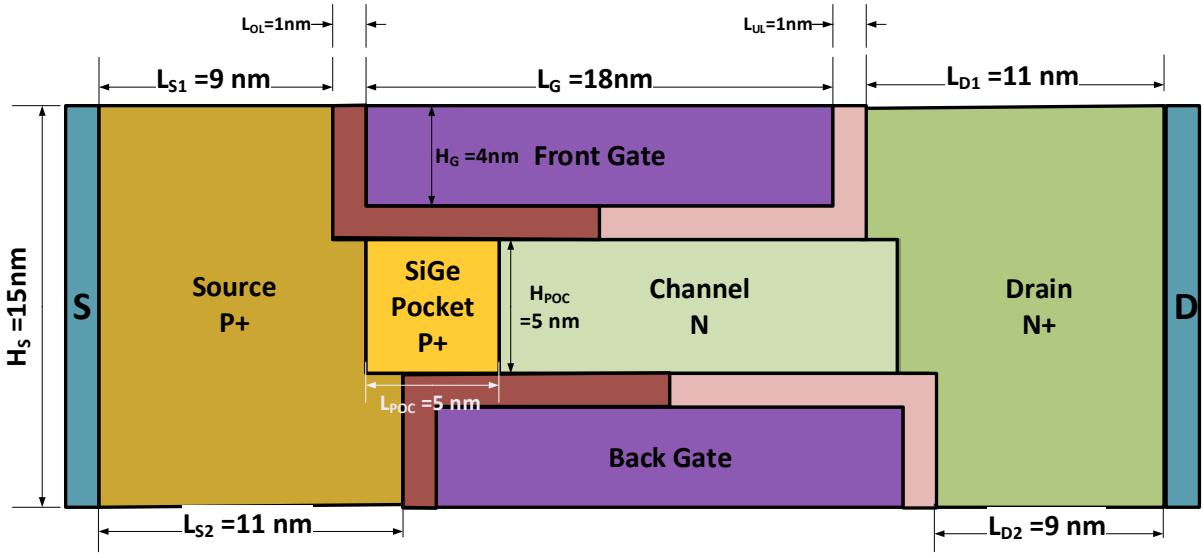


Fig. 5.1 proposed Asymmetric double gate P-I-N TFET structure

5.1 Dimensions and Structure of Asymmetric double gate P-I-N TFET

The Silvaco Atlas Device Simulator Tool is used to model the suggested device as it is seen in Fig. 5.1. Fig. 5.2 shows the device's structure as plotted on Tonyplot and modelled in Silvaco Atlas' DeckBuild Tool. The device's 18 nm channel length was established after a thorough simulation process. For the front and back gates, the overlap and underlap lengths are assumed to be 1 nm apiece. The P+, SiGe source pocket is 5 nm x 5 nm. Polysilicon is used to make the gate contacts for the front and back gates. The gate oxide is made of a combination of HfO_2/SiO_2. For the source and drain, 1e+20 cm^{-3} of doping is employed. 1e+16 cm^{-3} of extremely low doping is used to create the channel. Table 5.1 provides more illustrations of the device's size and thorough doping.

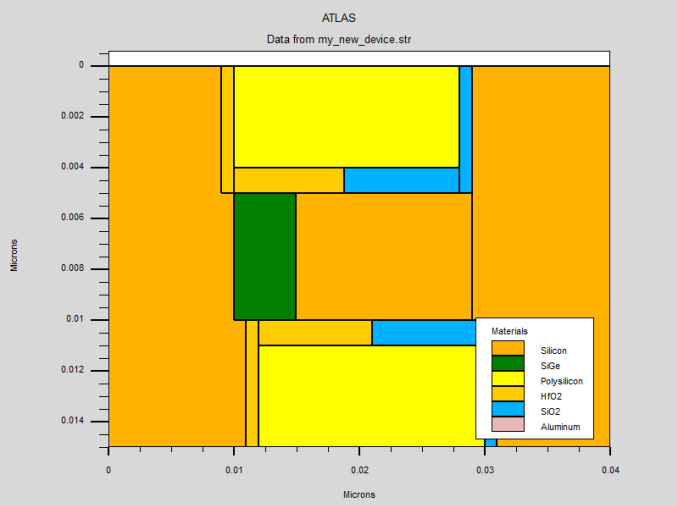


Fig.5.2 Asymmetric double gate P-I-N TFET on Tonyplot of Silvaco Atlas

Table 5.1 Asymmetric double gate P-I-N TFET Dimensions

Parameters of the Device	Labels Used	Values and Dimensions
Gate Overlap Length	L_{OL}	1nm
Gate Underlap Length	L_{UL}	1nm
Channel Doping	N_{CH}	1e+16 /cm^3
Source and Drain Doping	N_S and N_D	1e+20 /cm^3
Channel Length	L_{CH}	20nm
Gate Length	L_G	18nm
Length of the SiGe Pocket	L_{POC}	5nm
Source and Drain Length	L_S and L_D	10nm
Gate Height	H_G	4nm
SiGe Pocket Height	H_{POC}	5nm
Source and Drain Height	H_S and H_D	15nm

5.2 Findings and Interpretations

The Silvaco Atlas device simulator is used to simulate the suggested device. The device's transfer characteristics are shown in Fig. 5.3. In the I_D-V_{GS} characteristics, the gate to source voltage is adjusted in stages of 0.1 V from 0 to 1.5 V. It is found that the drain to source voltage has very little effect over the transfer curve, indicating nearly ideal characteristics and a very low Drain Induced Barrier Lowering (DIBL) value. According to the given device's drain characteristics, the drain current is completely dependent on changes in the gate to source voltage and is essentially independent of the drain to source voltage, functioning as an ideal voltage-controlled-current-source.

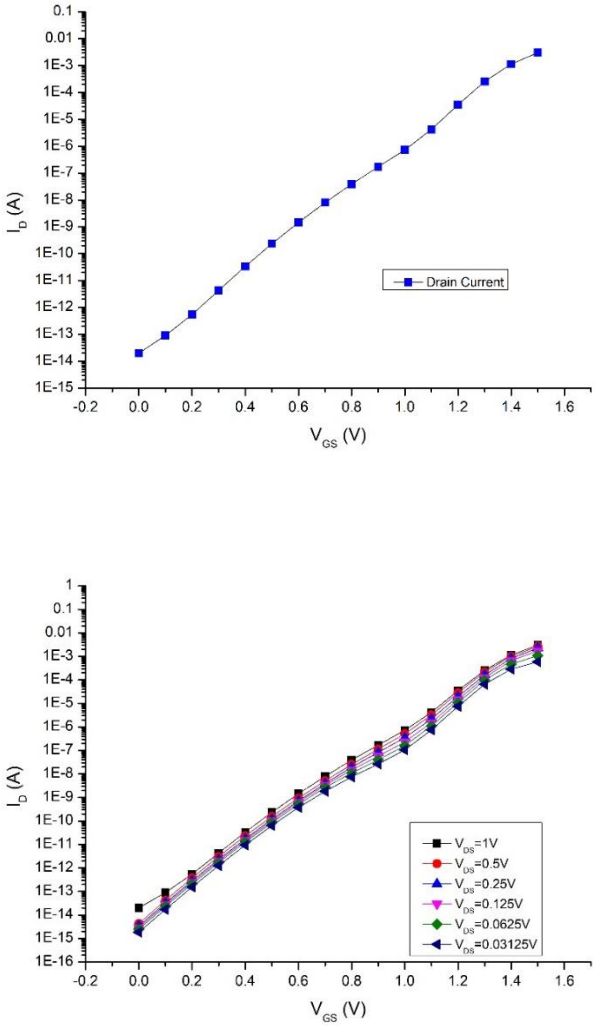


Fig.5.3 Asymmetric double gate P-I-N TFET Transfer Curve (a)for V_{DS}=1V (b) for various values of V_{DS}

The suggested device has a very low OFF current in addition to a very low ON current. The apparatus also produces a very low Subthreshold slope.

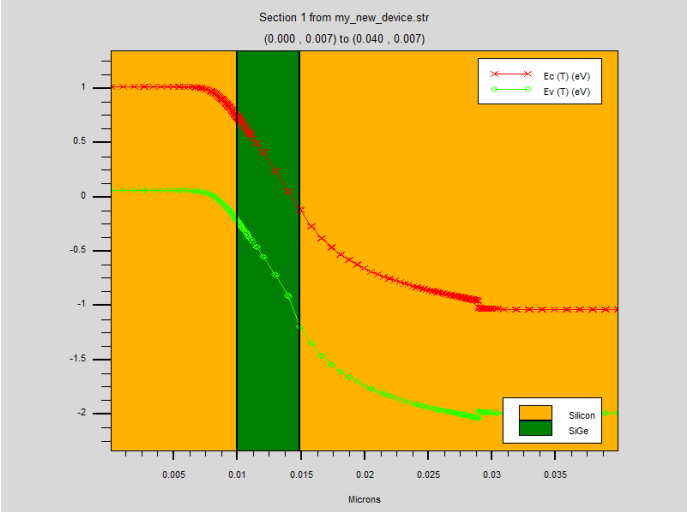


Fig.5.4 Valence Band (VB) and Conduction Band (CB) of the device at 300K

The suggested device's valence band (EC) and conduction band (ED) are shown in Fig. 5.4. The device's tunnelling connection is strengthened by the low band bandgap SiGe material. The Source (Si)-Pocket (SiGe) interface is where the most tunnelling current is produced. The electric field intensity in V/cm along a horizontal part of the proposed device is shown in Fig. 5.5. As is evident, the electric field is at its strongest along the x and y axes in the vicinity of the SiGe/SiO2 interface. By forming the tunnelling junction, the source pocket interface region plays a major role in increasing the device's ON current.

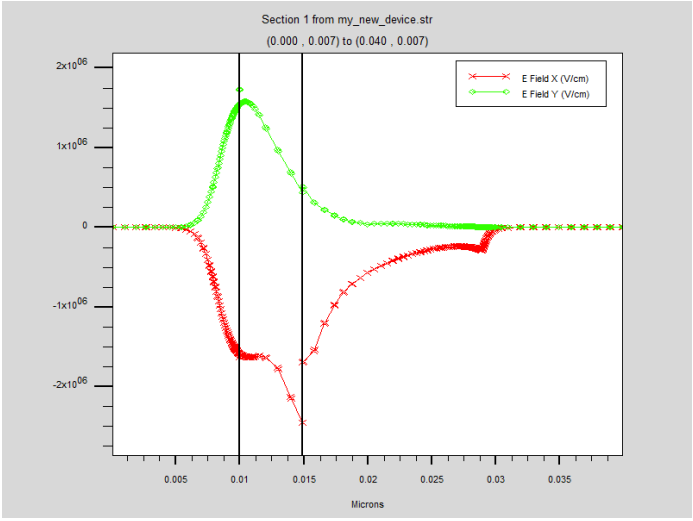


Fig. 5.5 The device's electric field intensity along the x and y axes

5.3 Summary

To regulate and improve the ON current, the suggested device uses a dual-gate TFET design. In order to achieve even higher ON current and a lower Sub-threshold slope for steeper and

faster switching, the SiGe pocket next to the silicon source end enhances lateral tunnelling even more. High VGS control over the drain current is made possible by the high-k gate oxide material close to the source region and the asymmetric source overlap created by the front and back gates. This is a prototype n-channel device. We may also develop the p-channel modified dual gate TFET using the same methodology, structure, and dimensions. Lastly, to replace MOSFET in ultra-low-power applications, a combination of n and p channel TFETs of the suggested types can be combined to build the CMOS compatible CTFET structure.

CHAPTER 6

Applications of the JL TFETs: Implementation of Transmission Gate & 2:1 MUX

As seen in Fig.6.1, a transmission gate (TG) is made up of a single nMOS and a single pMOS transistor connected in parallel. When a circuit employs a single MOS switch, it can pass a "0" signal with full power but not a "1" signal. On the other hand, if a pMOS device is utilised alone, it is limited to transmitting a powerful '1' signal. Therefore, the ideal answer is a transmission gate that consists of both of them in parallel. It serves as the ideal switch to pass both a strong "0" and a strong "1" with the same degree of clarity[6]. The transmission gate's truth table is shown in Table-6.1.

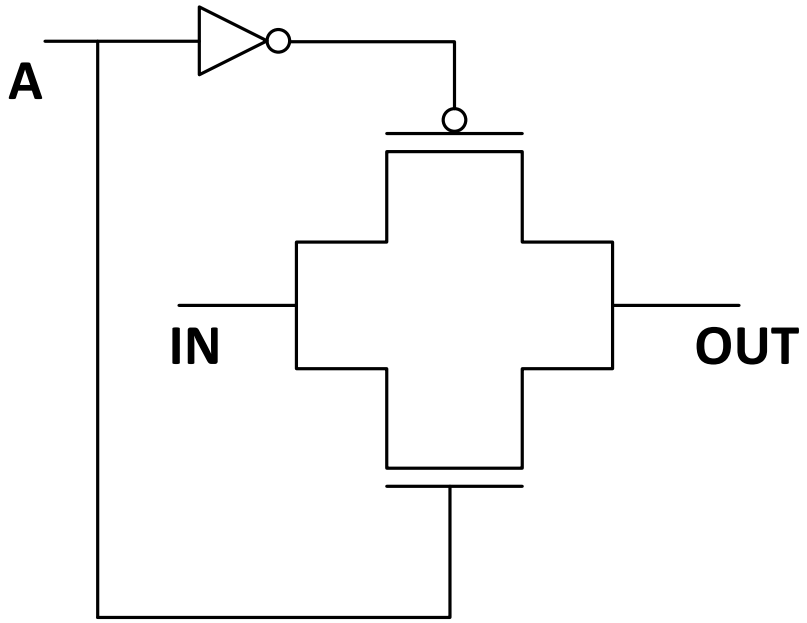


Fig.6.1 Conventional Transmission Gate with p & n MOS

According to the literature, nMOS and pMOS devices are typically used to implement the TG [65]–[74] Pass transistors likewise adhere to the same pattern [75]–[83]. In this chapter, modified single and double gate, n and p channel junction less TFETs with a p+ pocket close to the source end are used to implement TG. The construction and manufacturing processes of the single gate modified TFETs with SOI are shown in the following section. Subsequently, the advantages and usage of double gate TFET are illustrated. Ultimately, a comparative analysis of the two structures and a tabulation of the results finishes off the chapter.

Table 6.1 Transmission Gate Truth Table

A	IN	OUT
1	1	1
1	0	0
0	X	Z

6.1 Structure & Geometry of n-JL SG TFET

Fig. 6.2 shows the suggested n-channel single gate junction less TFET structure. The device is modelled at the 20nm technology node using the Cogenda Visual TCAD tool. The device contains a heavily doped P+ SiGe pocket of 5 nm near the source end of the channel, and it has a modified junction-less construction similar to a TFET[28], [45], [55]. The function of the highly doped P+ pocket is to increase the I_{ON} and I_{ON}/I_{OFF} ratio[20], [84], [85]. With p and n type gaussian doping of 1e+20 /cm^3, respectively, the source and drain have a thickness of 10 nm. Very little doped n type Si and the pocket produce the 20 nm channel. Platinum (Pt) is utilised as the gate metal because of its high work function value, which allows for better control over the conduction of the channel. To lower gate leakage and increase gate capacitance, a 1 nm-thick high k dielectric of HfO_2 is employed as the gate dielectric. Table 6.2 lists all of the device's dimensions in detail.

Table 6.2: Dimension Matrix for n-JL SG TFET

Parameters of the Device	Labels Used	Values and Dimensions
Channel Length	L_{CH}	20nm
Length of Source & Drain	L_S & L_D	10nm
Height of Source & Drain	H_S & H_D	5 nm
Length of the SiGe Pocket	L_{POC}	5 nm
Height of the SiGe Pocket	H_{POC}	5 nm
Source & Drain Doping	N_S & N_D	1e+20 /cm^3
Channel Doping	N_{CH}	1e+16 /cm^3
Gate Length	L_G	20nm
Gate Oxide Thickness	t_{OX}	1nm
Buried Oxide Thickness	t_{BOX}	1nm
Substrate Height	H_{Body}	4nm

The addition of a buried SiO2 layer, one nanometer below the channel on the substrate, is one significant change the proposed device makes over standard TFET devices. There are two benefits to using the buried oxide (BOX) layer. First, it removes the parasitic capacitance that develops between the source/drain areas and the substrate, resulting in devices with faster switching rates[49], [86], [87]. The next is a very steep subthreshold slope that results in very low subthreshold leakage [6], [33], [49], [50], [88].

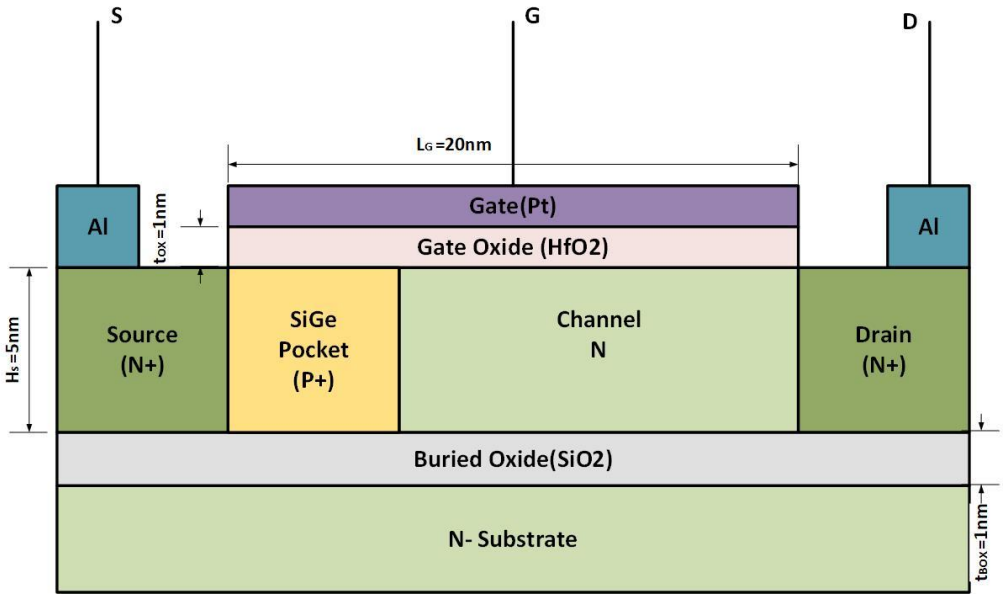


Fig. 6.2 n-JL SG TFET with P+ pocket & BOX Layer

The Cogenda Visual TCAD Tool's two-dimensional representation of the improved single gate n-channel JL TFET with buried oxide (BOX) and SiGe P+ Pocket is displayed in Fig. 6.3. The tool's GUI has been used to model the device. The substrate with an uneven n-type mild doping of 1e+16 /cm^3 is formed by the pink coloured region placed above the grey coloured body contact of aluminium (Al) metal. The silicon dioxide BOX layer above it is shown in dark purple. This displays the channel, drain, and source above. In the area farthest from the channel, the source and drain exhibit non-uniform gaussian doping, with a maximum value of 1e+20 /cm^3. At the source end of the channel, a heavily doped P+ SiGe pocket is placed, greatly increasing the ON current[20], [85]. High-k HfO_2 is used to make the gate oxide. Platinum (Pt) metal with a high work function is used to lay the gate over the oxide. As seen in Fig.6.3, the source and drain connections are made of Al.

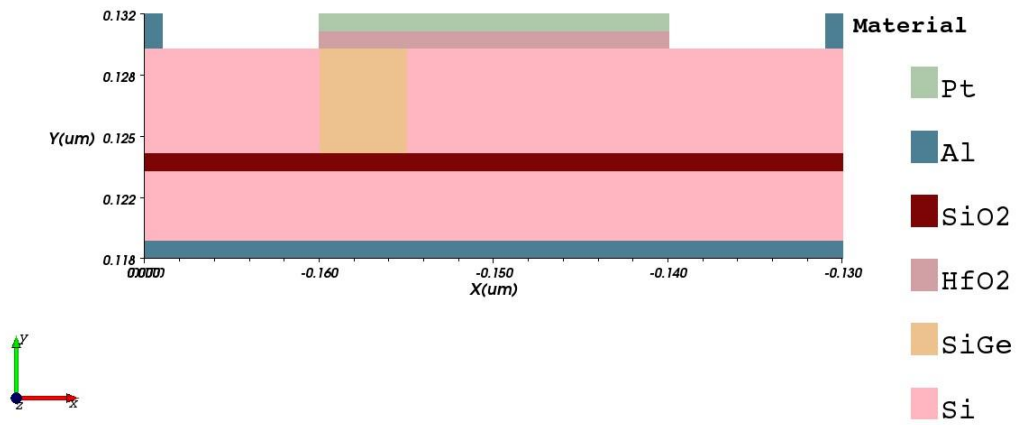


Fig.6.3 Tool view of n-JL SG TFET

6.2 Process for Fabrication of the n-JL SG TFET

Fig. 5.4 depicts the ideal manufacturing flow for fabricating the n channel SG JL TFET with P+ pocket and BOX layer [58], [59]. First, as shown in Fig. 6.4(a), a thin wafer of silicon, measuring 40 nm by 4 nm, that is weakly doped is used as the substrate or body. As seen in Fig. 6.4(b), an oxide vapour deposition layer of SiO_2 one nanometer thick is deposited over the narrow substrate wafer. The layer's thickness is appropriately regulated. Subsequently, the oxide surface is covered by intrinsic silicon vapour, as shown in Fig. 6.4(c), creating the intrinsic channel. A mask is placed 30 nm from the left edge of the device to establish the drain region. Ion implantation is used to form a highly doped (1e+20 /cm^3) n+ drain on the right edge, as shown in Fig. 6.4(d), to guarantee the proper depth. Using the same method, 30 nm of the device's right edge are covered to create the highly doped p+ type source, as shown in Fig. 6.4(e). Next, a high-k HfO_2 layer is deposited over the intrinsic channel by masking the source and drain, as shown in Fig. 6.4(f). Subsequent metallization, as shown in Fig. 6.4(g), forms the platinum metal gate. The drain and source connections are formed of aluminium metal. The finished design of the suggested gadget is shown in Fig. 6.4(h).

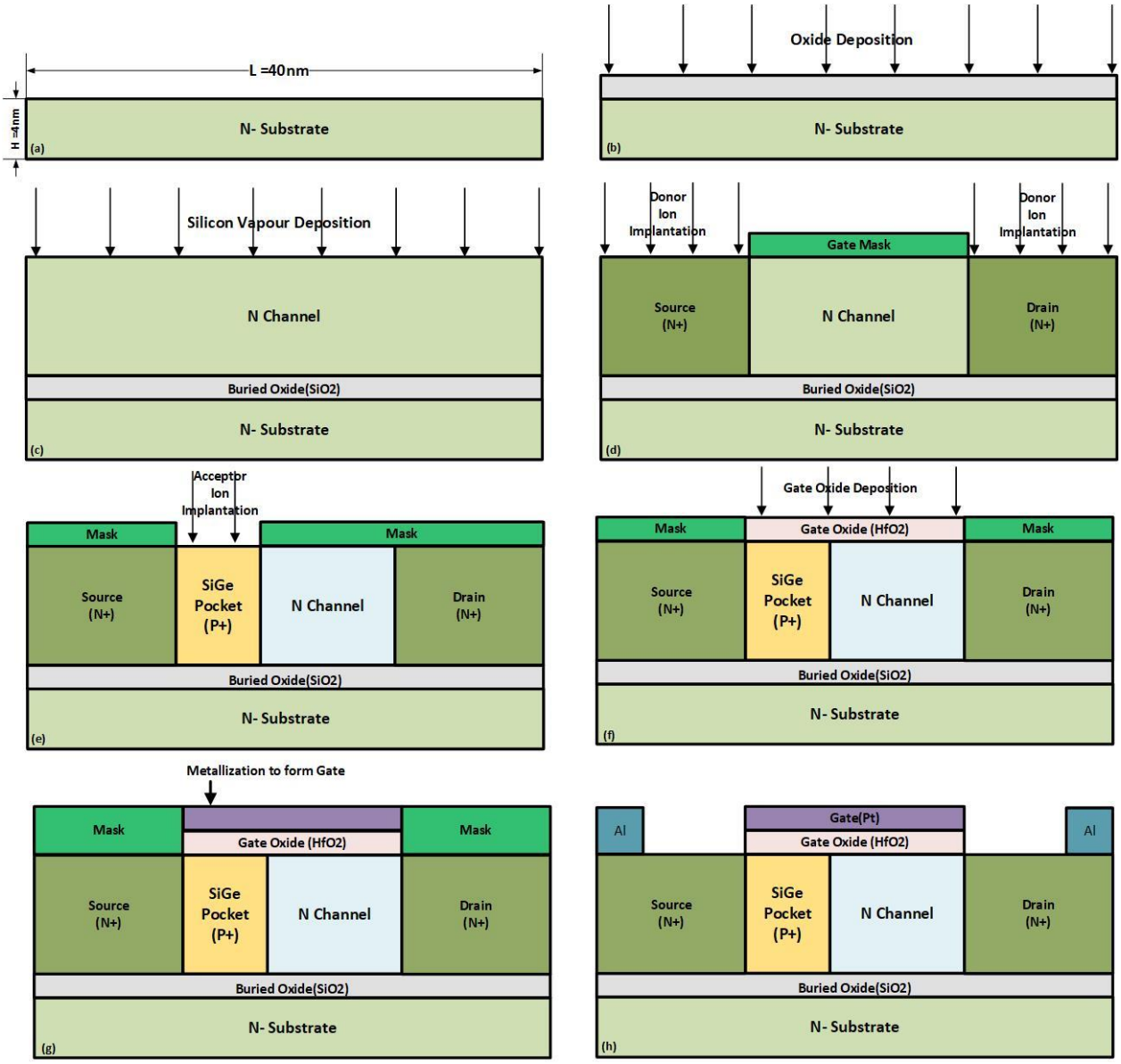


Fig. 6.4. (a)-(h) n-JL SG TFET wth BOX & P+ pocket process flow

6.3 Geometry & structure p-JL SG TFET

The modified p-channel single gate JL TFET with a N+ SiGe pocket close to the source end of the channel and a buried oxide layer covering the substrate is shown in Fig. 6.5. It is made using the same procedures as shown in Fig. 6.4(a)–(h). The structure of a p channel device is similar to that of a n channel device, with the exception that the source, drain, and pocket are all p+.

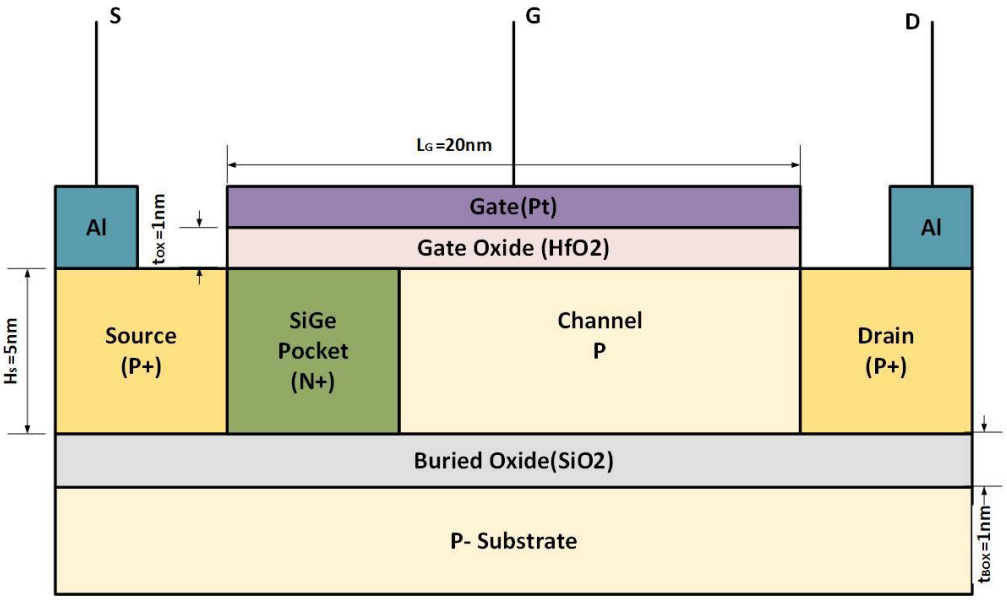
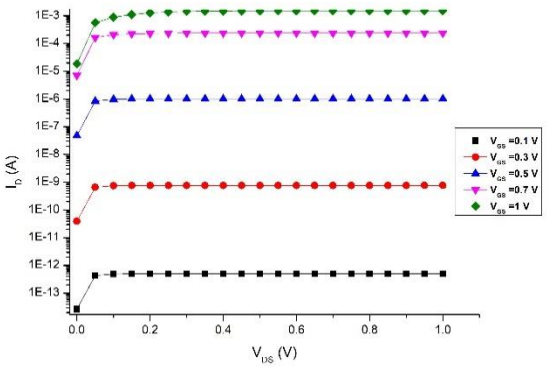


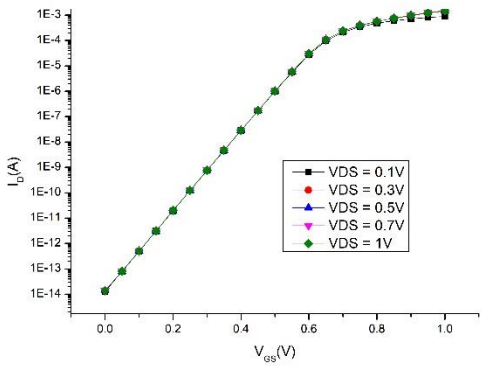
Fig. 6.5 p-JL SG TFET with N+ pocket & BOX Layer

6.4 Characteristic graphs for n & p SG TFETs with BOX layer

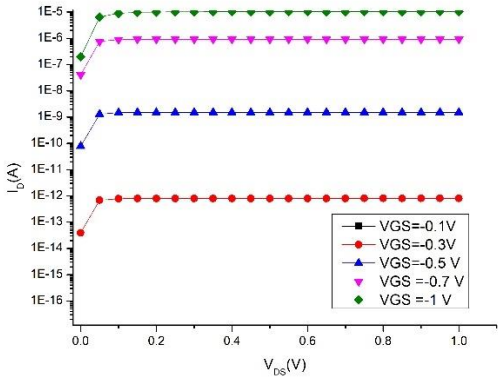
The characteristic graphs of the suggested single gate n and p channel devices are shown in Fig. 6.6. The qualities of an essentially perfect voltage-dependent current source are clearly illustrated by the output or drain characteristics, Figs. 6.6(a) and 6.6(c), where the drain current ID depends solely on the gate to source voltage VGS after a certain threshold and not on the drain to source voltage VDS. The above statement is further supported by the Transfer characteristics of the devices shown in Figs. 6.6(b) and 6.6(d), where the curve shows that changes in VDS have no effect on drain current and that VGS values are the only factors that determine it.



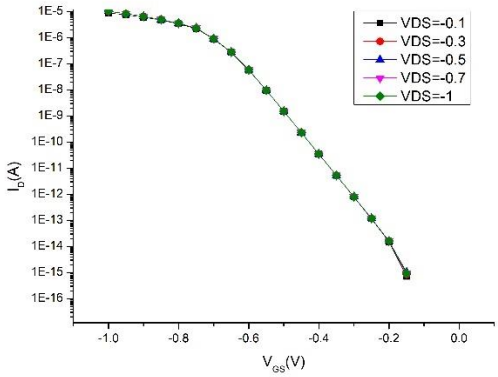
(a) Output graph of n SG JL TFET



(b) Transfer graph of n SG JL TFET



(c) Output graph of p SG JL TFET



(d) Transfer graph of p SG JL TFET

Fig. 6.6(a)-(d) Output and Transfer Characteristic curves of the n & p SG JL TFETs with BOX

6.5 Comparing the performance of the SG JL TFET to the traditional MOSFET

Comparing the suggested SG JL TFETs to traditional MOS devices, many metrics are examined, including SS, DIBL, ION, IOFF, and ION/IOFF ratio. Table 6.3, which is shown below, tabulates the detailed comparison.

Table 6.3: Table of Comparison for SG JL TFET and MOSFET

Parameters of the Device	SG JL TFET	MOSFET[89], [90]
I_{ON} (A)	0.00152	0.0026
I_{OFF} (A)	1.39E-14	2.59E-8
I_{ON}/I_{OFF}	1.09E+11	1.0E+6
SS (mV/dec)	62.5	63
DIBL (mV/V)	22.2	104

6.6 Construction of Transmission Gate (TG) with n & p JL SG TFETs

As shown in Fig. 6.7, a TG or pass transistor logic is created using the n and p channel single gate JL TFETs. A popular VLSI circuit called TG is utilised to pass both high and low signals with strong passing and minimal decay. However, up until now, the implementation of the same employing n and p channel MOSFETs has been the only focus of the literature review. For the first time, the TG is implemented with JL TFETs in this chapter. It is made up of a p JL TFET and a n JL TFET placed atop the same BOX layer and on the same n-substrate. Oxide spacers separate the n and p channel devices electrically from one another. The IN (input) terminal is formed by connecting the drain of the n JL SG TFET with the source of the p JL SG TFET. The

OUT (output) terminal is formed by the drain and source of the p and n channel devices, respectively, coupled together. The n channel device's gate receives the control input in true form, while the p channel device receives it in complement form. A separate inverter is employed to enhance the control signal.

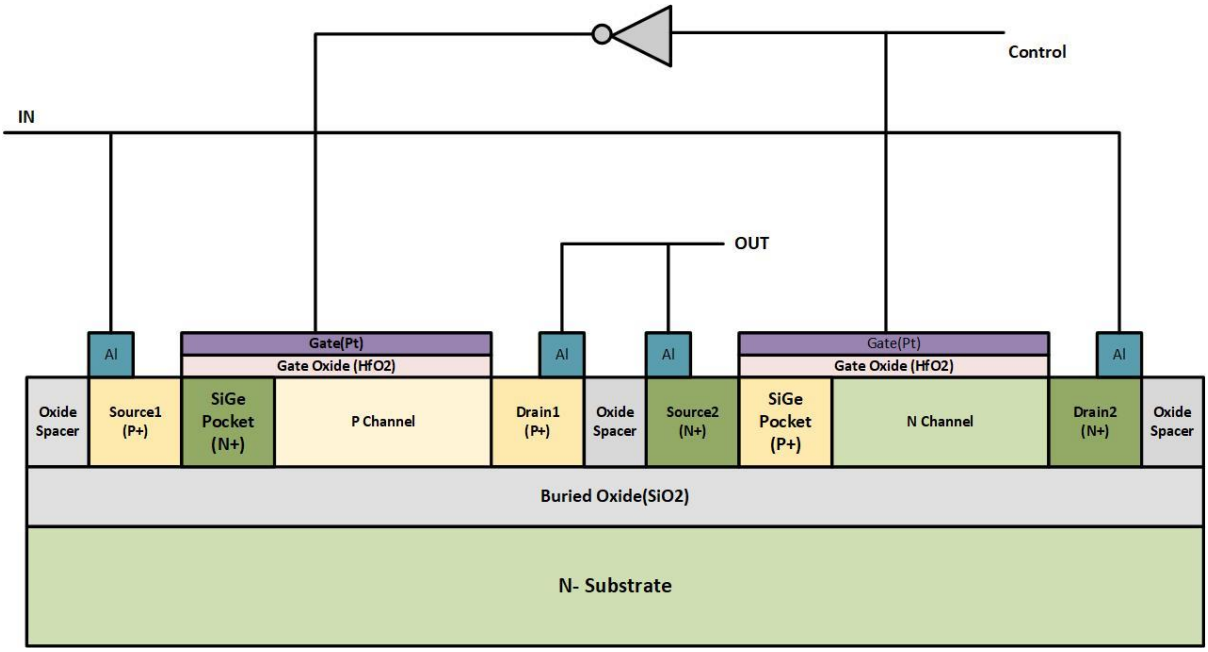


Fig.6.7 Structure of TG with n & p JL SG TFETs

6.7 VTC of the TG constructed with n & p JL SG TFETs

Figure 6.8 shows the plot of the output voltage V_{OUT} against the input voltage V_{IN}, or the voltage transfer characteristic of the transmission gate implement utilising the modified JL TFETs for the single gate n and p channels. The transmission gate turns transparent and only allows the input signal to reach the output when the control signal is high, which is why it displays the curve when the control signal is high. The Transmission gate becomes opaque to the input signal when the control signal is low. When the control is set to high, as seen in Fig. 6.8, the Transmission Gate's output voltage follows the input signal. The input translates to a low voltage at the output up to about 0.53V, which is the low threshold. The device faithfully delivers the high voltage to the output as soon as the threshold is crossed.

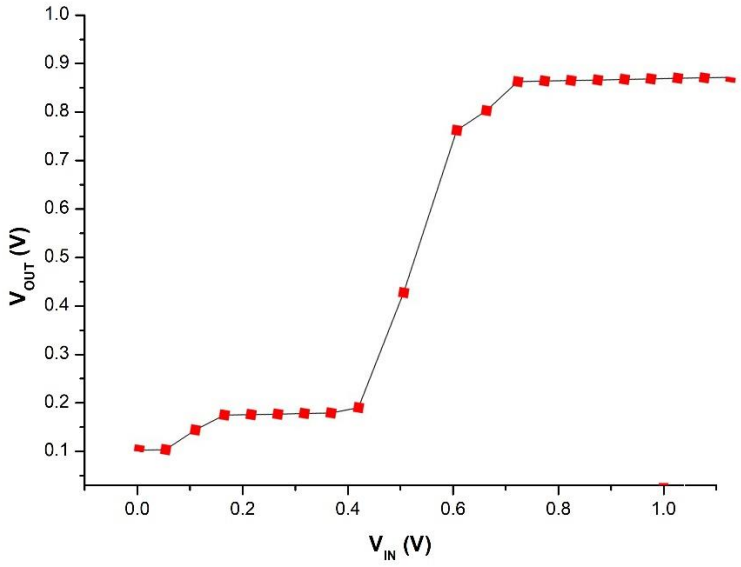


Fig.6.8 VTC of the TG constructed with n & p JL SG TFETs

6.8 Geometry & Dimensions of n-JL DG TFETs

Fig. 6.9 shows the suggested n channel double gate JL TFET structure with p+ SiGe pocket. The Cogenda Visual TCAD tool at the 20nm technology node is used to model the device. With N+ type Gaussian doping of $1x10^{20}$ /cm^3, the source and drain have a 10 nm size. N type silicon that has been slightly doped is used to construct the 20 nm channel. To boost the I_{ON}/I_{OFF} ratio and ON current, a heavily doped P+ SiGe pocket is placed nearer the source end of the channel. Platinum (Pt) is utilised as a gate metal because of its high work function value, which allows for improved channel conduction control. To lower gate leakage and increase gate capacitance, a 1 nm-thick high k dielectric of HfO_2 is employed as the gate dielectric. Table-6.4 lists all of the device's dimensions in detail.

Table 6.4 Dimension Matrix of n-JL DG TFET

Parameters of the Device	Labels Used	Values and Dimensions
Channel Length	L_{CH}	20nm
Length of Source & Drain	L_S & L_D	10nm
Height of Source & Drain	H_S & H_D	5 nm
Length of the SiGe Pocket	L_{POC}	5 nm
Height of the SiGe Pocket	H_{POC}	5 nm
Source & Drain Doping	N_S & N_D	1e+20 /cm^3
Length of Front & Back Gate	L_G	20nm
Thickness of Front & Back Gate Oxide	t_{OX}	1nm

The proposed device incorporates double gates, which is a significant change over traditional JL TFET devices. As illustrated in Fig. 6.9, there is a front Pt gate at the top and a back Pt gate at the bottom, both of which are insulated from the weakly doped channel by high-k HfO2 oxide material. There are two benefits to using the twin gate structure. First off, it solidifies the device's role as a voltage-controlled current generator and greatly improves the gates' control over the channel conduction. Additionally, the dual gate creates lateral tunnel current and transverse tunnelling, which greatly increases the ON current[20], [28], [39], [91]–[93].

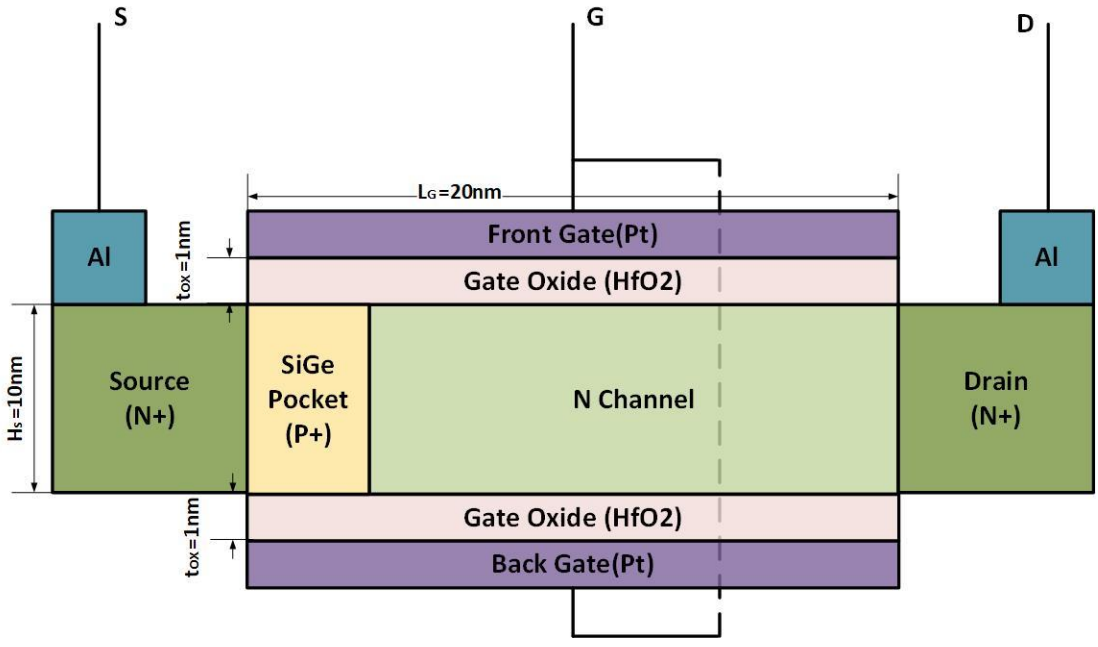


Fig. 6.9 n-JL DG TFET with P+ Pocket

The Cogenda Visual TCAD Tool's two-dimensional representation of the n channel double gate JL TFET with SiGe P+ Pocket is displayed in Figure 6.10. The tool's GUI has been used to model the device. The gadget is made up of a pink-colored, lightly doped P type Si bar, as seen in the figure. The N+ source region is strongly doped using N type doping up to 10 nm on the left, while the N+ drain region is likewise heavily doped using N type doping on the right. Its core is made up of a 20 nm-long, extremely mildly doped channel. A P+ SiGe pocket can be seen towards the source end of the channel; it is dark yellow in hue. The device, depicted in the image using light green hue, features front and back gates built of Pt metal at the top and bottom of the channel, respectively. High-k HfO_2, a dark pink substance, is used to isolate the metal gates from the intrinsic channel. As seen in Fig. 6.10, the source and drain connections are composed of Al metal.

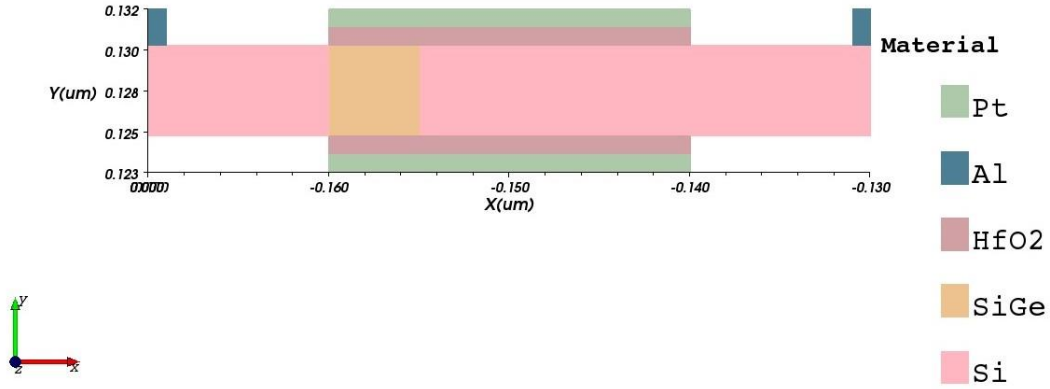


Fig.6.10 Tool view of n-JL DG TFET with P+ Pocket

6.9 Process for Fabrication of the n-JL DG TFET

Fig. 6.11(a)–(f) depicts the process flow for fabricating the n channel double gate JL TFET with P+ SiGe pocket[58], [59]. First, a 40 nm by 4 nm thin silicon wafer that has been very lightly doped is used, as shown in Fig 6.11(a). In order to create the drain region on the thin wafer, a mask is placed on top and bottom 30 nm from the left side of the device. Ion implantation is used to construct a highly doped (1e+20 /cm3) n+ drain on the right edge, as shown in Fig. 6.11(b), to guarantee the proper depth. Using the same method, the P+ SiGe pocket, shown in Fig. 6.11(c), and the highly doped n+ type source are created by masking 30 nm of the device from the right edge. The front and rear gate oxide are next formed by masking the drain and source to deposit a high-k HfO_2 layer above and below the channel, as shown in Fig. 6.11(d). Following metallization, the front and back gates made of platinum are formed

(Fig. 6.11(e)). Al metal is used to make the source and drain connections. Figure 6.11(f) shows the completed design of the suggested device.

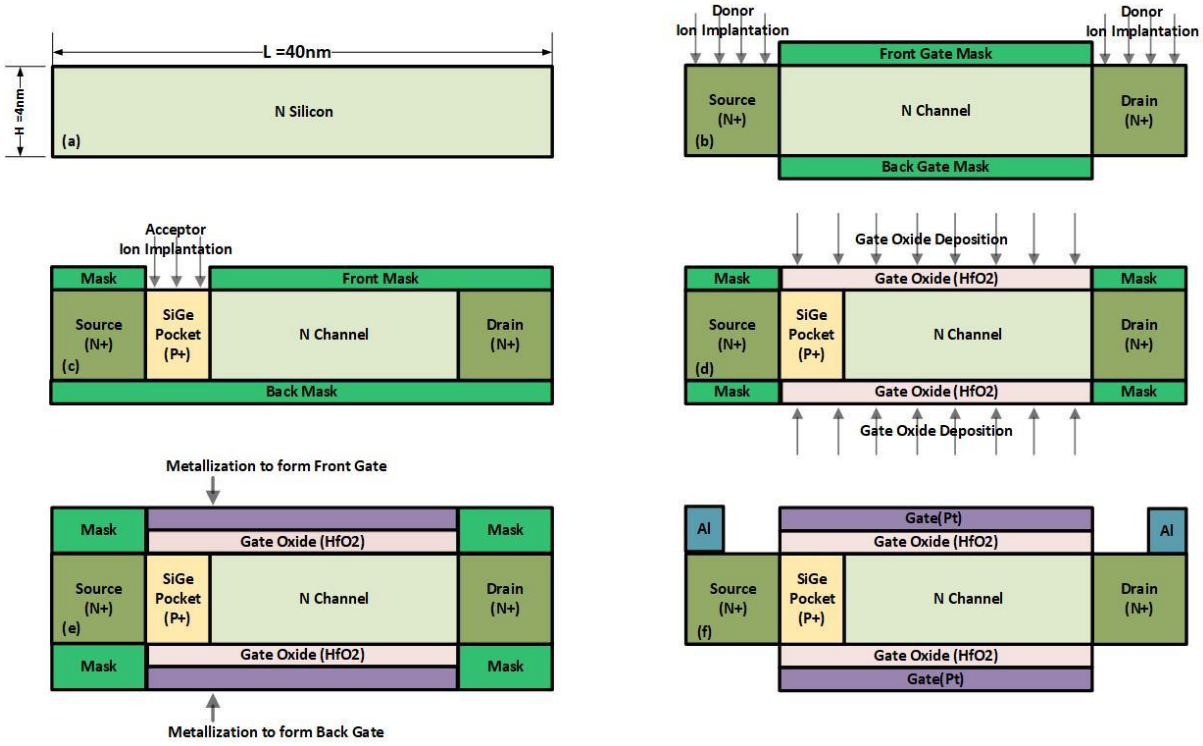


Fig. 6.11. (a)-(f) Fabrication flow of n-JL DG TFET with P+ SiGe pocket

6.10 Geometry and Measurements of p-JL DG TFET

The p-channel double gate JL TFET is shown in Fig. 6.12, with the SiGe P+ pocket close to the channel's source end and the front and back gates located at the top and bottom, respectively. Similar procedures are followed in its fabrication, as shown in Fig. 6.11(a)–(f). The structure of the p channel device is similar to that of its n counterpart, with the exception of the opposite kind of doping.

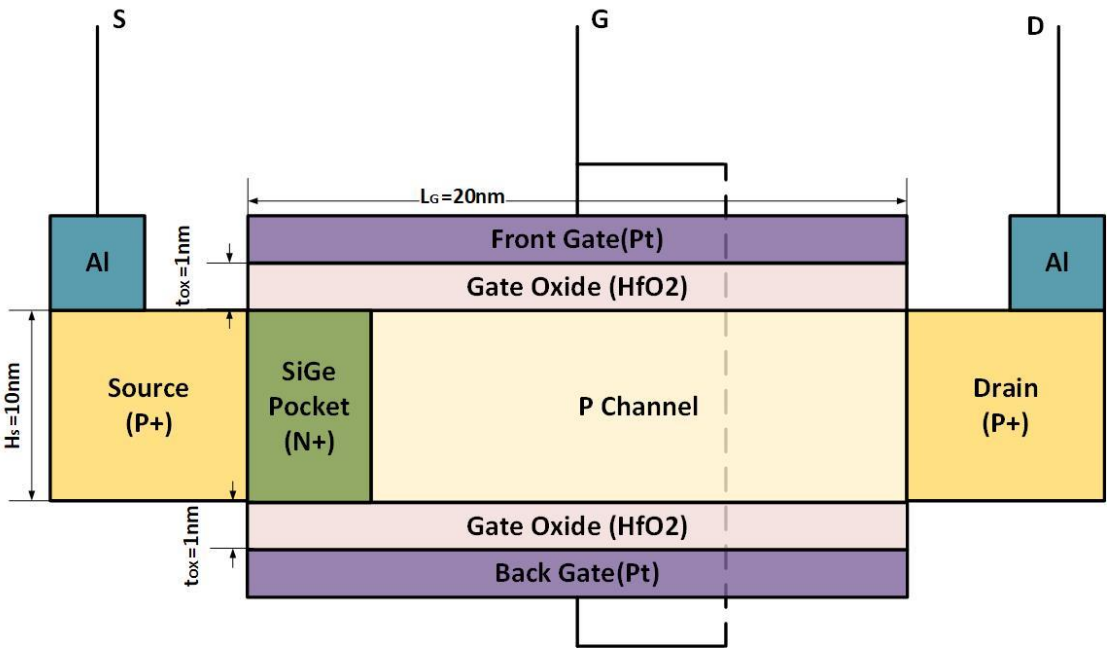
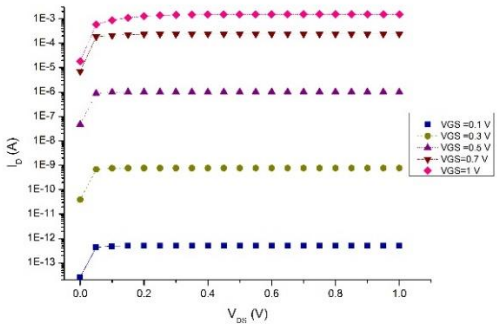


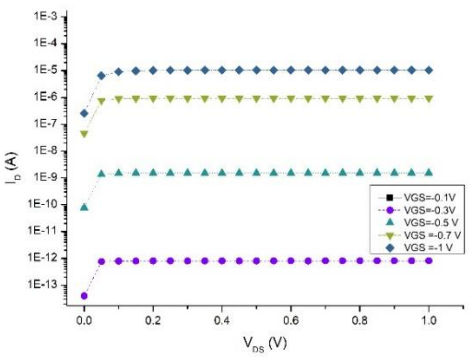
Fig. 6.12 p-JL TFET with SiGe N+ Pocket

6.11 Double gate n & p JL TFET characteristic curves

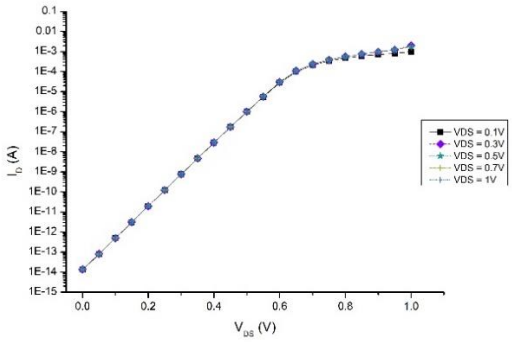
The characteristic curves of the suggested double gate n and p channel JL TFETs are shown in Fig. 6.13. (a)–(d). The attributes of an essentially perfect voltage-dependent current source are clearly illustrated by the output or drain characteristics, Figs. 6.13(a) and 6.13(b), where the drain current ID depends solely on the gate to source voltage VGS after a certain threshold and not on the drain to source voltage VDS. The above argument is further supported by the transfer characteristics of the devices shown in Figs. 6.13(c) and 6.13(d), where the curve clearly shows that changes in VDS have no effect on drain current and that VGS values are the only factors that determine it.



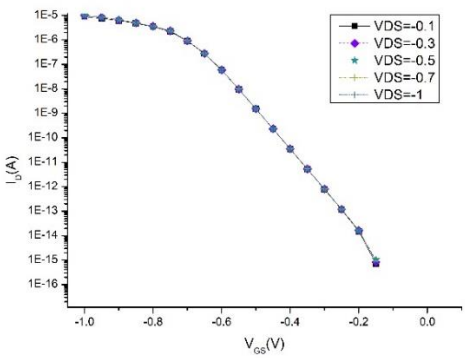
(a)Output Curves of n JL DG TFET



(b) Output Curves of p JL DG TFET



(c)Transfer Curves of n JL DG TFET



(d) Transfer Curves of p JL DG TFET

Fig. 6.13 Output & Transfer Curves of the n and p JL DG TFETs

6.12 Comparing the performance of DG JL TFET & SG JL TFET

Comparing the suggested DG JL TFETs to SG JL TFET devices, many metrics are examined, including SS, DIBL, ION/IOFF ratio, and IOFF and ION. Table 6.5, which is shown below, tabulates the detailed comparison.

Table 6.5: Table of Comparison for DG JL TFET and SG JL TFET

Parameters of the Device	SG JL TFET	DG JL TFET
I_{ON} (A)	0.00152	0.00863
I_{OFF} (A)	1.39E-14	1.27E-14
I_{ON}/I_{OFF}	1.09E+11	1.27E+11
SS (mV/dec)	62.5	61.4
DIBL (mV/V)	22.2	26.3

6.13 Transmission Gate (TG) Constructed with n & p JL DG TFETs

As shown in Fig. 6.14, a TG or pass transistor logic is created using the n and p channel DG TFETs. A popular VLSI circuit called TG is utilised to pass both high and low signals with strong passing and minimal decay. However, up until now, the implementation of the same employing n and p channel MOSFETs has been the only focus of the literature review. For the first time, double gate TFETs are used to implement the TG in this research. It is made up of a p channel and a n channel DG TFET. Oxide spacers composed of SiO_2 provide an electrical isolation between the n and p channel DG TFETs. The IN (input) terminal is formed by

connecting the drain of the n DG TFET with the source of the p DG TFET. The OUT (output) terminal is made up of the drain and source of the p and n channel devices, respectively, coupled together. The n channel device's gate receives the control input in true form, while the p channel device receives it in complement form. A separate inverter is employed to enhance the control signal.

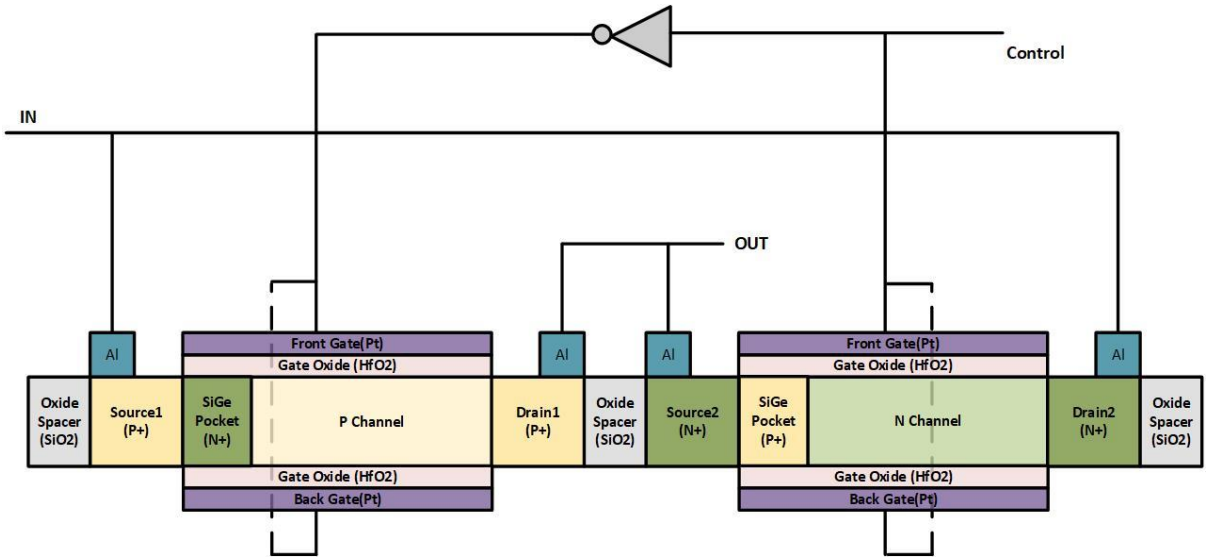


Fig.6.14 Transmission Gate (TG) Constructed with n & p JL DG TFETs

6.14 VTC of TG constructed with n& p JL DG TFETs

Using double gate n and p channel JL TFETs, the voltage transfer characteristic of the gearbox gate implement is plotted against the input voltage V_{IN} as shown in Fig. 6.15. The transmission gate turns transparent and only allows the input signal to reach the output when the control signal is high, which is why it displays the curve when the control signal is high. The Transmission gate becomes opaque to the input signal when the control signal is low. When the control is set to high, as Fig.6.15 plainly illustrates, the Transmission Gate's output voltage follows the input signal. The input translates to a low voltage at the output up to about 0.39V, which is the low threshold. The device faithfully delivers the high voltage to the output as soon as the threshold is crossed.

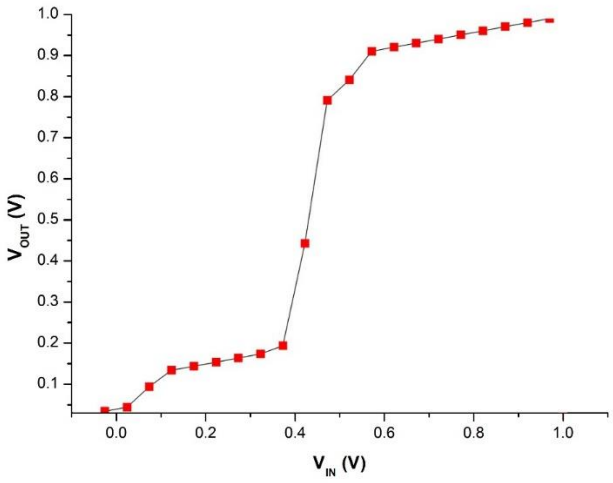


Fig.6.15 VTC of TG constructed with n& p JL DG TFETs

6.15 Comparative Study of TG with SG JL TFETs & DG JL TFETs

In this chapter, single and double gate junctionless tunnel field effect transistors with opposing & high dopings of SiGe source pockets have been used to develop TG, or the pass transistor logic. Since a TG is being built with TFETs for the first time in literature, it is a revolutionary approach for low power CMOS compatible VLSI circuits. Both single and double gate JL TFET variations are used to implement the TGs; Table 6.6 provides an illustration of a comparative research for the same. Using Si wafer and the Cogenda Visual TCAD tool, both the SG and DG devices are manufactured on the 20nm technology node. The SG JL TFET is built using Silicon-on-Insulator (SOI) technology, which has two key benefits. Firstly, it removes parasitic capacitance that forms between the substrate and source/drain regions, resulting in devices with faster switching rates.[49], [86], [87]. The next is a very steep subthreshold slope that results in very low subthreshold leakage.[6], [33], [49], [50], [88]. Due to its high work function and high control over the TFET's ON state current, Pt metal is used in the fabrication of the gates in both devices.[20][85][84]. By combining the transverse counterpart of the lateral tunnelling current with the ON state current, the use of double gates for the DG JL TFET TG improves the control of the gates over the channel conduction [24], [32], [48], [94]. When using the double gate structure, the maximum ON state current by including a double gate approaches 1.52 mA, while when using a single gate device, it is roughly 0.9 mA. Additionally, Fig. 6.14 makes it evident that, in contrast to the single gate version of Fig. 6.7, the double gate JL TFET TG offers a significantly steeper VTC. In contrast to the single gate model, which switches at a voltage above 0.5 V, the double gate device

switches from low to high at a very low voltage of about 0.4 V. As a result, the double gate JL TFET based TG offers superior responsiveness overall and is far more appropriate for use in low power VLSI designs.

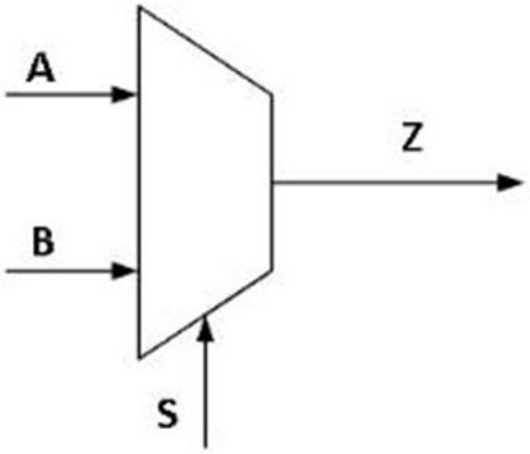
Table 6.6 Comparison Matrix of JL SG TFET & JL DG TFET based TGs

Parameters of the Device	SG TFET TG	DG TFET TG
Technology Node	20nm	20nm
Gates	1	2
Use of SOI	BOX Layer used	No
Gate Metal	Pt	Pt
Gate Oxide	HfO_2	HfO_2
Tunnelling Current	Lateral	Lateral & Transverse
I_{ONmax}	0.000972A	0.00152 A
Maximum V_{IN} to be translated as Low V_{OUT}	0.532V	0.393V

6.16 A Digital Multiplexer

Depending on control or select inputs, a digital multiplexer is a combo logic circuit with many data inputs and a single output[95]–[102]. $\log_2(N)$ selection lines are needed for N input lines, or n selection lines are needed for 2^n input lines, respectively. Many-to-one circuits, universal logic circuits, parallel-to-serial converters, and N-to-1 selectors are some other names for multiplexers.

Fig.6.16 illustrates the block diagram of 2:1 Multiplexer (MUX) along with its logic equation and truth table. A 2:1 multiplexer (MUX) is a digital logic device that selects one of two input signals and forwards the selected input to a single output line.



S	A	B	Z
0	0	0	0
	0	1	0
	1	0	1
	1	1	1
1	0	0	0
	0	1	1
	1	0	0
	1	1	1

Fig. 6.16 Block Diagram of 2:1 MUX, Logic Expression & Truth Table

6.17 Implementation of 2:1 Multiplexer (MUX) using n & p JL DG TFETs

This section describes the implementation of a 2:1 Multiplexer (MUX) for use in ultra-low power, nano size VLSI circuit applications employing n and p channel Modified Double Gate Tunnel Field Effect Transistors (TFETs). The schematics of the two transmission gates composed of double gate modified TFETs, which in turn include the schematics of a p channel modified TFET, a n channel modified TFET, and an inverter, which may be implemented using double gate TFETs themselves, make up the two-dimensional schematic of the 2:1 MUX with n and p channel modified double gate TFETs. Although the 2:1 MUX is already a well-known circuit for implementing many applications, it is built utilising MOS-based devices. Examples of these applications include lookup tables, universal logic components, and parallel to serial converters. The 2:1 MUX is implemented in this section utilising modified double gate TFETs, making it suitable for sub-micron and low power circuits. The successful implementation seen here will motivate researchers and businesses to investigate the unique characteristics of the modified double gate TFET in order to create power-efficient, nanoscale devices. This is one of the attempts to use double gate TFETs for purposes other than inverters in digital circuits. The precise structure of one of the transmission gates, which was used to build the 2:1 MUX seen in Fig. 6.18, is shown in Fig. 6.17. The input terminal of the device is formed by shorting

the drain contact of the n channel modified double gate TFET, called Drain2, to the source contact of the p channel modified double gate TFET, called Source1, in the transmission gate of Figure 6.17. The device's output terminal is formed by shorting the source contact of the n channel modified double gate TFET, known as Source2, and the drain contact of the p channel modified double gate TFET, known as Drain1. The gates of the n channel TFET in its true form and the p channel TFET in its inverted version are connected to the device's control terminal. Both TFETs are in cut-off and the device is turned off when the control voltage is low, meaning that no signal is transmitted from the input to the output. On the other hand, signal transmission occurs from the input to the output when the control voltage is a high signal, which also turns on the device and saturates both TFETs.

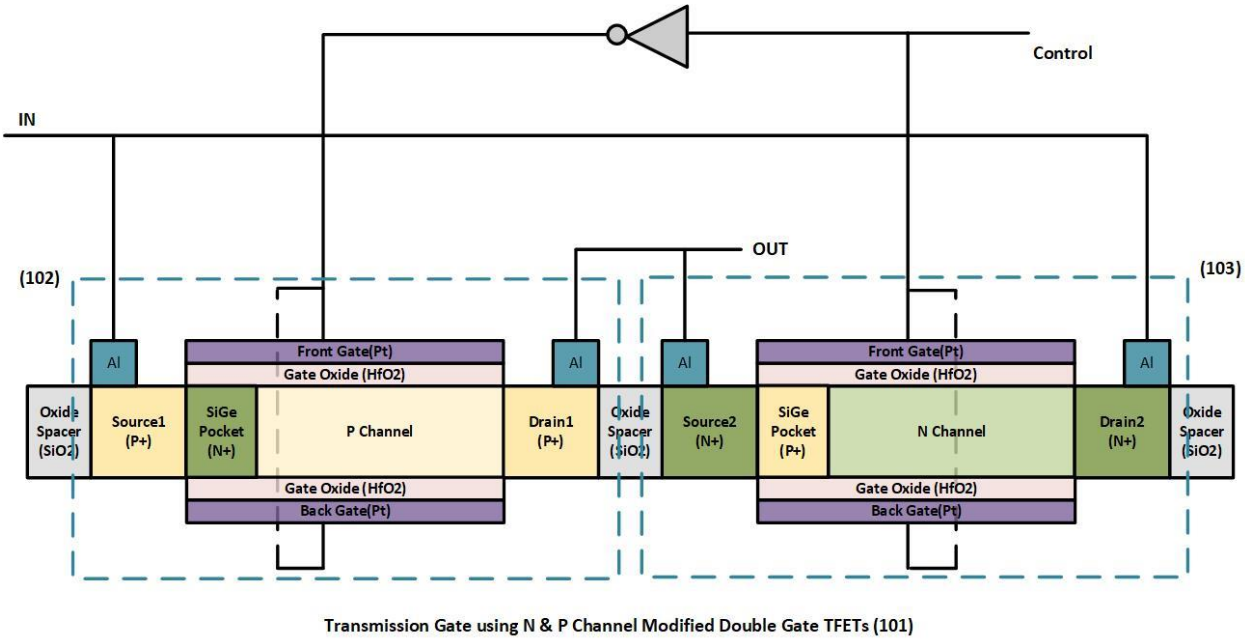
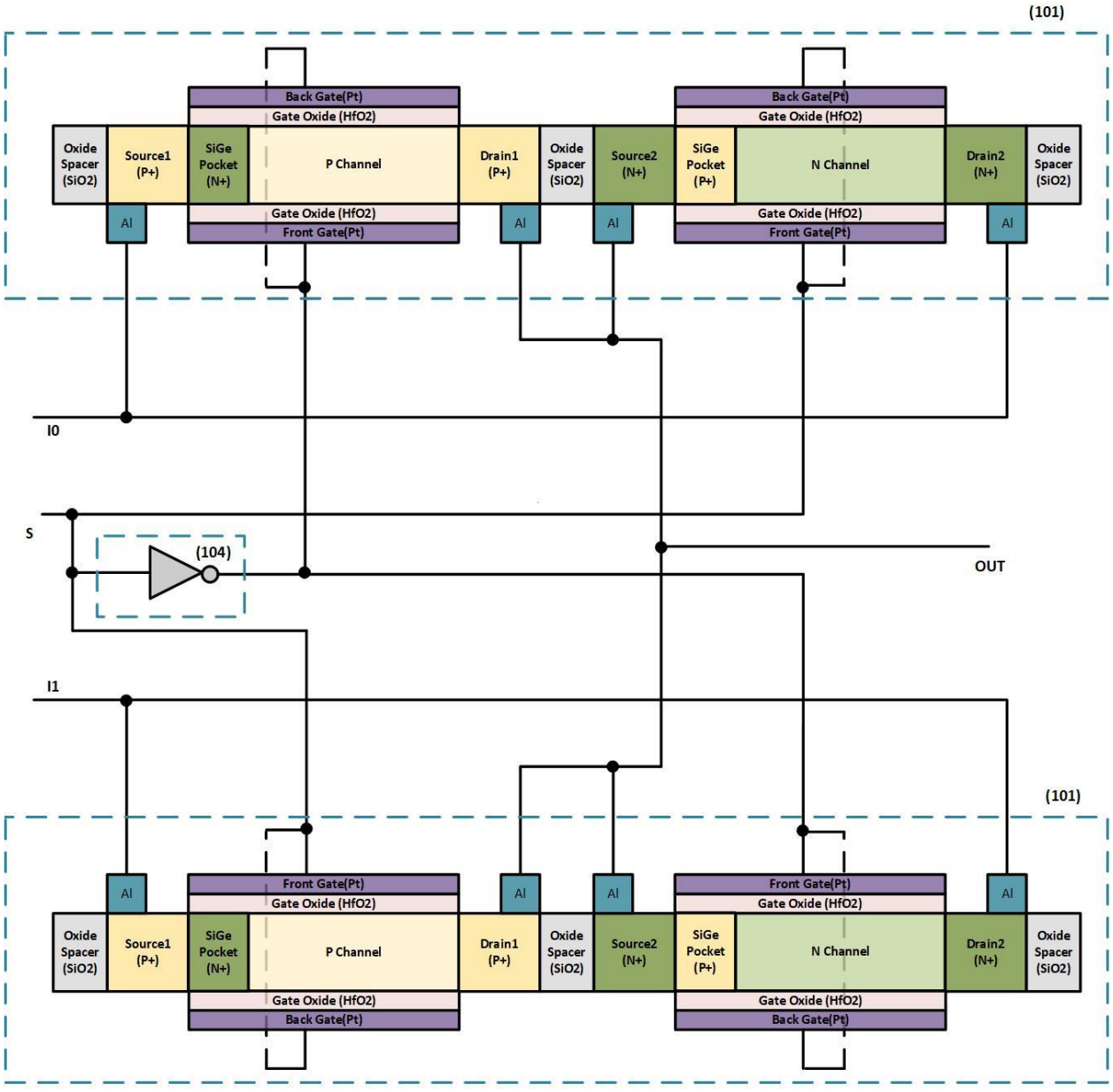


Fig.6.17 Transmission Gate with n & p JL DG TFETs

Lastly, the complete embodiment of our invention—a 2:1 MUX utilising Modified Double Gate TFETs—is shown in Fig. 6.18. As shown in Fig. 6.17, it is composed of two transmission gates made from modified double gate TFETs. The input terminals of the upper transmission gate get the input signal I0, while the input terminal of the tower transmission gate receives the input signal I1. The output signal of the MUX is created by shorting the outputs of the upper and lower transmission gates together. The gates of the bottom p channel TFET and the upper n channel TFET are connected to the 2:1 MUX's Select Line, S, in its actual form. Likewise, the gates of the bottom n channel and upper p channel TFETs are connected to the inverted form of the Select Line, S. The input I0 is routed to the output when the voltage at the select

line, S, drops. On the other hand, the input I1 is directed towards the output when the voltage at the select line, S, increases. Furthermore, larger multiplexers and other digital circuits can be designed using the same concept. The particular structures that are described here are only examples of a single application of the invention; they do not restrict its application.



2:1 MUX using Modified Double Gate TFETs (100)

Fig6.18 2:1 MUX using n & p JL DG TFETs

6.18 Conclusions

This chapter explains in detail the structure and geometry of n-JL SG TFET and p-JL SG TFET, followed by its fabrication process. Then the characteristic plots of the devices are illustrated with additional description for relevance of inclusion of the buried oxide layer. Then the device is compared with traditional MOS based structures and the same is tabulated. Next a dual gate structure of the single gate version of the device is developed and termed as JL DG TFET. Comparison of both JL SG TFET and JL DG TFET is drawn, and dual gate device is found to be more efficient as compared to the single gate counterpart. As an application for the developed device a well-established MOS circuit, namely transmission gate (TG) is constructed using n & p-JL SG TFETs, as well as using n & p-JL DG TFETs. Followed by the comparative analysis of both the TGs. The chapter concludes with the conversion of another established MOS circuit to its JL SG TFET counterpart, namely a 2:1 MUX. The construction of 2:1 MUX using TFET is a very novel approach which has not been done in recent years. As MUX is an integral part of LUT/CLB of an FPGA board, a MUX circuit made using TFET rather than MOS can lead to the development of FPGA technology for low power domain and can prove to be very much helpful in the advent ultra-low power VLSI circuit prototype development.

CHAPTER 7

CONCLUSION & FUTURE SCOPE

7.1 Conclusion

Our research began with motivation for finding a low power replacement for the already established CMOS circuits. The search led us to venture into the domain of Tunnel Field Effect Transistors (TFET) which is worthy contender as low power replacement of MOS as they are not limited by the thermal constraints of MOS. Their structural similarity with MOS makes them ideal for incorporating in already established CMOS circuits. But TFET has some inherent limitations, viz very low ON current & ambipolar current conduction. Our objective for the present research was to develop a modified version of the conventional TFET with structural, geometrical and material modifications which will be prone to the fundamental limitations of TFET. We developed a novel device termed Junction less Double Gate and Single Gate TFET, JL DG TFET and JL SG TFET. The n-JL DG TFET is developed and simulated for optimized responses, a P+ SiGe pocket is introduced in the device for enhanced conduction and double gate is utilized for enhanced control. Fourfold optimization with respect to metal contact, gate dielectric, mole fraction and temperature is done for the device to state the optimal values. The magnitude of I_{ON} to I_{OFF} ratio of the structure is much larger, of the order of 10^{11} when compared to 10^{6} for JL SGTFET,10^{7} for TDJLT and 10^{9} for SG SOI TFET for devices with alike dimensions. Thus, the proposed design illustrates approximately 10^{2} to 10^{5} order improvement in I_{ON} to I_{OFF} ratio with respect to the contemporary devices. The p channel counterpart of the device is also constructed using a similar process flow and optimized. Then an inverter circuit is successfully implemented using complementary TFET including both n and p channel devices. Finally the application perspective of the invented device verified fully by implementing two major circuits the Transmission Gate (TG) and the 2:1 Multiplexer Circuit (MUX) and both circuits are verified to give very efficient results in low power VLSI.

7.2 Future Scopes

In our future research we propose to implement

- The Analytical Model of the proposed JL SG TFET and JL DG TFET, implement it using MATLAB or Python script and verify the same with simulation results.
- Artificial Intelligence based model for optimizing our device parameters. Which can be applied after converting the Analytical model into relevant programs using MATLAB

or Python and using Machine Learning based trained models to obtain the best possible optimizations of each performance parameters of the device.

- The device in lower technology nodes (below 18nm) for improvement both DC parameters like I_{ON}, I_{ON}/I_{OFF}, SS & DIBL and analog parameters like transconductance(g_m), Cut-off frequency(f_T) & Gain-Bandwidth Product.

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LIST OF PUBLICATIONS

1. Design of tunnel FET architectures for low power application using improved Chimp optimizer algorithm
   Engineering with Computers, 2021 (SCIE & Scopus, IF=8.7)
   https://doi.org/10.1007/s00366-021-01530-4

2. Implementation of Low Power Inverter using $Si_{1-x}Ge_x$ Pocket N & P-Channel Junction-Less Double Gate TFET
   Silicon, 2022 (SCIE & Scopus, IF=3.4)
   https://doi.org/10.1007/s12633-021-01628-w

3. Design Transmission Gates Using Double-Gate Junction less TFETs
   Silicon, 2024 (SCIE & Scopus, IF=3.4)
   https://doi.org/10.1007/s12633-024-02927-8

Conference Papers

1. A novel junction less dual gate tunnel FET with SiGe pocket for low power applications
   Proceedings of 4th International Conference on Devices for Integrated Circuit, DevIC 2021
   doi: 10.1109/DevIC50843.2021.9455807

2. Analysis of modified P-I-N tunnel FET architecture for applications in low power domain
   Materials Today: Proceedings, 2022
   https://doi.org/10.1016/j.matpr.2022.09.449

Patent

1. **2:1 Multiplexer (MUX) using modified Double Gate Tunnel Field Effect Transistors (TFETs).**
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