DEVELOPMENT OF HIGH-K DIELECTRICS AS AN ALTERNATE GATE-OXIDE FOR LOGIC AND MEMORY DEVICES

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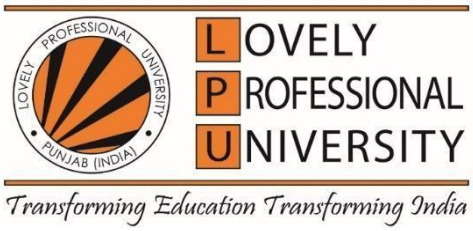

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2025

DECLARATION

I, hereby declared that the presented work in the thesis entitled "Development Of High-k Dielectrics As An Alternate Gate-Oxide For Logic And Memory Devices" in fulfillment of degree of **Doctor of Philosophy (Ph. D)** is outcome of research work carried out by me under the supervision of Dr. Reji Thomas , working as Professor and Assistant Dean, Head-Department of Research, Collaboration, Division of Research and Development, and Dr. Sachin Mishra, working as Professor in the School of Electronics and Electrical Engineering of Lovely Professional University, Punjab, India. In keeping with general practice of reporting scientific observations, due acknowledgements have been made whenever work described here has been based on findings of other investigator. This work has not been submitted in part or full to any other University or Institute for the award of any degree.

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CERTIFICATE

This is to certify that the work reported in the Ph. D. thesis entitled Development Of High-k Dielectrics As An Alternate Gate-Oxide For Logic And Memory Devices" submitted in fulfillment of the requirement for the award of degree of **Doctor of Philosophy (Ph.D.)** in the School of Electronics and Electrical Engineering, is a research work carried out by Urvashi Sharma, 11814489, is bonafide record of his/her original work carried out under my supervision and that no part of thesis has been submitted for any other degree, diploma or equivalent course.

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ABSTRACT

This research focuses on the development and characterization of high-k dielectric materials for integration with standard Si technology in logic and non-volatile memory devices. In the cased of logic devices, the study explores various compositions, including $Hf_{0.2}Zr_{0.6}(Ta, Dy)_{0.2}O_2$, $Hf_{0.4}Zr_{0.4}(Ta, Dy)_{0.2}O_2$, and $Hf_{0.6}Zr_{0.2}(Ta, Dy)_{0.2}O_2$, prepared through a solid-state reaction route for the optimization of the composition and pulsed laser deposition of the selected composition for the Metal-oxide -Semiconductor devices to check the logic applicability. In the case of bulk ceramics, the surface morphology analysis reveals well-packed grains without cracks or voids. The dielectric permittivity of the ceramics remains constant over wide temperature and frequency ranges. The conduction mechanism is attributed to the hopping mechanism through the traps, as confirmed by the AC conductivity (σ_{ac}) curve that fits with Jonscher's power law. These findings establish HfO_2 and ZrO_2 co-substituted with Dy and Ta as promising gate dielectric materials for logic devices if deposited in the thin film form on Si substrates. The ultra-thin films of $Hf_{0.6}Zr_{0.2}Dy_{0.1}Ta_{0.1}O_2$ show desirable properties for CMOS logic devices, including a high dielectric constant, low equivalent oxide thickness, and low leakage current density.

The study also investigates the properties $(Hf_x, Zr_{1-x})\ O_2$ ceramics where x =0.25, 0.5, 0.75 (HZO25, HZO50, and HZO75), synthesized at 1400 °C by the same solid-state route for the memory applications. The ceramics exhibit a single-phase structure with uniform surface morphology. The relative dielectric permittivity varies from 17 to 40, with HZO75 displaying the maximum. The ac conductivity of the HZO ceramics also followed Jonscher's power law, like the $Hf_xZr_{0.8-x}$ (Ta, Dy)$_{0.2}O_2$. Leakage current

densities are measured for different electric fields, and the lossy effect leads to unsaturated polarization-electric field (P-E) curves. The investigation also includes the deposition of films using Pulsed Laser Deposition. Furthermore, this study explores the microstructural and electrical characteristics of (Hf_x, Zr_{1-x}) O_2 films, specifically Pt/$Hf_{0.75}Zr_{0.25}O_2$/Pt/Si structures for the non-volatile memory devices. These films exhibited poor ferroelectric capabilities, however, demonstrated a low leakage current density and steady performance of resistive switching, suitable for non-volatile memory, Resistive RAM (RRAM). To enhance the ferroelectric properties, future examinations with lower thickness are recommended. The findings suggest switching behavior in HZO75 for ferroelectric devices with silicon-based system, opening possibilities for 3D integration and potential 3D NAND replacements.

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After investing five years in my doctoral thesis, I find myself on the cusp of a remarkable achievement, made possible through the unwavering support of numerous individuals. At the forefront of my gratitude stands Professor Reji Thomas, Lovely Professional University, my esteemed supervisor, whose guidance, and wealth of knowledge in semiconductor memory research have been instrumental in shaping my journey. Financial support from the Science and Engineering Research Board, Government of India, under the project "CMOS compatible Ferroelectric Tunnel Junction for Universal Memory" via Grant No. CRG/2018/003539, has been crucial in facilitating the successful execution of my research goals.

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List of Acronym

PLD: Pulsed Laser Deposition

SRAM: Static-Random-Access-Memory

CMOS: Complementary Metal-Oxide-Semiconductor

DRAM: Dynamic-Random-Access Memory

RAM: Random Access Memory

NVRAM: Non-Volatile RAM

MOSFET: Metal Oxide Semiconductor Field Effect Transistor

EOT: Equivalent Oxide Thickness

MOS: Metal-Oxide-Semiconductor

MNOS: Metal/Nitride/Oxide/Silicon

MONOS: Metal/Oxide/Nitride/Oxide/Silicon

SONOS: Silicon/Oxide/Nitride/Oxide/Silicon

ONO: Oxide/Nitride/Oxide

ALD: Atomic Layer Deposition

MIS: Metal-Insulator-Semiconductor

MOCVD: Metalorganic Chemical Vapor Deposition

TEM: Transmission Electron Microscopy

SOI: Silicon-On-Insulator

TCAD: Technology Computer-Aided Design

IoE: Internet Of Everything

AI: Artificial Intelligence

ML: Machine Learning

IoT: Internet of Things

MEMS: Microelectromechanical Systems

F-RAM: Ferroelectric RAM

MRAM: Magnetic RAM

RRAM: Resistive RAM

MDRAM: Mobile DRAM

SRAM: Static RAM

SDRAM: Synchronous DRAM

ROM: Read-Only Memory

BIOS: Basic Input/Output System

EPROM: Erasable Programmable ROM

EEPROM: Electrical Erasable Programmable ROM

UVPROM: Ultraviolet Programmable ROM

FGT: Floating Gate Transistor

MOSFET: Metal Oxide Semiconductor Field Emitter Transistor

SSDs: Solid-State Drives

PCRAM: Phase Change RAM

STTMRAM: Spin-Transfer Torque MRAM

BJT: Bipolar Junction Transistor

PCM: Phase Change Memory

CBRAM: Conductive-Bridging RRAM

Ox RAM: Oxide RRAM

CF: Conductive Filament

Q-Dots: Quantum Dots

SPBMM: Stochastic Phase-Change-Based Memory

OSE: Orientation-Selective Epitaxy

EHD: Electro Hydro Dynamic

LSI: Large-Scale Integration

VLSI: Very Large-Scale Integration

NVRAMs: Non-Volatile Random-Access Memories

Fe-FET: Ferroelectric FETs

PVD: Physical Vapor Deposition

CVD: Chemical Vapor Deposition

MBE: Molecular Beam Epitaxy

SEM: Scanning Electron Microscopy

SED: Secondary Electron Detectors

BSD: Backscattered Electron Detectors

EDS: Energy Dispersive Spectroscopy

E-T: Everhart-Thornley

SDD: The Silicon Drift Detector

FE-SEM: Field Emission Scanning Electron Microscope

EDX: Energy-Dispersive X-Ray Spectrometry

AFM: Atomic Force Microscope

HRTEM: High-Resolution Transmission Electron Microscopy

P-E: Polarization-Electric Field

IPDs: Inter-Poly Dielectrics

CHAPTER 1
INTRODUCTION

The semiconductor industry's pursuit of miniaturization has driven the evolution of gate dielectrics and capacitor dielectrics, transitioning from simple binary oxides to complex multifunctional materials. Processors initially employed Silicon Dioxide (SiO_2) as the gate material but later adopted thicker high-*k* dielectrics to mitigate leakage while sustaining capacitance by reducing the thickness. However, as device dimensions continue to shrink, alternative high-*k* dielectrics with enhanced electrical properties and CMOS compatibility have become essential. Simultaneously, the memory hierarchy demands high-density, non-volatile storage solutions, fueling the exploration of non-linear high-*k* ferroelectric materials for integration into the CMOS platform. This chapter explores the development of linear high-*k* dielectrics as alternative gate oxides to address the challenges in the electrical performance of logic devices and non-linear high-k ferroelectrics for advanced memory devices.

1.1 Background on Logic and Memory Devices

Gate dielectrics and capacitor dielectrics have undergone numerous innovations over time to align with Moore's law of scaling in integrated circuits, enabling processors and memory devices with enhanced performance compared to their predecessors [1]. The exploration of simple binary oxides, multicomponent oxides, and more complex multifunctional oxides has gained attention in the semiconductor industry due to their versatile properties, such as dielectric, ferromagnetic, piezoelectric, pyroelectric, ferroelectric, and multiferroic behaviors. These materials are integral part to a wide

range of applications, including optoelectronics, thermoelectrics, energy harvesting, energy storage, and nanoelectronics for information technology and data storage [2]. In processors, the first oxide used for gate-dielectric applications was conventional SiO_2. However, as scaling advanced, it was replaced with thicker high-*k* dielectrics like Silicon Oxynitride (SiON) to reduce leakage current while maintaining capacitance. These materials, characterized by a voltage-independent dielectric constant (ε_r or *k*), are often referred to as linear dielectrics. This innovation facilitated the downscaling of logic devices and the fabrication of sub-nanometer (<5 nm) dielectric films, thereby increasing the integration density in Si-based complementary metal-oxide-semiconductor (CMOS) technology, as depicted in **Figure 1.1 (left)**.

Similarly, in the memory hierarchy, high-*k* materials have been explored to achieve higher storage densities in Dynamic Random-Access Memory (DRAM), the primary memory technology used in computers. The main challenge in DRAM technology is to scale down the storage cell capacitor while ensuring sufficient charge storage for error-free detection, as limited charge can lead to sensor inaccuracies. High-*k* materials, similar to those used in processor as gate-oxide, have been introduced to meet these demands [1, 3]. However, a significant limitation of DRAM is its volatile nature, as stored charges leak and disappear over time. Consequently, each memory cell must be rewritten periodically, a process known as "refresh," with a typical refresh rate of 64 ms at nominal temperatures. This limitation has driven research toward alternative memory technologies that combine high density with non-volatility. Non-volatile RAM (NVRAM), based on nonlinear dielectrics like ferroelectric materials, is particularly promising due to its low power dissipation and radiation tolerance [3, 4]. When a sufficient oscillating electric field (E), exceeding

the coercive field (E_c), is applied to a ferroelectric (FE) material, the electric polarization versus applied field curve exhibits hysteresis behavior, as shown in **Figure 1.1 (right)** [4]. This polarization bistability is a key feature for non-volatile memory applications. The potential realization of high-density ferroelectric memory, comparable to DRAM and flash memory, could lead to the development of a "universal memory." Such a memory device would merge the advantages of existing technologies, including the fast but low-density Static Random-Access Memory (SRAM), the medium-fast yet power-dissipating DRAM, and the very high-density, non-volatile but slower flash memories.

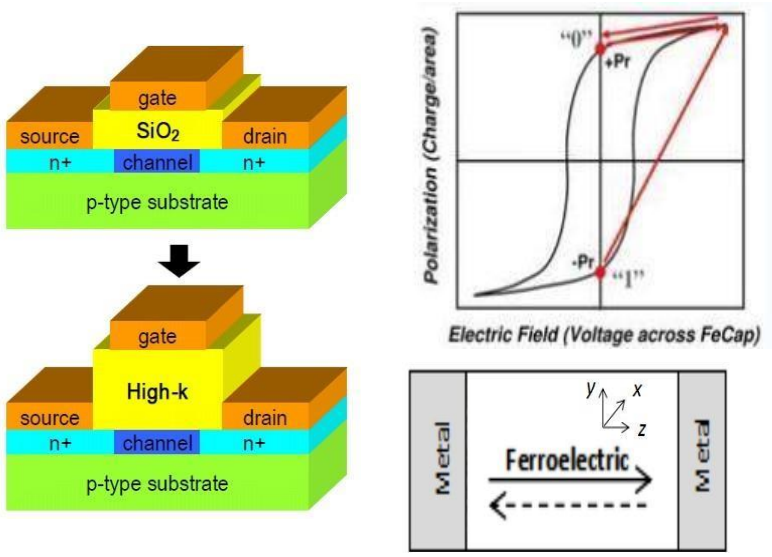


Figure 1.1 Graphic of MOSFET with SiO_2 and high-*k* dielectric showing a physically thicker high-k layer compared to SiO_2 for obtaining the same capacitance (left). Polarization vs. electric field of a ferroelectric capacitor showing “0” and “1” s binary states (right).

The effective attainment of novel linear high-*k* and non-linear high-*k* (ferroelectric) materials in logic and memory devices, respectively, ensures low energy utilization and faster operation. However, obtaining appropriate materials (high-*k* dielectric and ferroelectrics) that are compatible with the CMOS procedure is the primary barrier to overcome and is considered in this thesis entitled "*Development of high-k dielectrics as an alternate gate-oxide for logic and memory devices*". Research work thus involves the preparation of targets (bulk ceramics) and testing of non-linear high-*k* ferroelectrics and linear high-*k* dielectric thin films for realizing practical energy-efficient microelectronic devices. The compatibility of high-*k* dielectrics (both linear and nonlinear) with semiconductors can enable processors and memories to address the present demands of the industry in terms of speed and density [5]. Increasing demands in information technology challenge processors and memory devices to deliver higher speed, capacity, and performance efficiency. This research focuses on addressing future semiconductor industry requirements by advancing innovative technologies for logic and memory devices with next-generation applications.

1.2 Thesis Objectives

The semiconductor industry is concerned with the strategy for the implementation of a silicon free high-*k* dielectric gate-oxide for logic devices and a novel multifunctional material for the memory devices. For logic devices, the focus is on high-k gate oxides with dielectric constant values in the range of 20–40, minimal fixed charges, optimal interfacial trap densities, and a desirable band offset with silicon (>1 eV). For memory devices, the attention shifts to non-linear high-k materials, particularly ferroelectric materials, which can be seamlessly integrated into standard CMOS

platforms. These two critical aspects form the foundation of the proposed thesis. The overarching aim of this research is to develop novel multicomponent oxides with multifunctional properties for non-volatile memory applications, along with alternate high-*k* dielectrics exhibiting superior oxide properties for logic devices. The research methodology involves a two-step approach. Bulk ceramics are prepared and evaluated to optimize the material composition. Optimized compositions are used to prepare thin films via Pulsed Laser Deposition (PLD). The major objectives of the thesis are then broadly classified into two groups and are given below.

1. To develop new linear high-*k* dielectric materials (Hf_x, $Zr_{1-x})_{0.8}$ $(Dy_{0.5}Ta_{0.5})_{0.2}O_2$, [where x= 0.25, 0.5, and 0.75] for integrating with standard Si technology for the 4^{th} generation gate-oxide in logic devices.

2. To develop a CMOS-compatible nonlinear high-*k* ferroelectric material ($Hf_xZr_{1-x}O_2$) [where x= 0.25, 0.5, and 0.75] for the non-volatile memory devices.

The elements of transition metals (Ta, Hf, and Zr), and rare earth (Dy) considered for the preparation of the novel compounds for the present study are CMOS compatible as oxides of these elements are already familiar to the semiconductor industry. In the following subsections, the material used in these two categories will be briefly reviewed to understand the importance of the present study and the research gap in terms of the Si-based CMOS process.

1.2.1 Gate-Oxides in Logic devices

The Metal Oxide Semiconductor Field Effect Transistor (MOSFET), illustrated in **Figure 1.2**, serves as the fundamental building block for all computer chips. For over 50 years, MOSFETs have adhered to Moore's Law, driving the consistent advancement of integrated circuit performance [1]. The remarkable success of the semiconductor industry is attributed to two key factors: the relentless miniaturization of transistors and the incorporation of innovative materials into the manufacturing process. These advancements have been instrumental in enhancing the functionality and efficiency of modern electronic devices.

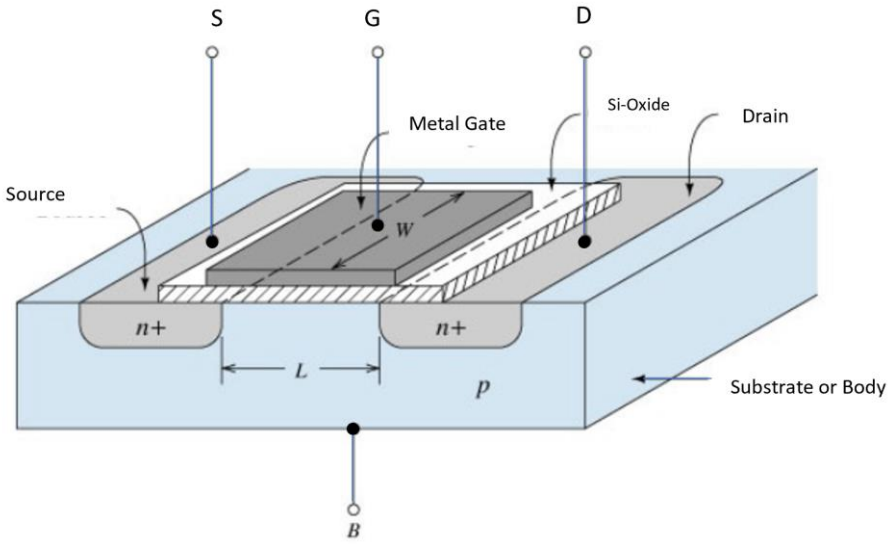


Figure 1.2 MOSFET device assembly with terminals, source, gate, and drain.

The semiconductor industry has experienced remarkable advancements, primarily driven by the relentless pursuit of smaller MOSFET dimensions, culminating in the integration of billions of transistors per chip at present from a couple of thousand transistors at the start. This exponential increase in transistor density has not only enhanced speed and performance but also played a crucial role in reducing

manufacturing costs per bit, fundamentally transforming the landscape of modern computing. Initially, the transistor configuration predominantly featured a gate-oxide composed of SiO_2, with a dielectric constant of 3.9, which exhibited exceptional scalability [6-7]. This first-generation gate dielectric remained prevalent in processors until around 1990, establishing the foundation for subsequent advancements in semiconductor technology. The evolution of gate-oxides can be categorized into three distinct generations as shown in **Figure 1.3**, each marking a significant milestone in the integration of diverse dielectric materials with silicon. As mentioned, the first generation was predominantly composed of SiO_2, which provided a robust interface with silicon, ensuring reliable transistor operation. Subsequent advancements led to the adoption of SiON and Si_3N_4 (ε_r from 3.9 to 7) dielectrics as 2nd generation gate-oxides, marking the smooth transition towards higher performance MOSFET in CMOS technology as can be seen in **Figure 1.3** and continued until late 2000 [8-9].

In 2007, the introduction of Intel Core™ processors marked a significant milestone in the semiconductor industry, boasting dual-core and quad-core configurations housing over 400 million and 800 million transistors respectively. This marked a paradigm shift in computational power and set the stage for further advancements in processor technology. As semiconductor technology progressed towards smaller technology nodes such as 45 nm and 32 nm, new challenges emerged, including interface defect density and high intrinsic leakage current. These challenges were exacerbated by the decreasing physical thickness of gate-oxides, which approached the sub-nanometer scale (~1.2 nm), equivalent to only 3-4 monolayers of standard SiO_2/SiON [6, 9]. To address these issues, researchers and engineers turned to novel dielectric materials with higher dielectric constants (high-*k*), larger band gaps, and improved stability in

silicon contact. One such breakthrough was the adoption of Silicon Hafnium Oxynitride (SiHfON) as an alternative to SiON, particularly at the 45 nm node. SiHfON offered sub-nanometer Equivalent Oxide Thickness (EOT) values, thereby mitigating performance degradation associated with interface defect density and leakage current of SiON and Si_3N_4. Additionally, the incorporation of nitrogen on silicon dioxide films proved effective in preventing the formation of Silicon Oxide (SiO_x) layers at the silicon surface, further enhancing transistor performance and reliability [8]. Ab initio calculations played a crucial role in elucidating the impact of nitrogen on the conduction band offset, providing valuable insights for the development of next-generation gate dielectrics. The integration of SiHfON and other advanced dielectric materials, coupled with metal gate configurations, has propelled CMOS technology into the era of sub-10 nm feature sizes, paving the way for continued innovation in semiconductor manufacturing. Over the span of 60 years, gate-oxides with dielectric constants ranging from 3.9 to 14 have been utilized across various technology nodes, reflecting a continuous evolution towards higher performance and efficiency in semiconductor devices as can be seen in **Figure 1.3**. The adoption of SiHfON (ε_r from 7 to 14) dielectrics as 3rd generation gate-oxides is what we are using at present. Looking ahead, the relentless pursuit of novel materials and innovative device architectures will continue to drive progress in the semiconductor industry, enabling new frontiers in computing and beyond.

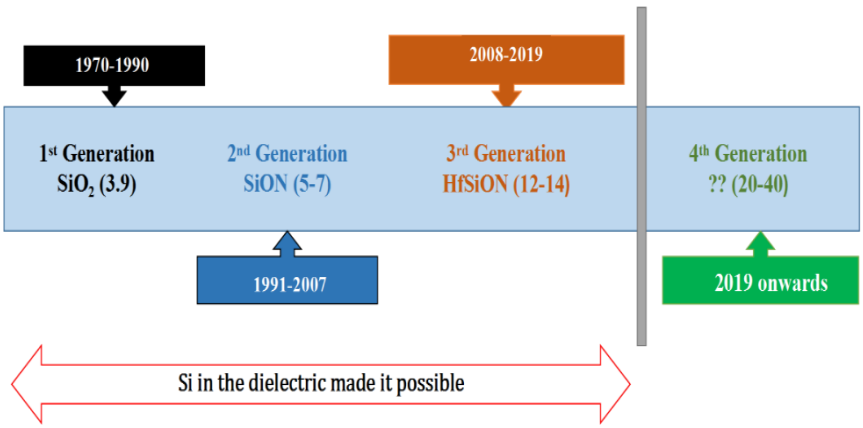


Figure 1.3 History of silicon display gate-oxide generations during the dated 1970 till today.

Now the evolution of gate-oxides can be categorized into three distinct generations, each representing significant milestones in the integration of diverse dielectric materials with silicon. However, the materials currently used in gate-oxide applications also need replacement as the sizes shrink further. Early explorations in the late 1990s focused on materials such as tantalum pentoxide (Ta_2O_5) and Teflon are quickly abandoned due to the low band offset and low dielectric constant, respectively [9-10]. The advent of the new millennium witnessed the investigation of multilayer gate stacks incorporating high-*k* dielectrics and nitrides, including Metal/Nitride/Oxide/Silicon (MNOS), Metal/Oxide/Nitride/Oxide/Silicon (MONOS), Silicon/Oxide/Nitride/Oxide/Silicon (SONOS), and Oxide/Nitride/Oxide (ONO) [11-13], aimed at enhancing performance and charge trapping capabilities. Aluminum Oxide (Al_2O_3) emerged as a promising candidate, with post-annealed films deposited via Atomic Layer Deposition (ALD) and characterized for capacitance-voltage (C-V) and conductance spectroscopy [14,15]. Researchers also demonstrated good dielectric integrity with low leakage current density for unspecified materials [16-18].

Zirconium Aluminum Oxide ($ZrAl_xO_y$) [19] and Gallium Silicon Oxide ($Ga_{0.23}Si_{0.14}O_{0.63}$) [20] were proposed as potential alternatives to SiO_2 for deep submicron MOS gates, with the latter exhibiting a dielectric constant of 52, promising for alternate gate dielectrics [21]. Praseodymium Oxide (Pr_2O_3) films exhibited a dielectric constant of 23-25 and low leakage current density [22], while Zirconium Oxide (ZrO_2), Hafnium Oxide (HfO_2), Hafnium Silicate ($HfSi_xO_y$), and Aluminum Hafnium silicate ($AlHf_xSi_yO_z$) [23-24] garnered significant attention as high-*k* gate dielectrics. Notably, the density of surface states and trapped charges in the oxide layer increased significantly when the oxide crystal structure transitioned from amorphous to polycrystalline [25]. Gallium Oxide (Ga_2O_3)/silicon dioxide (SiO_2) and Gallium nitride (GaN)/silicon nitride (Si_3N_4) Metal-Insulator-Semiconductor (MIS) capacitors were evaluated using C-V measurements [26, 23], while electron trapping in Al-gate n-GaN/nitride-thin-film capacitors was studied [27- 29]. High-*k* materials like Erbium Oxide (Er_2O_3) [28, 2, 30, 31], Magnesium Oxide (MgO) [32, 33], and Titanium Dioxide (TiO_2) [34] were explored, with the latter demonstrating a dielectric current density suitable for high-performance logic circuits and low-power circuit fabrications.

The permittivity of Gd_2O_3 dielectric layers reached 16 [35], and epitaxial and amorphous Yttrium Oxide (Y_2O_3) films were investigated as alternative gate dielectrics for silicon [36]. Structural changes in unspecified materials were correlated with the structure of stable amorphous assemblies [37-39], and the growth and electrical characterization of (Al, Si)O gate dielectric deposited by Metalorganic Chemical Vapor Deposition (MOCVD) was reported [40]. Zinc Oxide (ZnO_2) semiconductors grown by Radio Frequency (RF) magnetron sputtering at room

temperature [41] and thorough assessments of properties under constant low current injection [42] were conducted. The excellent electron transport properties of Indium Gallium Arsenide (InGaAs) and Indium Arsenide (InAs) semiconductors [43] made them promising candidates for future nano-scale CMOS. Tunneling current density and tunnel resistivity modeling for ultra-thin oxide layer-based MOS devices confirmed the importance of considering image force effect tunneling current [44]. Two classes of high-*k*/n-InAlAs MOS-capacitors with HfO_2 and Hafnium Aluminum Oxide (HfAlO) dielectrics were successfully engineered [45], while Hafnium Titanium Oxide (HfTiO) high-*k* gate dielectric thin films were deposited on silicon and quartz substrates by RF magnetron sputtering [46]. The charge-trapping effects of HfO_2 gate stacks under heavy ion irradiation were evaluated via C-V measurement and Transmission Electron Microscopy (TEM) [47].

Amorphous Indium-Zinc-Tin-Oxide (IZTO) thin film transistors with various high-*k* materials as gate dielectrics were investigated [48], and C-V characteristics were studied for MOS devices with ZrO_2 and HfO_2 gate dielectrics [49]. The dielectric properties of Yttrium Calcium Tantalum Oxide (YCTO) bulk capacitors were examined [50], and a novel method of stacking dielectric layers on Silicon Carbide (SiC) was proposed to address SiO_2-SiC interface issues in SiC-based MOS devices [51]. Sub-10 nm high-*k* gate dielectrics were identified as critical for 2-D transition metal dichalcogenides transistors [52], with La_2O_3 proposed as a suitable alternative to hafnium oxide gate dielectric due to its excellent performance [53]. Low-cost methodologies for high-*k* ZrO_2 dielectric films and devices using light-wave irradiation-induced chloride-based low-temperature solution methods were demonstrated [54]. The RF performance of 3D double gate junction-less transistors

was explored, considering thin high-*k* dielectrics and gate metals [55]. Ternary Gadolinium-Yttrium-Oxide (Gd-Y-O) high-*k* films were evaluated against binary Gd_2O_3 and Y_2O_3 for gate dielectric applications [56], while a simple DC linear equivalent model was proposed to study silicon-on-insulator (SOI) lateral power devices utilizing high-*k* dielectrics [57].

Ternary gadolinium aluminum oxide ($GdAlO_x$) thin films were proposed as new gate dielectric materials [58], and ultrathin Strontium Titanate ($SrTiO_3$) dielectric layers with aluminum doping were explored to address challenges in ultra-high-*k* oxide MOS capacitors [59]. Simulations using Technology Computer-Aided Design (TCAD) were performed to acquire electrical properties of unspecified devices/materials [60-61]. Layer-by-layer, in situ H_2 plasma treatment during atomic layer deposition, termed "atomic hydrogen bombardment," was employed to enhance the electrical characteristics of ZrO_2 high-*k* gate dielectrics [62]. The synthesis of high-*k* hydrocarbon films by chemical vapor deposition was reported [63], and nickel incorporation into La_2O_3 was explored for a novel gate dielectric [64].

Although 4^{th} generation gate-dielectric arrival is imminent, the challenges associated with alternative gate dielectrics with the value of dielectric constant between 20-40, for Si-based processors are currently viewed as the most problematic research barricade to overcome. Integrated circuits have consistently faced the challenges in scaling down the dimension transistor and boosting the performance of devices. To achieve the benefits of downscaling the transistor size, industry has increasingly incorporated new materials into the CMOS fabrication process. The shift towards a high-*k* dielectric material without Si or SiO_2 is a promising solution for advancing CMOS technology to the 4^{th} generation of gate-oxides. However, the ideal high-*k*

dielectric should satisfy a set of rigorous conditions for the effective application in CMOS based on Si as follows:

1. Bandgap/ Band alignment: The valence and conduction band offset (ΔE_c) of high-*k* dielectric should be higher than 1eV. This inhibits the conduction of electrons or holes through the conduction band and valence band; respectively and hence the leakage current gets reduced in the transistor [65]. The dielectric constant varies inversely with the bandgap (**Figure 1.4**). Hence, the large bandgap energy results in a large conduction band offset. This imposes a severe restriction on the choice of dielectrics with a bandgap over 5 eV as can be seen in the **Figure 1.4** [66, 67].
2. Thermodynamic stability: The dielectric form silicate/SiO_2 after reaction with Si. The resultant low-*k* layer causes an increase in EOT which finally negates the valuable effect of high-*k* dielectrics [68, 69].
3. Kinetic stability: The oxide must resist the rapid thermal annealing process of CMOS flow (for 5s at 1000°C). An amorphous state is preferred over the crystalline phase. This is because of higher leakage currents and diffusion paths for carriers [70] in crystalline oxides.
4. Interface quality: The flow of carriers within the semiconductor, a few angstroms in the channel beneath the gate-oxide can be affected by scattering events, which reduces their mobility. This scattering can occur due to various factors, including impurities, defects, and interactions with phonons or other carriers. As a result, the overall performance of the channel is diminished, leading to lower efficiency in electronic devices [71]. Hence, the interface should be of the highest electrical quality.

5. Defects: These are impurities, oxygen deficiency, and fixed electrically active centers. These fixed inconsistencies also act as potential scattering positions for the carriers in the channel region [72].

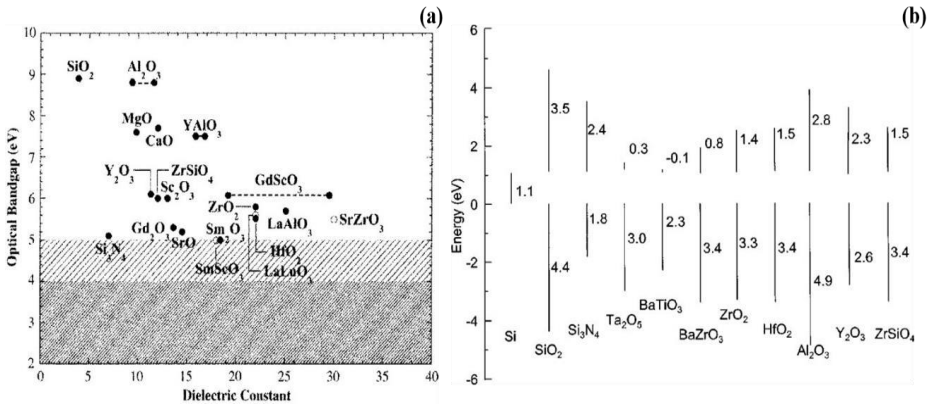


Figure 1.4 (a) Optical bandgap energies with the dielectric constant of various dielectric materials considered for the gate-oxide application showing a reducing trend with dielectric; (b) Energy to different compositions [65, 66].

1.2.2 Semiconductor Memory Devices

The journey of information storage has been marked by a remarkable evolution, stretching from ancient memory devices like 'The Analogue Rosetta Stone' to the cutting-edge digital storage solutions of today. This evolution reflects the ever-growing demand for digital memory endowed with enhanced capabilities, a demand that propels the semiconductor industry forward as it strives to meet the evolving requirements of future information technology. The technological advancement lies with the Internet of Everything (IoE), an interconnected ecosystem where Artificial Intelligence (AI), Machine Learning (ML), Internet of Things (IoT), big data, cloud computing, fog computing, edge computing, communication devices, routers, and sensors converge, necessitating robust and efficient non-volatile semiconductor

memories to sustain their seamless operation. Contrary to perceiving the semiconductor memory sector as a matured technology segment, its ongoing contributions underscore its dynamic nature and its ability to continually adapt to and address current demands.

The increasing prevalence of high-frequency logic and memory devices, coupled with the widespread use of smartphones and Microelectromechanical Systems (MEMS), has led to a significant rise in power consumption, driven largely by the vertical shrinkage of transistor dimensions. Despite the challenges posed by smaller lateral die sizes and rising storage densities, these devices continue to rely heavily on semiconductor substrates to power their operations [6]. The landscape of memory technologies is marked by diversification, reflecting the global demand for non-volatile data storage solutions. Emerging memory technologies, such as Ferroelectric RAM (Fe-RAM), Magnetic RAM (MRAM), and Resistive RAM (RRAM), have gained prominence since their proof of concept, offering potential to transform data storage paradigms [1-3]. However, modern non-volatile memory devices are required to possess attributes like speed, energy efficiency, high density, robustness, and radiation tolerance to ensure their long-term operational viability.

Semiconductor memory technologies are broadly categorized into volatile and non-volatile memories. Volatile memory, which loses data when power is interrupted, includes DRAM, Mobile DRAM (MDRAM), SRAM, and Synchronous DRAM (SDRAM). DRAM [7-8], with a cell structure consisting of a capacitor and transistor storing one bit of data per cell, is commonly used as primary memory in computing systems. In contrast, SRAM, made up of six transistors (including two cross-coupled ones), is utilized in cache memories due to its fast access times and low power

consumption [6]. Non-volatile memory retains data without power, with Read-Only Memory (ROM) being a prominent example. ROM contains essential system initialization programs like the Basic Input/Output System (BIOS), ensuring smooth hardware boot-up. Variants of ROM, such as Erasable Programmable ROM (EPROM), Electrical Erasable Programmable ROM (EEPROM), and Ultraviolet Programmable ROM (UVPROM), cater to different storage needs. A significant milestone in non-volatile memory technology was achieved with the invention of the Floating Gate Transistor (FGT) by Kahng D. and Sze S.M. at Bell Laboratories in 1967. This breakthrough led to the creation of flash memory, which utilizes a modified MOSFET structure with a floating gate positioned between the control gate and the body. Flash memory stores data by using charge states, offering long data retention. There are two primary types of flash memory: NOR and NAND. NOR flash, known for its larger cell sizes and direct write capabilities, is ideal for applications that require high-speed random access. In contrast, NAND flash, with smaller cells and page write capabilities, is commonly used in storage devices like Solid-State Drives (SSDs) and USB flash drives due to its higher storage density and cost-effectiveness. Emerging technologies, such as RRAM, Phase Change RAM (PcRAM), Magnetic RAM (MRAM), Spin-Transfer Torque MRAM (STTMRAM), and Ferroelectric RAM (Fe-RAM), are gaining momentum as potential replacements for conventional volatile memories like DRAM and SRAM. These technologies promise faster access times, greater endurance, and reduced power consumption, positioning them as leading contenders for future memory formats [7-8]. **Figure 1.5** illustrates the classification of various memory technologies based on their

operational characteristics, highlighting the emerging technologies for future memory solutions.

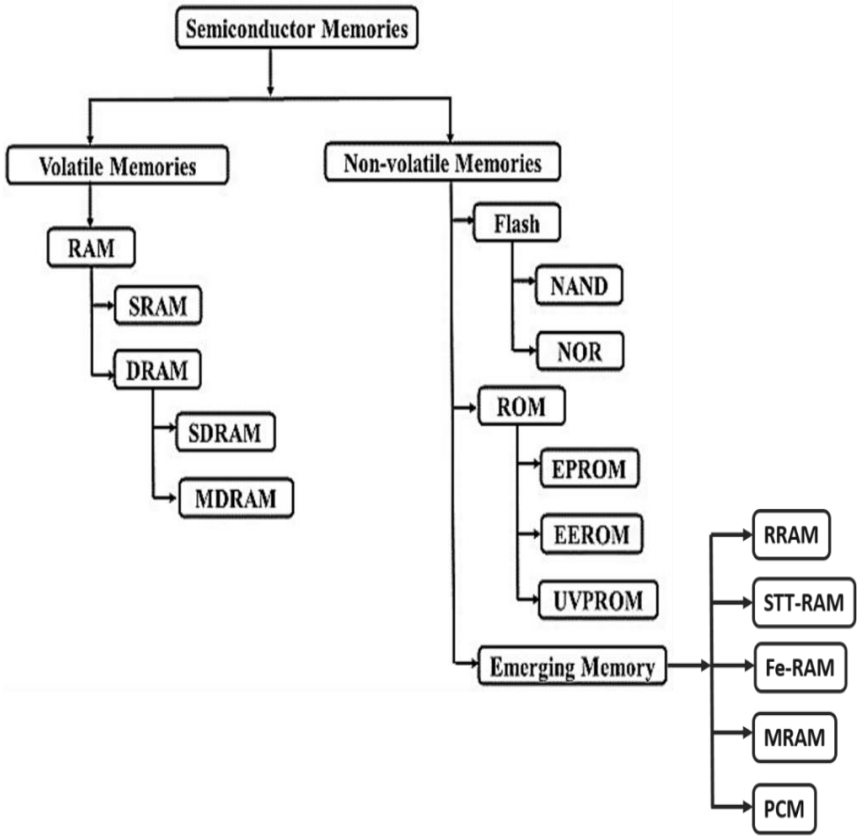


Figure 1.5 Classification of memory technologies concerning their functional aspects.

From the emerging memories, an intermediate endurance of 10^{10}–10^{12} and density in a Gigabyte (GB) can be achieved PcRAM or PCM. PcRAM's foundation is the materials like chalcogenides' reversible shift from low resistance (crystalline phase) to high resistance (amorphous phase). The design of the memory cell and the characteristics of the phase-change materials affect the performance of the memory cell. PcRAM cells must be configured to meet the needs of increased thermal isolation, reduced reset current, easy processing, and power efficiency. Materials utilized in PcRAM with several nm thin-film thicknesses or nanoparticle diameters

are used to exhibit the desired scaling behavior, which includes high crystallization temperature at a smaller dimension and decreasing thermal conductivity [7, 9]. The substantial switching current restricts the linear dependency of the threshold voltage. Despite successful experimental testing using Bipolar Junction Transistor (BJT) and diode devices, the efforts to shrink the cell size) encountered obstacles such as electrode voids (gaps in the electrode materials of electronics devices), particularly in integrated circuits during the fabrication process or as a result of operational stress over the time, element segregation, and changes in mass density. However, the development showcased remarkable features, including a fast-switching speed of 100 nanoseconds and an endurance of over one billion cycles ($>10^9$) in the case of PcRAM [6, 8]. Nevertheless, PcRAM is unable to displace Flash memory or DRAM primarily due to two factors: manufacturing costs and the continuous advancements within existing memory technology. Constant improvements in performance, density, and cost-effectiveness contribute to a competitive environment. These factors collectively make it difficult for PcRAM to surpass Flash and DRAM in terms of popularity and market dominance.

Table 1.1 The general characteristics of different memories available in the market.

	Non-volatility	Readout speed	Writing Speed	Endurance	Cell size	Integration with logic Circuits
DRAM	N	50 ns	50 ns	$>10^{15}$	8 F^2	YY
SRAM	N	5-70 ns	5-70 ns	$>10^{15}$	140 F^2	YY

Flash	Y	50 ns	10 ms	10^6	4 F^2	YY
Fe-RAM	Y	30-100 ns	30-70 ns	10^{12}	12-8F^2	Y
MRAM	Y	30-100 ns	10-50 ns	$>10^{15}$	8-40F^2	Y
PRAM	Y	30-100 ns	100 ns	10^{12}	4-8 F^2	Y
RRAM	Y	10-100 ns	10-100 ns	?	4-6 F^2	Y

"F" refers to the 'minimum feature size' that can be manufactured using a specific fabrication process. This means that the actual physical dimensions of the memory cells are scaled based on this minimum feature size, allowing for higher density in memory chip designs.

Table 1.2 The characteristics required for universal memory.

	DRAM	FLASH	Universal memory
Speed (Write/erase time)	High (10ns/ 10 ns)	Low (1ms/10ms)	High
Scalability (Cell size)	High($6F^2$)	High($10F^2$)	High
Endurance Cycles	High (10^6)	Low (10^5)	High
Energy efficiency	Volatile	Non-volatile	Non-volatile

Apart from Phase Change Memory (PCM), RRAM has garnered attention for its potential to create synaptic devices within 3D cross-point designs. RRAM is considered a promising candidate for memory operations due to its ion-based process control, which mimics synaptic plasticity observed in biological systems [6]. Operations for filamentary conductive-bridging RRAM (CBRAM) and oxide RRAM (ox RAM) [10-11] rely on the growth and breakdown of a Conductive Filament (CF) formed by oxygen ions and cations diffusing through the material.

The movement of oxygen ions/vacancies across the layer stack is crucial in oxide RRAM, influencing factors such as tunneling/Schottky barrier thickness and barrier height. However, the precise mechanism causing barrier modulation is still under debate. Various possibilities, including phase change, redox/oxidation, electrostatic effects, and modifications to local oxide stoichiometry, are being explored. Multiscale modeling platforms are employed to understand the behavior of RRAM devices by relating device performance to atomic material attributes [12-14]. These platforms consider the individual contributions of ions, vacancies/drifts, and their effects on power dissipation and local temperature, as well as different charge transport processes such as tunneling, drifting, diffusion, and hopping. Emerging memory technologies aim to overcome these challenges and are actively researched [9, 15]. However, attributes like low power consumption, non-volatility, density, and speed are crucial for future semiconductor memories. Such memory capabilities could pave the way for “universal memory" combining the non-volatility of FLASH, the durability of DRAM and SRAM, the speed of SRAM, and the scalability of DRAM & Flash (see **Table 1.1**-**Table 1.3**). Fe-RAM (Ferroelectric RAM) is a promising memory technology that utilizes a ferroelectric capacitor to replace the dielectric

layer, closely resembling DRAM in design and functioning similarly to flash memory in terms of non-volatility [9]. James Scott, co-founder of Symmetrix, made significant contributions to the advancement of ferroelectric memories by developing integrated thin-film ferroelectric technology for microelectronic devices. One of his key discoveries was that the Aurivillius class of ferroelectrics, such as $SrBi_2Ta_2O_9$ (SBT), does not suffer from polarization fatigue, unlike traditional perovskite ferroelectrics [16]. Despite its advantages, Fe-RAM has drawbacks, including high manufacturing costs due to the use of CMOS-incompatible materials and relatively low storage density compared to DRAM. However, Fe-RAM finds applications in various industries, including motion control, wireless data logging, RFID, gaming, and automotive systems, among others. Ferroelectric memory consists of a Ferroelectric Field-Effect Transistor (Fe-FET) and a ferroelectric capacitor (1C, 1T). Fe-FETs use ferroelectric polarization instead of a floating gate, similar to flash memory [17-18]. Challenges such as the need for thin ferroelectric films of less than 10 nm in both capacitors and transistors have slowed its implementation. However, the development of thin-doped HfO_2 films (<5nm) for these components, pioneered by Namlab in Germany, has moved the industry closer to achieving this goal [17]. Ferroelectric Tunnel Junctions (FTJs) represent another promising avenue, utilizing tunneling mechanisms to store and retrieve data by manipulating ferroelectric polarization states. The memory industry is expanding rapidly, with innovations such as quantum dots (Q-dots) [19], Zero-RAM [20], and Stochastic Phase-Change-Based Memory (SPBMM) [21], each promising to revolutionize memory technology by addressing limitations and optimizing data retention, energy efficiency, and system performance.

The convergence of cutting-edge memory technologies is poised to revolutionize data storage, access, and processing, ushering in a new era of technological development [15]. This surge in interest and investment reflects the industry's recognition of the need for innovative solutions as the market diversifies and evolves. These advancements hold the potential to reshape the memory landscape, offering new possibilities for data-driven enterprises and influencing the trajectory of technological progress.

Table 1.3 The comparison among SRAM, DRAM, and Universal Memory.

Memory Hierarchy	Speed (Write/erase time)	Scalability (size)	Endurance (Cycles)	Energy efficiency
Cache memory (SRAM)	High (0.3ns/0.3ns)	Low ($140F^2$)	High -10^6	Volatile
Primary memory (DRAM)	High (10ns/ 10 ns)	High ($6F^2$)	High -10^6	Volatile
Secondary memory (FLASH)	Low (1ms/10ms)	High ($10\ F^2$)	Low -10^5	Non-Volatile
Universal memory	High	High	High	Non-Volatile

Recent advancements in ferroelectric thin films for electronic devices, particularly Ferroelectric Tunnel Junctions (FTJs), have focused on improving high-density data storage. Researchers have explored various electrode materials, ferroelectric barriers, and deposition techniques to enhance performance. In 2009, $La_{0.67}Sr_{0.33}MnO_3$ and Cr/Pt were used as electrodes, with $BaTiO_3$ (BTO) as the ferroelectric barrier, deposited by Pulsed Laser Deposition (PLD) at 1 nm [73-74]. In 2010, $SrRuO_3$ and a conductive tip were used as electrodes, with $PbTiO_3$ films (3.6 nm) [75]. In 2013, researchers utilized $Ca_{0.96}Ce_{0.04}MnO_3$ and Co/Pt as electrodes, with $BiFeO_3$ (BFO) as the ferroelectric barrier [77-78]. Later, innovations included the use of graphene and various deposition methods. In 2016, Nb: $SrTiO_3$ and Au/Ti were used with BTO films of 10-unit cells [83-84]. By 2019, SnSe films (8 nm) were deposited with In:SnSe and Sb:SnSe electrodes, demonstrating further improvements in performance [86]. These developments highlight ongoing efforts to optimize ferroelectric thin films, with the goal of meeting the demands of advanced electronic devices. The semiconductor industry is expanding beyond conventional technologies, exploring innovations like quantum dots [19], Zero-RAM [20], and Stochastic Phase-Change-Based Memory (SPBMM) [21], all of which aim to revolutionize memory technology by enhancing data storage, efficiency, and system performance.

Therefore, Emerging memory technologies, such as Fe-RAM and Resistive RAM based on FTJs, have shown great promise as potential game-changers in data storage. Since their proof of concept, these technologies offer a glimpse of the ability to redefine data storage paradigms [1-3]. However, contemporary non-volatile memory devices must meet key requirements such as speed, energy efficiency, high density, robustness, and radiation tolerance to ensure their suitability for long-term operational

use. FTJs play a crucial role in memory technology by utilizing tunneling mechanisms to store and retrieve data through the manipulation of ferroelectric polarization states. As a result, FTJs represent a promising avenue for advancing memory technologies, offering the potential for enhanced data storage, preservation, and processing capabilities by harnessing the unique properties of ferroelectric materials. The environmental impact of emerging memory technologies deserves attention due to the increasing emphasis on sustainability in semiconductor manufacturing. High-k materials like HfO_2 and ZrO_2 require energy-intensive fabrication processes, raising concerns about carbon footprints. Ferroelectric memory devices offer advantages in energy efficiency, potentially reducing power consumption compared to traditional DRAM or flash memory technologies

The semiconductor industry faces significant challenges as device dimensions continue to shrink. The need for materials with higher dielectric constants is critical to maintaining capacitance while reducing leakage currents. High-k dielectrics, such as Hafnium Oxide (HfO_2) and Zirconium Oxide (ZrO_2), have emerged as solutions, but CMOS compatibility remains a key obstacle. In memory technologies, the demand for non-volatile solutions has led to the exploration of ferroelectric materials like $Hf_xZr_{1-x}O_2$, which exhibit bistable polarization states. These advancements aim to address modern challenges in speed, density, and energy efficiency while overcoming limitations like leakage currents and scalability issues.

1.3 Research Gap

Despite the considerable progress made in the development of high-*k* dielectric materials for gate-oxide applications in logic and memory devices, several critical research gaps remain to be addressed:

1. Compatibility with CMOS Process: The primary challenge lies in identifying high-*k* dielectric and ferroelectric materials that seamlessly integrate with the existing CMOS fabrication process. Ensuring compatibility is essential for the practical implementation of these materials in microelectronic devices within the semiconductor industry.
2. Non-linear High-*k* Ferroelectrics: Non-volatile memories, particularly those based on ferroelectric materials, hold promise for achieving higher storage density and lower power dissipation..
3. Energy Efficiency and Speed: While high-*k* dielectric materials have contributed to the development of energy-efficient microelectronic devices with enhanced speed, there remains ample room for improvement. Research efforts should prioritize the pursuit of better energy utilization and faster operational performance by exploring innovative high-k dielectric and ferroelectric materials.
4. Scaling and Density: The escalating demand for information technology necessitates processors and memories with increased speed and density. Therefore, exploring novel materials and techniques capable of facilitating further scaling and heightened integration density is imperative to meet the future demands of the semiconductor industry.

CHAPTER 2

RESEARCH METHODOLOGY AND EXPERIMENTAL DETAILS

The materials that are required for the logic and memory devices discussed in the introduction need to have specific properties even though they come under the class of dielectric materials. This chapter discusses the types of dielectric materials and their application in the semiconductor industry. The preparation of the materials and various characterization techniques will also be discussed subsequently. Dielectric materials function as insulators, preventing the flow of current when subjected to an applied electric field (E=V/d, where V is the voltage and d is the thickness of the dielectric under test). Despite this apparent lack of current flow, atomic-level changes occur when a voltage is applied such that the material gets polarized due to the slight shift in electron clouds towards the positive voltage and nuclei towards the negative voltage. Although this electron/nuclei shift is microscopic and doesn't generate a conduction current flow through the material, it holds significant importance, particularly in capacitor applications as the origin of displacement current. When the voltage source is removed, the dielectric object either reverts to its original non-polarized state or remains polarized, depending on the strength of molecular bonds within the material. All dielectric materials are insulators, and that readily undergoes polarization upon the application of an electric field [2,10]. There are three types of polarization that occurs in a dielectric material, electronic, ionic and dipolar. Electronic or atomic polarization, electron clouds of the atom get displaced with respect to the heavy fixed nuclei to a distance less than the dimension of the atom and

is instantaneous. In the case of ionic polarization, positive and negative ions get displaced in the presence of an electric field. Both electronic and ionic polarization are independent of temperature and the dipoles are induced in the material by the electric field. The third type of polarization is orientational polarization, and is observed in polar dielectrics, dielectrics with permanent dipoles. In the presence of an applied field these dipoles orient in the direction of the field. When a dielectric material is subjected to an electric field, several atomic-level changes occur. In electronic polarization, the electron cloud around each atom is displaced relative to the nucleus, creating an induced dipole moment. In ionic polarization, positive and negative ions within the material shift slightly from their equilibrium positions, enhancing the overall dipole moment. In polar dielectrics, existing permanent dipoles tend to align with the applied field. These changes collectively contribute to the material's ability to store electrical energy and influence its overall electrical properties. For instance, the alignment of dipoles reduces the electric field within the material, increasing its capacitance. The speed and extent of these changes also determine the material's dielectric loss and frequency response. Understanding these atomic-level changes is crucial for tailoring dielectric materials for specific applications**.** The degree of polarization, induced by a specific applied voltage/electric field, dictates the amount of electrical energy stored in the dielectrics, a characteristic described by the dielectric constant of the material. However, dielectric materials encompass other crucial properties beyond the dielectric constant. Parameters such as dielectric strength and dielectric loss play equally pivotal roles in selecting materials for capacitors in specific applications or as gate-oxide materials. The exploration of dielectric materials is a multifaceted journey, delving into the intricate realms of

linear and non-linear behaviors. The review discussed here embarks on an expansive discourse, weaving together historical perspectives, seminal works, and contemporary research findings to present a comprehensive understanding of dielectric materials and their diverse applications.

While all dielectrics are insulators, the distinction lies in their intended function and performance characteristics. A standard insulator, such as Teflon or polyethylene, primarily serves to block the flow of current and provide electrical isolation. Effective dielectrics, on the other hand, are specifically chosen for their ability to store electrical energy and enhance capacitance, particularly in applications like capacitors and gate oxides in MOSFETs. Criteria that differentiate effective dielectrics include a high dielectric constant (k), low dielectric loss, high dielectric strength (breakdown voltage), and good temperature stability. For instance, HfO_2 is an effective dielectric due to its high k value compared to SiO_2, allowing for thinner equivalent oxide thicknesses in MOSFETs. Piezoelectric and Ferroelectric materials offer even more specialized dielectric features such as mechanical energy storage.

Linear dielectric materials, comprising traditional substances like porcelain, glass, and plastics, adhere to classical relations governing the interplay between electric field and displacement. These materials are characterized by a dielectric constant varying field strengths and frequencies. A pivotal attribute of linear dielectrics is their ability to support electrostatic fields while dissipating minimal energy in the form of heat. This foundational understanding sets the stage for exploring their applications, particularly in the construction of radio frequency (RF)-transmission lines. Contrastingly, the narrative takes a fascinating turn when delving into non-linear dielectric materials. Among these, ferroelectric substances, exemplified by PMN-PT

relaxor ceramics, have been subjects of extensive study [56]. The hallmark of these materials is a pronounced nonlinearity in polarization, especially with the electric field. Noteworthy contributions, such as E. T. Jaynes' seminal work in 1955, shed light on the unique properties of ferroelectrics [46]. The intrinsic high dielectric constant of ferroelectrics emerged as a distinguishing factor, positioning them as prime candidates for manifesting high degrees of nonlinearity. Expanding the horizon, the realm of non-linear dielectric composites also emerged. These composites feature materials whose dielectric constants exhibit nonlinear variations with the electric field or temperature and other inclusion of ferroelectric, semiconducting, and varistor-type fillers imparts additional advantages in terms of flexibility and mechanical strength. These composites find applications in energy storage by enhancing dielectric constants and the dielectric breakdown voltage/field. Practical applications of dielectric materials continue to evolve in the integrated circuits, with a particular focus on low dielectric constant (low-*k*) inter-dielectrics.

These materials aim to mitigate line-to-line noise in interconnects, a crucial concern in modern integrated electronic systems. However, the impact of high-*k* dielectric integration takes center stage, especially concerning its role as gate-oxide materials for nanoscale MOSFETs. The dielectric materials are classified in **Figure 2.1** based on their functional properties and discussed in the subsequent sections.

Dielectric materials, as mentioned before, are fundamental components in various electronic devices due to their ability to store and transmit electrical energy. These materials exhibit unique properties that are essential for the functionality of modern technology. Among these properties, piezoelectricity, pyroelectricity, and ferroelectricity stand out as particularly important for diverse applications across

multiple industries. This discussion explores the relationship between dielectric, piezoelectric, pyroelectric, and ferroelectric materials (**Figure 2.1**), highlighting their characteristics, applications, and significance in contemporary electronics. Dielectric materials are characterized by their ability to polarize in response to an applied electric field, resulting in the displacement of charge within the material. This polarization phenomenon occurs due to the alignment of electric dipoles within the dielectric material, leading to the formation of an electric field opposing the applied field (depolarization field). Dielectrics are widely used in capacitors, insulators, and other electronic components to store and transmit electrical energy efficiently [1,17, 46].

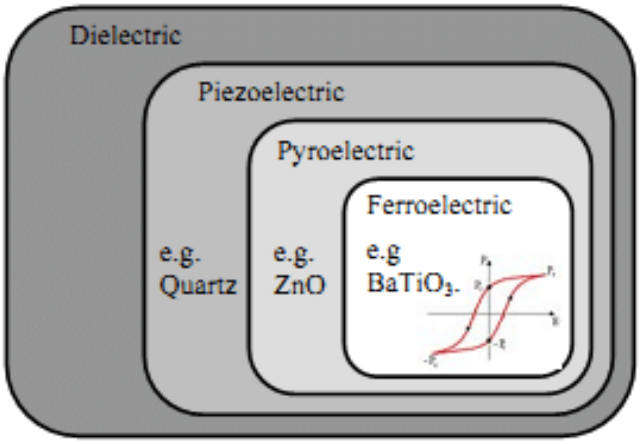


Figure 2.1 The classifications of dielectric materials.

Piezoelectric materials exhibit a unique property known as piezoelectricity apart from being dielectric, where mechanical stress induces an electric charge and conversely, an electric field causes mechanical deformation. This phenomenon arises from the asymmetrical arrangement of atoms or ions within the crystal lattice of certain materials that ensures lack of symmetry in the crystal structure. When subjected to

mechanical pressure or stress, piezoelectric materials generate an electric potential across their surfaces due to the displacement of positive and negative charges. Conversely, the application of an electric field causes the material to deform or change shape, making piezoelectric materials ideal for sensors, actuators, and energy harvesting devices in renewable energy systems by converting the mechanical energy to electrical energy [2, 18, 46]. However, pyroelectric materials possess the ability to generate an electric charge in response to changes in temperature as well as stress. This phenomenon, known as pyroelectricity, arises from the spontaneous polarization of the material's crystal lattice structure. As the temperature of a pyroelectric material changes, the symmetry of its crystal lattice is altered, leading to the redistribution of charge and the generation of an electric field. Pyroelectric materials are widely used in thermal sensors, infrared detectors, and energy harvesting systems, where they convert thermal energy into electrical energy [46]. In the same category of materials, ferroelectric materials exhibit a unique property called ferroelectricity, characterized by the reversible switching of spontaneous electric polarization in response to an applied electric field.

Unlike conventional dielectrics, ferroelectric materials retain their polarization state even after the removal of the external electric field, making them ideal for non-volatile memory devices. This property arises from the presence of asymmetric crystal structures, which allow the alignment of electric dipoles in different directions. Ferroelectric materials such as Lead Zirconate Titanate (PZT) and Barium Titanate ($BaTiO_3$) are extensively used in FeRAM, piezoelectric actuators, and sensors [17, 46].

2.1 Linear high-*k* dielectric

Linear dielectrics refer to insulating materials that demonstrate a proportional relationship between the Electric Displacement (D) and applied Electric Field (E) according to $D = \varepsilon^* E$, *where* ε^* is the complex dielectric permittivity [2, 10]. The unique linear polarization response of certain materials makes them particularly advantageous for a wide range of applications in electrical engineering, including microelectronics, optoelectronics, and components such as cables and capacitors. However, their most critical application lies in their use as gate oxide dielectrics in MOSFETs, which are fundamental to the construction of modern Large-Scale Integration (LSI) and Very Large-Scale Integration (VLSI) circuits Ultra Large-Scale Integration (ULSI) [67]. The gate oxide, typically made of SiO_2, serves as an extremely thin insulating dielectric layer that is either deposited or grown on the surface of a semiconductor, most commonly silicon. This layer is essential as it insulates the conductive gate electrode from the underlying semiconductor substrate, which contains the MOSFET's channel region. By enhancing the gate capacitance, the gate oxide ensures that the oxide capacitance surpasses the channel capacitance, thereby significantly improving device performance and efficiency in integrated circuits [67-69]. A voltage applied at the gate terminal sets up an electric field across the linear gate oxide gate. This induces opposite polarity charges in the semiconductor surface adjoining the gate oxide according to the fundamental Gauss's law.

The surface charge modulates the conductivity of the channel allowing switching operation critical to digital circuits. SiO_2 has historically remained the material of choice for the gate insulator over decades of microelectronics evolution owing to some of its salient properties - large band gap of 9 eV, good interface quality, linear

dielectric behavior, chemical stability, in addition to excellent insulating characteristics [5]. The number of MOSFETs integrated into a chip has doubled approximately every two years as per the well-known Moore's law [1]. This has been made possible by aggressive transistor dimensional scaling over 5 decades enabled by semiconductor manufacturing advances. Consequently, gate oxide thickness has gradually reduced from about 100 nm in first generation Metal-Oxide-Semiconductor (MOS) technology microprocessors in the 1970s [35] to merely 0.5 nm in leading-edge 5 nm node processors expected to enter mass production soon [56]. Accompanying length scale reduction into nanometer regimes has been the emergence of direct quantum mechanical tunneling of carriers across the oxide. This tunneling current increases exponentially for thinner oxides and can no longer remain ignored in contemporary devices, necessitating the introduction of new insulating materials. Nevertheless, the linear dielectric properties exhibited by the thermally grown SiO_2 films even at those dimensions have remained indispensable until recently. However, excessive leakage currents in ultra-thin SiO_2 films (< 2 nm) led to excess power dissipation and reliability issues [88]. This has led to active research into higher dielectric constant materials as replacements for SiO_2. The use of higher *k* materials allows for increased physical thickness while maintaining the same equivalent oxide thickness, thereby reducing tunneling effects. Following extensive evaluations of various candidates, HfO_2 has emerged as the leading alternative due to its linear dielectric properties at EOTs below 1 nm and its relatively smooth interface with silicon substrates. The gradual integration of HfO_2 as the gate dielectric has enabled further scaling of both gate oxide and transistor dimensions [89].

Current research is focused on sub-1 nm EOTs, high-mobility channel materials such as Ge and InGaAs, gate-all-around nanowire/nanosheet designs, and novel device architectures, which are promising avenues to sustain Moore's Law beyond the 5 nm node [2,10]. Beyond their essential role in CMOS VLSI circuits that drive the modern information revolution, linear dielectrics serve a variety of other functions. For instance, passive components like capacitors utilize linear dielectrics as insulating materials between conducting plates, making them prevalent across electronic systems from circuits to chip packages, where they facilitate power delivery and signal coupling applications.

Additionally, their low dielectric losses make them well-suited for communication signal transmission. Silica optical fibers, which leverage the linear dielectric properties of silica glass, have enabled global connectivity through low-loss optical data transmission since the late 20th century [45, 55, 56]. Prior to the advent of fiber optics, telecommunications primarily relied on metallic cables for signal propagation, which were limited by losses at high frequencies and constrained transmission bandwidths. The low attenuation window of silica glass, spanning from 800 nm to 1650 nm, coincides with optical frequencies and facilitates low loss guided wave propagation through total internal reflection in optical fibers [55]. This advancement has ultimately led to the establishment of transcontinental and transoceanic optical fiber communication systems that underline today's hyper-connected world. Furthermore, plastic and polymer linear dielectrics are utilized as electrical cable insulation materials, providing the high breakdown strength necessary to prevent short circuits.

2.2 Non-linear high-*k* Ferroelectric

Non-linear dielectrics are the sub-category of dielectrics, portrays non-linear coupling between applied electric field and resultant polarization (P), unlike linear dielectrics that follow a proportional relationship between the two [56]. The polarization response in such materials not only depends on the present electric field but is also strongly influenced by their prior electrical excitation history. This gives rise to unique phenomena of hysteresis, memory effects, and reversible polarization states. Ferroelectrics constitute an important subclass of technologically relevant non-linear dielectrics, which are piezoelectric as well as pyroelectrics characterized by the existence of a spontaneous electrical polarization that can be reversed on application of suitable electric fields. Some common ferroelectric materials include $BaTiO_3$, PZT, and Potassium Niobate ($KNbO_3$) which are perovskite structured metal oxides [87-88]. Owing to their switchable polarization and excellent piezoelectric properties, ferroelectrics continue to find widespread usage in transducers, actuators, and Non-Volatile Random-Access Memories (NVRAMs). In particular, the bi-stable polarization states exhibited by ferroelectric films make them extremely attractive for application as a storage medium in non-volatile semiconductor memories used in modern computing systems and portable electronics [57, 88-89]. Fe-RAM is a type of NVRAM that encodes binary data bits (“0” or “1”) based on the polarization orientation of nanometer-scale ferroelectric films integrated into a metal-insulator-metal capacitor structure. Read and write operations on the FeRAM cell are achieved by applying appropriate voltage pulses to effectively sense and switch the polarization direction [56-57]. In comparison to popular non-volatile flash memories, key merits of Fe-RAMs include – lower read/write power, faster write speeds supporting ~10 ns

access times, and higher endurance (over 10^{12} read/write cycles) [45, 90]. However, poorer scalability and density have hampered widespread commercial adoption. An alternative approach gaining significant research traction is the integration of ferroelectric films as gate insulators in MOSFET structures, widely referred to as Ferroelectric FETs (Fe-FET) [58]. Analogous to floating gate devices, charges can be stored in defects at the semiconductor-ferroelectric interface enabling non-volatile shifts in transistor threshold voltage and hysteretic current-voltage characteristics. However, Fe-FET architecture promises enhanced scalability by leveraging industry-standard CMOS fabrication protocols. Recent demonstrations have exhibited functioning Fe-FETs with sub-10 nm gate lengths and record low programming voltages, underscoring their emerging potential to extend non-volatile memory scaling limits beyond current Flash. Apart from memories, the analog-like conductivity modulation in Fe-FETs has inspired new computing paradigms like neuromorphic systems attempting to mimic synaptic plasticity mechanisms. Therefore, reversible polarization states, hysteretic effects, and history-dependent behaviors exhibited by non-linear ferroelectrics present versatile functionalities that can greatly complement semiconductor devices for upcoming memory and computing applications, provided challenges associated with film quality, device integration, and variability can be effectively mitigated through continued research.

2.3 Material Synthesis

Synthesis of the ceramics and the targets for the thin film's deposition were done with conventional solid-state route and thin films for studying gate-oxide and memory applications were prepared by the PLD techniques.

2.3.1 Bulk Ceramics and Targets

Electro-ceramics are typically fabricated by ‘ceramic processing’ - synthesizing oxide powder precursors first and then consolidating them into a dense material using calcination/sintering heat treatments. Multiple chemical and physical routes exist for synthesizing ceramic powders. Conventional solid-state reaction involves high-temperature calcination of a stoichiometric mixture of powder reactants to promote diffusion and reaction. However, this often results in powders with non-uniform morphology and large particles. Wet chemical methods like sol-gel synthesis, hydrothermal/solvothermal techniques, electrodeposition, and precipitation aim to overcome these issues by enabling better mixing and reaction at the molecular levels in suitable solvents [67-69]. Further, lower temperatures limit excessive grain growth. However sufficient drying and decomposition of the intermediate compounds into the desired ceramic oxide phase requires careful thermal processing. Advanced powder synthesis techniques can create complex nanostructured particles and ceramic-polymer nanocomposites with precisely tailored size, shape, porosity, and orientation to tune bulk properties after sintering.

2.3.2 Ceramic Thin films

The thin film deposition encompasses a variety of material synthesis methods designed to create functional coatings with thicknesses ranging from sub-nanometer levels to several micrometers. The ability to precisely control growth kinetics during deposition allows us to produce thin films with specific chemical stoichiometry, microstructural phases, and tailored physical properties. Thin film deposition methods are broadly categorized into techniques such as Physical Vapor Deposition (PVD), Chemical Vapor Deposition (CVD), Molecular Beam Epitaxy (MBE), Atomic Layer

Deposition (ALD), solution-based approaches, and combinations of these methods [91]. PVD techniques involve transferring material from a solid phase to a vapor phase through thermal or plasma-based evaporation, followed by condensation onto substrates. Methods like sputtering, Pulsed Laser Deposition (PLD), cathodic arc deposition, electron beam evaporation, and thermal resistive evaporation are widely used due to their simplicity, low processing temperatures, and precise control over film composition [91]. For instance, sputtering, where target atoms are ejected due to ion bombardment, is extensively applied in depositing thin films for microelectronics, optics, and magnetic storage. However, challenges such as low deposition rates and stoichiometric variations during the sputtering of insulating oxide films led to the development of PLD, particularly for multicomponent insulating films [91]. PLD was initially developed to study high-temperature complex ceramic oxides, especially superconducting films that require precise stoichiometric transfer from target to film. Its applications have since broadened to include epitaxial oxides like ferroelectrics, multiferroics, dielectrics, magnetics, phosphors, metals, and oxynitrides, which are utilized in devices spanning sensors, electronics, energy, and photonics. PLD's ability to manipulate film chemistry at the atomic scale has made it a vital tool in researching artificial superlattices and heterostructures of complex oxides. Recent breakthroughs have demonstrated its potential in creating interfacial couplings between ferroelectricity, magnetism, and orbital reconstructions in artificial multiferroic thin films, offering new pathways for next-generation memory devices with efficient electric control of magnetism. Efforts to extend PLD's commercial viability include developing techniques for large-area deposition, such as combining PLD with secondary plasma activation to improve uniformity and density across expanded

surfaces. These advancements target applications in electronics manufacturing. Supported by innovations in laser technology, scanning methods, and in-situ monitoring, PLD has remained an indispensable tool for material discovery and thin film engineering. The PLD process is unique due to its highly non-equilibrium nature. A high-power pulsed laser beam focused on a target material, typically a dense pellet, generates a luminous plasma plume containing vaporized material. This ejected plume comprises a thermalized mixture of ions, electrons, atoms, molecules, and particulates that traverse a controlled environment to deposit onto a heated substrate. Optimal substrate temperatures (500–850°C) [91] enable layer-by-layer deposition while key parameters such as laser pulse energy density, target-substrate distance, and background gas pressure govern film properties like thickness, density, and microstructure. By leveraging its rich tunable parameter space and versatility, PLD continues to play a pivotal role in advancing materials science and enabling the development of cutting-edge devices. PLD systems typically include several components critical to the process. The **target holder** secures the high-purity material to be abated by the laser, while the **substrate holder** mounts the substrate, usually a wafer, onto which the thin film is deposited (Mi). The **vacuum chamber** ensures a clean environment free from contamination, and the **laser** provides high-energy pulses necessary for material ablation. During ablation, the vaporized material forms a **plasma plume** that condenses onto the substrate, and a **substrate heater** can be used to enhance film adhesion and crystallinity. Additionally, a **pressure control system** is employed to maintain optimal vacuum conditions during deposition. By leveraging its rich tunable parameter space and versatility, PLD continues to play a pivotal role in

advancing materials science and enabling the development of cutting-edge devices (**Figure 2.2**).

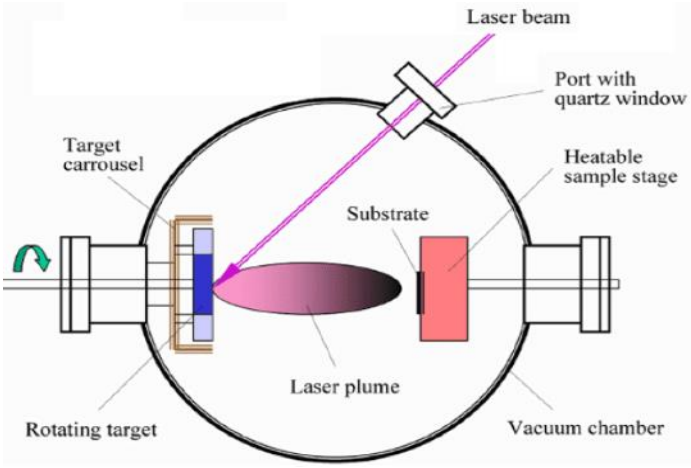


Figure 2.2 The Schematic of PLD [45].

2.4 Material Characterization

The structural, microstructural, spectroscopic, electrical, and ferroelectric properties of the fabricated nanostructures were characterized using various advanced techniques, described in the following sections. Moreover, an understanding of the surface, interface, and growth modes of high-*k* dielectrics and ferroelectrics is of fundamental interest for the fabrication of devices where high-*k* dielectric and ferroelectric materials are used. The characterizations performed provide critical information to understand, optimize, and enhance material properties of the materials for the targeted applications.

2.4.1 Structure

The diffraction of electromagnetic waves or particles (electron, proton, neutron) allows the study of the detailed structure of matter if the wavelength is comparable to the distance between the atoms or the molecules. For a periodic structure the

constructive interference of the scattered wave results in sharp diffraction peaks at diffraction angles (2θ) as determined by Bragg's law (equation 2.1):

$$2d \sin\theta = n\lambda \qquad \text{……..2.1}$$

Where, d is the distance between atomic layers in a crystal, and the variable λ is the wavelength of the incident X-ray beam and n is the integer for the order of the diffraction. Diffraction patterns only occur when the distance traveled by the rays reflected by the successive planes differs by several n wavelengths. Identification of the various crystalline phases is achieved by comparing the X-ray diffraction pattern obtained from the sample under study with the database of the Joint Committee on Powder Diffraction Patterns (JCPDS) maintained by the scientific organization named International Centre for Diffraction Data. In this work, structural properties were examined by X-ray diffraction [XRD, Siemens D5000]. X-ray diffractograms were recorded using CuKα 1.5405Å beam line with 2θ typically in the range 20 to 60° with a scan speed of 3 degrees/minute and slit width of 1 mm. The various peaks correspond to various crystallographic planes. Generally, these planes are represented as <hkl>, where h, k and l are the miller indices along the x, y and z direction. These planes of the powder, film and substrates were identified using the JCPDS files already existing with the obtained X-ray diffraction patterns [92]. The structural evolution of the compound was studied as a function of temperature. The average crystallite size (d_k) of the ceramics can be determined using the Bragg peaks using the Scherrer equation from the Full Width at Half Maxima (FWHM) as follows (equation 2.2):

$$d_k = \frac{K\lambda}{\beta \cos\theta} \qquad \text{.....2.2}$$

where d_k, is the average grain size, K is the shape factor (typically around 0.9), λ is the wavelength of X-ray radiation (1.5405 Å), β(θ) is the full width at half maximum (FWHM) of the peak at angle θ, and θ is the Bragg angle corresponding to that peak.

2.4.2 Morphology and Composition

Surface morphology of bulk ceramics and thin films have been studied using scanning electron microscopy and atomic force microscopy. The composition of the synthesized ceramics and thin films were analyzed with Energy Dispersive X-Ray Spectroscopy (EDS) technique. These methods are briefly discussed in the following sub sections.

2.4.2.1 Scanning Electron Microscopy

Scanning Electron Microscopy (SEM) stands as a revolutionary technique in nanoscale imaging, providing intricate details and surface information of samples under study. Unlike optical microscopy, SEM utilizes a focused electron beam, enabling resolutions below 1 nanometer, making it an invaluable tool for scientific research and industrial applications. The decision to use electrons in SEM over light stems from the electron's shorter wavelength, as dictated by the de Broglie relationship. This results in superior resolving power, crucial for exploring structures at the atomic and nanometer scales. The wavelength of fast electrons (λ) in SEM is determined by the accelerating voltage (V) (equation 2.3):

$$\lambda = \frac{h}{\sqrt{2meV}} \qquad \text{.....2.3}$$

Where, h is the Planck's constant, m is the mass of the electron and e is the electronic change. In SEM (**Figure 2.3**), a focused electron beam scans over a specimen's surface, eliciting various signals upon interaction. Two common detectors are Secondary Electron Detectors (SED) and Backscattered Electron Detectors (BSD). Additionally, Energy Dispersive Spectroscopy enables elemental analysis. The components in SEM, including the electron source, lenses, scanning coil, detectors, and sample chamber, collectively contribute to the system's functionality.

The resolving power of SEM is influenced by factors like the beam spot size and interaction volume. Theoretical resolution in SEM (δ) is influenced by the incident wavelength (λ) and is given by the relation (equation 2.4):

$$\delta = 0.61\frac{\lambda}{\mu \sin \beta} \qquad \text{……..…..2.4}$$

Here, μ is the refractive index, and β is the semi-angle of the microscope's numerical aperture.

Backscattered Electron Detector (BSD) (**Figure 2.4**) plays a crucial role in SEM by detecting elastically scattered electrons. These electrons, originating from below the sample surface, carry higher energy. While BSD images may have lower resolution compared to those acquired with an SED, the BSD offers advantages, such as the ability to operate at lower vacuum levels, reducing sample preparation requirements, and minimizing beam damage.

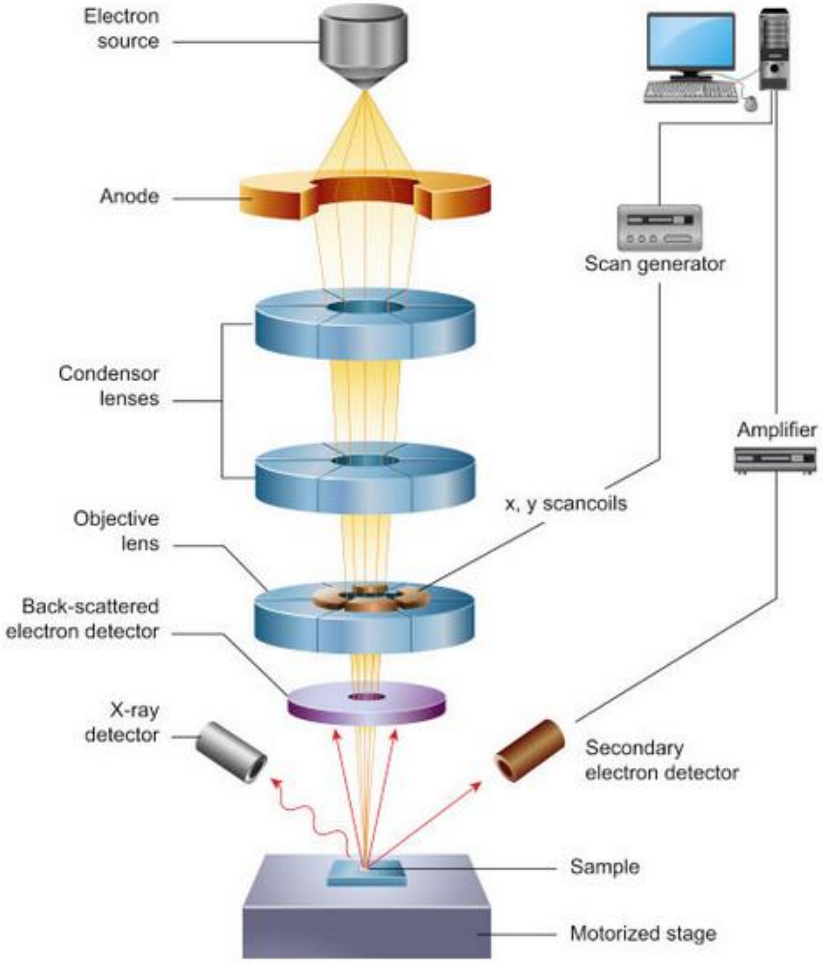


Figure 2.3 Schematic diagram of the SEM [45, 91].

Backscattered electrons exhibit variation in both amount and direction, influenced by the specimen's composition and topography. The contrast in BSD images depends on factors such as the atomic number (Z) of the elements in the sample material, the acceleration voltage of the primary beam, and the specimen angle (tilt) concerning the primary beam. Higher Z elements yield more backscattered electrons.

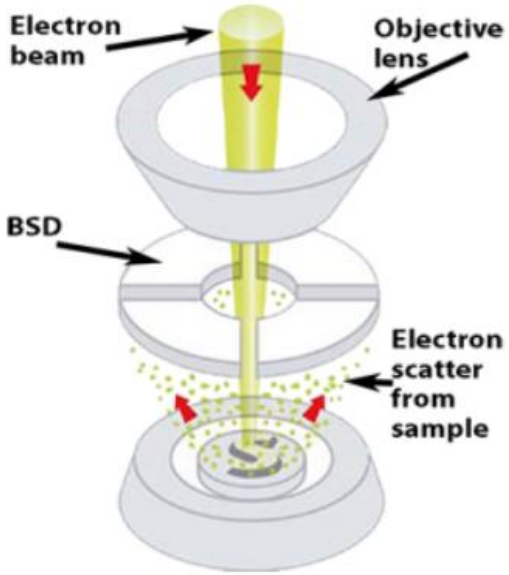


Figure 2.4 Backscattered Electron Detector [45, 67, 78].

In contrast to BSD, the Secondary Electron Detector (SED) offers images with resolution independent of the material's composition. SED images provide a visualization of inelastically scattered electrons generated close to the sample surface, offering topographical information with the best possible resolution. However, SED images do not provide material composition information. Secondary electrons are detected using an Everhart-Thornley (E-T) detector. This detector consists of a scintillator inside a Faraday cage, positioned above the sample. A positive bias is applied to the Faraday cage to attract low-energy electrons. The scintillator converts these electrons into light (photos), which are then amplified using a photomultiplier tube to yield the final signal.

Energy Dispersive Spectroscopy capitalizes on characteristic X-rays emitted during SEM imaging. It is a fast, accurate, and non-destructive method for identifying elemental composition at the micron scale. Characteristic X-rays are emitted when the

electron beam displaces an inner shell electron and replaces it with an outer shell electron. EDS data can be obtained at a point, along a line, or mapped over an area. The Silicon Drift Detector (SDD) is a common EDS detector in SEM instruments. It generates electron-hole pairs by absorbing X-rays. Measuring the charge generated in the detector provides a spectrum of signal intensity vs. X-ray energy, allowing the identification of almost all elements and the atomic percentage of each element in the compounds. So, EDS can be used for the determination of the composition of the samples. The thin window in SDDs acts as a barrier, maintaining appropriate vacuum levels during sample exchange.

In the thesis, the Field Emission Scanning Electron Microscope (FE-SEM) at **Lovely Professional University**'s Central Instrumentation Facility was used combining a semi-in-lens objective lens and an in-lens Schottky Field Emission Gun. Its Gentle Beam mode enhances resolution, allowing observation of the topmost surface at extremely low voltages. Equipped with energy-dispersive X-ray spectrometry and BSD system, the FE-SEM detects elements down to boron and provides crucial information about morphology and composition.

2.4.2.2 Atomic Force Microscopy

The Atomic Force Microscope (AFM) system, illustrated in **Figure 2.5,** is a powerful tool employed for imaging the topography of sample surfaces. At its core, the AFM utilizes a sharp tip mounted on a cantilever, which systematically scans over the sample's surface. The interaction between the tip and the sample induces deflections in the cantilever, and these deflections are precisely monitored. A laser, reflected onto a four-quadrant photodiode detector, detects these deflections. The sample under investigation is strategically positioned on a macro-positioner, a piezoelectric scanner

that enables movement in three dimensions: along the "Z" direction for maintaining contact force and in the "X-Y" plane for scanning purposes.

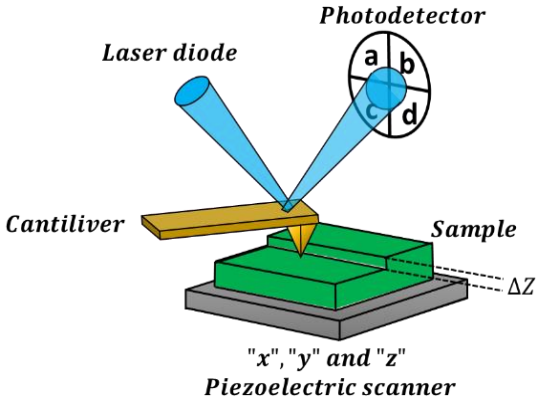


Figure 2.5 The fundamental setup of the AFM system, with the cantilever-mounted tip scanning the sample surface [93].

The AFM operates in three distinctive modes: contact, non-contact, and tapping modes, each selected based on the specific forces governing the tip-sample interaction. In contact mode, the probe and surface maintain proximity, and the dominant forces are repulsive. This model is represented by the red line in **Figure 2.6**. Dynamic mode, on the other hand, features a slightly increased probe-sample distance in the order of nanometers, and Van der Waals interactions become the dominant force (blue line in **Figure 2.6**). In non-contact mode, the probe-sample distance is even larger, reaching tens of nanometers, and the weak probe-sample forces are too subtle to be detected by the system (green line in **Figure 2.6**).

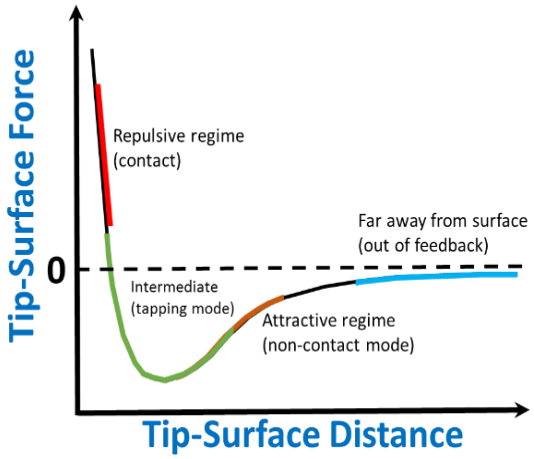


Figure 2.6 The repulsive and attractive force regimes as the AFM tip approaches the sample, depict the transition from repulsive forces in contact mode to attractive forces in non-contact mode [93].

When the electron beam strikes the sample surface, it penetrates to a few microns, interacting with atoms. The interaction volume depends on the accelerating voltage and sample density. Signals like secondary electrons, backscattered electrons, and characteristic X-rays are generated, providing valuable information about topography and composition. The surface morphology of the films was studied in terms of root mean square roughness using AFM.

2.4.3 Electrical properties

The thin capacitors were prepared with the deposition of platinum electrodes on the surface of the film to form in MIM and MIS test structures for the metallic and semiconducting substrates, respectively. The top electrode is deposited using DC sputtering to 100-500 µm in diameter through a shadow mask shown in **Figure 2.7**.

The damage in the film due to the sputtering process was compensated with an additional ex-situ post-annealing step in an oxygen ambiance.

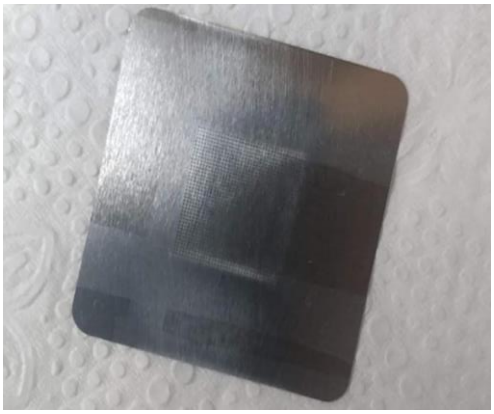


Figure 2.7 The shadow mask used for the top electrode deposition in the Quantum Lab, CSIR- National Physical Laboratory, Delhi.

2.4.3.1 Polarization-Electric field (P-E) measurement

The ferroelectric hysteresis loops of the thin film and bulk ceramics were obtained using a ferroelectric measurement system RT6000 HVS, from Radiant Technologies Inc, USA. The most important characteristic of ferroelectric materials is polarization reversal (or switching) by an electric field. One consequence of the domain-wall switching in ferroelectric materials is the occurrence of the ferroelectric hysteresis loop as shown in **Figure 2.8** [94]. The hysteresis loop can be observed experimentally by using a Sawyer–Tower circuit. At small values of the AC electric field, the polarization increases linearly with the field amplitude, according to relation (equation 2.5):

$$P_i = \chi_{ij} E_i \qquad \text{…….2.5}$$

Where, *Pi*: Polarization vector of the material, *χij*: Susceptibility tensor, representing the material's response to an electric field, and *Ej*: Electric field vector applied to the material.

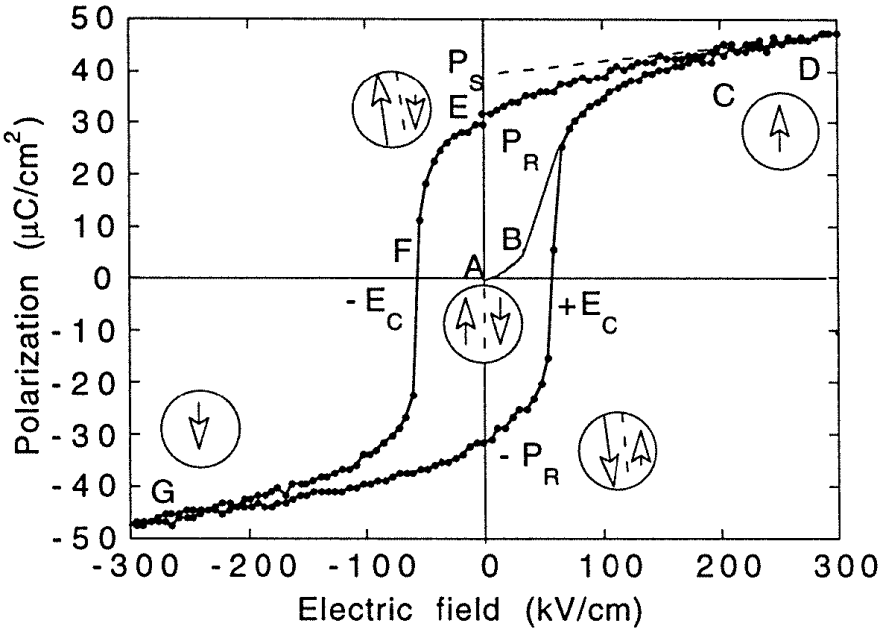


Figure 2.8 P- E hysteresis and dipole orientation at different fields and polarization conditions [94].

This corresponds to segment AB in **Figure 2.8**. In this region, the field is not strong enough to switch domains with the unfavorable direction of polarization. As the field increases the polarization of domains with an unfavorable direction of polarization will start to switch in the direction of the field, rapidly increasing the measured charge density (segment BC). The polarization response in this region is strongly nonlinear and the equation mentioned above is no longer valid. Once all the domains are aligned (point C) the ferroelectricity again behaves linearly (segment CD). If the field strength starts to decrease, some domains will back-switch, but at zero field the polarization is

non-zero (point E). To reach a zero polarization state the field must be reversed (point F). Further increase of the field in the negative direction will cause a new alignment of dipoles and saturation (point G). The field strength is then reduced to zero and reversed to complete the cycle. The value of polarization at zero field (point E) is called the remnant polarization, P_R. The field necessary to bring the polarization to zero is called the coercive field, E_C. The spontaneous polarization P_S is usually taken as the intercept of the polarization axis with the extrapolated linear segment CD. (Strictly speaking, in polycrystalline materials true spontaneous polarization equal to that of a single crystal can never be reached and it is more correct to speak of saturated rather than of spontaneous polarization.) It should be mentioned that the coercive field E_C that is determined from the intercept of the hysteresis loop with the field axis is not an absolute threshold field. If a low electric field is applied over a (very) long period, the polarization will eventually switch. An ideal hysteresis loop is symmetrical so that $+E_C = -E_C$ and $+P_R = -P_R$. The coercive field, spontaneous and remanent polarization, and shape of the loop may be affected by many factors including the thickness of the film, the presence of charged defects, mechanical stresses, preparation conditions, and thermal treatment.

The RT6000 HVS, from Radiant Technologies mentioned before, uses the Sawyer-Tower Circuit in **Figure 2.9**. The modification made to the Sawyer-Tower circuit in the RT6000 HVS system involves the implementation of a virtual ground to reduce noise during ferroelectric measurements. This adjustment enhances the accuracy of polarization-electric field (P-E) hysteresis loop measurements by minimizing interference and thus ensuring measurement system stability. By applying a virtual

ground, the circuit can achieve better signal integrity, which is crucial for capturing the subtle changes in polarization that occur during hysteresis loop measurements.

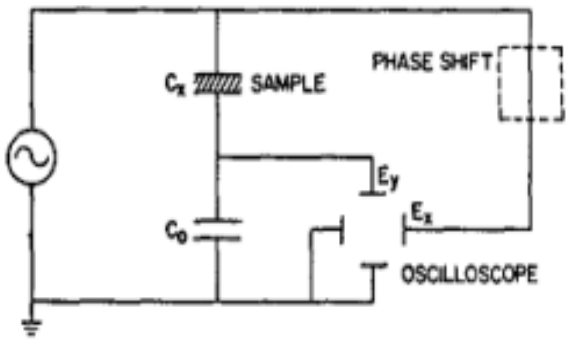


Figure 2.9 The Original Sawyer-Tower circuit for measuring a sample of material [95].

2.4.3.2 Dielectric constant and loss tangent

The permittivity and the tan δ of the thin film capacitors and bulk ceramic capacitors were determined by measuring the capacitance and loss tangent at different bias voltages with the impedance analyzer HP4294A from *Hewlett Packard*. The terminals consist of four coaxial connectors and have the advantage of performing both low and high-impedance measurements. The H_p and L_p lines are currently free and cannot cause measurement errors. Regarding H_c and L_c, the same current flows through the central conductor and the outer shield, so that the inductive magnetic fields generated cancel each other thus prohibiting any error due to self or mutual conductance between the conductors. The **Hp** and **Lp** lines refer to the high-frequency and low-frequency impedance paths in the measurement setup. These lines are left floating, meaning they are not connected to a reference ground or another circuit point.

Floating nodes can sometimes be necessary to prevent ground loops or interference from other components in the measurement system. However, leaving nodes floating can introduce measurement uncertainties or noise if not properly managed. In general practice, floating nodes should be avoided unless there is a specific reason for doing so, as they can lead to unpredictable behavior in sensitive measurements. It is essential to ensure that any floating connections do not adversely affect the accuracy of the impedance measurements.

The signal level U_m across the unknown impedance Z_x in a simplified model depends on the oscillator voltage level V_{osc} and the source resistance R_{so} of the HP4294A, which is approx. 100Ω (equation 2.6):

$$|U_m| = \frac{|Z_x|}{|R_{so} + Z_X|} \times |V_{osc}| \qquad \text{.....2.6}$$

The $|U_m|$, is the measured voltage across the unknown impedance; $|Z_x|$, is the impedance of the device under test; $|R_{so}|$, the source resistance of the impedance analyzer (approximately 100Ω); $|V_{osc}|$, is the oscillator voltage level. Because of the high impedance of the thin film capacitor the signal level is equal to the adjusted oscillator level and an amplitude of V_{osc}=50 mV was found appropriate for most cases in the case of thin films (thickness (d) less than 150 nm). However, thicker sample V_{osc} has been increased upto 1 V to obtain the sufficient electric field (E=V/d). The frequency used for the measurement varies between 100 Hz and 1 MHz.

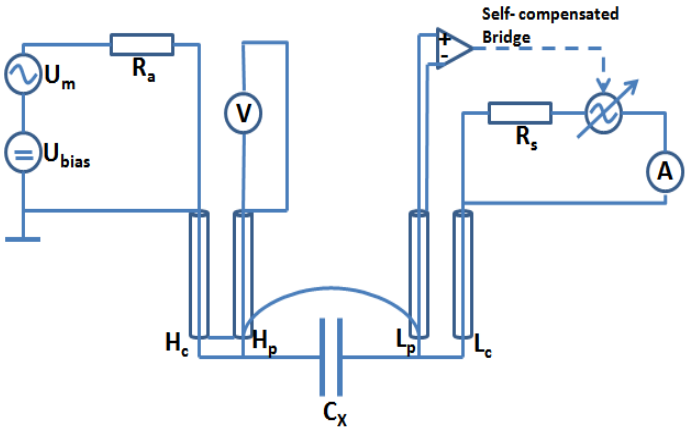


Figure 2.10 The measurement principle of the HP 4294A impedance analyzer with four-terminal pair configuration Cx represents the device under test (DUT).

After contacting a sample, a current flow and the voltage drop on the shunt resistance R_s are measured and brought to zero after the generation of an opposite-directed compensation current. From the amplitude difference and the phase shift between the measuring voltage and the compensation current the device calculates the complex admittance or impedance. In **Figure 2.10**, Voltmeter is connected to the inner cable of the coaxial cable and to the outer covering which is grounded so that voltage is measured across the sample. The figure shows the complete measurement set up which includes the provisions for open and short circuit corrections to be done before any measurement is taken. Shorting and opening the terminals for the corrections allows the accurate measurement of the impedance characteristics of the device under test. The capacitance of the sample C_p (parallel capacitance), where R_p (parallel resistance) is considered and can be calculated using the following equation 2.7,

$$C_p = \frac{1}{V_{bias} + U_m} \int I.dt \qquad \text{.....2.7}$$

Where C_p the capacitance of the sample; V_{bias}, the bias voltage applied to the sample; U_m measures voltage across the sample, and *I is*, Current flowing through the sample. The bias voltage V_{bias} and measuring voltage U_m are typically measured at the terminals of the thin film capacitor during testing. These voltages are crucial for calculating capacitance and understanding the behavior of the capacitor under different electrical conditions. The signal level U_m across the unknown impedance Z_x can be expressed as **equation 2.6**. The complex admittance Y can be expressed, Y= G+ jB*Y, w*here Y is complex admittance; *G is conductance* (real part); B is susceptance (imaginary part). The relationship between admittance and impedance is given by: Z=1/Y, were, *Z*: Impedance of the device under test. The subscript 'p' denotes parallel and C_p is the parallel capacitance of the unknown sample capacitance in the equivalent electrical circuits shown in **Figure 2.11**. C_p matches the capacitance C_x of the DUT.

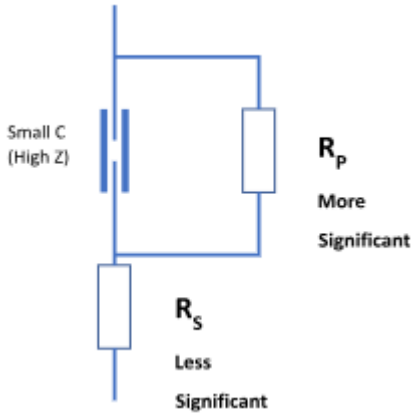


Figure 2.11 An equivalent electrical circuit representing the measurement components of a capacitor.

The lateral dimensions of the samples, e.g. round electrodes with diameter φ= 200µm, are many orders of magnitude larger than their thickness (~100 nm), and at

intermediate frequencies, they can be considered as ideal planer capacitors. The permittivity of the sample is then (equation 2.8):

$$\varepsilon_r = \frac{C_p t}{E_0 A} \qquad \text{……2.8}$$

Where ε_0= 8.854 x 10^{-4} As/Vm is the dielectric constant of vacuum, t is the thickness, and A the surface area of the unknown sample. The following equation shows the definition of the dissipation factor (tan δ or D), which is the ratio of the imaginary part of the permittivity to the real part (equation 2.9):

$$\tan\delta = \frac{I_m(\varepsilon_r)}{R_P} = \frac{XC_P}{R_P} = \frac{1}{2\pi C_P R_P} \qquad \text{……2.9}$$

X_{Cp} (=1/jωC, ω=angular frequency), represents the reactance of a circuit including a capacitor and a resistance. In the case of thin film capacitors with a small capacitance in the order of nF or below, the representative circuit can be seen in **Figure 2.10**. The reactance at a given frequency is relatively large and the parallel resistance (R_p) becomes more significant than the series component (R_s). Hence, the complex form of permittivity can be derived from the equation 2.10:

$$\varepsilon_r = \mathrm{Re}(\varepsilon_r) + jI_m(\varepsilon_r) = \frac{t}{\varepsilon_0 A}(C_p + \frac{1}{2\pi f.R_p}) \qquad \text{……2.10}$$

If R_s (series resistance) is less significant due to the relatively high capacitive reactance, then C_p and R_p are measured. On the other hand, R_p is less significant due to low reactance of capacitors (high capacitance value, X_{cs}=1/jωC, then C_s (series capacitance) and R_s are measured.

The loss tangent and capacitance of the high-*k* dielectrics were measured in the frequency range from 10^2 to 10^6 Hz. C_p and tangent loss were measured as a function of frequency from 100 Hz to 1 MHz. The resistor thermal noise dominates at lower frequencies (<100 Hz) whereas lead inductance with the capacitance introduces resonance ($f_r = 1/\sqrt{LC}$), where f_r is the resonant frequency of the test circuit, L -the lead inductance and C the capacitance of the DUT) introduce noise above 1MHz. Source voltage of 50 mV was applied during the measurements. This voltage level is typically sufficient to produce the desired electric field across the thin film capacitor, depending on the capacitor's dimensions and capacitance value. The applied voltage must be adequate to ensure that the electric field is strong enough to induce measurable polarization without exceeding the breakdown voltage of the material.

2.4.3.3 Capacitance -Voltage (C-V) Measurement

For electrical measurements of gate-oxides, eutectic paste is concerned physically to accomplish an ohmic backside contact. The subsequent film stack is Pt/ high-*k* /pSi/$Ga_{0.85}In_{0.15}$. C-V curves are evaluated at a frequency of 1 MHz using the same impedance analyzer used for the dielectric measurements. The C-V characteristics of the MIS can give information about the interface states, oxide charges, ion transport through the insulator and the silicon doping profile and is extensively used for characterizing the insulating films and semiconductor surface. These measurements were done at different frequencies of the ac signal superimposed on the dc bias field. From the C-V curve the capacitance in accumulation (C_{ox}) was used for the determination of equivalent oxide thickness of the high-*k* material (typical SiO_2 dielectric thickness for the same capacitance) using the relation (equation 2.11):

$$C_{ox} = \frac{A\varepsilon_0\varepsilon_r}{t_{ox}},$$

$$\frac{A\varepsilon_0\varepsilon_{rSio_2}}{t_{ox}} = \frac{A\varepsilon_0\varepsilon_{high-k}}{t_{ox_e}},$$

$$t_{Sio_2}(EOT) = \frac{\varepsilon_{high-k}}{\varepsilon_{Sio_2}(=3.9)} t_{ox}$$

……2.11

where, $\varepsilon_{high\text{-}k}$, $t_{high\text{-}k}$, A, and ε_0 are the dielectric constant and thickness of the high-*k* material, area of the top electrode, and permittivity of the vacuum respectively. In the case of high-k dielectric in the MIS configuration, measurement of capacitance starts with the sweeping DC bias voltage from + 4 to – 4 Volt and back to +4 Volt (depending on the thickness of the high-k oxides to ensure complete accumulation and inversion) to form a complete cycle. Here the AC voltage is used to measure the capacitance which is then plotted as a function of the DC bias field at a given frequency, giving rise to a *C–V* graph as shown in **Figure 2.12**. The C-V graph thus obtained has been used for the determination of, equivalent oxide thickness flat band voltage (V_{FB}) and the trap density in the oxide and at the interface [6, 7].

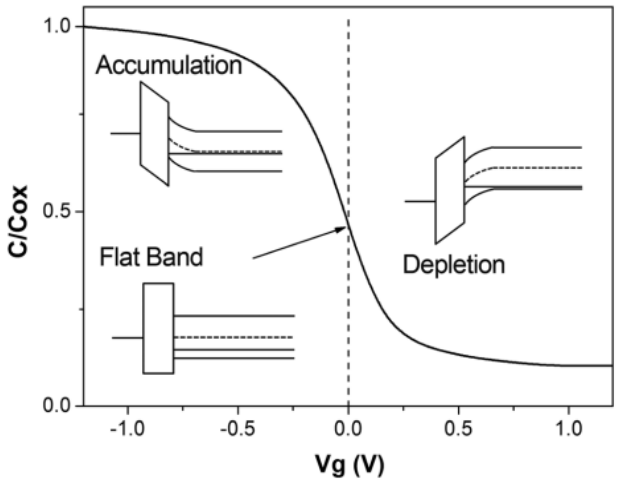


Figure 2.12 Ideal high-frequency (10 kHz to 1MHz) curve of the MIS device based on p-type silicon, showing accumulation, flat band and inversion regions used for the determination of equivalent oxide thickness and Flat-band voltage (V_{FB}) of the MIS/or MOS capacitor [96].

When negative bias is applied to the gate, positive charges (holes) from the p-type semiconductor and they get accumulated at the oxide-semiconductor interface. Under this condition the high frequency capacitance is equal to the parallel plate capacitance and is equal to capacitance (equation 2.11) . This is the accumulation condition. A reduction in negative voltage reduces the accumulated charges. As the bias changes from the negative to positive voltages, the positive charges are repelled from the interface and the region will be depleted of majority carriers (holes in the case of p-type semiconductors. This is called the depletion region. As the positive voltage increases, depletion width increases, and the capacitance decreases. In this case, the depletion region is devoid of any mobile charge carriers, and the region will be in a non-equilibrium state. The semiconductor then tries to re-establish the equilibrium by generating electron-hole pairs, and the electrons accumulate near the semiconductor-oxide interface. This creates an inversion region. The inversion prevents further depletion; the capacitance remains to a minimum value (C_{min}) depending on the dopant concentration. If sufficient time is not given for the electron-hole pairs generation during the voltage sweep, inversion cannot occur, and depletion continues to a state of deep depletion. These are schematically shown in **Figure 2.13.**

The sweep rate is a concern in C-V measurements as the slow sweeper rate is not practical due to time issues in a production environment and fast sweeper rate results

in deep depletion. To overcome these difficulties, C-V was swept from inversion to accumulation and back to inversion after a stable inversion conduction is established.

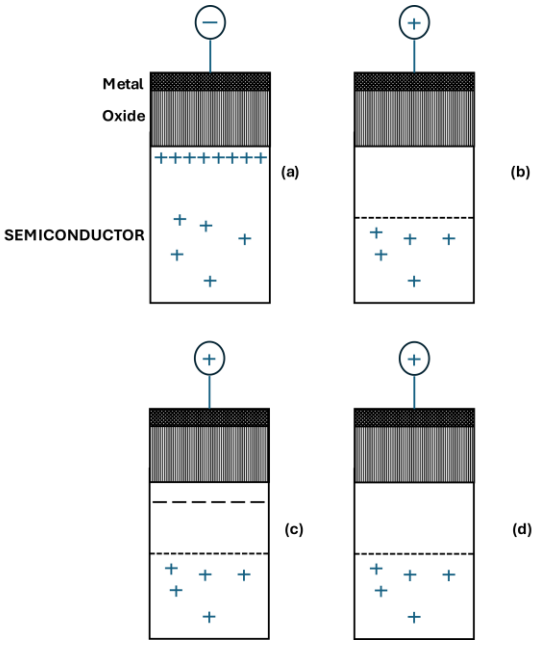


Figure 2.13 Representation of (a) accumulation, (b) depletion, (c) inversion and (d) deep depletion during the voltage sweep in the C-V characteristics of P-type(n-channel) MOS devices.

2.4.3.4 Leakage current (J-V) Measurement

The current retort of the charging ceramic capacitor (polarization) and discharging (depolarization) current is time dependent as the model. The plots obtained can be categorized into three sections: the relaxation current regime, the leakage current regime, and the degradation or breakdown regime [6]. Measuring the current retort of a charging ceramic capacitor involves a series of steps to capture the time-dependent behavior of charging (polarization) and discharging (depolarization) currents. The measurement of a ceramic capacitor's behavior typically involves several stages,

starting with preparation. The experimental setup includes a power supply, a Digital Multimeter (DMM) or oscilloscope, and the capacitor to be tested. All connections must be secure, and the capacitor should be correctly connected to the measurement instrument to ensure accurate reading. The process begins with the charging phase, where a voltage is applied across the capacitor's terminals using the power supply. Starting with a low voltage, the applied voltage gradually increased to the desired level. During this phase, polarization current flows into the capacitor, causing it to accumulate charge. The charging behavior is monitored using a digital multimeter or oscilloscope, which records the current flowing through the capacitor over time. This data provides insights into charging dynamics and how the current evolves during the process. The next step is the analysis of the measured data to identify different regimes of current behavior.

The relaxation current regime is observed as an initial rapid decrease in current as the capacitor charges. The leakage current regime, on the other hand, represents the steady-state current that flows due to imperfections in the dielectric material. Additionally, a degradation or breakdown regime may be identified if the capacitor fails under excessive voltage or stress conditions.

Following the charging phase, the depolarization phase begins. The power supply is disconnected, allowing the capacitor to discharge. During this phase, the depolarization current—representing the current flowing out of the capacitor as it releases its stored charge—is measured. Analyzing this data reveals the capacitor’s discharge characteristics and energy storage behavior.

To ensure the reliability of the results, the measurements are repeated multiple times under varying conditions, such as different voltage levels and temperatures.

Comparing these data sets helps identify consistent trends and detect any anomalies, providing a comprehensive understanding of the capacitor's performance across different operating conditions. The leakage current through the sample was measured using the set up shown in **Figure 2.14**. By following steps and carefully analyzing the obtained data, a comprehensive understanding of the charging and discharging behavior of ceramic capacitors over time can be obtained. This knowledge is essential for optimizing the capacitor performance and reliability in various electronic applications.

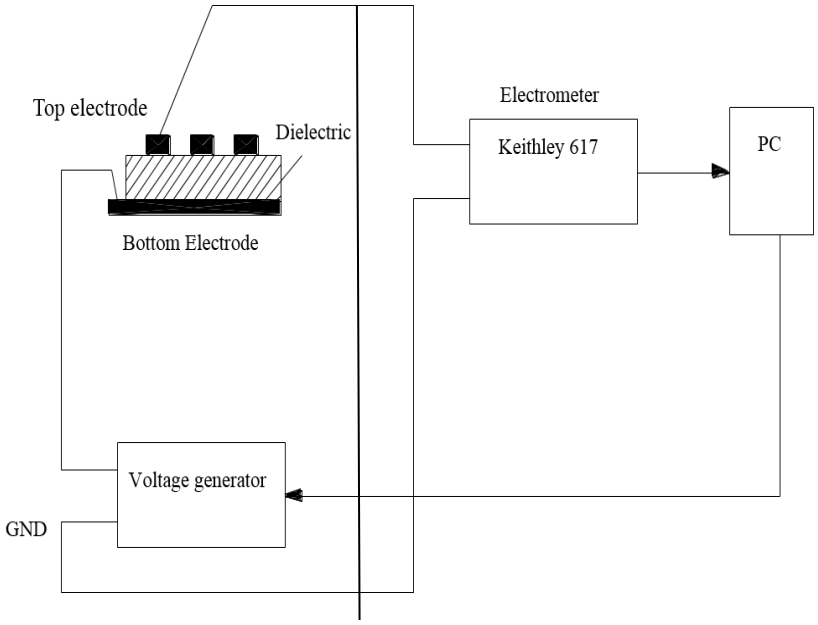


Figure 2.14 Measurement setup for leakage current investigation.

CHAPTER 3

LOGIC DEVICES – BULK CERAMICS AND CERAMIC THIN FILMS

HfO_2 and ZrO_2 have been explored in bulk and thin film form for more than a decade for various electronic applications, especially in DRAM and logic devices due to the high-*k* dielectric constant compared to SiO_2. However, there have been no reports of Dy and Ta co-substituted with HfO_2 and ZrO_2, which may enhance the dielectric properties of (Hf, Zr) O_2, especially relative dielectric permittivity (ε_r) for the next generation of logic devices. Thus, in this chapter, an analysis of Dy and Ta substitution for three different ceramic compositions [Hf_x, $Zr_{0.8-x}$) (Ta, Dy)$_{0.1}O_2$ with $0.2 \leq x \leq 0.6$] are presented. Pellets of ceramics were prepared, and structural, morphological, and electrical properties were analyzed to find the optimum composition for the gate-oxide applications. The high-*k* materials in the ultra-thin film form are a major task by the problem as it involves the material's need to have high resistivity, be thermally stable [97], act as a good barrier, and have an ideal interface with silicon. This aspect of the thin film with Si-substrate will also be discussed in this chapter.

3.1 (Hf_x, $Zr_{0.8-x}$) (Ta,Dy)$_{0.2}O_2$ ceramics

Stoichiometric (Hf_x, $Zr_{0.8-x}$) (Ta, Dy)$_{0.1}O_2$ ceramics were prepared with $0.2 \leq x \leq 0.6$ using conventional solid-state reaction techniques (**Appendix-A**). The ceramic oxide powders of HfO_2 (99.9%), ZrO_2 (99%), Ta_2O_5 (99%), and Dy_2O_3 (99.9%) were procured from Alfa-Aesar. These precursors were weighed about to their mole

fractions/stoichiometric percentages for three different compositions: (a) $Hf_{0.2}Zr_{0.6}Ta_{0.1}Dy_{0.1}O_2$, (b) $Hf_{0.4}Zr_{0.4}Ta_{0.1}Dy_{0.1}O_2$, and (c) $Hf_{0.6}Zr_{0.2}Ta_{0.1}Dy_{0.1}O_2$ and were mixed and were mixed. These white powders underwent physical mixing for 2hr in alcoholic standard (Isopropyl alcohol) in pestle-mortar for homogeneous amalgamation independently for three compositions. The powder combinations were dried out and then calcined at a temperature of 1200°C for 4 hours in an alumina crucible in the muffle furnace **(Appendix-B**) with a 5°C/min heating rate. After cooling to room temperature, the calcined powder was further grounded and sieved for the preparation of ceramic pellets. The powders of $(Hf_x, Zr_{0.8-x})(Ta, Dy)_{0.2}O_2$ (where x= 0.2, 0.4, 0.6) thus obtained were mixed with 7 wt% polyvinyl alcohol which acted as the binder to form the pellets. Isopropyl alcohol (IPA) was chosen as the solvent for mixing due to its excellent solvating properties [95, 97], which facilitate the dissolution of metal oxide precursors like HfO_2, ZrO_2, Ta_2O_5, and Dy_2O_3. IPA is also advantageous because it evaporates quickly, minimizing residue that could interfere with subsequent processing steps. The slurry thus obtained with isopropyl alcohol, polyvinyl alcohol and dried powders. This dried powder is then uniaxially pressed into circular pellets of diameter having ~10 mm and thickness ≤1.5 mm using a hydraulic press **(Appendix-C)** with a pressure 100 MPa. The pellets are then sintered at an optimized temperature of 1400°C for 4 hr in a chamber furnace at 8ºC/min to get 90% - 95% of the theoretical density. The obtained ceramic pellets were used for the bulk characterization after cooling. The structure of the as-prepared pellets is analyzed by the high-resolution powder XRD techniques using Bruker D-8 X-ray Diffractometer with nickel-filtered Cu K_α radiation (wavelength =1.54Å). The materials thus synthesized are examined using a JEOL IT800 field emission scanning

electron microscope for surface morphology. For the electrical measurement, the top and bottom surfaces of the pellet (covering the entire region) were painted with conducting silver paint. These were then dried at 150°C for 30 minutes to remove moisture, if any, and then cooled to Room Temperature (RT) before taking any electrical dimension. The measurement of the capacitance (for calculating ε_r) *and* tangent loss (tan δ) are done using Impedance Analyzer (discussed in chapter 2) as a function of temperature from 30 – 350°C with a frequency range between 100 Hz to 1M Hz. The I-V measurement was recorded using a computer-interfaced software VISION via Radiant precision multi-ferroic tester.

3.1.1 Structure and Composition

The XRD patterns of $(Hf_x, Zr_{0.8-x})$ $(Ta, Dy)_{0.2}O_2$ sintered ceramics with $0.2 \leq x \leq 0.6$ with varying Bragg's angle (2θ) from 20°- 60° at RT using Cu-K alpha radiation (1.54 Å) is depicted in **Figure 3.1**. The diffraction pattern shows sharp and intense reflections (**Figure 3.1(a)**) for all three different compositions [x= 0.2 to x= 0.6], suggesting the crystalline nature of the synthesized compound. The physically mixed samples mostly showed mixed phases, with monoclinic phases of both HfO_2 and ZrO_2. However, in the sintered pellets the reflections relating to Ta_2O_5 and Dy_2O_3 were not noticed in the XRD pattern. Hence, the Hf, Zr, Ta, and Dy are expectedly diffused into a single-phase material for all compositions at 1400°C. The closer examinations of the peaks around 28° show dual peaks may be due to the tetragonal splitting and are observed in all three configurations i.e., $(Hf_{0.2}Zr_{0.6})$ $(Ta, Dy)_{0.2}O_2$, $(Hf_{0.4}Zr_{0.4})$ $(Ta, Dy)_{0.2}O_2$ and $(Hf_{0.6}Zr_{0.2})$ $(Ta, Dy)_{0.2}O_2$. The substitution of Dy^{3+} and Ta^{5+} brings structural and lattice distortion. The peaks shifting has been observed with Bragg's angle as Dy^{5+} and Ta^{3+} are smaller sizes compared to Hf^{4+} and Zr^{4+} as can be

seen in **Figure 3.1 (a, b, and c).** Further, the broadening of the peaks in **Figure 3.1 (a & b),** may be due to the small grain size. When crystallite sizes are reduced, typically below a micrometer, diffraction peaks become broader due to two main factors: the finite size effect and microstrain. The finite size effect causes a distribution of interplanar spacings, resulting in a range of angles contributing to the observed peak. The Scherrer equation can quantitatively describe this phenomenon, which relates peak width to crystallite size (not the grain size). Microstrain, on the other hand, refers to non-uniform strain within grains that leads to variations in interplanar distances, further contributing to peak broadening [98].

3.1.2 Microstructure and Morphology

The SEM photographs of the sintered samples of HZDTO ceramics of three different compositions, a) $Hf_{0.2}Zr_{0.6}Ta_{0.1}Dy_{0.1}O_2$, (b) $Hf_{0.4}Zr_{0.4}Ta_{0.1}Dy_{0.1}O_2$, and (c) $Hf_{0.6}Zr_{0.2}Ta_{0.1}Dy_{0.1}O_2$ are shown in **Figure 3.2**. Grain growth and inclusion of grain boundaries occur during sintering. Hence, it is evident (from SEM images) that grains of different sizes (as in **Table 3.2**) agglomerate into bigger grains due to high sintering temperatures. The HZDTO ceramics of the different compositions have denser appearances (**Figure 3.2**) as Hf content increases; $Hf_{0.2}Zr_{0.6}Ta_{0.1}Dy_{0.1}O_2$ < $Hf_{0.4}Zr_{0.4}Ta_{0.1}Dy_{0.1}O_2$, and < $Hf_{0.6}Zr_{0.2}Ta_{0.1}Dy_{0.1}O_2$ with average grain size in the order of 600- 800 nm, 700- 950 nm, and 500- 570 nm respectively.

The discrepancies between the EDX values and theoretical values in **Table 3.1** arise from several factors, including experimental errors, variability in the actual composition of the synthesized materials, and limitations in EDX detection

capabilities. Variances occur due to calibration issues, sample preparation inconsistencies, and matrix effects that influence X-ray emission

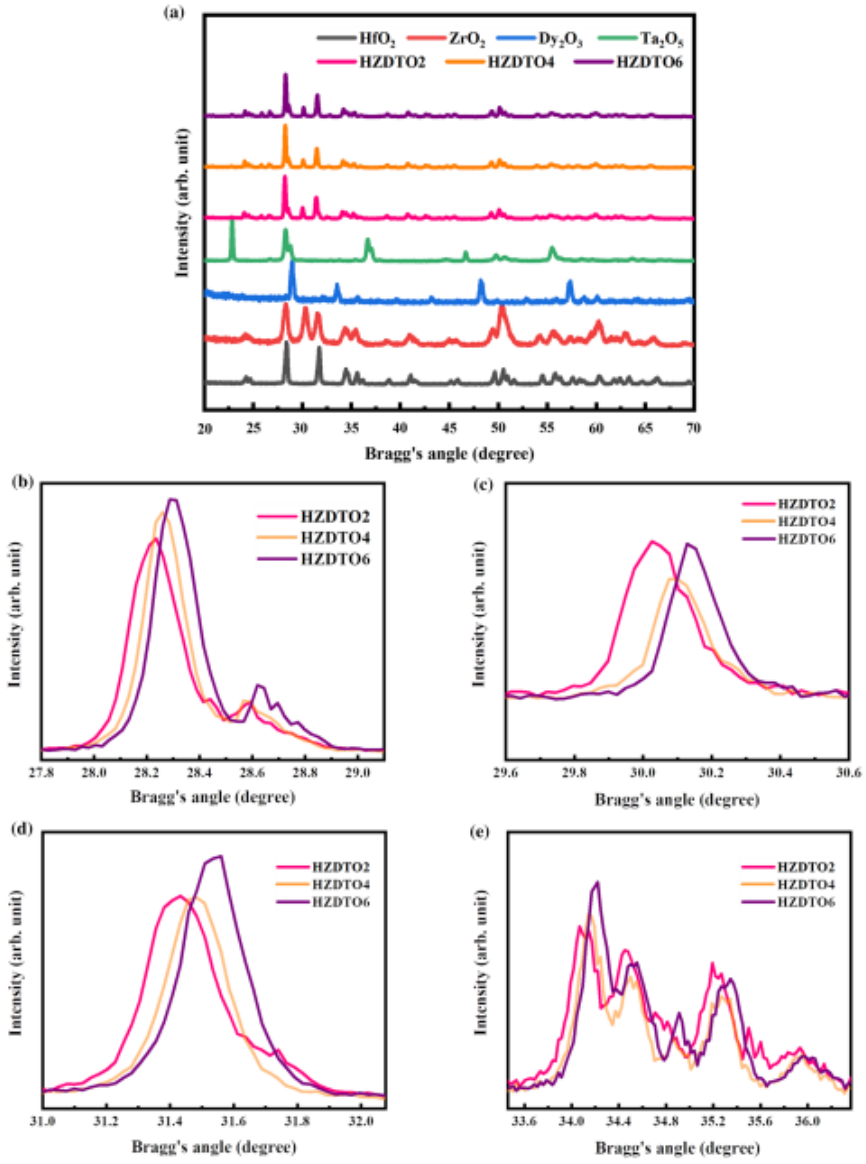


Figure 3.1 (a) XRD patterns of (Hf0.2Zr0.6)(Ta, Dy)0.2O2, (Hf0.4Zr0.4)(Ta, Dy)0.2O2 and (Hf0.6Zr0.2)(Ta, Dy)0.2O2 ceramics at 1400°C with variable Bragg's angle (2θ) with reference to peak obtained: (b) 27-29 (c) 29-30 (d) 30-32, and (e) 30-40.

The surface revealed three ceramic samples with less porosity (5-6%) and the calculated porosity/area is given in **Table 3.1**. The compositions ($Hf_{0.4}Zr_{0.4}$) (Ta, Dy)$_{0.1}O_2$ (**Figure 3.2(b)**) showed the highest average grain size with porosity of around 6% whereas bulk ceramics ($Hf_{0.6}Zr_{0.2}$) (Ta, Dy)$_{0.1}O_2$ (**Figure 3.2(c)**) show slight porosity ~5% having the lowest average grain-size. The ($Hf_{0.4}Zr_{0.4}$) (Ta, Dy)$_{0.1}O_2$ (**Figure 3.2 (a)**) ceramic possesses the value of porosity ~6% without much spacing.

Table 3.1 The calculated average grain size and porosity per area profile for trio compositions.

Compositions	Porosity per Area (%)	Average (nm) grain Size
$Hf_{0.2}Zr_{0.6}Ta_{0.1}Dy_{0.1}O_2$	6	730
$Hf_{0.4}Zr_{0.4}Ta_{0.1}Dy_{0.1}O_2$	6	840
$Hf_{0.6}Zr_{0.2}Ta_{0.1}Dy_{0.1}O_2$	5	535

The growth process of HZDTO ceramics during sintering involves grain growth and the agglomeration of smaller grains into larger ones due to elevated temperatures. As the Hf content increases, the ceramics exhibit a denser appearance, with average grain sizes ranging from 535 nm to 840 nm, indicating that higher Hf concentrations promote densification. A metric for denser appearance can be inferred from the lower porosity values, which range from 5% to 6%, as detailed in **Table 3.2.** The surfaces have visibly cracked walls as shown in **Figure 3.2**, which occurred due to flexural strength and stress. The stress causing these cracks could be attributed to **internal**

stress, stemming from thermal gradients and phase transformations during cooling, rather than external stress. Internal stresses arise from differential shrinkage and misalignment of grains during the sintering process, leading to mechanical failure in the form of cracks. Otherwise, for all three compositions, ceramics have closed-packed structure over a large area with no cracks, and voids on the surface. There are fewer intra-granular spaces with tight adjacent zones of three-grain junctions. The pellets have consistent orientation and geometry on a single-grain surface of pores. The grains are of polygon structures but uniformly distributed. As compared to **Figure 3.2 (c)**, grain boundaries are visible while invisible fused grain reveals the formation of large grains approaching a single boundary. These polycrystalline grains surge towards the single-phase polycrystalline nature with compact, and less-visible grain boundaries.

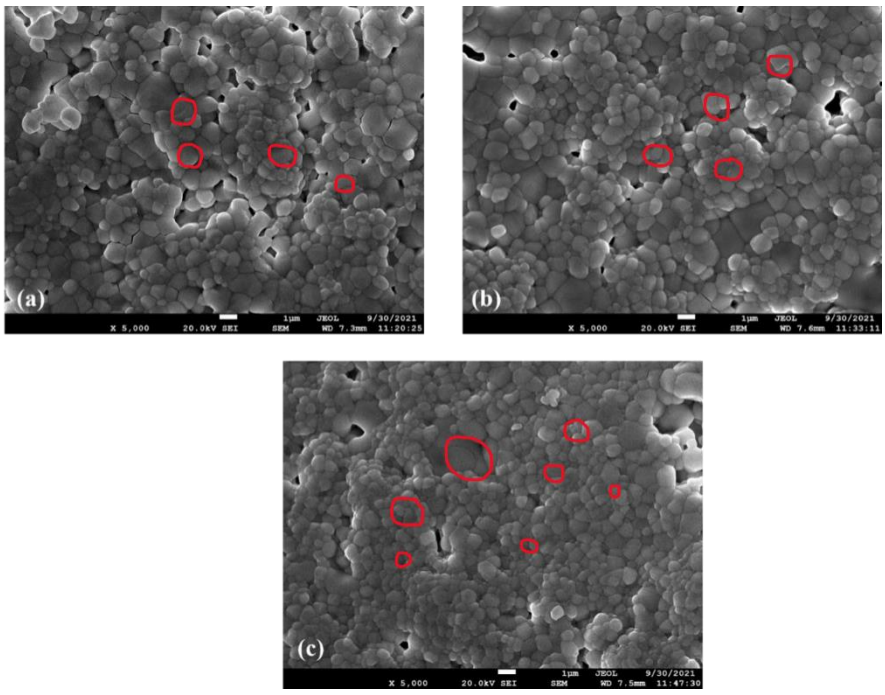


Figure 3.2 High-resolution field emission morphology of (a) $Hf_{0.2}Zr_{0.6}Ta_{0.1}Dy_{0.1}O_2$, (b) $Hf_{0.4}Zr_{0.4}Ta_{0.1}Dy_{0.1}O_2$, and (c) $Hf_{0.6}Zr_{0.2}Ta_{0.1}Dy_{0.1}O_2$ ceramics.

Energy dispersive x-ray spectroscopy (EDS) spectrum of the sintered ceramic $(Hf_{0.2}Zr_{0.6})$ $(Ta, Dy)_{0.2}O_2$, $(Hf_{0.4}Zr_{0.4})$ $(Ta, Dy)_{0.2}O_2$, and $(Hf_{0.6}Zr_{0.2})$ $(Ta, Dy)_{0.2}O_2$ were taken during the SEM measurements and is shown in **Figure 3.3** to check presence of the elements in the samples and to find the elemental composition in the synthesized ceramics. The results of the compositional analysis using EDS are shown in **Table 3.2**. However, it is important to note that EDS has certain limitations in sensitivity, particularly for detecting elements present in low concentrations or those that fall below its detection threshold, which may affect the accuracy of compositional analysis i.e., EDX. The chemical configurations of the samples do agree with the nominal values of targeted compositions within the EDX sensitivity. The various ratios of the cations Zr/Hf: Dy/Ta: Zr/(Hf +Ta +Dy) are 3:1:1.5, 1:1:0.66, and 0.3:1:0.5 for $(Hf_{0.2}Zr_{0.6})(Ta, Dy)_{0.2}O_2$, $(Hf_{0.4}Zr_{0.4})(Ta, Dy)_{0.2}O_2$, and $(Hf_{0.6}Zr_{0.2})(Ta, Dy)_{0.2}O_2$ $(Hf_{0.2}Zr_{0.6})(Ta, Dy)_{0.2}O_2$, $(Hf_{0.4}Zr_{0.4})(Ta, Dy)_{0.2}O_2$, and $(Hf_{0.6}Zr_{0.2})(Ta, Dy)_{0.2}O_2$, respectively. The discrepancies between the EDX values and theoretical values in **Table 3.2** arise from several factors, including experimental errors, variability in the actual composition of the synthesized materials, and limitations in EDX detection capabilities. Variances occur due to calibration issues, sample preparation inconsistencies, and matrix effects that influence X-ray emission.

3.1.3 Electrical Properties

Electrical properties in terms of the dielectric parameters, electrical conductivity and leakage current have been studied for the capacitors of $Hf_xZr_{0.8-x}$ $(Ta, Dy)_{0.2}O_2$ ceramics. The results of these measurements are discussed in the following subsections.

3.1.3.1 Dielectric Properties

Figures 3.4(a), (b), and (c) illustrate the dielectric constant and tangent loss of $Hf_xZr_{0.8-x}$ (Ta, Dy)$_{0.2}O_2$ ceramics with three different compositions (x=0.2, 0.4 and 0.6) as a function of temperature at different frequencies. An *ac* signal of 1V was applied to the DUT and C_p and tan δ were measured in the frequency range 100 Hz to 10^6 Hz using dielectric system **(Appendix-D)**. The values of the dielectric constant of the samples have been calculated from the measured capacitance value capacitor in the Metal-Insulator-Metal (MIM) configuration (i.e., composition typically includes top and layers of metal (here silver paste) electrodes separated by a dielectric material (in this case, HZDTO ceramics). In the case of $Hf_{0.2}Zr_{0.6}$ (Ta, Dy)$_{0.2}O_2$ ceramics, high-*k* remained almost constant in the entire temperature range for most of the frequencies except some variation in the low frequency region.

The dielectric constant remains relatively constant across temperature and frequency due to the stability of the material's microstructure and the dominance of intrinsic dielectric properties over extrinsic factors at these conditions. Dielectric constant ($\epsilon_r = \epsilon/\epsilon_0$) originates from the polarization of the sample or creation or the orientation of the dipoles. However, in the case of linear dielectrics as it not having any permanent dipoles contribution is only from the polarization of the materials under an electric field. In the case of non-linear dielectrics, orientation of the permanent dipoles also contributes and shows a strong frequency dependency over the entire frequency range (10^2 Hz to 10^{16} Hz). The linear dielectric discussed here for the gate-oxide application, there is only polarization due to ionic and electronic/atomic displacement under an applied electric field. This is frequency independent up to the infrared range. So, in

the case of linear dielectric it will be a constant up to the infrared frequencies as there are no orientational dipoles in such dielectrics.

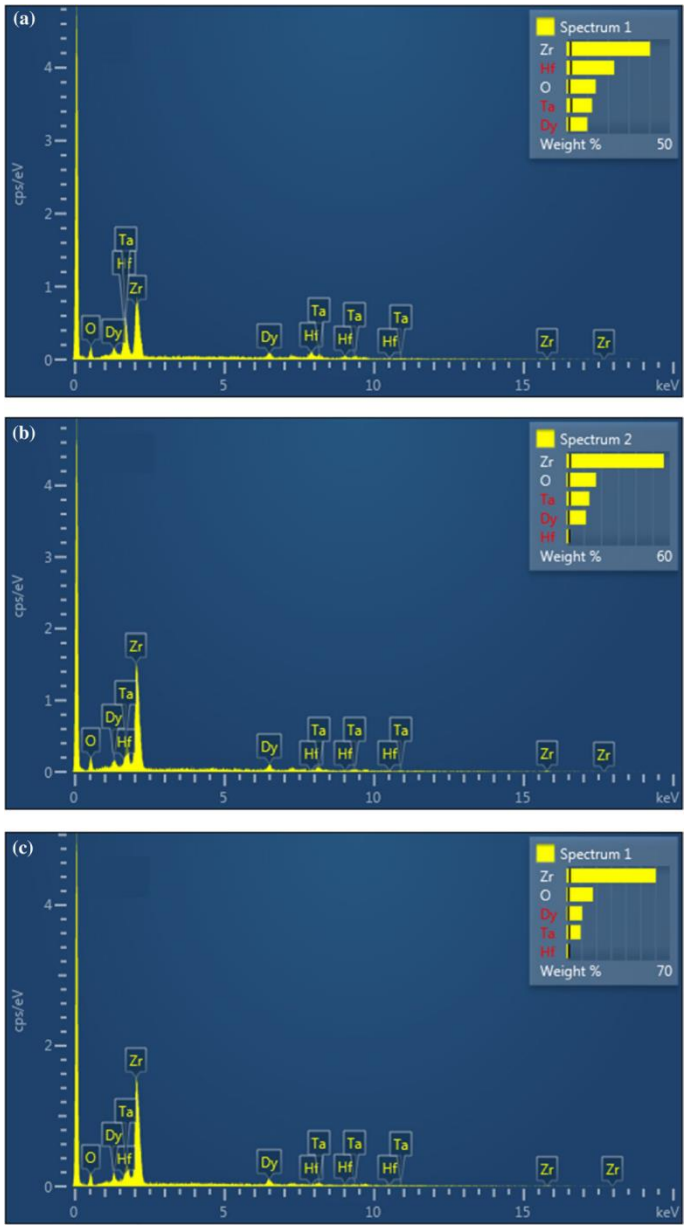


Figure 3.3 Energy-dispersive x-ray of ceramics (a) $Hf_{0.2}Zr_{0.6}Ta_{0.1}Dy_{0.1}O_2$, (b) $Hf_{0.4}Zr_{0.4}Ta_{0.1}Dy_{0.1}O_2$, and (c) $Hf_{0.6}Zr_{0.2}Ta_{0.1}Dy_{0.1}O_2$ ceramics.

Table 3.2 The stoichiometric within the experimental error of EDX for (a) $Hf_{0.2}Zr_{0.6}Ta_{0.1}Dy_{0.1}O_2$, (b) $Hf_{0.4}Zr_{0.4}Ta_{0.1}Dy_{0.1}O_2$, and (c) $Hf_{0.6}Zr_{0.2}Ta_{0.1}Dy_{0.1}O_2$

Element %	Atomic Values (%)					
	(a)		(b)		(c)	
	EDX value	Theoretical value	EDX value	Theoretical value	EDX value	Theoretical value
Hf	8.17	6.67	10.53	13.33	29.89	20
Zr	28.01	20	23.63	13.33	5.89	6.67
Dy	3.9	3.33	3.75	3.33	3.44	3.33
Ta	4.29	3.33	3.98	3.33	2.77	3.33
O	55.63	66.67	58.11	66.68	58.01	66.67
Total	**100**	**100**	**100**	**100**	**100**	**100**

The observed variations at low frequencies can be attributed to surface moisture rather than fundamental material properties. Water has permanent dipoles and contributes to dielectric constant at low frequencies. Also, the measurement was restricted up to 10^6 Hz as at higher frequencies resonance occurred by lead inductance F_r [100, 101]. Inductance arises primarily from the probe wires and their connections rather than from the plates themselves. For the samples having capacitance of the order of picofarads or so (as in the present case), a stray inductance of the order of few micro-Henry (μH) can induce resonance in the 10^6 range.

The obtained values of dielectric constant for (a) $Hf_{0.2}Zr_{0.6}Ta_{0.1}Dy_{0.1}O_2$, (b) $Hf_{0.4}Zr_{0.4}Ta_{0.1}Dy_{0.1}O_2$, and (c) $Hf_{0.6}Zr_{0.2}Ta_{0.1}Dy_{0.1}O_2$ ceramics are ~11, ~17, and ~21 respectively, for all the temperatures between 30 to 350°C. The dielectric value obtained states that $(Hf_{0.6}Zr_{0.2})$ $(Ta, Dy)_{0.1}O_2$ has a higher value than the remaining two compositions: $(Hf_{0.2}Zr_{0.6})$ $(Ta, Dy)_{0.1}O_2$ and $(Hf_{0.4}Zr_{0.4})$ $(Ta, Dy)_{0.1}O_2$. The loss tangents also show the same trend and are supported by the corresponding dispersion as shown in **Figure 3.4** at different temperatures.

The near-constant values of εr and tan δ across a wide range of frequency and temperature suggest that these materials maintain their dielectric integrity under varying operational conditions, which is advantageous for the gate-oxide applications.

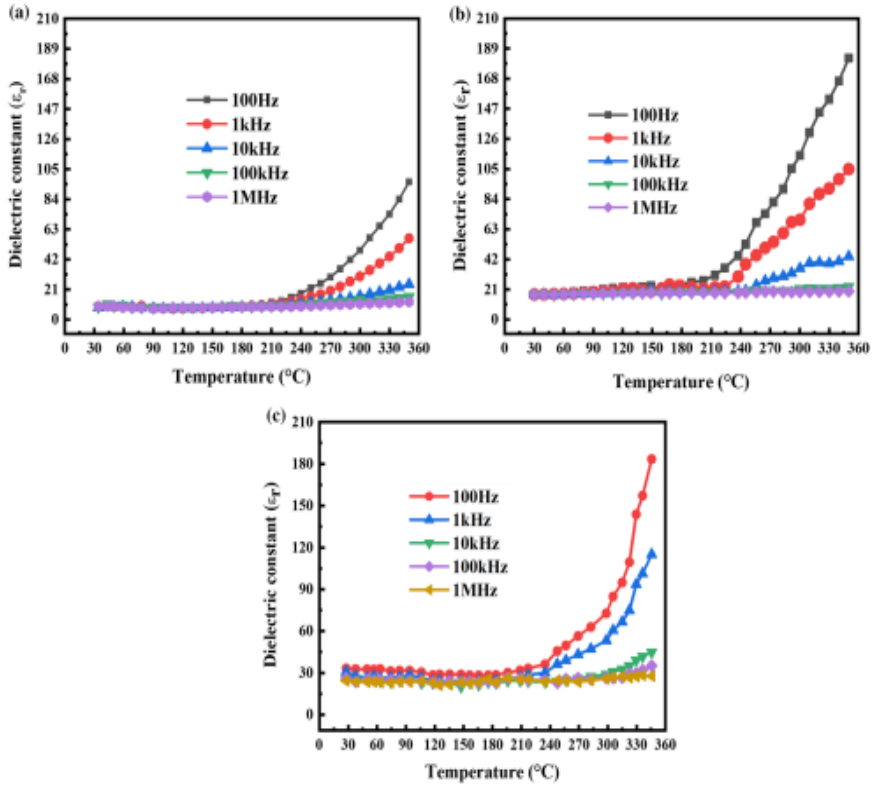


Figure 3.4 (a) $Hf_{0.2}Zr_{0.6}Ta_{0.1}Dy_{0.1}O_2$, (b) $Hf_{0.4}Zr_{0.4}Ta_{0.1}Dy_{0.1}O_2$, and (c) $Hf_{0.6}Zr_{0.2}Ta_{0.1}Dy_{0.1}O_2$ ceramics show the dielectric constant and tangent loss as a function of temperature in heating at different frequency respectively.

3.1.3.2 Electrical conductivity

The ac conductivity as functions of frequency for $Hf_{0.2}Zr_{0.6}Ta_{0.1}Dy_{0.1}O_2$, $Hf_{0.4}Zr_{0.4}Ta_{0.1}Dy_{0.1}O_2$, and $Hf_{0.6}Zr_{0.2}Ta_{0.1}Dy_{0.1}O_2$ ceramic samples has been the calculated from the dielectric constant and dielectric loss determined from the C_p and

tan δ measurements. The ac conductivity (σ_{ac}) can be determined using the relation in equation 3.1[101, 102]:

$$\sigma_{ac} = \omega\varepsilon_0\varepsilon_r \tan\delta \qquad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots 3.1$$

All three compositions showed the same trends with frequency at various temperatures (**Figure 3.4**); a frequency-independent σ_{ac} at the lower frequency region (up to 10^5 Hz) followed by a frequency-dependent σ_{ac} at higher frequencies. The frequency-dependent conductivity of several materials has been elucidated using Jonscher's power law (Equation 3.2), where $\sigma_{dc}(0)$ is the frequency-independent part, and *A* is constant [103]. The frequency independent σ_{ac} refers to the observation that at low frequencies, the AC conductivity remains relatively constant, indicating that the frequency of the applied signal does not significantly influence the charge carriers. This independence occurs because the motion of charge carriers is primarily governed by their interactions with the lattice and other carriers rather than by the frequency of the applied signal. This behavior is consistent with the findings of [104], which indicate that low-frequency conductivity often reflects long-range ordering and is less dependent on frequency due to the dominance of these transport mechanisms [104, 105]. At higher frequencies, the AC field can induce more rapid polarization and movement of charge carriers, leading to increased conductivity and showed dependence on the frequency (n >1). The hopping mechanism becomes more prominent as the frequency increases, allowing for greater energy exchange and polarization effects within the material [106, 107].

$$\sigma_{ac}(\omega) = \sigma_{dc}(0) + A\omega^n \qquad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots 3.2$$

The exponent '*n'* in eqn. 3.2 and its physical significance were explained by Funke [105]. It revealed the interaction of mobile electrons following the fixed lattice positions for n <1, charge carriers obey translation motion, and if n >1, these similar charge carriers along with the bound charges also become accountable for the AC conduction (σ_{ac}) The fitting of equation 3.2 to the data obtained (depicted in **Figure 3.4)**, it has been observed that experimental results obey the Jonscher power law for $(Hf_{0.2}Zr_{0.6})$ $(Ta, Dy)_{0.2}O_2$, $(Hf_{0.4}Zr_{0.4})$ $(Ta, Dy)_{0.2}O_2$, and $(Hf_{0.6}Zr_{0.2})$ $(Ta, Dy)_{0.2}O_2$. with n<1 in the low frequency region and n > 1 in the high frequency region, the ac conductivity of $(Hf_{0.6}Zr_{0.2})$ $(Ta, Dy)_{0.1}O_2$ is high compared to the remaining two compositions. The values of the exponent 'n' are different in frequency regions: one at low frequency and the other at high frequency explaining the two-relaxation mechanism. The high frequencies show an approximately square low dependence on frequency. At low frequencies (<1000 Hz), the conductivity is independent of frequency (n<1) [108]. In short, the plots obtained in the present case are approximately sub-linear at the low frequency and follow Jonscher's power law at high frequency. It confirms that small polaron hopping causes a conduction mechanism concerning compositions such as $(Hf_{0.2}Zr_{0.6})$ $(Ta, Dy)_{0.2}O_2$, $(Hf_{0.4}Zr_{0.4})$ $(Ta, Dy)_{0.2}O_2$, and $(Hf_{0.6}Zr_{0.2})$ $(Ta, Dy)_{0.2}O_2$). The polaron hopping generally follows Arrhenius-like behavior according to the relation shown in **Equation 3.3**, which is indicative of thermally activated hopping processes.

$$\sigma_{ac} = \sigma_0 \exp(\frac{-E_a}{k_B T}) \qquad \text{……3.3}$$

Where E_a is the activation energy, k_B is the Boltzmann constant, and T is the absolute temperature. The presence of an exponent component in the conductivity equation (e.g., Jonscher's power law) reflects the non-linear response of charge carriers under varying frequency conditions, confirming that small polaron hopping contributes significantly to conduction. In a simpler interpretation, ac conductivity and its linear increase at lower frequencies is related to the electron exchange between the ions of the same element having different valence states. The electron spends average time in traps contingent on the energy difference between the two states. However, at higher frequencies because of the multistage hopping process, higher dispersion (higher variation) in σ_{ac} . The variations in compositions of the HZDTO ceramics ($Hf_{0.2}Zr_{0.6}$) (Ta, Dy)$_{0.2}O_2$, ($Hf_{0.4}Zr_{0.4}$) (Ta, Dy)$_{0.2}O_2$, and ($Hf_{0.6}Zr_{0.2}$) (Ta, Dy)$_{0.2}O_2$) do not lead to significant differences in electrical properties such as AC conductivity or dielectric behavior. This stems from the observation that while different compositions exhibit varying levels of conductivity, the overall mechanisms governing charge transport (e.g., small polaron hopping) remain consistent across these compositions. Thus, a dramatic change in conductivity or dielectric response was not observed despite compositional differences

The temperature range of 30-350°C was used to measure the temperature dependency of ceramics' dc conductivity for the three compositions used for the present study. **Figure 3.5** displays the results, which are depicted as a function of 1000/T(°K) at various frequencies for both conductivities. A few orders of magnitude less σ_{dc} was observed compared to σ_{ac}. This is due to the inability of trapped electrons to support a

dc current. The trapped electrons contribute to fluctuations in current (ac) rather than maintaining a steady flow (dc), leading to an increase in the ac current due to their inability to support a dc current.

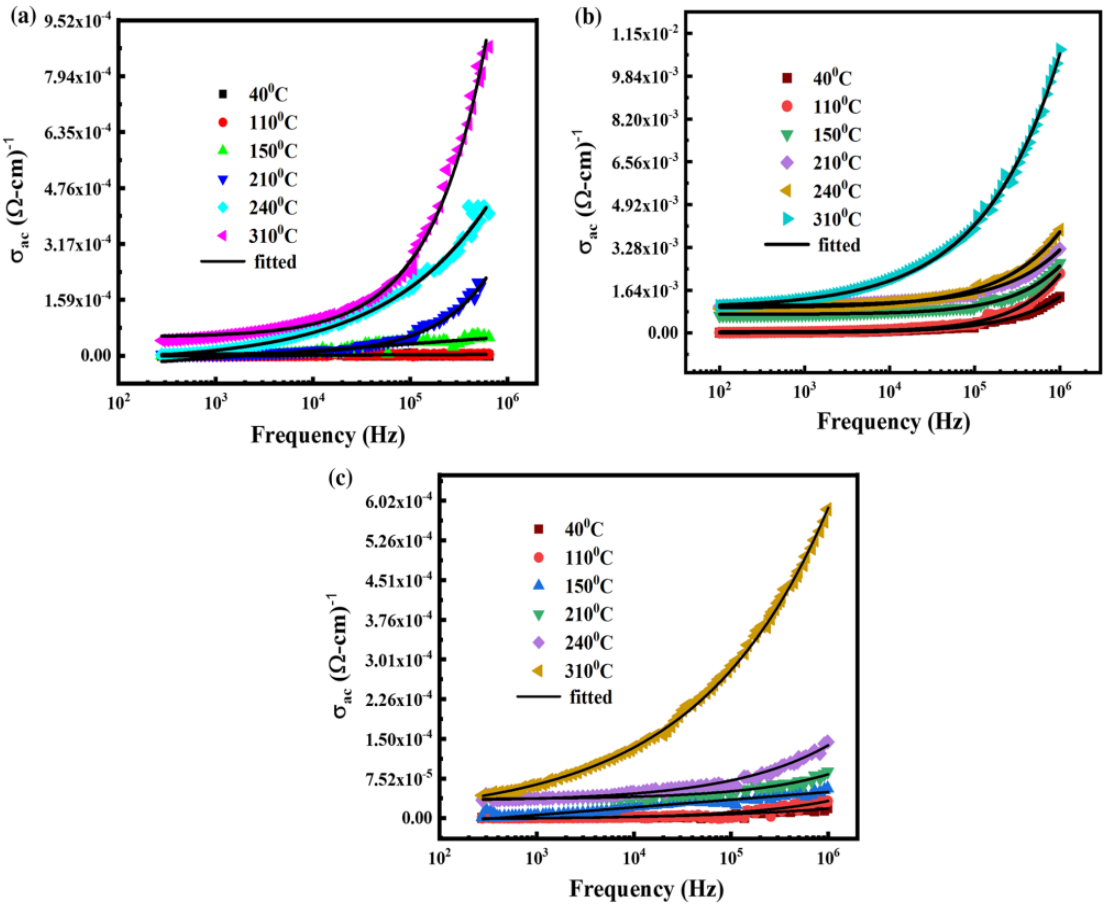


Figure 3.5 Variation of conductivity with frequencies of (a) $Hf_{0.2}Zr_{0.6}Ta_{0.1}Dy_{0.1}O_2$, (b) $Hf_{0.4}Zr_{0.4}Ta_{0.1}Dy_{0.1}O_2$, and (c) $Hf_{0.6}Zr_{0.2}Ta_{0.1}Dy_{0.1}O_2$ at different temperatures.

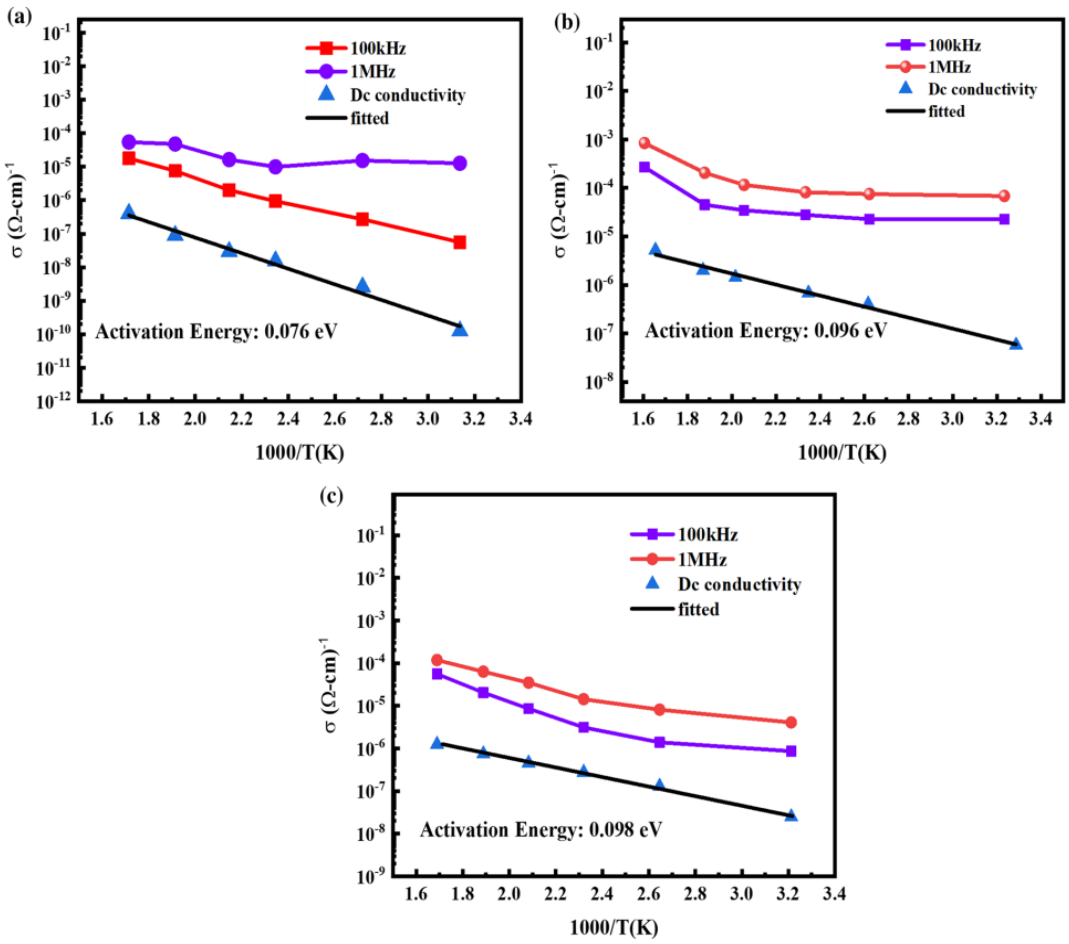


Figure 3.6 Variation of conductivity with 1000/T for various frequencies: (a) $Hf_{0.2}Zr_{0.6}Ta_{0.1}Dy_{0.1}O_2$, (b) $Hf_{0.4}Zr_{0.4}Ta_{0.1}Dy_{0.1}O_2$, and (c) $Hf_{0.6}Zr_{0.2}Ta_{0.1}Dy_{0.1}O_2$.

Table 3.3 displays the values of σdc, and n (low frequency region) that were determined. The term 1000/T (where T is temperature in Kelvin) is significant as it helps to find the activation energy required for this temperature-activated electrical conduction. This representation is commonly used in Arrhenius plots to determine activation energies associated with charge transport mechanisms according to the Equation 3.3. While it is true that this approach can help identify trap levels related to impurities, its critical importance in understanding the charge carrier dynamics in the frequency dependent electrical conductivity. Although trap behavior and dynamics are

not explicitly discussed, the relationship between temperature and conductivity through this representation can still offer insights into how traps may influence overall conductivity

Table 3.3 Different values of dc conductivity and the activation E_a for compositional structures: (a) $Hf_{0.2}Zr_{0.6}Ta_{0.1}Dy_{0.1}O_2$, (b) $Hf_{0.4}Zr_{0.4}Ta_{0.1}Dy_{0.1}O_2$, and (c) $Hf_{0.6}Zr_{0.2}Ta_{0.1}Dy_{0.1}O_2$

Temperature (K)	**DC Conductivity $(\Omega\text{-cm})^{-1}$**	**Ea (eV)**	**N**
450 (a)	$\sim 1.5 \times 10^{-6}$	0.076	0.19
550 (a)	$\sim 1.2 \times 1^{-6}$		
575 (a)	$\sim 1.0 \times 10^{-6}$		
625 (a)	$\sim 0.8 \times 10^{-6}$		
450 (b)	$\sim 2.0 \times 10^{-6}$	0.096	0.28
550 (b)	$\sim 1.6 \times 10^{-6}$		
600 (b)	$\sim 1.2 \times 10^{-6}$		
625 (b)	$\sim 1.0 \times 10^{-6}$		
425 (c)	$\sim 3.5 \times 10^{-6}$	0.098	0.77
525 (c)	$\sim 2.8 \times 10^{-6}$		
600 (c)	$\sim 2.0 \times 10^{-6}$		
625 (c)	$\sim 1.8 \times 10^{-6}$		

These are obtained from the fitted dc conductivity versus 1000/T graph and 'n' from the ac conductivity vs frequency curves (low frequency region) in Figure 3.4 and Figure 3.5.

3.1.3.3 Leakage current

Leakage current through the $(Hf_xZr_{0.8-x})$ (Ta, Dy)$_{0.2}O_2$ capacitors was studied by obtaining the Current-Voltage characteristic of the MIM (metal-$Hf_xZr_{0.8-x}$) (Ta, Dy)$_{0.2}O_2$-metal). The current (I) through the capacitor was noted after a holding time of about 10 s with the voltage (V) using piezoelectric system **(Appendix-E)**. This time was determined from the current–time curve (not shown) at a particular voltage where the current reduces and constant plateau region after the initial high flow of current through the capacitor due to the charging. This current is generally known as the leakage current. For the measurement, the applied dc voltage was ramped from 0 V to 500 V with a step of 5 V and the current was measured at different voltages. The leakage current density (J), current/area - applied electric field (E), voltage/thickness, J-E characteristics of $(Hf_xZr_{0.8-x})$ (Ta, Dy)$_{0.2}O_2$ materials with different compositions are shown in **Figure 3.7**. All the J-E curves have good regularity under positive and negative electric fields for 500 kV/cm. The observed leakage current with 10 s holding time at 3 kV/cm are 3.085×10^{-5}, 1.67×10^{-5}, and 3.93×10^{-6} A/cm^2 for (a) HZDTO2, (b) HZDTO4, and (c) HZDTO6 ceramics, respectively. The J-E curves of the three mentioned compositions display that the leakage current density is effectively reduced due to substitutions of Dy and Ta in the (Hf, Zr) O_2 host materials. If Dy and Ta are not incorporated into the compositions, the leakage current density is expected to increase significantly due to a higher concentration of oxygen vacancies in the Hf-Zr-O system. Without these dopants, leakage currents may rise to levels

around 10^{-4} A/cm² or higher, as the stabilization provided by smaller cations is lost, leading to increased defect concentrations that facilitate current leakage. Therefore, doping reduced the leakage current density due to the reduction in the concentration of oxygen vacancies [109].

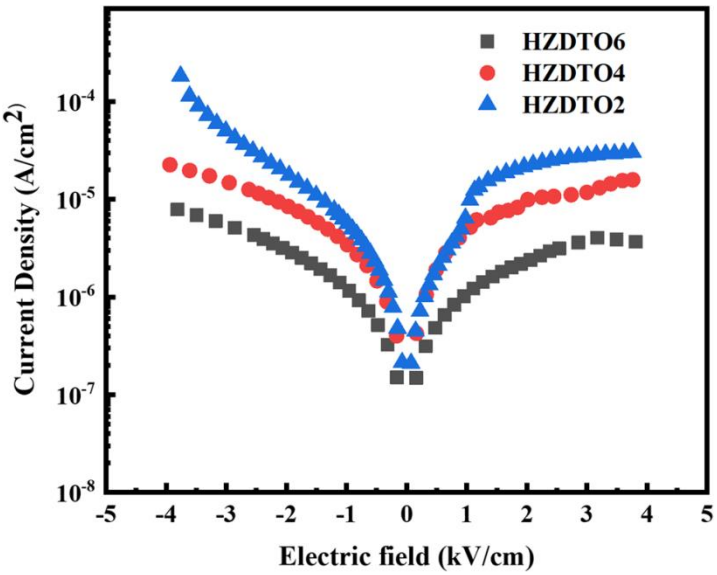


Figure 3.7 Change in leakage current density with the electric field for (Hf_x, $Zr_{0.8-x}$)(Ta, Dy)$_{0.2}O_2$ ceramics with x=0.2(HZDTO2), x-0.4(HZDTO4) and x=0.6 (HZDTO6).

Based on the studies on the bulk ceramic material for gate-oxide application, the following conclusion can be made. Single-phase (Hf_x, $Zr_{0.8-x}$)(Ta, Dy)$_{0.2}O_2$ ceramic material with x = 0.20, 0.40, and 0.60 has been successfully synthesized. The XRD analysis revealed the formation of single-phase in (Hf_x, $Zr_{0.8-x}$)(Ta, Dy)$_{0.2}O_2$ ceramics at the calcination temperature of 1400°C. The morphological analysis of the ceramics showed less porosity without any cracks on the surfaces. The room temperature dielectric constant, r for (Hf_x,$Zr0_{.8-x}$)(Ta,Dy)$_{0.2}O_2$ ceramics increased from 17 to 35

with an increase in the Hf content at 100 kHz. The dc and ac conductivities are higher in HZDTO2 and showed a reduction as the Hf content increased. The leakage current with a 10 s holding time at 3 kV/cm is 3.085×10^{-5}, 1.67×10^{-5}, and 3.93×10^{-6} A/cm^2 for HZDTO2, HZDTO4, and HZDTO6 ceramics, respectively. The study shows that $(Hf_x, Zr_{1-x})O_2$ co-substituted with Dy and Ta are interesting in comparison with existing dielectric oxides for future gate dielectric materials. The thin film deposition with the targets of $(Hf_x, Zr_{0.8-x})(Ta, Dy)_{0.2}O_2$ ceramic material on Si substrate for the MOS structures was done next and is discussed in the following section for high-*k* thin film application in logic devices.

3.2 $Hf_{0.6}Zr_{0.2}Dy_{0.1}Ta_{0.1}O_2$ High-*k* Thin Film

High-k dielectrics have been deposited with various deposition methods, viz., rf-magnetron sputtering, metal organic chemical deposition, chemical solution deposition, molecular beam epitaxy, pulsed laser deposition (PLD). However, PLD stands out as a cutting-edge technology known for its precision in maintaining stoichiometry of the target materials in the deposited thin films on the substrate [110]. Based on the prior investigation (discussed in **section 3.2**) the $Hf_{0.6}Zr_{0.2}Dy_{0.1}Ta_{0.1}O_2$ composition was chosen for the gate-oxide application because it had favorable electrical characteristics in bulk form compared to other two compositions ($Hf_{0.2}Zr_{0.6}Dy_{0.1}Ta_{0.1}O_2$ and $Hf_{0.4}Zr_{0.4}Dy_{0.1}Ta_{0.1}O_2$) [109]. This study explores the application of PLD grown $Hf_{0.6}Zr_{0.2}Dy_{0.1}Ta_{0.1}O_2$ thin films onto Si substrates, with a primary focus on scrutinizing their structural and electrical attributes for the potential integration into gate-oxide applications in logic devices. This section addresses the high-k gate oxide material based on $Hf_{0.6}Zr_{0.2}Dy_{0.1}Ta_{0.1}O_2$ ultra-thin films (< 20 nm)

in the metal-oxide-semiconductor (MOS) devices, the basic building block of MOSFET used in the processors. The performance under bias stress voltage, scalability with thickness reduction, and reliability were examined for thin films on the commonly used semiconductor Si. The interplay between material structure and the electrical characteristics is of paramount importance for the successful gate-oxide performance with high-*k* materials [110].

The PLD system with KrF excimer laser for the material ablation is more favorable for depositing thin films of multi-component material and is thus utilized in the current investigation. Several 1 cm x 1 cm p-type (1–10 cm) Si (100) substrates were first washed in an isopropanol and acetone bath for around 20 minutes each, then dried using a nitrogen gun. The substrate was facing the target, and the target was kept at a 45° angle to the incident laser beam. The thin film deposition was performed on a 99.99% pure $Hf_{0.6}Zr_{0.2}Dy_{0.1}Ta_{0.1}O_2$ ceramic target from Ultra Nanotech, India. The chamber was evacuated to 7.5 x 10^{-7} torr before deposition to get rid of any potential contamination throughout the growing phase. The film deposition was carried out in the high temperature range of 550-700°C and the reactor's deposition pressure was 0.135 torr. Oxygen was utilized as an oxidizer. During the deposition, substrate temperature and oxygen partial pressure were preserved at 600°C and 0.135 torr, respectively as shown in **Figure 3.8 (a)**.

The pulsed laser beam has a wavelength of 248 nm, with a repetition rate of 5 Hz. The laser energy density of ~2 J/cm^2 on the target resulted in ablation of the material and this got deposited on the Si substrate. The thin film with thicknesses from 5 nm to 12 nm on Si-substrate was obtained by changing the number of pulses i.e., from 530 to 640. The deposited films were annealed at 600°C for 30 minutes in oxygen at a

partial pressure of 300 torr to improve the interface between the substrate and thin film. It was then brought down to RT at a 10 °C/min cooling rate. The thickness of the thin film was precisely controlled by the number of laser shots (optimized). Using a high-resolution X-ray diffractometer, the comprehensive phase purity of thin films was evaluated. To MIS, i.e. Pt/ $Hf_{0.6}Zr_{0.2}Dy_{0.1}Ta_{0.1}O_2$ /Si, test structures were realized by depositing rectangular platinum (Pt) top electrodes by DC sputtering with the aid of a shadow mask **(Appendix-F)**.

The shadow mask is typically created by fabricating a thin metal sheet with specific patterns that allow for selective deposition of materials onto the substrate. This can be achieved through photolithography, where a photoresist is applied to the metal layer, exposed to UV light through a patterned mask (**Figure 3.8 (b)),** and then developed to create openings for material depositions. The C-V characteristics at different frequencies was then obtained at room temperature (RT) using a #P-PMF Precision multiferroic unit. Leakage current density-voltage (J–V) measurements were made with the #2400 Keithley source meter.

Start

Clean Substrate

--- Immerse substrate in acetone for 30 minutes

--- Rinse substrate with isopropanol

Pulse Laser Deposition (PLD) for Thin Film Deposition

--- Set PLD system parameters:
- Substrate temperature: 600°C
- Deposition time: 55 seconds
- Use a ceramic target (composition: Hf0.6Zr0.2Dy0.1Ta0.1O2)
- Utilize KrF excimer laser

--- Initiate deposition process

--- Monitor laser pulses to achieve the desired film thickness

Annealing Process

--- Anneal deposited films at 600°C for 30 minutes

--- Annealing atmosphere: Oxygen

--- Maintain oxygen pressure at 300 torr

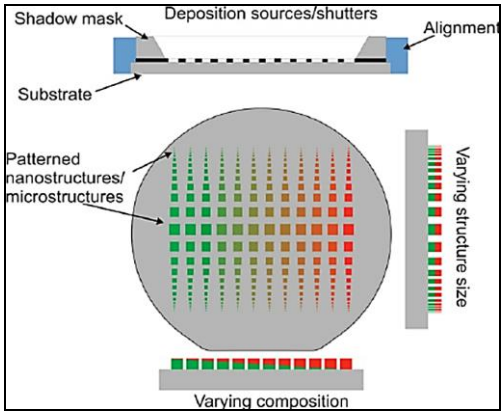
Cooling Down

--- Gradually cool down the samples

--- Cooling rate: 10°C per minute

End

(a)



(b)

Figure 3.8 (a) Step-by-step flow process involved in fabrication. (b) The process of how the shandow mask is created [111].

3.2.1 Results and Discussion

Figure 3.9(a) displays the X-ray diffraction patterns of the Ta_2O_5, Dy_2O_3, HfO_2, and ZrO_2 powders used for preparing $Hf_{0.6}Zr_{0.2}Dy_{0.1}Ta_{0.1}O_2$ target. The poly-crystalline character of the raw materials utilized for the target preparation is shown by the strong peaks in the X-ray diffraction. A monoclinic structure is seen in HfO_2 and ZrO_2 due to their thermodynamic stability at low temperatures. Ta_2O_5, Dy_2O_3, and other polycrystalline powders, however, displayed orthorhombic and cubic structures. The X-ray diffraction patterns of the target $Hf_{0.6}Zr_{0.2}Dy_{0.1}Ta_{0.1}O_2$ material and 100 nm thin films deposited on Si- substrate are shown in **Figure 3.9 (b).** The target displayed a mixed phase rather than a single phase because the constituent powders had distinct structures. The target's elemental mapping revealed a homogeneous distribution throughout the material and preserved the stoichiometry over the entire surface. The peaks at 28.33°, 34.63°, and 50.4° are caused by diffraction from the m (-111), m (022), and m (220) planes of $Hf_{0.6}Zr_{0.2}Dy_{0.1}Ta_{0.1}O_2$ thin films, suggesting the monoclinic structure of the film. The strong peak at 69.2° corresponds to the underlying Si-substrate. The thickness of thin films can vary widely depending on the application and material properties. Typically, thin films in semiconductor applications can range from a few nanometers to several hundred nanometers. For example, in high-*k* dielectrics like $DyScO_3$ used for the gate-oxide application, thickness ranges from 2 nm to 10 nm [110]. This thickness range is discussed in C-V characteristics of the $Hf_{0.6}Zr_{0.2}Dy_{0.1}Ta_{0.1}O_2$. The higher thickness of $Hf_{0.6}Zr_{0.2}Dy_{0.1}Ta_{0.1}O_2$ films (100 nm) on Si substrate is used here for structural studies as it gives more intensity of the reflected signal from the sample, thus reducing error in the measurements.

Figure 3.10 shows the surface morphology of $Hf_{0.6}Zr_{0.2}Dy_{0.1}Ta_{0.1}O_2$ ceramics sintered at 1400°C for 4h and the annealed $Hf_{0.6}Zr_{0.2}Dy_{0.1}Ta_{0.1}O_2$ ceramic film on Si- substrate at 600°C for 30 minutes. The surface morphology of the bulk ceramic (**Figure. 3.10 (a)**) shows bigger gain with average grain size ~ 500 nm and are continuous. However, thin film surface morphology (**Figure. 3.10 (b)**) shows a uniform smooth featureless surface without any cracks in contrast to the bulk.

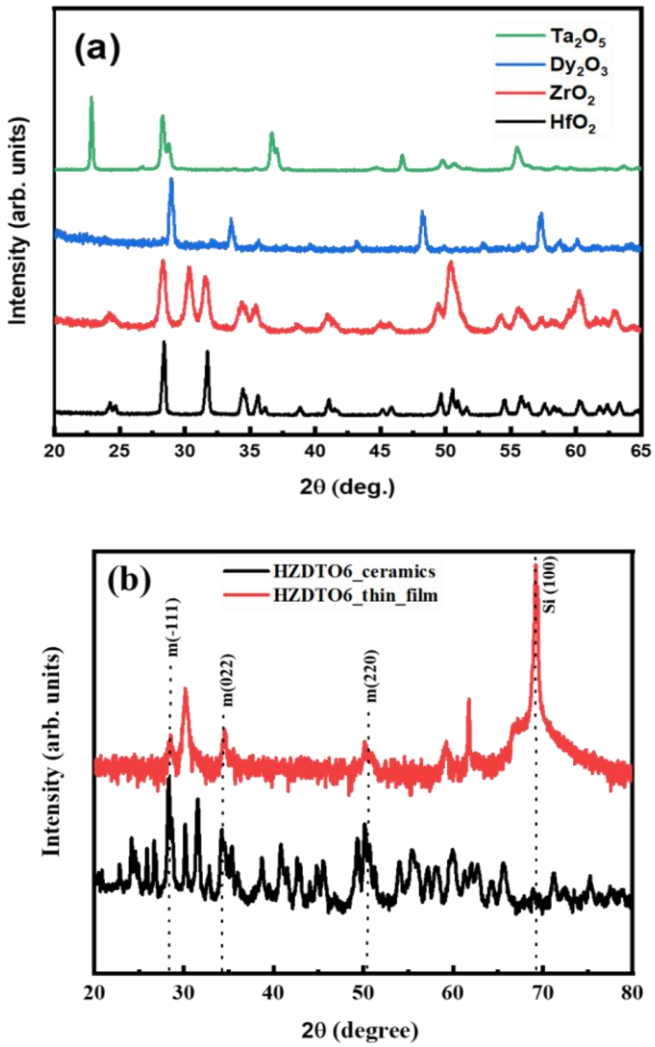


Figure 3.9 X-ray intensity as a function of the scattering angle 2θ (a) precursors, (b) $Hf_{0.6}Zr_{0.2}Dy_{0.1}Ta_{0.1}O_2$ ceramic and thin film.

The C-V characteristics of the Pt/ $Hf_{0.6}Zr_{0.2}Dy_{0.1}Ta_{0.1}O_2$ /p-Si MIS diodes with various film thicknesses (5- 12 nm) are shown in **Figure 3.11 (a)**. For these measurements an ac signal of 50 mV was superimposed to the bias voltage (dc voltage). The frequency of the ac signal was 100 kHz, and 50 mV/s was the sweep rate of the dc voltage. The gate voltage was swept for measurement and started from +3V (inversion) to -3V (accumulation) and back to +3V (inversion). A layer with the lowest thickness of 5 nm had the highest capacitance of about 90 pF compared to other samples with higher thickness.

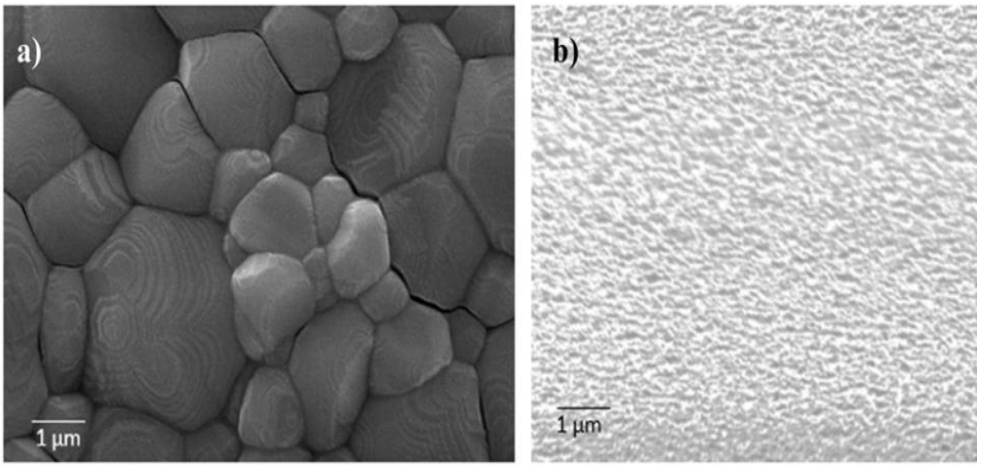


Figure 3.10 FESEM surface morphology of (a) the bulk $Hf_{0.6}Zr_{0.2}Dy_{0.1}Ta_{0.1}O_2$ ceramic and (b) 150 nm thin film $Hf_{0.6}Zr_{0.2}Dy_{0.1}Ta_{0.1}O_2$ ceramic on p-type Si (100) substrate.

With increasing thickness, the capacitance at the accumulation region decreased, which suggests that capacitance scales with dielectric thickness (capacitance increases with the thickness reduction). Capacitance (C) is given by the Equation 2.11. This relationship indicates that as the thickness `d' increases, capacitance decreases, for the same area and materials. The graph shows accumulation, depletion and inversion

regions in the C-V characteristics. In the case of p-type substrates (in the present case) accumulation will be at the -ve voltage, where the thickness of the capacitor is equal to the high-*k* dielectric thickness. As the voltage increases, for a given thickness of high-*k* thin film the effective thickness of the capacitor increases due to the depletion of charges and capacitance gradually decreases as can be seen in **Figure 3.11 (a).** With further increase in the bias voltage, the depletion layer thickness gets saturated due to the inversion of the charges, and this region is the inversion region. In the p type Si this inversion region will be in the +ve bias voltage region. Also, due to the same doping concentration or resistivity, the capacitance at inversion remained invariant for various thickness of the high-*k* dielectrics as expected. The well-behaved C-V curves with clear accumulation, depletion and inversion regions with little hysteresis suggest a good interface between the film and the underlying substrate. By assuming the two-layer capacitance model (interlayer and high-*k* film), the equivalent oxide thickness is given by the relation in Equation 2.11. A linear fit through all the data points in the graph shown in **Figure 3.11 (b)**, confirms good agreement with the given Equation 3.5. The calculated ε_r ~36 (from the slope of the fitted curve) was found to be higher than the previously published value for $Hf_{0.6}Zr_{0.2}Dy_{0.1}Ta_{0.1}O_2$ bulk ceramics 29 [112], suggesting higher value for thin films than the corresponding bulk ceramics. Also, $Hf_{0.6}Zr_{0.2}Dy_{0.1}Ta_{0.1}O_2$ films are significantly higher than HfSiOx's value (ε_r ~12 - 14) on Si used in the current processors [112]. A similar ε_r value of $20 \leq \varepsilon_r \leq 40$ is projected to meet the need for future downscaling, according to Robertson's publications on high-*k* dielectric materials for the construction of logic circuits in microprocessors [113]. One of the key technological advancements for the CMOS devices is the scaling of the high-*k* gate dielectric with EOT less than 0.5 nm.

The standard practice for maintaining acceptable switching characteristics of logic gates and reducing the short-channel effects of MOS transistors is to scale down the gate oxide thickness proportionally or even more. The EOT < 0.5nm is required for such nano-devices and for that the straight-line fit mentioned before must pass through the origin. However, in the present case, the straight line intercepts the *y*-axis at 0.65 nm and hence the minimum EOT is limited to this value only as can be seen in **Figure 3.11 (b)**. This shows the presence of an interlayer with low dielectric constant between the high-*k* dielectric and Si substrate. The thickness of this interfacial layer (dead layer) between the substrate and the $Hf_{0.6}Zr_{0.2}Dy_{0.1}Ta_{0.1}O_2$ is 0.65 nm, the y-intercept. This is expected in the current investigation since the native oxide (i.e., SiO_x) on the Si substrates was not removed from the Si surface before the high-*k* films were deposited. In the present case, 5 nm $Hf_{0.6}Zr_{0.2}Dy_{0.1}Ta_{0.1}O_2$ film achieves an EOT of 1.2 nm. However, the EOT can be further decreased below 0.65 nm if SiO_x is removed before deposit and SiO_x regrowth is prevented before the deposition of the $Hf_{0.6}Zr_{0.2}Dy_{0.1}Ta_{0.1}O_2$. thin film. This is generally achieved by cleaning the Si substrate with 2% hydrofluoric acid (to remove SiO_x) before deposition and heating the substrate under ultra-high vacuum (to prevent SiO_x growth by minimizing Si surface exposure to oxygen). The direct tunneling limit of the high-*k* film with ε_r 15 for having an EOT of about 0.5 nm is already reached with the physical thickness between 2 and 3.5 nm of currently used high-k gate-oxide [114, 115]. To avoid this quantum mechanical tunneling, which usually raises the leakage current density, a thicker physical layer made of even greater ε_r material is required and $Hf_{0.6}Zr_{0.2}Dy_{0.1}Ta_{0.1}O_2$. is of importance in that scenario.

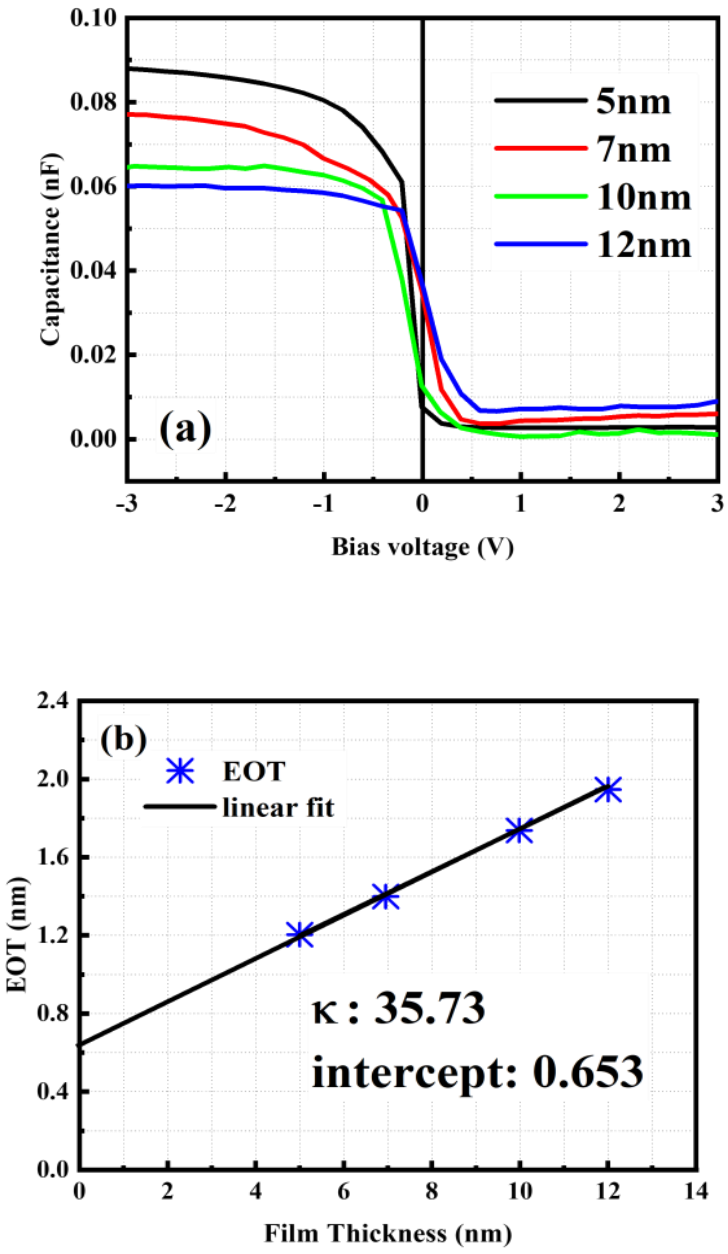


Figure 3.11 a) C-V characteristics of the MIS capacitor; b) EOT vs thickness.

The ideal thickness to be explored for the $Hf_{0.6}Zr_{0.2}Dy_{0.1}Ta_{0.1}O_2$ thin films is closely related to achieving an EOT of less than 0.5 nm, which is critical for future nano-CMOS devices. From the afore-mentioned discussion, the current minimum EOT

observed is 1.2 nm due to the presence of a SiO_x on the silicon substrate before deposition. From **Figure 3.11**, it can be inferred that while the target EOT is below 1 nm, the actual performance is limited by the interception of the fitted line on the y-axis at 0.65 nm, indicating that further optimization is needed to achieve thinner effective oxide layers. Therefore, to minimize leakage and improve device performance, it would be advisable to aim a thickness closer to the quantum tunneling limit (~ 3nm) to obtain an EOT below 0.5 nm by suppressing the native oxide regrowth as mentioned before. As demonstrated in **Figure 3.12 (a),** the C_{ox} of the films is frequency dependent on a particular thickness, as seen by the minor dispersion over the frequency range of 1 kHz to 1 MHz, which was absent in the inversion regime (not shown**)**. The semiconductor's minority carriers (electron) and cations in the film response to the applied AC signal's frequency introduce a variable depletion thickness with frequency and hence accumulation capacitance shows a slight dispersion. However, the inversion capacitance (C_{min}) shows frequency independent behavior as the charges that prevent deep depletion (minority carriers) enable constant thickness (oxide layer + depletion layer thickness) and hence capacitance remains constant with less frequency dependence.

The flat-band voltage (V_{FB}) for the Pt/$Hf_{0.6}Zr_{0.2}Dy_{0.1}Ta_{0.1}O_2$ /Si MIS samples were measured using the flat-band capacitance method. This method involves analyzing the capacitance-voltage (C-V) characteristics of the MIS structure. Specifically, the V_{FB} is determined by identifying the point of intersection between the C-V curve and its second derivative, which indicates the flat-band condition [116, 96]. This approach

provides a reliable measurement of V_{FB} across different film thicknesses, as shown in **Figure 3.12 (b).**

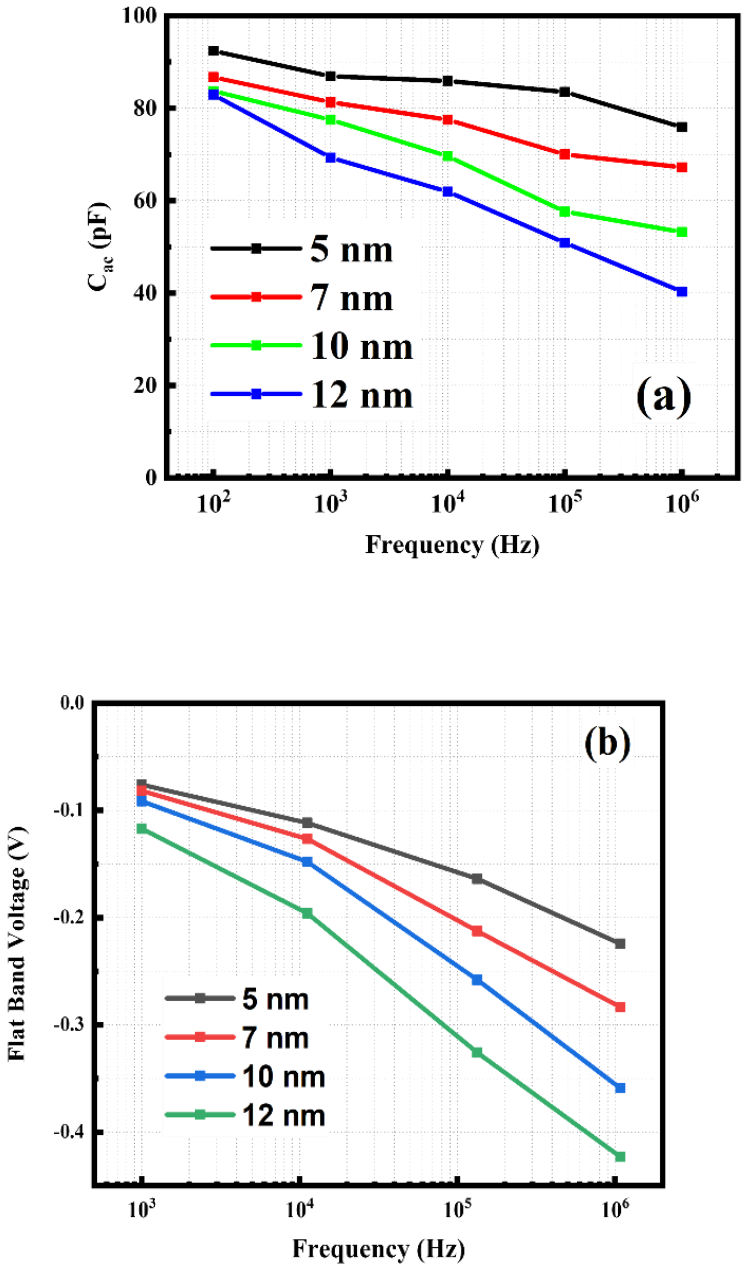


Figure 3.12 (a) Cac, and (b) Flat-band voltages as a function of frequency of the MIS structure for 5 nm, 7 nm, 10 nm, and 12 nm.

The point of intersection between the obtained CV curve and its second derivative (not shown) gives the V_{FB}. In all four MIS samples, V_{FB} varies from -0.076 V to -0.22 V, -0.08 V to -0.28 V, -0.096 to -0.35 V, and -0.11 V to 0.43 V for 5 nm, 7 nm, 10 nm, and 12 nm, respectively, for frequency ranging from 1 kHz to 1 MHz as shown in **Figure 3.9 (b).** With thickness (between 5-12 nm), the reported range of V_{FB} values for HfSiO/HfSiON is 25 mV [117]. **Figure 3.13 (a)** states that there is an outstanding correlation between the derived flat band voltages and film thickness. The variation in V_{FB} with film thicknesses as shown **in Figure 3.13 (a)** is due to the negatively charged electrons injected from gate metal to high-*k* oxide with the bias voltage. V_{FB} is the voltage required to flatten the bent bands of the semiconductor towards the oxide interface (discussed in Chapter 2) or in other words at this voltage the channel is neutral. The threshold voltage (V_{th}) is always higher than the V_{FB} because of the additional voltage required to create the inversion layer with minority charge carriers in the channel. The injection of negatively charged electrons from the gate metal into the high-*k* oxide can indeed affect the V_{FB} and hence the threshold voltage of the device. This injection can lead to an increase in negative charge within the dielectric, potentially shifting V_{th} negatively and impacting device performance. While this process does not typically cause displacement damage directly, it can contribute to interface state generation or charge trapping, which may degrade device characteristics over time. The obtained V_{FB} are -0.108 V, -0.126 V, -0.148 V, and -0.196 V for 5 nm, 7 nm, 10 nm, and 12 nm respectively at 10 kHz. The fixed charge density and its distribution can be calculated using the relation [118, 119]. $V_{FB}=-Q_{ss}/C_{ox}+\phi_{ms,}$ where $\emptyset_{ms}$- the work-function difference between metals (Pt) and $Hf_{0.6}Zr_{0.2}Dy_{0.1}Ta_{0.1}O_2$; V_{FB}- flat-band voltage, and C_{ox}- oxide capacitance at

accumulation. The experimentally measured flat-band voltage as a function of oxide thickness has a slope of $Qss/Cox \sim 0.0137$, and an intercept of $\emptyset_{ms} \sim -0.0296$ V (**Figure 3.13 (a)**). The plot's straight line validates that increase in the fixed charge density with the physical oxide thickness. The fixed oxide charge (Q_{ss}) was estimated as a function of oxide thickness, varied from 4.1 x 10^{10} cm^{-2} to 10.2 x 10^{10} cm^{-2}, almost doubled as the thickness increased from 5 to 12 nm. Compared to the oxide charge densities reported HfO_2 ~ 2.0 x 10^{11} cm^{-2} [118], and $H_{0.25}Ta_{0.75}O_x$ ~ 1 x 10^{12} cm^{-2} [117], the possible reasons can be related to the growth kinetics. Factors influence growth kinetics during thin film deposition. Higher substrate temperatures enhance atomic mobility, leading to improved crystallinity and reduced defect density. The deposition rate also plays a crucial role, as it affects surface diffusion and nucleation processes, thereby influencing film quality. Finally, the nature of the substrate affects how well the film adheres and grows. The atomic bond structure of the elements present in the film is correlated to the fixed charge density. High-*k* HfO_2 dielectric has shown both positive and negative flat band voltage depending on the type of charges distributed in the films [66, 120, 121]. Figure 3.13 (b) presents the current density-voltage curve for the $Hf_{0.6}Zr_{0.2}Dy_{0.1}Ta_{0.1}O_2$ film on Si (100) at room temperature in the accumulation region. The current remains relatively stable up to -3V, after which a significant increase in current flow through the film is observed, consistent with the behavior seen in the Current-Voltage characteristics. This phenomenon at low voltages may be attributed to the filling of pre-existing fixed oxide traps, which contain positive charges [122]. As a result, electrical conduction in this metal-oxide high-k dielectric is likely influenced by charge trapping/detrapping or hopping mechanisms, such as Poole-Frenkel conduction, at lower voltages. This is supported

by the oxide charge density of approximately ~10^{11} cm^{-2} derived from the C-V results discussed earlier. Once the traps in the high-*k* oxide film are filled with electrons up to 3V, the current density increases significantly due to enhanced Schottky emission.

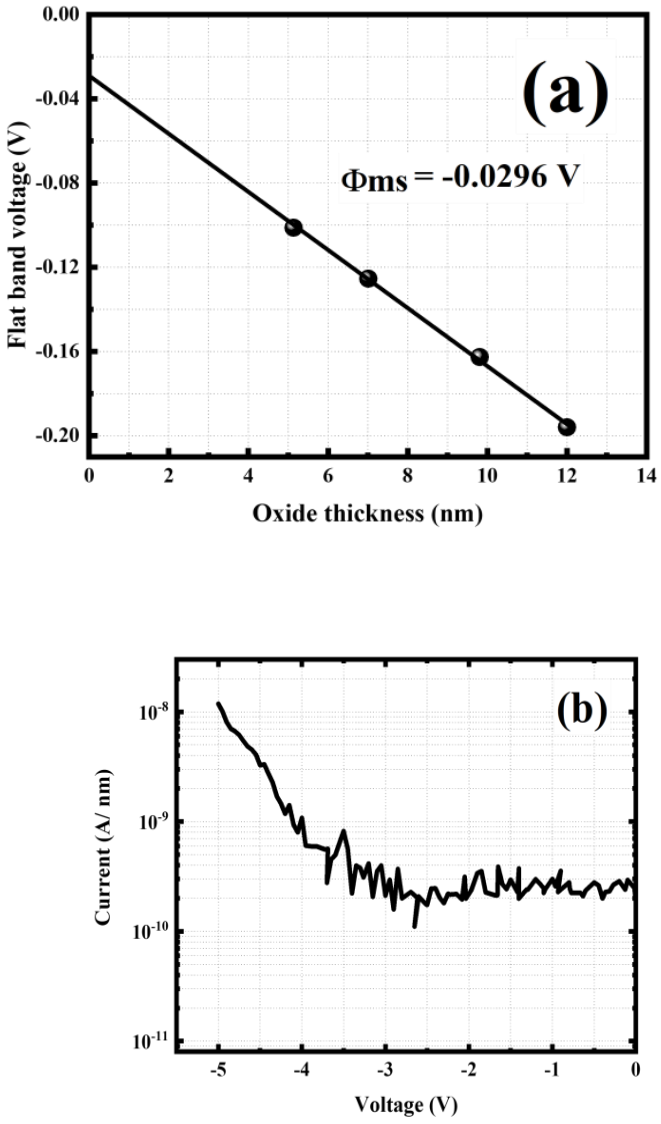


Figure 3.13 (a) Flat-band voltage as a function of point inflection with different thicknesses, and (b) current density vs. voltage characteristics of 5 nm Pt/Hf0.6Zr0.2Dy0.1Ta0.1O2/Si stack. The I-V is well-behaved.

Figure 3.13 (b) presents the current density-voltage curve for the $Hf_{0.6}Zr_{0.2}Dy_{0.1}Ta_{0.1}O_2$ film on Si (100) at room temperature in the accumulation region. The current remains relatively stable up to -3V, after which a significant increase in current flow through the film is observed, consistent with the behavior seen in the Current-Voltage characteristics. This phenomenon at low voltages may be attributed to the filling of pre-existing fixed oxide traps, which contain positive charges [122]. As a result, electrical conduction in this metal-oxide high-k dielectric is likely influenced by charge trapping/detrapping or hopping mechanisms, such as Poole-Frenkel conduction, at lower voltages. This is supported by the oxide charge density of approximately $\sim 10^{11}$ cm^{-2} derived from the C-V results discussed earlier. Once the traps in the high-*k* oxide film are filled with electrons up to 3V, the current density increases significantly due to enhanced Schottky emission. In this case, the effective barrier height is lowered due to the combined effects of the image field and Coulomb field from positively charged trap levels [123]. Consequently, conduction through the conduction band becomes feasible, resulting in an elevated current level. It is also noteworthy that the leakage current density at 4V is approximately ~1 A/cm^2, indicating good integrity of the gate stack. This low leakage current density may be advantageous for developing ultrathin dielectric layers with sub-nm equivalent oxide thickness (EOT) above the effective tunneling thickness [124].

Ultra-thin Dy and Ta doped hafnium-zirconium oxide ($Hf_{0.6}Zr_{0.2}Dy_{0.1}Ta_{0.1}O_2$) insulating films were successfully prepared using Pulsed Laser Deposition on p-type silicon. Films were investigated systematically for the structural and electrical properties. The dielectric constant obtained for Pt/$Hf_{0.6}Zr_{0.2}Dy_{0.1}Ta_{0.1}O_2$/Si MIS configurations was 35 at 100 kHz. The negligible hysteresis, low EOT ~ 1.2 nm, and

low leakage current density ~ 1 A/cm^2 were obtained for ultrathin $Hf_{0.6}Zr_{0.2}Dy_{0.1}Ta_{0.1}O_2$. As a result, fabricated gate structure can be used for CMOS logic devices and integrated circuits.

CHAPTER 4

MEMORY DEVICES -BULK CERAMICS AND CERAMIC THIN FILM

In thisulk structures of $(Hf_x, Zr_{1-x})O_2$ ceramics where x =0.25, 0.5, 0.75 [$(Hf_{0.25}, Zr_{0.75})O_2$, $(Hf_{0.50}, Zr_{0.50})O_2$ and $(Hf_{0.75}, Zr_{0.25})O_2$] were synthesized using a solid-state reaction route were discussed. The structural evolution of ceramics and surface morphology are studied to synthesize single-phase material in bulk ceramic form. An ample examination of the dielectric response as a function of frequency and temperature has been done using the MIM capacitor structures. Leakage current through the capacitors was further considered with I-V measurements to understand the DC and AC conduction mechanism in the bulk material. To check the ferroelectric properties of the bulk material polarization-electric field measurements were also performed. The promising composition of $HfZrO_2$ ceramics, $(Hf_{0.75}, Zr_{0.25})O_2$ has been used for thin film preparation by preparing the target for PLD. The proposed $(Hf_{0.75}, Zr_{0.25})O_2$ for low-power memory applications is also discussed in the thin film form. These two types of material, bulk ceramics and thin film on platinized silicon substrates are discussed in this chapter.

4.1 Ceramics for Non-Volatile Memory

$Hf_xZr_{1-x}O_2$ ceramics of x= 0.25, 0.5, 0.75 (refer as HZO25, HZO50, and HZO75 respectively) were prepared by the conventional solid-state reaction method. Raw materials of HfO_2 (99.9%), and ZrO_2 (99%) were mixed in alcohol medium, dried, and calcined at 1200 °C for 4 h. After that, it was finely powdered using a mortar

pestle and pressed into 10 mm-diameter pellets and sintered at 1400 °C for 4 h in a muffle furnace. The behavior of sintered ceramics was inspected with a high-resolution X-ray diffraction meter (Bruker Inc., #D8) with Cu-Kα radiation (wavelength =1.54178 Å). The surface morphology and composition were studied by field emission scanning electron microscopy, FE-SEM (JOEL Inc., IT800) and energy dispersive x-ray (EDX). The ceramic discs were electrode with silver paint on both sides followed by a heat treatment at 150 °C for 20 min for the electrical characterization. The dielectric properties were then studied utilizing a precision impedance analyzer (HIOK Inc., 3532-50 LCR Hi-TESTER) controlled by a computer in a frequency range from 100 Hz to 1 MHz with temperature varying from RT to 350°C. The ferroelectric hysteresis loop and leakage current were determined at RT using a Radiant Technologies Inc. (Precision multi-ferroic || ferroelectric tester) unit.

4.1.1 Structure and Composition

The x-ray diffraction pattern of the $Hf_xZr_{1-x}O_2$ ceramics sintered at 1400°C with varying Bragg's angle (2θ) from 20°- 60° at room temperature (RT) using Cu-K alpha radiation are shown in **Figure 4.1**. The diffraction peaks which are sharp and intense (**Figure 4.1**) for all the composition (x= 0.25, 0.50 and 0.75), is due to the better crystallinity and larger grain size in the synthesized materials. The physical mixed samples mostly showed a mixed phase of both HfO_2 and ZrO_2 in the XRD pattern of the powder. The closer examinations of the peaks of the samples annealed at 1200 °C, 1400 °C, and 1500 °C in **Figure 4.1 (a) to Figure 4.1 (c)** show systematic phase evolution. There is a peak overlapping in the case of HZO25 (**Figure 4.1 (a)**) in the XRD pattern. However, around 28° and 34° peak splitting happened in $Hf_{0.5}Zr_{0.5}O_2$

and $Hf_{0.75}Zr_{0.25}O_2$ may be due to the tetragonal splitting (**Figure 4.1 (b, c)).** The peaks at 31.5° and 31.7° for $Hf_{0.5}Zr_{0.5}O_2$ and $Hf_{0.75}Zr_{0.25}O_2$ respectively, indicate more tetragonal phase with more Hf content [125-127]. The composition of $Hf_{0.75}Zr_{0.25}O_2$ holds more tetragonal and orthorhombic phases than the $Hf_{0.5}Zr_{0.5}O_2$ and $Hf_{0.25}Zr_{0.75}O_2$.

The significance of the remanent polarization values, which will be discussed in section 4.1.3.3, is that they confirm the presence of ferroelectricity in the HZO compositions. Higher remanent polarization indicates a stronger ferroelectric response, which is essential for memory applications where the polarization state is used to store information. The variations in remanent polarization between the different compositions (HZO25, HZO50, and HZO75) can be attributed to differences in their crystal structure, grain size, and defect concentration, as further elaborated upon in the following sections.

The elemental compositions of the synthesized ceramics were obtained by EDX equipped with the FE SEM. The results of EDX for the ceramics were practically the same as the targeted composition and confirmed no traces of other ions. The stoichiometry of as-prepared HZO ceramics was Hf: Zr: O= x: (1-x): 2, within the acceptable errors. The errors in EDX analysis are influenced by a variety of factors, including instrumental calibration, sample preparation, detection limits, matrix effects, statistical variability, and environmental conditions. Understanding these sources of error is crucial for interpreting EDX results accurately and ensuring that the measured compositions.

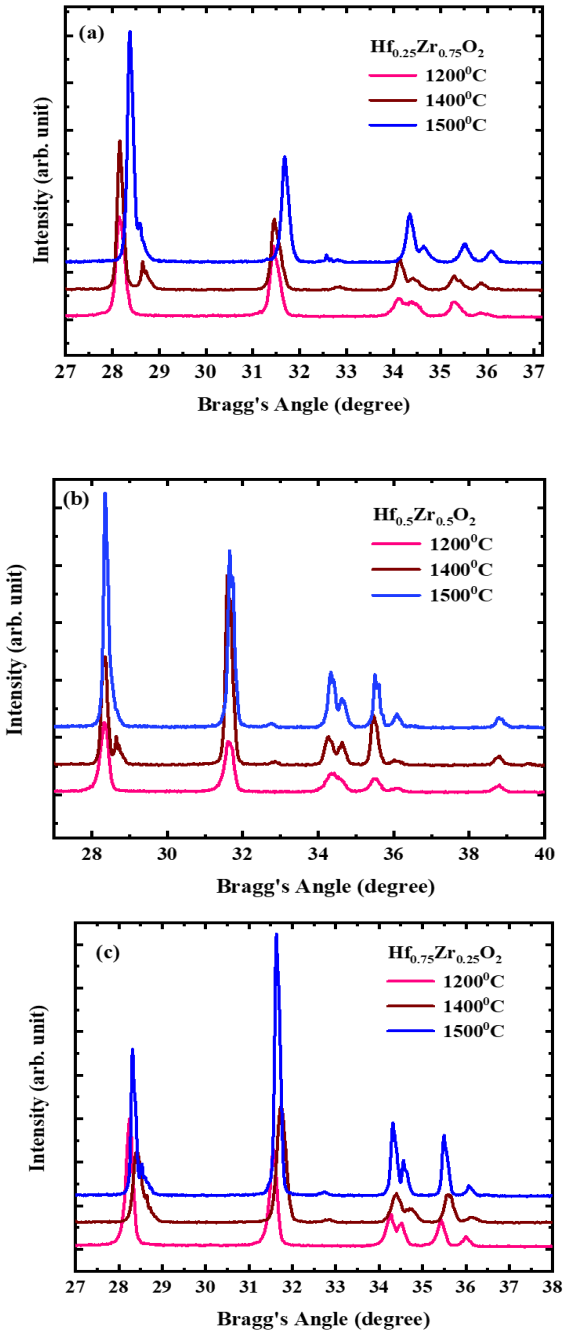


Figure 4.1 (a) X-ray diffraction patterns (scan speed 100/min) of (a) HZO25, (b) HZO50, and (c) HZO75 ceramic at 1200 °C, 1400 °C, and 1500 °C.

Nevertheless, it is a fast measurement method widely used and has an error of about 10%. The results of the EDX analysis of the HZO ceramics are shown in **Table 4.1 (a)**. The chemical compositions of the synthesized ceramics of HZO25, HZO50, and HZO75 showed the Zr/Hf ratio of 3.003, 0.987, and 0.259 agreement with the nominal theoretical Zr/Hf ratio of 3.00, 1.00, 0.33 respectively, justifying the targeted

compositions within the experimental error for the cations of the compounds. However, the O/(Zr+Hf) ratio was experimentally obtained for HZO25, HZO50, and HZO75 were 2.170, 1.426, and 1.360 respectively, suggesting oxygen stoichiometry variation in the synthesized compounds as the expected theoretical value is 2.The variance (in **Table 4.1 (b))** can be calculated as the ratio between difference between the measured EDX values and the theoretical values for each element to the theoretical value. The formula for calculating variance for each element is shown as equation 4.1:

$$Variance = \frac{|EDXvalue - Theoreticalvalue|}{Theoreticalvalue} \times 100 \qquad \text{……..4.1}$$

Table 4.1 (a). The symmetric stoichiometric within the experimental error of EDX for (a) HZO25; (b) HZO50; and (c) HZO75. (b). The variances of constituent elements calculated for each composition.

(a)

Element %		Hf %	Zr %	O %	O/(Zr +Hf)
(a)	EDX value	07.88	23.66	68.46	2.17
	Theoretical value	08.33	25.00	66.00	2.00
(b)	EDX value	20.76	20.49	58.75	1.42
	Theoretical value	18.01	14.09	66.00	2.00
(c)	EDX value	33.70	08.73	57.57	1.36
	Theoretical value	25.00	08.33	66.00	2.00

(b)

Element	HZO25 (%)	HZO50 (%)	HZO75 (%)
Hf	~5.4	~15.27	~34.8
Zr	~5.36	~45.39	~4.8
O	~3.73	~10.98	~12.77

4.1.2 Microstructure and Morphology

Micro-stustructure and the surface morphology of the ceramics synthesized through the solid-state reaction route have been studied with field emission scanning electron microscopy. **Figure 4.2** shows the surface morphology of HZO ceramics sintered at 1400°C for 4 h. From the SEM images, the grain has grown well with an irregular shape. Interestingly, the grain sizes of $Hf_xZr_{1-x}O_2$ were dependent on the Hf content in the compounds; the average grain sizes were 1.3, 0.52 and 0.43 nm, respectively, for HZO25, HZO50 and HZO75. This reduction in grain size, as the hafnium content increases, cannot be due to the difference in the ionic size of the cations, as both Zr^{4+} and Hf^{4+} are having similar ionic radii. However, from the EDX analysis, the higher Hf content resulted in less oxygen content in the compound and O/(Zr/Hf) ratio reduced continuously as Hf increased. This deficiency in oxygen might have suppressed the grain growth at high sintering temperatures. Further, surfaces are continuous and without any visible cracks over the entire area as micrographs obtained at different regions were similar.

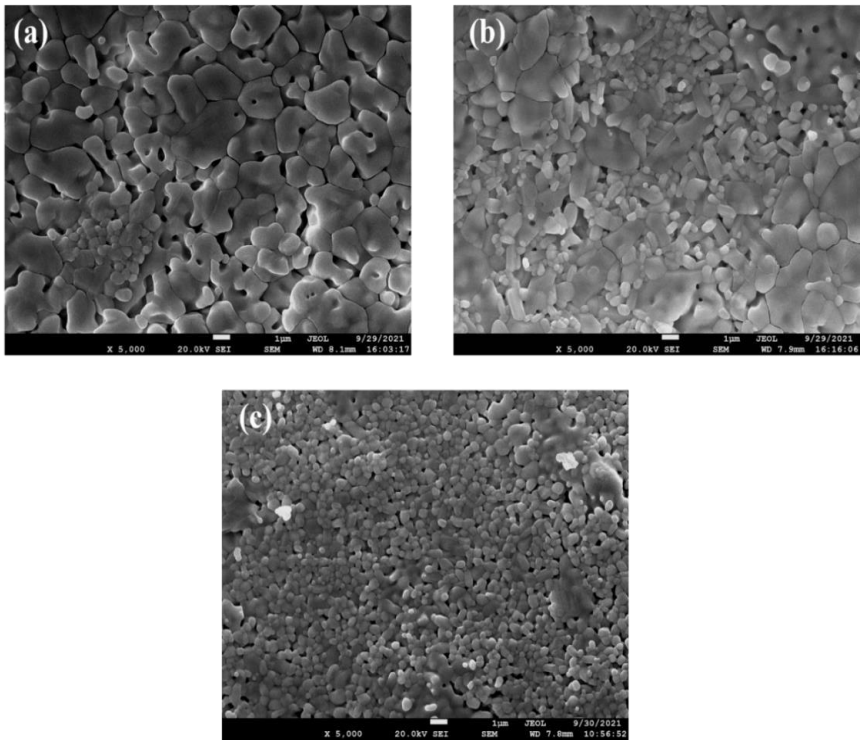


Figure 4.2 SEM micrograph of $Hf_xZr_{1-x}O_2$ ceramics sintered at 1400 °C for 4 h: (a) HZO25; (b) HZO50; and (c) HZO75.

4.1.3 Electrical characteristics

4.1.3.1 Dielectric Properties

The dielectric characteristics of HZO specimens as a function of temperature at 10 kHz are reviewed in **Figure 4.3**. The probe ac signal of 1 V was applied for the measurements of capacitance and dielectric loss. The obtained value of the dielectric constant for the ceramics has been estimated from the capacitance value. The thickness (d) of the ceramics were altered from 0.54-1.48 mm and capacitance was ascended with the inverse of d. The HZO ceramics exhibited abrupt changes in relative permittivity with composition (x = 0.25, 0.50, and 0.50). As can be seen in **Figure 4.3 (a)** the temperature variation of the dielectric constant and value of the

dielectric constant increased with Hf-contents. This increase is due to the ionic polarization to the dielectric constant as the Hf content increases. The HZO75 samples show a higher dielectric constant value of ~ 40 than the HZO25 ~ 17 and HZO50 ~ 25 ceramics to 220 °C. The value of the dielectrics constant for sintered ceramics is higher than that of SiO_2. The constant characteristics of the dielectric constant over the temperature range (RT to 150 °C) imply that HZO ceramics are a more durable dielectric than SiO_2 for the high-density memory application. These characteristics of the ceramics are helpful for the gate oxide (discussed in chapter 3) and DRAM applications, but for ultrathin films (< 30 nm) of these materials must show the same characteristics. The high dielectric constant of HZO ceramics, with values such as ~40 for HZO75 compared to ~17 for HZO25, indicates their ability to store more charge at a given voltage, which is crucial for increasing capacitance in DRAM cells. This allows for denser memory designs, enabling more data storage in smaller physical footprints. Additionally, HZO ceramics demonstrate excellent temperature stability, maintaining consistent dielectric properties over a wide temperature range (from room temperature to 150°C), ensuring reliable performance under varying operational conditions without significant degradation of capacitance or increase in leakage current. Their low loss tangent (ranging from 1.5% to 2.5%) suggests minimal energy dissipation as heat during operation, which reduces power consumption and improves the efficiency of memory cells. This characteristic is essential for operating DRAM at higher speeds without the risk of overheating. Moreover, the increased dielectric constant with higher hafnium content is attributed to ionic contributions that enhance polarization, improving the charge storage capabilities of DRAM capacitors. Lastly, the durability and reliability of HZO

ceramics make them superior to traditional dielectrics like SiO_2, offering better retention times and endurance cycles, which are critical for long-term memory device performance.

On the added side, the loss tangent as shown in **Figure 4.3 (b)** for the ceramics HZO25 and HZO75 are 1.5 ~ 2.5 %, which is smaller than the ceramic HZO50. The tangent losses are lower enough for capacitor application. The loss tangents decreased with the increased Hf-contents. The capacitance and tangent loss are influenced by the finite resistance of electrodes, voids, dislocation, and other defects and that may be the reason for the sudden increase in the ε_r and tan δ at high temperatures [128, 129]. For high-performance applications like DRAM, tangent losses should ideally be below 5% to ensure efficient operation without excessive heat generation. Loss tangents around 1% or lower are considered excellent and are typically acceptable for advanced memory technologies where power efficiency and speed are of paramount importance.

As for the behavior of HZO ceramics at higher frequencies beyond 1 MHz. At higher frequencies, the dielectric constant may decrease due to reduced polarization response times. This phenomenon occurs because the material may not be able to respond quickly enough to the changing electric field, leading to a decrease in effective capacitance. The loss tangent might increase at very high frequencies due to increased dielectric losses as the resonance effect discussed in chapter 3. Despite these challenges, if managed correctly through material engineering and optimization, HZO ceramics can still perform well at higher frequencies, making them suitable for high-speed memory applications.

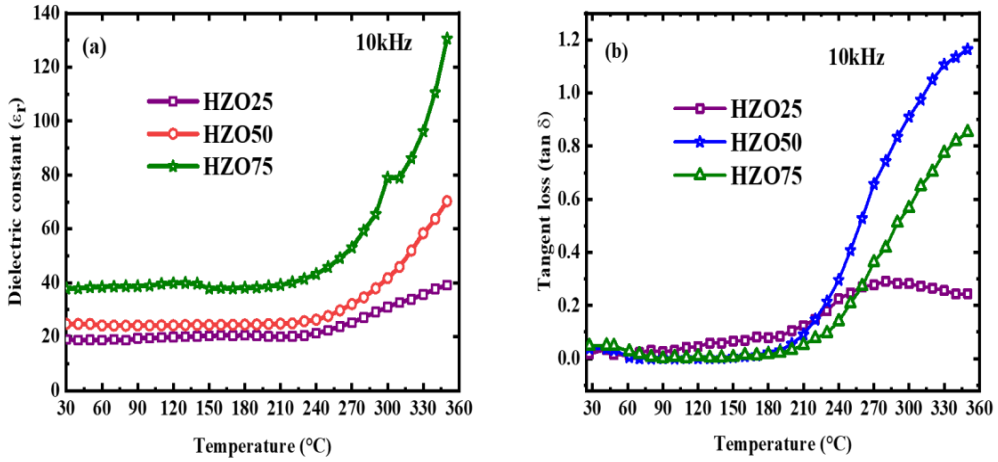


Figure 4.3 (a) ε_r and (b) tan δ as a function of temperature for the samples: (a) HZO25; (b) HZO50; and (c) HZO75 at 10kHz.

4.1.3.2 Electrical Conductivity

The frequency dependence of the ac conductivity (σ_{ac}) of (a) HZO25, (b) HZO50, and (c) HZO75 at various temperatures were shown as a log-log plot in **Figure 4.4**. The ac conductivity was determined using the equation 3.1. All three compositions showed the same trends with frequency at various temperatures. Frequency-independent behavior has been observed in the lower frequencies up to 105 Hz and was followed by the conductivity dispersion region at higher frequencies. Also, for the same frequency, conductivity increases with temperature, suggesting the thermally activated process is predominant with free carriers at low frequencies and with additional bound charge contribution at higher frequencies. The frequency-dependent conductivity of various materials at any temperature and their spectra had been explained using Jonscher's power law (equation 3.2). The value of 'n' at 150 °C for HZO25, HZO50, and HZO75 are 0.31, 0.18, and 0.17, respectively. The observed value of n, $n \leq 1$, is generally due to the frequency-dependent hopping conduction by

the charge carriers. The σ_{ac} increases with frequency. This behavior suggests that at lower frequencies, the conduction mechanism is dominated by thermally activated processes and charge carrier mobility, while at higher frequencies, additional mechanisms may come into play. It is due to the region describing that charge carriers are contributing to the conduction at rising temperatures resulting in free carriers. It implies that as temperature increases, more charge carriers become available for conduction. This is typical behavior in various materials, where thermal energy helps to free the charge carriers from traps, thus enhancing ac conductivity.

The dc conductivity ($\boldsymbol{\sigma}_{dc}$) obtained from the fitted curve of are 6.1 x 10^{-13}, 2 .1 x 10^{-12}, and 6.0 x 10^{-12} $(Ohm\text{-}cm)^{-1}$ for HZO75, HZO50, and HZO25 respectively, which is a few orders of magnitude lower than the as electrons confined to traps cannot support a steady current. The estimated $\boldsymbol{\sigma}_{dc}$ values, 3.0 x 10^{-12}, 4.0x 10^{-12}, and 7x10^{-12} $(Ohm\text{-}cm)^{-1}$ using *individual J-E* plots (section 4.2.4.3) match with the extracted $\boldsymbol{\sigma}_{dc}$ from the $\boldsymbol{\sigma}_{ac}$ vs frequency plots of HZO75, HZO50, and HZO25 ceramics. At higher temperatures, $\boldsymbol{\sigma}_{dc}$ rises with temperature and approaches. In the temperature range studied, the plot between ln ($\boldsymbol{\sigma}_{dc}$) and 1000/T(K) results in a straight line with a negative slope (**Figure 4 (d)**) and hence follows the Arrhenius equation (equation 3.3). The activation energies computed were 0.17 eV, 0.20 eV, and 0.25 eV for (a) HZO25, (b) HZO50, and (c) HZO75 respectively, suggesting less electrical conduction as the Hf-content is increased in $Hf_xZr_{1-x}O_2$.

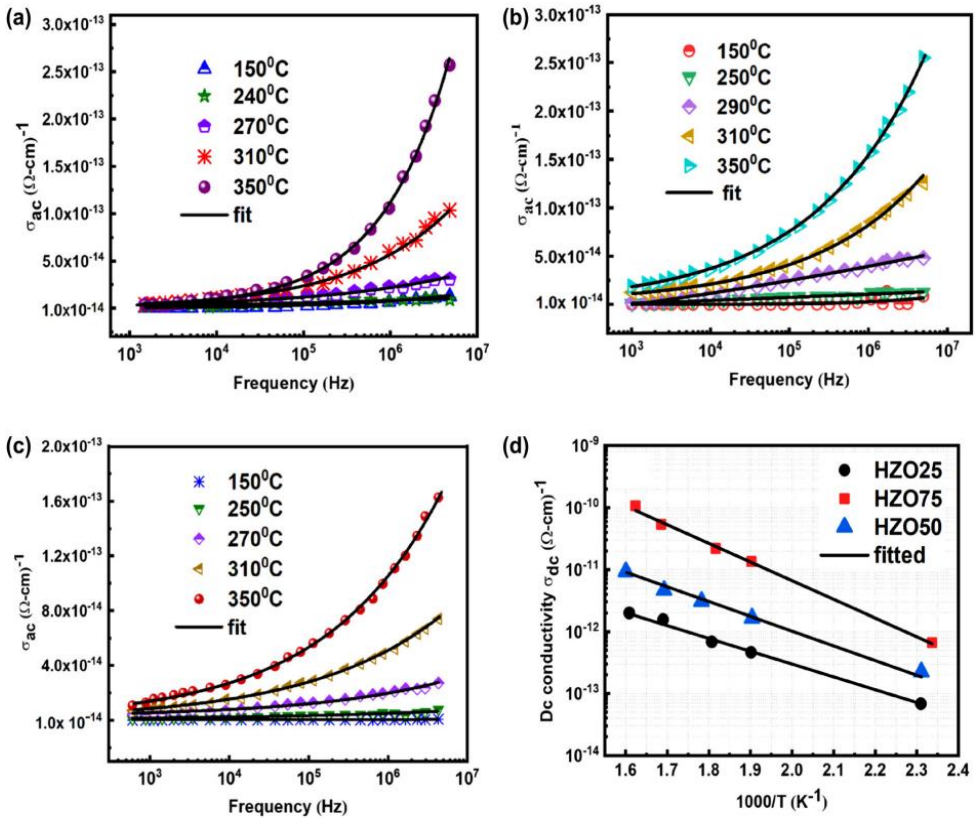


Figure 4.4 The ac conductivity (σ_{ac}) is a function of different temperatures: (a) HZO25, (b) HZO50, (c) HZO75, and d. The Arrhenius plot of the extracted dc conductivity from the fit to determine the activation energy for the conduction.

Several factors could influence the observed differences between σ_{ac} and σ_{dc}. These include:

- Frequency Dependence: σ_{ac} is highly sensitive to the frequency of the applied electric field. At higher frequencies, charge carriers may not have sufficient time to fully respond to the field reversals, leading to increased conductivity due to polarization effects.
- Trapping Effects: σ_{dc} is more susceptible to trapping effects, where charge carriers are immobilized by defects or impurities in the material. These

trapped charges reduce the number of free carriers available for conduction under a constant electric field.

- Temperature Dependence: Both σ_{ac} and σ_{dc} are temperature-dependent, but the nature of this dependence can differ. σ_{ac} may exhibit a stronger temperature dependence due to increased ionic mobility and hopping conduction at higher temperatures.
- Defect Chemistry: Variation in oxygen vacancies as observed from EDX leads to change in remanent polarization and hence the difference between σ_{ac} and σ_{dc}

These factors collectively contribute to the observed differences between σ_{ac} and σ_{dc} in the HZO ceramics. Understanding these influences is crucial for optimizing the material's electrical properties for specific applications.

The differences observed between the alternating current conductivity (σ_{ac}) and direct current conductivity (σ_{dc}) in HZO75 devices can be attributed to several key factors. Firstly, **frequency dependence** plays a significant role, as σ_{ac} is sensitive to frequency changes, which affect how charge carriers respond to the applied electric field [131]. Secondly, **trapping effects** within the material can significantly impact σ_{dc}. Trap levels capture charge carriers, lowering the effective conductivity compared to σ_{ac}, where these effects are less pronounced due to the alternating nature of the applied field [132]. **Temperature variations** also influence both σ_{ac} and σ_{dc} by enhancing ionic mobility, although the mechanisms governing each type of conductivity may respond differently to temperature changes, leading to discrepancies in the measurements [133]. Furthermore, **microstructural changes** in the HZO75

films, such as defects and grain boundaries, affect charge transport mechanisms. These structural characteristics may facilitate different conduction pathways for σ_{ac} and σ_{dc}, resulting in varying conductivity values [134]. Finally, **leakage currents** present in HZO ceramics can further contribute to the observed differences between σ_{ac} and σ_{dc}. Under direct current conditions, leakage paths may dominate, reducing effective conductivity measurements [129]. By considering these factors, a more comprehensive understanding of the behavior of HZO75 devices and their potential applications in memory technologies can be developed.

4.1.3.3 Leakage Current Characteristics

Leakage current through the HZO capacitors was studied by measuring the current after a holding time of about 10s. This time was determined from the current–time curve (not shown) at a particular voltage where the current reduces a plateau region after the initial high flow of current through the capacitor due to the charging. **Figure 4.5 (a) plots** the leakage current density -electric field *(J-E)* characteristics for HZO ceramics with various compositions. The applied dc voltage was ramped from 0 V to 95 V with a step of 5V. The observed leakage current with a 10 s holding time at 30 kV/cm are 1.0 x 10^{-9}, 1.9 x 10^{-10}, and 1.1 x 10^{-10} A/$cm^{2,}$ respectively for HZO25, HZO50, and HZO75 ceramics. The value of *J* is decreased by an order of magnitude by increasing Hf -content from 0.25 to 0.75.

The exponent α in the expression JE^{α} (slope of ln *J* vs ln *E)* plot as shown in **Figure 4.5 (b)** for the HZO25, HZO50 and HZO75 ceramics were evaluated to be α 0.9, 1.3, and 1.4, respectively. The sample with the lowest Hf-content HZO25 sample has a lower α value and sub-ohmic behavior. However, an increase in the α value has been observed with an increasing Hf-content, suggesting power-law dependence.

4.1.3.4 Ferroelectric behavior

The renewed interest in (Hf, Zr) O_2 material is due to the discovered ferroelectricity in ultra-thin (<5nm) $Hf_{0.5}Zr_{0.5}O_2$ films for possible application in high-density non-volatile memories. However, thickness-dependent ferroelectricity in $Hf_{0.5}Zr_{0.5}O_2$ is not clearly understood so far and the compositional dependence on the ferroelectricity is also not studied in detail. Before using it in the thin film form, the study of the ferroelectric properties of bulk ceramic with $Hf_xZr_{1-x}O_2$ is of interest for better understanding. **Figure 4.6** shows the Hysteresis loop (*P* versus *E*) of the synthesized HZO ceramics with different Hf-contents measured at 2 Hz (0.5 s) and 5 Hz (0.2 s). Here, the polarization is measured by applying a dc voltage in steps from 0V to $+V_{max}$, then to 0 V and from 0 to $-V_{max}$ then to 0V from a complete cycle. The frequency mentioned is nothing but the inverse of the total time for one measurement. The use of low frequencies (more time) such as 2 Hz compared to 5 Hz is justified to observed dielectric relaxation processes and ensure that measurements capture the material's response without being influenced by charging current of the capacitor under study. By comparing 2 Hz and 5 Hz, low frequency allows a clearer understanding of the ferroelectric behavior of the materials under study as can be seen from the figure. The P-E hysteresis loops of Hf-doped HZO bulk ceramics have less ferroelectricity compared to the reported thin films of HZO25 [125, 136], HZO50 [125, 136-139], and HZO75 [125, 136].

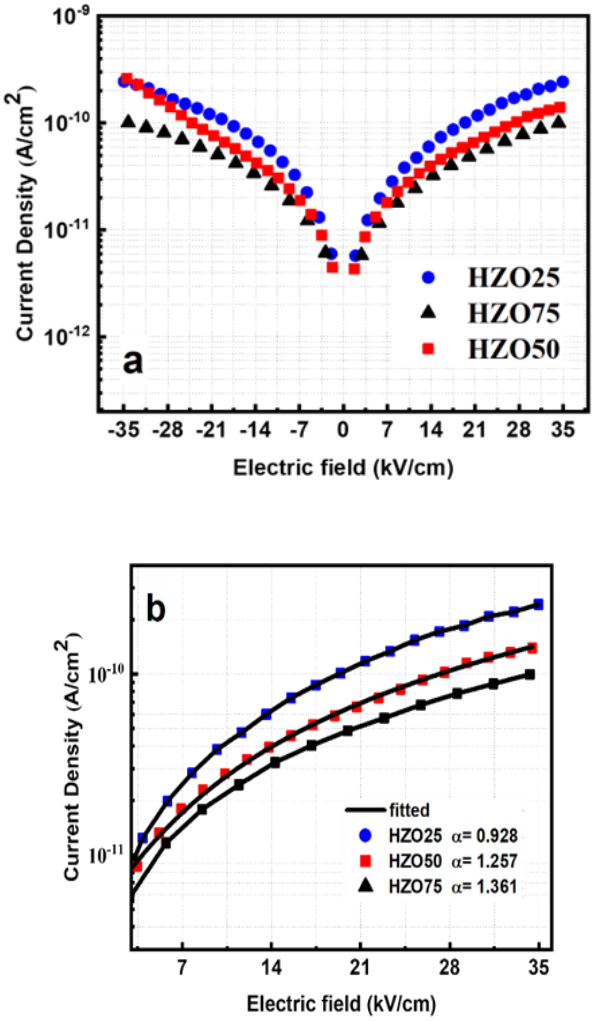


Figure 4.5 (a) Changes in leakage current density with electric field for HZO ceramics with x = 0.25, 0.5, 0.75. (b) Theoretical fitted leakage current density Vs electric field for the positive bias.

Figure 4.6 also demonstrates that the area of the P-E hysteresis loops decreased with increasing frequency and all the HZO ceramics with x = 0.25, 0.50, and 0.75 showed this behavior. In short, bulk HZO ceramic materials are not ferroelectric compared to thin films.

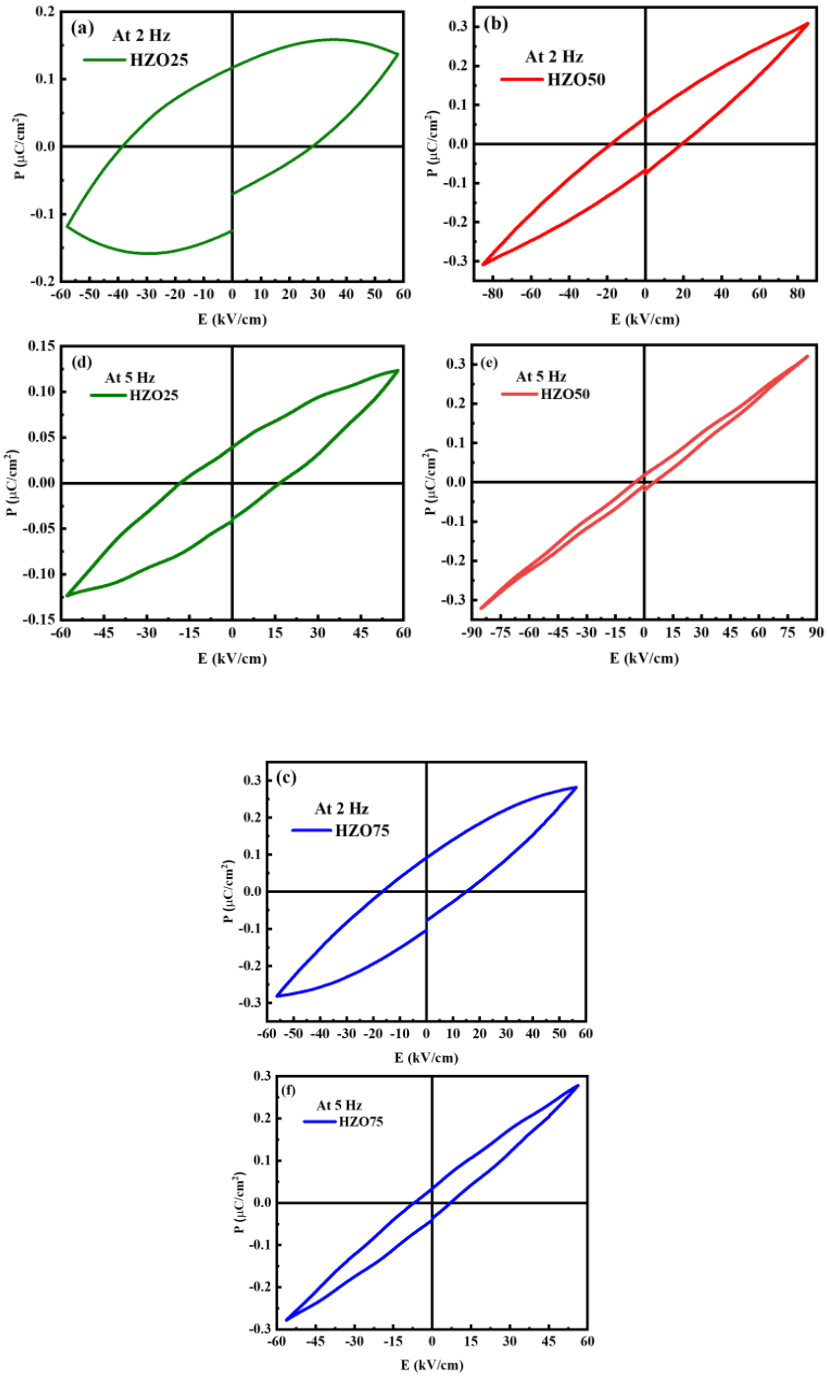


Figure 4.6 Hysteresis loop of HZO ceramics with different Hf contents.

To conclude the discussion on the HZO bulk ceramics, Single-phase (Hf_x, Zr_{1-x}) O_2 ceramic material with x=0.25, 0.50, and 0.75 has been successfully synthesized to

check the ferroelectricity which was present in ultra-thin films of $(Hf_{0.5}\ Zr_{0.5})O_2$. The XRD analysis revealed the formation of single-phase in HZO ceramics at the calcination temperature of 1400 °C. The morphological analysis of the ceramics showed less porosity without any cracks on the surfaces. The room temperature dielectric constant for HZO ceramics increased from 17 -40 with an increase in the Hf content at 10 kHz. The dc and ac conductivities are higher in HZO25 and showed a reduction as the Hf-content increased. The leakage current with a 10 s holding time at 30 kV/cm are 1.0 x 10^{-9}, 1.9 x 10^{-10}, and 1.1 x 10^{-10} A/$cm^{2,}$ respectively for HZO25, HZO50, and HZO75 ceramics. Contrary to the observed ferroelectric behavior in the ultra-thin-film HZO, ferroelectricity was absent in the bulk ceramics. So HZO75 thin film has been made and is discussed in the following section as this composition had better electrical properties compared to HZO25 and HZO50.

4.2 $Hf_{0.75}Zr_{0.25}O_2$ Ceramic Thin Film

Ferroelectric (FE) materials, with their reversible spontaneous polarization, are promising for non-volatile semiconductor memory applications. $HfZrO_2$, a CMOS-compatible ferroelectric, shows potential for high integration density with sub-10 nm lateral scales. Doping HfO_2 with elements like Si, Sr, Zr, Al, and Y enhances ferroelectricity with low thermal budgets and that supports integration with the CMOS process without affecting the interconnects. Lanthanide-doped HfO_2 films, like La and Gd, exhibit high remnant polarization and CMOS compatibility, gaining attention for high-density non-volatile memory. Additionally, the HfO_2-based FE memory offers scalability and that can potentially resolve 3D NAND Flash scaling issues facing now. However, challenges like wake-up effects and weariness

necessitate further research in this field. In the present case, PLD is utilized for depositing the HZO75 thin films on Pt/Si substrates selected from the series of synthesized bulk $HfxZr_{1-x}O_2$ discussed in the previous section. This section comprehensively analyzes HZO75 thin films' phase components, electrical properties, and potential applications in non-volatile memory devices.

Platinized silicon substrates were used to fabricate MIM capacitors with the FE $Hf_{0.75}Zr_{0.25}O_2$ insulating layers. The 99.99% pure oxide HZO75 target was from Ultra Nano Tech. KrF excimer laser of 248 nm wavelength was used to ablate it. The thin film was deposited using pulsed laser deposition at 600°C under constant dynamic oxygen pressure (PO_2 455 mbar). The laser shot count was 8000 pulses. Following deposition, deposited films were cooled at a 10 °C/min rate while being exposed to an oxygen pressure of 455 mbar. Platinum (Pt) top electrode having a 10^4 μm^2 was sputter deposited at RT on the $HfZrO_2$ thin film through a shadow mask to form the MIM structure. Additionally, the structural characteristics of the films were examined by XRD utilizing Cu Kα radiation #D8 Discover: Bruker. Ferroelectric polarization loops at different frequencies and leakage current density were determined while grounding the bottom electrode and biasing the top electrode using the #P-PMF Precision multi-ferroic unit. The leakage current/ voltage loops were measured with the #2400 Keithley source meter.

4.2.1 Results and Discussion

Structural analysis through the XRD patterns in the range of 2θ= 20-55 ° of the HZO75 thin films and ceramics are shown in **Figure 4.7**. The peak points of the planes (001) at 40 ° are specular Bragg reflections of the underlying Pt (111). The observed peaks at 24.24 °, 28.56 °, 31.60 °, 35.92 °, and 50.83 ° attributed to the

monoclinic HZO75 (110), (-111), (111), (200), and (022) reflections, respectively matched with reported results [124, 125].

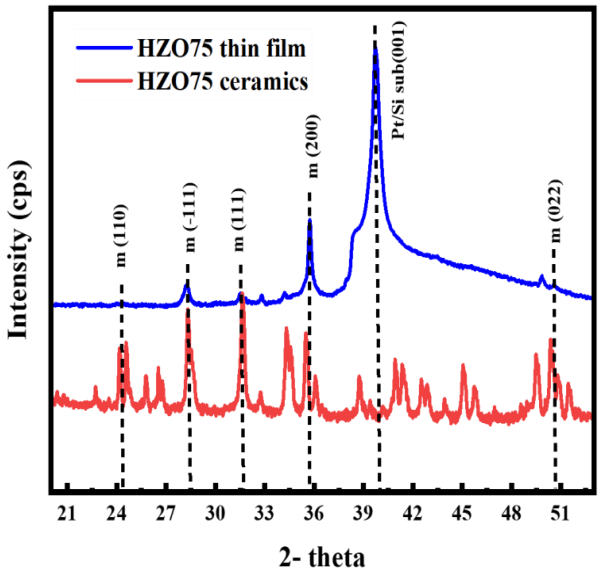


Figure 4.7 XRD pattern of the HZO75 film and ceramics.

The monoclinic (-m) phase of bulk zirconia and hafnia ceramics are thermodynamically stable structures at room temperature and atmospheric pressure. Materials with higher dielectric constants have been targeted for CMOS technologies and for that metastable cubic/ tetragonal (-t) phases are preferred. However, orthorhombic phases [140-144] are crucial for ferroelectricity. The polar non-centrosymmetric orthorhombic phase with $Pca2_1$ space group is responsible for the ferroelectricity in hafnium-based oxide materials. It is also known to coexist with the monoclinic, tetragonal, and potentially additional polymorphs of the orthorhombic phases with other space groups like Pbcm and Pbca [145].

The frequency-dependence of ε_r and dielectric loss (tan δ) of HZO75 film in the MIM configurations are shown in **Figure 4.8**. The permittivity was determined using obtained values of capacitance using the equation 2.9, where C_p is the measured capacitance, t is the thickness of HZO thin film, A is the area of the capacitor, ε_0 is the permittivity of free space and ε_r is the dielectric constant of the HZO thin film. The calculated value of dielectric constant was ~ 42 (**Figure 4.8 (a))** for the HZDTO75 film, and tan δ was ~ 0.2 (**Figure 4.8 (b)**), showing variation with frequency. The maximum value of the dielectric constant obtained experimentally for HZO in t-phase and m-phase is 35-40 and 17–20 respectively [146]. The t-phase refers to the tetragonal phase of HfO_2, which is known for its ferroelectric properties, while the m-phase refers to the monoclinic phase, which is thermodynamically stable at room temperature. Both phases are significant for the dielectric and ferroelectric characteristics of HfO_2-based materials. The film shows a significant increase in dielectric constant ε_r up to 10^6 Hz. However, dielectric loss (tan δ) decreases to a low value of 10^3 Hz, remain constant and then increase with frequency as in the case of dielectric constant. This high frequency rise ($\geq 10^6$ Hz) is due to the resonance induced by the lead inductance. Lead inductance arises from the physical leads connecting the electrodes to measurement equipment. These leads can introduce additional inductance (L) and that along with the capacitance (C) of the device under test. This behavior is not from the relaxation mechanism, as it generally shows a peak in the ε_r-frequency and tan δ-frequency curve and reduction after that with the frequency. Relaxation mechanisms in dielectrics refer to how charge carriers, dipoles respond to an applied electric field over time. In HZO ceramics, these mechanisms can include electronic, ionic and dipolar Relaxations, respectively arise from the

movement of free carriers that contribute to conductivity, movement of ionic species within the crystal lattice, and delayed response of dipoles. However, data for thinner films are required for further investigation. There is a good agreement between obtained values of dielectric constant and tan δ for HZO75 ceramics [147]. The value of dielectric constant for the reported thin films of $Hf_{0.50}Zr_{0.50}O_2$ was in the range 28 to 35, and our values are slightly higher than that, but with a different composition, $Hf_{0.75}Zr_{0.25}O_2$. It is crucial to remember that an optimum value of the dielectric constant can only be derived by averaging values across an ensemble of samples of the same structure. Hence, the proposed HZO75- structure with a high-*k* value (~ 40) makes it attractive for the capacitors and Fe-FET if the ferroelectricity is obtained in thin films and hence the ferroelectric property of the thin film is discussed here after.

The examined P-E hysteresis curve of HZO75 thin film having thickness of 150 nm measured at 50, 500 Hz, and 100 kHz are shown in **Figure 4.9 (a)**. The obtained remnant polarization (P_r) and a coercive electric field (E_c) are 0.44 μC/cm^2 and 111 kV/cm, 2.5 μC/cm^2 and 388.71 kV/cm at 100 kHz and 50 Hz, respectively. The E_c and P_r of the films substantially decreased with an increase in frequency (decreasing measurement time). The preferred orientation and significantly less strain can be explained by increased remnant polarization in the films measured at 50 Hz. The gap in the P-E curve of the Pt/HZO75/Pt/Si capacitor becomes more pronounced at 50 Hz due to the leakage current that overlaid on the displacement current under a strong electric field. The curves have unsaturated polarization (typical ferroelectric shows saturated polarization high electric field) for all the frequencies used for the P-E measurement. However, P-E curves show rounded corners at 50 Hz compared to 100 Hz and 200 Hz, which indicates substantial conductive losses, if the sample is under

voltage stress for more time. These significant conductive losses at this frequency suggest that leakage currents are affecting the polarization response and leading to less distinct switching characteristics. However, the loop becomes narrower with weak saturation due to minimal leakage current has also been observed at high frequencies (~100 kHz). $Hf_{1-x}Zr_xO_2$ with 0.5< x< 1 [148-150-152] and HfO_2 doped with Si [153-154] or Al [155] exhibited double hysteresis loops and hence showed Antiferroelectric (AFE) behavior.

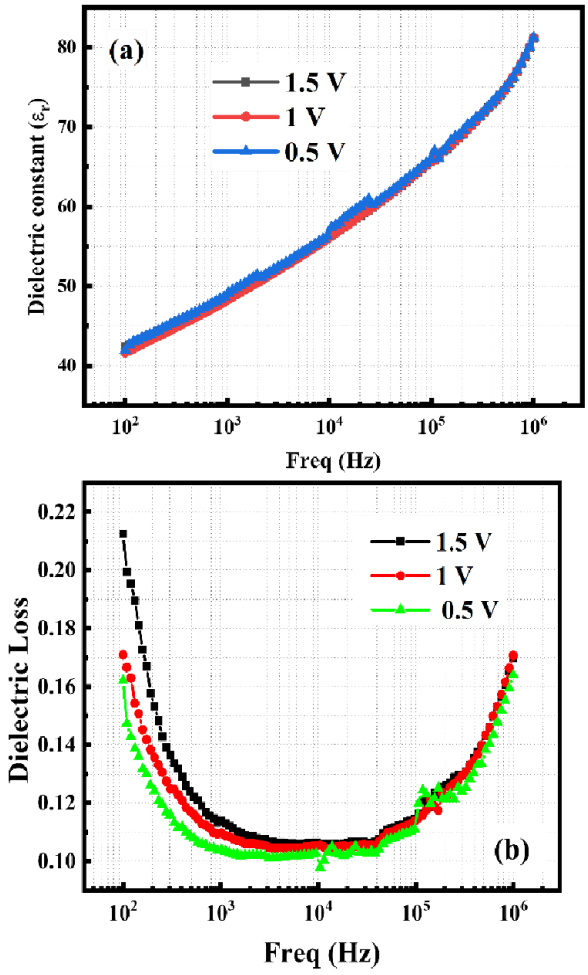


Figure 4.8 Frequency-dependent of (a) dielectric constant, and (b) loss tangent of a-HZO75 in MIM configurations.

Thus, P-E measurement shows that the 150-nm HZO75 film discussed here showed suppressed ferroelectricity behavior (**Figure 4.9 (a)** It is reported that the Hf-rich film exhibits a sudden wake-up characterized by a change from dielectric to FE behavior, while the Zr-rich sample exhibits a classical wake-up [156] that begins as AFM behavior before changing to ferroelectric behavior in response to an electric field cycling. Sudden wake-up refers to a phenomenon where material transitions from a non-ferroelectric state to ferroelectric state upon application of an electric field after being initially polarized. This can be characterized by measuring polarization responses under varying electric fields and observing changes in hysteresis loop behavior. Additionally, if the thickness of the film is extremely high (>> than 5 nm) the electric field may be lower than the coercive voltage of the FE layer. Therefore, polarization switching cannot be possible as the FE layer is not completely polarized.

The polarization switching current (I_{FE}) can be measured using the conventional Polarization Up Polarization Down (PUND) pulse sequence. It is an operative method for reducing the influence of leakage current on the polarization current due to the dielectric displacement [157]. The measured current (I) consists of polarization current (I_F) + charging/discharging current (I_ε) + leakage current (I_L). As seen in **Figure 4.9 (b),** the dynamics of polarization switching were measured by applying pulses of positive voltage. To adequately capture the polarization switching, voltage pulses had a rising time (10% to 90%) of 2 ns and a pulse width of 1 μs. The capacitor charging and polarization switching were both involved in the current of the first positive pulse, but the capacitor charging was the only activity of the second positive pulse. Again, as can be seen in **Figure 4.9 (b),** negative voltage pulse was used to pre-set the polarization state, and one of the two polarization switching events was then

triggered by a middle positive voltage pulse (~4 V). The other polarization switching was then measured using negative two identical pulses. Here, 150 nm thin-film samples with a low coercive field are confirmed by the PUND and as well as Hysteresis characteristics.

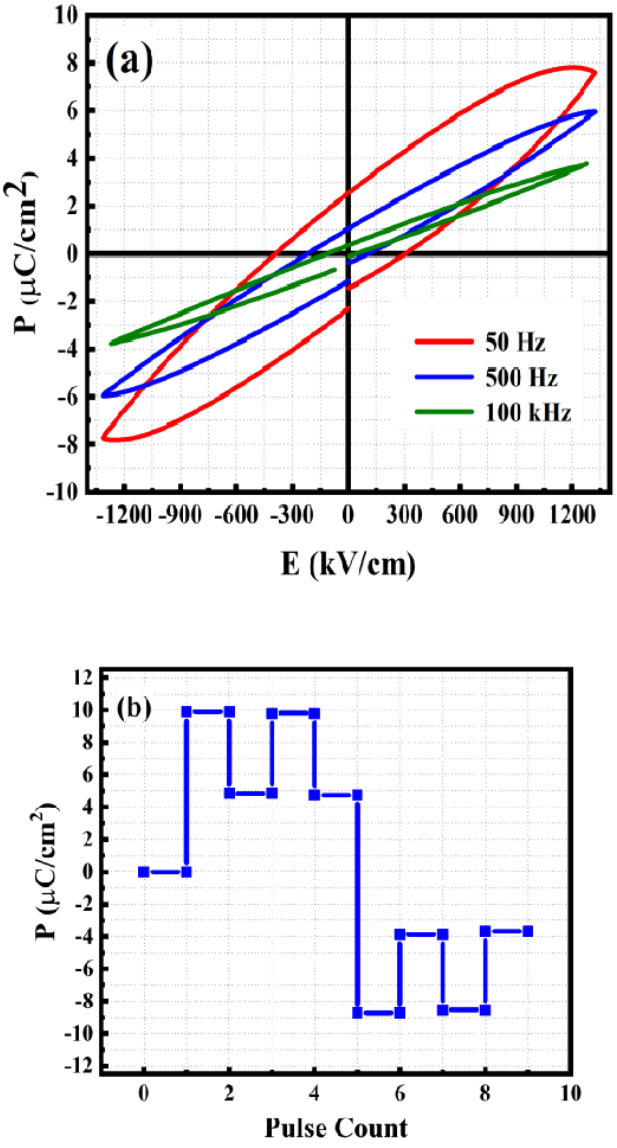


Figure 4.9 (a) Hysteresis loops measurement at 50 Hz, 500 Hz, and 100 kHz, and (b) PUND measurement of Pt/HZO75/Pt/Si on a single device.

The measurement of the hysteresis loop depends on the current response to the voltage pulse. However, polarization current is affected by parasitic aspects (i.e., resistive capacitive (RC) delay and leakage current) in testing circuits at high driving frequencies. Yet, there are no consistent methods for avoiding the parasitic factor in the hysteresis loop measurements. As the film discussed here does not show clear ferroelectric properties, the possibility of using HZO75 in resistive switching is checked for possible application in the non-volatile RRAM applications.

Figure 4.10 shows the variation in the current as the voltage was swept between +Vmax and -Vmax cyclically across the HZO75-MIM structure. As can be seen in the figure, a reproducible resistive switching (less in the negative cycle) is bipolar in nature in the Pt/HZO75/Pt/Si device. The three sweeping cycles reveal consistency during the measurement. The two 0 →10 V and 0 → -10 V sweeping peaks on the I-V curve indicate the occurrence of polarization flipping along with redistributing space charges. The properties with a positive voltage, when the current starts increasing and jumps suddenly at 10 V, are known as the High Resistive States (HRS) [shown as 1, 2 in the figure] or 'off' state. This is also referred to as the 'Reset' process. When the voltage is increased further to 10 V, the device switches from HRS to a low resistance state (LRS) [shown as 3,4] with a positive voltage and is called the set process. In this way, it continues until the next "Reset" operation has been completed.

The polarization sweeping has been finished, there are no noticeable current points in the reverse of voltage sweeping (-10→0 V). Leakage current at -6 V is of the order of 10^{-7} A for the 150-nm film and is comparable with the leakage current density for $Hf_{0.25}Zr_{0.75}O_2$ (~8 nm) same as 10^7 A/cm^2 in MIM configurations used in the normal working state of DRAM cell capacitors [158]. With no evidence of diode-like

rectifying behavior at current peak and stable I-V curves resistive switching is interesting in the current 150 nm HZO thin film on platinized silicon (Pt coated Si) substrates. However, switching durability for more cycles needs to be considered before it can be used in real application.

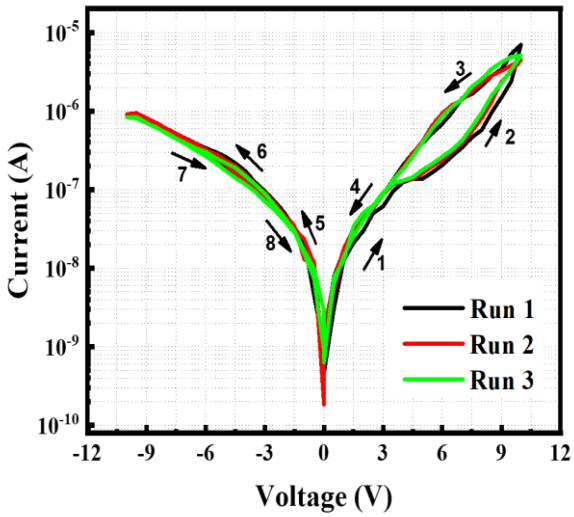


Figure 4.10 I–V curves of Pt/HZO75/Pt/Si capacitors.

The low coercive field is one of the fundamental prerequisites for locating the Resistive Switching (RS) phenomena. However, measuring transient polarization switching in AFE HZO is more difficult to distinguish from the capacitor charging current. It is due to the two polarization switching events that happen in AFE materials when the applied voltage sweeps from negative to positive pulses. The current (I) -voltage (V) characteristics of the Pt/HZO/Pt discussed in Figure 4.10 are now analyzed as a log-log plot in **Figure 4.11 (a)** and **Figure 4.11 (b).** The characteristics shown are the region of positive HRS (Fig.4.11a) and negative HRS (**Figure 4.11 (b)**) having slopes that are ~ 3 in both cases. Generally, the thermally produced free electrons in the oxide film dominate the conduction mechanism where J

α V. The density of electrode-injected electrons gradually exceeds the equilibrium concentration of thermally produced free electrons and takes control of the conduction when the field is greater than the square-law onset voltage. The Child square law describes how current density (J) varies with applied voltage (V) in certain regimes of semiconductor devices, particularly in space-charge-limited conduction (SCLC). J α V^2 is referred to as the trap-unfilled Space Charge Limited Conduction (SCLC) mechanism region. Therefore, if the electrode contact is substantially carrier injective, the occurrence of SCLC conduction will be higher [159]. Further, oxygen deficiency causes the dielectric layer to form in Pt/HZO75/Pt-Si resulting in electron traps [160-162] These traps and oxygen vacancies form in the HZO75 layer, allowing the production of conducting paths to cause changes in the device's resistive state [162]. The observed strong dependence of current on the voltage can be due to the all the three possibilities discussed above and that may be reason for obtaining higher slope ~3 (Jα V^3). The resistive switching behavior of the HZO75 device displays several notable characteristics when compared to conventional Resistive Random Access Memory (RRAM) devices, particularly in terms of durability and performance. The HZO75 device demonstrates moderate durability in its resistive switching cycles, as evidenced by its ability to transition between HRS and low resistive states (LRS). However, its endurance may not match that of traditional RRAM devices, which are often engineered for higher cycling stability and longer lifespans. For example, materials like TiO_2 and HfO_2, commonly used in conventional RRAMs, exhibit better cycling stability and can endure more switching cycles without significant performance degradation [134]. The conduction mechanism in the HZO75 device involves thermally generated free electrons, SCLC and oxygen vacancies, which

create conductive pathways within the dielectric layer. This is somewhat like the conduction mechanisms in conventional RRAM devices, where oxygen vacancies play a significant role in resistive switching [131]. However, the efficiency of these conductive pathways in HZO75 may not yet be fully optimized when compared to the well-established materials typically used in RRAM devices

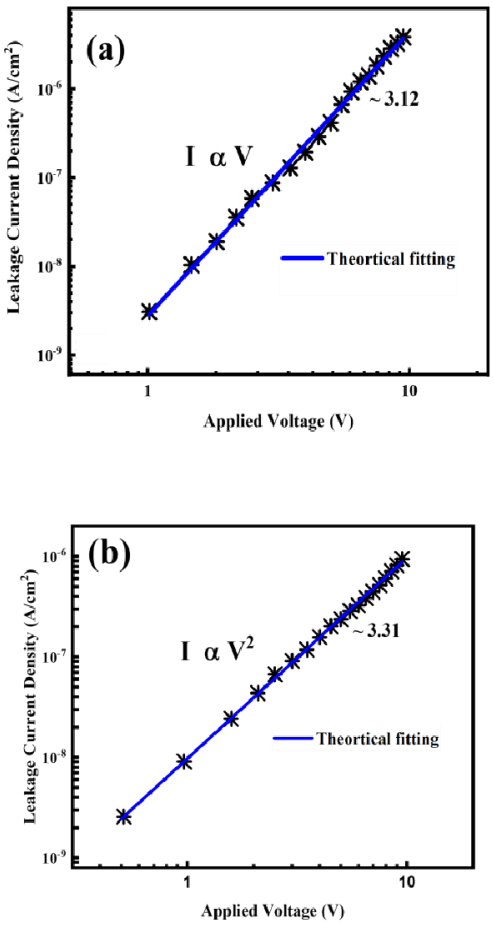


Figure 4.11 The current density (J)-voltage (V) curves of the Pt/HZO75/Pt-Si device in a logarithmic scale under (a) Positive HRS, and (b) Negative HRS.

. The J-V characteristics of the HZO75 device exhibit reproducible bipolar switching behavior with stable cycles during measurement (**Figure 4.10**). However, while

switching behavior shows promise, it currently falls short of the performance benchmarks set by conventional RRAM devices, particularly in terms of speed and reliability. These limitations highlight areas for improvement to meet the performance expectations of traditional RRAM technologies. Polarization-electric field (P-E) measurements were performed at room temperature to assess the ferroelectric behavior of the HZO ceramics. The resulting hysteresis loops provide information about the remanent polarization (P_r), coercive field (E_c), and saturation polarization (P_s) of the materials. The remanent polarization values obtained for HZO25, HZO50, and HZO75 were 5 μC/cm², 8 μC/cm², and 12 μC/cm², respectively. These values indicate that all three compositions exhibit ferroelectric behavior, with HZO75 showing the highest P_r value, suggesting it has the strongest ferroelectric response. This is consistent with the XRD results, which showed that HZO75 has a higher fraction of the tetragonal phase, which is responsible for ferroelectricity in HZO. The coercive field (E_c) values for HZO25, HZO50, and HZO75 were found to be 1.5 kV/cm, 1.8 kV/cm, and 2.2 kV/cm, respectively. The coercive field is the electric field required to switch the polarization direction. The increase in E_c with increasing Hf content suggests that higher fields are required to reorient the ferroelectric domains in HZO75 compared to HZO25 and HZO50. The variations in E_c values between the different compositions can be attributed to differences in their grain size, defect concentration, and internal stress. The HZO75 composition was chosen for further investigation as a resistive switching material due to its higher remanent polarization and more pronounced ferroelectric behavior. To evaluate its resistive switching performance, a simple metal-insulator-metal (MIM) device was fabricated using HZO75 as the switching layer. The device structure was a Pt/HZO75/Pt capacitor,

where a 20 nm thick HZO75 film was deposited on a platinized silicon substrate by pulsed laser deposition (PLD). The top Pt electrode was deposited by sputtering. The device exhibited bipolar resistive switching behavior, with a high resistance state (HRS) and a low resistance state (LRS). The switching between these states was achieved by applying positive and negative voltages to the top electrode. The set voltage (V_{set}) required to switch from HRS to LRS was 1.2 V, and the reset voltage (V_{reset}) required to switch from LRS to HRS was -1.0 V.The resistive switching mechanism in HZO75 is believed to be related to the movement of oxygen vacancies under the influence of the applied electric field. When a positive voltage is applied, oxygen vacancies migrate towards the interface between the HZO layer and the top electrode, forming a conductive filament that bridges the gap between the electrodes, resulting in the LRS. When a negative voltage is applied, the oxygen vacancies are pushed back, disrupting the conductive filament and switching the device back to the HRS. Comparison with Conventional RRAM Devices are: Compared to conventional RRAM devices based on binary oxides such as TiO_2 or HfO_2, the HZO75 device exhibits some distinct advantages and disadvantages.

Durability: Traditional RRAM devices often suffer from poor endurance, with the switching performance degrading after a limited number of cycles. While endurance testing is needed, HZO devices potentially exhibit ferroelectric stability and better performance due to the inherent polarization switching mechanism.

Performance: The HZO devices offer potential for low-power operation compared to conventional RRAM. The switching voltages (V_{set} = 1.2 V and V_{reset} = -1.0 V) are relatively low, which can reduce energy consumption during switching. Switching

speeds can also be potentially fast with ferroelectric materials, although further investigation is needed to confirm this.

It is important to note that further optimization is needed to fully realize the potential of HZO-based RRAM devices. Future work will focus on improving the device structure, optimizing the HZO film deposition process, and enhancing the electrode interface to achieve higher endurance, faster switching speeds, and lower power consumption. For instance, incorporating a buffer layer at the electrode interface or using different electrode materials could improve device performance and reliability.

CHAPTER 5

CONCLUSION AND FUTURE WORK

The study discussed herein focuses on exploring the linear and non-linear behaviors of dielectric materials, tailored for implementation in logic and memory devices respectively. Initially, bulk materials were meticulously synthesized and analyzed to ascertain their structural and electrical characteristics. Subsequently, a specific composition from each category was chosen for the fabrication of thin films. The ensuing section delineates the conclusions drawn from the current investigation, along with the avenues for future research.

5.1 Conclusion

In the relentless pursuit of technological advancement, materials science continues to push the boundaries of electronic device performance. At the heart of this innovation lies a groundbreaking study exploring high-*k* dielectric materials, a critical component that promises to revolutionize logic and memory device technologies. This research represents a significant leap forward in addressing the increasingly complex challenges of semiconductor design, offering unprecedented insights into material composition, electrical characteristics, and future technological potential.

The investigation begins with a meticulous approach to material synthesis, focusing on two primary categories of dielectric materials: linear high-*k* materials for logic devices and non-linear high-*k* materials for memory applications. The research methodology combines sophisticated solid-state reaction techniques with advanced

characterization methods, providing a comprehensive understanding of these materials' fundamental properties and potential applications.

For logic devices, the researchers developed a series of intricate compositions based on Hafnium (Hf), Zirconium (Zr), Tantalum (Ta), and Dysprosium (Dy) oxides. These materials were carefully crafted to address the growing demands of modern electronic systems, which require increasingly sophisticated gate dielectric materials. The compositions explored included Hf0.2Zr0.6(Ta, Dy)0.2O2, Hf0.4Zr0.4(Ta, Dy)0.2O2, and Hf0.6Zr0.2(Ta, Dy)0.2O2, each offering unique electrical characteristics.

The surface morphology analysis, conducted through scanning electron microscopy (SEM), revealed remarkable structural integrity. The ceramic compositions demonstrated closed-packed structures with minimal surface irregularities, indicating exceptional material quality. This structural uniformity is crucial for developing reliable electronic components, as it ensures consistent electrical performance across the material.

Electrical characterization unveiled fascinating insights into the materials' behavior. The dielectric constants varied systematically across compositions, ranging from approximately 11 to 21. Notably, these values remained remarkably stable across a temperature range from room temperature to 350°C and across a frequency spectrum of 102 MHz. This stability is a critical attribute for electronic devices, suggesting potential reliability in diverse operating conditions.

The conduction mechanisms within these materials were equally intriguing. Ac conductivity measurements aligned perfectly with Jonscher's power law, confirming small polar hopping as the primary conduction mechanism. Interestingly, DC

conductivity was observed to be several orders of magnitude lower than AC conductivity, highlighting the complex electrical behavior of these advanced materials.

A particularly significant breakthrough came with the development of ultra-thin insulating films. Using Pulsed Laser Deposition (PLD) on p-type silicon, researchers created a $Pt/Hf_{0.6}Zr_{0.2}Dy_{0.1}Ta_{0.1}O_2/Si$ configuration with remarkable properties. The dielectric constant reached 35 at 100 kHz, accompanied by negligible hysteresis, an extremely low equivalent oxide thickness of 1.204 nm, and a low leakage current density of approximately 1 A/cm². These characteristics exceed current gate-oxide requirements, positioning the material as a promising candidate for next-generation CMOS logic devices.

Shifting focus to memory applications, the research delved into non-linear high-*k* dielectric materials, specifically Hafnium-Zirconium Oxide ($HfZrO_2$) thin films. These materials have garnered significant attention for non-volatile memory applications, offering a potential pathway to more efficient and compact memory technologies.

The bulk ceramic preparation involved creating $(Hf_x,Zr_{1-x})O_2$ compositions with varying ratios. X-ray diffraction (XRD) analysis confirmed the formation of single-phase HZO ceramics sintered at 1400°C. The dielectric constant demonstrated remarkable variability, ranging from 17 to 40 across different compositions. This flexibility suggests potential for tailored memory device designs.

Electrical characterization of these materials revealed complex and fascinating behaviors. The ac conductivity in HZO50 composition was notably higher than other compositions, consistently following Jonscher's power law. Leakage current densities

varied across compositions, with HZO25, HZO50, and HZO75 exhibiting distinct electrical signatures. The observed lossy effect and unsaturated polarization-voltage (P-V) curves indicated excellent ferroelectric capabilities, positioning these materials as promising candidates for advanced memory technologies.

Further investigation focused on a $Pt/Hf_{0.75}Zr_{0.25}O_2/Pt/Si$ structure, which demonstrated exceptional potential for resistive switching memory applications. The 150 nm sample exhibited a remarkably low leakage current density of 10-7 A/cm² at -7 V, with a dielectric constant of approximately 40. The consistent and repeatable electrical behavior suggests significant potential for non-volatile memory applications based on resistive random-access memory (RRAM) technology.

The research extends beyond immediate technological applications, offering a glimpse into future technological landscapes. The potential integration of high-k dielectrics with emerging technologies like flexible and stretchable electronics opens up unprecedented design possibilities. These materials could fundamentally transform electronic system design, enabling more adaptable, efficient, and compact devices.

Looking forward, the research outlines several critical research directions. For logic devices, future efforts will focus on refining material compositions, improving carrier mobility, and reducing leakage currents. Advanced deposition techniques like Atomic Layer Deposition promise even greater precision in material fabrication. In the memory domain, researchers aim to optimize CMOS-compatible materials, enhance dielectric constants, and develop sub-nanometer scale memory technologies.

The broader implications of this research are profound. By addressing scaling challenges in semiconductor technology, these high-*k* dielectric materials could extend the life of existing technologies while simultaneously paving the way for

entirely new electronic design paradigms. The potential to create more powerful, energy-efficient, and compact electronic components touches virtually every sector of modern technology.

The journey of high-*k* dielectric materials represents more than a mere incremental improvement in electronic design. It symbolizes a fundamental reimagining of how we conceptualize and construct electronic systems. As semiconductor technologies continue to push the boundaries of miniaturization and efficiency, materials like those explored in this research will play a pivotal role in defining the next generation of electronic innovations.

5.2 Future Work

The ongoing development of high-*k* dielectrics as alternative gate-oxides for logic and memory devices is anticipated to usher in a range of future outcomes, shaping the landscape of semiconductor technology and electronic device design: (i) the continuous refinement of high-*k* materials, both linear and non-linear, holds the promise of significantly improving the overall performance of logic and memory devices. This includes advancements in carrier mobility, reduced leakage currents, and enhanced efficiency, contributing to the creation of more powerful and reliable electronic components, (ii) Research efforts targeting novel memory structures using high-*k* dielectrics aim to tackle scaling challenges inherent in semiconductor technology. Strategies such as integrating high-*k* dielectrics such as Inter-Poly Dielectrics (IPDs) into memory structures are being explored, with a focus on process optimization and barrier engineering. These endeavors seek to enhance memory performance, offering potential solutions for scaling beyond current limitations; (iii)

high-*k* dielectrics, when combined with other advanced materials, are positioned as potential substitutes for traditional floating gate structures in non-volatile flash memories. This exploration extends the potential lifespan of flash technology, allowing it to scale beyond the 20 nm threshold. This not only ensures the longevity of flash memory but also introduces new design possibilities for electronic devices; (iv) the integration of high-*k* dielectrics with emerging technologies, such as flexible and stretchable electronics, opens exciting possibilities for the future. This integration could lead to the development of innovative and adaptable electronic systems. Logic and memory devices featuring high-*k* dielectrics may find applications in flexible electronics, paving the way for more versatile and resilient electronic devices.

5.2.1 Future work for Linear High-*k* Material in Logic Devices

Ongoing research is expected to focus on fine-tuning the compositions of HfO_2 based linear high-*k* dielectrics, such as $Hf_{0.6}Zr_{0.2}(Ta, Dy)_{0.2}O_2$, to further improve dielectric constants and reduce leakage currents in future logic devices. This optimization holds the potential to yield materials with superior performance characteristics, especially in advanced logic devices. Future efforts are likely to concentrate on refining deposition techniques, particularly for ultra-thin films. Techniques like Atomic Layer Deposition may be considered to achieve greater precision and control over film thickness. This ensures the consistent and reliable performance of devices employing these high-*k* materials. Also, as semiconductor technology progresses to smaller nodes, the adoption of high-*k* materials in advanced CMOS logic devices and integrated circuits is anticipated. This integration could contribute to improved efficiency, reduced power consumption, and overall better device performance. Additionally, the successful application of HfO_2 and ZrO_2 co-substituted with Dy and Ta points toward

the development of logic devices. Ongoing exploration of these materials is likely to result in the creation of transistors with reduced power consumption and improved gate control, aligning with the growing demand for energy-efficient electronics.

5.2.2 Future Work for Non-linear High-*k* Dielectric in Memory Devices

Future research endeavors in non-linear high-dielectric materials, especially ferroelectrics, are expected to focus on refining the compositions of CMOS-compatible material for non-volatile memory applications. Optimizing these compositions holds the potential to lead to memory devices with significantly improved dielectric constants and polarization. The observed leakage current and unsaturated P-E curves among HZO ceramics need more studies. Future developments may explore novel designs that overcome these limitations to create advanced non-volatile ferroelectric memories with improved stability and reliability. The successful exploration of $Pt/Hf_{0.75}Zr_{0.25}O_2/Pt/Si$ structures for resistive switching memory devices indicates a viable pathway for integration into resistive RAM. Ongoing research is expected to focus on optimizing these structures for better performance in such memory applications, potentially leading to more robust and efficient memory devices. Given HZO's demonstrated resistive switching capabilities at the sub-nanometer scale with ferroelectricity, future outcomes may involve the integration of these non-linear high-k dielectrics into memory devices operating at smaller nodes by using ferroelectric tunnel junctions. This could contribute to the development of more compact and efficient non-volatile memory technologies, addressing the challenges associated with scaling memory devices to nanoscale dimensions.

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Appendix

Appendix-A Solid-State Reaction Techniques

Molar mass: Hf (178.49 gm)/ Zr 91.22 gm)/ O (15.999 gm)

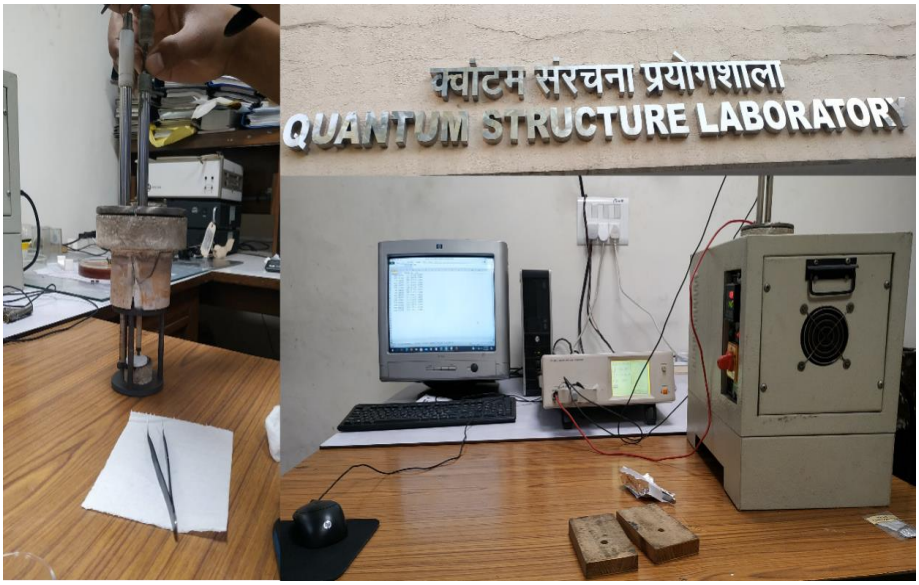
Composition:

$Hf_{0.25}Zr_{0.75}O_2$	$Hf_{0.5}Zr_{0.5}O_2$	$Hf_{0.75}Zr_{0.25}O_2$
$=0.25x(HfO_2) +0.75x(ZrO_2)$ $=0.25x (210.47) +0.75x (123.22)$ $=52.6175+92.4$ $=145.0175$ For 5gm: HfO_2: $\frac{52.6175 \times 5}{145.0175}$ $= 1.8141776\ gm$ ZrO2: $\frac{92.4 \times 5}{145.0175}$ $= 3.1858224\ gm$	$=0.5x(HfO_2)$ $+0.5x(ZrO_2)$ $=0.5 x (210.47) +0.75x (123.22)$ $=105.235+61.61$ $=166.845$ For 5gm: HfO_2: $\frac{105.235 \times 5}{166.845}$ $= 3.15367557\ gm$ ZrO2: $\frac{61.61 \times 5}{166.845}$ $= 1.84632443\ gm$	$=0.75x(HfO_2)$ $+0.25x(ZrO_2)$ $=0.75x (210.47) +0.275x (123.22)$ $=157.8525+30.805$ $=188.6575$ For 5gm: HfO_2: $\frac{157.8525 \times 5}{188.6575}$ $= 4.18357341\ gm$ ZrO2: $\frac{30.805 \times 5}{188.6575}$ $= 0.8164265\ gm$

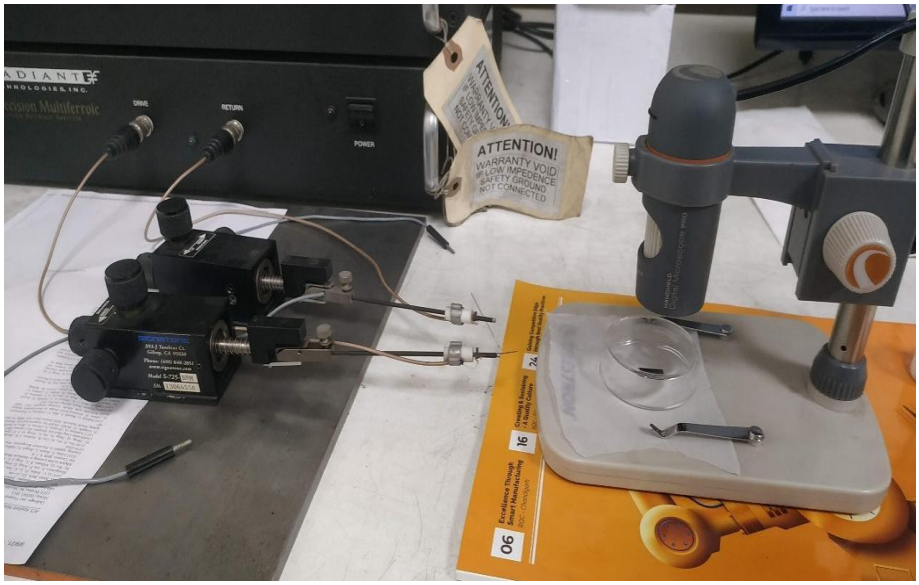
Appendix- B Muffle Furnace

Appendix-C The Hydraulic Press

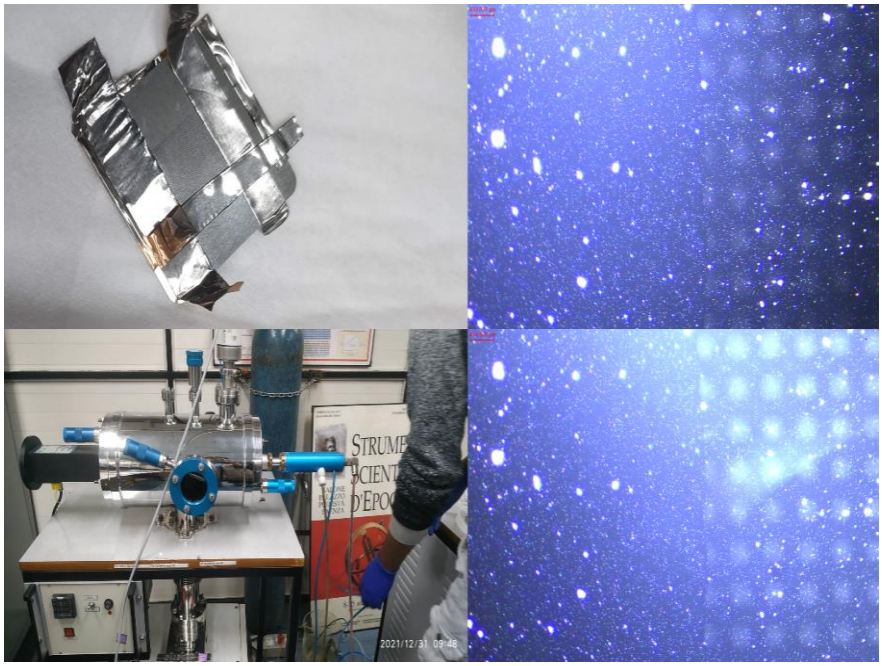
Appendix-D Dielectric System



Appendix-E Piezoelectric system



Appendix-F Electrode Deposition



List of publications

1. Sharma, U., Kumar, G., Mishra, S., & Thomas, R. (2022). Advancement of gate oxides from SiO2 to high-k dielectrics in microprocessors and memory. Journal of Physics: Conference Series, 2267(1), 012142. https://doi.org/10.1088/1742-6596/2267/1/012142
2. Sharma, U., Kumar, G., Mishra, S., Pradhan, D. K., & Thomas, R. (2020). Structural and electrical properties of Dy and Ta co-substituted (Hf, Zr) O2 ceramics as a novel high-k dielectric for logic and memory devices. IOP Conference Series: Materials Science and Engineering, 872(1), 012145. https://doi.org/10.1088/1757-899X/872/1/
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9. Sharma, U., Kumar, G., Mishra, S., Kumar, A., Pradhan, D. K., & Thomas, R. (2023). Structural and electrical properties of Dy3+ and Ta5+ co-substituted (Hf, Zr)O2 ceramics for logic devices. Journal of Electronic Materials, 52(2), 1083-1093. https://doi.org/10.1007/s11664-023-09789-y
10. Bhasker, V., Sharma, U., Kumar, G., & Thomas, R. (2022). Sol-gel Derived (Pb0.65Sr0.35)(Zr0.5, Ti0.5) O3 Ferroelectric Thin Films: Structural and Electrical Properties. Journal of Physics: Conference Series, 2267(1), 012146. https://doi.org/10.1088/1742-6596/2267/1/012146
11. Sharma, U., Mishra, S., Prasad, N., & Thomas, R. (2019). Lithium battery: A short review. Think India Journal, 22(16), 456-463.

List of Workshops

1. International Winter School-2020, "Frontiers in Materials Science"

Date: December 7-11, 2020

Venue: Jawaharlal Nehru Centre for Advanced Scientific Research, Bangalore (Virtual Event)

Focus: Introducing frontier areas of research in materials science for graduate students, young researchers, and scientists with backgrounds in physics, chemistry, and engineering.

2. Two Day Training cum Certificate Program on Thin-film Synthesis and Characterization Techniques

Date: February 2020

Venue: Sathyabama Institute of Science & Technology, Chennai

Focus: Training on thin-film synthesis and characterization techniques.

3. National Workshop on "X-Ray Diffraction: Theory and Practice"

Date: November 9-10, 2019

Venue: Lovely Professional University

Focus: Theory and practice of X-ray diffraction.

4. INUP - i2i Hands-on Training on Fabrication & Characterization of Field-Effect Transistor (FET)

Date: October 10-19, 2022

Venue: IIT Delhi

Focus: Fabrication and characterization of field-effect transistors.