DESIGN AND ANALYSIS OF RING STRUCTURED BASED VCO FOR HIGH FREQUENCY APPLICATIONS

Thesis Submitted for the Award of the Degree of

DOCTOR OF PHILOSOPHY

in

Electronics and Communication Engineering

By

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2025

DECLARATION

I, hereby declared that the presented work in the thesis entitled "**Design And Analysis Of Ring Structure Voltage Controlled Oscillator For High Frequency Applications**" in fulfilment of degree of **Doctor of Philosophy (Ph.D.)** is outcome of research work carried out by me under the supervision of **Dr Sobhit Saxena**, working as Professor, in the **School of Electronics and Electrical Engineering** of Lovely Professional University, Punjab, India. In keeping with general practice of reporting scientific observations, due acknowledgements have been made whenever work described here has been based on findings of other investigator. This work has not been submitted part or full to any other University or Institute for the award of any degree.

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CERTIFICATE

This is to certify that the work reported in the Ph.D. thesis entitled **Design And Analysis Of Ring Structure Voltage Controlled Oscillator For High Frequency Applications**" submitted in fulfillment of the requirement for the award of degree of **Doctor of Philosophy (Ph.D.)** in the **Electronics & Communication Engineering**, is a research work carried out by **Priyanka Kumari B S**, **41800147**, is bonafide record of his/her original work carried out under my supervision and that no part of thesis has been submitted for any other degree, diploma or equivalent course.

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ABSTRACT

VCO is the basic building block in many communications and signal processing equipment and plays a crucial role in generating essential high-frequency clock signals that drive data transmission and reception, and that can be adjusted by a control voltage. Generally, LC oscillators provide superior phase noise and greater oscillation frequencies, but this comes at the expense of a limited frequency tuning range and a complicated manufacturing procedure for inductors and capacitors on the silicon surface.

Device scaling uncovered many short channel effects (SCEs), and the bulk CMOS technology behavior upsets with these SCEs. To overcome these exposed effects, single gate devices should be substituted with multiple gate devices to enrich the gate control over the conducting channel. Fin gate FET technology is a promising device to provide efficient gate control over the conducting channel. There are few multi gate Fin-FET devices are Double gate Fin-FET (DG-Fin-FET), Triple gate Fin-FET (TG-Fin-FET) and gate around Fin devices. Ring-based voltage-controlled oscillator (VCO)'s frequency of oscillations should be less sensitive to the supply voltagevariations. A sudden drop in supply voltage significantly affects the performance of the VCO. Supply voltage insensitive circuit or low voltage operated designs are the backbone of the constantVCO performance. CMOS based supply compensation techniques reduce the oscillation frequency with the supply voltage decrease. Hence fully customized Fin-FET based circuits designs are unveiled as the solutions to reduce the significant amount of power wastage and delay of the stages as the switching characteristics of the Fin-FET is better than the bulk CMOS transistor, which eliminates the losses and negates supply noise.

In this thesis, we proposed a new low power technique to lower the power of VCO and enhance battery life. The CMOS ring oscillator designs are made on different nano scale technologies and verified the major design parameters such as frequency of oscillations, power, and area of the designs as one part of the thesis. The other part of thesis is related to the designs of ring oscillators to improve the oscillation frequency and power. An 18 nm technology Fin-FET has been modeledin order to achieve desired characteristics. This FinFET greatly reduced the SCEs compared to thebulk MOSFET hence used in the designs of three stage, five stage and twenty-one stage ring oscillators. Supply voltage considered as 1V. The oscillator has exceptional performance across several domains, such as the microwave frequency range inside the L-band,

sensitivity to supply variations, occupied area, power consumption, and phase noise. The frequency of oscillations increased along with reduced stage number; we got 17.7GHz frequency from the three-stage ring circuit. Verilog A and Cadence Virtuoso helped with our designs.

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CHAPTER 1
INTRODUCTION

The introduction of Voltage-controlled oscillator (VCO), types of VCOs, the characteristics of VCOs required to be used in different kinds of applications, the benefits and setbacks are discussed here. On the other side the motivation of the thesis, research gaps and the well-defined objectives explained in this chapter. Finally, the thesis organization of therest of the chapters explained here.

1.1 INTRODUCTION

VCO is the fundamental building block in many electronic circuits, especially for communication and signal processing applications. It plays a crucial role in modern communication systems such as both in wired and wireless. They act as the heart of the system, generating the essential high-frequency clock signals that drive data transmission and reception, and that can be adjusted by a control voltage. Depending on the components and the intended usage, the terms "ring oscillator," "relaxation oscillator," and "LC oscillator" refer to the various electrical and electronic components that can create VCO circuits. LC oscillators often exhibit superior phase noise and higher oscillation frequencies, but this comes at the expense of a limited frequency tuning range and a more complex manufacturing procedure for the inductors and capacitors on the silicon substrate. Ring oscillators provide advantages over LC oscillators in terms of simplicity of manufacture onsilicon and an extensive frequency tuning range [1]. VCO contributes the following to the communication systems.

i) **Highly stable clock generation**: VCO can generate precise and stable clock signals within specific frequency ranges. This stability is crucial for ensuring accurate data timingand synchronization throughout the communication process.

ii) **Frequency agility**: VCO can adjust its output frequency based on a control voltage. This enables communication systems to switch between different channels, bands, or protocols seamlessly.

iii) **Phase modulation and frequency modulation**: By modulating the control voltage of a VCO, information can be encoded onto the carrier signal using either phase modulation(PM) or frequency modulation (FM). This is how Analog and digital data are carried over the communication channel.

1.2 VCO APPLICATIONS:

VCO is an essential component in communication systems due to their ability to generate stable, tunable, and modulatable high-frequency signals. Their accuracy makes them vital for efficient and reliable data transmission and reception. VCO is the important block in various applications such as frequency synthesizer circuits, phase- locked loop (PLLs) circuits, and wireless communication systems. Radio and television transmitters for generating the carrier frequencies for broadcasting. Radar systems for generating high-frequency pulses are used for target detection. Global position systems (GPS) receivers for generating the reference signal for time synchronization [4-6]. The application of VCO in PLL is shown in figure 1.1. Input signals of the PLL circuit are two frequencies, one is direct signal, and the other is fed from the output itself (feedback).

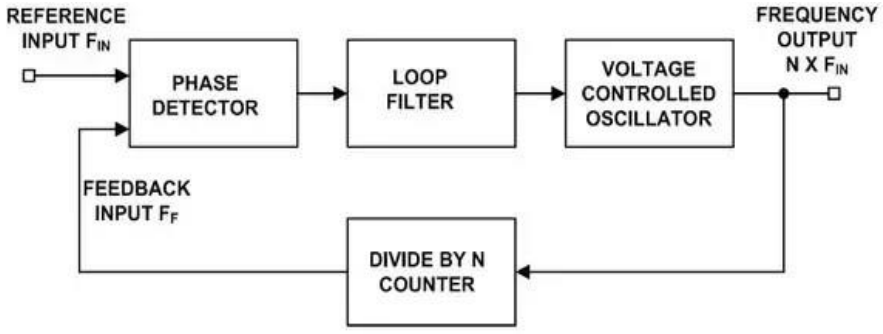


Figure 1.1: Block Diagram of PLL [6].

The Phase frequency detection network is a comparator circuit that compares and detects a phase difference between the two signals. The low pass filter bypasses only the lowest frequency component (difference of frequency) and is fed to a bias generator (not mentioned in figure) which generates a DC value corresponding to the difference signal. The DC value is fed as the input of VCO. It generates a frequency signal in accordance with the DC bias. The generated frequency is compared (divide by N is optional) again. Process stops when both the frequencies are equal [31].

1.3 VCO CHARACTERISTICS:

VCO performance is defined by several key metrics [31-32]. Such as:

i) **Frequency Range**: This specifies the range of frequencies the VCO can generate by adjusting the control voltage. A wider range provides more flexibility for various applications. Ring oscillators typically offer a wide tuning range compared to other VCO topologies.

ii) **Power Supply**: This denotes the voltage required to operate the VCO. Lower power consumption is usually preferred, especially for portable devices. Ring oscillator circuits arewell known for their low power consumption compared to some other VCO designs.

iii) **Area Occupied**: Compact designs are desirable for minimizing overall system size and cost. Ring oscillators have a relatively small footprint due to their simple cascade.

iv) **Power Consumption**: This measures the amount of power consumed by the VCO during operation. Lower power consumption improves battery life and reduces heat generation. As mentioned earlier, ring oscillators are generally energy-efficient compared to the other VCOs.

v) **Delay**: This is defined as the time required for the VCO circuit to stabilize at another frequency after the control voltage is changed. Shorter delays are preferred for fast tuning and responsiveness. Ring oscillators tend to have fast tuning times due to their simple structure.

vi) **Phase Noise**: This is a critical metric that describes the unwanted fluctuations in the VCO's output phase. Lower phase noise ensures a cleaner signal and better data transmissionquality. Ring oscillators exhibit relatively higher phase noise compared to some other VCOdesigns, which can be a limitation for demanding applications [39].

After studying the above characteristics of the VCO, there are many VCO topologies but out of all the topologies, ring oscillator topology is very popular as it covers all the characteristics that a VCO requires.

While ring oscillators offer many advantages like simplicity, small size, and low power consumption, their limitations in phase noise and tuning accuracy need to be considered for demanding communication systems.

1.4 OSCILLATOR:

Oscillator is an electronic circuit that generates a periodic signal without an external input. Unlike amplifiers that utilize negative feedback, oscillators employ positive feedback to sustain oscillations. The oscillator block diagram is shown in figure 1.2. Where, in the forward path there is an amplifier with amplification factor A, and the feedback path frequency dependent on attenuation factor is β(jω).

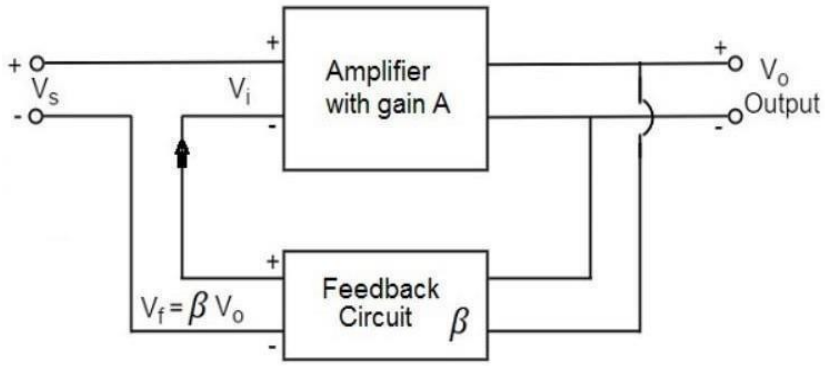


Figure 1.2: Simple Oscillator circuit.

Assume the positive feedback, then to produce sustained oscillations, the oscillator circuit must fulfill the Barkhausen criteria [72-73].

To maintain stable oscillations, an oscillator must fulfill the following conditions:

- **Loop Gain:** The product of the amplifier's gain and the feedback factor must be equal to or greater than 1.

  i.e the total loop gain, $T(j\omega) = |A\beta(j\omega)| \approx 1$ ---- (1.1)

- **Phase Shift:** The total phase shift around the feedback loop must be an integer

multiple of 360^0.

i.e the phase angle, $\angle T(j\omega 0) = 0^0$ or 2π----- (1.2)

By adhering to these criteria, the circuit can avoid damp or divergent oscillations, ensuringa stable output signal. Once power is switched on, oscillations may begin to decline or even rise if the amplitude criterion is satisfied ($|T(j\omega o)|=1$ or even >1), but the phase condition is not fulfilled. When the phase criterion is met, the circuit becomes susceptible to oscillations. Even with minimal initial disturbances, the system will tend to produce sustained output oscillations. This is the only way to enable a system's self-excitation via positive feedback. Furthermore, the frequency often deviates from the precise frequency where the design meets the amplitude criterion. Therefore, the system will attempt to oscillate at a different frequency, denoted as 'ω_c'. Until a limiting mechanism activates, oscillation amplitudes will increase at the new frequency 'ω_c', provided the amplitude criterion remains met. However, if the amplitude of the loop gain is < 1, at the frequency w1, will witness damped oscillations or no oscillations at all [76-77].

Oscillator performance is evaluated based on multiple parameters including operating frequency, tuning range, power consumption, output power, and phase noise. To provide a standardized comparison, a figure of merit (FOM) is introduced, as defined by equation (1.3).

$$FOM = 10\log\left(\frac{f_0}{\Delta f}\right)^2\left[\frac{1}{V_{DD}*I*PN}\right] \text{----------} (1.3)$$

Where ,

'V_{DD}' is the supply voltage

'I' is the current

'PN' is the phase noise

'f_0' is the oscillating frequency

'Δf' is the frequency drift or offset

Clock generation typically employs two types of oscillators: LC oscillators and ring oscillators. LC oscillators leverage the resonance of inductor-capacitor (LC) tanks to produce clock signals, offering excellent noise performance. In contrast, ring oscillators

comprising a series of delay stages, such as CMOS inverters, connected in a loop are more compact in area. They are also capable of generating multi-phase outputs, making them particularly suitable for system-on-chip (SoC) applications where space is limited, and multi-phased clocks are essential for I/O interfaces. Ring oscillators typically exhibit lower FOM values compared to LC oscillators due to higher power consumption and degraded phase noise at equivalent frequencies. To address these limitations, current-starved ring oscillators have emerged, offering improvedtuning range, reduced area, and lower phase noise [2].

1.5 RING OSCILLATOR

Ring oscillator is the common configuration for VCOs using cascaded odd-number inverter stages are presentedas in figure 1.3. Each stage in the ring oscillator is known as the delay stage which produces the delay of 'τ_d' and the inverter is designed with either NMOS or PMOS or CMOS or BiCMOS or e.t.c. First delay stage output is connected to the second stage as the input, second delay stage output is conned to the third delay stage as the input and the third delay stage output is connected back to the first stage as the input [7].

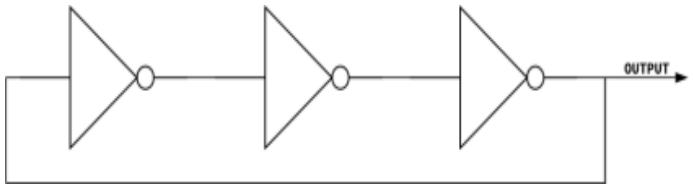


Figure 1.3: Simple three inverter ring oscillator

The frequency (f) of this ring oscillator canbe measured with equation 1.4.

$$f = \frac{1}{2N\tau_d} \quad ----(1.4)$$

Where 'τ_d' is the delay of each inverter stage, N is the number of delay stages.

The transfer function of the single stage is given by

$$H = \frac{A_0}{1+\frac{s}{\omega_0}} \quad (1.5)$$

For 'N' stages, the overall transfer function is

$$H_T = \left[\frac{A_0}{1+\frac{s}{\omega_0}}\right]^N \text{ – – – – – (1.6)}$$

The angle is $\theta_{tot} = N\,Tan^{-1}(\frac{\omega}{\omega_0})$ -----(1.7)

From the angle criteria, $\omega_{osc} = \omega_0\,Tan(\frac{180^0}{N})$ ----(1.8)

Here, 'ω_0' indicates the angular frequency of the oscillator when the loop is completely closed and the equations (1.1) and (1.2) are satisfied. While the odd number of stage configurations always satisfies the oscillation condition, for an even number of stages, the loop establishes positive feedback rather than a negative one, which may result in latch-up.

Ring oscillators hold a special place due to several reasons [12-13]:

i) **Simplicity and Cost-Effectiveness**: Unlike other VCO designs that rely on complex tuning mechanisms like LC tanks or crystal resonators, ring oscillators leverage a chain of interconnected inverters. This simple architecture translates to easier design, fabrication, andlower cost compared to other VCOs.

ii) **Wide Tuning Range**: By adjusting the supply voltage or biasing currents in the inverters, ring oscillators can achieve a substantial range of output frequencies.

iii) **Low Power Consumption**: Due to their minimal circuitry, ring oscillators inherently consume less power compared to other VCOs.

iv) **Easy Integration and Scalability**: Ring oscillators rely on standard CMOS technology, making them readily compatible with other integrated circuits and easily scalable for miniaturization in modern electronics.

v) **Robustness and Stability**: Their simple design makes ring oscillators inherently robust against environmental fluctuations and temperature changes.

vi) **Phase Noise:** While inherently higher than some VCOs, phase noise of ring oscillators can be improved through various techniques.

Limitations of ROs compared to VCOs:

This arrangement leverages the delay in each inverter stage to create a self-oscillating loop. The frequency depends on the number of inverters, their individual delays, and the supply voltage. While simple and efficient, ring oscillators have their limitations, especially in terms of phase noise and tuning linearity. It is assumed that each stage delay time is constant for every inverter stage which makes thecircuit restricted to only to the lower frequency tuning range and linearity. And, if the number of stages is increased then circuit will have an increased chip area and power consumption [10].

However, designing high-performance ring oscillators poses several challenges. Their oscillation frequency is influenced by a complex set of variables, including process variations, the number of stages, transistor sizing, and supply/control voltage—often in non-linear ways. This complexity makes it difficult to derive a clear analytical or empirical model linking these parameters. Furthermore, ring oscillator design requires extensive transient simulations to obtain critical time-domain performance metrics, such as operating frequency and RMS jitter, unlike small-signal analog circuits like amplifiers, which are easier to analyze. However, their limitations in phase noise, tuning accuracy, and output power need to be considered for specific application requirements. Ring oscillators come with some limitations compared to other VCOs [16-18]:

i) **Higher Phase Noise**: They generally exhibit higher phase noise, which can introduce unwanted jitters and affect signal integrity.

ii) **Limited Tuning Accuracy**: While offering a wide range, the tuning accuracy of ring oscillators is lower than other configurations, especially at higher frequencies.

iii) **Lower Output Power**: Their simple design limits their output power compared to other VCOs, potentially requiring additional amplification stages in certain applications.

1.6. IMPORTANCE OF MINIATURIZATION

Miniaturization is a rapidly advancing technological approach aimed at creating extremely small electronic, mechanical, and optical devices. This includes components such as computers, semiconductor chips, sensors, biosensors, integrated circuits (ICs), and microprocessors used in vehicles and other modern systems. Today, the prevalence of compact, portable gadgets easily carried in a pocket is a direct result of miniaturization, which enables the downsizing of components while delivering numerous advantages and broad applications. Beyond electronic devices, miniaturization plays a crucial role in the advancement of nanotechnology, allowing for the fabrication of a wide array of structures with unique features and enhanced properties. The benefits of miniaturization are evident in hybrid microcircuits, offering reduced size and weight. With continuous progress in integrating and shrinking portable devices, the concept of wearable computing is becoming a practical reality [11]. The trend of miniaturization is shown in figure 1.4

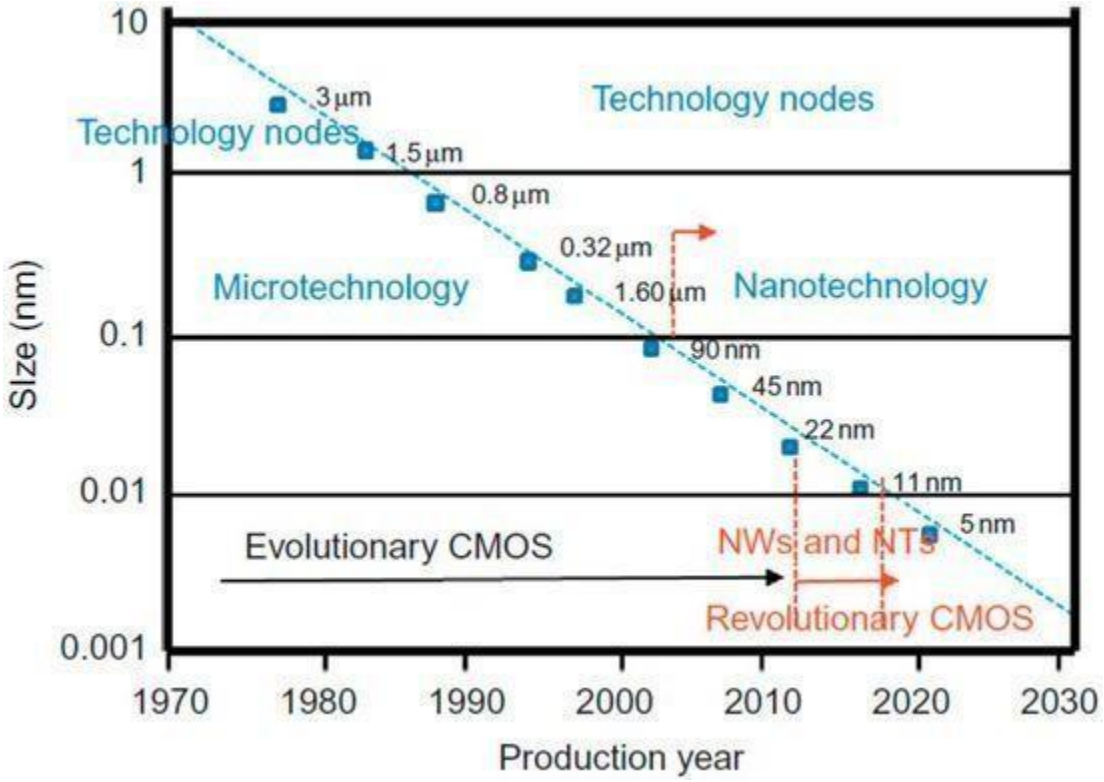


Figure 1.4: Miniaturization trend [36]

Miniaturization offers numerous advantages, including reduced device size, lower manufacturing costs, increased speed, lower power consumption, improved efficiency, and enhanced portability.

There are a few disadvantages also in Miniaturization, like thermal increase or overheating issue. Decreasing feature size and increasing package densities are making thermal issues extremely important in integrated circuit designing. Extra cooling system is needed for thermal management

1.7. LOW-POWER TECHNIQUES

As mentioned, ring oscillators are popular choices because of their ease of implementation and small power consumption. Still, additional optimizations can be applied. To achieve optimal efficiency in portable systems, employing dedicated low-power techniques alongside device scaling is crucial.

These can include **Circuit-level techniques**: Optimize transistor sizing, reduce switching activity, use low-power logic styles, and utilize power gating to shut down unused circuit blocks. **Architecture-level techniques**: Employ pipelining, low-power clocking schemes, and sleep/idle modes to minimize active power consumption. **System-level techniques**: Optimizesoftware algorithms, utilize dynamic voltage scaling, and implement energy harvesting fromambient sources [14-15].

Few low power technologies in ring oscillator design are

i) **Current-starved technique**: Reduce supply voltage and utilize current steering techniques to minimize power consumption [13].

ii) **Multi-phase technique**: Generate multiple clock signals from a single oscillator, reducing overall circuit complexity and power [77].

iii) **Dynamically adjustable frequency**: Adapt the operating frequency based on workload demands, reducing unnecessary power consumption when not at peak performance [27].

Overall, the combination of device scaling and low-power techniques proves a potent strategy for maximizing battery life and minimizing system size in portable circuits.By understanding the limitations of scaling alone and actively implementing innovative low-power design principles, we can create efficient and long-lasting electronic devices for the future.

1.8 IMPORTANCE OF ENERGY EFFICIENT DESIGNS

Ultra-low power is one of the main inherent aims of energy efficient designs. Ultra- low power ring oscillator addresses this demand by minimizing power consumption while maintaining reliable performance. Designing ultra-low power circuits in nanoscale technologies poses several challenges. These challenges include overcoming process variations, minimizing power consumption, ensuring stable and accurate frequency generation, and addressing the impact of technology scaling on device characteristics. Nanoscale technologies have revolutionized the field of integrated circuits, enabling the developmentof highly efficient and compact electronic devices.

Moore's law states that when devices get smaller, planar transistors have negative consequences such as gate oxide tunnelling, increased leakage currents, and the amplification of SCEs. As semiconductor technologies advance, the transistor sizes decrease, leading to increased integration density and reduced power supply voltages. This necessitates the development of novel circuit topologies and design techniques to achieve ultra-low power operation [34].

Research in VLSI unveiled many new device structures such as Double gate FET(DG-FET), Fin-FET and Tunnel FETs (TFET) [4]. A buried oxide layer acts as an insulator on the silicon substrate, making the SOI- MOSFET different from the MOSFET. This configuration leads to a decrease in junction virtual capacitance, the prevention of undesirable latch-up generation, and a reduction in leakage power [5]. The two different categories of the Silicon on Insulator MOSFETs are namely fully depleted SOI-MOSFET and the partially depleted SOI-MOSFET.

The SOI-MOSFET has several drawbacks, including self-heating and challenges associated with producing thin silicon bodies. DGMOSFET is an extreme subject for VLSI research because it can be scaled to the shortest channel length for a given gate oxide thickness. FinFET device is a type of transistor design used in the construction of electronic circuits, particularly in the integrated circuits (ICs). It is an evolution of traditional MOSFET technology and is employed to overcome certain limitations associated with scaling down transistor size. The outstanding electrostatic integrity, minimal leakage current, improved short-channel effect, outstanding efficiency from the un-doped channel structure, elevated carrier mobility, and reduced random dopant fluctuation of FinFET make it an excellent option for future transistor technologies [19-23].

1.9 Fin-FET TECHNOLOGY:

The key feature of Fin-FETs is the fin-like structure that protrudes from the surface of the silicon substrate, serving as the channel through which current flows. This design provides better control over the flow of current compared to traditional planarMOSFETs, allowing for improved performance and energy efficiency. The fin structure effectively increases the surface area for controlling the flow of current. The transition to Fin-FET technology became essential as semiconductor manufacturers faced challenges in shrinking transistor sizes using traditional planar designs. As transistors become smaller, quantum mechanical effects and leakage currents can adversely impact performance and power efficiency. Fin-FETs help address these issues, enabling the continued miniaturization of semiconductor devices. Fin-FET technology has been widely adopted in the semiconductor industry, and it has played a crucial role in the development of advanced processors, memory devices, and other integrated circuits. Technology has contributed to the enhancement of performance, energy efficiency, and overall functionality of electronic devices. The evolution of Fin-FET technology has followed a path of continuous refinement and optimization, with each subsequent generation introducing improvements in terms of performance, power efficiency, and manufacturability as in figure 1.5. Intel introduced the first generation of Fin-FET technology with its 22 nm process technology. Later, the 14 nm process node was introduced, incorporating further refinement [40-43].

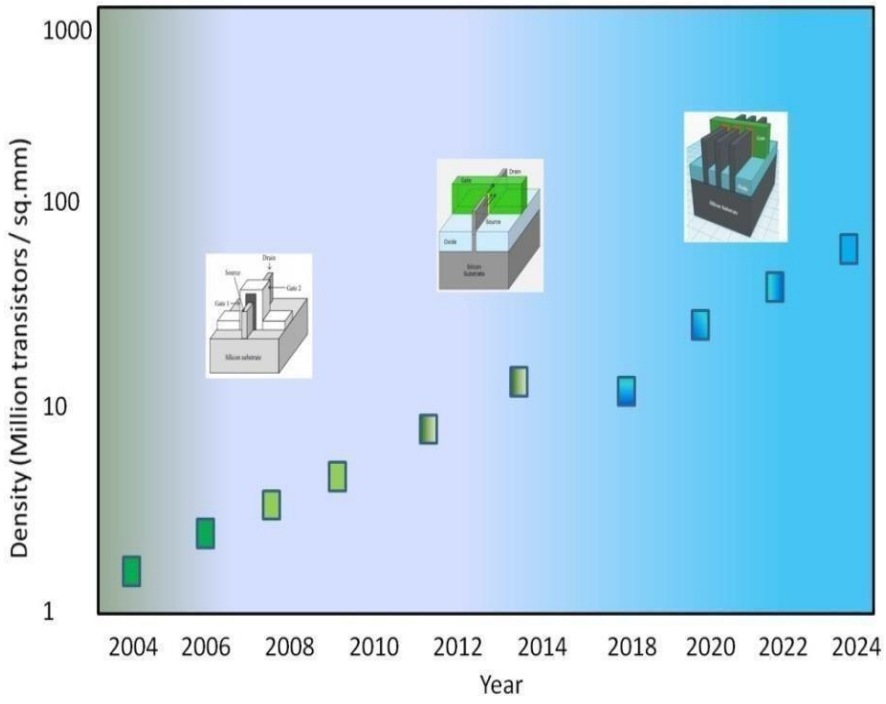


Figure 1.5: Chip density across technological nodes [2].

Semiconductor manufacturers, including Intel and other leading foundries like TSMC and Samsung, moved to the second generation of FinFET technology at 10nm and 7nm process nodes. These nodes featured improvements in transistor density, performance, and energy efficiency compared to the first generation. The industry transitioned to even smaller process nodes, reaching 5nm and 7nm using EUV (Extreme Ultraviolet Lithography) technology.

Advances in materials, transistor design, and manufacturing techniques are being employed to overcome the technical challenges associated with scaling down to these dimensions.

1.9.1 Fin-FET:

Fin-FET is a type of three-dimensional transistor structure, which has emerged as a leading design for integrated circuits (ICs). They offer significantperformance and power efficiency advantages over traditional planar devices. The Key Features and Benefits of Fin device are i) 3D structure, ii) improved electrostatic control, iii) low power consumption, iv) scalability and v) versatility.

In 3D Structure, a vertical fin, surrounded by gate electrodes on three sides, provides superior control over the electric current flow compared to planar transistors. The gate electrodes can be made from polysilicon or metal alloys, offering flexibility in design. Fin-FETs provide better electrostatic control over the channel, reducing short-channel effects (SCEs) and enhancing carrier mobility. This leads to faster switching speeds and higher operating frequencies, making them ideal for applications like processors and GPUs. The lower operating voltage of Fin-FETs results in reduced leakage currents, contributing to lower power consumption compared to planar devices. This is particularly beneficial for battery-powered devices. Fin-FETs are highly scalable, allowing for continued miniaturization and increased chip density. This enables the development of smaller and more powerful electronic devices. FinFET technology encompasses various configurations, including multi-gate MOSFETs (Mu-GFETs) and Gate-All-Around FETs, to address different design requirements [50].

Fin-FET is a type of transistor that offers significant advantages over traditional MOSFET. Fin-FET is a non-planner 3D structure device with the gate surrounding the channel on three sides, providing enhanced performance and power efficiency. The basic Fin-FET structure is shown in figure 1.6 [55-57]. Here, Fin dimensions play a key role in the device performance. The important geometrical parameters are drawn gate length (L_{gate}) between the source and drain nodes, and the fin dimensions such as fin height (H_{fin}) and fin thickness (t_{fin}) or width (W_{fin}).

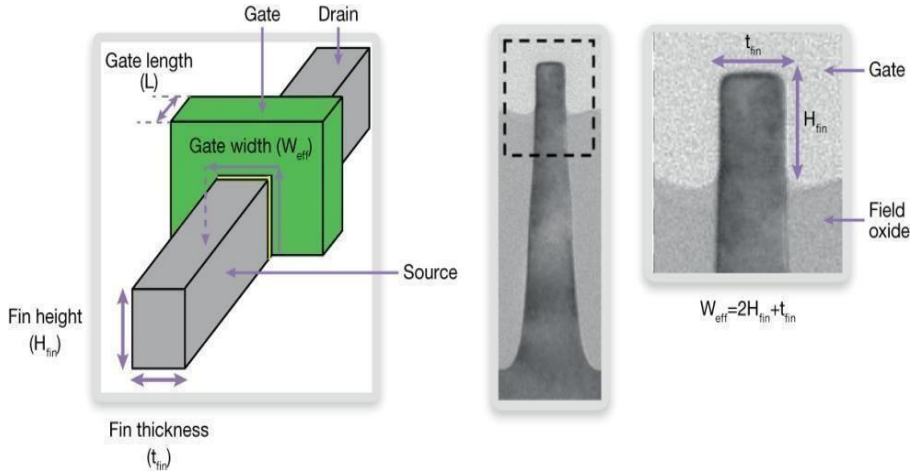


Figure 1.6: Basic Fin-FET structure.

The key advantages of Fin-FET include **Higher On-State Current**: Fin-FET exhibit higher on-state current compared to bulk MOSFETs and DG-MOSFETs. **Lower Off-State Current**: Fin-FET have a lower off-state current, which is crucial for reducing leakage power. **Faster Switching Speed**: The improved channel control in Fin-FET enables faster switching times, making them suitable for high-performance applications.

The effective channel length (L_{eff}) and width (W_{effe}) is calculated as in equations (1.9) and (1.10).

$$L_{eff} = (L_{gate} + 2*L_{ext}) \quad (1.9)$$

$$W_{effe} = (t_{fin} + 2*H_{fin}) \quad (1.10)$$

The number of fins in Fin FET can be increased to more to achieve more control over the channel. For 'n' number of parallel fins in FinFET, the total width of the channel equation is modified as in equation (1.11).

$$W_{tot}=n(t_{fin}+(2*H_{fin})) \text{ ---------- } (1.11)$$

Then the drain current equation of FinFET is given by equation (1.12)

$$(I_D) = \frac{1}{2}\mu_n \frac{\varepsilon_{ins}}{EOT}\frac{[t_{fin}+2*H_{fin}]}{[L_{gate}+2*L_{ext}]}(V_{Gs}-V_{th})^2 \text{ ---(1.12)}$$

1.10 MOTIVATION OF THESIS

Most modern electronic systems, especially in the field of telecommunications, both wired and wireless require high-precision Voltage-Controlled Oscillators to function across a wide range of frequencies. These VCOs are essential components for tasks such as frequency synthesis, signal modulation, and clock generation. Among various VCO architectures, ring oscillators are considered a strong candidate due to their compact size, ease of integration, wide tuning range, and simple design, which make them ideal for System-on-Chip (SoC) applications. They can be easily implemented using standard CMOS or Fin-FET technologies, making them highly compatible with current fabrication processes. There are some design challenges with the ring oscillator such as miniaturization, short channel effects, gain and phase noise issues. In this thesis it is required to address these critical challenges and make them thrive the thirst of battery-operated communication technologies.

1.11 RESEARCH GAPS

After the deep review of the deep literature on ring oscillators, I strongly conclude that there are a few issues in the existing designs. Balancing ultra-low power consumption with high frequency and low phase noise is still an ongoing challenge. Ring Oscillators are highly sensitive to temperature and process variations, affecting frequency stability and reliability. Techniques to reduce phase noise without increasing power or die area are limited.

1.12 OBJECTIVES OF THE THESIS

Based on the research gaps mentioned above after literature study, the following objectives are defined to meet the problem statement.

Objective-1: To study literature and investigation of various low power schemes and propose and design a Five stage ring structured based voltage-controlled oscillator using 45 nm technology.

Objective-2: Achieve high frequency oscillations in the band ranging above higher frequency according to TRAI millimeter band using dual loop topology.

Objective-3: Optimization of power dissipation while maintaining high frequency

oscillations implement 3, 5 and 21 stage ring oscillator circuits with Fin-FET technology.

Objective-4: Simulate the designs and observe the power, delay, frequency and phase noise with tuning linearity

1.13 METHODOLOGY

The Proposed methodology for achievement of the objectives is here.

a) Study of various low power schemes to apply inverter circuit design.
b) Implementation of CMOS Inverter on different nanoscale technologies along withlow power schemes. Performing simulations to measure power, delay, and frequencies.
c) Consider the design whose parameters are very optimized parameters to design ring oscillator circuit.
d) Design the Fin-FET, design Fin-FET base5 and 21stage ring oscillators.
e) Simulate the circuit using Cadence Virtuoso tool and compare the results with open literature.

1.14 THESIS ORGANIZATION

Chapter 1: Fundamental concepts of ring oscillators, their significances and potential advantages for portable, high-frequency applications are discussed. Subsequently, the importance of miniaturization, the trend of device scaling, ring oscillator characteristics, discussed along with Fin-FET technology.

Chapter 2: The deep literature study on VCO topologies, ring oscillator circuit designs, simulations and the results matching with the technological requirements. The aim is to identify established design principles, innovative optimization techniques,and emerging trends that inform the development of efficient and miniaturized communication circuits.

Chapter 3: In this chapter, various low-power schemes discussed by implementing those techniques to implementation of basic inverter circuit, evaluating the effectiveness of various parameters on different nanoscale technologies.

Chapter 4: Fin-FET device geometry, characteristics, advantages and challenges are discussed. The impact of parameters like power consumption, frequency range, and area efficiency are discussed.

Chapter 5: In this chapter, three, five and twenty-one stage Fin-FET based ring oscillator designs, simulations and results achieved are presented.

Chapter 6: Conclusion remarks along with the future scope direction of this research work topic ring oscillator design with the optimized parameters discussed.

CHAPTER 2
LITERATURE SURVEY

This chapter delves into the various types of oscillator circuits and the design approaches, merits and setbacks of the designs process. It focuses on the slope of improvement of figures of merits of various ring oscillator designs.

(**Neha thakur, 2014**) [3] explained a low power design, which observed that it depends on the device supply voltage and the threshold voltages. This is commonly beneficial because threshold voltage and supply voltages can be controlled easily. The circuit is further designed effectively to make it operate at higher speed with lower power requirement in the circuit. Thus, by doing so effective care must be taken for designing the circuit elsetrade off will affect the design.

(G. Jovanovic, 2009) [4] explained an N- stage VCO circuit implementation to achieve lownoise. In communication, it is applied for better frequency and high phase noise. It is not required for LC tank oscillator but is useful for the purpose of multistranded wireless transceiver. Power consumption has been reduced with better controlling of output frequency along with the advantage of full swing output signal acquired by controlling reverse body bias. Sushil Kumar et al, suggests differential LC and Voltage Controlled Oscillator generation of the ISM (Industrial, Scientific, and Medical) band, power consumption and layout design.

(Madhusudan Maiti, 2020,) [5] proposed a current-starved technique in the ring oscillator- based VCO circuit. This was designed on the 90 nm CMOS process and is operated with a 1.2Vsupply. This design results 44.59 µW of power consumption while generating a frequency of 1.78 GHz using a 7-stage configuration. This approach effectively balances power consumption and operating frequency.

(**Bodhisatwa Sadhu, 2013**) [6] presented a VCO design to achieve low-phase-noise. This was implemented in 32 nm SOI CMOS process and operated with 1.5V supply voltage in generating 22 GHz frequency. This design power consumption was 36 mW and

exhibiting a phase noise of -127.3 dBc/Hz. The design incorporated a transconductance linearization technique to improve phase noise performance.

(**Viashali, 2014**) [7] designed a single-ended seven stage ring oscillator circuit. This design was implemented in 130 nm CMOS process and operates at 1V supply. This seven-stage oscillator achieved the frequency of 917 MHz while consuming 16.55 µW of power. Thisdesign demonstrated a significant reduction in power consumption compared to previous approaches.

(**T. Sato, 2011**) [8] introduced a novel figure of merit (FOML) to evaluate the frequency tuning range of LC oscillators. This metric addresses the limitations of conventional methods that often degrade phase noise when attempting to widen the adjusting range. FOML is derived from the ruin of the inductor's quality factor caused by tuning mechanisms.

$$FOM_L = FOM(f_{cent}) - 20\log\left(1 + \frac{FTR}{2}\right) \text{ ---- (2.1)}$$

where $FTR = \frac{f_{max} \pm f_{min}}{f_{cent}}$

and $f_{cent} = \frac{f_{max} \pm f_{min}}{2}$

(Razavi, 2019) [9] discussed the ring oscillator circuit importance in different applications, different types of ring oscillators and their design approaches along with the performancecomparisons. Finaly explained how the ring oscillator is used in the VCO.

(**Bhavana Goyal, 2016**) [10] Proposed a differential configuration type ring oscillator to design VCO for the implementation of PLL circuit. Charge pump based PLL is designed. A five stage differential pair of ring oscillators is designed in 180 nm CMOS process. The circuit was operating with 3V power supply, then 6.5 GHz frequency achieved this circuitand consumed 36 mW of power.

(**Sreenivasa Rao Ijjada, 2011**) [11] discussed various low power techniques in VLSI circuits implementation. Proposed stacking of transistors techniques in the implementation of inverter, SRAM and few of other circuits and observed that a significant amount of power reduces with the stack techniques comparing with the conventional design approaches.

(**Ebrahimi, 2023**) [12] designed the ring oscillator which was operated in the subthreshold region to attain low power consumption. Unlike traditional ring oscillators whose frequency is strongly linked to temperature variations, this design incorporates two current sources such as a temperature-independent current source and a CTAT (Complementary to Absolute Temperature) current source. The CTAT current compensates for frequency drifts caused by temperature changes. This was designed in 180 nm RF-CMOS process, the prototype demonstrated a significant reduction in thermalcoefficient (TC) from 240 ppm/°C to 80.4 ppm/°C while maintaining a power consumption of 44.5 µW at the frequency of 1 MHz and a supply voltage of 1.8V.

(**Mahato, 2014**) [13] implemented a low-frequency ring oscillator circuit with CMOS thyristor concept. This design was Implemented in a 250 nm CMOS process and operated with a voltage of 2.5V. the design generated a sinusoidal output waveform operating at 8.94 Hz while consuming 5.7 µW of static power.

(J. C. Park and V. J. Mooney III, 2006) [14] introduced a "sleepy stack" approach in the design of ring oscillator circuit in reaching the low power. This logic circuit maintains its logic state in sleep mode, resulting in low power consumption due to minimal leakage. However, it is the most effective method for reducing leakage power consumption compared to other known strategies. This provides circuit designers with different options for addressing theissue of power leakage.

(**Sharma, 2021**) [15] highlighted the trade-off between device miniaturization for faster response times and the adverse impact on battery life. Scaling down MOSFET dimensions and operating voltages (V_{DD} and Vth) is crucial for achieving low power consumption. However, aggressive threshold voltage scaling introduces leakage currents. The study explored various leakage control techniques and applied them to NAND gate designs implemented in a 16 nm technology node for comparative analysis.

(**Ramesh, 2018**) [16] derived a formula for the computation of frequency of oscillations of the ring oscillator very quickly. This has three terms such as number of stages, device channel length and empirical constant. A three stage and 23 stage ring oscillators were designed in 180 nm CMOS technology and measured 3.1 GHz and 0.7 GHz frequencies for the 5 and 23 stages respectively.

(P. S. Shanbhag, 2021) [17] designed a stacked inverter-based ring oscillator in 90nm CMOS technology with a mechanism to minimize the PVT variations at the temperature of 25^0C. Here, a voltage biased circuit is added to minimize the temperature variations and trim bits are added to decrease the frequency variations. The circuit operated at a voltage of 1.8V and generated 1MHz oscillations and 22.36 µW power.

(**Y. Ho, 2013**) [18] designed a single stage ring oscillator with bootstrapping technique in 90 nm IP9M SPRVT CMOS technology and operated near threshold voltageof 0.3V to make it temperature insensitive over the period of frequency. This circuit oscillates at a frequency of 235 MHz with a power consumption of 7 µW.

(**Sreenivasa Rao Ijjada D. C., 2016**) [19] discussed scaling limits and issues when it is beyond 45nm technology. And sighted many alternative devices to bulk CMOS especially at ultra nanoscale technologies. FinFET, TFET, SET, etc. are few of those kinds of devices. ExplainedFinFET merits and demerits in the present VLSI circuits.

(**Sreenivasa Rao Ijjada C. M., 2016)** [20] discussed the FinFET device full custom design using TCAD tool. To subdue the scaling issues a 20 nm FinFET designed using TCAD tools is characterized to check its superior control over the channel, performance and power budget.

(**Ajaykumar Dharmireddy, 2019)** [21] Designed tri gate SOI 32 nm technology Fin-FET. The fin dimensions such as fin width fixed as 5 nm, Wk=4.43, V_{GS}=0.7V, V_{DD}=0.7V, V_{DS}=0.05Vand the channel length is at 10nm. The fin height varied from 5 nm to 35 nm to see the impact of fin height on the device performance and observed its IV characteristics. From this it's observed that as the fin height increases effective channel with increase and the device performance increases.

(**Saurabh Sinha, 2012**) [22] discussed the predictive technology models (PTM) for FinFET technology forecasted and presented in the ITRS 2011. Explained the use of these modelsfrom the technology node 20nm to 7nm in the circuit implementation.

(**Sreenivasa Rao Ijjada A. d., 2020**) [23] designed a SOI-TG-FinFET using Verilog-A. The specifications of this device were considered as length=20nm, fin height=40 nm, fin

width=20 nm and the supply potential=0.7V. And designed CMOS inverter along with power gating low power scheme. Then a three-stage ring oscillator was designed and measured its frequency of oscillations as 2GHz, and power dissipation is 15% less than conventional ring oscillator.

(**A. A. Zayed, 2019**) [24] proposed and nine stage ring oscillator using Fin FET technology. The geometrical definitions of Fin-FET are defined as Lg=24 nm, Hfin=28 nm, Wfin=15 nm and operated at the voltage of 0.9V. The power consumption of this circuit is 264 µm and generates 4 GHz of oscillations.

(**Acharya, 2011**) [25] proposed a novel ring oscillator design optimized for performance. A nine-stage ring oscillator was implemented using a 130 nm CMOS process with transistor dimensions of Wn=200 nm, Wp=334 nm, and L=174 nm. The optimal device sizes were determined through a multi-objective optimization process using the CMODE algorithm. Phase noise, a critical performance metric, was calculated based on a specific formula.

$$\mathcal{L}\{\Delta f\} = \frac{8}{3\eta}\frac{\boldsymbol{\kappa T}}{P_{avg}}\frac{V_{DD}}{V_{char}}\frac{fo_{sc}^{2}}{\Delta f^{2}} \quad \text{—(2.2)}$$

Where $V_{char} = \frac{\Delta V}{\gamma}$

ΔV gate overdrive potential,

γ coefficient=2/3 for LCDs,

Δf offset frequency from carrierat which the phase noise measured,

η characteristic constant =0.7 to 0.9.

$$P_{avg} = \eta V_{DD} I_{avg}$$

$$P_{avg} = \eta V_{DD} N q_{max}\, f_{osc}$$

$$P_{avg} = \eta V_{DD}\, N C_{tot} V_{DD}\, f_{osc} \text{ ------- (2.3)}$$

(Lourts Deepak, 2012) [26] designed Fin-FET based three stage and five stage ring oscillator circuits in 32 nm technology for the frequencies of 40 GHz and 60 GHz. In this paper the resistor value is fixed at 10k ohms. The capacitor values are 4.3 pF and 2.65 pF for 40 and 60 GHz frequencies respectively. The delays of each stage in five stages ring circuits are 0.46 ps,0.48 ps,0.52 ps,0.54 ps and 0.56 ps.

(**N. Collaert, 2004**) [27] Discussed the modification of 180nm planner ring oscillator layoutfor the Fin-FET devices. Fabricated p-FET with gate length Lg=35nm and n-FET gate length Lg=25 nm, and10 nm fin width. Implemented 41-stage ring oscillator circuit with fin dimensions as Hfin=80 nm and Wfin=10 nm. The. P and N channel FETs effective channel widths are derived from Wp=92 (Wfin+2Hfin) and Wn=60 (Wfin+2Hfin) and set as Wp=17 µm and Wn=10 µm respectively. The potentials are set as Vth=0.2V and V_{DD}=1.5V. Then the fabricated 41 stage Fin-FET based ring oscillator circuit obtained 60 ps delay, Ioff = 60 nA and Idsat=380 µA.

(**A. A. Zayed, FinFET Based Low Power Ring Oscillator Physical Unclonable Functions, 2019**) [40] implemented a Fin-FET based ring oscillator for implementation of physical unclonable functions (PUFs) in order to use in low power IoT applications. Frequency divider and D-FFs were used in the place of counters. NCSU PDK 20 nm Fin-FET technology used in the design process, operated with a potential of 0.8V and achieved 264 µW of power.

(**K. Das, 2020**) [29] designed 180 nm CMOS and NMOS ring oscillators based on current staved technique to achieve a center frequency of 2.5 GHz suitable for Wi-Fi and Bluetooth applications. Made a comparison between two types of ring oscillators and made the conclusions as NMOS-based ring oscillator is optimal for phase noise performance and CMOS Ring oscillator is optimized for power of 4.61 µW.

(**K. S. Zaman, 2020**) [30] presented a three-stage ring oscillator design with current-starved technique to achieve low power for wireless applications which are operating within the ISM band of 5 GHz. This was designed in 130 nm CMOS process and simulated using ELDO Spice. This design was operated with a voltage of 1.2V and provided power consumption of 8 mW and a phase noise of -78 dBc/Hz at 1 MHz offset. The proposed delay cell occupied an area of 81.27 µm².

(**M. S. K. Hemel, 2023**) [31] described the role and importance of healthcare workers in monitoring the patients. IoT-based wireless health monitoring systems have the potential to significantly reduce human intervention. This research incorporates a single-ended ring oscillator VCO, fabricated using 50 nm CMOS technology, as a core component. The VCO demonstrated a tunable frequency range from 1.67 GHz to 3.13 GHz by adjusting the control voltage between 0.9 V and 1.5 V. To achieve an oscillation frequency of 2.4 GHz, an input voltage of 1V is applied.

(**Akanksha Gupta, 2020**) [32] proposed a hybrid CMOS VCO designed to achieve low power consumption and a wide linear operating range. The core of the design involved a CMOS voltage-controlled oscillator constructed using three-transistor CMOS NAND gates. Ring oscillator configurations with three, five, and seven stages were explored. A novel delay cell comprising three CMOS NAND gates operating at a supply voltage of 0.7V was introduced. The study focused on regulating output frequency, power dissipation, and the overall performance of the hybrid CMOS VCO across different stage configurations. The hybrid approach demonstrated superior linearity compared to traditional CMOS circuits, eliminating the need for additional components like resistors for tuning.

CHAPTER 3
CMOS RING OSCILLATOR DESIGN

In this chapter, discussed the implementation of basic inverter design and the importance of low power schemes in VLSI circuits design. Applied these low power schemes in the design of different inverter circuits for the implementation of five stage ring oscillator.

3.1 SCALING THEORY

The high-density chips in VLSI technology require transistors of sizes as small as possible. The concept of device size reduction is commonly known as scaling. Device scaling refers to deliberately reducing a device's total size using current technology while maintaining the exact geometric proportions of larger devices. Device scaling is a principle that involves reducing the size of a transistor by a constant factor in both horizontal and vertical dimensions. We anticipate that the scaling process will alter the gadget's operating parameters. The scaling trend according to ITRS (International technology road map for semiconductors) is presented in figure 3.1. Increased switching speed, reduced size and power dissipation are the benefits of scaling. With the scaled SiO2 thickness loses gate dielectric properties. In scaled devices, in addition to gate potential V_{GS}, drain potential V_{DS} will also show greater impact on the carrier flow in the channel [38].

With increase in drain potential V_{DS} the channel current can be increased by reducing the potential barrier even when $V_{GS} < V_{Th}$ is called subthreshold current The scaling process unavoidably causes noise, reducing high-density chips' dependability. In Long channel devices (LCD), the leakage components are tolerable, whereas in short channel devices (SCD), there is a significant number of leakages, which makes the device inefficient [1].

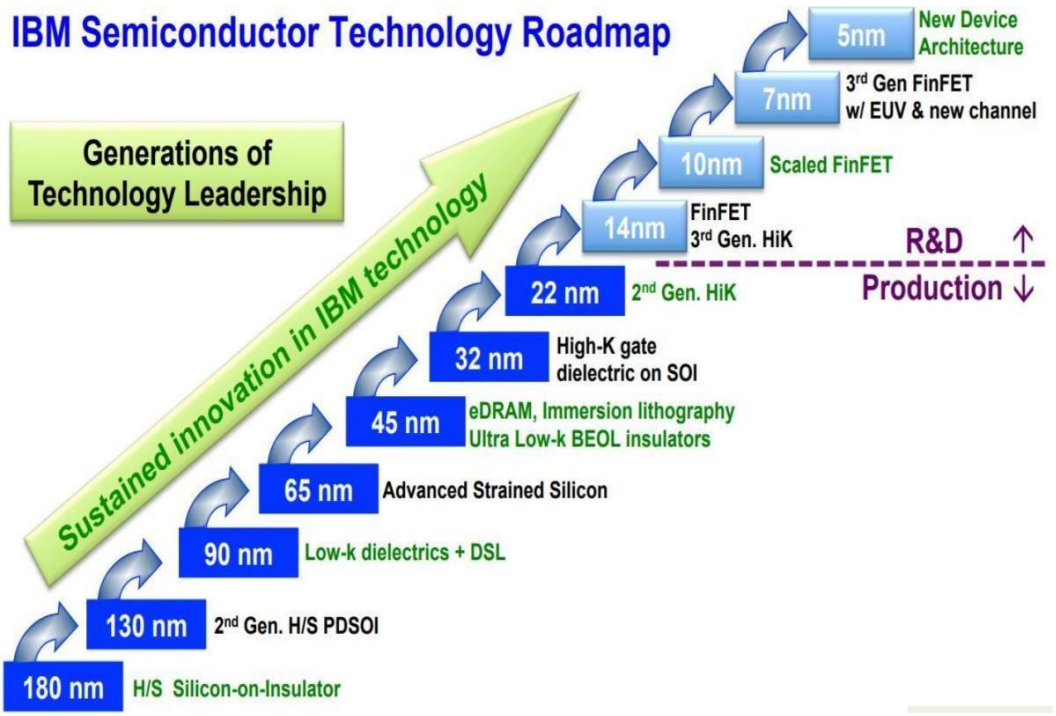


Figure 3.1: Trends in future size over time [36].

In LCDs, the dynamic power is more than the static power, whereas in SCDs, the static power is more than the dynamic power and increases rapidly along with the device scaling with respect to the dynamic power in a VLSI chip. The progress of the Bulk MOSFET scaling leads to serious Short Channel Effects (SCEs), which include the gate oxide, Sub-threshold, reverse bias, gate induced drain leakages, and device-to-device variations and punch-through effects [34]. Sub-threshold and gate oxide leakages contribute more shares in static power in the SCDs. In MOSFET, sub-threshold leakage current has dominated the gate leakage current up to the 65 nm technology. But, beyond this technology the scenario has reversed. According to the ITRS scaling trend, for a new technology, the amount of gate oxide thickness (t_{ox}) in the MOSFET was reduced by 18%. In MOSFET, for reliable operation, the minimum 't_{ox}' should not be less than 2 nm thickness. But practical calculation of t_{ox} at 65 nm technology, oxide thickness becomes 1.4 nm. Hence, there is a gate leakage which is 1000 times more than the sub- threshold leakage [14].

3.2 RING OSCILLATOR

The introduction about ring oscillators is well defined in section 1.5. Ring oscillators are thefundamental building blocks in PLLs and frequency synthesizers. Employing an odd number of inverter stages in a delay buffer chain ensures signal inversion, leading to sustained oscillations. This configuration effectively minimizes power consumption compared to even-numbered chains. Lower power consumption, stable frequencies, and rapid response times all contribute to more efficient and reliable communication systems.

A perfect ring oscillator should have the following features [16-18]:

- Low power consumption: Minimizes energy footprint and operating costs.
- Low phase noise: Ensures reliable signal transmission and minimizes data errors.
- Minimal stage delay: Reduces overall VCO delay and improves response time.
- Low jitter: Provides stable frequencies and accurate synchronization.
- Wide frequency range: Allows for versatile usage in various communication applications.

Traditional ring oscillator designs often suffer from high power consumption and temperature- dependent frequency variations. Increasing the number of stages for wider frequency range unfortunately amplifies stage delay, leading to slower oscillation and higher power draw. Addressing these challenges requires innovative approaches:

- **Bias current control**: Adjusting the bias currents of transistors in each delay unit allows precise control of propagation delay, enabling faster oscillations without increasing stage count.
- **Sleepy stack approach**: This technique combines bias current control with a dedicated network to regulate power consumption.
- **Single-stage inversion loop**: Which involves only one inversion between the output and input stages, is employed to minimize power consumption. This approach effectively reduces power dissipation compared to designs with multiple inversions.

By strategically implementing these techniques, modern ring oscillator designs can achieve significantly improved performance compared to traditional approaches. VCO is responsible for generating precise and stable clock signals, and is achieved through the ring oscillator, and a crucial aspect of their performance is low jitter. Jitter is defined as the short-term variations in the timing of a clock signal. These variations can be initiated by noise, power supply fluctuations, and the temperature changes.

High jitter can disrupt digital circuits and degrade signal integrity, leading to errors and performance issues. Several inherent features of ring oscillators contribute to their ability to achieve low jitters:

- **Differential operation**: Many ring oscillators utilize differential designs, where two identical loops run in opposite directions. This cancels out common noise sources, reducing jitters.
- **Symmetrical delays**: By carefully matching the delays of each inverter stage, we willachieve more stable and predictable oscillations, minimizing jitters.
- **Controlled biasing**: Adjusting the bias current of the transistors in the inverters allows fine-tuning of the oscillation frequency and jitter performance.

Ring oscillators used to use more power and have more excellent phase noise for the same frequency, but they had a lower FOM than LC oscillators. The target performance for the VCOis the center frequency of 200 MHz and a phase noise requirement of -100 dBc @ 100 kHz. The implemented VCO was compared to an existing LC oscillator with similar specifications. The key trade-off between the ring oscillator and LC oscillator lies in area and power consumption. Ring oscillators generally occupy a smaller area but consume more power compared to LC oscillators [8]. This trade-off is a critical consideration when selecting the appropriate oscillator type for a specific application.

3.3 RING OSCILLATOR DESIGN

A ring oscillator involves an odd number of inverter stages which are connected in a closed loop configuration. In this configuration, the output of each inverter stage is the input to the subsequent stage and the final stage of inverter output is feeding back to the first stage. This arrangement offers advantages such as straightforward implementation and a wide operating frequency range at low control voltages. Each inverter stage within the ring oscillator contributes a delay to the overall oscillation period. For example, consider the five-stage CMOS ring oscillator as in figure 3.2, It consists of five basic CMOS inverters connected in a circular pattern [25]. The oscillator only relies on electricity for its operation. Within the realm of semiconductor physics, there exists a point at which the oscillations become uninterrupted. Circuits may employ this approach. Amplify the vibrations at a frequency of 33 oscillations per unit of time. Due to their comparable power consumption, people often use voltage-controlled oscillators (VCO) and ring oscillators. The oscillator's speed limitations stem from the maximum voltage it can supply to its circuits. The delay occurs at different stages of the chain.

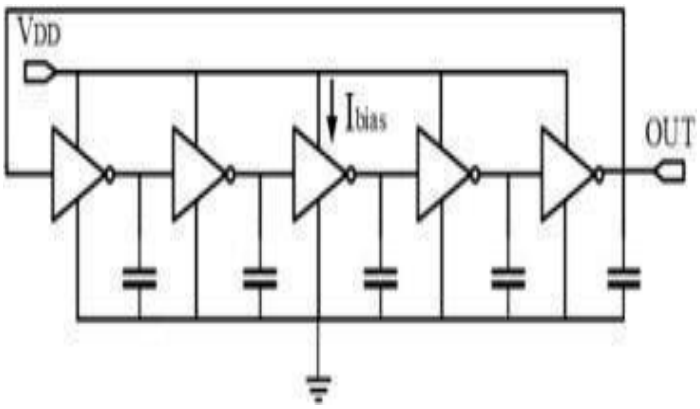


Figure 3.2: A Five stage Ring Oscillator [28].

In ring oscillator,

- Each inverter introduces a slight delay due to its switching time.
- The cumulative delay of the loop will determine the oscillation frequency.
- The output signal transitions between high and low voltage levels, creating a clock signal.

For an 'N' stage ring oscillator, the frequency of oscillations (f_{osc}) can be calculated with equation earlier presented in (1.1) and once again shown in equation (3.1). Where, the delay (τ_d) is the single inverter delay which is approximated by the time constant of an equivalent RC low-pass filter.

$$f_{osc} = \frac{1}{2N\tau_d} ----(3.1)$$

3.4 BASIC INVERTER

As we know, inverter is the basic component in the ring oscillator. The fundamental CMOS inverter employed with a PMOS and an NMOS transistor connected as shown in figure 3.3. When the input voltage (Vin) is low (logic 0), the PMOS will conduct, and pulls the output high to V_{DD}. Conversely, when Vin is high (logic 1), the NMOS transistor will conduct, pull the output low to ground (GND). This complementary structure enables low static power consumption [29-30]. For optimal inverter operation, both the NMOS and PMOS transistors must operate in the saturation region, defined by the conditions in equation (3.2). Where V_{GS} and V_{Th} are the gate to source and threshold potentials.

$$V_{GS} > V_{Th} \text{ and } V_{DS} > (V_{GS}-V_{Th}) ------ (3.2)$$

This operating region introduces inherent resistance and parasiticcapacitances within the transistors, contributing to propagation delay (τ_d). Propagation delay is the sum of rise and fall times. Therefore, the rise time or rise time delay ($\tau rise = \tau dHL$) and fall time or fall time delay ($\tau fall = \tau dLH$) are measured with equation (3.3) and equation (3.4) respectively.

$$\tau rise = \tau dHL = \ln(2)\, Rnon\, Cload ----(3.3)$$

$$\tau fall = \tau dLH = \ln(2)\, Rpon\, Cload \text{ - } (3.4)$$

Where, '$Rnon$' is the saturation on resistance of NMOS device and '$Rpon$' is saturation on resistance of PMOS transistor. '$Cload$' is the load capacitance of the inverter stage.

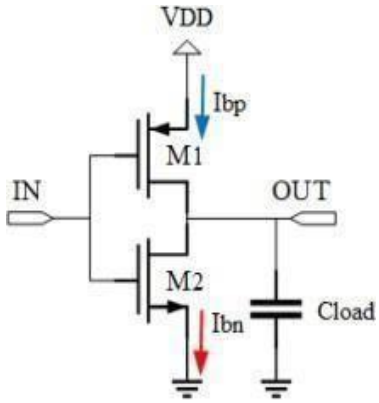


Figure 3.3: Basic Inverter circuit [28].

Total delay of an inverter is given by equation (3.5) and the frequency of the inverter circuit is given by the equation (3.6).

$$\tau d = (\tau dHL + \tau dLH)/2 \text{ ------ (3.5)}$$

$$f_{osc} = \frac{1}{2\tau_d} - - - \text{(3.6)}$$

In integrated circuits, with technology above 180 nm, dynamic power makes up most of the power share,whereas static power predominates in chips with technology below 180 nm. Subthreshold leakage or current primarily causes static power dissipation. Subthreshold leakage occurs when the potential in between gate and source is lower than the device threshold voltage, a current flows in the device to the source from the drain [32-33]. Subthreshold current exhibits an exponential dependence on device threshold voltage. As device dimensions shrink into the nanoscale regime, aggressive threshold voltage reduction starts to a pronounced rise in subthreshold leakage. Consequently, minimizing this leakage current becomes crucial for optimizing device performance and energy efficiency at advanced technology nodes.

Numerous strategies have been proposed to mitigate static power consumption, including the stack approach, sleep transistor approach, sleepy stack approach (**SS**), zigzag approach, sleepy keeper (**SK**) technique, dual Vth technique, dual Vth with sleep transistor, dual Vth with zigzag (**dVth Zigzag**), sleepy dual Vth, Sleepy stack with dual Vth (**SS dVth**) and dual Vth with sleepy keeper (**SK dVth**) [37].

While each method offers specific advantages, they all come with certain trade-offs, as outlined in reference [49]. Optimizing the inverter design itself (e.g., using current-starved inverters) can help achieve higher oscillation frequencies without significantly increasing the number of inverters. Techniques like variable biasing or using additional control circuits can be employed to adjust the oscillation frequency within a certain range, even with a fixed number of inverters in the ring. NMOS based, CMOS inverter based, CS amplifier based, Source follower type and Differential amplifier based are the few techniques. The fundamental inverter depicted in Figure 3.3 comprises PMOS and NMOS transistors with respective widths of Wp=2 and Wn=1 units.

3.4.1 Stack Technique

The stack technique involves replacing each individual transistor with a pair of identical transistors connected in series. This modification results in a 50% reduction in the width of each transistor, as depicted in Figure 3.4. This is a power-saving strategy in CMOS circuits that involves replacing individual transistors with pairs of series-connected transistors. This modification has several benefits:

Increased Series Resistance: The series connection of transistors increases the effective resistance between the power supply (V_{DD}) and ground (GND). This higher resistance limits the flow of leakage current when the circuit is in the off state.

Reverse Bias: When both transistors in a stack are turned off, a reverse bias condition is induced between them. This reverse bias helps to further suppress leakage current.

Reduced Switching Noise: The increased resistance introduced by this technique can help to attenuate the switching noise, which is the major supplier of power expenditure and circuit instability.

While the stack technique offers power advantages, it comes with some trade-offs: **Increased Area:** The addition of extra transistors can lead to a slight increase in circuit area. **Potential Performance Impact:** The increased resistance and additional capacitance introduced by the stacked transistors might slightly degrade the circuit performance in the view of speed.

3.4.2 Sleepy Transistor Method (STM)

Sleepy transistor approach involves inserting an additional-transistor between the power supply and the pull-up network, as well as between the ground and the pull-down network, as illustrated in Figure 3.5. This differs from the standard inverter circuit in CMOS technology, where the PMOS transistor is directly connected to V_{DD} and the NMOS transistor to the ground. When the circuit is in sleep mode, the sleep transistors are deactivated, effectively isolating the main circuit from the power supply and significantly reducing leakage current [34]. By isolating the main circuit from the power supply during idle periods, the sleepy keeper effectively minimizes leakage current. However, this technique incurs area overhead and potential state loss due to floating node issues. Despite these drawbacks, it remains a viable option for power reduction. This technique is also known as gated V_{DD}, multi-threshold CMOS (**MTCMOS**), or gated GND. These sleep transistors can be configured with either high or low threshold voltages (V_{Th}).

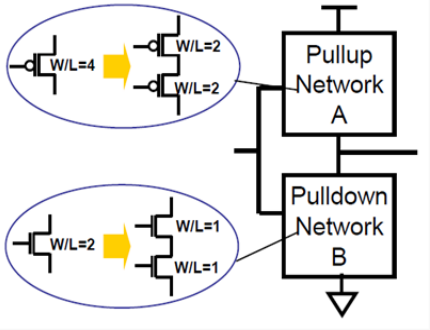


Figure 3.4: Stack inverter circuit**.**

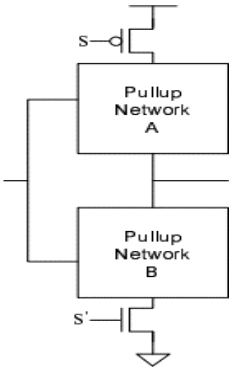


Figure 3.5: Sleepy transistor inverter.

While the sleep transistor approach offers significant power savings, it comes with some trade-offs: **Additional Area:** The insertion of sleep transistors requires extra space on the chip. **State Retention Issues:** In certain scenarios, floating node conditions can arise, leading to potential state loss during sleep mode. **Design Complexity:** Integrating sleep transistors into a circuit design can increase design complexity and require careful consideration of transistor sizing and biasing. The sleepy keeper approach introduces additional transistors between the power supply and the main circuit elements to reduce power consumption Sleepy Plus stack technique.

3.4.3 Sleepy stack technique

The sleepy stack technique combines the stack and the sleepy transistor approaches. In this configuration, a stacked pair of transistors is used, with each transistor having a specific width-to-length (W/L) ratio. This arrangement is designed to maintain an equivalent input capacitance compared to the original stacked structure. In the sleepy stack configuration, the sleep transistors function similarly to their role in thestandalone sleep transistor approach. When the circuit is active, the sleep transistors are inthe ON state, allowing for proper operation. In sleep mode, they are deactivated, effectively isolating the main circuit and reducing leakage current. Compared to the stacktechnique alone, the sleepy stack offers a faster switching speed. This is because the sleep transistors can quickly activate and de-activate, ensuring that the main circuit remains connected to the power supply during active mode and isolated during sleep mode.

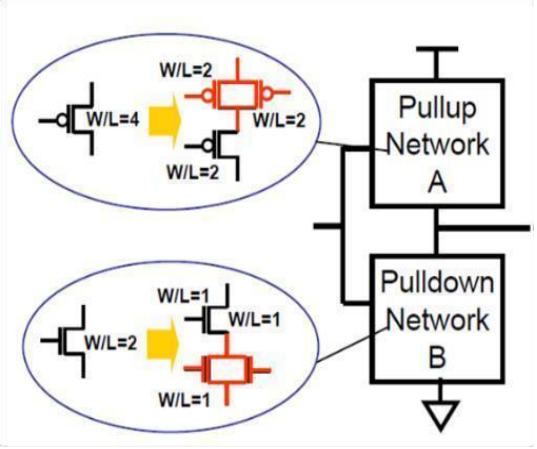


Figure 3.6: Sleepy stack inverter

The sleepy stack design also maintains a consistent voltage level at the drain of each sleep transistor, regardless of the state of the other parallel transistors. This ensures that the low-V_{TH} transistor connected to the gate output receives current promptly, preventing state lossduring sleep mode [14]. For example, the stack might consist of two PMOS transistors with a W/L of 3 and two NMOS transistors with a W/L of 1.5. To implement the sleepy stack, a high V_{Th} PMOS sleep transistor (W/L = 3) is connected in parallel with one of the PMOS transistors in the stack. Similarly, a high V_{Th} NMOS sleep transistor (W/L = 1.5) is connected in parallel with one of the NMOS transistors in the stack. While the sleepy stack provides significant power savings, it comes with the trade-off of increased area overhead due to the additional sleep transistors.

3.4.4 Zigzag technique

The zigzag technique is another power-saving method that focuses on reducing the active time overhead associated with the sleep transistor approach. In a single-logic circuit (Figure 3.7), the zigzag technique involves deactivating the pull-down network for gates with high outputs and activating the pull-up network for gates with low outputs. This strategic switching helps to minimize power consumption. To set the output logic to 1, a pull-down sleep transistor is employed. Conversely, a pull-upsleep transistor is used to set the output logic to 0. This approach can effectively address the floating state issue that sometimes arises in sleep transistor techniques, although the success may vary. The inclusion of sleep transistors in the circuit design can increase the resistance of the active signal path, leading to a shorter transmission delay.

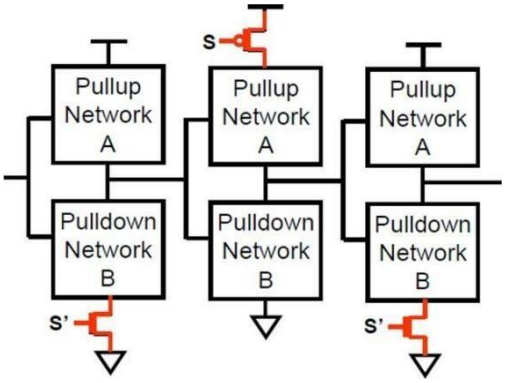


Figure 3.7: Zigzag inverter circuit**.**

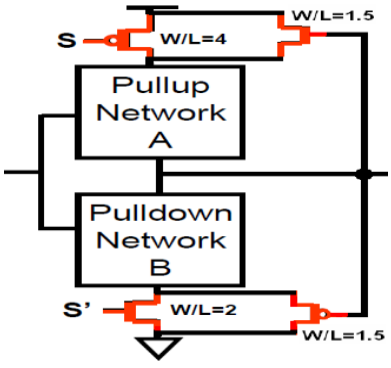


Figure 3.8: Sleepy keeper inverter

This approach is employed to maintain the circuit's logical state during sleep mode. To construct a ring oscillator, an odd number of inverting and non-inverting stages are interconnected in a loop configuration. This research focuses on ring oscillators utilizing source-coupled differentially loaded delay cells implemented in CMOS technology.

3.4.5 Sleepy keeper technique

To reduce the transmission time and maintain the logic states, we have implemented two modifications to the sleep transistor circuit shown in Figure 3.5. Figure 3.8 illustrates amodified sleepy stack technique that incorporates additional sleep transistors for improvedperformance. The sleepy keeper technique is a highly effective method for reducing power consumption in digital circuits. It involves the strategic placement of additional transistors(sleep transistors) within the circuit to selectively isolate specific parts of the circuit from the power supply during idle periods. This isolation significantly reduces leakage current, leading to substantial power savings. By strategically placing these transistors, the circuit can effectively maintain its logical state while minimizing power consumption. Specifically, an NMOS keeper transistor with W/L = 1.5 is attached in parallel with a sleepy transistor of PMOS type in the pull-up network. Similarly, a PMOS keeper transistor of W/L = 1.5 is attached in parallel with another sleep transistor of NMOS type in the pull-down network.

This configuration offers several advantages: **Improved State Retention:** The keeper transistors help to maintain the desired logic state during sleep mode, even when the main sleep transistors are deactivated. **Faster Recovery:** The presence of the keeper transistors can accelerate the circuit's recovery from sleep mode, enabling a quicker return to active operation. **Reduced Floating Node Issues:** The keeper transistors can help to mitigate the risk of floating nodes, which can lead to unpredictable behavior and potential state loss.

3.5 RING OSCILLATOR ANALYSIS

In the ring oscillator circuit, the frequency of oscillations decreases as the number of inverting stages increases. This inverse relationship arises due to the cumulative effect of individual stage delays. Therefore, minimizing the delays associated with each stage is crucial for achieving higher operating frequencies. Adjusting the bias currents within the oscillator can effectively regulate the propagation delay of each stage. By optimizing these currents, it is possible to reduce the overall delay and consequently increase the oscillation frequency. Operating the PMOS and NMOS transistors in the subthreshold region can lead to a rise in current within each stage. This increase in current can contribute to a higher oscillation frequency (f_{osc}). The infinite gate input impedance of MOSFETs ensures that all stages in ring oscillator behave identically. A five-stage ring oscillator has been designed and simulated using various technological nodes (180 nm node, 90 nm node, 65 nm node, and 45 nm node). The focus of this thesisis to calculate the effect of different low-power techniques on the oscillator's performance. Key metrics analyzed include static power consumption and dynamic power consumption, delay of the circuit response, and the area of the design.

3.5.1 Design: The design of the ring oscillator targets the following specifications:

Frequency Range: 1 GHz to 2 GHz Supply

Voltage (VDD): 1.8 V to 0.4 V Power

Consumption: Less than 30 mW

Technology Nodes: 0.180µm, 0.090 µm, 0.065 µm, and 0.045 µm.

In the basic CMOS inverter shown in figure 3.2. The source current (Ibp) flows via the PMOS transistor, while the sink current (Ibn) flows through the NMOS transistor. Under balancing conditions, the currents of both transistors have the same magnitude, hence we can write equation (3.7). The proper sizing of components in the inverter enables this task. The NMOS and PMOS saturation currents are expressed as in equation (3.8).

$$I_{bn} = I_{bp} \text{ ---------} (3.7)$$

$$k_n(V_{GS} - V_{THn})^2 = k_p(V_{SG} - V_{THp})^2 \text{-----(3.8)}$$

The rise and fall time delays in equations (3.3) and (3.4) are influenced by the bias currents within the device. By adjusting the bias currents, it's possible to modify these delays and consequently optimize the overall performance of the ring oscillator. The modified rise and fall delays are now expressed in equations (3.9) and (3.10) in terms of bias currents, capacitance and supply voltage.

$$\tau_{rise} = \tau_{dHL} = \frac{C_{eff}(V_{DD} - V_1)}{I_{bn}} \text{-----(3.9)}$$

$$\tau_{fall} = \tau_{dLH} = \frac{C_{eff}V_1}{I_{bp}} \text{-----(3.10)}$$

In equation (3.9), the effective capacitance (Ceff) includes the parasitic capacitance (C_G) of the inverter, which is in series with the load capacitance (Cl). In equations 3.7 and 3.8, assume $V_{SG} = V_{DD} - V_1 \& V_{GS} = V_1$. V_1 is the triggering voltage of the inverter (the voltage at which the inverter transitions from the off to the on state)

$$k_n(V_1 - V_{THn})^2 = k_p(V_{DD} - V_1 - V_{THp})^2$$

$$(V_1 - V_{THn})^2 = \frac{k_p}{k_n}(V_{DD} - V_1 - V_{THp})^2$$

$$V_1 = \frac{\sqrt{\frac{k_p}{k_n}}(V_{DD} - V_{THp}) + V_{THn}}{(\sqrt{\frac{k_p}{k_n}} + 1)} \text{----(3.11)}$$

After making changes and simplifying, equation (3.8) gives the NMOS device size.

$$\frac{W}{L} = \frac{C_l}{\tau_d \mu_n C_{ox}(V_{DD} - V_{THn})}\left[\frac{2V_{Th}}{V_{DD} - V_{THn}} + ln\left(\frac{4(V_{DD} - V_{THn})}{V_{DD}}\right) - 1\right] \text{---(3.12)}$$

When considering the impact of bias currents, oscillation frequency, and amplitude on the ring oscillator, equations (3.2) and (3.5) can be modified to incorporate these factors. These revised equations would express the relationships between oscillation frequency, amplitude, and bias currents more comprehensively.

Assume that $I_{bn} = I_{bp} = I_{cont}$.

$$\tau_d = \frac{V_{osc} C_G}{I_{cont}} \quad \text{------(3.13)}$$

$$f_{osc} = \frac{I_{cont}}{2NV_{osc}C_G} \text{----------(3.14)}$$

Where 'V_{osc}' is the aamplitude of oscillations, C_G' is the parasitic capacitance associated with both PMOS andNMOS transistors and 'Icont' is the control current.

These parameters are likely used in equations (3.13) and (3.14) to describe the relationship between oscillation frequency, amplitude, and bias currents. Once all the above equations substitute all these in equations (3.9) and (3.10), the equation (3.14) is written as in equation (3.15).

$$f_{osc} = \frac{I_{cont}}{NV_{DD}C_{eff}} \text{----------(3.15)}$$

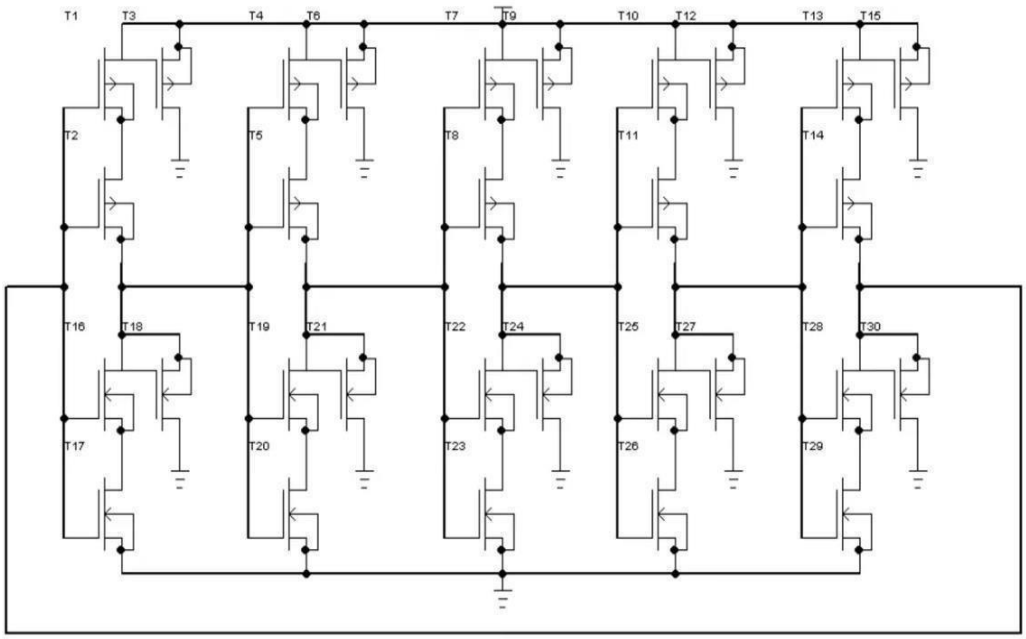


Figure 3.9: Five Stage Sleepy Keeper Ring Oscillators

Figure 3.9 illustrates a five-stage ring oscillator circuit incorporating the sleepy keeper technique and a bias current. To ensure proper operation, the network input impedance must be significantly larger than the output impedance of the last inverter amplifier stage. To match with the output impedance of the amplifier, which is typically in the scale of 50 kΩ, RC network resistance should be selected to be around 10 kΩ. This impedance mismatch helps to minimize reflections and ensure efficient signal transfer. The frequency of an RC network is given by

$$f = \frac{1}{2\pi RC}$$

To achieve 2 GHz of frequency, in the RC network chooses R=10KΩ. Then the capacitor value is $C = \frac{1}{2\pi Rf} = 31.4fF$

The equations (3.3) and (3.4)

$$r_{dHL} + r_{dLH} = 0.7(R_{non} + R_{pon})\, C_l \text{------(3.16)}$$

$R_{non} = 3.4K\Omega$ and $R_{nop} = 3.4K\Omega$, $C_{oxn} = 0.625fF$ and $C_{oxp} = 1.25fF$.

N=5 for five stage ring oscillator, hence $C_l = \frac{N}{2(C_{oxn}+C_{oxp})} = 1.33fF$.

Substitute all the values in equation 3.16, then

$$r_{dHL} + r_{dLH} = 0.701(3.4K + 3.4K)1.33f = 6.33\text{psec.}$$

Therefore, the frequency of the five-stage ring oscillator is

$$f_{osc} = \frac{1}{2*5*6.33} = 15.7GHz.$$

With the simulations, the total delay is measured as

$$\tau_d = \tau_1 + \tau_2 + \tau_3 + \tau_4 + \tau_5 = 1.91 + 2.12 + 2.89 + 3.75 + 4.91.$$

3.6 RESULTS

A five-stage ring oscillator is implemented using CMOS technology on different technological nodes such as 180 nm node, 90 nm node, 65 nm node, and 45 nm node. Different low-power techniques, including the stack technique, sleep transistor technique, zigzag technique, sleepy stacktechnique, sleepy keeper technique, dual Vth technique with sleep transistor, dual Vth with zigzag (**dVth Zigzag**), sleepy dual Vth, Sleepy stack with dual Vth (**SS dVth**) and dual Vth with sleepy keeper (**SK dVth**), were incorporated into the design.

Among all these techniques, dual Vth with sleep transistor approach demonstrated superior results across all performance metrics. This technique effectively combined the advantages of dual threshold voltages and sleep transistors to achieve optimal power savings and performance. The design results of all the low power techniques implemented in 180 nm technology node are presented in table 3.1 for the comparison.

Table 3.1: Five stage ROs results in 180 nm technology.

180nm	Delay (s)	Static Power (W)	Dynamic Power (W)	Area (μm^2)
Base Case	7.18250E-11	5.01080E-09	1.56650E-05	3.25100E+02
Stack	2.08090E-10	3.43690E-10	1.21850E-05	1.12550E+03
Sleep	1.18510E-10	8.63775E-10	1.61330E-05	1.02590E+03
Zigzag	7.34040E-11	1.00790E-09	1.58310E-05	7.40900E+02
Sleepy Stack	1.45740E-10	6.01490E-10	1.18560E-05	1.96310E+03
Sleepy Keeper	**1.58320E-10**	**3.51200E-10**	**1.07110E-05**	**1.74170E+03**
Sleep dVth	1.44420E-10	1.42100E-12	1.66510E-06	1.02590E+03
SS dVth	1.65210E-10	7.95120E-14	1.15490E-05	1.96310E+03
SK dVth	**1.94390E-10**	**3.62535E-12**	**1.10540E-05**	**1.74170E+03**

The five-stage ring oscillator circuit is designed in 90 nm technology with all the forementioned low power schemes and simulated with Cadence tools, extracted the parameters are presented in table 3.2 for the comparison. The oscillator incorporates various low-power techniques. Among these techniques, the SK dVth method and the sleepy keeper approach consistently outperformed the others in terms of overall performance.

The five-stage ring oscillator circuit is designed in 65 nm technology with all the forementioned low power schemes and simulated with Cadence tools, and extracted the parameters are presented in table 3.3. The oscillator incorporates various low-power techniques. Among these techniques, the SK dVth method and the sleepy keeper approach consistently outperformed the others in terms of overall performance.

Table 3.2: Comparison of five stage ROs in 90nm technology.

90nm	Delay (s)	Static Power (W)	Dynamic Power (W)	Area (μm^2)
Base Case	6.62200E-11	4.46590E-09	1.46650E-06	8.94000E+01
Stack	1.94770E-10	2.37820E-10	1.22250E-06	3.09510E+02
Sleep	1.09060E-10	5.71665E-10	1.51950E-06	2.82120E+02
Zigzag	6.69080E-11	6.92145E-10	1.48070E-06	2.03750E+02
Sleepy Stack	1.32350E-10	4.25730E-10	1.09050E-06	5.39850E+02
Sleepy Keeper	**1.4204E-10**	**2.50765E-10**	**1.00890E-06**	**4.78970E+02**
Sleep dVth	1.60600E-10	5.61005E-13	1.56180E-06	2.82120E+02
SS dVth	1.85890E-10	1.01260E-12	1.10070E-06	5.39850E+02
SK dVth	**2.1112E-10**	**1.56305E-12**	**1.04640E-06**	**4.78970E+02**

Table 3.3: Comparison of five stage ROs in 65 nm technology.

65nm	Delay (s)	Static Power (W)	Dynamic Power (W)	Area (μm^2)
Base Case	1.01950E-10	1.82580E-08	8.68370E-07	4.66300E+01
Stack	2.81180E-10	2.51305E-09	7.29060E-07	1.61440E+02
Sleep	1.68330E-10	7.07990E-09	9.32530E-07	1.47160E+02
Zigzag	1.03690E-10	6.58590E-09	8.89820E-07	1.06280E+02
Sleep Stack	1.94630E-10	3.91935E-09	6.21660E-07	2.81590E+02
Sleepy Keeper	**2.0754E-10**	**2.98780E-09**	**5.6278E-07**	**2.49830E+02**
Sleep dVth	4.05620E-10	2.90255E-11	9.99960E-07	1.47160E+02
SS dVth	4.28350E-10	3.42585E-11	6.46130E-07	2.81590E+02
SK dVth	**4.98760E-10**	**8.64475E-10**	**6.02250E-07**	**2.49830E+02**

Table 3.4: Comparison of five stage ROs in 45nm technology

45nm	Delay (s)	Static Power (W)	Dynamic Power (W)	Area (μm^2)
Base Case	6.57570E-12	1.01260E-06	1.27880E-06	2.23500E+01
Stack	4.15930E-11	1.52715E-07	2.73180E-07	7.73800E+01
Sleep	1.95040E-11	3.94875E-07	1.25520E-06	7.05300E+01
Zigzag	9.74120E-12	3.92655E-07	1.27300E-06	5.09400E+01
Sleepy Stack	1.98220E-11	2.32115E-07	6.07150E-07	1.34960E+02
Sleepy Keeper	**2.00950E-11**	**1.65355E-07**	**5.96430E-07**	**1.19740E+02**
Sleep dVth	2.26550E-11	8.65395E-09	1.22420E-06	7.05300E+01
SS dVth	3.07810E-11	1.02790E-08	5.84470E-07	1.34960E+02
SK dVth	**3.10200E-11**	**7.41560E-09**	**5.8760E-07**	**1.19740E+02**

The five-stage ring oscillator circuit is designed in 65 nm technology with all the forementioned low power schemes and simulated with Cadence tools, and the parameters are presented in table 3.4 for the comparison. The oscillator incorporates various low-power techniques. Among these techniques, the SK dVth method and the sleepy keeper approach consistently outperformed the others in terms of overall performance. Sleepy keeper technique consistently outperformed the others in terms of overall performance.

Figure 3.10 presents a comprehensive comparison of five-stage ring oscillators implemented using various technologies (180 nm node, 90 nm node, 65 nm node, and 45 nm node). All the designs are simulated with a Cadence tool and results are noted in tables 3.1-3.4, and the graphs are presented for static and dynamic power, delay, area and area overheads are provided in figure 3.10. Based on this the following performance metrics are evaluated:

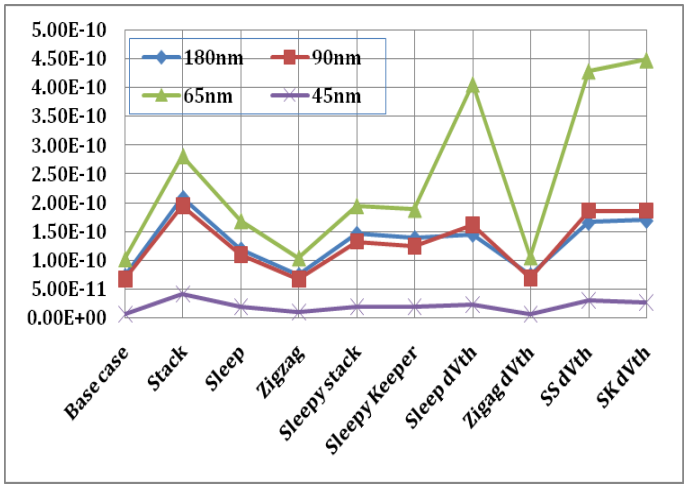
Comparison of Delay Values: This plot illustrates the propagation delay for each ring oscillator configuration across different technology nodes. From this plot, we can understand that the designs using sleepy keeper and zigzag dVth technique on 45nm technology offers reduced delay.

(a) Comparison of Static Power: This plot compares the static power of the oscillators. From this plot, we can understand that the sleepy keeper and SS dVth techniques offers low static power on 180 nm technology node.

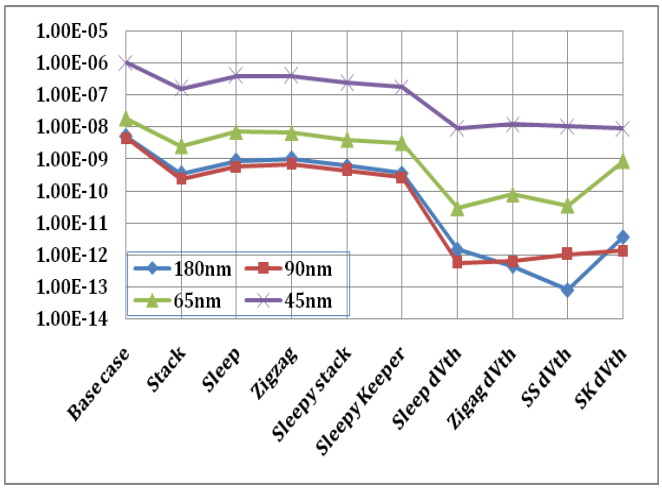
(b) Comparison of Dynamic Power: This plot shows dynamic power consumption. From this plot, it can be understood that sleepy keeper and SS dVth technics offer low dynamic power on 45nm node.

(c) Comparison of Areas: This plot compares the physical area occupied by each ring oscillator design. From this plot we can understand that sleepy keeper and SS dVth techniques on 45 nm node occupies less area after base technique.

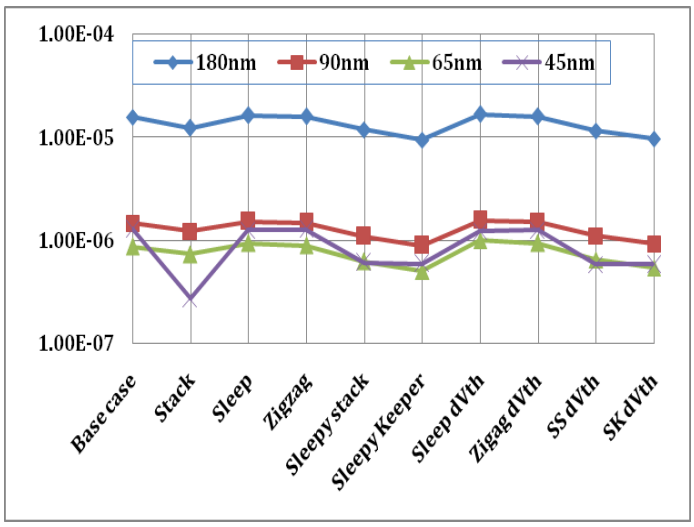
(d) Comparison of Area Overheads: This plot focuses specifically on the additional area overhead introduced by the different low-power schemes employed in the oscillators. As mentioned in the above, the area overhead is less for the sleepy keeper and SS dVth.



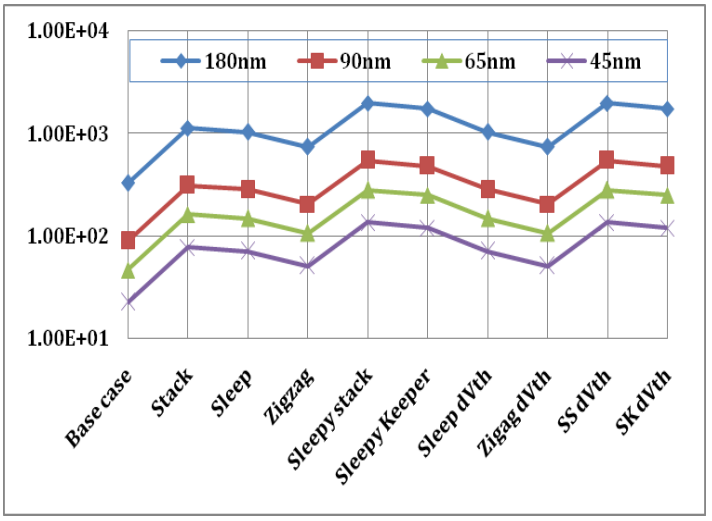
(a)



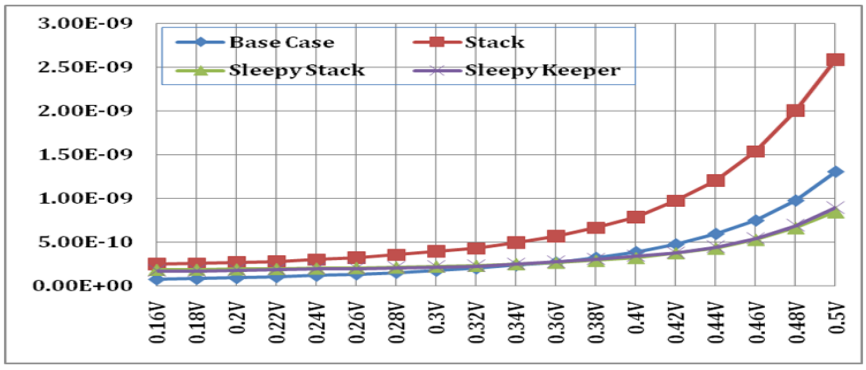
(b)



(c)



(d)



(e)

Figure 3.10: Five stage ROs results: (a) Delay values (b) Static power (c) Dynamic power (d) Area (e) Area overhead.

Technology Node Impact: As the technology down scaling from 180 nm technology node to 45 nm node, significant improvements in delay and area are observed. The SK dVth and sleepy keeper approaches consistently outperformed other techniques in terms of overall performance. Compared to the base case (no low-power techniques), the sleepy stack and sleepy keeper methods achieved substantial reductions in static and dynamic power consumption.

Delay: The design with 45 nm technology node the ring oscillator circuit exhibited the shortest delay compared to the other nodes designs.

Area: Designs with 45 nm technology node usually take less overhead area than the designs performed at the higher technology nodes.

Power Consumption: The sleepy keeper and dual Vth techniques achieved significant reductions in both static and dynamic power consumption.

The transient response of the five-stage ring oscillator circuit with sleepykeeper and bias current techniques in figure 3.9 is shown in figures 3.11 and 3.12. From this response, it is observed that the frequency of oscillations of the circuit is 1.27 GHz.

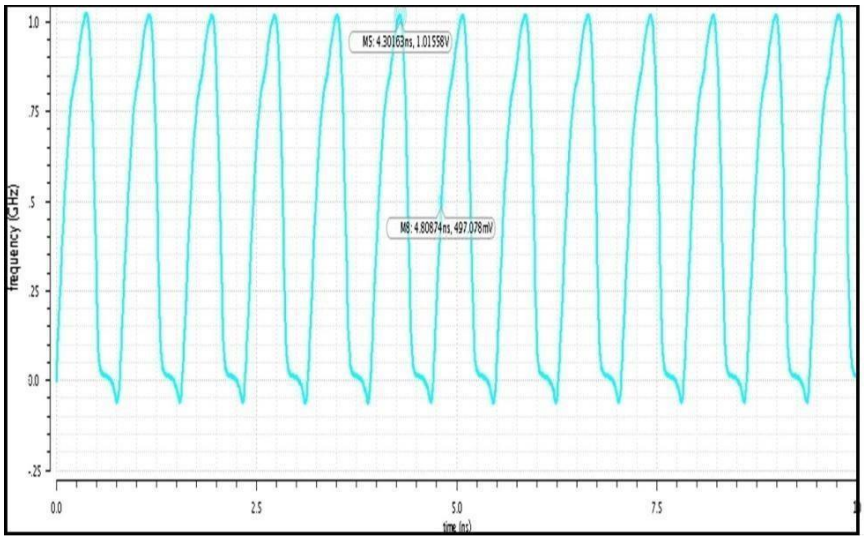


Figure 3.11: Five stage ring oscillator output

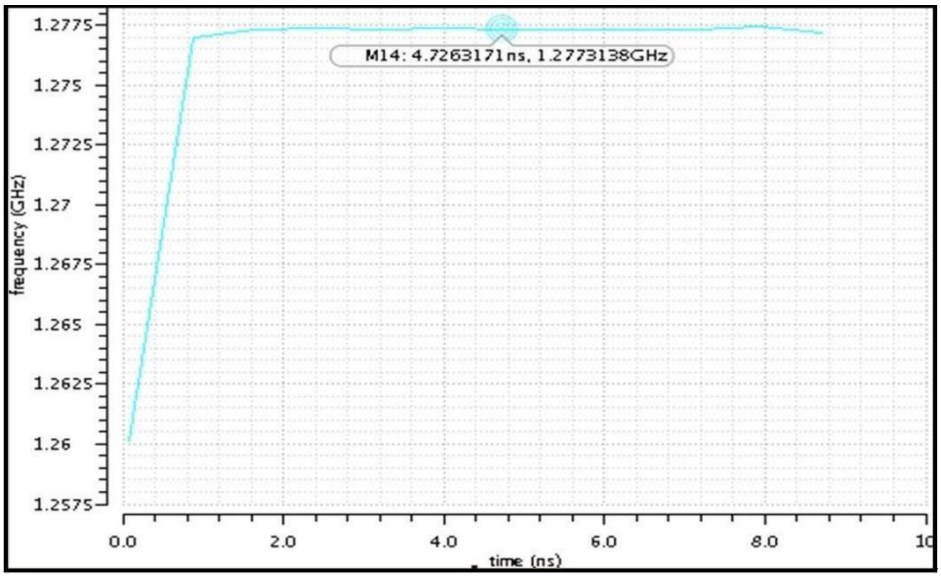


Figure 3.12: Five stage ring oscillator frequency response**.**

Table 3.5 provides a detailed comparison of power, delay, and area of the proposed ring oscillator with other ring oscillator designs along with different low power techniques.

Table 3.5: Comparison parameters of proposed work and existing work

Process parameter	[41]	[42]	[27]	[44]	[24]	[48]	[this work]
Process, nm	90	130	130	130	180	90/90	45
Stages	7	5	5	3	5	9/3	5
Supply, V	1.2	1	1.8	3.3	1.8	1.3/0.3	1
Delay, sec	43.84p	---	--	4.37n	--	--	0.025p
Frequency, Hz	1.2G	24M	20M	199.5M	1M	2G/235M	1.28G
Power, W	0.047m	16.85 µ	0.56m	55.56µ	34.1 µ	3m/10µ	16µ
Area, mm^2	111.3	1.22	0.22	13.2	0.084	0.56/0.02	0.0119
Technique	Current starved	Current starved	Dual Vth	RC Network	Sleepy dVth	Differe /boot strap	Sleepy keeper

From the information available in table 3.5, it is clearly understood that the sleepy keeper approach used in the ring oscillator design consistently outperformed the others in terms of overall performance. The ring oscillator design incorporating the sleepy keeper technique demonstrated superior results in terms of power consumption, area, and delay compared to existing literature. The proposed design achieved the highest oscillation frequency and bandwidth within the studied group of ring oscillators.

The proposed oscillator design results compared the designs on the same 45nm node are presented in table 3.6. Still our design shows the same superiority

Table 3.6: Comparison with only 45nm technology work

Process	[82]	[83]	[84]	[85]	[this work]
Process, nm	45	45	45	45	45
Stages	3	3	5	9	5
Supply, V	1	1	1	0.7	0.5
Delay, sec	4.53n	---	--	4.37n	0.025p
Frequency, Hz	200K	2.2G	1.01M	341M	1.28G
Power, W	1.73	52.7m	20.5m	1.93µ	16µ
Area, mm^2	--	--	--	--	0.0119
Technique	Current straved	Current starved	Current starved	Boot strap	Sleepy keeper

Summary: CMOS inverter-based ring oscillator designed with different low power techniques. The designs are carried out at various nanoscale technology nodes. After evaluating the performance metrics of all these designs, it's observed that the design with sleepy keeper low power technique performs better than all other low power schemes. Five stage ring oscillator design produces the frequency of 1.28 GHz, power =16µW and delay = 0.025p Sec @1V supply. To further increase the frequency, reduce the power and area, in the next chapter will design the Fin-FET based designs.

CHAPTER 4

Fin-FET DESIGN

In this chapter we discussed the importance of Fin-FET devices, types of fin devices, shapes, and operation modes. The modeling procedure and extraction of characteristics of the Fin-FET device has been explained. Finally, an inverter has been implemented with the proposed Fin-FET device.

4.1 INTRODUCTION

The aim of the device scaling is to accommodate a greater number of transistors in a given silicon area and ensure consistent performance. Continuous scaling of a transistor leads to several undesired short channel effects (SCEs), including subthreshold leakages. Subthreshold leakage is the leakages produced in the device when the device is in “off state", which shows strong impact on the battery lifespan. The primary challenge faced by MOSFET is the advancement of scaling below the 45 nm technology. The subthreshold current of a MOSFET is a type of short-channel effect (SCE) that is highly influenced by the scaled magnitude of the threshold voltage. The scaling of MOSFETs has been limited by many constraints related to geometric and process characteristics [55-57]. According to scaling, it is necessary to decrease both the V_{DD} and V_{TH}, reducing the device's overdrive potential due to the exponential relationship between the drain current in the subthreshold region and the overdrive voltage, as depicted in equation (4.1).

$$I_{off} = I_o \exp\left(\frac{V_{GS}-V_{Th}}{n.^{*}V_T}\right) \text{-----(4.1)}$$

Where

‘I_0’ is the reverse current

‘V_T’ is the thermal equivalent voltage

‘n’ is the constant

In the scaled bulk MOSFET, as the source and drain are very near, there was a great loss in scaling benefits because of more leakages dominates. Hence, it is a big challenge to enjoy the scaling benefits in short channel devices (SDCs). Compared to long channel Devices (LCDs), in SCDs, the gate control over the channel is very poor, hence, to improve the control over the channel, the number of gates in the device should be increased. In a scaled device, the scaled threshold voltage will severely damage the performance ofthe device by increasing the static current. Increasing device threshold voltage will do the reverse operation. That is this has a low drive current by lowering the leakage current.

To resolve this problem in scaled devices, it is imperative to have a reliable method of controlling the channel through multiple gate FETs, which outperform single gate devices. New appliances, including the Single Gate MOSFET (SGMOSFET) and Double Gate MOSFET (DGMOSFET) [52], have appeared as the principal alternative for CMOS devices in the nano scale designs due to studies into this static power dissipation. DGMOSFET utilizes two gates placed on opposite sides of the channel to enhance control. One of the key challenges in the fabrication of DG-MOSFETs is the precise alignment of the top gate and back gate. Misalignment between these two gates can lead to uneven electric fields, degraded device performance, and variability in threshold voltage. This misalignment issue arises because the top and bottom gates are typically formed in separate processing steps, which can introduce slight shifts in positioning due to limitations in lithography and layer registration. To overcome this challenge, advanced fabrication techniques like self-aligned gate process, where both the top and bottom gates are defined simultaneously or using a common mask to ensure perfect alignment. And fabricating the device on Silicon-On-Insulator (SOI) substrates, which allows better control over the back gate and simplifies the gate alignment process.

Additionally, newer architectures like Fin-FETs and Gate-All-Around (GAA) FETs inherently provide better gate-channel control and reduce reliance on precise dual-gate alignment, offering a practical solution to this fabrication issue [58].

Fin-FET offer superior gate control over the channel, exhibiting steeper subthreshold characteristics compared to traditional bulk MOSFETs. In Fin-FET, channel is shaped

like a vertical fin, and the gate wraps around three sides, both sidewalls and the top effectively forming a tri-gate structure. This configuration significantly improves the ability of the gate to modulate the channel, reducing leakage currents and improving switching behavior [53]. Gate-All-Around (GAA) Fin-FETs further advance this concept by surrounding the channel entirely with the gate, providing complete electrostatic control. This full gate enclosure minimizes short channel effects and enhances scalability for future technology nodes.

Compared to bulk MOSFETs, which only have gate control on one side of the channel, these multi-gate architectures DGMOSFET, Fin-FET, and GAA Fin-FET represent a major leap in device design, offering much better electrostatic control, improved performance, and reduced power consumption [59].

Fin-FETs are more viable for high-performance and low-power applications in modern semiconductor devices. Also allows higher transistor densities, enabling more transistors to be packed into a smaller areaon a chip. Fin-FET used in CPUs, GPUs, and memory chips where energy efficiency and processing speed are critical.

The Fin-FET introduction is discussed in section 1.7.1. One of the significant advantages of Fin-FETs is their ability to decrease leakage currentwhen the transistor is in the off state. This is because the gate wraps around the fin, effectively shutting off the transistor when not in use, which helps conserve power.

4.2 Fin-FET STRUCTURE

Fin-FET is a non-planar, tri gate switching device and Fin-FET stands for “Fin” shape Field Effect Transistor. In Fin-FET, thin gate oxide is sandwiched between the silicon fin structure and gate electrodes i.e the gates are surrounded by the channel. Unlike traditional planar transistors, Fin-FETs have a three-dimensional structure as shown in figure 4.1. Fin-FET has vertical channel whereas MOSFET has horizontal channel. In Fin-FETs, the fin height plays a role similar to the channel width in traditional MOSFETs, serving as a critical parameter that greatly influences the device’s electrical performance and overall characteristics. Increasing the number of fins in Fin-FETs leads to a higher charge density within the channels, which allows for more precise gate control and, in turn, improves the

overall performance of the device [60-63].

This particular structure offers improved screening from the source due to its proximity to the channel. As a result, it effectively reduces SCEs suchas DIBL) and subthreshold leakage. Better Electrostatic Control, Lower Power Consumption, Reduced Short-Channel Effects, Better Performance, Scalability and Compatibility with Advanced Manufacturing Processes are the benefits of Fin device.

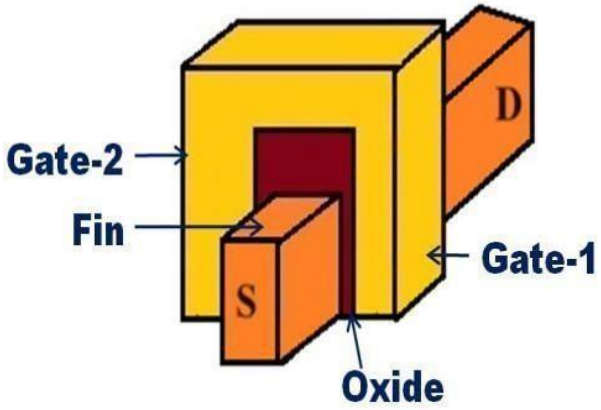


Figure 4.1: Basic structure of Fin-FET [65].

However, it is important to recognize that practical manufacturing limitations and performance considerations require Fin-FETs to have relatively small fin heights. Excessively tall fins can lead to instability in device operation. To ensure stable and reliable performance, engineering best practices recommend keeping the fin height to less than four times the fin thickness. Additionally, the effective channel width of a Fin-FET can be determined by multiplying the number of fins by the height of each individual fin. This simple relationship is crucial in optimizing and fine-tuning the device's electrical characteristics [67-69].

4.2.1 Classification of Fin-FET structures

FinFETs can be categorized into different aspects, which are as follows [70-71].

a) Based on physical structures

b) Based on no.of terminals

c) Based on dielectric thickness

Based on physical structure: Bulk Fin-FETs and SOI (Silicon-On-Insulator) Fin-FETs are two distinct types of FinFET architecture, each with unique structural and characteristics. In Bulk Fin-FETs, the fins are formed on a shared silicon substrate, resulting in physical connectivity between them. In contrast, SOI Fin-FET fins are electrically and physically isolated from the substrate by an insulating layer, eliminating direct contact. This structural difference is illustrated in figure 4.2. Bulk Fin-FET is the best option for many semiconductor companies because of ease of integration into existing fabrication processes. Whereas SOI Fin-FET offers reduced junction capacitance, higher I_{ON}/I_{OFF} ratio and lower SCEs.

Choice between Bulk and SOI Fin-FETs involves trade-offs between manufacturing cost, performance, and design complexity. Ultimately, selecting the appropriate FinFET type depends on a careful evaluation of these factors in relation to specific application requirements.

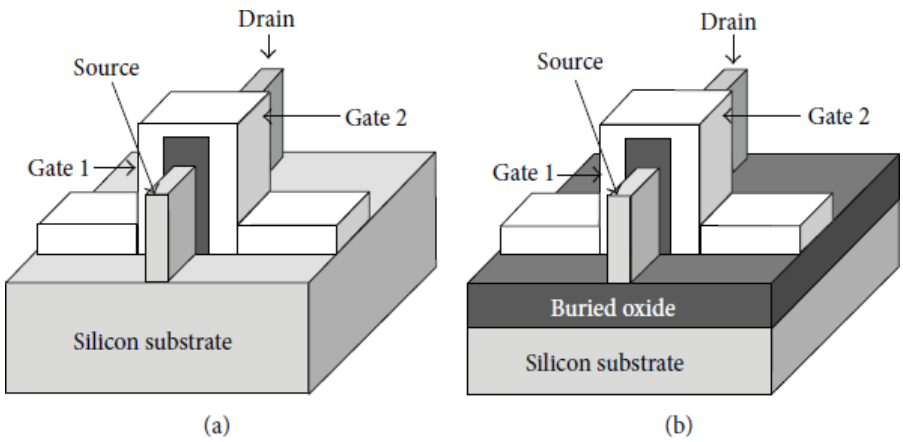


Figure 4.2: Comparisons of structures (a) Bulk Fin FET (b) SOI FinFET device [74]

Based on gate connections: Fin-FET can be broadly classified into two main types based on the number of terminals: Short-Gate (SG) Fin-FET (SGF) and Independent-Gate (IG) Fin-FET(IGF). SG Fin-FET has three terminals, while IG Fin-FET has four. The fundamental difference between these two lies in their structural

configuration. In SG Fin-FET, the two gates are electrically shorted and physically connected, functioning as a single gate.

In contrast, IG Fin-FET have two gates that are physically separated by a dielectric material, allowing them to operate independently. Figure 4.3 a and b illustrates the structural distinctions between SG and IG Fin-FETs. The total number of terminals in IGF is four, source, drain, gate 1 and gate 2 and the number of terminals in SGF is three, sources, drain and two gates.

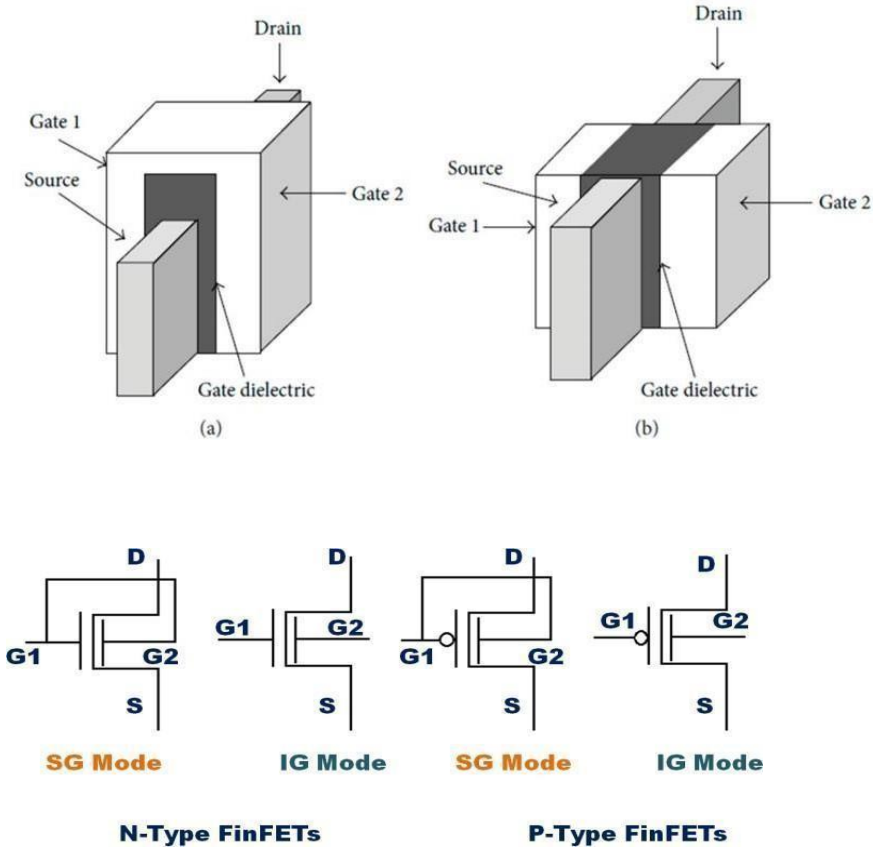


Figure 4.3: Structure schematic of (a) SG FinFET and (b) IG FinFET
(c) N-Type and P-Type SGF and IGF Symbols.

SGF offers higher ON current (ION) and OFF current (IOFF) hence fits for high-speed operation but may lead to increased leakage. IGF offers more precise tuning of the device electrical characteristics, but it also introduces additional complexity in the fabrication process. Notably, IG FinFETs can achieve a better Ion/Ioff ratio by

dynamically adjusting one gate's voltage through the influence of the other. As a result, IG FinFETs are particularly well-suited for power management applications, where energy efficiency and fine control are critical.

n-channel and p-channel devices of SGF and IGF configurations are illustrated in figure 4.3 (c). Based on work functions, the SGF devices are further classified into symmetric SGF and asymmetric SGF configuration. If the work function is the same for both the gates, then it is symmetric SGF (SSGF) and if both the gates work functions are different, it is called asymmetric SGF(ASGF).

Based on dielectric thickness: Fin-FET can also be categorized based on the dielectric thickness into Double-Gate (DG) Fin-FET and Tri-Gate Fin-FET. In DG Fin-FET, a hard mask is applied on top of the transistor structure, which limits gate coverage to the two sidewalls of the fin. Fin is defined with fin height ($Hfin$), fin width ($Wfin$), and number of fins (n). As a result, the effective channel width is defined as (2n× Hfin), making DG Fin-FETs functionally like split transistors. Tri-Gate Fin-FETs, on the other hand, utilize a thinner dielectric layer that allows the gate to cover not only the sidewalls but also the top surface of the fin. This structural enhancement increases the effective channel width to (2n×Hfin +Wfin).

This expanded gate control area contributes to a reduced gate-to-source capacitance, leading to improved switching performance and energy efficiency in certain applications. Despite the added gate surface, tri-gate Fin-FET maintain strong electrostatic integrity, making them a highly effective design choice. The total effective channel width in tri-gate Fin-FET can therefore be seen as the equivalent of a DG FinFET's channel width plus the top surface width of the fin, providing both enhanced drive strength and better overall device performance [88-90].

4.3. Fin-FET Challenges

Transition from planar to Fin-FET technology introduces several challenges. These include corner effects and increase parasitic capacitance, as well as fabrication complexities like precise control of channel doping concentration, silicon surface

irregularities, and fin oxidation. Each of these issues can significantly affect device performance and reliability, highlighting the need for careful engineering solutions.

To address these challenges, a strategy has been developed such as advanced simulation techniques and optimized fin geometries help mitigate corner effects and parasitic capacitance. Meanwhile, improvements in doping techniques and surface treatment processes enhance channel uniformity and reduce variability. Additionally, controlled oxidation methods are employed to maintain the structural integrity and electrical characteristics of the fins.

Fin-FET exhibits a higher degree of parasitic capacitance compared to traditional planar MOSFET. This is because Fin-FET is a 3D structure where the gate wraps around the fin-shaped channel on multiple sides i.e the two vertical sidewalls and the top. This wrap-around design increases the gate-to-channel interface area, and in some configurations, especially in double-gate or closely packed fins, there's also greater interaction between the front and back gates. These factors contribute to the rise in parasitic capacitances, which can negatively impact switching speed and power efficiency. Increasing fin height and reducing fin pitch are the two solutions for this issue.

In Fin-FET, the solution for SCEs (like threshold voltage roll-off and drain-induced barrier lowering) is the decrease of fin width. As the fin becomes narrower, the resistance in the source and drain regions increases significantly. This degrades the drive current and transconductance. As the fin narrows and sharp corners are formed at the edges, a phenomenon called the “corner effect” arises. Where a higher electric field concentrates at the fin corners, making these regions more susceptible to subthreshold leakage i.e even when the transistor is 'off', a current can still leak through these corner regions.

4.4 Fin-FET OPERATION

In all Fin-FET variants, the fundamental operating principle is the field effect. This means that the flow of drain current is regulated by a gate electrode, which, despite not making direct contact with the silicon substrate, controls the channel through an electric field. Specifically, a transverse electric field generated across the gate oxide modulates the conductivity of the fin beneath it. The gate material may consist of heavily doped or silicide polysilicon with a silicon dioxide (SiO_2) dielectric, or it may use a high-k metal gate (HKMG) stack, featuring refractory metals such as tungsten (W), titanium (Ti), molybdenum (Mo), or their alloys.

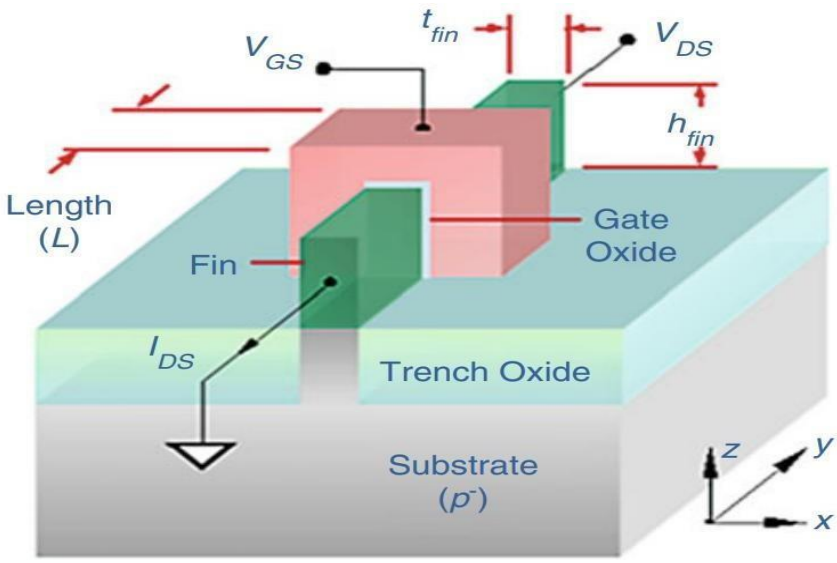


Figure 4.4: Fin-FET geometry [50]

A rectangular Fin-FET is geometry is shown in figure 4.4, Current flow in the Fin-FET depends on two voltages, gate to source voltage (V_{GS}) and drain to source voltage (V_{DS}). With the application of voltage between gate to source, a transverse electric field produced in the gate dielectric, this transverse electric field modifies the conductivity of the fin and acts as the channel for the current. When the gate voltage is greater than threshold voltage, it creates a conducting path in the fin. Once the channel is formed, applying a voltage V_{DS} causes carriers to flow through the channel. Higher the V_{DS} increases the electric field along the channel, which in turn increases the current.

4.5 Fin-FET CHARACTERISTICS

Device subthreshold characteristics are crucial to evaluating the speed and the power of the device. Low voltage-high speed electronic circuits require a device with significantly sharper I-V characteristics in its subthreshold region. A proper biasing technique is required to operate the device at low voltages in the subthreshold region. The device performance can be measured by evaluating the sub-threshold slope (SS), I_{ON}, and I_{OFF}, which are the design parameters. Subthreshold slope (SS) refers to the minimum change in the applied gate voltage needed to cause a tenfold rise in the drain current.

Figure 4.5 displays a log-linear plot demonstrating the linear relationship between the drain current in the subthreshold area and the subthreshold slope (SS). The desired subthreshold swing (SS) value for a MOSFET at average temperature is 60mV/dec, while, in practice, it is typically around 72mV/dec. The ideal choice is for applications requiring high-speed performance, a device with a subthreshold slope (SS) value of less than 60mV/dec. A low SS value indicates a fast speed; conversely, a high SS number indicates a low speed. SS or switching speed, is a metric used to evaluate the performance of a device. It quantifies the speed at which transitions occur between the two states ON and OFF states.

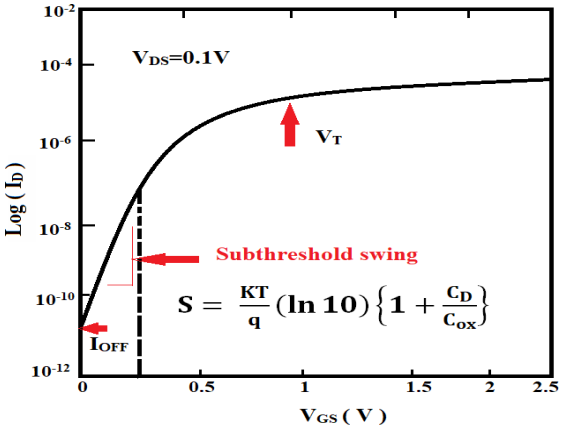


Figure 4.5: Log-Linear Input characteristics of MOSFET

To measure the subthreshold slope of the device, equation (4.2) used.

$$SS = \ln(10)\left(\frac{KT}{q}\right)\left(1 + \left(\frac{C_d}{C_{ox}}\right)\right) \text{ ------ (4.2)}$$

Where, 'C_d' is the device depletion capacitance, C_{ox} is the oxide capacitance in the device. KT/q is the thermally equivalent voltage ≈ 26mV@ room temperature 300^0K. To measure the ideal slope value in the MOSFET, assume Cd≈0 and C_{ox}≈∞ and ln (10) ≈ 2.3. The equation (4.2) is approximated as $SS \approx 2.3 * 26 \frac{mV}{dec} = 59.8mV/dec.$

It is convenient to define the x-y-z coordinate system with the origin at the lower right corner of the structure. The silicon fin, with a thickness W_{fin}, plays a critical role in device behavior. To derive the I-V characteristics of a Fin-FET operating in the inversion mode (i.e., when $V_{GS} > V_{th}$ for an n-type device), focus on the charge behavior in the channel. In this condition, a positive voltage applied to the gate induces a positive charge on the gate electrode. This is balanced by an equal and opposite negative charge in the silicon fin beneath the gate. The total negative charge per unit area on the fin (Qfin) is composed of two distinct components: depletion charge (Qd) and inversion layer charge (Qi). Then the total charge of the fin is in equation (4.3)

$$Q_{fin} = Q_d + Q_i \text{--------} (4.3)$$

Assume that the $V_{DS} < V_{DD}$. This allows us to treat the charge densities as uniform along the y-direction (i.e., from source at y = 0 to drain at y = L), as no significant variation occurs in the channel. Part of the applied gate voltage is dropped between the surface of the fin and its interior, and this is described by the surface potential (Φs). The gate voltage can therefore be related to the surface charge using the oxide capacitance per unit area (Cox) as in equation (4.4).

$$V_{GS} = \frac{-Q_{fin}}{C_{ox}} = \Phi_s \text{------} (4.4)$$

For a uniform channel, it is reasonable to assume that the surface potential (Φs) remains constant along the y-direction, meaning it does not vary from source to drain. In this analysis, we neglect non-ideal effects, such as trapped charges in the oxide layer or at the fin–oxide interface.

Therefore, the entire charge in the fin is assumed to be solely induced by the gate bias. By rewriting the above equation (4.4) and substituting in equation (4.3), we can get equation (4.5).

$$-Q_i = C_{ox}[V_{GS} - \Phi_s] + Q_d = C_{ox}[V_{GS} - (\Phi_s - \frac{Q_d}{C_{ox}})] \text{ --- (4.5)}$$

Once inversion is reached, assume that the surface potential (Φs) remains relatively constant even as V_{GS} continues to increase. At the threshold voltage of an n-type transistor, the Qi is considered to be zero. Then the above equation (4.5) is written as

$$V_{Th} = \Phi_s - \frac{Q_d}{C_{ox}} \text{---------(4.6)}$$

Now substitute the equation (4.6) in the inversion charge equation (4.5), we can get as equation (4.7).

$$-Q_i = C_{ox}[V_{GS} - V_{Th}] \text{ --- (4.7)}$$

As V_{GS} increases further, above threshold, more negative charge must appear on the fin and Qi, grows exponentially with gate bias, flooding the fin with mobile electrons. The inversion electrons in the channel is mobile carriers. When a small V_{DS} is applied, these electrons begin to drift along the channel from the source to the drain in a linear manner. The average drift velocity of these electrons moving through the silicon lattice is directly proportional to the applied electric field. The constant of proportionality is μn, known as the electron mobility.

$$\bar{v}_y = -\mu_n E_y \text{------ (4.8)}$$

A negative sign in equation (4.8) indicates the electrons move in the direction opposite to the electric field. On average, the electrons drift from source to the drain over a certain time interval (τ). This transit time is calculated by dividing the channel length by the average drift velocity of the electrons as in equation (4.9).

$$\tau = \frac{L}{\mu_n |E_y|} = \frac{L^2}{\mu_n V_{DS}} \text{ ----- (4.9)}$$

The total mobile inversion charge distributed across all three surfaces of the fin within this small elemental volume is given by the equation (4.10).

$$dq = Q_i(2H_{fin} + W_{fin})dy \text{------ (4.10)}$$

We know the current is the rate at which charges are moved, therefore divide the equation (4.10) with time, got equation (4.11).

$$I = \frac{dq}{dt} = \frac{Q_i(2H_{fin}+W_{fin})dy}{dt} = Q_i(2H_{fin} + W_{fin})\bar{v}_y \text{------(4.11)}$$

Substitute the equation (4.8) in equation (4.11), we get the equation (4.12)

$$I = \mu_n (2H_{fin} + W_{fin}) Q_i \frac{dV_y}{dy} \quad (4.12)$$

Substitute equation (4.7), will get equation (4.13)

$$I = \mu_n C_{ox}[V_{GS} - V_{Th} - V(y)](2H_{fin} + W_{fin}) \frac{av_y}{dy} \quad (4.13)$$

To solve the above differential Eq. (4.13), integrate over the entire length of the channel, from 0 to L. And achieve current equation as in (4.14)

$$\int_0^L I\, dy = \mu_n C_{ox}(2H_{fin} + W_{fin}) \int_0^L [V_{GS} - V_{Th} - V(y)]dV$$

$$I = \mu_n C_{ox} \frac{(2H_{fin}+W_{fin})}{L} [(V_{GS} - V_{Th})V_{DS} - \frac{1}{2} V_{DS}^2] \quad (4.14)$$

4.6 Fin-FET DESIGN

In this thesis, the Verilog-A language is used to model both n-type and p-type FinFET. Verilog-A is a hardware description language specifically designed for analog circuit modeling. It allows us to simulate the electrical behavior of semiconductor devices like Fin-FEs by defining their characteristics and equations in a compact and reusable form. By using Verilog-A, it creates custom FinFET models that can be used in circuit simulators (such as SPICE or Cadence), enabling accurate analysis of device performance in both digital and analog applications. This enables the model developers to focus solely on developing precise current and charge models without dealing with the complex mathematical details of deriving and implementing the derivatives of currents and charges. Using the Hierarchy editor, the Verilog A language uses transistor-level and parasitic removed circuit views to enable system-level modelling. This method is highly effective for verifying complex designs. A language construct is similar to digital Verilog RTL, albeit with several differences. Verilog A code for Fin-FET is shown in Appendix.

4.6.1 Fin-FET implementation and characterization

Fin dimensions and fin shape play a significant role in channel control, for better channel control, a combination of fin and a lightly doped channel together should be considered.

Device performance depends on the $Wfin$ and $Hfin$, this can be explained by the following analysis.

In double gate FET, the effective channel width

$$W_{eff} = 2H_{fin} \quad (4.15)$$

In FinFET, the effective channel width

$$W_{eff} = 2H_{fin} + W_{fin} \quad (4.16)$$

In multiple fin structured FinFET, the effective channel width,

$$W_{eff} = n\,(2H_{fin} + W_{fin}) \quad (4.17)$$

The effective channel length in the above devices,

$$L_{eff} = L_{gate} + 2L_{ext} \quad (4.18)$$

Where, L_{gate} is the gate length covered by the fin and $L_{ext}$is the fin length on two sides joining the source and drain. Here, to investigate the device performance H_{fin} should be kept constant at a particular value and sweep the W_{fin} from 4nm to 20nm.

From equation 4.17, it's understood that for larger fin width there is an enlarged gate width. When gate length scaled, there should be corresponding scaling in the W_{fin} to maintain an efficientsuppression of SCEs.

Specification of Fin-FET: Here, the specifications for the SG Fin-FET considered as, the gate length, L_{gate}= 20 nm, tox = 2.4 nm, H_{fin}= 10 nm to 40 nm, W_{fin}= 4 to 20 nm, fin pitch =29 nm based on ITRS 10 nm technology node, drain to source voltage, V_{DS}=0.8V, work function = 4.39 eV, source-drain-channel doping range is $10^{16}/cm^3$to$10^{19}/cm^3$.

Fin-FET I-V characteristics, transconductance (g_m), and threshold voltage variations with respect to the H_{fin} and W_{fin}variation is observed and explained in the following.

i) Impact of number of fins on device Drain Current (I_{DS}):

From the equation 4.17, as the number of fins increases, the effective channel width, $Weff$ of the Fin-FET increases. The current in Fin-FET is directly proportional to the $Weff$ as in equation (4.14), the current increases as the number of the number of fins increases in both the devices.

Table 4.1: pFET and nFET drain currents with respect to the no. of fins varies from 1-8 for W_{fin}=H_{fin}@10nm

nFin-FET				PFin-FET			
W_{fin} (nm)	**H_{fin} (nm)**	**NFin (n)**	**Current (nA)**	W_{fin} (nm)	H_{fin} (nm)	**NFin (n)**	**Current (nA)**
10	10.00	1	77.13	10.00	10.00	2	76.21
10	10.00	2	154.2	10.00	10.00	4	152.3
10	10.00	3	231.2	10.00	10.00	6	228.5
10	10.00	4	308.3	10.00	07.00	8	304.6

The Impact of number of fins of the Fin-FET on the device current is studied by keeping the fin height and fin width at 10 nm and increasing the number of fins (n) from 1 to 8, fix the drain to source potential (V_{DS}) at 1V, and gate to source potential (V_{GS}) varies from 0V to 0.8V. Observe the drain current in both pFin-FET and nFin-FET devices and the values are tabulated in table 4.1.

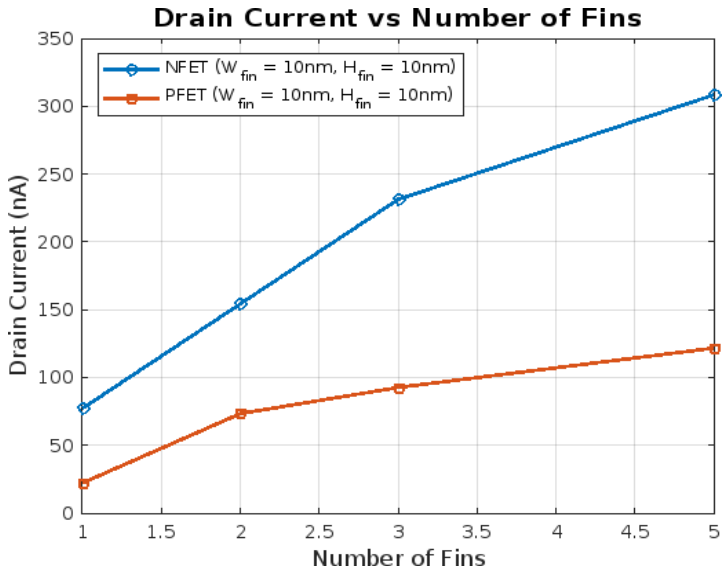


Figure 4.6: Drain current Vs number of fins at $Wfin = Hfin$ @10nm **(a)** nFin-FET **(b)** pFin-FET.

The graphs for the values in table 4.1 are presentedin figure 4.6. They show the trend of drain current with respect to the number of fins increases. From the figures, it is observed that the current in both the devices increases as the number off in increases, but the incremental currents are somehow more in n Fin-FET.

ii) Impact fin height on the device drain current (I_{DS})

From the equation 4.17, it isobserved that as the fin height increases, the effective channel width ($Weff$) of the device increases. Since the device drain current is directly proportional to the $Weff$. The drain current increases as the fin height increases in both pFin-FET and nFin-FET.

To know the impact of fin height on the current device, fix the fin width value at a value of 10 nm and vary the fin height from 10 nm to 40 nm. The biasing values are kept as in the above case. The drain current readings of both the Fin-FETs for the different fin heights are presented in table 4.2. For the readings in table 4.2, the graphs for the values are shown in figure 4.6. It is observed that, as the fin height ($Hfin$) increases, the drain current in both n-type and p- type Fin-FETs increases proportionally.

Table 4.2: Drain current of both the Fin-FETs at$Wfin$ @10nm, with changing $Hfin$ from 10nm to 40nm.

nFin-FET				PFin-FET			
W_{fin} (nm)	H_{fin} (nm)	NFin (n)	Current (nA)	W_{fin} (nm)	H_{fin} (nm)	NFin (n)	Current (nA)
17.00	10.00	1	82.25	17.00	10.00	2	90.54
20.00	10.00	1	239.8	34.00	10.00	2	239.8
25.00	10.00	1	302.4	35.00	10.00	2	302.6
28.00	10.00	1	521.4	38.00	10.00	2	521.4

The graphs for the values in table 4.2 are presentedin figure 4.7. They show the trend of drain current with respect to the fin height increase. From the figures, it is observed that the current in both the devices increases as the fin height increases, but the incremental currents are somehow more in nFET.

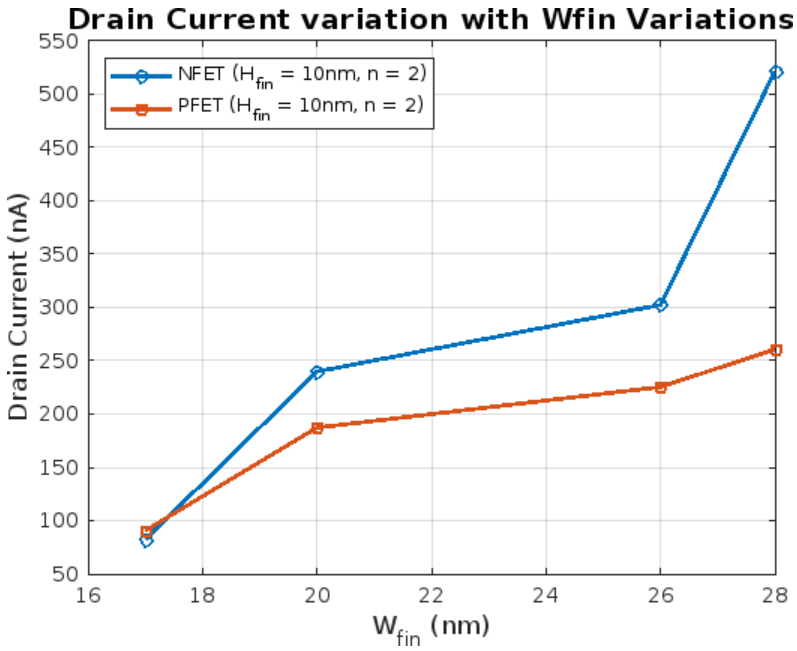


Figure 4.7: Drain current of both the Fin-FETs at$Wfin$ @10nm, with changing $Hfin$ from 10nm to 40nm.

iii) Impact of fin width on the device drain current (I_{DS}):

From the equation 4.17, it is observed that the effective channel width ($Weff$) of the device increases as the fin width increases. Since the device drain current (I_{DS}) is directly proportional to $Weff$, thedrain current also increases proportionally.

To know the impact of fin width on the device current, fix the fin width at a value of 10nm, fix number of fins to one and vary the fin height from 10 nm to 40 nm. The biasedvalues are kept as in the above case. The drain current readings of both the Fin-FETs forthe different fin heights are presented in table 4.3.

Table 4.3: Drain currents of both the Fin-FETs at n=1, $Hfin = 10\ nm$, $Wfin$ changing from 10 nm to 40 nm.

nFin-FET				PFin-FET			
W_{fin} (nm)	H_{fin} (nm)	NFin (n)	Current (nA)	W_{fin} (nm)	H_{fin} (nm)	NFin (n)	Current (nA)
10.00	10.00	1	83.47	10.00	10.00	2	88.76
10.00	20.00	1	278.5	10.00	30.00	2	286.3
10.00	30.00	1	524.1	10.00	50.00	2	535.1
10.00	40.00	1	760.6	10.00	60.00	2	774.9

For the readings in table 4.3, the graphs for those values are shown in figure 4.8. From these graphs, it is observed that, as the width of the fin, W_{fin} increases, the drain current of both n-type and p-type Fin-FETs increases proportionally. When the fin width increases, the cross-sectional area of the channel through which current flows also increase.

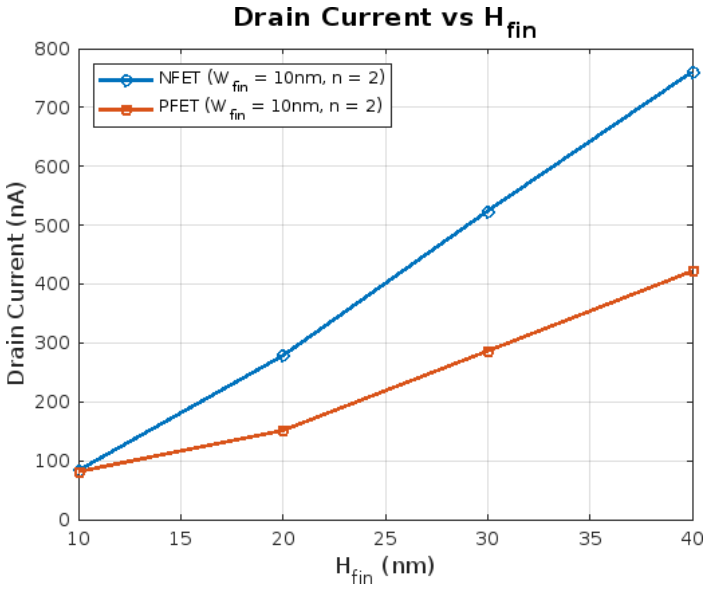


Figure 4.8: Drain current of n-type and p-type Fin-FET varying TFIN.

iv) Impact of gate length on Drain current (I_{DS}):

Substitute the equations 4.5 and 4.6 in the equation 4.14. then the effective channel is closely related to the gate length covered by thefin $Lgate$ and fin length on two sides joining the source and drain $Lext$. And the drain current is reciprocal to the $Leff$, as the gate length increases, the current reduces as show in the graph presented in figure 4.9.

$$I_{DS} = \mu_n C_{ox} \frac{W_{eff}}{L_{eff}} [(V_{GS} - V_{Th})V_{DS} - \frac{V_{DS}^2}{2}] \text{----- (4.19)}$$

To conduct this experiment, keep $Wfin$ = 20 nm, $Hfin$ =10 nm and V_{DS} = 1V. I_{DS} is measured by swapping the V_{GS} from 0V to 0.8V, this is repeated for different gate lengths, $Lgate$= 5 nm to 20 nm. For $Lgate$=20 nm produces off current = 8 nA @ V_{GS}=0Vwhich is called Ioff, and the Ion =10^{-5}A is registered @ V_{GS}=0.3V. Similarly, for $Lgate$ = 5 nm produces off current=10^{-5}A @V_{GS}= 0V which is called off state current, and the on-state current=8 µA registered @V_{GS}= 0.3V.

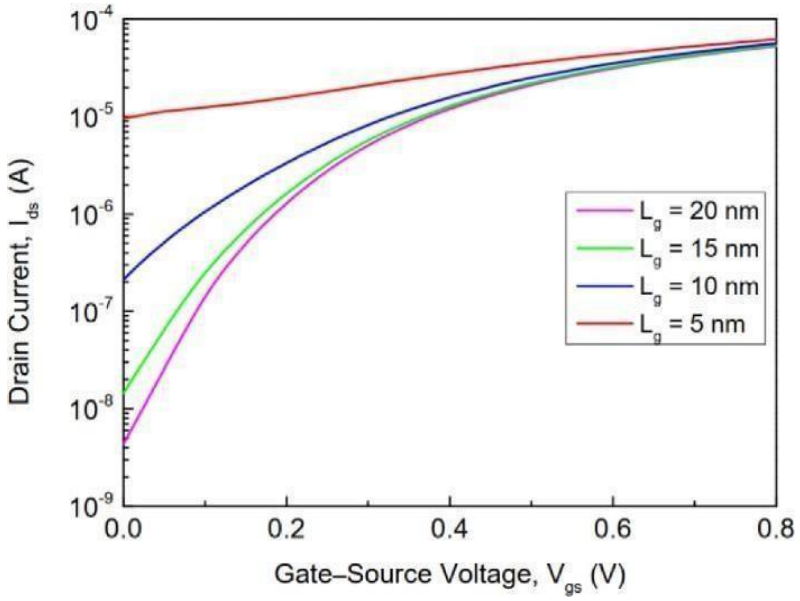


Figure 4.9: Fin-FET transfer characteristics

Figure 4.10 shows how drain current (I_D) changes with respect to gate length in a FinFET device. When the gate length is small, the drain current is high. As the gate length increases, the drain current decreases. This is because a shorter channel (gate length) allows electrons to travel a shorter distance, resulting in less resistance and higher current flow. The off current, also increases with smaller gate lengths because the gate loses some control over the channel, leading to higher leakage.

v) Impact of Fin width on Drain current (I_{DS}) and transconductance(g_m):

Larger the fin width in Fin-FET, larger the drain current (I_{DS}) and the transconductance (g_m) [9]. From the current equation in (4.14), it is observed that the current is proportional to the fin width. To investigate the optimum fin width, experiment was conducted with fixing the V_{DS} =1V, $Hfin$=10 nm and vary the V_{GS} from 0V to 0.8V. For different $Wfin$ values from 4 nm to 20 nm. The remaining parameters of the devices are considered as above derived.

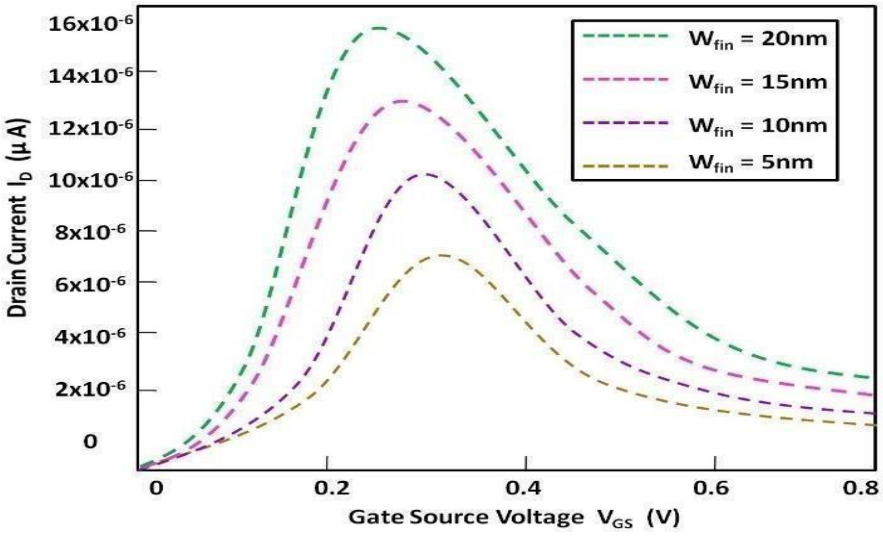


Figure 4.10: Impact of $Wfin$ on I_{DS} and gm.

Graph which shows the impact of Fin width on I_{DS} and gm is presented in figure 4.10. From the graph it is understood that as the fin is wider, the current increases because more surface area is for the current to flow. This directly influences the electrical performance of the device.

From the graph it is observed that for $W_{fin} = 20\ nm$, the device produces low off current=1 nA@ V_{GS}=0V and high on state current=1.5x10^{-5}A @ V_{GS}=0.3V. The better transconductance is obtained as 3x10^{-5}S @$Wfin = 20\ nm$.

vi) Impact of Gate length on device cutoff frequency:

Cutoff frequency of the device is defined as the frequency at which the drain and gate currents are equal, thereby its current gain is unity. In other words, it defines the maximum frequency at which the transistor can operate effectively as an amplifier. Mathematically as in equation (4.20).

$$f_T = \frac{g_m}{2\pi(C_{GS}+C_{GD})} \text{----------} (4.20)$$

Where,

f_T is the unity gain frequency,

C_{GS} and C_{GD} are the diffusion capacitances.

Fin-FET with shorter gate length can operate at higher frequencies. Reducing the gate length decreases channel resistance and improves carrier velocity. This increases the transconductance and can reduce gate capacitance, both of which push f_T higher.

To know the impact of gate length on the Fin-FET cutoff frequency, the experiment was conducted by fixing the W_{fin} = 20 nm, H_{fin}=10 nm, and V_{DS} =1V, and the cutoff frequency is measured by swapping V_{GS} from 0V to 0.8V. This is repeated for different L_{gate}, from 5 nm to 20 nm. The impact of L_{gate} on device cutoff frequency is presented in the figure 4.11. The higher cutoff frequency is reported as 6.1x1012@ V_{GS}=0.33V and L_{gate}=10 nm. Because longer gate length increases the carrier transit time and capacitance, hence the gm decreases thereby lower cutoff frequency.

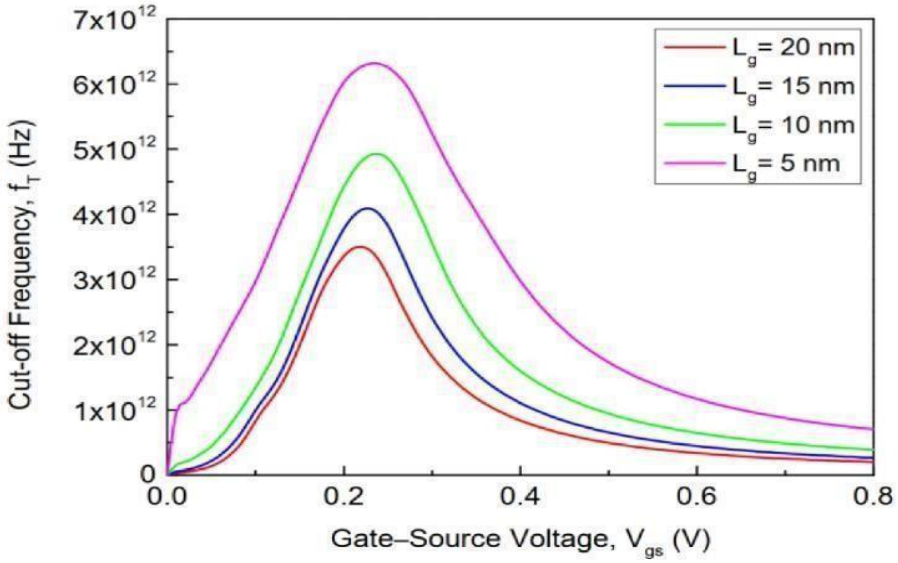


Figure 4.11: FinFET cutoff frequency as a function of VGS

vii) Impact of Fin height on Device Threshold Voltage:

The threshold voltage of Fin-FET depends on many process parameters and is measured with equation 4.21.

$$V_{th} = V_{FB} - \left(\frac{1}{(1-(A_1 - A_2))}\right) * A_1(V_{Bi} + V_D) + A_2 V_{Bi} - V_T \, ln\left[\frac{Q_{th} N_A}{n_i^2 H_{fin}}\right] \text{-----(4.21)}$$

Where, V_{FB} flat band voltage, V_{Bi} built in potential, N_A acceptor concentration, V_D is the drain potential and V_T is the temperature equivalent voltage.

$$A_1 = \frac{2H_{fin}\gamma_{11} + W_{fin}\gamma_{12}}{W_{fin} + 2H_{fin}} \quad \text{and } A_2 = \frac{2H_{fin}\gamma_{21} + W_{fin}\gamma_{22}}{W_{fin} + 2H_{fin}}$$

From the equation 4.21, it is observed that the device threshold voltage reduces with the corresponding increase in the $Wfin$. The influence of fin dimensions on device threshold voltage (Vth) is clearly shown in the graph in figure 4.12. Experiments conducted with fixing the V_{DS} =1V and V_{GS}= 0.35V. And sweeps the $Hfin$ from10 nm to 40 nm.

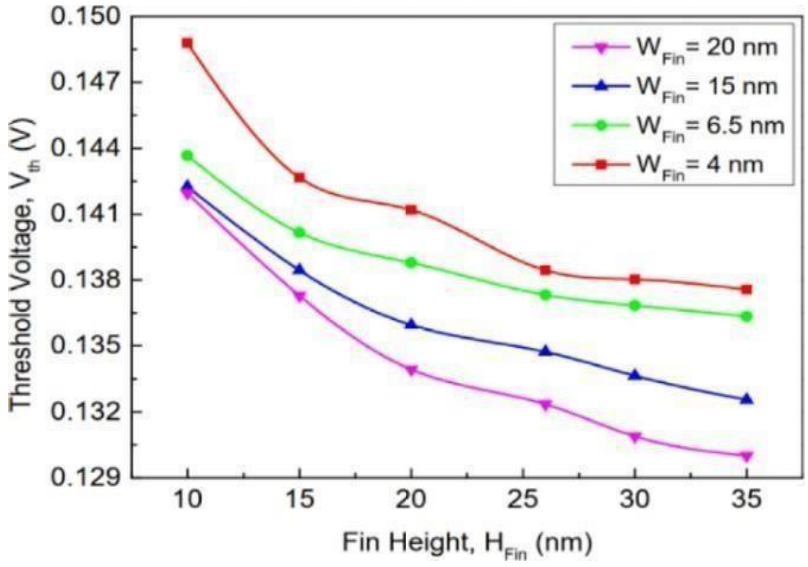


Figure 4. 12: Impact of Fin height on Threshold Voltage

Each curve in the graph represents the trend for different fin widths such as 4 nm, 6.5 nm, 15 nm and 20 nm. From the graph it is understood that the V_{th} falls as the riseof fin height. At the same time the threshold voltage holds a good lower fin width. Finaly, concluded as the optimum fin dimensions for better threshold considered as $W_{fin} = 20\ nm$ and H_{fin}=10 nm. Once both the Fin-FETs have been determined with the characteristics required, the next step is the implementation of the inverter circuit.

4.7 Fin-FET INVERTER

The relationship between the input and output of the inverter is complementary. There is a transition region between the high and low states of the output where both transistors are partially conducting. This region is critical for proper signal propagation and ensures that the inverter operates within its specified voltage and current limits. The noise margin of the inverter represents its tolerance to noise or variations in the input voltage. Basic inverter has been explained in sections 1 and 3. In the basic inverter, NMOS and PMOS devices are replaced with PFin-FET and NFin-FET respectively. As in the case of basic inverters, one Fin-FET acts as pull-up device and the other acts as a pull-down device. PFin-FET is the pull up device, when the signal (Vin) is low '0', it would be turned on and creates a path to V_{DD}. Hence, it pulls the output (Vout) to a high voltage V_{DD}, therefore the output is high [64-66].

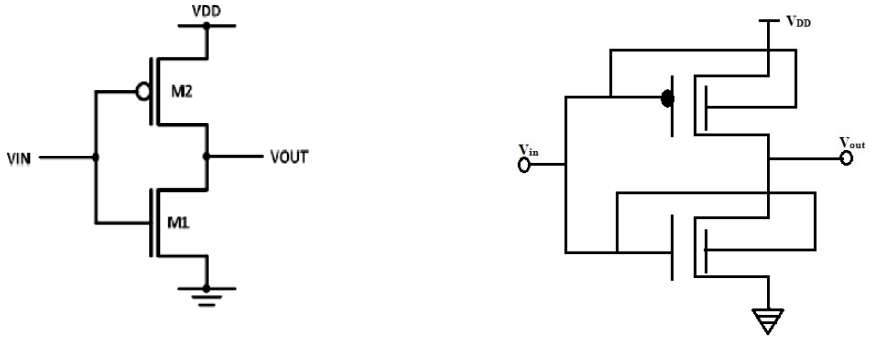


Figure 4.13: Inverter circuits (a) Basic circuit (b) Fin-FET based.

NFin-FET is the pull-down transistor, when the input signal (Vin) is high '1', this will turn on and create a path to the ground. Therefor it pulls the output (Vout) to a low voltage '0'. Fin-FET inverter circuit is shown in figure 4.13.

4.7.1 SG-Fin-FET INVERTER DESIGN

Symmetrical SG-Fin-FET devices which are based on the surface potential model have been implemented. The parameters both geometrical and process related have been considered as

Silicon thickness=6 nm,

tox= 1.5 nm, Leff=18nm,

Weff= 40nm,

μ_n =300 cm^2/Vs.

And consider various bias conditions, the surface potential, drain current, terminal charges, capacitances are characterized. Initially the work started with the modeling of nFin-FET and pFin-FET in Verilog A andverified its characteristics. The Inverter has been designed with the nFin-FET and pFin-FET and operated in SG mode. The schematic is shown in figure 4.14. Independent gatemode can provide threshold voltage modulation which can be used to various innovativedesign circuits.

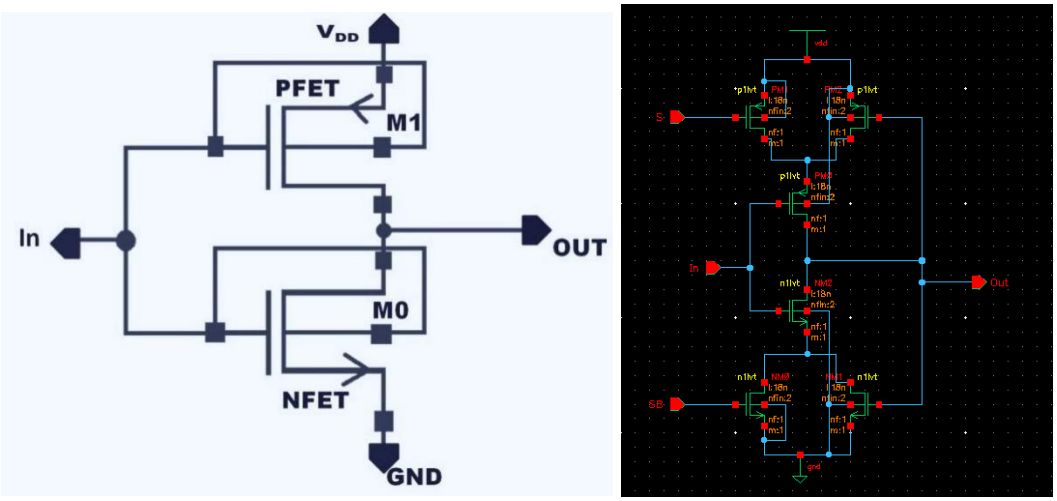


Figure 4.14: Fin-FET based Inverters: (a) basic (b) sleepy stack.

For an inverter, we can do three different types of analysis in the cadence environment; they are Transient analysis, AC analysis and DC analysis. DC analysis generates the steady state behavior of the circuit, similarly AC analysis generates small signal frequency behavior of the circuit, and the transient analysis generates the circuit performance over a period. The cells are made to get the best balance of delay, energy, and power in both planar and non-planar transistors.

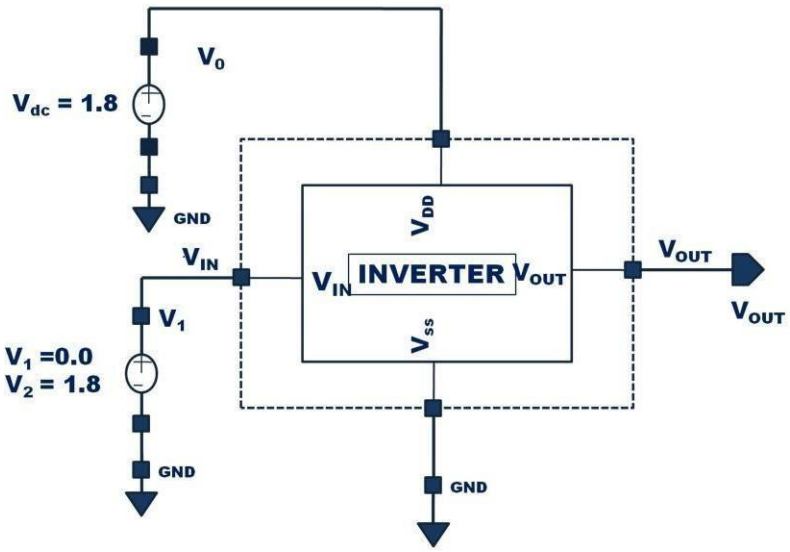


Figure 4.15: Inverter test circuit.

Transient analysis: Here, we performed transient analysis for the inverter by choosing 'tran' icon in the ADE environment. Apply a pulse at the input with setting the following parameters, such as V_{DC}=1.7V, delay time, rise time, fall time, pulse width, period and stop time values and the simulation results for 18 nm technology nodes are shown in figure 4.16.

DC power dissipation (P_{DC}) is measured as: $P_{DC} = V_{DD}I_{DC}$

Depending on the precise amounts of input and output voltage, the inverter may establish I_DC at a variable location. If the input voltage level is linked to logic "0" for half of the time the circuit is working and logic "1"for the other half, then.

$$P_{DC} = 2(I_{DC}V_{IN}(low) + I_{DC}V_{IN}(high))$$

It could be used to estimate how much DC power the course uses. Another term of powerdissipation can be included switching power dissipation; it's the dynamic power dissipation parameter. It can be expressed as average power dissipation.

The analysis focused on four performance metrics: energy-delay product (EDP), power delay product (PDP), average power and propagation delay. The standard calculated in the inverter of CMOS, HCMOS, and Fin-FET technology. A PDP determines how much energy is used on average for each change event. The EDPis another important statistic that makes it possible to measure both efficiency and energy. Here are the

equations for PDP and EDP:

PDP [J] = Average Power Loss ÷ Propagation Delay,

EDP [Js] = PDP × Propagation Delay.

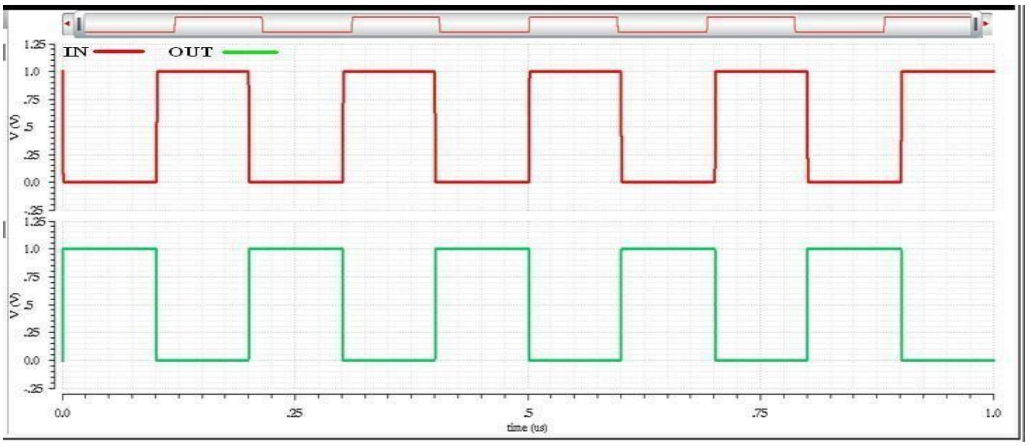


Figure 4.16: 18 nm Fin-FET based Inverter output.

From the results, it is observed that the rise time = 1nsec, fall time=1nsec, period= 200ns, hence the delay is 7ps, and the average power as 1.474 nw. the transmission delay as 1.339 ps from the pattern above. For the leakage current is 828pA (where for a bulk MOSFET it would be 43.89nA). Table 4.4 illustrates the transmission delay and average power consumption data of a Fin-FET-based inverter at the 16nm technology node for a range of V_{DD} values from 0.2V to 0.85V. Ring oscillator has an odd number of CMOS inverters. What comes out of one inverter goes into the next one. The last result goes back to the first converter.

Conclusion: In this chapter, pFin-FET and nFin-FET devices implemented with Verilog A tool, for desired characteristics and verified the impact of its geometry on the performance and optimized sizes are measured. Then a Fin-FET based inverter is designed and tested. Observed its power and delay.

Table 4.4: Comparison of inverters with different technologies

Circuit	Power	Propagation Delay	PDP(J)	EDP (Js)	I_{ON} (µA)
CMOS- Inverter [47] 45nm Tech	16 µW	0.25 p sec	4.0×10^{-18}	4.0×10^{-30}	7.91
DG CMOS [58] 45nm Tech	4.49 µW	2.51 p sec	11.27×10^{-18}	28.28×10^{-30}	2.14
Fin-FET- based Inverter [89] 20nm Tech	3.8 nW	2.2 P sec	8.36×10^{-21}	18.39×10^{-33}	4.21
Fin-FET- based Inverter (this work**) 18 nm Tech**	3.19 nW	1.34 p sec	4.26×10^{-21}	5.72×10^{-33}	4.74
Fin-FET based sleepy keeper inverter (this work**) 18nm Tech**	1.474 nW	9.8 p sec	14×10^{-21}	137.2×10^{-33}	6.18

CHAPTER 5

FINFET BASED RING OSCILLATOR

In this chapter, Fin-FET-based five-stage and twenty-one-stage ring oscillator circuits are designed. The Fin-FET model developed in Chapter 4 is utilized for these designs. To achieve low power operation, the optimization technique introduced in Chapter 3 is applied. Following the design implementation, simulations were carried out to evaluate key performance metrics, which were then compared with those from similar existing works.

5.1 INTRODUCTION

A typical ring oscillator consists of N amplifiers interconnected in a feedback loop. Because each amplifier stage functions as an inverter, it simply causes a delay in the signal by a specific amount of time, referred to as (τ_d), hence this is called a delay stage. The purpose of a ring oscillator is to operate the inverters in a manner where each one adds 60^0 of phase shift in addition to the natural 180^0 resulting from inversion. Usually, ring oscillators can be implemented with the cascade connection of odd or even number of identical stages.The basic building block of a ring oscillator is the inverter and is designed to convert a high input signal into a low output signal, and vice versa.

In this work, the inverter is constructed using Fin-FET-based pMOS and nMOS transistors connected in series, sharing a common input gate. The design employs the short-gate mode configuration to enhance performance. Compared to conventional CMOS and SOI-based inverters, the Fin-FET-based inverter offers significantly improved control over SCEs [69]. Fin-FET benefits, including enhanced speed, reduced leakage, and low power consumption, making it suitable for low-power circuit design. However, it acknowledges certain drawbacks such as quantum effects, corner effects, width quantization, and fabrication difficulties as mentioned in the chapter 4. The dominant features of IG-FinFET are controlling threshold voltage by back gate, low power consumption and minimizing transistor count. But the merit of SG-Fin-FET is less delay.

The number of inverters in a ring depends on the desired target frequency, noise performance, and power consumption. The number of inverters connected in the loop plays a crucial role in determining several key factors [80-82]:

i) **Frequency:** With more inverters, the total propagation delay increases, resulting in a slower oscillation frequency.

ii) **Gain:** An odd number of inverters are preferred since, even numbers of inverters result in zero net phase shift around the loop, preventing sustained oscillations. With an odd number of inverters, the overall loop gain becomes positive. The positive gain helps overcome losses within the inverters and other circuit elements.

iii) **Noise:** While a higher number of inverters can improve noise cancellation to some extent, it can also introduce additional noise sources due to each inverter's inherent noisecontribution.

iv) **Power Consumption:** More inverters typically translate to higher power consumption because there are more active devices in the ring.

5.2 BASIC RING OSCILLATOR

Ring oscillator has an odd or even number inverters connected in a loop. They are connected in cascaded, which means the first stage inverter output is connected to the next stage as the input, second stage inverter output is connected to the third stage as the input and so on. The last stage output is connecting back to the first stage as the input. Since all stages in the loop are identical, their time constants, threshold voltages and amplitudes are same. Each stage in the ring oscillator introduces the delay, hence the frequency of oscillation produced by the circuit can be measured with the equation (5.1).

$$f = \frac{1}{2N\tau_d} --(5.1)$$

where:

- f is the oscillation frequency
- N is the number of inverter stages
- τ_d is the delay time of an individual inverter

The transfer function of a single stage inverter is in the ring oscillator mathematically represented as in equation (5.2).

$$H_i = \frac{A_0}{1 + j\omega R_D C_l} - - - - (5.2)$$

Phase Noise calculation:

Transfer function of the oscillator, $H(\omega) = \frac{A(\omega)}{1+A(\omega)}$ - ---- (5.3)

At the frequency of oscillations $A(\omega)|_{\omega=\omega_0} = A(\omega_0)$

$$H(\omega)|_{\omega=\omega_0} = H(\omega_0)$$

With the noise, $A(\omega_0 + \Delta\omega)$ $H(\omega_0 + \Delta\omega)$

$$H(\omega_0 + \Delta\omega) = \frac{A(\omega_0+\Delta\omega)}{1+A(\omega_0+\Delta\omega)} \text{ ---------} (5.4)$$

$$A(\omega_0 + \Delta\omega) \approx A(\omega_0) + \Delta\omega \frac{\partial A(\omega_0)}{\partial\omega} + \text{--------}$$

$$H(\omega_0 + \Delta\omega) = \frac{A(\omega_0) + \Delta\omega \frac{\partial A(\omega_0)}{\partial\omega}}{1 + A(\omega_0) + \Delta\omega \frac{\partial A(\omega_0)}{\partial\omega}}$$

at $\omega = \omega_0$, $A(\omega_0) = -1$ & $\Delta\omega \frac{\partial A(\omega_0)}{\partial\omega} \ll 1$

$$H(\omega_0 + \Delta\omega) = \frac{-1+0}{1-1+\Delta\omega\frac{\partial A(\omega_0)}{\partial\omega}} \approx \frac{-1}{\Delta\omega\frac{\partial A(\omega_0)}{\partial\omega}}$$

$$\frac{\partial A(\omega_0)}{\partial\omega} \approx \frac{\partial}{\partial\omega}|A(\omega_0)|e^{j\emptyset(\omega_0)} \approx \left|\frac{\partial A(\omega_0)}{\partial\omega}\right| e^{j\emptyset(\omega_0)} + j\left|\frac{\partial\emptyset(\omega_0)}{\partial\omega}\right| e^{j\emptyset(\omega_0)}$$

$$\approx \sqrt{\left(\frac{\partial A(\omega_0)}{\partial\omega}\right)^2 + \left(\frac{\partial\emptyset(\omega_0)}{\partial\omega}\right)^2}$$

$$|H(\omega_0 + \Delta\omega)| = \frac{1}{\Delta\omega\sqrt{\left(\frac{\partial A(\omega)}{\partial\omega}^{0}\right)^2 + \left(\frac{\partial \emptyset(\omega)}{\partial\omega}^{0}\right)^2}} - - - (5.5)$$

5.3 THREE STAGE RING OSILLATOR:

Figure 5.1. shows the block diagram of 3-stage ring oscillator, each inverter output is connected to the input as next inverter and the output of the 3rd inverter is feedback to the input of first inverter to make the oscillation in output. In an oscillator, the output usually gets shifted by 180° from the input. This is due to the presence of phase delay circuit in the oscillator. These phase shift circuits use an RC network in the feedback loop of a transistor to generate the required phase shift at a particular frequency to sustain oscillations [83-84]. They are moderately stable in frequency and amplitude, and very easy to design and construct. In order to create sustain oscillations at a particular frequency, the circuit must have a gain higher than unity, and a total phase shift around the loop of 360^0 (which is equivalent to 0^0, or positive feedback).

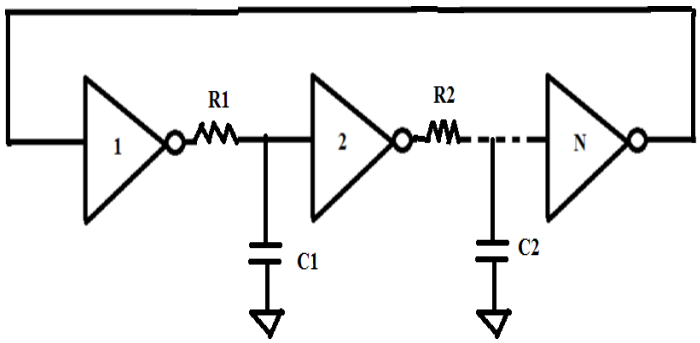


Figure 5.1: Basic Three stage ring oscillator circuit.

An inverter circuit produces180^0 phase shift between its input to output, the remaining 180^0 of phase shift necessary to provide a total of 360^0 is provided by an external network of resistors and capacitors. By selecting the positions of R and C, the phase can be made to lead or lag the input. Due to the identical nature of the three stages, the overall transfer function of the ring oscillator can be expressed as: For three stages, the transfer function is

From equation (5.2), for three stages the overall transfer function becomes

$$H_T = \left[\frac{A_0}{1 + j\omega R_D C_l}\right]^3$$

$$\text{At } H_T = -1$$

$$\left[\frac{A_0}{1 + j\omega_0 R_D C_L}\right]^3 = -1$$

Angle criteria, $-3\tan^{-1}\omega_0 R_D C_L = -180^0$

$\tan^{-1}\omega_0 R_D C_L = 60^0$

$$\omega_0 = \frac{\sqrt{3}}{R_D C_L}$$

Magnitude criteria,

$$\frac{|A_0|^3}{|1 + j\omega_0 R_D C_L|^3} = 1$$

$$|A_0|^3 = |1 + j\omega_0 R_D C_L|^3$$

$$A_0 = 1 + j\omega_0 R_D C_L$$

$$A_0 = 1 + j\frac{\sqrt{3}}{R_D C_L} R_D C_L \text{ ---(5.6)}$$

Hence, the DC gain is, $A_0 = |1 + j\sqrt{3}| = 2$

For Fin-FET, $A_0 = g_m R_D$

5.4 THREE STAGE Fin-FET BASED RING OSILLATOR

A Fin-FET-based three-stage ring oscillator circuit is shown in figure 5.2, where three Fin-FET inverters are connected in cascade, and the output of the third stage is fed back to the input of the first stage. Fin-FET based inverter designed in Chapter 4, along with the low-power optimization technique discussed in Chapter 3, together considered for this implementation. Fin-FET technology offers superior voltage control and enhanced output resolution due to its multi-gate architecture, where multiple gate terminals are connected to improve device performance [54].

Traditional transistor scaling faces limitations due to short-channel effects, beyond which performance degrades. Fin-FETs address these limitations by using a thin silicon fin as the channel, enabling low-power operation, reduced operating voltage, higher speed, and significantly lower static power consumption.

This study designs and implements a regional system using a standard 18 nm CMOS process, incorporating a dual-channel low-noise amplifier applied to remotely located transistors. The entire CMOS-level architecture is developed using the Cadence EDA tool, and key performance parameters such as delay, power consumption, and area are analyzed and compared with conventional approaches.

From equation (5.1), frequency is the function of delay and the number of stages. The delay of a single inverter stage (τ_d) can be calculated as the time constant of an RC low-pass filter i.e the delay is proportional to the product of the resistance (R) and capacitance (C) in the equivalent RC circuit. The oscillation frequency of the ring oscillator can be expressed in terms of the bias current (I), amplitude of oscillations (Vosc), and parasitic capacitances (C_G) by using equations (7) and (8). These equations likely incorporate the relationships between theseparameters and the overall performance of the ring oscillator [52-53].

$$\tau_d = \frac{V_{osc} * C_G}{I_{cont}} \text{----- (5.7)}$$

$$f_{osc} = \frac{Icont}{2NV_{osc} * C_G} \text{--------- (5.8)}$$

By analyzing these equations, designers can gain insights into how adjusting bias currents, controlling the amplitude of oscillations, and minimizing parasitic capacitances can impact on the overall frequency and performance of the ring oscillator.

Specifications of the design:

Device type: SG FinFET

Gate length(L_gate) = 18 nm, tox=2.4 nm, V_{DS}=0.8V,

H_fin=10 nm to 40 nm, W_fin=4 to 20 nm, fin pitch=29 nm,

work function=4.39eV,source-drain/channel doping range= $10^{16}/cm^3$- $10^{19}/cm^3$.

With the Fin-FET based sleepy keeper type which was shown in figure 4.14 (b) , a three-stage self-oscillating ring oscillator topology is implemented in 18 nm Fin-FET technology in the Cadence environment and shown in figure 5.2, where all transistors are connected asynchronously to realize the Fin-FET based low power oscillator.

The simulation waveform demonstrates the behavior of the self-oscillating ring oscillator, capturing the signal response from input to output. As the number of transistors in the circuit increases its power delay product also increases. This represents the time delay analysis of the self-oscillating ring oscillator, evaluated using Cadence EDA software. Transient, DC and AC analysis has been done to verify the frequency and power.

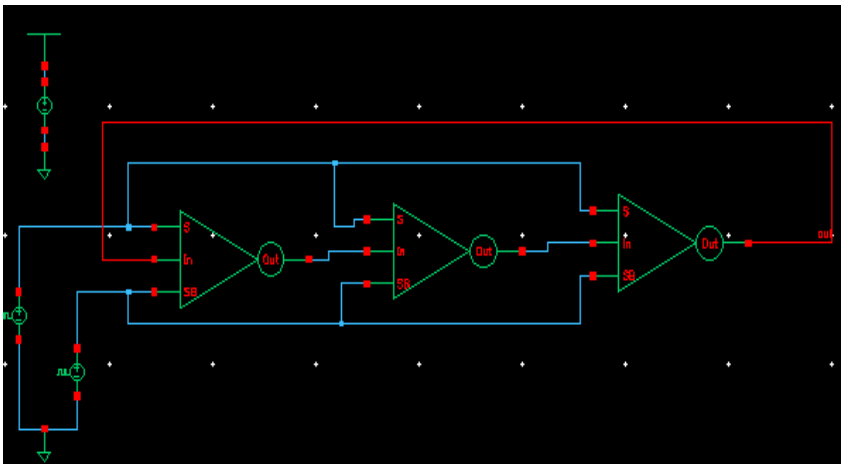


Figure 5.2: Three stage Fin-FET ring oscillator schematic circuit.

The proposed design demonstrates high-speed operation with significantly reduced path and propagation delays, as well as minimized rise and fall times. As a result, this methodology achieves faster performance compared to conventional approaches.

To analysis the ring oscillator, five different analyses can be in the Cadence environment, they are

- ❖ Transient analysis
- ❖ Stability analysis
- ❖ Phase Noise analysis
- ❖ Jitter analysis
- ❖ PSS analysis

5.4.1 Transient analysis:

Transient analysis is performed to find the frequency of oscillations and power consumption. To do the transient analysis, click on ***launch → ADE explorer → create new view → ok.*** Then the popup window will open as shown in figure 5.3, where select the response as ***tran***, choose stop time in nano seconds then click **ok**.

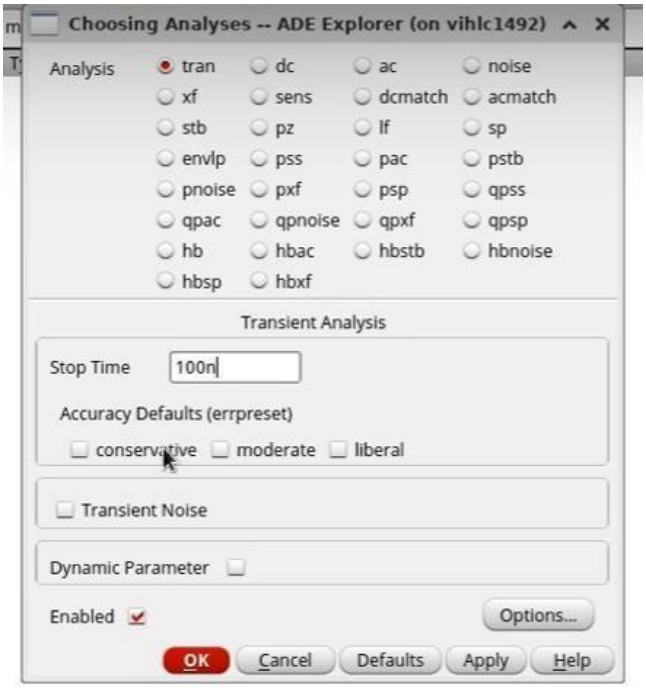


Figure 5.3: Analysis choosing popup window

Then define the V_{DD} and Vcntr voltages to the circuit. Then add Vout, frequency and power to know the simulation values.

The oscillator is tested by applying two different types of sources as the test input and are discussed here and the transient response is shown in figure 5.4. To verify the transient response, a DC voltage source with V_{DC} =1V is connected in the feedback path of the ring oscillator circuit and vary its voltage from 0V to 700 mV for the tuning range. Three-stage ring Fin-FET based ring oscillator frequency calculation screenshot is shown in figure 5.5.

From this it is shown that the frequency of oscillations is 44.1 GHz @ VG=566 mV. From this analysis, we observed that the simulation results achieved as PDC=4.1 µW.

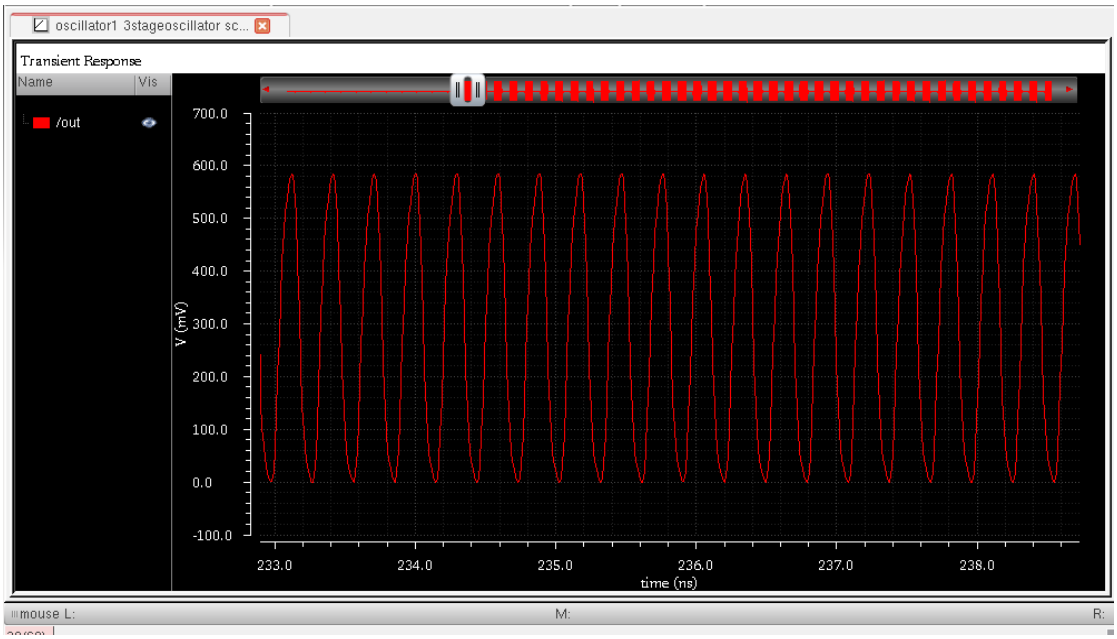


Figure 5.4: Transient response of proposed three stage Fin-FET ring oscillator.

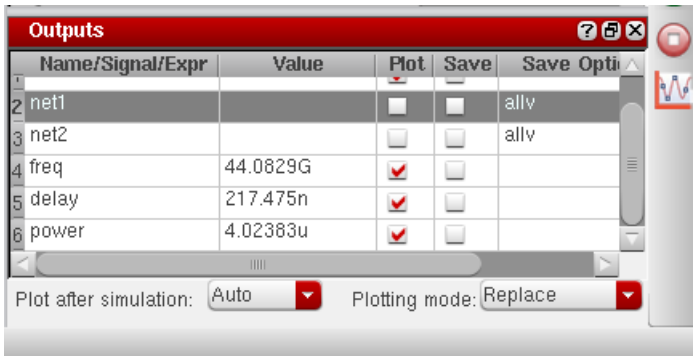


Figure 5.5: Three stage Fin-FET ring oscillator frequency.

Now, connect a pulse source'VPWL' in the feedback path of the oscillator circuit with the specifications of 2 nsec duration and 1V peak to peak amplitude. Now obtained these results as P_{DC} =2.4 µW, f_{osc}=13.9 GHz @ V_G=556 mV. Table 5.1 has all these readings.

Table 5.1: Fin-FET based 3 stage ring oscillator simulation results.

	DC voltage	**Pulse**
Technology	18 nm Fin-FET	18 nm Fin-FET
Supply	566 mV	556 mV
f_{osc}	44.1	13.9 GHz
Power	4.02 µW	2.4 µW
Delay	217 n sec	413 nsec

5.5 A FIVE STAGE RING OSCILLATOR

A five stage Fin-FET based ring oscillator circuit is designed by cascading five Fin-FETbased inverter circuits, which were designed in chapter 4, and the circuit is shown in figure 5.6.

From equation (5.2), for five stages, the overall transfer function is

$$H_T = \left[\frac{A_0}{1 + j\omega R_D C_l}\right]^5$$

and at $H_T = -1$

$$\left[\frac{A_0}{1 + j\omega_0 R_D C_L}\right]^5 = -1$$

From the angle criteria we can write, $-5\tan^{-1}\omega_0 R_D C_L = -180^0$.

Then $\tan^{-1}\omega_0 R_D C_L = 35^0$

$$\omega_0 = \frac{3/4}{R_D C_L}$$

Magnitude criteria is, $\frac{|A_0|^5}{|1+j\omega_0 R_D C_L|^5} = 1$

$$|A_0|^5 = |1 + j\omega_0 R_D C_L|^5$$

$$A_0 = 1 + j\omega_0 R_D C_L$$

$$A_0 = 1 + j\frac{3/4}{R_D C_L} R_D C_L$$

Then the DC gain is, $A_0 = |1 + j3/4|$=2

Usually, $A_0 = g_m R_D$

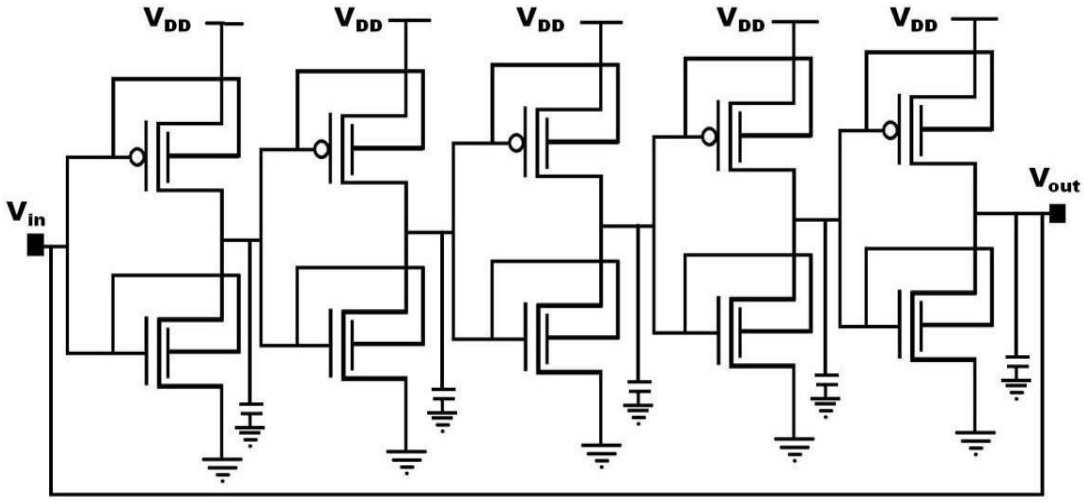


Figure 5.6: Five stage Fin-FET ring oscillator circuit.

The schematic of proposed five stage low-power Fin-FET based self-oscillating ring oscillator topology is implemented with 18nm Fin-FET technology in the Cadence environment and shown in figure 5.7, where all transistors are connected asynchronously to realize the Fin-FET based low power oscillator. The Ring oscillator is tested by applying two different types of sources as mentioned in the above design are tested by apply as the input are discussed here.

Transient, DC, and AC analysis are performed to verify its frequency and power characteristics. Figure 5.8 shows its transient response. To verify the transient response, a DC voltage source with V_{DC}=1V is connected in the feedback path of the ring oscillator circuit and varies its voltage from 0V to 700 mV for the tuning range.

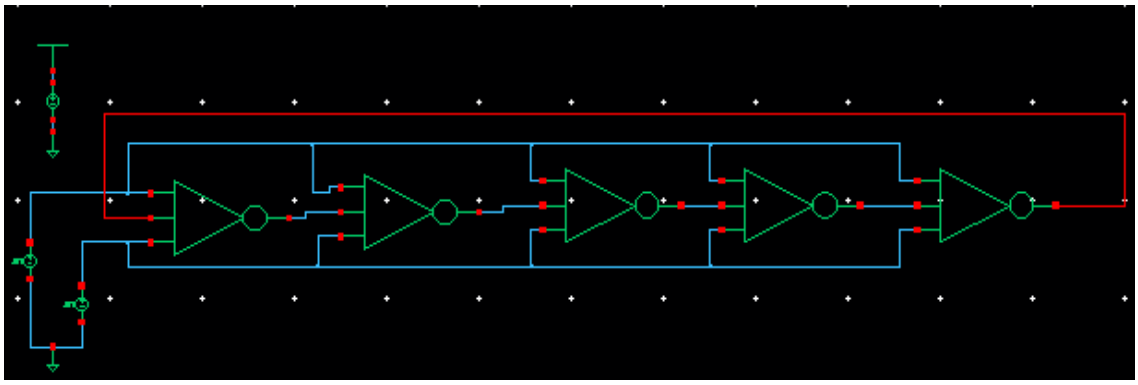


Figure 5.7: Five stage Fin-FET ring oscillator schematic circuit.

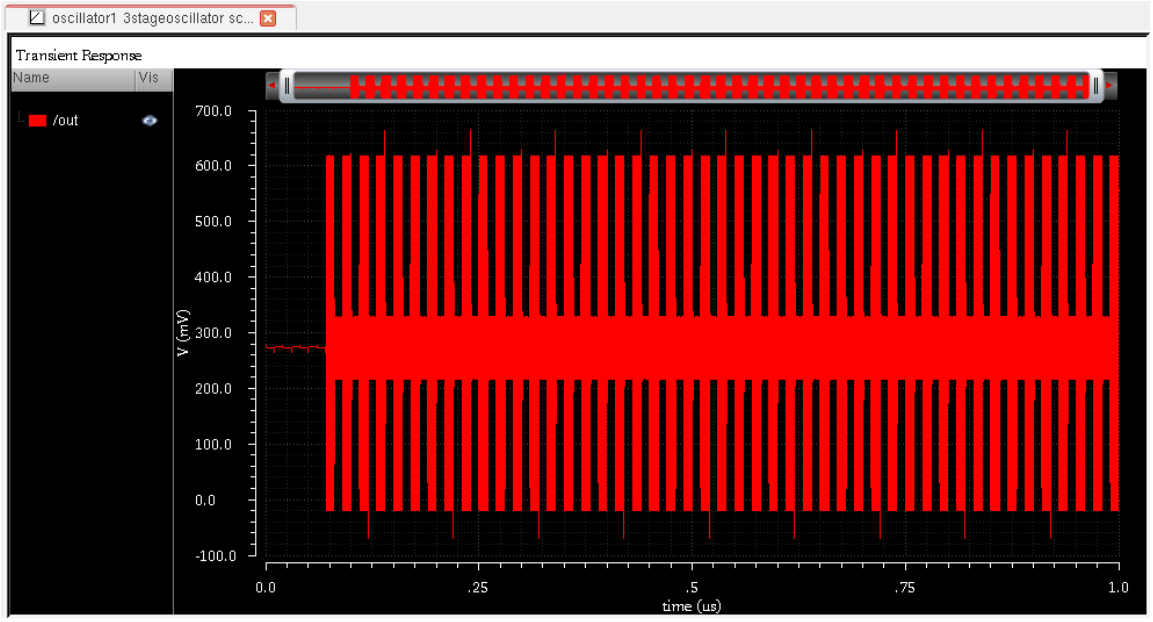


Figure 5.8: Five stage Fin-FET ring oscillator transient response.

Five-stage ring FinFET based ring oscillator frequency calculation screen shot is shown in figure 5.9.From this it is shown that the frequency of oscillations is 7.7 GHz @VG=566mV and power PDC=12.9 µW.

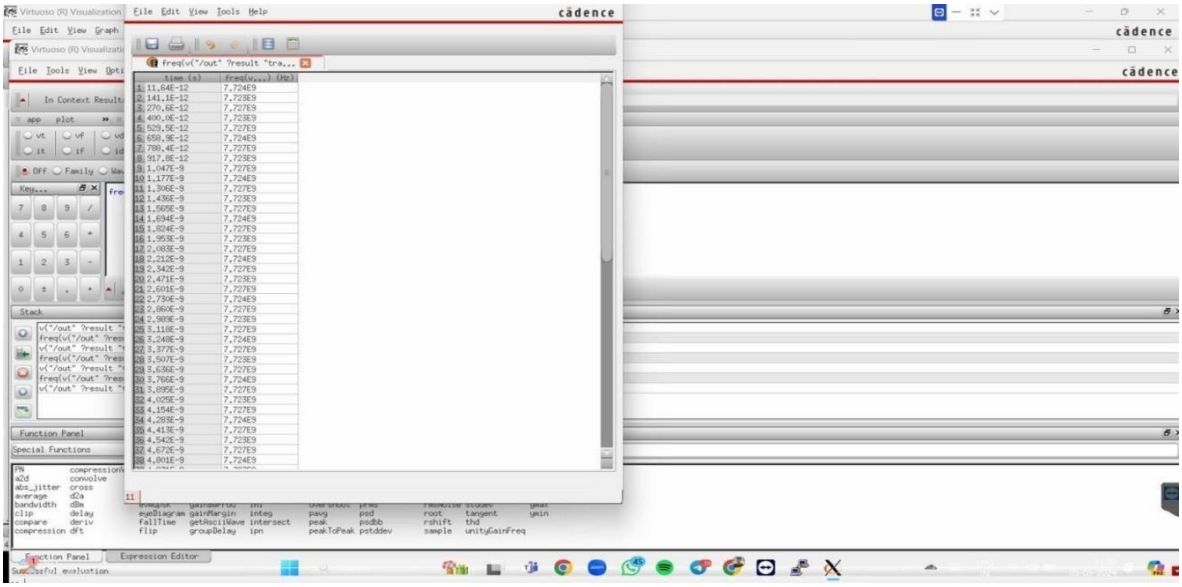


Figure 5.9: Five stage Fin-FET ring oscillator frequency.

Now, connect a pulse source 'VPWL'in the feedback path of the oscillator circuit with the specifications of 2n sec duration and 1V peak to peak amplitude. Now obtained as P_{DC}=10.4 µW, f_{osc}=8.1GHz @ V_G=556 mV. Table 5.2 has all the readings.

Table 5.2: Fin-FET based 5 stage ring oscillator simulation results

	DC voltage	**Pulse**
Technology	18 nm Fin-FET	18 nm Fin-FET
Supply	566 mV	556 mV
f_{osc}	7.7 GHz	8.1 GHz
Power	12.9 µW	10.4µW
Delay	66.1996 nsec	66.1996 nsec

Additional performance metrics such as phase noise, jitter, and supply voltage sensitivity could be evaluated based on the simulation results.

5.6 TWENTY-ONE STAGE RING OSCILLATOR:

To investigate the impact of increasing the number of stages, a 21-stage ring oscillator was designed. The schematic of this circuit is depicted in Figure 5.11. The inverter stages within the ring oscillator are identical, a characteristic attributed to the MOSFET's infinite gate input impedance. This ensures consistent behavior and simplifies analysis. Each inverter stage introduces a significant delay, resulting in a noticeable time lag between input changes and output updates. To address this, an RC circuit is connected to each inverter stage to maintain the output logic value for a specific duration. The RC circuit acts as a filter, providing temporary storage for the output signal. This helps to prevent rapid changesin the output value, ensuring a more stable and predictable response.

From equation (5.2), the transfer function of 21 stage oscillator is

$$H_T = \left[\frac{A_0}{1+j\omega RC}\right]^{21}$$

Assume that at $H_T = -1$

$$\left[\frac{A_0}{1+j\omega RC}\right]^{21} = -1$$

Apply the angle and magnitude conditions to the above equation.

Then the angle criteria, $-21\tan^{-1}\omega RC = -180^0$.

$\tan^{-1}\omega RC = 8.6^0$ and $\omega = \frac{0.15}{RC}$

Magnitude criteria, $\frac{|A_0|^{21}}{|1+j\omega_0 R_D C_L|^{21}} = 1$

$$|A_0|^{21} = |1 + j\omega RC|^{21} \text{ and } A_0 = 1 + j\omega RC$$

substitute ω value, then, $A_0 = 1 + j\frac{0.15}{RC}RC$.

The DC gain, $A_0 = |1 + j0.15| \approx 2$

Usually, $A_0 = g_m R_D$.

Where, $A_0 = g_m R_{tot}$;

$$g_m = \sqrt{\mu_n C_{ox} \frac{W}{L} I_{DS}} \text{-----(5.9)}$$

$$R_{tot} = (\gamma_{oce}' // R_{eq1})$$

$$\gamma_{oce}' = (1 + g_{m1} 2\gamma_{oce})\gamma_{01}$$

$$A_0 = (\sqrt{\mu_n C_{ox} \frac{W}{L} I_{DS}})\ R_{tot}$$

$$\frac{W}{L} = \frac{A_0^2}{\mu_n C_{ox} R_{tot}^2}$$

$$C_{tot} = C_{in1} + C_{eq1}$$

$$C_{tot} = 2W_r C_{ov} + \frac{2}{3} W_r C_{gs1} + C'_{gd1} (1 + g_{m1} R_{tot}) \text{ ----(5.10)}$$

Where, $C_{gs1} = W_1 C_{gs0}$ & $C'_{gd1} = W_1 C_{gd0}$

$$R_{tot} = \frac{V_{swing}}{I_{DS}} \text{---(5.11)}$$

$$\frac{\tau_d}{C_{tot}} = \frac{V_{swing}}{I_{DS}}$$

$$\tau_d = \frac{V_{swing}}{I_{DS}} C_{tot} \text{---(5.12)}$$

Assume, Vswing=0.8V and I_{DS} from power requirement is 1mA

$$R_{tot} = \frac{0.8V}{1mA} = 800$$

For $f_{osc} = 10GHz$, $f_{osc} = \frac{1}{2N\tau_d}$

$$\tau_d = \frac{1}{2*21*10G} = 238 \text{ f Sec}$$

$$238\,f = \frac{0.8}{1m}\,C_{tot}$$

$$C_{tot} = \frac{238f*1m}{0.8} = 29.75\text{x}10^{-18}$$

$$\tau_d = R_{tot}C_{tot}$$

$$f_{osc} = \frac{1}{2N*R_{tot}(2W_rC_{ov}+\frac{2}{3}W_rC_{gs1}+C'_{gd1}(1+g_{m1}R_{tot}))} \quad (5.13)$$

Assuming that the drain-source capacitance and load capacitance are equal, each inverter stage within the ring oscillator contributes 180^0 of phase shift. Therefore, to achievea total phase shift of 360^0, the remaining 180 degrees must be provided by the RC network connected to each inverter.

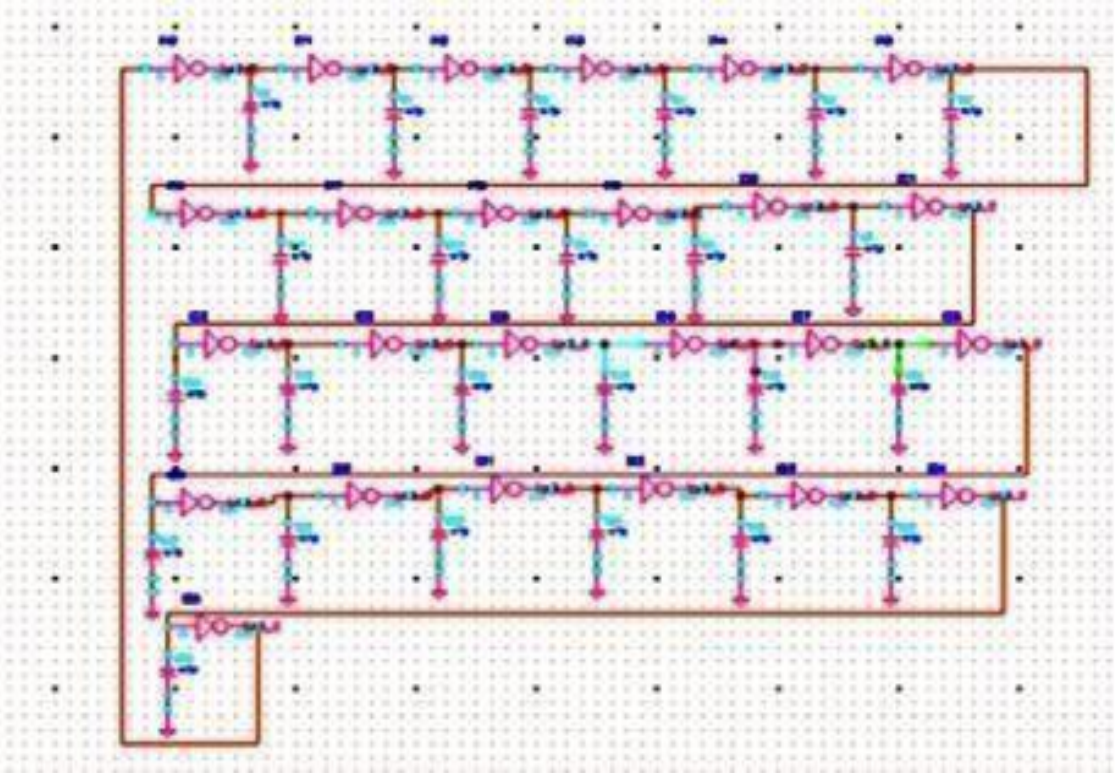


Figure 5.10: Schematic of twenty-one stage ring oscillator

For optimal performance, the input impedance of the RC network (Zrc) should be significantly larger than the output impedance of the inverter stage (Za). This impedance mismatch helps to prevent the RC network from loading the inverter, which could reduce its gain and potentially destabilize oscillation.

$$Z_{rc} \geq Z_{Inv} \quad \text{and } 50 > 10\text{k}\Omega * C * 21 \text{ ----(5.14)}$$

The schematic in Figure 5.10 shows the 21-stage ring oscillator. The value of the capacitance in the RC network connected to each inverter is 23 µF.

Transient analysis: A 21-stage ring oscillator designed with 18 nm Fin-FET technology and simulated using. To simulate, the input signal settings are set as rise time = 1 ns, fall time= 1 ns and period: 200 ns.

Simulation Results: Figure 5.11 shows the transient response of the 21-stage ring oscillator, the following are the observes from this.

- Delay=7 ps
- Leakage Current=828 pA (compared to 43.89 nA in bulk CMOS)
- Oscillation Frequency= 4.126 GHz
- Power Consumption= 51 µW

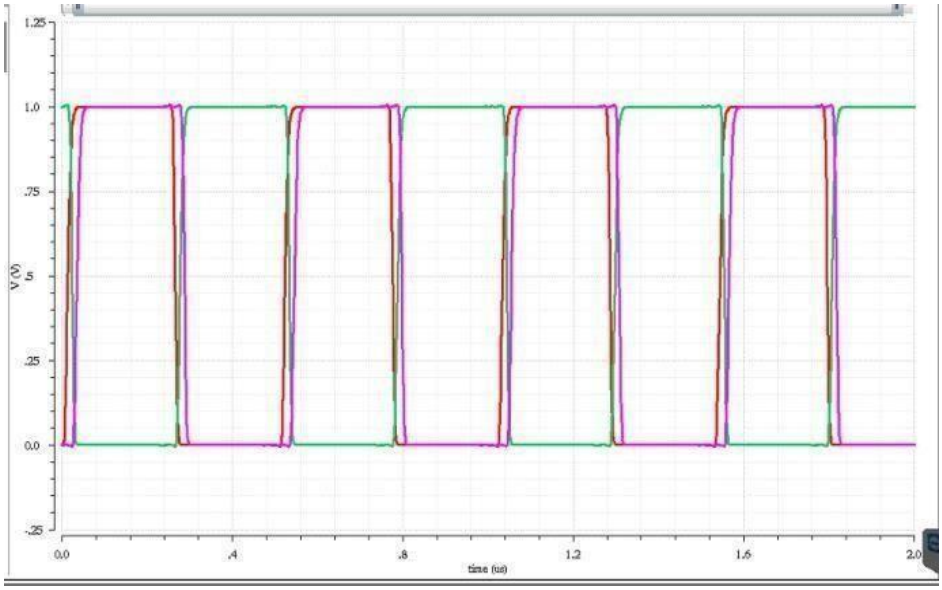


Figure 5.11: Transient Analysis of first four stages in twenty-one stage RO

The Key Observations:

- The ring oscillator achieved a frequency of 4.126 GHz with a relatively low power consumption of 51 µW.
- The use of the sleepy keeper technique contributed to improved power efficiency.
- The 21-stage configuration, while increasing the overall delay, also offers advantages such as enhanced noise immunity and improved stability.

Layout and Area: Figure 5.12 shows the layout of the 21-stage ring oscillator. The total area occupied by the circuit is calculated to be 289.5 µm x 129 µm x 0.09 µm = 1492.89 μm^2.

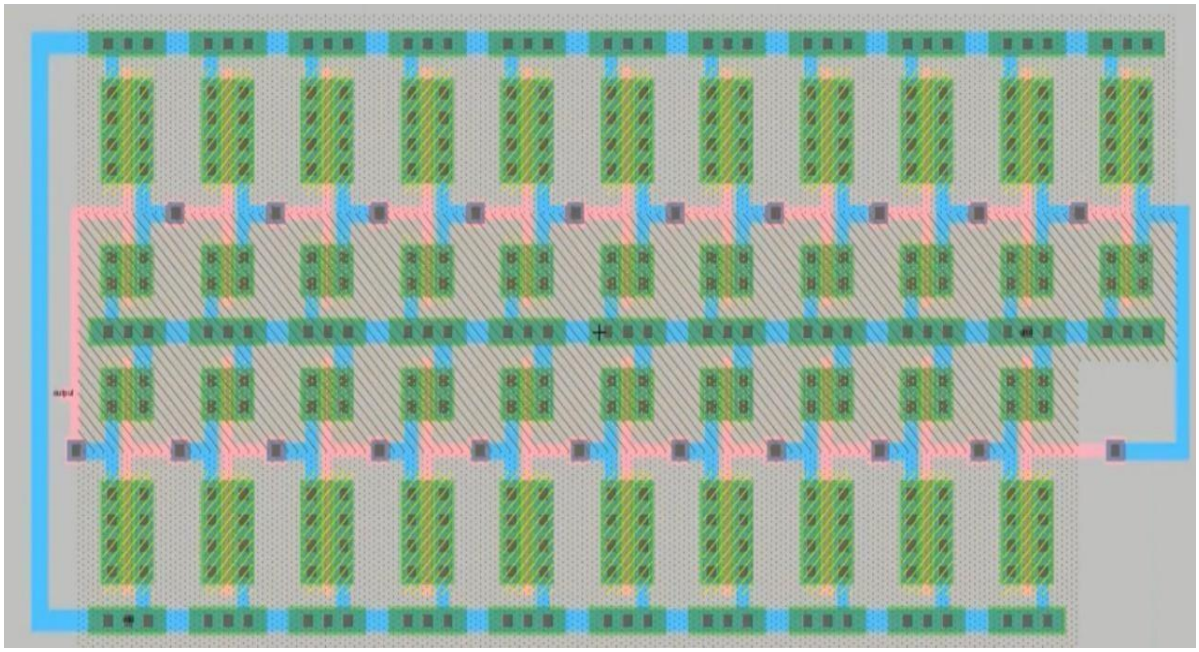


Figure 5. 12: Twenty-one stages RO Layout

5.7 STABILITY ANALYSIS:

The stability analysis is used to check the stability of the oscillator by selecting stability analysis or periodic stability analysis button in the add analysis window. The loop gain and phase margins of the oscillators should be measured through gain and phase plots. Of the gain margin and phase margins are 0 dB and 0^0, it's more stable.

5.8 PHASE NOISE:

Phase noise is the variation of the output phase with respect to the ideal output phase and is a continuous process in both the time and frequency domains. That is, the output phase is defined for all points in time. The phase noise profile of an oscillator provides insight into its stability in the frequency domain.

There are two types of oscillator phase noise: Thermal (Johnson) noise in resistors and FET channels. Shot noise in diodes and bipolar transistors. The sources of these two noise types have a spectral density that is constant with frequency. Therefore, they are generically referred to as additive white Gaussian noise (AWGN). Single sideband phase

noise is defined as the power in one phase modulation sideband per Hertz bandwidth [86-87].

$$L(f_{off}) = \frac{P_s}{P_{ssb}} \text{----------} (5.15)$$

Where,

Ps-carrier power

F_{off}- frequency offset

Pssb-side band power in one Hz bandwidth at an offset frequency 'f' from the center

$$SSB\ PN = L(f)\ in\ \frac{dBc}{Hz} = 10\log[L(f)]$$

$$L(f_{off}) = \frac{\tau_{rms}^2}{8\pi^2 f_{off}^2} = \frac{\overline{in^2}/\Delta f}{q_{max}^2}$$

$$\overline{in^2}/\Delta f\ \alpha\ \mu_{eff}\ C_{ox}\ \frac{W_{eff}}{L}\Delta V$$

Where,

'W_{eff}' is the effective fin width of the inverter is the sum of fin widths of both pFET and nFETs as shown in the following equation

$$W_{eff} = W_n + W_p$$

'μ_{eff}' is the effective mobility of the carriers in the inverter

$$\mu_{eff} = \frac{\mu_n W_n + \mu_p W_p}{W_n + W_p}$$

'q_{max}' is the maximum charge stored across the capacitor

$$q_{max} = C_L V_{DD}$$

'ΔV' is the change in gate overdrive potential due to the charge stored

$$\frac{V_{DD}}{2} - V_{Th}$$

$$f_{osc} = \mu_{eff}\ C_{ox}\ \frac{W_{eff}}{8\ \rho\ N\ L\ q_{max}}\Delta f^2$$

$$= 13.44\ \text{GHz}$$

Phase Noise with the frequency offset Δf =1MHz

$$L(f_{off}) = -75.2\ dBc/Hz$$

Phase noise curve is shown in figure 5.13, has three parts, 0 dB/dec part, -20 dB/dec part and -30 dB/dec part. 0 dB/dec part represents thermal noise from the buffer circuits. -20 dB/dec part is the thermal noise from the oscillator core part. -30 dB/dec part is the flicker noise. -20 dB/dec part is the high and main at the low frequencies is known as phase noise.

The oscillator circuit acts as a noise integrator, introducing a factor of '$1/f^2$' to the phase noise as a function of frequency offset. In ring oscillators, this transforms the white noise in the circuit into a '$1/f^2$' phase noise distribution.

At very low frequencies, variations in the surface conductivity due to contact and surface irregularities cause an increase in noise that varies approximately as '1/f'. This noise is known as the flicker noise or 1/f noise. In ring oscillators, flicker noise adds a '$1/f^2$ ' term to the phase noise distribution at low frequencies.

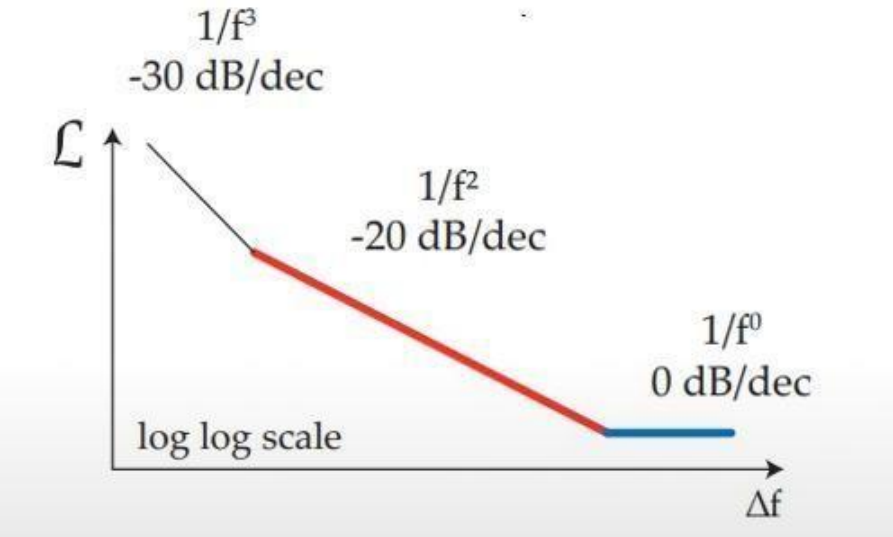


Figure 5.14: Phase Noise curve

In the ring oscillator circuit, the capacitive loading on the inverter outputs introduces

delay into the feedback loop and the inverters provide the gain, nonlinear saturation, and output noise. Ring oscillators have the advantage of occupying a relatively small area in an integrated circuit. But the loop gain in a ring oscillator goes to DC, which makes them susceptible to flicker noise as well as Johnson noise, resulting in higher phase noise at low frequency offsets.

Phase Noise Measurement Setup and simulation: Go to the maestro, then the popup window shown in figure 5.14 will open.

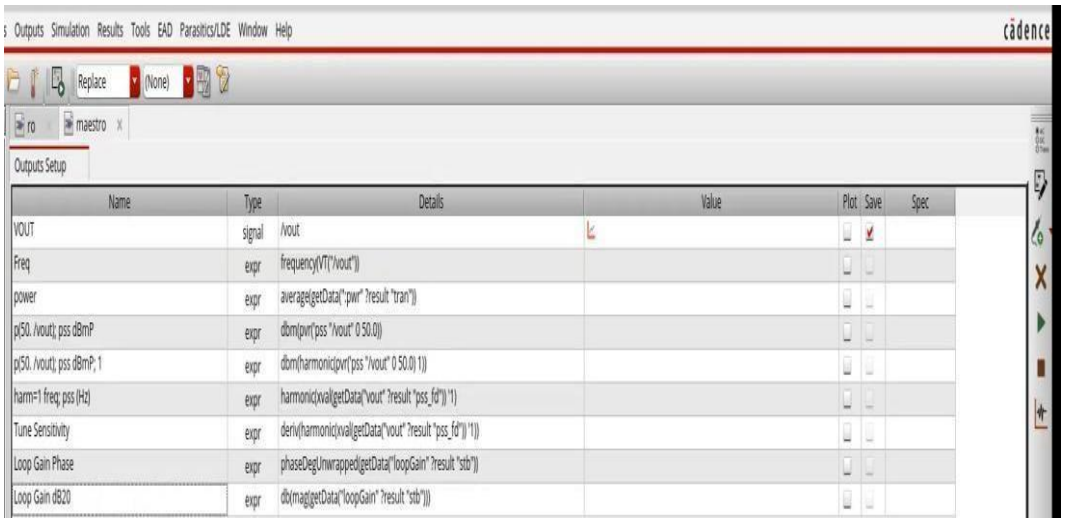


Figure 5.14: Phase noise setup window

Then click on ***click to add analysis***, then the popup window will open as in figure 5.15 and do the selections as in the window.

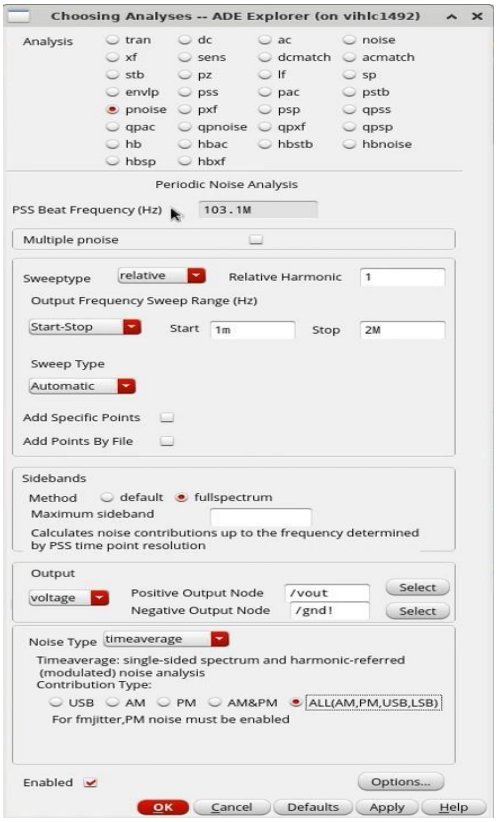


Figure 5.15: Phase noise analysis setting window

Then click the ***run*** button in ***Maestro***. Then simulations will run. Then click on the ***results Direct plot → main form***. Then one popup window will open as in figure 5.16 and do the selections as specified.

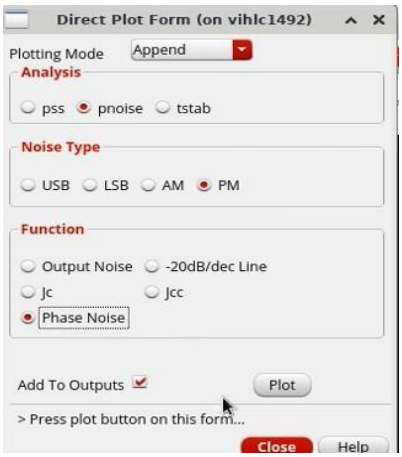


Figure 5.16: Popup window

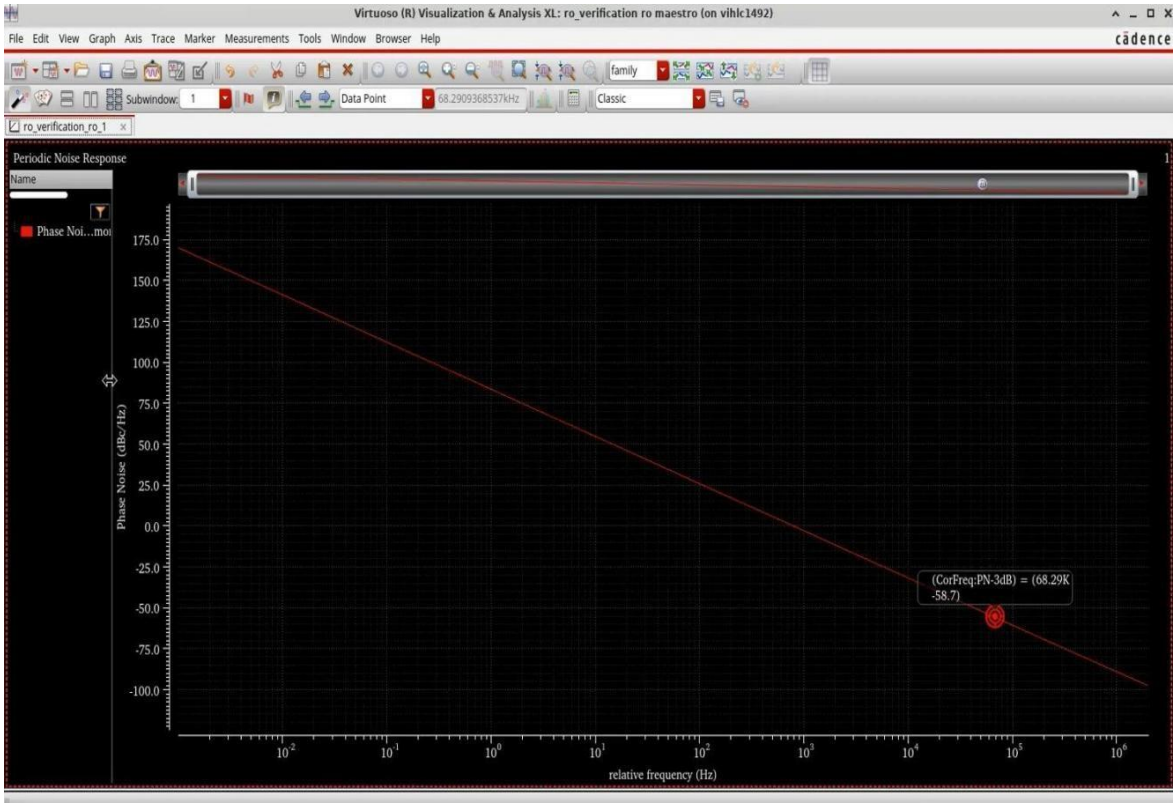


Figure 5.17: Phase Noise response

The phase noise plot of the ring oscillator is shown in figure 5.17 and phase noise recorded as -58.7 dBc/Hz. To check the output noise, for doing necessary settings the popup window shown in figure 5.18 will be used.

Figure 5.18: Settings for output noise measurement

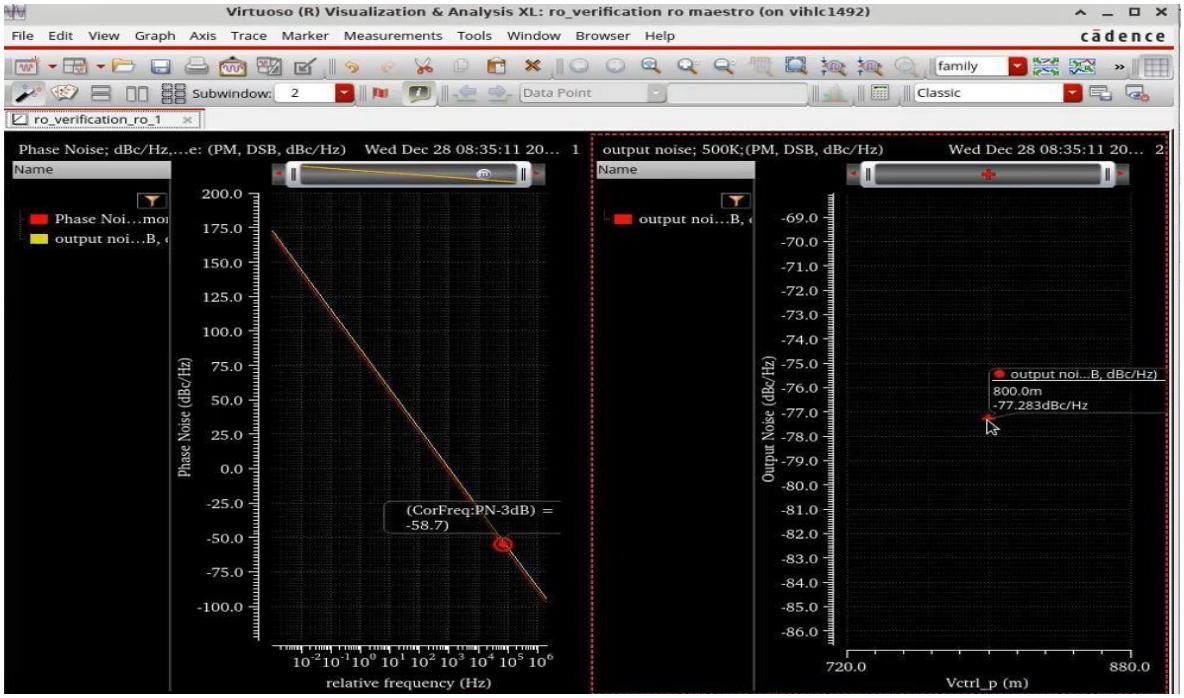


Figure 5.19: Output noise and phase noise plots

Output noise and phase noise plots are shown in figure 5.19. The output noise is measured as -77.28 dBc/Hz.

5.8.1. Jitter analysis:

Go to ***Maestro*** and click the ***run*** simulation button for simulation with phase noise analysis settings. Then click on the ***results → Direct plot → main form***. Then one popup window will open as in figure 5.20 and do the settings as specified.

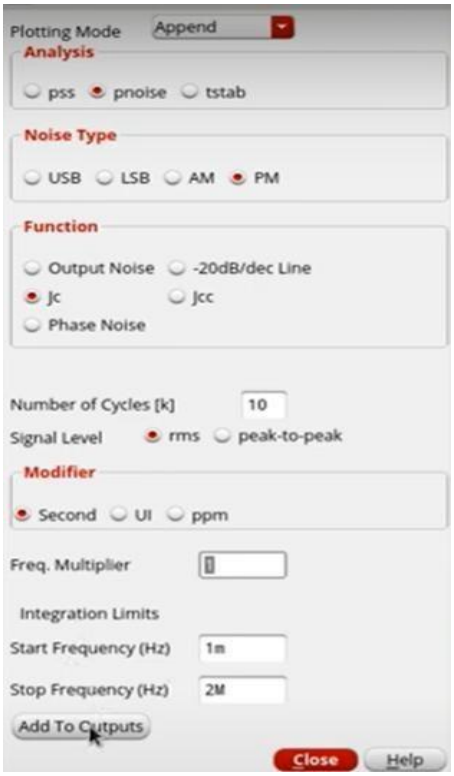


Figure 5.20: Jitter settings popup window

After settings, then click the **Close** the window button. Then click the ***run*** button in ***Maestro*** to do the simulation again. Then the waveforms will result as in figure. The jitter is recorded as 132.778Sp. The jitter noise plots are in the figure 5.21.

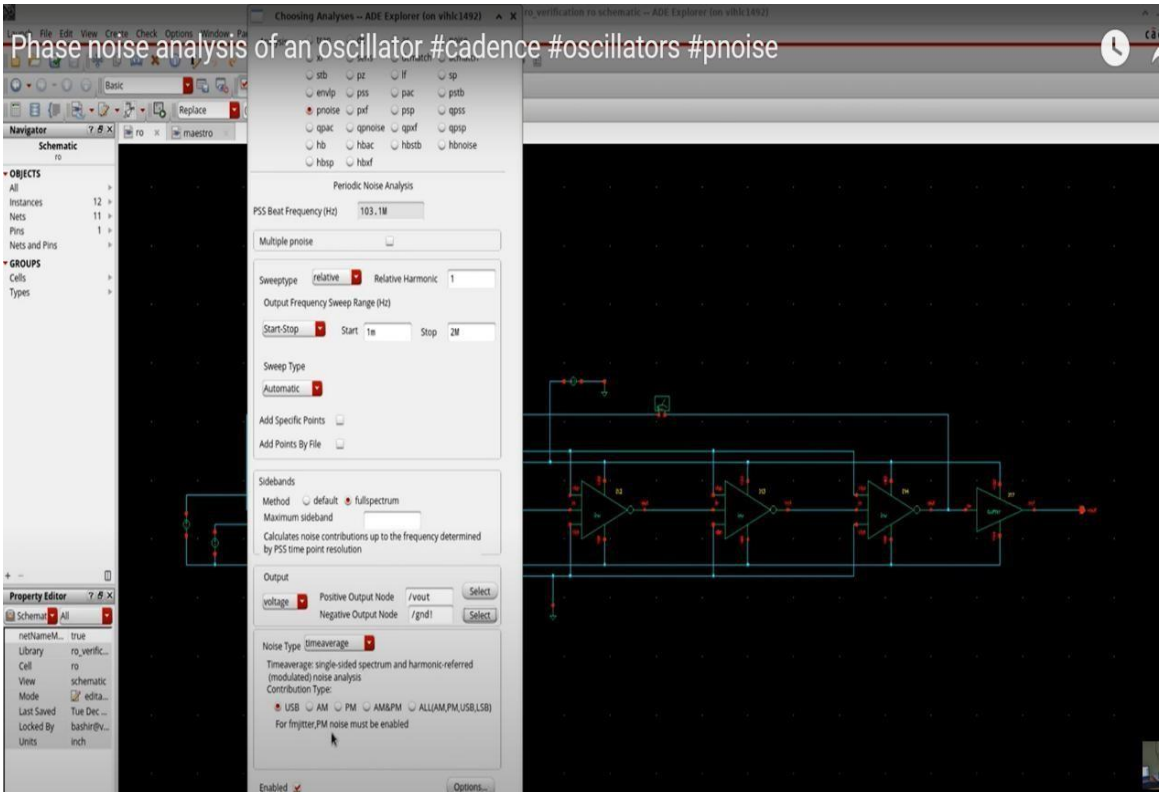


Figure 5.21: Ring oscillator Jitter

5.8.2 Power Spectrum analysis (Ring Oscillator):

Periodic Steady State (PSS) is an extension to DC analysis and is used to find the steady state frequency analysis. Click ***add analysis*** in the ADE environment after transient analysis, then choose ***PSS*** analysis. It is not a straightforward method to calculate the phase noise and needs some setups under PSS. Under the PSS analysis there are two engines such as shoot engine and Hormonic engine. Hormonic engine is the frequency domain method, easily handled if using s-parameters model. Its accuracy is limited by the number of harmonics selected and is not suitable for strongly modelled responses. Shoot engine is the time domain method, time setup should be enough to simulate maximum frequency response. It can't handle frequency domain models. The figures 5.22 and figure 5.23 show the popup windows for setting the PSS analysis. Figure 5.24 shows the periodic steady state response of the ring oscillator.

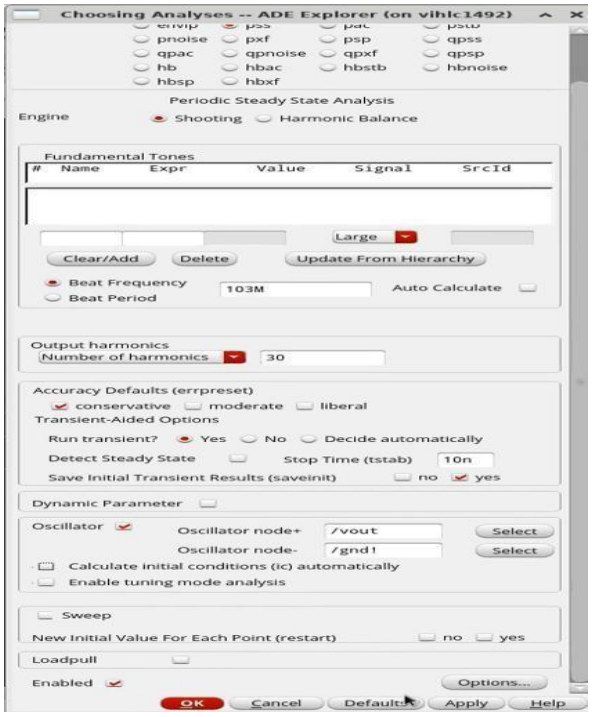


Figure 5.22: Periodic Steady State setting window

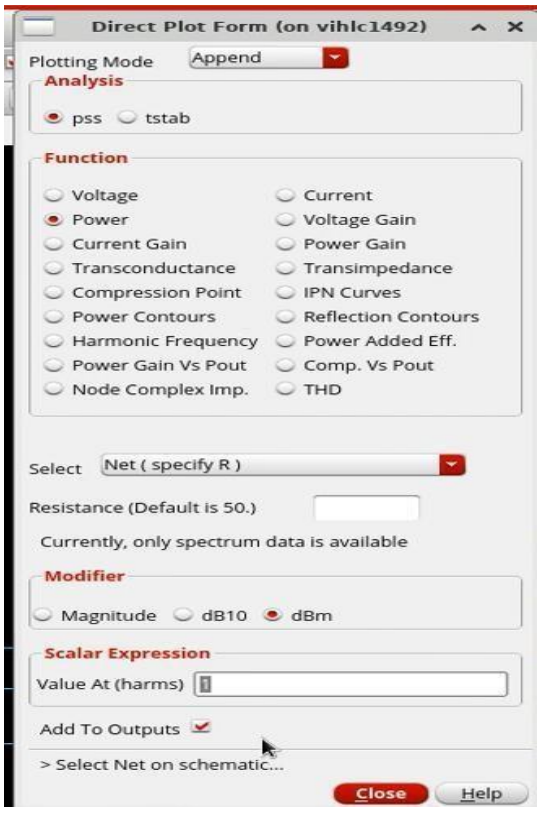


Figure 5.23: Direct plot form window

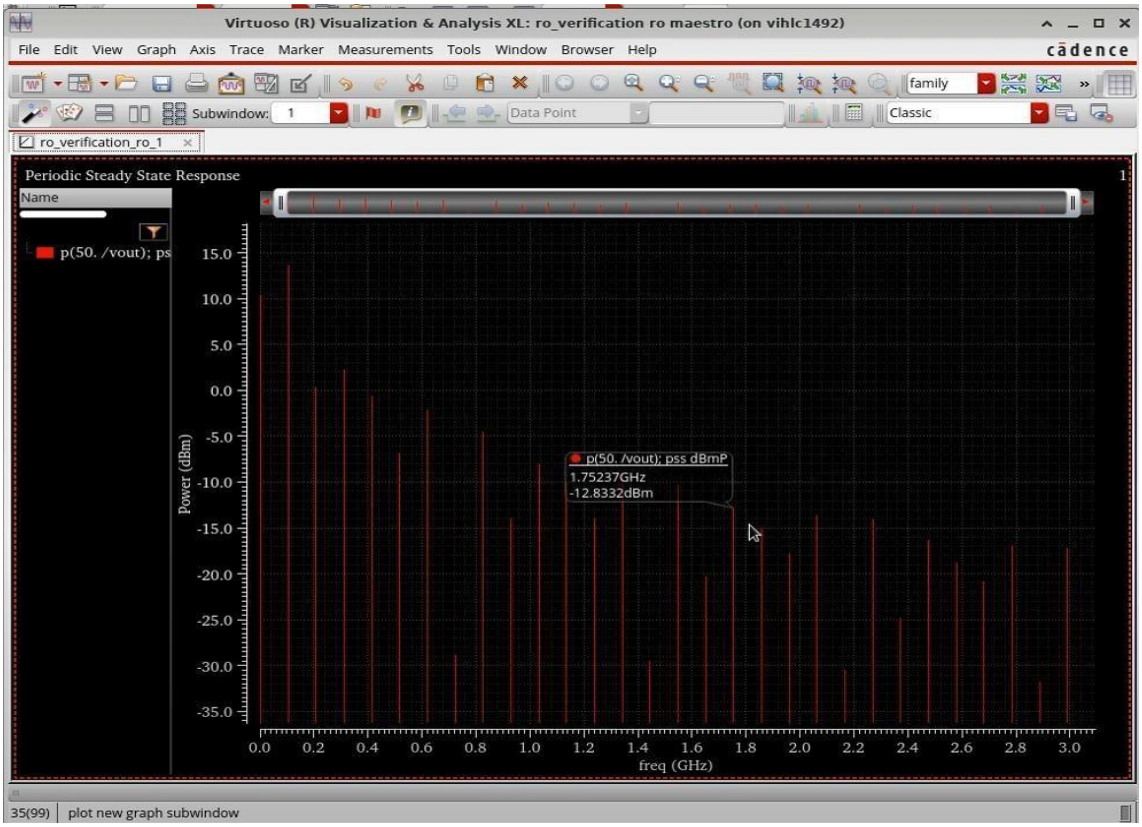


Figure 5.24: Periodic Steady State response plot

In this thesis, the five stage CMOS Ring Oscillator with 1V power supply, the frequency of oscillations fosc=7.6 GHz and Phase noise is PN= -105 dB/Hz @ 2GHz. Whereas five stage Fin FET based Ring Oscillator with 1V power supply, the oscillating frequency is fosc=1.79 GHz and the phase noise PN= -81 dB/Hz @1.54Ghz.

Table 5.1 presents a comparison of the proposed ring oscillator designs with similar existing works. The table focuses on key performance metrics: frequency, power consumption, and area.

Table 5.1: The performance comparison of ring oscillator circuits.

	Process (nm)	Freq (GHz)	Power (µW)	Phase noise (dBc/Hz)	Area ($\mu m^{2)}$	Supply (V)
[87] 9 stage RO	20	4.0	264	-125@1.2GHz	1002.89	1.0
[86] 3 stage RO	45	2.5	82.76	-100@1GHz	972	1.2
FinFET based -3 stage RO	18	44.085	5.022	-105@1.5GHz	392.77	1.0
FinFET based -5 stage RO	18	8.1	10.4	-81.5@1.5GHz	512.21	1.0
FinFET based -21 stage RO	18	89.12M	51	-77.8@1.5GHz	1492.89	1.0

5.9 CONCLUSIONS

The 18 nm Fin-FET inverter has been designed in chapter 4. With this FinFET inverter circuit three, five and twenty-one stage ring oscillators were implemented. Through the transient, DC and AC analysis, measured frequency of oscillations and power. Frequency of oscillations are noticed as 13.7 GHz, 7.9 GHz and 4.9 GHz respectively. The power valuesare 3.9µW,10.9µW and 51µW respectively.

CHAPTER6

CONCLUSIONS & FUTURE SCOPE

Thesis conclusion remarks and the extension of this research are discussed in this chapter.

Different low power techniques applied to the basic CMOS inverter and designed on different technology nodes such as 180 nm, 90 nm, 65 nm, and 45 nm. The simulations were performed on them to evaluate their performance metrics such as power, delay and area. From this analysis the conclusion is sleepy keeper and zig zag dVth schemes outperform than other schemes. Then, a five-stage ring oscillator is implemented with sleepy keeper technique and find the following:

(a) As the technology node shrinks from 180 nm to 45 nm, significant improvements in delay and area are observed i.e lower technology nodes offer small delays, low dynamic power and less space. Compared to other schemes sleepy keeper techniques offer at max 10% dynamic power saving, 3.5% less space and 5.2% less delay. But it produces 2% more static power.

(b) The sleepy keeper and zigzag dVth consistently outperformed other techniques in terms of overall performance. Compared to the base case, the sleepy stack and sleepy keeper methods achieved substantial reductions in static and dynamic power consumption.

(c) **Performance Trade-offs:** While the dual Vth techniques offer significant power savings, they might introduce additional area overhead and slightly increase delay compared to other methods. Five stage ring oscillator with sleepy keeper approach produced the frequency of oscillations as 1.27GHz.

(d) Because of SCEs at 45nm technology, the designs at 45 nm node produced more static power when compared to 180nm node. The work focus is diverted to new devices. To reduce these short channel effects, an 18 nm Fin-FET inverter implemented, power and delayare measured.

(e) Three stage, five stage and twenty-one stage ring oscillator circuits implemented with Fin-FET technology. Through the transient, DCand AC analysis, measured frequency of oscillations and power. The oscillations frequency of three stage circuit is 44. 08 GHz, five stage circuit is 8.1 GHz and 21 stage circuit is 4.9 GHz. The power consumption of three stage circuit is 4.02 µW, five stage circuit is 5.02 µW. and 21 stage circuit is 51µW. The delay of three stage circuit is 217.5 nsec., five stage circuit is 661.19 nsec. and 21 stage circuit is 2 nsec.

(f) From three stages to five stages, the frequency decreased by 81.6%, 67% of delay increased and 2% power increased.

Future scope of this thesis: SG-Fin-FET is implemented with Verilog A to implement the ring oscillator. Full custom Fin-FET design with TCAD tool may give better characteristics, hence it is suggested that go this way to enhance the frequency stability, better power reduction with optimum tradeoff between power and delay.

APPENDIX

Verilog A model for Double Gate MOSFET (tied mode)

```
// VerilogA, id_test, veriloga//

`include "constants.vams"
`include "disciplines.vams"

`define T                273.15
`define q                1.60217e-19
`define k_b              1.3806505e-23
`define eps_si           1.03593374589e-12
`define eps_ox           3.45211124863e-13
`define phi              3.14
`define u                300

 module id_test(D,FG,S,BG);
inout D,FG,S,BG;
 electrical D,FG,S,BG;

branch (FG,S) b_FGS;
branch (BG,S) b_BGS;
branch (D,S) b_DS;
branch (S,S) b_SS;

 `ifdef _VAMS_COMPACT_MODELING_
  electrical noi_filt,nor_corr;
 `endif

      parameter real N_a  = 1e15;
```

```
        parameter real n_i  =  1.5e10;
        parameter real tox  =  25e-7;
        parameter real tsi  =  1.5e-5;
        parameter real vt   =  25e-3;
        parameter real Lg       10e-7;

analog function real phi_b;
input N_a,n_i;
real N_a,n_i;
begin
            phi_b = (`k_b*`T*log(N_a/n_i))/`q;
end
endfunction
analog function real vbg_bar;
input vbg,vbg_fb;
real vbg,vbg_fb;
begin
vbg_bar = vbg-vbg_fb;
end
endfunction
analog function real vfg_bar;
input vfg,vfg_fb;
real vfg,vfg_fb;
begin
            vfg_bar = vfg-vfg_fb;
end
endfunction
analog function real x;
input Lg;
real Lg;
begin
            x = Lg/2;
```

```
end
endfunction
analog function real Ldi;
input n_i;
real n_i;
begin
        Ldi = sqrt((2*`eps_si*`k_b*`T)/`q/`q/n_i);
end
endfunction
analog function real cox;
input tox;
real tox;
begin
        cox  = `eps_ox/tox;
end
endfunction
analog function real r;
input tox,tsi;
real tox,tsi;
begin
        r =  (2*`eps_si*tox)/(`eps_ox*tsi);
end
endfunction
analog function real F_d;
input vfg,vds,tsi,n_i;
real vfg,vds,tsi,n_i;
begin
        F_d = (`q*(vfg-vds)/(2*`k_b*`T)-ln(2*Ldi(n_i)/tsi));
end
endfunction
analog function real F_s;
input vfg,vs,tsi,n_i;
```

```
real vfg,vs,tsi,n_i;
begin
        F_s = (`q*(vfg-vs)/(2*`k_b*`T)-ln(2*Ldi(n_i)/tsi));
end
endfunction
analog function real bta;
input vg,vx,tsi,tox;
real vg,vx,tsi,tox;
real x_1,x_2,x_3,z_1,g_1,g_2,d_2,n_0,n_1,n_2,n_3;
real z_2,g_3,d_3,l_0,l_1,l_2,l_3,z_3;
begin
        //step1//
      x_1 = 8/(`phi*`phi*r(tox,tsi)*r(tox,tsi));
      x_2 = 4/(`phi*r(tox,tsi));
      x_3 = ln(1+exp(F(vg,vx,vt)/2));
      z_1 = pow((x_1*x_1+x_2*x_2*x_3*x_3),0.5)-x_1;
//step2//
      g_2 = atan(z_1);
      d_2 = 1/(1+z_1*z_1);
      n_0 = 0.5*ln(g_2*g_2/d_2)+r(tox,tsi)*z_1*g_2-F(vg,vx,vt);
      n_1 = (d_2/g_2)+(1+r(tox,tsi))*z_1*d_2+r(tox,tsi)*g_2;
            -(d_2*d_2)/(g_2*g_2)-(2*z_1*d_2*d_2/g_2)+(1+2*r(tox,tsi)-
            z_1*z_1)*d_2*d_2;



            2*d_2*d_2*d_2/(g_2*g_2*g_2)+(6*z_1*d_2*d_2*d_2)/(g_2*g_2
            )+(6*z_1*z_1-2)*(d_2*d_2*d_2)/(g_2)+(2*z_1*z_1-6-
            8*r(tox,tsi))*z_1*d_2*d_2*d_2;


            z_1-(n_0/n_1)*(1+(n_0*n_2)/(2*n_1*n_1)+
```

```
                n_0*n_0*(3*n_2*n_2-n_1*n_3)/(6*n_1*n_1*n_1*n_1));



    //step 2//
     g_3 = atan(z_2);
     d_3 = 1/(1+z_2*z_2);
     l_0 = 0.5*ln(g_3*g_3/d_3)+r(tox,tsi)*z_2*g_3-F(vg,vx,vt);
     l_1 = (d_3/g_3)+(1+r(tox,tsi))*z_2*d_3+r(tox,tsi)*g_3;
                -(d_3*d_3)/(g_3*g_3)-(2*z_2*d_3*d_3/g_3)+(1+2*r(tox,tsi)-
                z_2*z_2)*d_3*d_3;



                2*d_3*d_3*d_3/(g_3*g_3*g_3)+(6*z_2*d_3*d_3*d_3)/(g_3*g_3
                )+(6*z_2*z_2-2)*(d_3*d_3*d_3)/(g_3)+(2*z_2*z_2-6-
                8*r(tox,tsi))*z_2*d_3*d_3*d_3;



                z_2-(l_0/l_1)*(1+(l_0*l_2)/(2*l_1*l_1)+l_0*l_0*(3*l_2*l_2-
                l_1*l_3)/(6*l_1*l_1*l_1*l_1*l_1));



bta = atan(z_3);
end
endfunction

real vfg,vbg,vg,vds,vsd,vs,VFG,VDS,VBG,VS,VD;
real bta_d,bta_s,bta_sum,bta_diff,bta_avg;
real psi_s,psi_d,psi_mid,del_psi;
```

```
real gr_s,gr_d,gr_change;
real qis,qid,qi_mid,q_inv_mid,gm,gds,gn,kx,v_ox_mid,vx;
real alpha_dr,alpha_nr,yn,alpha,H,QG,QD,QS,c_DD,c_GD,c_SD;
real c_DG,c_SG,c_GG2,c_GG;
real c_dgn,c_ggn,c_sgn,c_ddn,c_gdn,c_sdn;
real pbi,vbi,vbg_bar,vfg_bar,lmda_y,delta_y;
real eta_s,eta_d,Ay,By,psi,pshi_d,psi_min,A,B,C,vthl,vths,vth,m1,wdm;
real psi_xys,psi_xyd,psi_xym,idw;
real idwi,idsi;
real Ld;

analog begin
vfg = V(FG,S);
vbg = V(BG,S);
vds = V(D,S);
vs = V(S);
vg = vfg;
vsd = V(S,D);
Ld = Ldi(n_i,vt);

        bta_s = bta(vg,vs,tsi,tox);
        bta_d = bta(vg,vds,tsi,tox);
        bta_sum = bta_s+bta_d;
        bta_diff = bta_s-bta_d;
        bta_avg = 0.5*(bta_s*bta_s+bta_d*bta_d);
        psi_s =  vs-(2*vt)*ln(tsi/(2*Ld*bta_s)*cos(2*bta_s*x(tsi)/tsi));
        psi_d = vds-(2*vt)*ln(tsi/(2*Ld*bta_d)*cos(2*bta_d*x(tsi)/tsi));
        psi_mid=0.5*(psi_s+psi_d);
        del_psi = psi_d-psi_s;
        gr_s = bta_s*tan(bta_s)-
    (bta_s*bta_s)/2+r(tox,tsi)/2*bta_s*bta_s*tan(bta_s)*tan(bta_s);
        gr_d = bta_d*tan(bta_d)-(bta_d*bta_d)/2+r(tox,tsi)/2*bta_d*bta_d*
```

```
 tan(bta_d)*tan(bta_d);
gr_change = gr_s-gr_d;
v_ox_mid = vg-(psi_mid);
qis = bta_s*tan(bta_s);
qid = bta_d*tan(bta_d);
qi_mid = 0.5*(qis+qid);
q_inv_mid = 8*csi(tsi)*vt*qi_mid;
gm = `u*(W/Lg)*8*csi(tsi)*vt*(qis-qid);
 gds = `u*(W/Lg)*8*csi(tsi)*vt*qid;
gn =(1-bta_sum*bta_diff/(qis-qid))/qi_mid;
kx = 1+gn/(2*r(tox,tsi));
vx = 2*kx*v_ox_mid;
alpha_dr = (q_inv_mid*q_inv_mid+q_inv_mid+bta_avg)*(q_inv_mid*
 q_inv_mid+q_inv_mid+bta_avg)*(q_inv_mid*q_inv_mid+q_inv_m
 id+bta_avg);
alpha_nr = q_inv_mid*(2*(q_inv_mid*q_inv_mid)+2*(bta_avg)-
 1)+q_inv_mid*q_inv_mid+bta_avg;
yn = alpha_nr/alpha_dr;
alpha = 2+(1.5/r(tox,tsi))*q_inv_mid*yn;
H = (vx+2*vt)/alpha;
 QG = 2*cox(tox)*W*Lg*(v_ox_mid+(del_psi*del_psi)/(12*H));
 QD = -2*cox(tox)*W*Lg*(v_ox_mid/2-(del_psi/12)*(1-del_psi/(2*H)-
 (del_psi*del_psi)/(20*H*H)));
 QS = QG+QD;
c_GD = -(Lg*Lg*gds*gds/idsi)/`u+(QG*gds/idsi);
c_DD = -(Lg*Lg*gds*gds/idsi)/`u-(2*QD*gds/idsi);
c_SD =  c_DD-c_GD;
c_GG = -(Lg*Lg*((gm+gds)*(gm+gds)-gds*gds))/(`u*idsi)+(QG)/idsi*gm;
c_DG = -(Lg*Lg*gds*gds)/(`u*idsi)+(QG/idsi)*(gm+gds)+(QD*2/idsi)*gm;
c_SG = c_GG+c_DG;
vbi= (`k_b*`T/`q)*ln(N_d*N_a/n_i/n_i);
pbi = (`k_b*`T/`q)*ln(N_a/n_i);
```

```
        vbg_bar = vbg-vbg_fb;
        vfg_bar = vfg-vfg_fb;
        lmda_y = sqrt(`eps_si/(2*`eps_ox)*(1+(`eps_ox/`eps_si)*(x(tsi)/tox)-
         (`eps_ox/`eps_si)*x(tsi)*x(tsi)/tox/tsi)*tox*tsi);
delta_y = (`q*N_a*lmda_y*lmda_y/`eps_si)+(vfg_bar-vbg_bar)/
            ((2*`eps_si*tox+`eps_ox*tsi)/(`eps_si*tox+`eps_ox*x(tsi)))-vfg_bar;
        eta_s = vbi+delta_y;
        eta_d = vbi+vds+delta_y;
        A = (2*(sinh(Lg/lmda_y))-1)/(sinh(Lg/lmda_y)*(sinh(Lg/lmda_y)))-1;
        B = (2*(sinh(Lg/lmda_y))*(eta_d+eta_s)-2*(eta_d+eta_s))/
         (sinh(Lg/lmda_y)*sinh(Lg/lmda_y))-4*pbi;
        C = ((2*sinh(Lg/lmda_y)*eta_d*eta_s)-(eta_d*eta_d+eta_s*eta_s))/
         (sinh(Lg/lmda_y)*sinh(Lg/lmda_y))-4*pbi*pbi;
        Ay = (eta_d-eta_s*exp(-(Lg)/lmda_y))/(1-exp(-2*Lg/lmda_y));
        By = (eta_s-eta_d*exp(-Lg/lmda_y))/(1-exp(-2*Lg/lmda_y));
        psi = (eta_s*sinh(Lg/2/lmda_y)+eta_d*sinh(Lg/2/lmda_y))
         /sinh(Lg/lmda_y)-delta_y;
        psi_min = 2*(sqrt(Ay*By))-delta_y;
vthl = vfg_fb-(`eps_si*tox*vbg_bar)/(`eps_si*tox+`eps_ox*tsi)
         +((2*`eps_si*tox+`eps_ox*tsi)/(`eps_si*tox+`eps_ox*tsi))*
         (`q*N     _a*tox*tsi/(2*`eps_ox)+2*pbi);
vths =  vfg_fb-(`eps_si*tox*vbg_bar)/(`eps_si*tox+
`eps_ox*tsi)+((2*`eps_si*tox+`eps_ox*tsi)/(`eps_si*tox+`eps_ox*tsi))*(`q*N_a*tox*tsi/(2*`eps_
ox)-(-B+sqrt(B*B-4*A*C))/2*A);
vth = (2*`eps_si*tox+`eps_ox*tsi)/(`eps_si*tox+`eps_ox*tsi)
         *(2*pbi-(-B+sqrt(B*B-4*A*C))/2*A);
        psi_xys =psi_s+psi;
        psi_xyd = psi_d+psi;
psi_xym = 0.5*(psi_xys+psi_xyd);
        m1 = 1+3*tox/wdm;
wdm =sqrt(4*`eps_si*`k_b*`T/`q/`q/N_a*ln(N_a/n_i))/1e3;
idwi = `u*cox(tox)*(W/Lg)*(m1-1)*(`k_b*`T/`q)*(`k_b*`T/`q)*exp((vg-
```

```
        vths)/m1/vt)*(1-exp(-vds/vt));
      I(D,S) <+ ids;
end
endmodule
```

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