ANALYSIS AND MINIMIZATION OF LOSSES IN MULITLEVEL INVERTER USING VARIOUS MODULATION TECHNIQUES

Thesis Submitted for the Award of the Degree of

DOCTOR OF PHILOSOPHY

in

Electrical Engineering

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2026

DECLARATION

I, hereby declared that the presented work in the thesis entitled "**ANALYSIS AND MINIMIZATION OF LOSSES IN MULTILEVEL INVERTER USING VARIOUS MODULATION TECHNIQUES** " in fulfillment of degree of **Doctor of Philosophy (Ph.D.)** is outcome of research work carried out by me under the supervision of **Dr HIMANSHU SHARMA**, working as **ASSISTANT PROFESSOR** , in the School of Electronics and Electrical Engineering of Lovely Professional University, Punjab, India. In keeping with general practice of reporting scientific observations, due acknowledgements have been made whenever work described here has been based on findings of other investigator. This work has not been submitted in part or full to any other University or Institute for the award of any degree.

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CERTIFICATE

This is to certify that the work reported in the Ph.D. thesis entitled "**ANALYSIS AND MINIMIZATION OF LOSSES IN MULTILEVEL INVERTER USING VARIOUS MODULATION TECHNIQUES**" submitted in fulfillment of the requirement for the award of degree of **Doctor of Philosophy (Ph.D.)**in the School of Electronics and Electrical Engineering, is a research work carried out by **HARESH NANDA** ,Registration No **42000180** , is bonafide record of his original work carried out under my supervision and that no part of thesis has been submitted for any other degree, diploma or equivalent course.

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ABSTRACT

In recent years, the demand for densestructurepower converters has surged, particularly for submissionssuch ashigh-frequencyAC systems, active power filters,and photovoltaicsystems. To meet these needs, multilevel inverters (MLIs) have been introduced, offering improved performance in power electronics. This researchapplies afreshtechniqueto MLI design through a reduced-component switched-capacitor MLI. Utilizing a single input source and strategic series-parallel arrangements of capacitors, the proposed design achieves a four-time step-up in output voltage. The effective management of capacitor charging and discharging within each cycle results in naturally balanced voltages and minimized component stress. Detailed analysis and comparisons confirm the efficiency and operational robustness of the proposed MLI across various scenarios, including changes in modulation index and load.

This work also introduces a Static Synchronous Compensator (STATCOM) depending on the proposed nine-level switched capacitor MLI to enhance dynamic stability and power quality in recent power schemes. By optimizing the settlement of the STATCOM using the green anaconda optimization (GAO) method, the inverter is positioned for maximum impact on power loss reduction and quality improvement. The design demonstrates substantial improvements in efficiency and voltage balancing with fewer switches, as validated by MATLAB/Simulink simulations. Additionally, the novel inverter achieves a low total harmonic distortion (THD) of 1.04% and an efficiency of 99.02%, showcasing its effectiveness under different faulty conditions. This innovative approach to power electronics paves the way for more efficient, reliable, and high-performing systems

The EDL_KDF model leverages a deep explainable distillation approach with SHapley Additive Explanations (SHAP) to forecast at-risk students and provide strategies for early intervention. By combining the knowledge distillation framework with improved data augmentation techniques, the model achieves 99.6% accuracy and 99.21% precision over the OULAD dataset. The work supports educational institutions' efforts to improve teaching quality, enhance students' academic success, and optimize Virtual Learning Environments (VLEs).

PREFACE/ACKNOWLEDGMENTS

All praise goes to **Bhagwan Shree SatyaSai Ram** who gave me power and the strength to start a journey towards accomplishing this task. May His infinite mercy be upon us.

I would like to give my sincere thanks to my supervisor **Dr. Himanshu Sharma**, Assistant Professor, School of Electronics & Electrical Engineering, Lovely Professional University, Phagwara Jalandhar Punjab, India from the bottom of my heart and with great respect, and Co-supervisors **Dr. Kamaldeep**, Assistant Professor, Electrical Engineering, Sri Mata Vaishno Devi University Jammu for their guidance, encouragement and valuable suggestions throughout my research work.

Dr. Himanshu Sharma has an optimistic personality with a helpful nature, he has always made himself ready to clarify my doubts and motivate me every moment, and it was a great opportunity to work under his supervision. Whenever I felt like I was getting nowhere with my research goals, he would always provide clarity. Their diligent work, systematic approach, and one-on-one assistance allowed me to finish this research project on scheduled time.

I want to thank everyone at Lovely Professional University for providing the necessary resources and setting so that I could finish my research project on schedule. Also, I like to thank the Division of Research & Development and the School of Electronics and Electrical Engineering for efficient help and encouragement in my entire Ph.D. journey.

I am deeply grateful to my mother **Smt N Rangamma** for her abundant blessings, consistent support, sacrifices, and unwavering faith in my capabilities. Her steadfast support has been the foundation upon which my academic aspirations have flourished.

I am indebted to my uncle **Dr K.V. Ramana Rao (M.D)**, who has always supported and cooperated with me during the challenging times while conducting research work.

Date: 13-02-2026 HARESH NANDA

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ABBREVATIONS

ASMLI	A five-level asymmetric stacked multilevel inverter
CF	Cost Function
CHBMLI	Cascaded H-Bridge MLI
CSI	current source inverters
DCMLI	Diode Clamped MLI
DCMLI	Diode Clamped Multilevel Inverter
DSP	Digital signal processor
D-STATCOM	Distribution-static synchronous compensator
FCMLI	Flying Capacitor MLI
FCs	Floating capacitors
GAO	Green anaconda optimization
GTOs	Gate Turn-Off thyristors
HVDC	High-Voltage Direct Current
HVDC	High Voltage Direct Current
MLI	Non-conventional Multilevel Inverter
MLI	Multilevel Inverter
MLIs	Multilevel inverters
MOA	Mayfly optimization algorithm
OCF	Open circuit fault
PWM	Hybrid Pulse Width Modulation
SC	Switched-capacitor
SCCs	Switched-capacitor circuits
SHAP	SHapley Additive Explanations
SHE	Selective Harmonic Elimination
STATCOM	Static Synchronous Compensator
THD	Total harmonic distortion
TVS	Total Voltage Stress

VLEs	Virtual Learning Environments
VSI	Voltage source inverters

ABSTRACT

In recent years, the demand for compact design power converters has surged, particularly for applications such as photovoltaic systems, active power filters, and high-frequency AC systems. To meet these needs, multilevel inverters (MLIs) have been introduced, offering improved performance in power electronics. This paper presents a novel approach to MLI design through a reduced-component switched-capacitor MLI. Utilizing a single input source and strategic series-parallel arrangements of capacitors, the proposed design achieves a four-time step-up in output voltage. The effective management of capacitor charging and discharging within each cycle results in naturally balanced voltages and minimized component stress. Detailed analysis and comparisons confirm the efficiency and operational robustness of the proposed MLI across various scenarios, including changes in modulation index and load.

This work also introduces a Static Synchronous Compensator (STATCOM) based on the proposed nine-level switched capacitor MLI to enhance dynamic stability and power quality in modern power systems. By optimizing the placement of the STATCOM using the green anaconda optimization (GAO) method, the inverter is positioned for maximum impact on power loss reduction and quality improvement. The design demonstrates substantial improvements in efficiency and voltage balancing with fewer switches, as validated by MATLAB/Simulink simulations. Additionally, the novel inverter achieves a low total harmonic distortion (THD) of 1.04% and an efficiency of 99.02%, showcasing its effectiveness under different faulty conditions. This innovative approach to power electronics paves the way for more efficient, reliable, and high-performing systems.

The EDL_KDF model leverages a deep explainable distillation approach with SHapley Additive Explanations (SHAP) to forecast at-risk students and provide strategies for early intervention. By combining the knowledge distillation framework with improved data augmentation techniques, the model achieves 99.6% accuracy and 99.21% precision over the OULAD dataset. The work supports educational institutions efforts to improve teaching quality, enhance students academic success, and optimize Virtual Learning Environments (VLEs).

CHAPTER 1

INTRODUCTION

1.1 Overview

The rising demand for electrical energy has led to a depletion of fossil fuels, prompting the need for action to increase their lifespan. In the existing research, two prominent approaches have been identified to address this challenge [1]. Firstly, existing energy resources must be utilized efficiently. Secondly, there should be a greater emphasis on the use of renewable energy sources such as photovoltaic, wind, geothermal, or nuclear power [2]. From a technical perspective, power electronic converters play a crucial role in achieving these goals with high efficiency. One common power electronic converter, the DC-to-AC converter (inverter), is used to generate an AC waveform from DC input sources [3]. However, traditional inverters often produce square waveforms containing all odd harmonics, which can degrade the quality of the output waveform. To mitigate this issue, low-pass filters are essential to eliminate these harmonics and improve waveform quality [4].

Additionally, for high-power applications where a single switch cannot handle higher voltages, Multilevel Inverters (MLIs) have emerged as a suitable solution. MLIs offer several advantages over traditional two-level inverters, including reduced voltage stress on power switching devices and improved efficiency. The basic configurations of MLIs include Diode Clamped MLI, Flying Capacitor MLI, and Cascaded MLI, each offering unique features and facing specific challenges. Increasing the number of levels in an MLI can enrich the output waveform quality, and employing appropriate switching strategies can further enhance their performance in terms of charge balancing, energy efficiency, power factor, and voltage stress reduction. Various modulation techniques have been introduced to improve the overall performance of MLIs, addressing specific application requirements and operational constraints [5, 6].

In recent years, MLIs have found widespread use across various industries and applications. They are employed in power-quality devices, traction systems, renewable energy utilization, automotive applications, energy transmission, uninterruptible power supplies, industrial drives, mining operations, marine propulsion, conveyors, and medical equipment such as MRI systems. The versatility and effectiveness of MLIs make them indispensable components in modern power systems, enabling efficient energy conversion and utilization

across a diverse range of applications [7]. However, Switched-capacitor (SC)-based circuits have emerged as a popular technique among various families of improved MLIs. These circuits utilize capacitors, power switches, and/or diodes to convert a fixed DC-link voltage into multilevel voltage outputs using a series–parallel switching conversion technique [8]. In pure SC-based switching circuits, multiple capacitors are integrated to generate discrete output voltages by charging and discharging them in series or parallel fashion, either with or without the input DC source. This single-stage operation, which does not require inductors or transformers, facilitates voltage step-up and ensures self-voltage balancing among the capacitors [9]. Consequently, SC-MLIs offer an attractive solution for a wide range of applications, making them valuable and intriguing alternatives in modern power conversion systems. Hence in this research discusses about inverters, its classification, modulation control schemes of multilevel inverters, applications of multilevel inverters, then about the application of multilevel inverters in STATCOM applications, and switched capacitor multilevel inverters.

1.2 Inverters and its classification

Inverters play a pivotal role in converting DC voltage from various sources, including renewable energy sources (RES), into AC voltage suitable for powering electrical loads or feeding into the grid [10]. They are essential components in a wide range of applications such as battery storage systems, High-Voltage Direct Current (HVDC) transmission lines, electric vehicles, and photovoltaic (PV) panels.

Inverters can be broadly classified into two types based on their input and output characteristics: voltage source inverters (VSI) and current source inverters (CSI), which is shown in Figure 1.1.

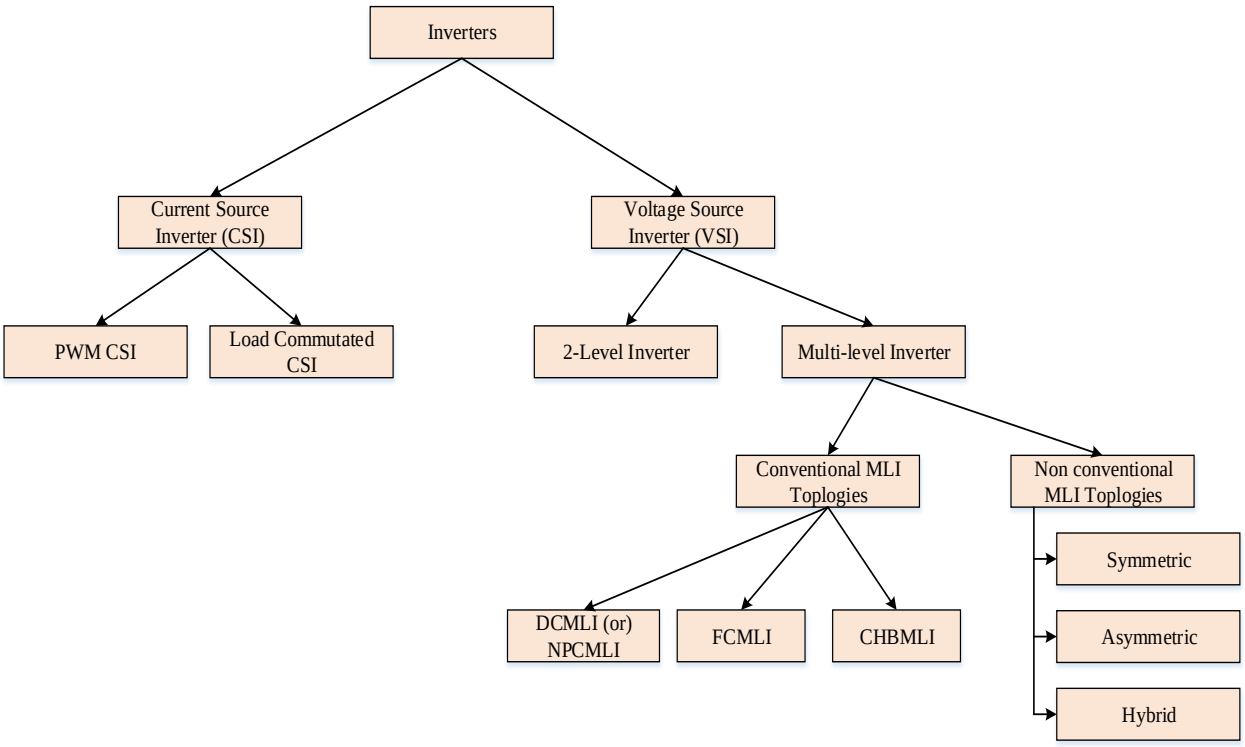


Figure 1.1: Classification of inverters

1.2.1 Voltage Source Inverters (VSI)

Voltage Source Inverters (VSIs) are a type of power electronic device used to convert a DC voltage into an AC voltage with a constant voltage input and regulated output current according to load requirements [11]. They are widely employed in applications where a stable voltage waveform is crucial, such as grid-connected systems or motor drives. In a VSI, the output voltage waveform quality is enhanced by increasing the switching frequency, which helps reduce harmonic distortion. This is essential for applications requiring high-quality AC power, as it ensures smooth operation and minimizes electrical noise. The basic circuit diagram of a two-level VSI comprises switches that alternate to generate either positive or negative output voltage levels, resulting in a square waveform. Two common types of VSIs are the 2-level inverter and the multilevel inverter.

2-Level Inverter:

In a 2-level inverter, also known as a conventional inverter, the output voltage is generated by switching the DC input voltage across the load using two switches per phase [12]. These switches typically operate in two states: ON and OFF, resulting in two voltage levels:

positive and negative. The output voltage waveform of a 2-level inverter consists of a square wave or modified sine wave, depending on the switching pattern. Despite its simplicity, the 2-level inverter suffers from high harmonic distortion and limited voltage levels.

Advantages:

- Simple topology with fewer components.
- Low cost and easy implementation.
- Suitable for low to medium power applications.

Disadvantages:

- High harmonic distortion in the output waveform.
- Limited voltage levels, leading to reduced output quality.
- Not suitable for high-power applications due to higher switching losses.

Multilevel Inverter:

Multilevel inverters (MLIs) are advanced VSI topologies that generate output voltage waveforms with multiple voltage levels, typically using a series of power semiconductor switches and capacitors. By combining multiple voltage levels, MLIs can achieve lower harmonic distortion, reduced voltage stress on switches, and improved output waveform quality compared to 2-level inverters. Common types of MLIs include diode-clamped (neutral-point-clamped), flying capacitor, and cascaded H-bridge inverters, which are discussed in section 1.4.

Advantages:

- Reduced harmonic distortion in the output waveform.
- Improved output waveform quality, closer to sinusoidal.
- Lower voltage stress on switches, leading to improved reliability.
- Suitable for high-power applications and grid-connected systems.

Disadvantages:

- Increased complexity due to a larger number of components.
- Higher cost compared to 2-level inverters.
- More sophisticated control algorithms are required.

Hence, while 2-level inverters are simpler and more cost-effective, they suffer from limitations such as high harmonic distortion. Multilevel inverters offer improved output waveform quality and reduced harmonic content, making them more suitable for high-power applications where power quality is critical. The choice between the two depends on factors such as the application requirements, cost constraints, and desired output waveform quality.

1.2.2 Current Source Inverters (CSI)

Current Source Inverters (CSI) are a type of power electronic device used for converting DC power into AC power [13]. They differ from Voltage Source Inverters (VSI) in that they have a constant current output on the AC side, while the VSI has a constant voltage output. CSIs are commonly used in high-power applications, such as motor drives, traction systems, and renewable energy systems. There are two main types of CSIs: Pulse Width Modulation (PWM) CSI and Load Commutated CSI.

PWM CSI (Pulse Width Modulation CSI):

In PWM CSI, the switching of the power semiconductor devices is controlled using pulse width modulation techniques. The modulation index, which represents the ratio of the peak value of the fundamental output voltage to the amplitude of the triangular carrier waveform, determines the output voltage magnitude. PWM CSI provides precise control over the output voltage and frequency, making it suitable for various applications requiring high-quality power, such as motor drives and grid-connected systems.

Advantages:

- Precise control over output voltage and frequency.
- Low harmonic distortion in the output waveform.
- High efficiency.
- Suitable for variable-speed drives and grid-connected systems.

Disadvantages:

- Complex control algorithms.
- Higher switching losses compared to other types of CSIs.

- Requires sophisticated control hardware.

Load Commutated CSI:

Load Commutated CSI relies on the natural commutation process of the load to control the output voltage. The load, typically an inductive load like a motor, assists in commutating the current from one phase to another. This type of CSI is commonly used in high-power applications where the load characteristics facilitate natural commutation, such as high-speed railway traction systems and large industrial drives.

Advantages:

- Simplified control circuitry compared to PWM CSI.
- Reduced complexity in control algorithms.
- Higher reliability due to fewer components.
- Suitable for high-power applications with inductive loads.

Disadvantages:

- Limited control over output voltage and frequency.
- Requires specific load characteristics for proper operation.
- Limited suitability for applications requiring precise control over output parameters.

Overall, both PWM CSI and Load Commutated CSI have their own advantages and disadvantages, making them suitable for different applications based on requirements such as precision control, efficiency, and reliability. The choice between the two depends on factors such as the nature of the load, the required level of control, and the application's power rating. However, there are challenges in traditional inverters, such as Current Source Inverter (CSI) and Voltage Source Inverter (VSI), which arise due to various limitations in their design and operation:

- Limited Output Voltage Range: Both CSI and VSI have a restricted output voltage range relative to the input DC voltage. In the case of VSI, the output voltage is limited below the input DC voltage, functioning as a step-down inverter (DC to AC). Conversely, when operating as a rectifier (AC to DC), VSI behaves as a step-up

converter. This limitation restricts the flexibility of the inverter's operation and may necessitate additional circuitry to achieve desired output voltages.

- Need for Additional Circuits: When the available DC voltage is insufficient to produce the desired AC voltage at the output, an additional circuit known as a chopper (DC to DC converter) is required. The inclusion of this extra circuit increases system complexity and cost while reducing overall efficiency.
- Risk of Shoot-Through State: In both CSI and VSI, the semiconductor switches in the upper and lower legs of the inverter within the same branch must not receive gating pulses simultaneously. If this occurs, either intentionally or due to electromagnetic interference (EMI), it can lead to a shoot-through state where two or more semiconductor switches in the inverter's leg are simultaneously closed. This shoot-through state can damage the converter's circuit.
- Need for Filtering Circuits: To mitigate distorted waveforms at the output, filtering circuits comprising passive elements are necessary. These filtering circuits add complexity and increase power losses in the system, thereby reducing overall efficiency.

Additionally, both CSI and VSI share common complications:

- Limited Output Range: The output range of both CSI and VSI is limited, resulting in the output voltage being either higher or lower than the input DC voltage. Consequently, they can function as either buck or boost inverters, but they cannot replace each other.
- EMI Susceptibility: Both CSI and VSI are susceptible to electromagnetic interference (EMI) noise, which can adversely affect their operation and performance.

Addressing these challenges is crucial for improving the efficiency, reliability, and performance of traditional inverters in various applications. To overcome the limitations of conventional two-level inverters, Multilevel Inverters (MLIs) have been introduced as cutting-edge technology. MLIs consist of multiple semiconductor switches and DC sources or capacitors arranged in specific configurations to generate stepped output voltage waveforms with multiple voltage levels. By employing proper switching techniques, MLIs aim to produce waveforms closely resembling sinusoidal voltage waveforms.

The primary advantage of MLIs over traditional two-level inverters is their ability to generate multiple voltage levels, thereby reducing harmonic distortion and improving waveform quality. MLIs are classified into three main types:

- Diode Clamped MLI (DCMLI)
- Flying Capacitor MLI (FCMLI) and
- Cascaded H-Bridge MLI (CHBMLI)

These classifications are based on the topology and configuration of semiconductor switches and DC voltage sources used in the inverter circuit. MLIs offer several advantages, such as lower dv/dt stress, reduced Total Harmonic Distortion (THD), improved power quality, increased blocking voltage capability, reduced torque ripple in motor applications, higher voltage gains in RES applications, and fault-tolerant operation without voltage level reduction. MLIs can theoretically produce limitless voltage levels depending on the available DC sources, making them highly versatile and suitable for various applications across different industries. Their extensive classification is based on topological structure, including symmetric, asymmetric, and hybrid configurations, which aim to meet specific voltage level requirements with reduced semiconductor switches and improved performance metrics.

1.2.3 Conventional Multilevel Inverter

Conventional Multilevel Inverter (MLI) topologies have been developed over the years to address the need for improved waveform quality and reduced harmonic distortion in power conversion applications. One such topology, known as Diode Clamped MLI (DCMLI), was patented in 1980 [14]. In DCMLI, diodes are collectively connected at a common point, forming what is also referred to as Neutral Point Clamped MLI (NPCMLI). Another variation of DCMLI utilizes clamped capacitors instead of diodes, introduced in 1992.

In addition to DCMLI, the Cascaded H-Bridge MLI (CHBMLI) topology was developed in 1975 by cascading H-Bridge inverter cells. Unlike DCMLI, each H-Bridge unit in CHBMLI requires an individual DC source to generate multi-step output levels. This topology has found extensive applications in various industries due to its ability to achieve high-voltage outputs with reduced harmonic distortion.

The operation of these traditional MLIs relies on gate signals provided to semiconductor switches within the inverter. The generation of these gate signals is facilitated by a control circuit integrated with the inverter. Thus, the controller plays a crucial role in regulating the

operation of different conventional and non-conventional MLIs, ensuring optimal performance and efficiency in various power conversion applications.

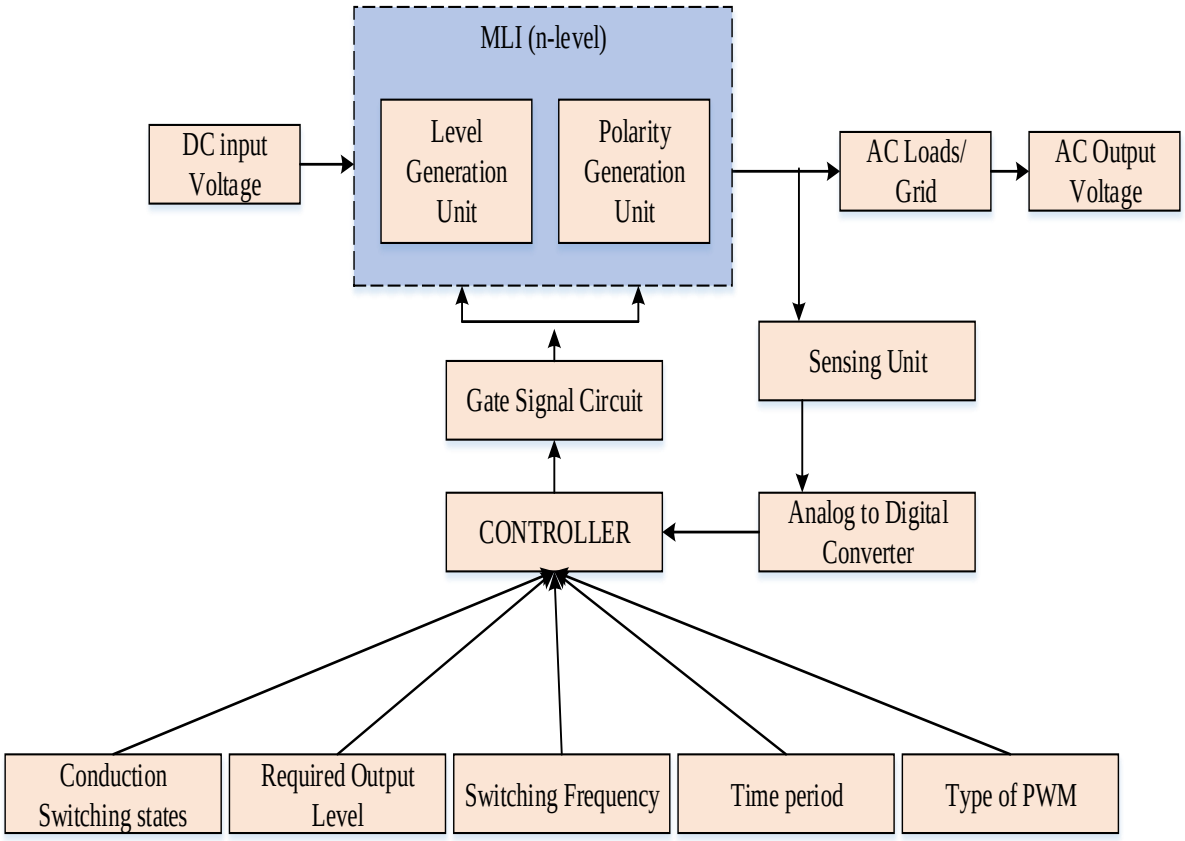


Figure 1.2: Control block diagram for MLI

1.2.3.1 Diode Clamped Multilevel Inverter (DCMLI)

The Diode Clamped Multilevel Inverter (DCMLI) is capable of generating 'n' output voltage levels using 'n-1' capacitors, 2(n-1) semiconductor switches, and (n-1)(n-2) clamping diodes. In high-power medium voltage applications, Neutral Point Clamped (NPC) inverters, a type of DCMLI, are widely utilized due to their high efficiency and ability to operate at fundamental switching frequencies [15]. One of the key advantages of DCMLI is its ability to control both real and reactive power, eliminating the need for additional filters to reduce Total Harmonic Distortion (THD). Additionally, DCMLI requires only a single DC source to produce multiple output voltage levels, simplifying the overall system architecture. However, DCMLI does have some limitations. One significant drawback is the indirect coupling between internal devices and the presence of multiple blocking voltages across the clamping diodes. An improvement to the original DCMLI topology involves serially connecting clamping diodes to share the diode voltage, addressing some of these drawbacks. One of the

primary challenges of DCMLI is voltage balancing among the DC bus capacitors. In practical applications, this limitation often restricts DCMLI to operating with only three voltage levels, reducing its overall flexibility and applicability in certain scenarios.

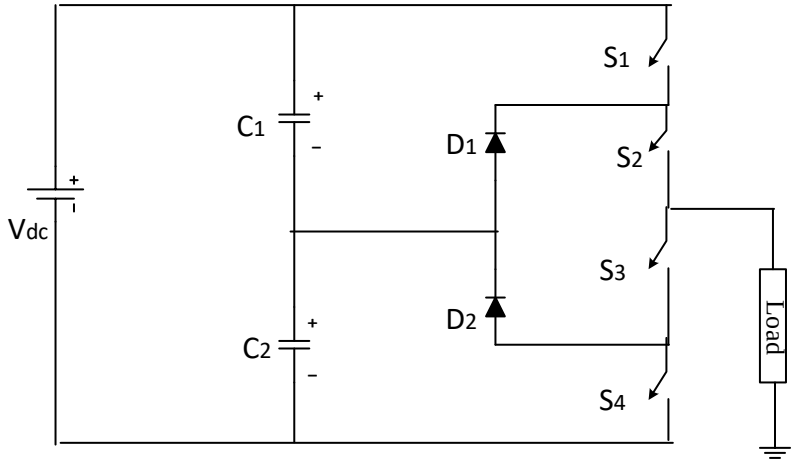


Figure 1.3: General circuit of DCMLI

1.2.3.2 Cascaded H-Bridge Multilevel Inverter (CHBMLI)

The Cascaded H-Bridge Multilevel Inverter (CHBMLI) is constructed by cascading multiple H-bridge inverter cells, earning it the nickname "Multi-cell Inverter." In this configuration, each H-bridge is independently powered by its own separate DC source on the DC side, while on the AC side, they are all connected in series. Isolated DC sources such as batteries, ultra-capacitors, or fuel cells can be employed to power each H-bridge. Each H-bridge consists of four power switches and a single DC source, as depicted in Figure 1.4. Notably, each H-bridge is capable of producing three levels of output voltage: positive, zero, and negative polarity levels [16]. The combined output voltages from each H-bridge contribute to the overall output voltage of the CHBMLI.

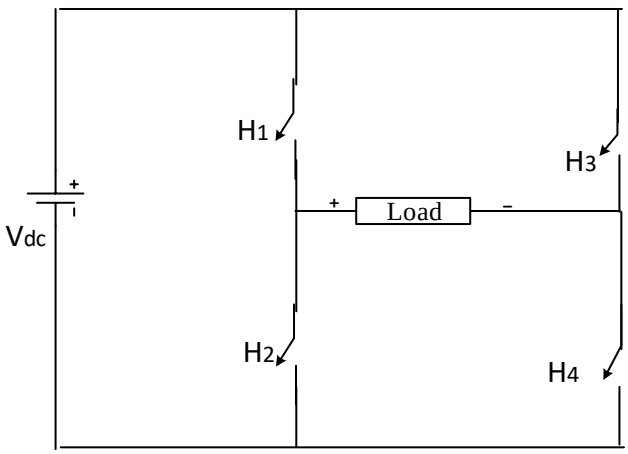


Figure 1.4: General circuit of CHBMLI

As the number of output voltage levels increases, the output waveform of the CHBMLI exhibits a sinusoidal fashion, even without the need for additional filtering. This feature enables CHBMLIs to generate high-quality output waveforms suitable for various power conversion applications.

1.2.3.3 Flying capacitor MLI

The primary distinction between the Diode Clamped Multilevel Inverter (DCMLI) and the Flying Capacitor Multilevel Inverter (FCMLI) is that the DCMLI uses diodes as clamping devices, whereas the FCMLI uses capacitors. Because of this feature, FCMLI is frequently called Capacitor Clamped MLI. A single DC source, two (n-1) semiconductor switches, (n-1)(n-2)/2 floating capacitors, and 'n-1' DC-link capacitors can all be used by FCMLI to provide 'n' output voltage levels.

The difference in voltage between neighboring capacitors determines the voltage steps at the output [17]. For example, the output voltage levels in a 3-level FCMLI arrangement are Vdc/2, 0, and -Vdc/2. Turning ON switches S1 and S2, and switches S3 and S4, creates the output voltage levels with positive and negative polarity, respectively. The switches (S1 and S3) or (S2 and S4) are switched ON in order to reach the zero-output level.

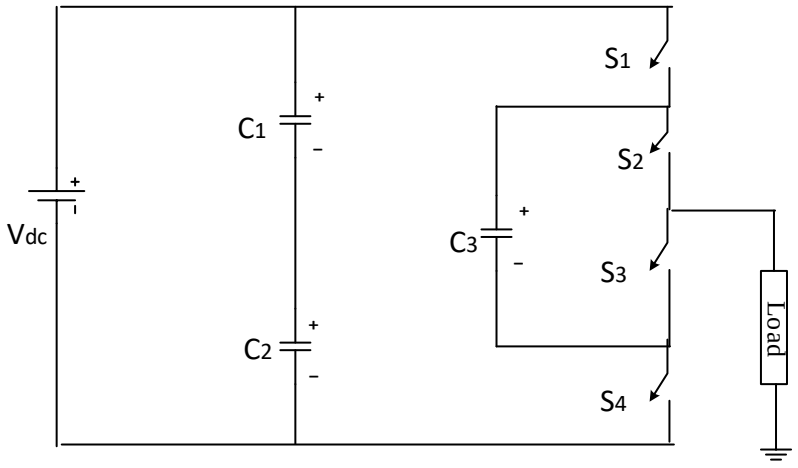


Figure 1.5: General circuit of FCMLI

Reducing voltage stress on switches improves their lifetime and dependability, which is one of FCMLI's benefits. Furthermore, FCMLI eliminates the need for large filters by enabling real and reactive power flow management. The difficulty of voltage balancing across all

capacitors is one of FCMLI's disadvantages; however, it gets worse as the number of output levels rises. Moreover, FCMLI frequently experiences greater costs and a decline in power conversion efficiency, especially when additional capacitors are needed to achieve higher output levels. Larger capacitors also make tracking the pre-charging level more difficult, which raises the system's total complexity and expense.

1.2.4 Non-conventional Multilevel Inverter (MLI)

Non-conventional Multilevel Inverter (MLI) topologies have emerged as alternatives to traditional MLIs due to their ability to address certain limitations and challenges associated with conventional configurations [18]. These non-conventional topologies feature modified structural arrangements, asymmetric DC sources, and combinations of multiple configurations, aimed at improving efficiency, reducing complexity, and lowering costs.

1.2.4.1 Symmetric MLIs

These MLIs maintain symmetry in their structural arrangements and utilize symmetric DC sources. They aim to achieve multi-step output waveforms with an 'n' number of levels while minimizing component count and complexity. Despite their symmetrical nature, symmetric MLIs may still require different Pulse Width Modulation (PWM) techniques for Total Harmonic Distortion (THD) reduction, leading to increased complexity in control scheme design.

1.2.4.2 Asymmetric MLIs

Asymmetric MLIs depart from traditional symmetrical arrangements by employing asymmetric DC sources. This allows for greater flexibility in achieving multi-step output waveforms while potentially reducing component count and circuit complexity. By utilizing asymmetric configurations, these MLIs can optimize performance and efficiency for specific applications, potentially lowering overall system costs.

1.2.4.3 Hybrid MLIs

Hybrid MLIs combine elements from multiple traditional or non-conventional configurations to create hybridized topologies. By merging different structural arrangements or incorporating features from various MLI categories, hybrid MLIs aim to leverage the strengths of each component while mitigating their respective weaknesses. This approach

enables the development of tailored solutions that optimize performance, efficiency, and cost-effectiveness for specific application requirements.

Overall, non-conventional MLI topologies represent a diverse range of innovative approaches to multilevel power conversion, offering promising alternatives to traditional configurations. These topologies provide opportunities for improved performance, reduced complexity, and enhanced cost-effectiveness in a wide range of power conversion applications.

1.3 MLI Control and Modulation Schemes

Modulation methods are essential for enhancing efficiency factors, including switching losses and harmonic reduction, as well as for regulating inverters [19]. In order to guarantee balanced voltage sources, these methods are in charge of generating reference control signals. During steady-state operation, the main goal of modulation is to produce a staircase DC voltage signal that closely matches a sinusoidal reference signal. Usually, a modulating waveform is used to manipulate several aspects of a carrier signal waveform throughout the modulation process. It is simply a method of controlling the switching action by adjusting a carrier signal's properties while referencing another signal.

The selection of a modulation technique for a specific Multilevel Inverter (MLI) family depends on several important factors, including:

- Total generated harmonics: The modulation technique should aim to minimize the total harmonic distortion in the output waveform.
- Level of distortion: It should ensure that the distortion in the output waveform is kept at a minimum level.
- Frequency of switching: The switching frequency should be optimized to balance efficiency and performance.
- Amount of losses: The modulation technique should minimize losses in the system, including conduction and switching losses.
- Response speed: It should ensure fast response times to changes in the system's operating conditions.

Before operation, MLI modulation methods must fulfill several requirements, including:

- High voltage quality: The output voltage should meet high-quality standards, resembling a sinusoidal waveform as closely as possible.

- Modular structure: The modulation scheme should be adaptable to the modular structure of the MLI.
- Avoidance of simultaneous switching of multiple voltage levels: Simultaneous switching of multiple voltage levels should be avoided to prevent shoot-through and ensure safe operation.
- Minimum frequency of power device operation: Power devices should operate at the lowest possible frequency to minimize losses and improve efficiency.
- Uniform load sharing: Load sharing among power modules should be uniform to ensure balanced operation and prevent overloading of individual modules.
- Simplicity of control algorithm: The control algorithm used should be simple and easy to implement.
- Cost-effectiveness: The implementation cost of the modulation technique should be kept to a minimum.

The modulation index also plays a crucial role in all control schemes, with modulation techniques depending on modulation ratio (over or under modulation), leading to variations in Total Harmonic Distortion (THD). While multiple techniques have been proposed in the existing research based on switching frequency, low losses are typically observed when operated at fundamental or low frequencies. Figure 1.6 provides an overview of various control and modulation schemes for MLIs.

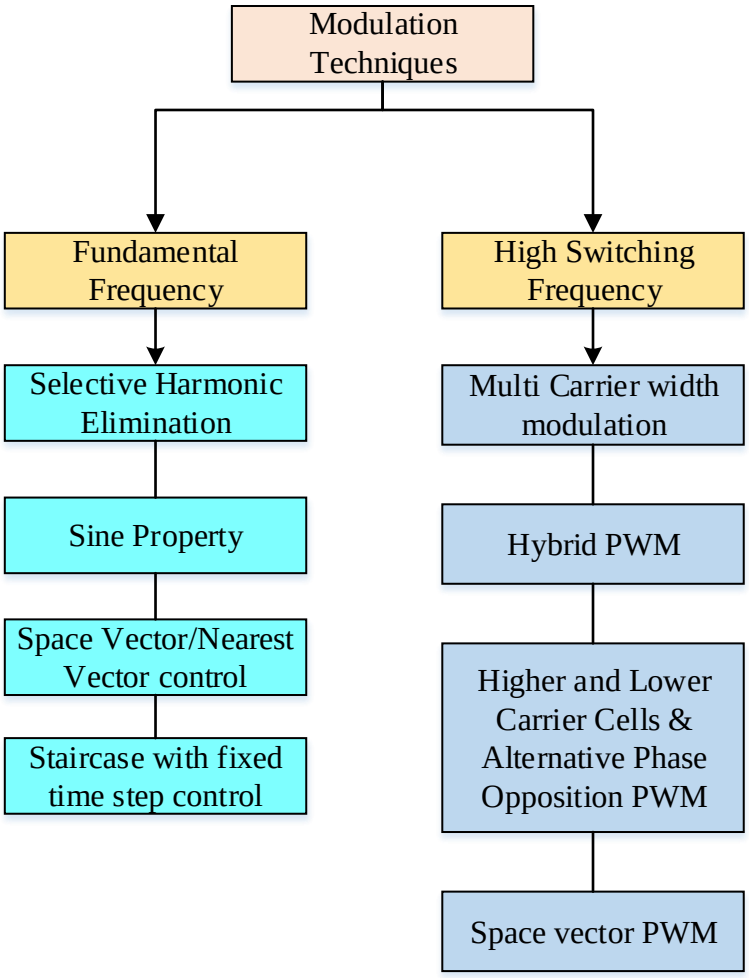


Figure 1.6: Types of modulation techniques

Modulation techniques play a crucial role in controlling the operation of inverters and ensuring the synthesis of desired output waveforms. These techniques are essential for achieving specific performance parameters such as harmonic reduction, switching losses minimization, and overall system efficiency improvement. Modulation methods can be categorized based on the switching frequency employed: fundamental switching frequency and high switching frequency.

1.3.1 Fundamental Switching Frequency

- Sine Property Modulation (SPM) is a modulation technique used in inverters to generate output voltage waveforms that closely resemble sine waves. It achieves this by adjusting the width of the pulses based on the amplitude of a reference sine wave. The modulation process ensures that the pulse width varies in proportion to the instantaneous amplitude of the sine wave, resulting in an output waveform that

mimics the shape of the reference signal. By closely following the sine wave profile, SPM helps in producing output voltages with minimal distortion, making it suitable for applications where low harmonic content and high waveform fidelity are required.

- Selective Harmonic Elimination (SHE) is another modulation technique employed to reduce harmonic distortion in the output voltage waveform of inverters. In SHE, specific harmonic components in the output waveform are targeted for elimination by strategically selecting the switching angles of the power devices. By carefully choosing the switching instants, it is possible to cancel out certain harmonics, effectively shaping the output waveform to contain only desired frequency components. This approach allows for precise control over the harmonic content of the output voltage, enabling the generation of clean and distortion-free sinusoidal waveforms. SHE is particularly useful in applications where strict harmonic limits must be adhered to, such as in power distribution systems and sensitive electronic equipment.
- Space Vector/Nearest Vector Control: In this method, the space vector representation of the three-phase voltages is used to control the inverter switches. By modulating the magnitude and angle of the space vector, the desired output voltage can be achieved. This technique offers precise control of the inverter and allows for efficient utilization of the available voltage levels.
- Staircase with Fixed Time Step Control: This approach involves dividing the reference waveform into small time steps and generating staircase voltage pulses at each step. By adjusting the width and timing of these pulses, the output voltage closely follows the reference waveform. This method is relatively simple and effective for generating low-distortion output waveforms.

1.3.2 High Switching Frequency

- Multi-Carrier Pulse Width Modulation (PWM): Multi-carrier PWM involves modulating multiple carrier signals with different frequencies to control the inverter switches. By combining these carrier signals, the desired output voltage waveform can be synthesized. This technique offers better harmonic performance and lower distortion compared to traditional sinusoidal PWM.
- Hybrid Pulse Width Modulation (PWM): Hybrid PWM methods combine the advantages of different PWM techniques to achieve optimal performance. For example, a hybrid PWM scheme may use sinusoidal PWM for fundamental frequency

components and space vector PWM for high-frequency harmonics. This approach provides flexibility and improved harmonic performance.

- Higher and Lower Carrier Cells & Alternative Phase Opposition PWM: These PWM techniques utilize multiple carrier signals at different frequencies to control the inverter switches. By adjusting the carrier frequency and phase, the output voltage waveform can be optimized for specific applications. Alternative Phase Opposition PWM alternates the phase of the carrier signals to reduce harmonic distortion.
- Space Vector PWM: Space vector PWM is a sophisticated modulation technique that calculates the voltage vectors required to achieve the desired output voltage. By dynamically adjusting the switching states of the inverter switches, space vector PWM can generate precise control over the output voltage. This method offers excellent harmonic performance and is commonly used in high-performance applications.

Overall, modulation techniques play a crucial role in optimizing the performance of inverters by controlling switching patterns to synthesize desired output waveforms efficiently while minimizing harmonic distortion and switching losses. Different modulation methods offer varying levels of complexity, precision, and harmonic performance, allowing for flexibility in designing inverters for diverse applications.

1.4 Switched-Capacitor Multilevel Inverter (SCMLI)

A Switched-Capacitor Multilevel Inverter (SCMLI) is a type of multilevel inverter that utilizes switched-capacitor circuits to generate multiple voltage levels from a single DC power source [24, 25]. The concept behind SCMLI involves the charging and discharging of capacitors in a controlled manner to achieve different voltage levels, which are then combined to synthesize the desired output waveform. The basic SCMLI typically consists of multiple capacitors connected in series or parallel configurations, along with power electronic switches such as MOSFETs or IGBTs. These capacitors are switched in various combinations to achieve the desired output voltage levels. The switching pattern is controlled by a microcontroller or digital signal processor (DSP) based on the desired output waveform and system requirements. This allows for the generation of multilevel output waveforms with reduced total harmonic distortion (THD) compared to traditional two-level inverters.

Advantages:

1. Reduced THD: SCMLIs can produce multilevel output voltages with lower harmonic distortion compared to conventional two-level inverters, leading to improved power quality.
2. Simplified circuit topology: SCMLIs require fewer components compared to other multilevel inverter topologies, resulting in reduced complexity and cost.
3. Voltage balancing: The inherent operation of SCMLIs helps in self-voltage balancing among the capacitors, eliminating the need for additional balancing circuits.
4. Efficiency: SCMLIs can achieve high efficiency due to their simplified topology and reduced switching losses.

Limitations:

1. Limited voltage levels: The number of voltage levels that can be achieved in an SCMLI is limited by the number of capacitors and the switching scheme employed. This may restrict its applicability in high-voltage applications.
2. Switching losses: While SCMLIs offer advantages in terms of reduced switching losses compared to other multilevel inverter topologies, switching losses can still occur and affect overall efficiency.
3. Complexity of control: The control algorithm for SCMLIs can be more complex compared to traditional inverters, especially when dealing with high-level voltage synthesis and voltage balancing among capacitors.

A comparison of Diode Clamped MLI (DCMLI), Flying Capacitor MLI (FCMLI), Cascaded H-Bridge MLI (CHBMLI), and Switched Capacitor MLI (SCMLI), along with their advantages and disadvantages,is provided in Table 1.1:

Table 1.1: Comparison of MLIs

MLI Type	Advantages	Disadvantages
Diode Clamped MLI (DCMLI)	- Lower switching losses due to fewer switches - Simpler control compared to other topologies - Suitable for medium-voltage applications	- Limited number of output voltage levels - Limited scalability for higher voltage levels

Flying Capacitor MLI (FCMLI)	- Higher number of output voltage levels - Greater flexibility in voltage regulation - Suitable for medium to high-voltage applications	- Increased complexity due to flying capacitors - Voltage balancing challenges
Cascaded H-Bridge MLI (CHBMLI)	- Scalable to higher voltage levels - Can achieve high-power ratings - Improved voltage balancing	- Requires a large number of power devices - Complex control algorithms - Higher cost and complexity
Switched Capacitor MLI (SCMLI)	- Reduced component count - Simplified control and voltage balancing - Lower voltage stress on switches	- Limited to lower power ratings - Limited output voltage levels - Reduced efficiency at higher power levels

1.5 Applications

In recent decades, multilevel inverters have found widespread applications across various industries, offering efficient and flexible solutions for power conversion [20]. These inverters, available in both conventional and customized configurations, power a diverse range of applications:

- Renewable Energy Systems: Multilevel inverters are extensively used in renewable energy systems such as solar photovoltaic (PV) and wind energy conversion systems. They help convert the DC power generated by renewable sources into AC power suitable for grid integration. Multilevel inverters enhance the efficiency, reliability, and power quality of renewable energy systems, thereby facilitating the widespread adoption of clean energy.
- HVDC Transmission Systems: High Voltage Direct Current (HVDC) transmission systems utilize multilevel voltage source converters (VSCs) at both ends of the

transmission line for efficient long-distance power transmission. Multilevel inverters enable HVDC systems to achieve precise voltage control, low harmonic distortion, and improved fault tolerance, contributing to the stability and reliability of the grid.

- STATCOMs: Static Synchronous Compensators (STATCOMs) are voltage-source converter-based devices used for reactive power compensation and voltage regulation in power systems. Multilevel inverters are employed in STATCOMs to inject or absorb reactive power as needed to stabilize grid voltage, improve power factor, and mitigate voltage fluctuations. The superior voltage control capabilities of multilevel inverters make them well-suited for STATCOM applications, enhancing the overall stability and power quality of the electrical grid.
- Adjustable Speed Drives: Multilevel inverters are widely used in adjustable speed drives (ASDs) for controlling the speed and torque of electric motors in various industrial applications such as pumps, fans, and compressors. By providing precise control over motor operation, multilevel inverters enhance energy efficiency, reduce mechanical stress, and improve system performance in variable speed drive applications.
- Electric Vehicles (EVs) and Hybrid Electric Vehicles (HEVs): Multilevel inverters play a crucial role in the powertrain of electric vehicles and hybrid electric vehicles, where they are used to convert DC power from batteries or fuel cells into AC power to drive the vehicle's electric motor. Multilevel inverters enable efficient energy conversion, regenerative braking, and smooth torque control, thereby enhancing the performance and driving range of electric vehicles.
- Industrial and Grid-Connected Applications: Multilevel inverters find applications in various industrial and grid-connected systems such as uninterruptible power supplies (UPS), industrial motor drives, FACTS devices, active power filters, and grid-tied inverters for distributed energy generation. They offer improved power quality, reduced electromagnetic interference, and enhanced reliability in diverse industrial and utility-scale applications.

Overall, multilevel inverters play a pivotal role in modern power systems and industrial applications, offering advanced voltage control, harmonic mitigation, and power quality improvement capabilities across a wide range of domains, including renewable energy integration, grid stabilization, and electric transportation.

1.6 Multi-level Inverter Application in STATCOM for Distribution System

Multi-level inverters play a crucial role in enhancing the performance and efficiency of Static Synchronous Compensators (STATCOMs) used in distribution systems. STATCOMs are voltage-source converter-based devices employed for reactive power compensation, voltage regulation, and power quality improvement in electrical grids. By integrating multi-level inverters into STATCOMs, several benefits can be achieved, making them a preferred choice for distribution system applications [21]. The increasing interconnection of electric power supply systems has led to the need for improved reliability and stability in distribution networks, especially in handling frequently changing loads and damping out transient oscillations. Conventional transmission systems have struggled to meet these demands, leading to severe blackouts worldwide. In response, Flexible AC Transmission Systems (FACTS) technology has emerged as a solution to enhance grid security, stability, and control.

Reactive power compensation is identified as an effective method to enhance the performance of AC systems. Therefore, the design of STATCOMs with multi-level inverters has gained significant attention. These systems utilize advanced control schemes and power electronics switching devices to provide voltage control, reactive power flow control, and transient stabilization.

Several research studies have focused on designing STATCOM controllers integrated with multi-level inverters to address distribution system challenges. These studies include the development of cascaded two-level inverters for harmonic reduction, implementation of fuzzy control schemes for high-voltage and high-power applications, and the introduction of hybrid fuzzy-PI control for multi-level STATCOMs. Furthermore, studies have explored the operation of multi-level STATCOMs in unbalanced systems and their effectiveness in improving transient stability. Nonlinear STATCOM controller designs have also been proposed to enhance the transient stability of power systems.

Overall, the application of multi-level inverters in STATCOMs for distribution systems offers a promising approach to enhance grid reliability, stability, and power quality. Through advanced control strategies and efficient power conversion techniques, multi-level STATCOMs contribute to the efficient operation and functionality of modern distribution networks, ultimately improving overall system performance and minimizing operation costs. Hence, in the below section, STATCOMs are discussed in a detailed manner.

1.6.1 Operation of STATCOM

The Static Synchronous Compensator (STATCOM) serves as a primary shunt device within the Flexible AC Transmission Systems (FACTS) family, employing power electronics to manage power flow and enhance transient stability in power grids. Its primary function is to regulate voltage by controlling the amount of reactive power injected into or absorbed from the power system. Maintaining the pure reactive power flowing through its three-phase voltages in phase with the system voltages is crucial for effective operation [22].

The variation in reactive power is achieved through a Voltage Source Converter (VSC) connected via a coupling transformer. The VSC utilizes forced commutated power electronic devices such as GTOs (Gate Turn-Off thyristors) or IGBTs (Insulated Gate Bipolar Transistors) to generate the voltage from a DC voltage source.

If the voltage at the output of the VSC (Voltage2) is greater than the voltage at the point of connection (Voltage1), reactive current (Iq) flows from the converter to the AC system through the coupling transformer, injecting reactive power into the system. Conversely, if Voltage2 is less than Voltage1, current Iq flows from the AC system to the converter, absorbing reactive power from the system. When Voltage2 equals Voltage1, no exchange of reactive power occurs. The magnitude of the reactive power exchanged depends on the voltage difference [23].

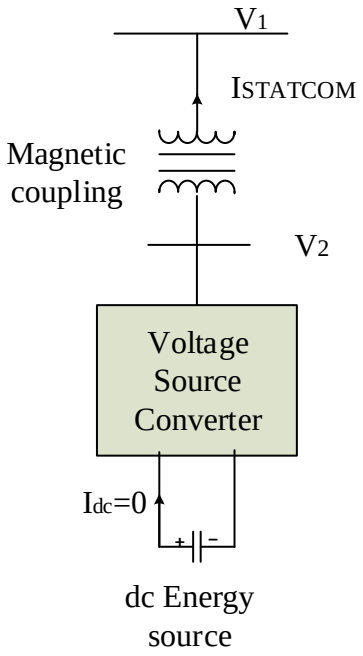


Figure 1.7: General circuit of STATCOM

Figure 1.7 depicts the schematic configuration of a STATCOM, which includes magnetic coupling and voltage source coupling. A capacitor connected on the DC side of the VSC serves as a DC voltage source. For medium to high-power applications, it is challenging to directly connect a single semiconductor switch. Therefore, multilevel inverters have been developed for AC high and medium power applications. The concept of multilevel converters originated in 1975 with the introduction of 3-level converters. Since then, significant advancements have been made in the development of high-power multilevel inverter topologies. These high-power multilevel inverters utilize a series of switches in conjunction with lower voltage DC sources to facilitate power conversion, thereby synthesizing staircase voltage waveforms. Multiple DC voltage sources, such as capacitors or batteries, can be employed to achieve high power output efficiently.

1.7 Problem Statement

The demand for compact and efficient power converters has surged across various domains, including photovoltaic systems, active power filters, and high-frequency AC systems. Among the evolving technologies, multilevel inverters (MLIs) have garnered substantial attention for their ability to enhance power quality, minimize harmonics, and elevate voltage levels, surpassing the capabilities of conventional inverters. However, conventional MLIs are plagued by inherent drawbacks, such as high component count, escalated voltage stress, and intricate voltage balancing mechanisms, constraining their practical adoption in diverse applications.

The complexity associated with conventional MLIs presents a significant challenge to their widespread implementation. High component counts increase manufacturing costs and complexity, while heightened voltage stress demands robust insulation and protection measures. Moreover, intricate voltage balancing mechanisms necessitate sophisticated control strategies, further complicating system design and operation. Consequently, there exists a pressing need to devise innovative solutions that mitigate these challenges and propel the adoption of MLIs in real-world applications.

1.8 Motivation

The motivation behind this research stems from the urgent need to overcome the limitations of existing MLIs and pave the way for more efficient and reliable power conversion systems. Furthermore, the potential impact of advancements in MLIs extends beyond traditional

applications, with implications for various industries and sectors. For instance, improved MLIs could facilitate the integration of renewable energy sources into the grid, enhance the efficiency of electric vehicle charging infrastructure, and enable more reliable power distribution networks in smart cities. By surmounting barriers such as voltage unbalances, power quality deficiencies, and optimal deployment in distributed systems, this research aspires to advance the realm of power electronics, fostering stability, efficiency, and reliability across diverse industries and applications, including renewable energy integration and EV infrastructure development.

1.9 Research Objectives

- To develop a new multilevel based VSC configuration that can optimize the performance and improve the power quality aspects.
- To compare the performance of new VSC with conventional CMLI in respect of switching and harmonic losses under different switching techniques.
- To use new VSC as STATCOM and optimal location of it in 9-bus system

The functionality of the MLI is validated when integrated into the IEEE 9 bus distribution system, a standard test system for power distribution studies was used. The MLI's performance is evaluated as a Static Synchronous Compensator (STATCOM) under various fault conditions within the distribution system. Analyze how the MLI can improve power quality during these faults.

1.10 Thesis Organization

Chapter 1: Introduction

This chapter discussed inverters, their classifications, multilevel inverters, their application in STATCOM for the distribution system, and then about STATCOM, and then about switched capacitor MLI. Also provided with the problem statement, motivation, and objectives of the research. Finally concluded with a summary.

Chapter 2: Literature Survey

This chapter discussed the various research works in the field of multi-level inverters and provided with comparison table discussing the advantages and limitations. Also provided with a research gap was provided, and finally, this chapter concluded with a summary.

Chapter 3: Design and Implementation of a High-Gain Switched-Capacitor Step-Up MultilevelInverter with Reduced Component Count

This chapter discussed about Proposed Nine-level Inverter Topology, Generation of the 9-level output, Voltage balancing and Capacitance Calculation, Switch voltage stress analysis, Calculation of Power Losses in NSC MLI, Comparison of 9-level SC-MLI, and Simulation and Experimental Analysis. Finally concluded with a summary.

Chapter 4: Novel Nine Level Switched Capacitor Multi-level Inverter Based STATCOM forDistribution System

This chapter discussed about Novel Nine Level Switched Capacitor Multi-level Inverter Based STATCOM for Distribution System. It includes about GAO based allocation in the IEEE-9 bus, a proposed 9 level inverter based STATCOM. Also, provided with results and discussion with various performance analyses.

Chapter 5: Conclusion and Future Scope

This chapter discussed the conclusion of the entire research and provided directions for future enhancement.

1.11 Summary

This chapter provided a comprehensive overview of inverters, covering their classifications and the emergence of multilevel inverters (MLIs), including their applications in systems like STATCOM for distribution. It delved into the functionality of STATCOM in power grids, emphasizing its role in voltage regulation and reactive power control. Additionally, the chapter explored the concept of switched capacitor MLIs, highlighting their ability to generate multilevel voltage outputs efficiently. Furthermore, it presented the research's problem statement, motivation, and objectives, aiming to address challenges and explore opportunities in the field. In conclusion, the chapter emphasized the significance of these topics in advancing power system technologies and achieving enhanced efficiency and reliability in energy distribution networks.

CHAPTER 2

LITERATURE SURVEY

2.1 Overview

Green energy sources are extensively used to lessen reliance on systems that rely on fossil fuels and, therefore, pollution. Although renewable, green energy sources are erratic in nature [26]. Today's most companies employ renewable energy sources owing to advancements in power electronics, rising fossil fuel prices, and a worldwide trend toward reducing greenhouse gas emissions [27]. The load or the grid becomes crucial in order to ensure the maximum possible power quality. This is made possible in large part by the management of several power electronic converters. The core of these systems is an inverter, which is a type of power converter that conveniently transforms DC to AC. Over the years, a great deal of research has been done to build new inverter topologies. Recently, multilayer inverters (MLIs) of two, three, and more levels have been created for various purposes [28]. These renewable energy sources are connected to the local grids via a variety of electrical power converters, such as inverters, which convert DC to AC electricity. Recently, the use of multilevel inverters (MLIs), which can provide a high-quality voltage, has increased [29]. MLIs have left its mark on applications, including solar photovoltaic (PV) systems, electric vehicles, FACTs, etc., in comparison to the previous structures. This can be attributed to benefits including reduced dv/dt stress, little magnetic interference, and superior output quality [30]. Diminished switch, the greatest substitute offering a small and modular architecture,isanMLI. Recent proposals of various symmetrical and asymmetrical topologies have proven beneficial for photovoltaic and battery energy storage applications. Comparatively speaking, symmetrical structures require a greater number of switches than asymmetrical ones. These structures are also capable of functioning in low power factor and unity power factor scenarios in various bidirectional modes [31]. The configuration given necessitates a notably higher number of switches for operation under low power factor conditions. The additional modules that are suggested are highly helpful in increasing the number of levels while maintaining compactness [32]. Multilevel inverters, or MLIs, are becoming more and more important as essential components with a broad range of uses that impact power electronics. Numerous advantages have been cited for them, including superior electromagnetic properties, minimal stress on switches, high-quality output voltage, and more [33].

2.2 Related works

ErfanAzimi et al. [34] suggested a brand-new multi-level inverter with switching capacitors. Using a single DC source and a few capacitors to stepup the input voltage, the construction as shown produces a staircase that approaches a sinusoidal AC voltage. The converter's functioning is managed by the nearest level control (NLC) technique. These switching states are intended to constantly guarantee the capacitors' self-voltage balancing. Among the benefits of the inverter that is being offered are its low switching frequency, straightforward operation, and built-in bipolar output. The structure requires fewer circuit components than other current topologies. The suggested topology's capacity to transfer power in both directions makes it easier for the circuit to function under a variety of load conditions, making it suitable for use in most industries. In addition, a 13-level lab prototype is put into practice to validate and actualize the MATLAB Simulink model's effectiveness under various load scenarios. The results of the experiment and simulation validate the converter's proper performance. Ultimately, 92.73% theoretical efficiency is attained.

Kaibalya Prasad Panda et al. [35] presented a step-up 17-level SC MLI with one DC source, three capacitors, and fewer switches. Using no additional capacitor voltage balancing circuit, the steady-state voltage across the capacitors is kept in the 1:2:0.5 ratio, which helps to triple the boosting ability. Additionally, fewer switches in the conduction route and 50% of the switches operating at fundamental frequency guarantee that all power loss in the suggested circuit is eliminated. The benefits of the suggested MLI are explained by a comparison with previously created 17-level MLIs in terms of gain, stress, cost factor, and component count. Following a thorough circuit study and loss assessment, simulations are run to confirm the suggested MLI's step-up and intrinsic balancing properties. To further confirm the operational viability of the 17-level prototype, comprehensive experimental test results under various transient situations are provided utilizing both the fundamental frequency and high-frequency switching methodologies.

MarifDaula Siddique et al. [36] proposed a novel boost multilevel inverter architecture based on switched capacitors (SCMLI). With one DC voltage source, two capacitors, and nine power semiconductor switches, the suggested design can produce a nine-level output voltage waveform with double the voltage gain. The suggested design can be utilized for applications requiring higher voltage gain by adding two switches. The suggested topology also has lower

voltage stress across the switches, intrinsic polarity switching capabilities, parallel functioning of capacitors, and self-voltage balancing of capacitors. The selective harmonic elimination pulse width modulation (SHEPWM) approach is used to produce an output waveform of the highest quality. With this method, the harmful low-order harmonics in the MLI output voltage may be readily controlled and removed. To establish the suggested topology's benchmark, it is compared to the newly introduced SCMLI topologies, taking into account a number of different factors. Using a laboratory prototype setup, a variety of experimental data are used to examine the performance of the proposed MLI.

Mohammad Fahad et al. [37] proposed a dual input SCMLI with a high boosting factor, few components, and self-balancing capacitor voltages to provide an output of nineteen levels. A thorough examination of the suggested structure is provided, with particular attention paid to the costs, dynamic performance, and component needs. During operation, the efficiency and loss distribution are also shown. Simulations have been used to validate the SCMLI's functionality and real-time performance. The outcomes of the experiments confirm the simulations even more.It has been explained how to create a multisource step-up multilevel inverter with good power quality and minimal component needs. It is illustrated how the suggested SCMLI works and how capacitor voltages have the ability to balance themselves. Analysis of earlier efforts to create different MLIs and switched-capacitor designs, along with their benefits and drawbacks, is provided. A study was done to compare the suggested SCMLI with current topologies. To demonstrate the thermal behavior and efficiency of the topology, a thermal loss study was conducted. The outcomes of the simulation are shown. The experimental findings validate the performance under various operating situations (load and MI variations).

Yaoqiang Wang et al [38] introduced a revolutionary multilevel inverter that uses new switched-capacitor circuits (SCCs) to provide the required number of output levels with fewer elements. Both parallel and series modes of operation are available for the SCC's two input sources and capacitors. Without the need for additional circuits, the capacitor voltage imbalance problem is naturally resolved in the parallel mode when the SCC's capacitor voltage is charged to the DC source voltage. The capacitor may be utilized as a substitute source in the series mode, which aids in achieving a large voltage gain. The suggested architecture is appropriate for use in renewable energy generating systems with numerous DC sources accessible due to the SCC's many input sources. At the load terminal, a configuration consisting of two half-bridges and two switches is utilized as a polarity generating circuit

rather than an H-bridge module. Two SCCs' input sources can be chosen in both symmetric and asymmetric patterns, which can provide a wide range of output voltage values. This article describes the inverter's circuit architecture, operating principle, modulation technique, capacitor analysis, and performance comparisons. Furthermore, the inverter's validity and practicality are confirmed by experimental findings.

PrabhatRanjanBana et al. [39] suggested an SC MLI with two sources. Voltage boosting is accomplished by the use of a proper charging-discharging sequence to selfbalance the SCs. A detailed description of the planned 25-level MLI's characteristics and operational analysis is provided. The suggested extensible SC MLIs are superior to state-of-the-art MLIs when compared in terms of component count, voltage stress, and cost factor. Using both the low and high switching frequency control techniques, a thorough simulation of the suggested MLI structure is carried out using the MATLAB/Simulink environment. Additionally, a prototype of the suggested MLI under load fluctuations, frequency change conditions, and modulation index variation is developed in order to test simulation results experimentally. This study presents a unique DSC MLI that generates a 25-level staircase output with fewer switches and just two DC sources. The voltage levels are synthesized by the use of capacitors, which greatly lowers the number of sources. Because of the SCs' configuration, voltage boosting may be accomplished without the need for extra voltage balancing circuits. Consequently, the suggested DSC MLI maximizes both the total size and the expense.

Yat Chi Fong et al. [40] developed a modular cell and soft-charging approach to create a step-up switched-capacitor (SC) multilevel inverter (MLI) with lower ripple power loss. SCMLI is a very desirable option for high-frequency ac applications because of its various advantages. The voltage ratings of the components in the proposed SCMLI, which has a two-phase alternating structure, are significantly lower than those of the unfolding H-bridge based topologies while maintaining the self-voltage balancing and voltage step-up capabilities provided by the series-parallel SC technique. This construction also increases the maximum charging period of capacitors, allowing for greater working frequencies. Soft-charging is accomplished in all SC units in the inverter by introducing a tiny resonant inductor, which reduces the ripple loss and electromagnetic interference problems seen in many SCMLIs. The idea of the underdamped SC circuit provides an explanation of the soft-charging action of the suggested inverter under staircase modulation. The modeling and practical results, which demonstrate a significant decrease in the ripple power loss by using the soft-charging

approach, confirm the mathematical analysis. The method works very well for distributing electricity at high frequencies.

SaeidDeliri et al. [41] suggested a fundamental multilayer inverter design with a diamond-shaped high step-up switching capacitor foundation. Two active switches, two diodes, and two capacitors make up the fundamental switched-capacitor (SC) stage. With the unfolding circuit (10 switches, 5 capacitors, and 5 diodes), 17 voltagesteps with a gain of up to 8 times the input voltage may be produced at the output using a single DC source. The stages of the diamond-shaped switched-capacitor can be extended to achieve larger voltage levels and voltage gains. In order to generate positive, zero, and negative steps, the proposed topology uses two half-bridges rather than a complete bridge. This lowers the Voltage Stress (VS) on two output switches, which in turn lowers the Total Voltage Stress (TVS). Furthermore, because capacitors naturally balance their voltage, there is no need for extra control circuitry, which lowers the overall size, complexity, and expense of the converter. Among the benefits of the suggested architecture are also its adaptability, scalability, low voltage ripple on capacitors, low overall voltage stress, good power quality, and capacity to provide low- to medium-power factor (R-L) loads. The benefits of the suggested topology are confirmed by the low Cost Function (CF) found in the comparison section and by the outcomes of the experiments.

Kasinath Jena et al. [42] suggested a step-up, three-level, switched-capacitor multilevel inverter design with fewer voltage stressors and switches. The suggested architecture is appropriate for medium- and low-voltage applications as it can provide five different output voltage levels from a single isolated DC source. The suggested architecture has four switches, one power diode, and one capacitor in each leg. Additionally, a universal modulation technique called staircase is used to create the switching signals. The suggested architecture will therefore function at both low and high switching frequencies. A comparison of three-phase topologies with the most recent literature was done in order to demonstrate the benefits of the suggested design. The switching components, voltage stress, component count per level factor, and cost function were all considered. Because of this self-balanced capacitor voltage, fewer sensors are needed, and the control system's complexity may be greatly decreased. A consideration of efficiency and loss is included in the mathematical modeling of the proposed five-level SC-MLI topology. Under dynamic loading circumstances, the output current, line voltage, and pole voltage profiles are shown. Through both simulated and experimental research, the effectiveness of the PT is demonstrated across a range of output

voltages and capacitance counts. After conducting a mathematical model with loss and efficiency analysis, it is concluded that the proposed five-level SC-MLI topology has an appropriate efficiency.

AnzarAhmadet al. [43] proposed a generalized MLI that generates a significant number of output voltage levels with a lower number of components. A significant number of output voltage levels with a lower number of components. The demonstration of symmetric and asymmetric designs' operation involved the creation of output voltage at 13 and 31 levels, respectively. Boosting capabilities and self-capacitor voltage balancing are the main characteristics of the suggested SCMLI (switched-capacitor multilevel inverter) construction. The output voltage was managed and regulated using the closest level control modulation method. The ideal capacitance value was also determined using the longest discharging period. Additionally, a generalized formula for producing greater voltage levels was obtained.

Junfeng Liu et al. [44] proposed a pair of symmetric/asymmetric hybrid MLIs by integrating switched-capacitor techniques into conventional hybrid MLIs. Simplified modulation results from avoiding complex balancing controls for capacitor voltage. The backside H-bridges that can tolerate the accumulated voltage stress are eliminated when compared to SCMLIs. Device peak inverse voltages are lowered, necessitating the use of only low-voltage components. In the meantime, there are many fewer components. These benefits all add to increased effectiveness and lower expenses. As a result, the suggested hybrid MLIs are particularly suitable for producing a staircase output straight from a low-voltage input source. First, analyses for the suggested topologies are provided, along with their guiding concepts. After that, comparisons are made to show how great they are. In order to assess performance, experimental prototypes and simulations are used, and the outcomes validate the viability of the suggested hybrid MLIs.

Sze Sing Lee et al. [45] proposed one-switched-capacitor integrated MLI (1SCI-MLI). An additional switched-capacitor circuit is appropriately included to provide an expanded topology of 1SC-MLI. Both of the suggested topologies have the capacity to enhance voltage. They also have a small number of DC sources and switches. More significantly, they fix the current equivalents' high voltage stress issue. There is a discussion of their matching operational analysis and contrasts with current MLI topologies. A laboratory prototype's simulation and experimentation results are provided to confirm the viability of the suggested topologies. Two enhanced switched-capacitor integrated MLI topologies with a DC source

string are developed in this work. They address the high voltage stress issue that their current counterparts were having. They also showed off a variety of benefits, including a decrease in the number of DC sources, an increase in voltage boosting gain, and a reduction in switch count. Through the use of simulations and tests, the effectiveness of the suggested topologies with the implementation of SHEPWM and SPWM is verified. Strong agreement was found between theoretical analysis, simulations, and experiments, confirming the suggested topologiesconceptual soundness and functionality.

Dhananjay Kumar et al. [46] suggested two different "modified MLI topologies," eachcentered on an implementation of "reduced device counts" (RD-MLIs) with the FT capability added. The article suggests topologies that modify single-phase T-Type RD-MLI. The "modified T-Type topologies" may achieve intrinsic self-voltage balancing in DC-Link capacitors and are FT against open circuit fault (OCF). The MATLAB/Simulink environment is utilized to examine the healthy, faulty, and post-failure operations of the suggested topologies in this article. Additionally, a hardware prototype is created to verify the concept's and control strategy's effectiveness through experimentation. The Simulink model that is interfaced with dSPACE DS-1104 to generate control pulses to drive switches of modified MLI topologies is the control approach that has been created. The suggested "modified single-phase fault-tolerant MLI topologies" experimental results confirm the FT feature against OCF. When compared to similar other analogous MLI topologies documented in the literature, the modified topologies essentially provide advantages of having fewer diodes, power switches, DC sources, capacitors, drivers, and total blocking voltage (TBV in each unit).

ASGHAR TAHERI et al. [47] suggested a new, less complex switched capacitor (SC-Type) inverter for asymmetrical multilevel inverters (MLIs). The suggested design charges and discharges the capacitors using a unique technique in order to balance their voltages. The number of switches, the number of DC voltage sources, the quantity of blocked voltage in the switches, and the power losses are all decreased in the suggested inverter. The size, complexity, and cost of MLI decrease with the number of components. The suggested topology's cascade connection is utilized to increase the number of output voltage levels. A 25-level MLI's testing findings and MATLAB simulations confirm the suggested inverter's high performance. The architecture that is being given makes use of a unique technique for the capacitors' charging and discharging, which helps maintain the capacitors' voltage balance. To confirm its effectiveness, the cascaded topology that was provided was compared

to a few alternative topologies. This comparison shows that, in comparison to certain topologies, the suggested cascaded MLI requires the fewest number of components, the lowest power losses, and a lower amount of blocked voltage in switches.

AbhinandanRoutray et al. [48] suggested a multilayer inverter with switched capacitors (SC-MLI), which guarantees the peak inverse voltage (PIV) across all switches within the dc source voltage. In the proposed SC-MLI, a single DC source can create thirteen (or higher) voltage levels in total. In the proposed circuit, the number of DC sources is greatly reduced. Additionally, the suggested SC-MLI achieves a voltage increase of three or greater. Lower-rated power devices are needed, and the total standing voltage (TSV) is also reduced, because the PIV of the switches is within the input DC source voltage in the proposed SC-MLI. The suggested SC-MLI has self-balancing capacitors. In this study, the suggested SC-MLI has been compared with current SC-MLIs in terms of PIV, TSV, and active/passive components. An experimental prototype rated for 550 W has been used to test the performance of the planned 13-level SC-MLI.

Tapas Roy et al. [49] proposed a novel structure of a switched capacitor converter (SCC). First, the fundamental component of the suggested SCC is explained. Next, a generalized structure of the suggested SCC is discussed. The SCC that is being shown produces a multistep boosted output voltage from a single DC source, several switches, diodes, and capacitors. It is possible to charge the capacitors in the SCC in a trinary asymmetrical manner. A thorough analysis of the suggested structure with other recently created SCC structures is provided. Compared to the majority of recommended SCC structures, it is demonstrated that the proposed SCC can provide an output voltage level with lower total standing voltage (TSV) and lower maximum switch stress voltage. Additionally, a symmetric and asymmetric DC source configuration Switched Capacitor Multilevel Inverter (SCMLI) has been designed and evaluated based on Cross-Switched Multilevel Inverter (CS-MLI). In order to provide a fair comparison with the current SCMLI structures, a cost function (CF) is used to compare the overall costs of the structures. Compared to the majority of previous SCMLI structures, the suggested SCMLI offers a reduced cost function/output voltage level (CF/NL) for both symmetric and asymmetric DC source configurations. Several experimental investigations have confirmed the effectiveness and functioning of the suggested SCMLI structure.

Mohammad Ali Hosseinzadeh et al. [50] presented two extendable configurations for switched-capacitor multilevel inverters to be applied to solar photovoltaic systems. While the second extensible configuration employs a mix of DC sources and capacitors, the first extendable configuration only applies to two DC suppliers. It increases the number of levels by connecting several capacitors in series. The suggested inverters may self-balance their voltage and lessen the voltage stress on switches, which lowers the amount of switching losses. According to the comparison, both extendable topologies have benefits over the majority of multilayer inverters that have been documented, including low voltage stress, large boost factors, low cost, and few capacitors and semiconductors. Additionally, an efficiency evaluation is provided, demonstrating that the proposal's efficiency outperforms more contemporary topologies. A high-power solar photovoltaic system is used to test and simulate the proposed inverter, and the results demonstrate its great performance and high-quality output waveform. By constructing a lab prototype, the proposal's functioning is examined and tested.

M. JagabarSathik et al. [51] introduced a new cross-connected compact switched capacitor (C3SC) cell for multilevel inverter applications. The floating capacitors (FCs) and the input DC source are connected by the proposed CCS cell using two diodes and four switches. With the suggested C2SC cell, a nine-level inverter is generated with just 10 switches and two FCs. The suggested MLI based on C3SC cells has a voltage gain of two and is self-balancing. The maximum blocking voltage for each switch in the suggested architecture is contained within the input DC voltage (Vin) value. A basic logic gate based pulse generating system is described, along with a full explanation of the working concept. To verify the functionality of the suggested architecture, thorough calculations and experimental data from an 850 W prototype with many test scenarios are provided. Finally, to prove the benefits and superiority of the suggested topology, a thorough comparison analysis is carried out with other recent SCMLIs.

N. Sandeep et al. [52] explained a revolutionary nine-level inverter that uses switched capacitors (SCs) and has the capacity to triple boost while using fewer components. The series/parallel connectivity of SCs is essential to the structure of the suggested topology. There are two SCs and twelve switches in all. The suggested design does not use a back-end Hbridge, in contrast to comparable SC-based inverters, and none of the switches' voltage stress is greater than double the input DC voltage. A basic pulseswidth modulation approach based on logic gates is devised to gate the switches within the suggested topology. To verify

the superior qualities of the suggested topology, a thorough comparison with the most advanced topologies in terms of the quantity of components needed is carried out. Ultimately, a range of experimental findings is showcased to confirm the practicability and functionality of the suggested design. An extensive comparative analysis demonstrated the advantages of the suggested topology over comparable state-of-the-art topologies. The experimental findings confirmed the circuit's functionality and confirmed that the suggested topology is feasible under a wide range of real-time operating situations. The SC-based topology described in this study provides good structural and operational benefits for high power-quality DC-AC power conversion systems, and it has these appealing properties.

Amir Taghvaie et al. [53] presented a DC to AC converter with the ability to increase of voltage. There is just one DC source utilized in the construction of this inverter. Additionally, output voltage levels can be raised by employing the power storage technique and connecting charged capacitors and a DC source in series. This inverter can self-balance the voltage of its capacitors and has a modular construction. The entire converter, including the H-bridge inverter, can withstand a voltage stress equivalent to the amount of the input DC source. Peak inverse voltage and total standing voltage both noticeably drop as a result. The suggested inverter's performance potential in high-frequency applications is an additional benefit. The suggested inverter's modular design facilitates maintenance and offers the option of expansion to higher voltage levels. Furthermore, the performance in high voltage is added to the features of the recommended inverter, taking into account that the stress of all its components is equivalent to the input source. To verify the suggested inverter's performance, a laboratory test is conducted, and its nine-level structure is simulated.

MarifDaula Siddique et al. [54] recommended a boost multilevel inverter topology in this paper. The suggested structure creates a nine-level output voltage waveform by combining 11 unidirectional switches with one switched capacitor unit. The primary benefits of this design, aside from the double voltage gain, have been decreased voltage stress and self-voltage balancing of capacitor voltage without the need for an additional technique. The integration of switching capacitors into the topology in accordance with contemporary developments, as well as a range of comparative metrics such as component counts, voltage stresses, cost, and efficiency, with a maximum value of 98.3%, has all been used to assess the advantages of the suggested topology. Switches have been controlled by the phase disposition pulse width modulation (PD-PWM) and closest level control PWM (NLC-PWM) techniques. The study

includes various hardware and simulation findings under various operating situations to illustrate how well the suggested architecture performs.

M. JagabarSathik et al. [55] presented a compact switched capacitor multilevel inverter topology with reduced switch count and with self-voltage balancing and boosting ability. It is described how the suggested CSCMLI operates. A comparison of the most recent switched capacitor multilevel inverter topologies and the number of switches and blocking voltages is provided. It is advised to use a novel level shifted multicarrier PWM modulation technology in order to further improve the output voltage quality. Low THD and high RMS voltage are produced by this modulation approach. With a single DC source and two capacitors, the nine-level CSCMLI uses the suggested modulation mechanism. Using the suggested PWM control, the simulated and experimental findings are confirmed at switching frequencies of 50 Hz and 2.5 kHz. Capacitor voltages are independent of load power factor, meaning that fluctuations in load have no effect on them. Furthermore, the suggested modulation approach may be used for AC drive applications, renewable energy power conversion systems, and other low- and high-switching-frequency applications.

HamedJalalat et al. [56] had utilized a variety of Flexible Alternating Current Transmission System (FACTS) devices, and the power system's dependability and power quality are increased. The utilization of such devices is restricted not only by technical limitations but also by the expenses associated with installation and upkeep. In order to optimize FACTS's efficiency, the network's device placement must minimize the total number of devices. Numerous studies have been carried out in this spirit to provide ideal placement solutions. These techniques result in the best placement, although they are typically extremely computationally demanding. As a result, this method for intelligent optimal placement focuses on minimizing computational volume. The recommended strategy limits the number of buses that are monitored in order to achieve this goal and employs an estimating methodology for monitoring other buses. The fewest monitoring buses are chosen in order to prevent escalating computations for this option, which applies the worst fault condition rather than all fault kinds. Additionally, high-risk zones are identified for every monitoring bus so that the study can be carried out by applying various fault conditions in just these locations, resulting in an additional reduction in computational burden. Ultimately, the genetic algorithm is used to solve the optimal placement problem.

M. S. Giridhar et al. [57] In order to solve the optimal allocation of photovoltaic (PV) distributed generation (DG) in the electrical distribution network (EDN), taking grid linked mode into consideration, a new and effective meta-heuristic mayfly optimization algorithm (MOA) is provided. Eventually, in order to maintain under islanding mode, the best hybrid energy systems should be designed and allocated using PV, battery energy storage (BESS), and distribution-static synchronous compensator (D-STATCOM) in mind. The IEEE 33-bus EDN was used for the simulations. Having an ideal PV system in the network leads to a considerable improvement in the voltage profile and decreased losses as compared to the base situation. Furthermore, the suggested hybrid energy system has ample capacity to handle the whole network demand. Hence, the aneed for self-sufficient and environmentally friendly microgrids in response to the steadily rising demand for electricity. However, MOA is thought to be better than a few of the heuristic methods employed in the literature and is also highly competitive with other methods.

MostafaElshahed et al. [58], the innovative AROA is carried out for the purpose of allocating separate PV distributed energy resources and concurrent PVSTATCOM in order to minimize the goal function under consideration over a 24-hour daily horizon. By contrasting it with the golden search optimization (GSO) and differential evolution (DE) algorithms, the efficacy of the suggested AROA is shown. It was shown that the suggested AROA was more efficient than DE and GSO at reducing energy losses and voltage profile aberrations while upholding all operational restrictions. Furthermore, because there are a lot of constraint violations, PV sources are insufficient to meet all of the criteria during the day. Furthermore, by reducing energy losses and enhancing the voltage profile throughout the day, the reactive power assistance via PVSTATCOM based on the suggested AROA significantly improves the distribution system. In comparison to DE and GSO, the proposed AROA can discover an exact solution more quickly based on convergence characteristics.

K Radha Rani et al. [59],the proposal suggests utilizing a distribution-static synchronous compensator (D-STATCOM) to achieve appropriate reactive power compensation. This will help reduce losses, improve voltage profiles, and boost voltage stability for various loads, such as electric vehicles and agricultural loads. Improved Bald Eagle Search (IBES), a new and effective meta-heuristic technique, is used to solve the suggested optimization problem while taking various operational and planning limitations into account. The simulation results are run for various load modeling scenarios on the IEEE 33-bus. IBES's computational efficiency is contrasted with that of other literature works and basic BES. Based on the

findings, IBES has outperformed all of the works that were compared in terms of computing capabilities. Conversely, as observed in contemporary EDNs, the ideal placement and dimensions of D-STATCOM resulted in a notable decrease in loss, enhancement of voltage profile, and increase of voltage stability for various types of loads.

Samson OladayoAyanlade et al. [60], using FA as an optimization tool, investigated an optimization technique was investigated to reduce actual and reactive power losses in a power network by appropriately positioning and scaling STATCOM. The Newton Raphson algorithm was extended to include the STATCOM power flow equations in order to analyze the steady state power flow of an IEEE 14-bus transmission network. To conduct the network power flow analysis both with and without FA-optimized STATCOM, a MATLAB software was developed. The findings showed that transmission network efficiency could be raised by improving the STATCOM controller with FA without the need to expand the power system. The implemented FA technique was found to be advantageous for optimal STATCOM controller allocation in minimizing both real and reactive power losses while enhancing the network voltage profile, hence satisfying the study's objectives. To further enhance the performance of the transmission networks, it is advised that the optimal allocation of numerous STATCOMs be done in future studies on this issue.

Anzum Ansari et al. [61] had suggested the TLBO-PSO Algorithm, a hybrid teaching-learning-based optimization algorithm, for the best STATCOM placement and distributed generation (DG). The IEEE 33 and real-time 52 bus distribution system's DG and STATCOM placement is optimized using a multi-objective formulation. The developed objective function entails minimizing power losses and network security index while optimizing voltage stability and cost-benefit parameters. MATLAB/Simulink is used to do simulations for many systems and scenarios. When TLBO and PSO algorithms are used to compare the results for single and multiple STATCOM and DG, the hybrid optimization technique shows superior convergence performance.

Mostafa Q. Kasim and Raaed F. Hassan [62] had offers a novel approach to finite control set model predictive current control (FCS-MPCC) for regulating the performance of grid-tied multilevel inverters acting as STATCOM. A five-level asymmetric stacked multilevel inverter (ASMLI) is controlled using this control technique, and it is connected to the network via an LCL filter. The FCS-MPCC's cost function takes into account the problems that multilevel inverters face due to unbalanced capacitor voltage and the need for an

effective dampening technique for LCL filters. There are two ways to design the FCS-MPCC strategy. The conventional approach, which involves 729 calculations for each sample instant, is the first way. Since the first technique requires 27 calculations at each sample instant, an efficient calculation method has been offered as a backup. To make sure that the suggested approach has no impact on STATCOM performance, these two approaches are contrasted. Both of these models are simulated using MATLAB and Simulink. The outcome shows that the suggested way, with balanced capacitor voltage, dampened filter performance, and no loss of reference traceability, decreases implementation time five times faster than the alternative method.

Table 2.1: Comparison table for related works.

SL no	Author	Techniques	Advantages	Disadvantages
1	ErfanAzimi et al. [34]	X-Type multilayer inverters (MLIs)	• Reduction in the number of semiconductor components compared to other topologies, leading to lower implementation costs. • Detailed investigation of modulation strategy, capacitance calculation,	• Limited discussion on potential challenges or limitations in specific operating conditions. • No mention of scalability or adaptability to different power levels or grid requirements.

			and losses, ensuring optimized performance.	
2	Kaibalya Prasad Panda et al. [35]	17-level SC MLI	• Reduced switch single-source SC MLI introduces quadruple boosting ability with only 12 switches and three capacitors. • Simulation and experimental investigations demonstrate structural operability under various conditions, including changes in load, supply voltage, power factor, and frequency variation.	• Detailed implementation and complexity of the reduced switch single-source SC MLI may pose challenges in practical application. • Real-world performance may vary from simulation and experimental results.
3	MarifDaula	switched-	• Utilizes a	• Detailed

	Siddique et al. [36]	capacitor based boost multilevel inverter topology (SCMLI)	lower voltage rating of capacitors, potentially reducing cost and improving efficiency. • Utilizes the SHEPWM technique for pulse generation, effectively removing dominant lower order harmonics from the output voltage waveform.	implementation and complexity of the topology may pose challenges in practical application. • Real-world performance may vary from simulation and experimental results.
4	Mohammad Fahad et al. [37]	Dual input SCMLI	• Demonstrated the operation of the proposed SCMLI and showcases its self-balancing property of capacitor voltages, enhancing stability and efficiency.	• Detailed implementation and complexity of the SCMLI topology may pose challenges in practical application. • Real-world performance may differ from simulation and

				experimental results.
5	Yaoqiang Wang et al [38]	Switched-capacitor circuits (SCCs).	• Utilizes capacitors as auxiliary power to boost output voltage in series mode, enhancing voltage boosting capability and efficiency. • Cascade two switched-capacitor circuits with a polarity generation circuit to achieve desired output voltage levels for symmetric and asymmetric DC source configurations. • Lower number of circuit	• Detailed implementation and complexity of the novel switched-capacitor circuit may pose challenges in practical application. • Real-world performance may differ from theoretical analysis and simulation results.

			components compared to existing multilevel inverters, reducing complexity and cost.	
6	PrabhatRanjanBana et al. [39]	DSC MLI	• Utilization of capacitors to synthesize voltage levels reduces the source count significantly, optimizing overall size and cost of the system. • Less than 50% of switches are in conduction for synthesizing any voltage level, indicating lower conduction loss of the proposed	• Computational complexityduring the processing of this approach.

			MLI, potentially improving efficiency.	
7	Yat Chi Fong et al. [40]	Step-up switched-capacitor (SC) multilevel inverter (MLI)	• A special gate drive is presented to reduce the complexity of the driver, potentially enhancing reliability and efficiency. • Equivalent impedance transformation allows modeling of the charging path of the SC network with a resonant inductor by a simple series RLC circuit, aiding in analysis and design optimization.	• Limited discussion on potential drawbacks or limitations in specific operating conditions or environments. • Detailed implementation and complexity of the soft-charging technique may pose challenges in practical application.
8	SaeidDeliri et al.	High step-up	• Use of two	• Reduction in

	[41]	switched-capacitor	half-bridges instead of a full-bridge to create negative steps reduces switch count and total voltage stress, potentially improving reliability and efficiency. • High-quality and low THD output voltage may eliminate or downsize the need for an output filter, reducing overall system complexity and cost.	semiconductor device count may result in limitations in terms of achieving desired voltage levels or performance characteristics.
9	Kasinath Jena et al. [42]	Step-up 3-φ switched-capacitor multilevel inverter.	• Fewer switching components reduce complexity and cost.	• The fact that one capacitor is being used to charge another capacitor is the primary issue

			• Mathematical modeling allows for precise analysis of performance, losses, and efficiency.	with this arrangement.
10	AnzarAhmadet al. [43]	SCMLI (switched-capacitor multilevel inverter)	• Utilizes a combination of switched-capacitor cell and cascaded H-bridge module for improved functionality. • Achieves maximum output voltage level by connecting capacitors in series with the DC source voltage.	• Conventional two-level inverters suffer from high total harmonic distortion (THD) and require higher blocking voltage rating devices, limiting their application to a small power range.
11	Junfeng Liu et al. [44]	A hybrid seven-level inverter integrating the switched-capacitor technique.	• Lower voltage stress on devices and switches, leading to the requirement of only low-	• Limited to low-frequency outp ut occasions by the unbalance of the floating capacitor.

			voltage devices. • Direct synthesis of a staircase output from a low-voltage input source makes the proposed topologies particularly suitable for such applications.	
12	Sze Sing Lee et al. [45]	MLI (1SCI-MLI)	• Resolution of high voltage stress experienced by existing counterparts. • Reduction in switch count, enhancement of voltage boosting gain, and decrease in the number of DC sources. • Validation of proposed topologies	• MLI requires a considerable number of sensors and complicated voltage balance control of floating capacitors across each H-bridge.

			through simulations and experiments, confirming conceptual validity and operational effectiveness.	
13	Dhananjay Kumar et al. [46]	RD-MLIs	• Utilization of the LS-PWM technique for control ensures effective operation, validated by simulation and experimental results. • Cost-effective and efficient, it provided additional benefits beyond fault tolerance.	• Limited low frequency output.
14	ASGHAR TAHERI et al. [47]	(SC-Type) inverter	• Offered versatility for various applications in medium-to-	• However, it becomes complicated to strike a balance in the voltage

			high voltage systems. • Required the fewest components, experiences the lowest power losses, and has fewer blocked voltage values in switches compared to alternative topologies.	of the capacitors.
15	AbhinandanRoutray et al. [48]	13-level SC-MLI	• Achieved reduced voltage stress and requires fewer active and passive components while utilizing a single DC voltage source. • Capacitor voltage balance is achieved without the need for	• It was evident that the output voltage was generated first, followed by the output current.

			additional circuits, simplifying design and implementation.	
16	Tapas Roy et al. [49]	switched capacitor converter (SCC)	• Capable of producing boosted multistep DC voltages from a single DC source, utilizing trinaryasymmetrical patterning for capacitor charging. • Cost-effective compared to most other SCMLIs for symmetric DC source configurations, making it suitable for various applications, including solar PV standalone	• The overall cost comparison of the proposed approach was very high.

			systems.	
17	Mohammad Ali Hosseinzadeh et al. [50]	Simple multicell switched-capacitor MLI	• Enhancing affordability for PV applications. • Demonstrated good performance for stand-alone and grid-connected PV applications while reducing costs.	• Less accurate
18	M. JagabarSathik et al. [51]	cross-connected compact switched capacitor (C3SC)	• Reduced the number of conducting switches and gate drivers, thereby enhancing efficiency. • Equal charging and discharging of floating capacitors (FCs) minimizes capacitance requirements.	• It was an active role in the charging current route, which results in considerable high thermal stress.

19	N. Sandeep et al. [52]	Nine-level inverter based on switched-capacitors (SCs)	• It had a self-balancing capability, offering enhanced performance • Offers structural and operational improvements for high power-quality DC-AC power conversion systems.	• Large voltage deviation
20	Amir Taghvaie et al. [53]	DC to AC converter	• Low losses calculation and acceptable efficiency demonstrate the effectiveness of the proposed converter for its intended applications. • Generated a staircase multilevel voltage, providing	• However, the voltage stress of each switch increases by voltage level increment as well as increasing the number of series diodes.

			flexibility and efficiency.	
21	MarifDaula Siddique et al. [54]	Multilevel inverter	• Detailed comparative analysis confirms the superiority of the proposed topology over existing alternatives. • Enhances the reliability and validity of the proposed solution.	• However, the unequal voltage step increases the harmonic content of the output voltage.
22	M. JagabarSathik et al. [55]	Compact switched capacitor multilevel inverter	• Capacitor voltages remain unaffected by load variations, ensuring stability and reliability. • Limited voltage across each switch to Vin, reducing the number of	• Comparatively not minimize the number Of a DC source.

			active switches and minimizing power losses.	
23	HamedJalalat et al. [56]	GA	• Reduce computational complexity	• Useful for a limited number of buses
24	M. S. Giridhar et al. [57]	MOA	• The voltage profile was improved	• It may cause losses.
25	MostafaElshahed et al. [58]	AROA	• Computational time was less, and attained reactive compensation	• Large voltage deviation
26	K Radha Rani et al. [59]	IBES	• Voltage stability was improved.	• The size was increased.
27	Samson OladayoAyanlade et al. [60]	FA	• The active and reactive power were reduced.	• Performance was not improved.
28	Anzum Ansari et al. [61]	TLBO-PSO	• Better convergence performance	• Execution time was not analyzed.
29	Mostafa Q. Kasim and Raaed F. Hassan [62]	ASMLI	• Reduced computational burden	• Less accurate

2.3 Research gap

There are some research gaps in the field of power electronics, and multilevel inverters are highlighted by the limitations identified in the reviewed literature across a number of proposed topologies and approaches. The lack of adequate consideration of potential difficulties or disadvantages in particular operating locations or conditions is one obvious omission. Although many of the suggested solutions have theoretical advantages, there may be difficulties and restrictions with their actual application that are not adequately discussed in the literature. Furthermore, the disparity between experimental and simulation results and real-world performance emphasizes the necessity of additional verification and improvement of suggested approaches. Furthermore, a number of topologies and methodologies present practical difficulties due to their intricate implementation and intricacy, indicating the need for more efficient and useful solutions.The literature review identifies a number of research gaps in the multilevel inverters (MLIs) and power electronics fields that are directly related to the objectives of this research. Bulky, intricate, and expensive designs are the result of existing switched-capacitor inverter topologies' inability to attain a high voltage step-up ratio without appreciably increasing the number of components. This indicates that a small, high-gain switched-capacitor MLI with a single DC source and a low number of switches is required, as stated in the first two research objectives. The number of inverter designs have demonstrated encouraging theoretical performance, but little research has been done on how best to use them in real-world power distribution networks. In accordance with the third research goal, this work fills the vacuum left by the majority of studies' neglect of optimization methodologies for integrating MLIs into actual grid systems by applying the Green Anaconda Optimization (GAO) method to determine the best placement. Lack of validation on common test systems, like the IEEE 9-bus distribution system, is another weakness. Many suggested techniques find limited application in simulation environments due to insufficient experimental validation. This serves as motivation for the fourth objective, which is to verify that the suggested MLI works in a well-known test system. The performance of MLIs in dynamic fault conditions when used as a STATCOM has also received limited attention, despite the fact that some research has looked into power quality improvement. The fifth aim looks at how the suggested MLI can improve power quality and stability during distribution system outages in order to address this issue.This research gap includes the requirement for low-complexity, high-gain inverter designs; optimizing their integration into power networks; effectively validating using conventional test systems; and

analyzing performance under fault conditions.

2.4 Summary

This chapter reviewed many existing papers related to Capacitor Step-Up Multilevel Inverters.The emergence of compact design power converters has revolutionized various applications, including photovoltaic systems, active power filters, high-frequency AC systems, and more. Among the innovative solutions, multilevel inverters (MLIs) have gained significant attention due to their ability to address key challenges in power conversion. MLIs offer advantages such as improved power quality, reduced harmonic distortion, enhanced voltage control, and increased efficiency compared to traditional inverters. These benefits are particularly crucial in applications like photovoltaic systems, where maintaining stable voltage levels is essential for optimal energy harvesting. Additionally, MLIs find applications in active power filters for mitigating harmonics and improving grid stability, as well as in high-frequency AC systems for efficient power transmission and distribution.

CHAPTER 3

DESIGN AND IMPLEMENTATION OF A HIGH-GAIN SWITCHED-CAPACITOR STEP-UP MULTILEVEL INVERTER WITH REDUCED COMPONENTS COUNT

3.1 Overview

Green energy sources are extensively used to lessen reliance on systems that rely on fossil fuels and, consequently, pollution. Although renewable, green energy sources are erratic in nature. Therefore, it becomes crucial to use them appropriately while maintaining the maximum level of power quality as required by the load or the grid. This is made possible in large part by the control of numerous power electronic converters. The core of these systems is an inverter, which is a type of power converter that conveniently transforms DC to AC. Over the years, a great deal of research has been done to build new inverter topologies. Recently, multilayer inverters (MLIs) of two, three, and more levels have been created for various applications [63]. MLIs have left its mark on applications, including solar photovoltaic (PV) systems, electric vehicles, FACTs, etc., in comparison to the previous structures. This can be attributed to benefits including reduced dv/dt stress, little magnetic interference, and superior output quality [64-67]. The flying capacitor type, neutral point clamped type, and cascaded H-bridge (CHB) type are the most practical and traditional MLIs [68]–[70]. The other two types of MLI are not as useful in various applications as the CHB MLI because of problems like using more diodes, adding more capacitors, having a voltage unbalancing problem across the capacitor, neutral point potential balancing, etc.

On the other hand, CHB MLIs have been used extensively because of their simplicity and versatility. It is made up of multiple DC sources that are linked to separate H-bridge modules. The generation of the staircase multilevel output is contingent upon the availability of DC sources. Said another way, it satisfies the criterion for PV applications by producing the step-up output from a single DC source. Furthermore, a compact MLI structure with greater power quality must be designed due to the huge number of switch requirements that require special attention. Diminished switch, the greatest substitute offering a compact and modular architecture,is MLIs. In PV and battery energy storage applications, many symmetrical and asymmetrical topologies that have been recently proposed in [71]–[73] have proven beneficial. Comparatively speaking, symmetrical structures require a greater number of switches than asymmetrical ones. These structures are also capable of functioning in low power factor and unity power factor scenarios in various bidirectional modes. The voltage

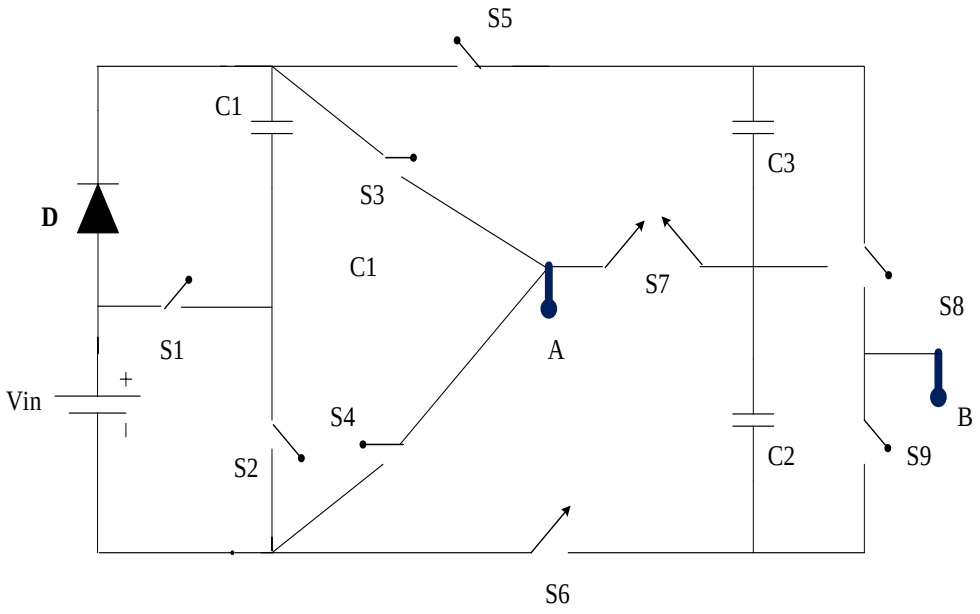
stress across the switches, however, is an important factor that cannot be disregarded. The voltage stress increases because some parts of the construction use an H-bridge. Furthermore, even decreased switch MLIs still cannot achieve the needed step-up output synthesis from a single source in PV applications. Switched-capacitor (SC) type MLIs are the subject of new advancements aimed at resolving the problems associated with step-up voltage demand. While these SCs are charged in parallel with the source, the capacitors in SC-MLIs are discharged in series to provide a step-up output. Another benefit of the recently suggested SC-MLIs is that capacitor voltages are naturally balanced in this fashion. The SC-MLIs that are suggested can produce greater voltage steps by further generalizing their capacity to synthesis a 9-level output. Despite synthetic staircase output, these systems require high voltage rating switches due to their limited step-up voltage capabilities.

For PV applications, step-up SC-MLIs, which were created early in [74], [75], are appropriate substitutes for the current structures. Higher voltage steps at the output can be produced by extending these arrangements. The step-up output is naturally produced by both structures using the same series-parallel voltage balancing method that was previously mentioned. The former, however, can handle any kind of load, whilst the latter can only handle unity or high power factor. The H-bridge need in both MLI topologies is a significant problem. Compared to the previously studied MLIs, the new structure presented in [76] uses comparably fewer components to create a 9-level output. Nevertheless, it is also constrained by the high voltage stress caused by the H-bridge, and the voltage gain is only twice as large for a 9-level output. Although [77] and [78] eliminate the problem of voltage stress caused by the H-bridge, the number of components per level is a major worry that must be avoided in light of various applications. More capacitors in the circuit result in worse quality output voltage and higher overall costs; this is discussed in [79]. One important difficulty that is avoided in the architecture suggested in [80]–[82] is the requirement for many sources. Because of their arrangement, the capacitors are charged to half the input voltage. As a result, only a twice voltage step-up output can be synthesized, although a nine-level output can have a maximum gain of four.Modern 9-level high-gain topologies have a major role in lowering the component count. An innovative technique for producing multilayer and higher voltage level output is introduced in Structure [83]. In comparison, there are fewer switches in [84]. Maximum voltage stress is still applied to several of the switches. Comparable structures can effectively lower the number of switches, as seen in [85] and [86]. Increased capacitor count

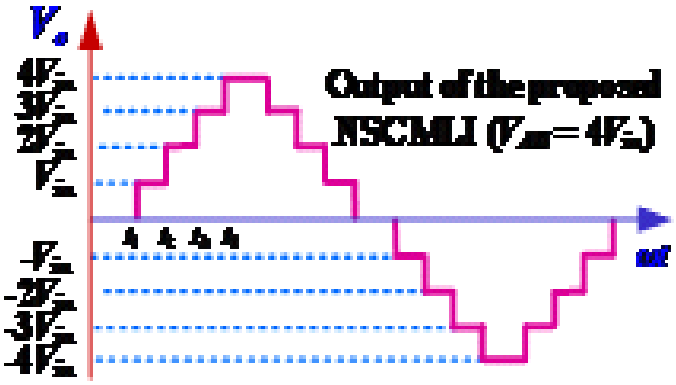
is still a problem that requires care, though. In terms of compact design, other recently created structures are competitive, as seen in [87] and [88].

3.2 Proposed Nine-level Inverter Topology

Figure 3.1 depicts the proposed NSC MLI, which comprises two distinct SC units. There are two switches (S_1, S_2), one diode (D), and one capacitor (C_1) in the first SC unit of the NSC MLI. These two switches function in different ways. The SC unit uses a single DC input V_{in}. Any green energy source, fuel cell, or renewable energy source can provide this input. The first SC unit generates two steps in the output (V_{in} and $2V_{in}$) from a single input. The other SC unit is made up of two capacitors (C_2, C_3) and seven switches ($S_3 - S_9$). Only switch number seven (S_7) is bidirectional; the other six switches are unidirectional. With the aid of polarity generating switches (S_8, S_9) and the output of the first and second SC units combined, the NSC MLI produces a 9-level AC output $(0, \pm V_{in}, \pm 2V_{in}, \pm 3V_{in}\ and \pm 4V_{in})$ from a single DC source.



(a)



(b)

Figure 3.1: (a) Proposed NSCMLI topology, (b) 9-level output of the NSCMLI

3.2.1 *Generation of the 9-level output*

Table 3.1 displays the planned NSC MLI's switching states. Minimal conduction loss is shown by the fact that less than half of the switches conduct in each level. The switches (S_1 and S_2) and (S_3 and S_4) are not designed to conduct simultaneously in order to prevent a short-circuit problem on the source side. Each mode in the suggested NSC MLI is examined in Figure 3.2 and explained as follows in order to comprehend how it operates:

- When capacitors C_2 and C_3 discharge in series under modes a and i, respectively, the peak voltage level in both the positive and negative half cycles ($4V_{in}$ and $-4V_{in}$) is produced.
- Switch S_2 is activated in modes b and h, bringing capacitor C_1, C_2, and C_3 into the load current path and producing $\pm 3V_{in}$. S_4, S_5, S_9, and S_3 switches are in the positive half cycle when they conduct, and they are in the negative half cycle when they are turned on.
- To charge the capacitors C_2 and C_3, turn on the bidirectional switch S_7 in modes c and g. Furthermore, capacitor C_1 is permitted to discharge in series with the source by switch S1. By turning on the switches S_3, S_6, S_9 in the positive half cycle and S_4, S_5, S_8 in the negative half cycle, one can also offer the load energy $\pm 2V_{in}$.
- The input source in modes d and f provides the necessary load energy, which results in $\pm V_{in}$ in the output. In this mode, capacitor C_1 is charged while the other two capacitors are in an idle state due to the activation of the switch S_2.

- Because of the way the load is linked, no energy is delivered by the source or capacitor, resulting in zero levels being produced in the output. To achieve zero level output, there are two alternative switching configurations, as shown in Table 3.1.

Table 3.1: Conduction of the Switches in Different Modes

V_{AB} (V_A- V_B)	Mode	On switch (1) and Off switch (0)								
		S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9
$4V_{in}$	*a*	0	0	1	0	1	0	0	0	1
$3V_{in}$	*b*	0	1	0	1	1	0	0	0	1
$2V_{in}$	*c*	1	0	1	0	0	1	1	0	1
V_{in}	*d*	0	1	1	0	0	1	0	0	1
0	*e*	0	0	0	1	0	1	0	0	1
		0	0	1	0	1	0	0	1	0
$-V_{in}$	*f*	0	1	0	1	1	0	0	1	0
$-2V_{in}$	*g*	1	0	0	1	1	0	1	1	0
$-3V_{in}$	*h*	0	1	1	0	0	1	0	1	0
$-4V_{in}$	*i*	0	0	0	1	0	1	0	1	0

3.2.2 *Voltage balancing and Capacitance Calculation*

Voltage balancing and capacitance calculation are critical aspects in the design and operation of multilevel inverters (MLIs), including the suggested NSC (Non-Switching Capacitor) MLI topology. Voltage balancing is essential to ensure that the voltage across each capacitor in the MLI remains nearly equal, minimizing voltage ripple and improving the quality of the output waveform. Imbalanced voltages can lead to uneven power distribution among the switches, potentially causing reliability issues and reducing the overall efficiency of the system. Various techniques, such as modulation strategies and control algorithms, are employed to achieve effective voltage balancing in MLIs. These methods aim to regulate the switching states of the switches dynamically, adjusting the voltage across each capacitor to maintain balance within acceptable tolerances. Capacitance calculation is crucial for determining the appropriate size and number of capacitors required in the MLI to achieve desired performance characteristics. Capacitors store energy and help to smooth out voltage fluctuations, reducing ripple and enhancing the stability of the output voltage. The capacitance value is determined based on factors

such as the required output voltage levels, the frequency of operation, the load characteristics, and the desired level of voltage ripple. Additionally, considerations such as the internal resistance of the capacitors and their voltage rating are taken into account to ensure safe and reliable operation of the MLI. Voltage balancing and capacitance calculation play integral roles in optimizing the performance, efficiency, and reliability of multilevel inverters, including the proposed NSC MLI topology. Through careful design and calculation, voltage balancing is achieved to minimize ripple and ensure uniform operation across the switches, while appropriate capacitance sizing ensures stable and efficient operation of the MLI under varying load conditions.

It is evident from Figure 3.2 that the capacitor C_1 is discharged in parallel during mode-c and g, while it is charged in series with the source during modes-b, d, f, and h in both positive and negative half cycles. Similar to this, during modes c and g, the energy stored in the capacitor C_1 is combined with the source to charge the other two capacitors in series. While in modes A, B, H, and I, the capacitors C_2 and C_3 discharge. Therefore, the capacitors employed in the proposed NSC MLI are considered to be self-balanced if (i) the capacitors' sizes are appropriately chosen, (ii) they are charged in series and discharged in parallel, and (iii) the charging and discharging period is maintained within a single full cycle.

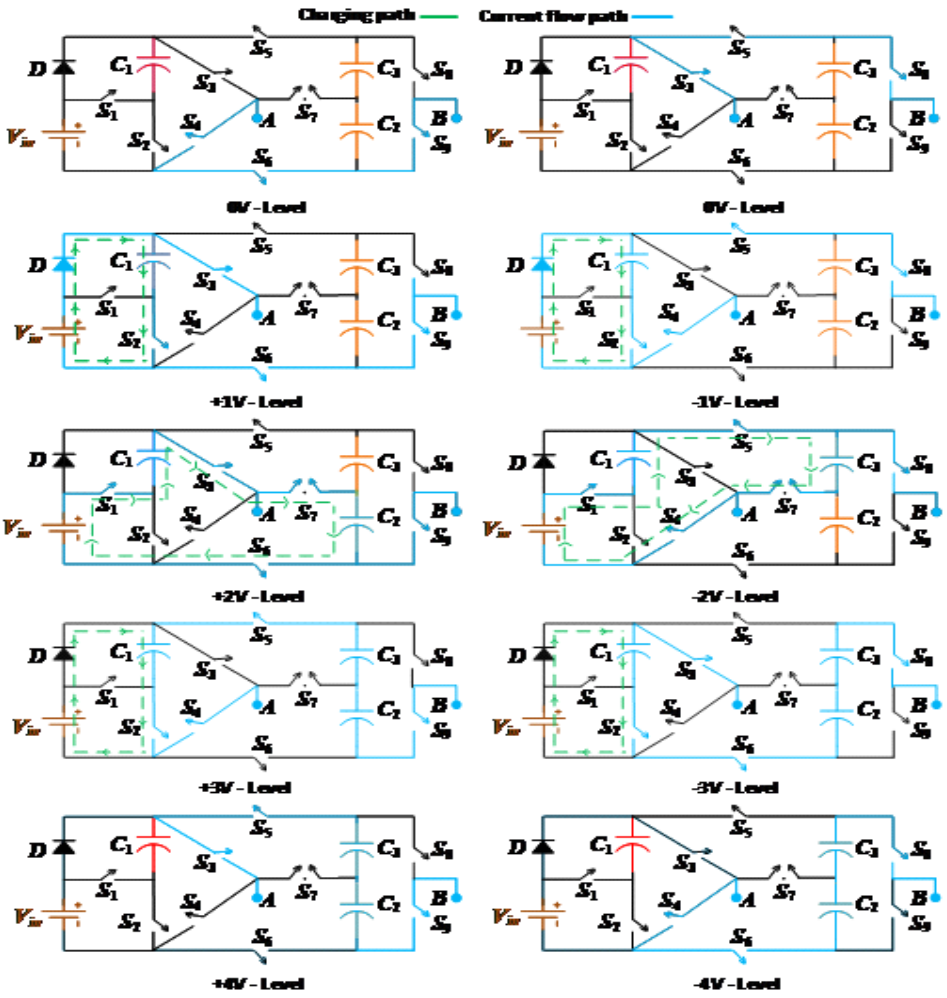


Figure 3.2: Operation of the proposed NSC MLI in both half cycles of ac output

Operational study shows that the load is powered by the capacitor. Consequently, it is best to keep the voltage ripple to a minimum. The appropriate value of capacitance, the length of the cycle's discharging time, and the circuit's loading all affect voltage ripple and voltage balancing. Limiting the voltage ripple will help to keep the overall power loss low. While the capacitor C_1 discharges during $[t_1, t_3]$, it is charged during $[t_1, t_2]$ and $[t_3, t_4]$. Comparably, C_2 releases during $[t_3, \pi - t_3]$. In light of this, the maximum discharging quantity of any capacitor can be written as follows:

$$Q_{\max} = i_{lp}.(t_x - t_y) \tag{3.1}$$

Where i_{lp} the peak is the load current and t_x *and* t_y denotes the instant of the discharging duration. As the peak load voltage is $4V_{in}$ and assuming the load resistance of R_l, (3.1) can be further simplified as;

$$Q_{\max} = \frac{4V_{in}}{R_l}.(t_x - t_y) \tag{3.2}$$

The discharging quantity can also be calculated as $\Delta Q = C * \Delta V_r$ and thus the minimum capacitance can be determined as follows;

$$C = \frac{\Delta Q}{\Delta V_r} \tag{3.3}$$

3.2.3 *Switch voltage stress analysis*

Switch voltage stress analysis is a crucial aspect in the design and evaluation of power electronic converters, especially in multilevel inverter (MLI) topologies. It involves assessing the voltage stress experienced by the switches within the circuit during operation. The voltage stress across switches determines their reliability, cost, and overall performance. In an MLI, switches are subjected to high voltages, particularly in multilevel configurations where multiple voltage levels are generated. Voltage stress analysis aims to determine the maximum voltage that the switches must withstand, which influences the choice of components and impacts system efficiency. Typically, voltage stress analysis involves examining various operating conditions, including steady-state and transient states, to identify peak voltage levels across switches. Factors such as switching frequency, load variations, and circuit topology influence voltage stress. Mitigation strategies are often employed to reduce voltage stress, such as incorporating snubber circuits, utilizing advanced semiconductor devices with higher voltage ratings, or optimizing circuit layout to minimize parasitic effects.

A crucial component taken into account when creating new MLI topologies is voltage stress. Total standing voltage (TSV) should be minimal, and this is taken into consideration in the design of the proposed NSC MLI. When the switches S_1 and S_2 are in the off condition, they can withstand a certain amount of input voltage stress. The switches can withstand up to $V_{in} + V_{c1}$ (i.e., $2V_{in}$) of stress when S_3, S_4, and S_7 do not conduct, such as in $\pm 2V_{in}$ or zero-level. The switches S_5 and S_6 can withstand a maximum stress of $V_{c3} + V_{c2} - V_{c1}$ (i.e., $3V_{in}$) while taking into account the $\pm 4V_{in}$ level. Similar to this, the switches S_8 and S_9 can withstand up to $4V_{in}$, or $V_{c3} + V_{c2}$ as the maximum stress. It is evident that just two switches whose TSV is $22V_{in}$ can sustain the highest voltage stress.

TABLE 3.2: Voltage Stress on the Switches in Each Level

V_{AB}	Voltage stress (x V_{in})								
$(V_A - V_B)$	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9
$4V_{in}$	1	0	0	1	0	3	2	4	0
$3V_{in}$	1	0	1	0	0	3	1	4	0
$2V_{in}$	0	1	0	2	2	0	0	4	0
V_{in}	1	0	0	1	3	0	1	4	0
0	1	0	1	0	3	0	2	4	0
	1	0	1	0	0	3	2	0	4
$-V_{in}$	1	0	1	0	0	3	1	0	4
$-2V_{in}$	0	1	2	0	0	2	0	0	4
$-3V_{in}$	1	0	0	1	3	0	1	0	4
$-4V_{in}$	1	0	1	0	3	0	2	0	4

3.2.4 Calculation of Power Losses in NSC MLI

The calculation of power losses in the Non-Switching Capacitor Multilevel Inverter (NSC MLI) involves several key considerations to assess its efficiency and performance. To begin with, the NSC MLI's inherent design characteristics, including the reduced number of switches and drivers, offer advantages in terms of component count and complexity compared to traditional topologies. This design choice, coupled with the avoidance of high voltage stress switches like those found in H-bridge configurations, contributes to minimized power losses and improved reliability. Central to the power loss calculation is the understanding of conduction losses, which occur due to parasitic parameters such as internal resistance and equivalent series resistance of switches and diodes. The total parasitic resistance is evaluated considering the number of switches and diodes conducting in each voltage level. By accounting for the load current path in various voltage levels, the conduction energy loss can be accurately quantified. Ripple losses stemming from capacitor charging also play a significant role. As the capacitors are charged in parallel with the DC source, voltage ripple occurs due to potential differences between the input and capacitor voltages. Balancing voltage ripple with the number of capacitors is crucial to maintain voltage quality and minimize ripple loss. Power losses in switches, diodes, and capacitors in

an SC-type MLI affect any converter's efficiency. The overall power loss is made up of three separate losses: switching loss (P_{sl}), conduction loss (P_{cl}), and capacitor voltage ripple loss (P_{rl}).

3.2.5 Switching loss calculation

Switching loss calculation is a crucial aspect in the analysis and design of power electronic circuits, particularly in devices like multilevel inverters. This calculation involves assessing the energy dissipated during the switching transitions of semiconductor devices such as switches and diodes. During operation, these devices experience transitions between their on and off states, leading to energy losses due to internal capacitances, resistances, and other parasitic effects. To compute switching losses accurately, factors such as the voltage and current waveforms, switching frequency, device characteristics, and circuit topology must be considered. The switching loss calculation typically includes both turn-on and turn-off losses, which occur during the transition of the device from conducting to non-conducting states and vice versa. Turn-on losses are primarily attributed to the charging of internal capacitances and forward voltage drop across the device, while turn-off losses stem from the discharge of these capacitances and reverse recovery currents in diodes. Various methods can be employed to estimate switching losses, ranging from simple analytical models to more complex numerical simulations. These methods often take into account the switching characteristics of the semiconductor devices, including their switching times, on-state and off-state resistances, and parasitic elements. Moreover, considerations such as snubber circuits and gate drive strategies may be incorporated to mitigate switching losses and improve overall system efficiency. Switching loss calculation plays a vital role in the optimization of power converter designs, enabling engineers to identify potential areas for improvement and make informed decisions regarding component selection, thermal management, and system reliability. Accurate estimation of switching losses aids in achieving desired performance metrics such as efficiency, power density, and reliability in various power electronic applications.

Switching transitions happen while the MLI is in operation. The internal capacitance of the switches determines both the switching speed and the loss. When the switch flips from the off to the on position, this capacitance increases and decreases [76]. Stated differently, during the switching transition, the internal capacitor (C_n) charges and discharges. Furthermore, the

energy loss can be calculated as follows, taking into account that the switches must be able to bear a voltage stress (V_n) when they are off:

$$P_{switch} = \frac{1}{2} C_n V_n^2 \quad \textbf{(3.4)}$$

Additionally, if we take into account the nominal frequency as f_n and the average number of switching transitions (N), which is dependent on the switching time, in a switching cycle, the total switching power loss for the nine switches is as follows:

$$P_{switch} = N \times f_n \times \sum_{n=1}^{9} \frac{1}{2} \times C_n V_n^2 \quad (3.5)$$

3.2.6 Conduction loss calculation

The calculation of conduction loss in the proposed NSC MLI involves assessing the energy dissipated due to the conducting switches and diodes during operation. This loss stems from the inherent resistances within the components, namely the switches, diodes, and capacitors. The conduction loss is influenced by the number of switches and diodes conducting at different voltage levels throughout the switching cycle. For instance, during specific voltage levels, the load current flows through multiple switches and diodes, resulting in varying levels of resistance. The total parasitic resistance is evaluated considering the conduction paths of the load current, accounting for both the on-state resistance of switches and diodes. Additionally, the forward voltage drop across the diodes is taken into consideration. The energy dissipation due to conduction loss is calculated based on the square of the load current and the total parasitic resistance. Furthermore, the total conduction loss is determined by multiplying the conduction energy loss by the nominal frequency of operation. This analysis provides insights into the efficiency and reliability of the NSC MLI by quantifying the energy dissipated during conduction, aiding in the optimization of component selection and design parameters for enhanced performance. When parasitic characteristics like the internal resistance and equivalent series resistance of the switches and diodes are taken into account, conduction loss happens. The total parasitic resistance can be evaluated by considering the number of switches and diodes that conduct in each instant from $t_0 - t_4$.For example, at zero-level, three switches receive the load current (i_o), which leads to a total parasitic resistance ($\mathrm{Re}\,q0$) of $3R_s$. The total parasitic resistances in each level are $(\mathrm{Re}\,q1, \mathrm{Re}\,q2, \mathrm{Re}\,q3, \mathrm{Re}\,q4)\ 3R_s + R_d, 4R_s + R_c, 4R_s + 3R_c \ and \ 3R_s + 2R_c$ where

$R_s, R_d, and\ R_c$ are the switch's on-state resistance, the diode's on-state resistance, and the internal resistance of the capacitor, respectively. This is also true when looking at the load current path in the $\pm V_{in}, \pm 2V_{in}, \pm 3V_{in}, and \pm 4V_{in}$ level. The conduction energy loss and total conduction loss are stated in (3.6) & (3.7), respectively, taking into account the forward voltage drop of the diode V_d .

$$E_{con} = \frac{1}{2}(i_o)^2(\mathrm{Re}\, q_0 + \mathrm{Re}\, q_1 + \mathrm{Re}\, q_2 + \mathrm{Re}\, q_3 + \mathrm{Re}\, q_4)V_d \tag{3.6}$$

$$P_{con} = f_n E_{con} \tag{3.7}$$

3.2.7 Ripple loss calculation

Ripple loss calculation in power electronics refers to the assessment of energy dissipation resulting from fluctuations or variations in voltage or current levels, commonly known as ripple, within a circuit or system. Ripple loss is a critical factor in determining the efficiency and performance of converters, inverters, and other power electronic devices. In a multilevel inverter (MLI) system, capacitors are often utilized to mitigate voltage fluctuations and provide smooth, regulated power output. However, during operation, these capacitors can experience voltage ripple due to factors such as switching transitions or load variations. Ripple loss calculation aims to quantify the amount of energy dissipated as heat within the system due to these voltage fluctuations. The process of ripple loss calculation typically involves analyzing the voltage ripple across capacitors during operation. This involves considering the charging and discharging cycles of the capacitors, as well as the timing and duration of these cycles. The voltage ripple is then used to calculate the associated energy loss using appropriate mathematical models and equations. Factors such as the capacitance value, voltage levels, switching frequency, and load characteristics all influence the magnitude of ripple loss in the system. Let's look at a capacitor C_1, which is charged in parallel with the DC source, to illustrate how the capacitors are charged in parallel. There is a potential difference between the input voltage and the capacitor voltage during the practical charging process. This results in voltage ripple, which can be stated as follows:

$$\Delta V_r = V_{in} - V_{cap} \tag{3.8}$$

The time instants of discharging the capacitor $[t_x, t_y]$ are given in Section IIB. The total ripple loss thus becomes,

$$P_{ripple} = \frac{1}{2} C\left(V_{in} - V_{cap}\right)^2 f_n\left(t_y - t_x\right) \tag{3.9}$$

Ultimately, the total efficiency of the proposed NSC MLI is calculated as;

$$\eta_{total} = \frac{P_{out}}{P_{in}} \times 100\% \tag{3.10}$$

where P_{out} is the output power and P_{in} is the input power.

3.2.8 Comparison of 9-level SC-MLI

Table 3.3 presents a thorough comparison between the proposed NSC MLI and the current 9-level structures in order to prove the benefits of the latter. Numerous multi-input structures as well as newly created topologies that employ a single DC source, are available. Only comparisons are made with the most recently constructed single-dc 9-level structures that resemble the suggested NSC MLI. The suggested NSC MLI has the advantage of requiring fewer components than other topologies in terms of competency in reducing the number of switches and drivers, and it does so without the need for an H-bridge (avoids the use of high voltage stress switches). Moreover, the demand for a driving circuit has decreased because one of the switches is bidirectional. In comparison to other existing topologies, the suggested circuit uses a very small number of components, just one diode. It is important to employ diodes with the understanding that when various loads are connected to the circuit, there should be a backflow path at every voltage level. Due to high ripple, using more capacitors might lower the voltage quality and increase ripple loss in the circuit. The majority of step-up MLI circuits need two or three capacitors. Power loss increases with the number of switches in the load current path, as was covered in Section III. Only a minimum number of switches must conduct at all voltage levels for the planned NSC MLI. One further noteworthy benefit of the suggested construction over alternative architectures in [74], [75] is that only two switches out of all the switches need to be able to bear the highest amount of stress. This is because the H-bridge is not used to generate the AC output at the load.

One important factor that determines cost and dependability is the voltage stress across the switches. The maximum blocking voltage for the majority of structures that resemble the NSC MLI is 1 per unit. That being said, the total blocking voltage is still minimal for a few topologies at most. In [83], for example, it is minimal but comes at the expense of a significant number of switches. The comparison takes into account a number of factors, which might not fully support the benefit of the new design. Therefore, a performance factor

(P_f) is generated and provided as follows in order to further validate the benefit of the proposed NSC MLI:

$$P_f = \sum_{i=A}^{I} \frac{W_i \ parameter_i}{N} \quad (3.11)$$

Where W the weight is constant and N is the number of output voltage levels. The parameters A to I are specified in Table 3.3. To assess, two values of W, 0.5 and 1.5, are chosen.

TABLE 3.3: Comparison of Single-input Switched-capacitor 9-level MLI Topologies

Parameters	**A**	**B**	**C**	**D**	**E**	**F**	**G**	**H**	**I**	**J**	**K**
[74]	10	10	3	3	5	4	4	1	5.5	YES	YES
[75]	8	8	3	6	5	4	4	1	5.5	YES	YES
[76]	9	9	2	2	5	4	2	1	5.75	YES	YES
[88]	9	9	2	1	5	4	4	1	6	YES	YES
[89]	12	12	4	0	8	2	1	1	6.5	NO	NO
[68]	12	12	1	0	6	2	1	1	6	NO	NO
[83]	19	19	3	0	8	0	4	0.25	4.75	NO	YES
[85]	12	12	3	0	6	2	4	1	6	NO	YES
[86]	12	12	2	0	5	0	4	0.5	5.25	NO	YES
[80]	11	11	2	0	7	0	2	0.5	5	NO	YES
[82]	11	10	3	0	6	0	2	0.5	5	NO	YES
[81]	10	10	2	3	5	2	2	1	5.75	NO	YES
Proposed	**10**	**9**	**3**	**1**	**5**	**2**	**4**	**1**	**5.5**	**NO**	**YES**

A: Number of switches, **B:** Number of driver circuits, **C:** Number of capacitors, **D:** Number of discrete diodes, **E:** Maximum switches conducting in the load current path, **F:** Number of peak voltage rated switches, **G:** Gain, **H:** Maximum blocking voltage (per unit), **I:** Total blocking voltage (per unit), **J:** H-bridge required, **K:** Step-up voltage ability

Analyzing design parameters such as switches, capacitors, diodes, and driver circuits can help to better understand the circuit's performance and efficiency.

- The number of switches produces nine voltage levels from a single DC input; the topology usually employs multiple power electronic switches (MOSFETs/IGBTs).

Fewer switches than conventional cascaded H-bridge inverters enhance reliability and cost-effectiveness.

- Number of driver circuits: Since every switch needs a gate driver circuit, the number of active switches directly affects the overall number of drivers. The goal of optimized SC topologies is to minimize driver circuits in order to lower system costs and control complexity.
- Capacitor count: The SC inverter's capacitors are its central component, allowing for self-voltage balancing and voltage boosting.As voltage levels rise, more capacitors are needed, and the size of these capacitors affects power density, efficiency, and voltage ripple.
- Discrete diode count. Diodes are used to clamp voltage, stop reverse current flow, and allow freewheeling. A lower diode count guarantees a more compact design and fewer conduction losses.
- Maximum switches conducting in the load current path: This parameter indicates the number of switches that are operational at the same time when the load is receiving current. Efficiency is increased when there are fewer switches in the path because conduction losses are decreased.
- The quantity of switches with peak voltage ratings: Certain switches need to be able to tolerate the highest DC-link or boosted capacitor voltage. Reducing the number of peak-rated switches improves the inverter's dependability while lowering size, cost, and switching stress.

Low W indicates high weightage to the components and high W indicates high weightage to the blocking voltage. Figure 3.3 shows the comparison among different MLIs with respect to P_f . The proposed MLI [P] is therefore proven as the best alternative for 9-level high-gain output generation in a single-phase PV system.

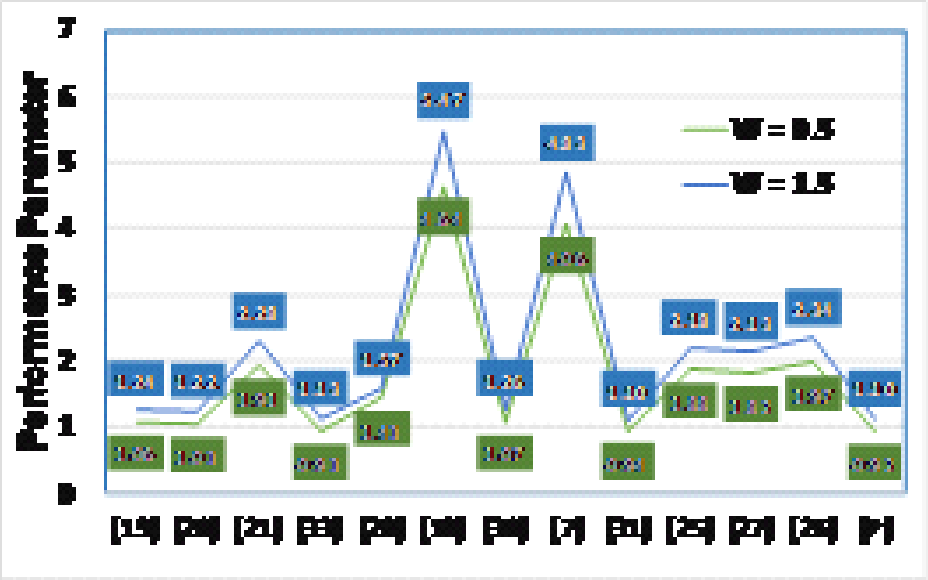


Figure 3.3: Evaluation of the Performance factor for different 9-level MLIs

3.3 Results and Discussion

3.3.1 Simulation and Experimental Analysis

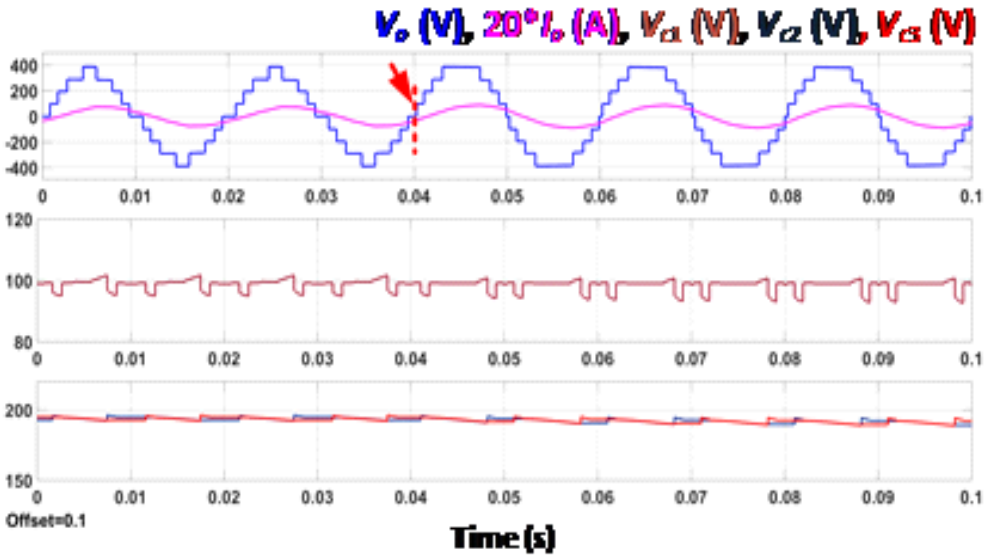
The suggested NSC MLI's operational capabilities are tested under various steady-state and transient scenarios using the MATLAB/Simulink platform. Several parameters, as shown in Table 3.4, and MOSFET switches are used in the design of the simulation setup. In the literature, various PWM control techniques have been examined. One of the basic frequency control schemes is the nearest level control scheme, which is taken into consideration here. Processing the switching signals is easier and more straightforward when using NLC. Sample points are obtained in this method by first taking into account the reference sinusoidal signal. Next, each sample point is used to rank the closest level. The switching instances are then calculated using the modulation logic specified in Table 3.1, and they are subsequently processed further to produce the pulses.

TABLE 3.4: Parameters used in Testing

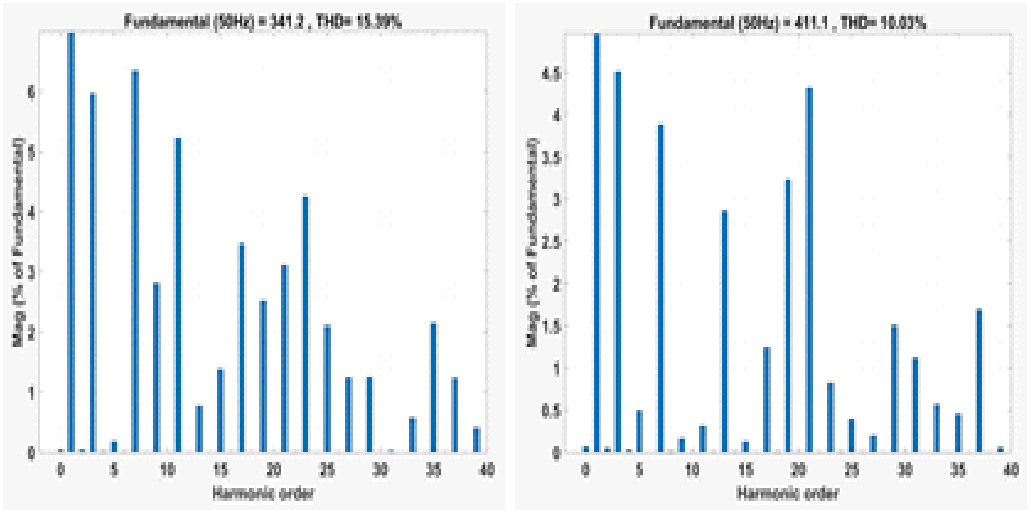
Parameters	Values
Input voltage magnitude (V_{in})	100 V
Nominal frequency (f_n)	50 Hz
Capacitors (C_1 –	1000 μF, 2500 μF, 2500

C_3)	μF
R-load (Load-A)	80 Ω
RL-load (Load-C)	120 Ω-150 mH
RL-load (Load-B)	80 Ω-150 mH

First dynamic results are produced with a modification in the modulation index from 0.2 to 0.95 in order to prove that the modulation index is indirectly proportional to the harmonics. Figure 3.4(a) displays the output voltage, current, and capacitor voltage under these conditions. According to the harmonic analysis displayed in Figure 3.4(b), the total harmonic distortion is 15.3% at low modulation indices and roughly 10% at high modulation indices.



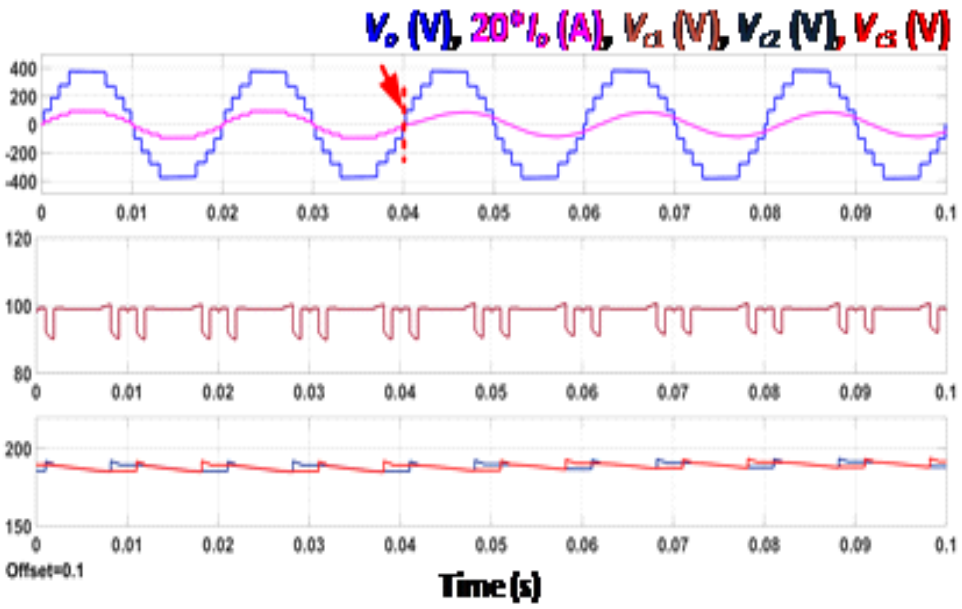
(a)



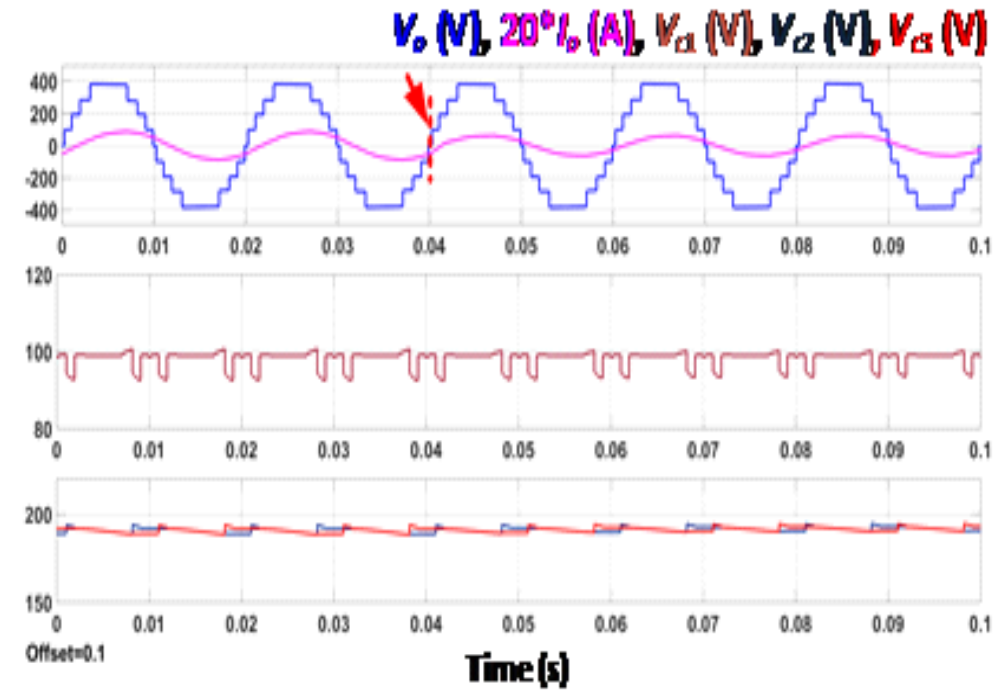
(b)

Figure 3.4: Simulation results (a) With a change in modulation index, (b) Harmonic analysis shown under high and low modulation index

The results of testing the suggested NSC MLI at various loads are displayed in Figure 3.5(a). The load is abruptly switched from A to B (see Table 3.4), and the load current is also visible to observe. When inductance is added, loading increases and voltage ripple decreases while load voltage stays constant. In a similar manner, load is increased from B to C, and the outcomes are displayed in Figure 3.5(b). It is evident that only a change in the load current is felt, with the capacitor voltages remaining important at a 1:2 ratio. Figure 3.5(c) displays the source and capacitor currents throughout charging and discharging cycles.



(a)



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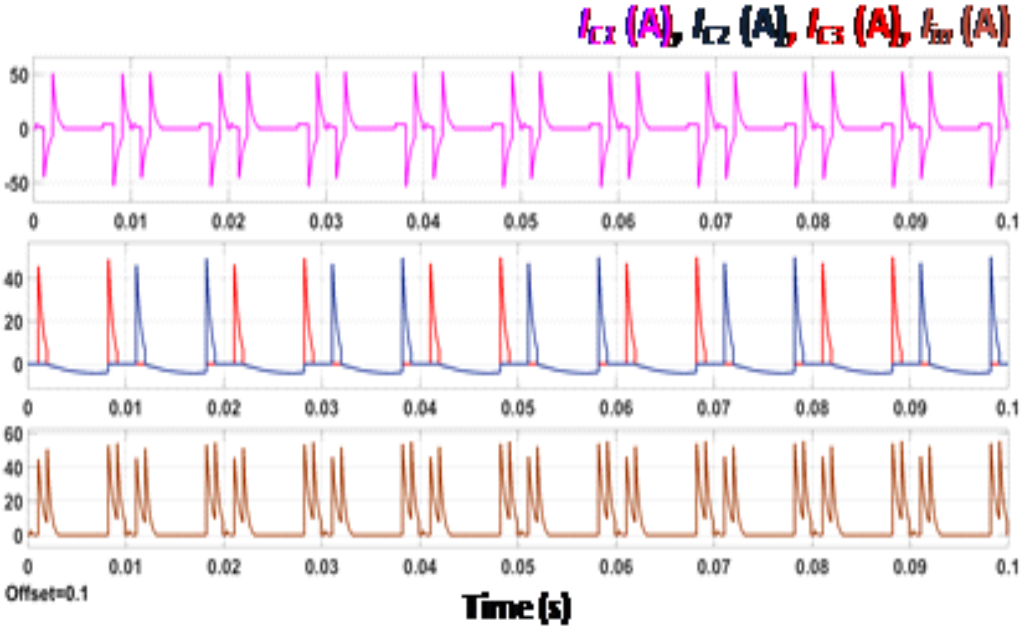
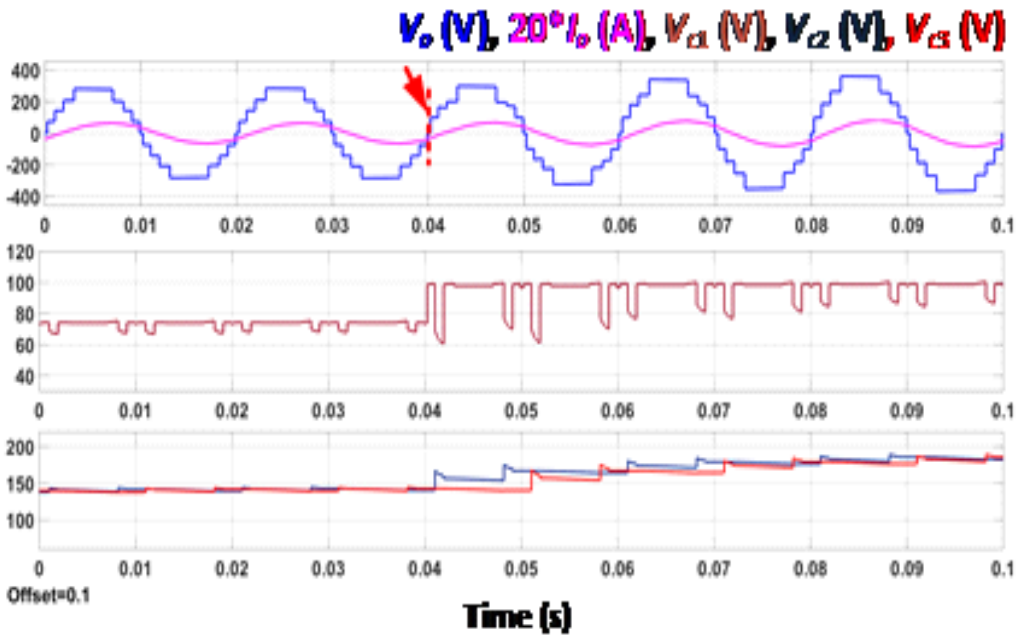


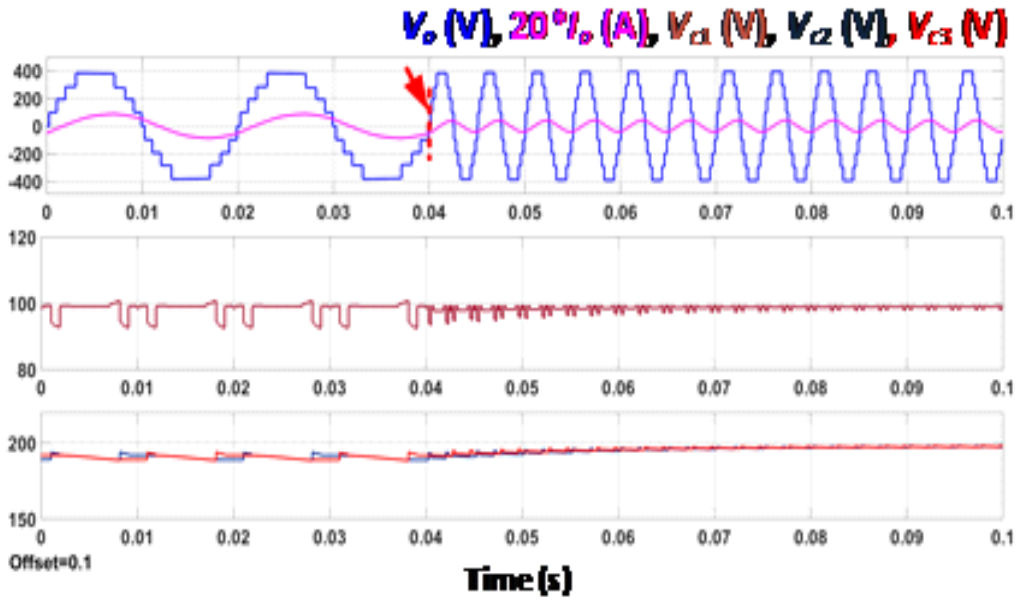
(c)

Figure 3.5: Simulation results (a) When the load changes from A to B, (b) when the load changes from B to C, (c) Current through the capacitors and input current

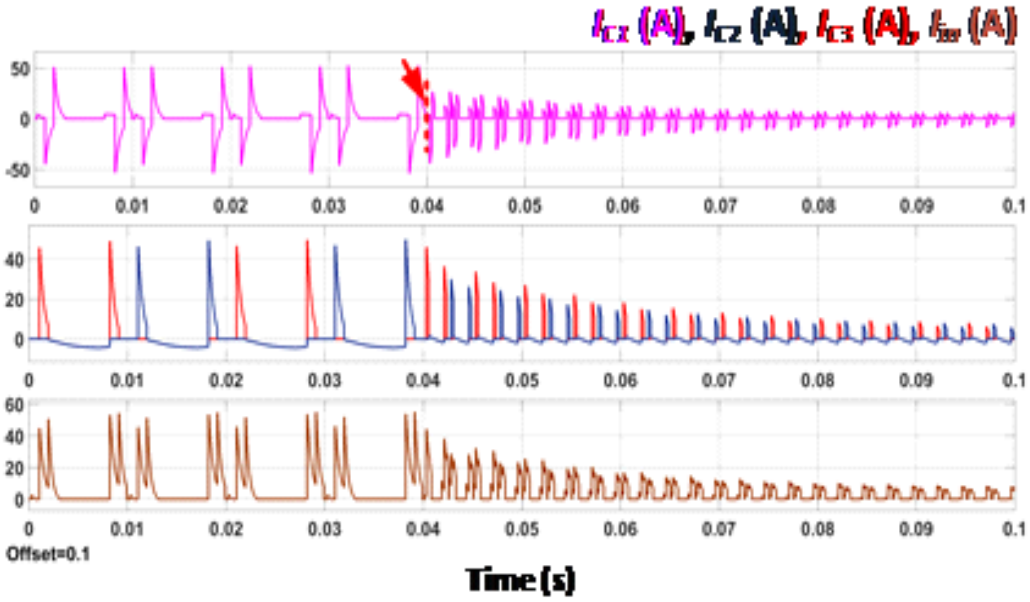
Practical PV system inverters may encounter voltage variations; in such cases, self-balancing performance evaluation is necessary. Conversely, Figure 3.6(a) verifies the self-balanced step-up voltage feature of the suggested NSC MLI. The voltage is 75 V at first and returns to the desired 100 V in 0.04 seconds. Naturally, the capacitors can follow the dynamic voltage change over the course of a cycle, resulting in a 9-level step-up output that changes the peak voltage from about 300 V to 400 V. The outcomes when there is a frequency shift are shown in Figure 3.6(b). Voltage ripple is efficiently reduced with a dynamic variation in frequency from the nominal value to fourtimes (50-200 Hz). As a result, ripple losses decrease, albeit at the expense of an increase in switching losses brought on by a rise in frequency. Due to inductive type loading, there is a natural change in load current under certain circumstances. The suggested NSC MLI is ideally suited for integration in a high-frequency ac grid application since, as Figure 3.6(c) illustrates, the current magnitude drastically decreases in the source and capacitor. The blocking voltage across the switches, as shown in Figure 3.7, is consistent with the analysis reported in Section. IIC. Additionally, one switch out of the nine switches is bidirectional, which is remarkable.



(a)



(b)



(c)

Figure 3.6: Simulation results (a) When the supply input changes, (b) When the frequency varies, (c) Capacitor currents and input current with a change in frequency

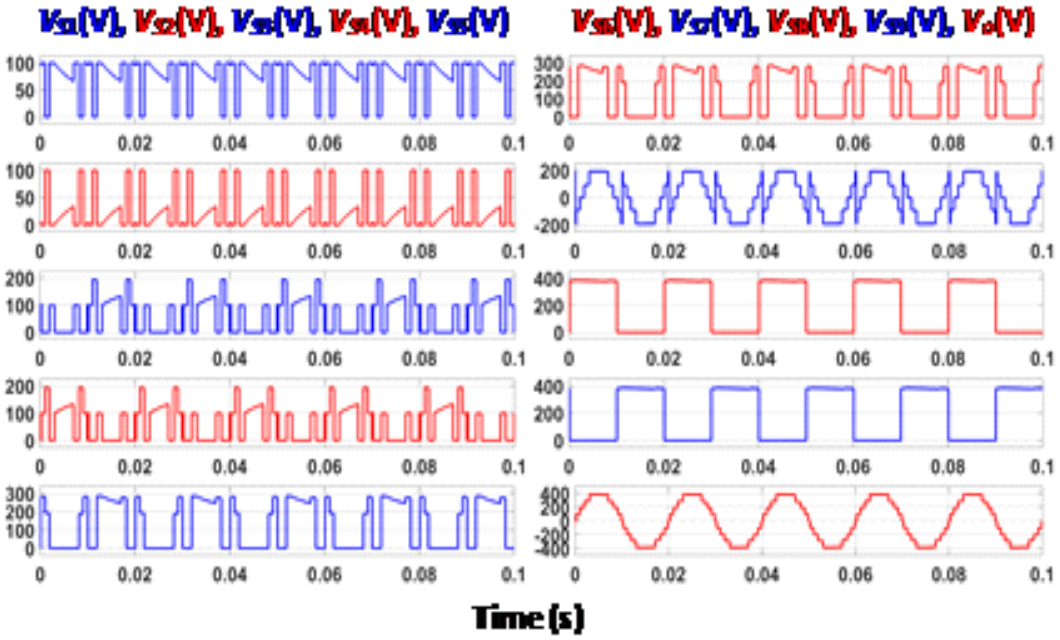


Figure 3.7: Voltage stress analysis

A further experimental test is carried out under conditions akin to those of the simulation, taking Table 3.4's parameters into account. In the lab, a test configuration with every part as illustrated in Figure 3.8 is created. MBR20200 diodes (Maximum rating 200 V, 20A) and IRFP460 MOSFETs (Maximum rating 500 V, 20A) are used in the power circuit. A 28335 DSP controller activates the switches, and a TLP250 driver circuit feeds pulses to the switches.

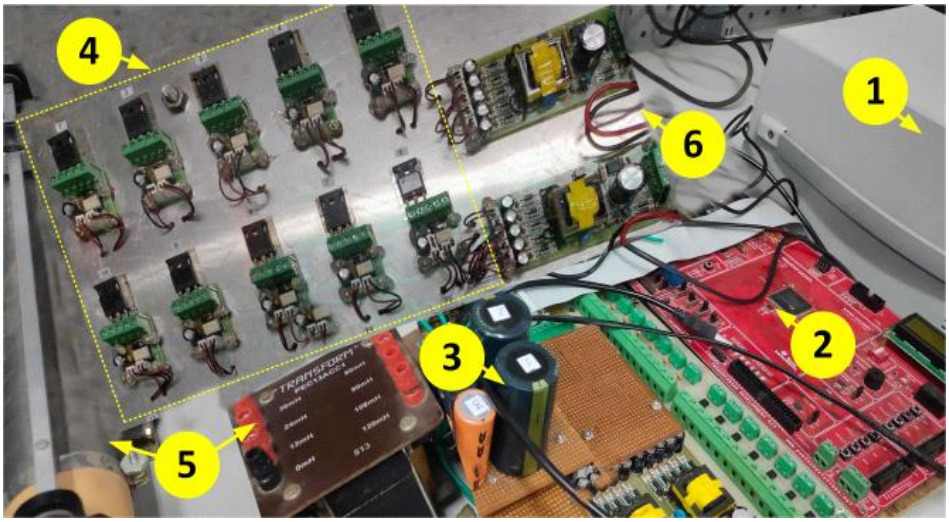
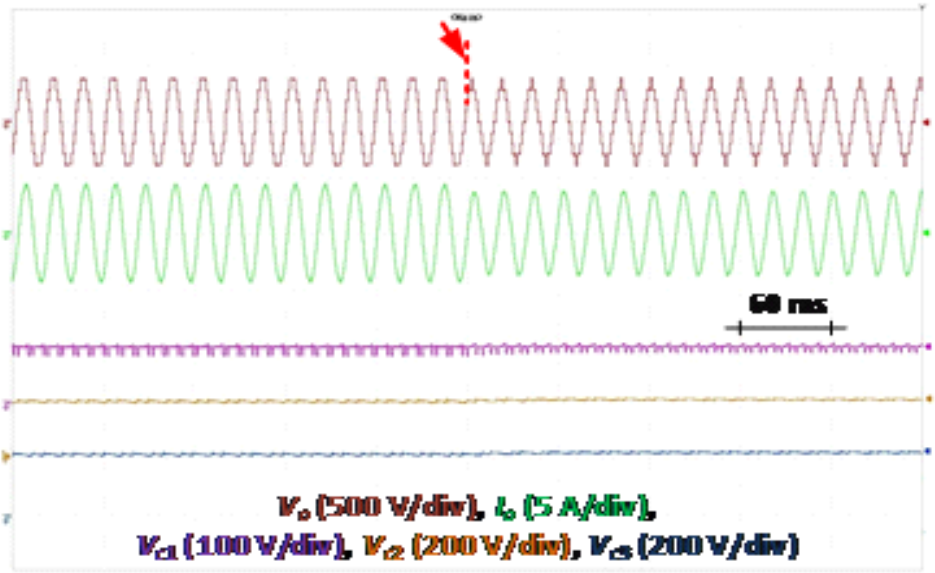
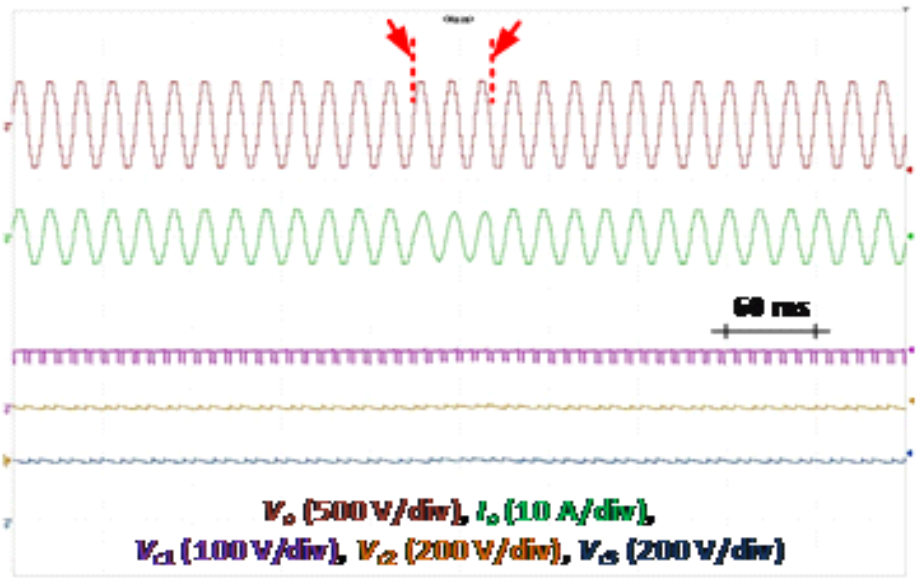


Figure 3.8: Experimental setup of the proposed NSC MLI (1: DC source, 2: DSP controller, 3: Capacitors, 4: MOSFET switches with TLP 250 drivers, 5: *RL*-load combination)

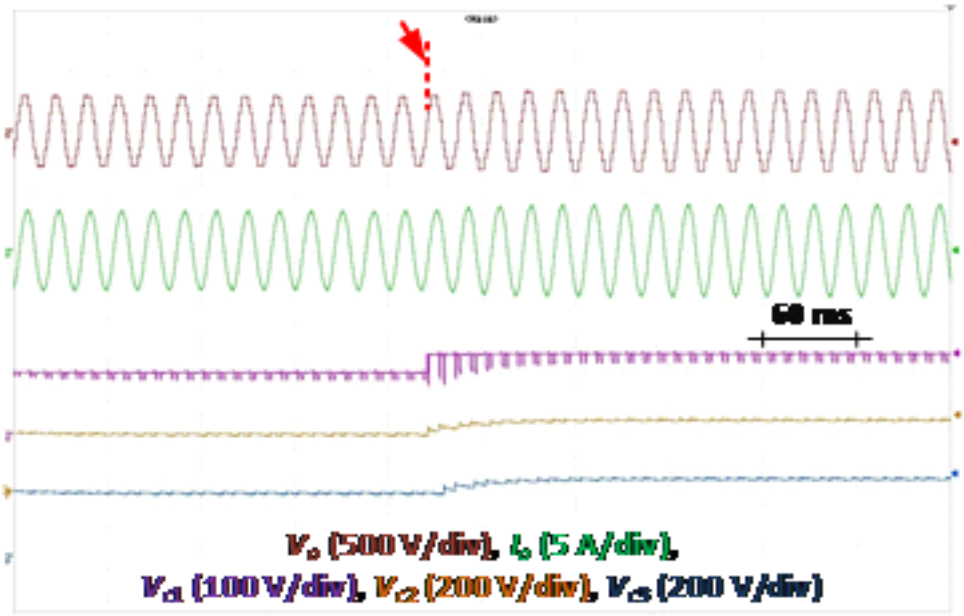
The output voltage, current, and capacitor voltages obtained when the modulation index was changed from 0.95 to 0.2 while the load was kept constant (Load-B) are displayed in Figure 3.9(a). At a lower modulation index, the average output voltage and current are decreased. Furthermore, for lower modulation indices, there is a noticeable reduction in the ripple of the capacitor voltage. The load current pattern shifts when the load moves from A to B and then back to A, as seen in Figure 3.9(b). It can be confirmed that a change in the loading causes a change in the ripple voltage across the capacitor. In the event of a load disturbance, the load voltage remains constant. A step jump of 75 V to 90 V is applied to the input voltage, and the result in Figure 3.9(c) illustrates how the capacitors naturally track the dynamic voltage shift and still generate a 9-level step-up output. The outcomes when there is a frequency shift are shown in Figure 3.9(d). Voltage ripple efficiently decreases when the frequency is changed from the nominal value to four times (50-200 Hz), which is comparable to the simulation's outcome. These findings confirm that the suggested NSC MLI can effectively generate a 9-level, 4-times boosting voltage in real-time under various brief input/output side variations.



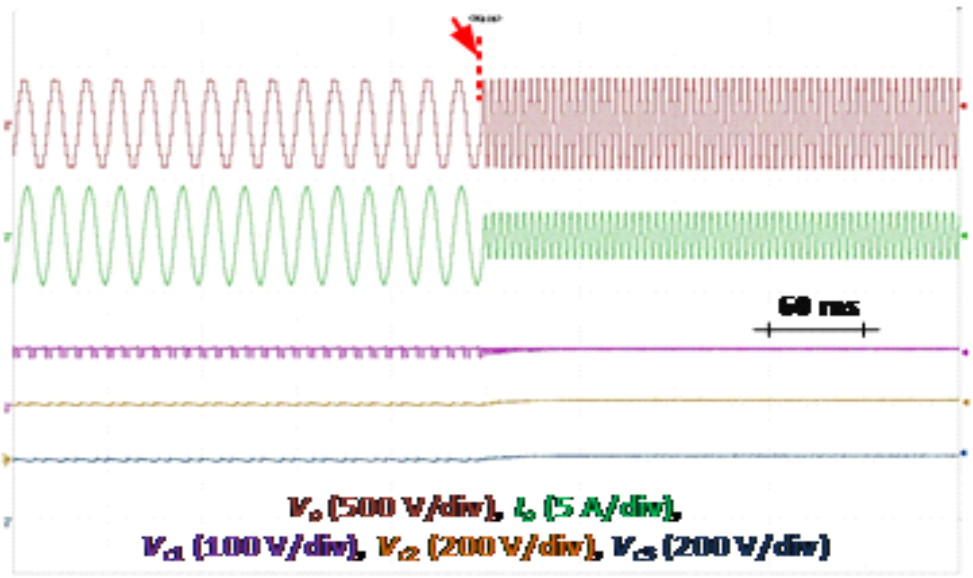
(a)


60 ms
V_o (500 V/div), I_o (10 A/div),
V_{G1} (100 V/div), V_{G2} (200 V/div), V_{G3} (200 V/div)

(b)


60 ms
V_o (500 V/div), I_o (5 A/div),
V_{G1} (100 V/div), V_{G2} (200 V/div), V_{G3} (200 V/div)

(c)



(d)

Figure 3.9: Experimental results (a) Change in modulation index, (b) Sudden load change, (c) Step change in input voltage, (d) Sudden increase in the frequency

3.4 Summary

This work presented a new MLI that was created by fusing two SC units. One of the units uses one capacitor to step up the voltage to two times the input, and the other SC unit uses two capacitors to step up the output to four times the input. Consequently, it is possible to get a high-voltage step-up output without integrating several sources. The suggested NSC MLI is designed with a minimal number of switches. As opposed to typical MLIs, which require additional voltage balancing complexity, naturally charged and discharged capacitors eliminate this issue. Power losses are studied along with a thorough topological study. The suggested MLI is more competitive when compared to the recently created single-input MLI structures since it is more effective at lowering both the voltage stress and the number of components. Simulation testing under abrupt transient conditions validates the NSC MLI's operation. The real-time operation of the proposed MLI to produce a 9-level, 4-times boosting voltage under various instantaneous input/output side changes is verified experimentally under transient conditions.

CHAPTER 4

Novel Nine Level Switched Capacitor Multi-level Inverter Based STATCOM for Distribution System

4.1 Overview

Power systems are used to provide consumers with energy that is more dependable and of higher quality while keeping costs as low as possible. To control system parameters and boost transmission capacity, these power systems are either connected in series or parallel to the grid [90]. A series of power electronic components called Flexible AC Transmission Systems (FACTS) is included in dispersed systems in order to enhance power quality [91]. Among the FACTS controllers are unified power quality conditioners (UPQC), static synchronous compensators (STATCOM), and dynamic voltage restorers (DVR) [92]. The most popular FACTS device among them is the voltage source inverter based on STATCOM [93]. To account for reactive power, a STATCOM device is introduced to the power system [94]. The STATCOM operates in capacitive mode while introducing reactive electricity into the electrical grid. It functions in the inductive mode if it receives reactive power from the system [95]. Points of common coupling are used by the STATCOM system to introduce current into the network. It produces voltage management, harmonic filtering, neutral current compensation, load balancing, and power factor correction [96]. Voltage instability is caused by the voltage source converter, which converts DC power into AC power with varying amplitude and phase angle. Reactive power can be supplied to the system through STATCOM in fixed or adjustable amounts, assisting in the maintenance of the proper voltage profile [97]. The main STATCOM component that produces a multi-level or multi-pulse type is the voltage source inverter [98].

The efficiency loss at high gain, increased switching stress, and control complexity are some of the main drawbacks of high-gain topologies that help in creating compact designs with fewer components in STATCOM applications. Additionally, they have limited fault tolerance under grid disruptions, scaling concerns at higher power levels, harmonic distortion that affects power quality, and reliability issues brought on by thermal stress. As a result, albeit helpful, their incorporation into STATCOM necessitates cautious compromises and further advancements.Power device installation in distributed systems has been done in a number of ways, both suggested and actualized. These techniques do have certain drawbacks, though, like power loss, voltage instability, lengthy computation times, etc. To address these problems, a novel approach using inverter topology was presented in this study. The potential

of FACTS-based devices to increase system stability makes them the most common in power systems. Power compensation, power balancing, and improving dynamic stability are the uses of the Static Synchronous Compensator (STATCOM), a shunt-connected device in the FACTS device family, in modern power systems. This work proposes to alleviate power quality difficulties by using a unique nine level switching capacitor based multi-level inverter (MLI) based on STATCOM. Multiple switches are connected to a single voltage source in the new inverter that is being suggested. Disadvantages to power loss and electricity quality can result from positioning STATCOM-based inverters incorrectly. The suggested system is distributed in an ideal location using green anaconda optimization (GAO), which addresses these problems. A MATLAB/Simulink tool is used to analyse the performance of the proposed inverter. Comparing this inverter to all other current conventional topologies, it requires fewer switches and achieves DC link voltage balances. A variety of defective situations are used to validate the STATCOM-based inverter in order to demonstrate its efficacy. With its nine stages, the suggested new inverter enhances power quality and makes up for the weak state. This suggested approach keeps the efficiency at 99.02% but with a significantly reduced total harmonic distortion (THD) of 1.04%.

4.2Proposed methodology

The STATCOM is a fixed regulator that can modify a few system parameters to increase power transfer efficiency based on power electronics. It has been effectively applied to transmission networks to adjust for power and voltage. This study suggests an SC-MLI architecture with nine switches that is based on STATCOM. For this reason, a unique multi-level inverter with nine levels of switching capacitors is introduced in this study. In order to function well,it needs to be positioned carefully on the transmission network. The STATCOM's performance is established by its placement inside the network. Consequently, this paper proposes an allocation method based on the Green Anaconda Optimization algorithm. Based on objective functions including voltage stability and real and reactive power losses, the suggested method determined the best position for MLI as STATCOM.An analysis of the suggested model is conducted on the IEEE-9 distribution network.The overall architecture of the proposed approach is illustrated in Figure 4.1 given below.

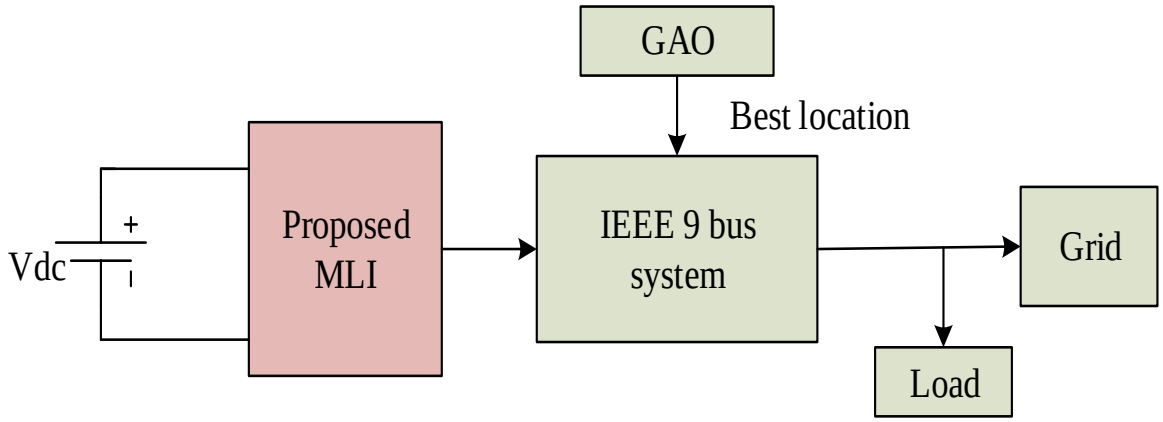


Figure 4.1: Proposed system architecture

4.2.1 GAO based allocation in IEEE-9 bus

In every developed country, electrical energy is necessary for residential, industrial, economic, agricultural, and social applications. Thus, generating stations, distribution lines, and transmission lines have evolved into crucial elements of the contemporary socio-industrial sector. The IEEE-9 bus system is used in this instance for traditional computation and simulation. Three load buses and one bus designated as a swing bus get power from a transmission line when three generators and three transformers are connected. With nine buses arranged in a certain configuration in accordance with IEEE standards, it is a specially designed grid system. This test system will take advantage of simulation. Both overhead and subterranean line systems constitute the network.It is an extremely unbalanced system with single- and three-phase laterals. It has only spot loads, not distributed loads. The GAO algorithm is used in this distributed system to set the inverter as a STATCOM with a DC source. Based on the objective function, this algorithm will determine the best spot to install the suggested inverter. The GAO algorithm's fitness is determined using the following formulas.

The primary goal of this study is to suggest a novel MLI and allocation that will lower power loss and boost voltage stability. Equation (4.1) is used to get the system's total power loss p_{Loss}.

$$p_{Loss} = \sum_{M=1}^{9} S_M * \mathrm{I}_M^2 \qquad (4.1)$$

$$\mathrm{I}_M^2 = \frac{p_M^2 + T_M^2}{v_M^2} \qquad (4.2)$$

where, M is the number of buses in the distributed system, v_M , I_M , T_M , p_M , and S_M , stand for the voltage, current, active power, and reactive power in each branch, respectively [99]. Therefore, the following describes the first objective function:

$$F_1 = \min\left(p_{Loss}\right) \quad (4.3)$$

The system voltage stability index may be used to establish the ideal DG size and location. A distribution system's voltage stability is measured by a metric called stability; a node with a high stability is one that is less likely to experience voltage collapse [100].

$$vs_{M+1} = \left|v_M\right|^4 - 4\left(p_{M+1}A_M - T_{M+1}S_M\right)^2 - 4\left(p_{M+1}A_M - T_{M+1}S_M\right)\left|v_M\right|^2 \quad (4.4)$$

where, A_M denotes reactance in the distributed system and vs denotes the voltage stability index [101]. High voltage stability is the second objective function for allocation, and it is assessed in the manner described below:

$$F_2 = \max\left(vs\right) \quad (4.5)$$

The distributed system of IEEE 9 is shown in Figure 4.2.

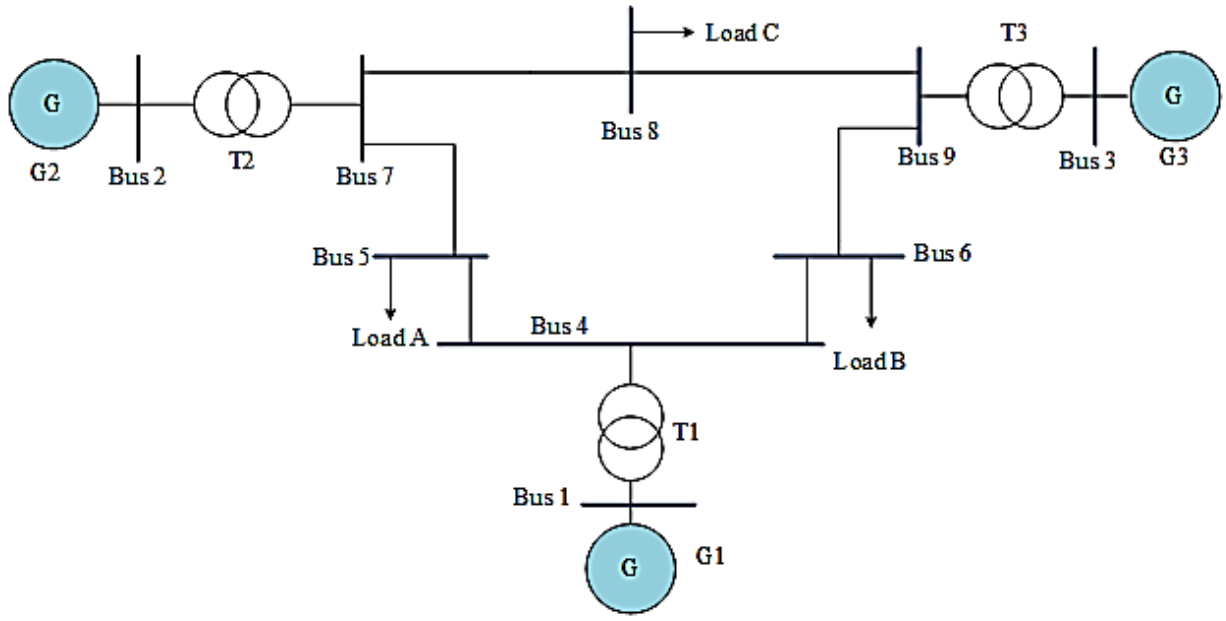


Figure 4.2: IEEE 9 bus system

Reliability, quality, and total cost can be impacted if the suggested inverter is installed in the incorrect locations. Accordingly, by taking into account each of the above described objectives at the same time, the GAO technique can be utilized to enhance the system.

Female green anaconda species leave pheromones in their wake during mating season so that the males can locate them. Males approach females by using their tongues to detect the chemical effects of pheromones, which are signs of the presence of a female species. During the mating season, the male species uses this information to determine the location of the female species and move toward them. This approach is used to update the position of green anacondas during the first phase of GAO. Large displacements in the position of green anacondas in the search space are the result of this method, which shows the exploratory capability of GAO in global search and precise scanning of the problem-solving space to prevent getting stuck in ideal local regions.

The GAO algorithm is a metaheuristic that mimics the behaviors and personalities of green anacondas. This method takes note of anaconda behavior in its natural state, including mating and hunting ceremonies. In the GAO technique, the phases of exploration and exploitation perform properly. The best spot for the suggested inverter model to be placed in the IEEE 9 bus system is determined in this study using GAO [102]. The following describes the GAO initialization process:

$$A=\begin{bmatrix} A_1 \\ \vdots \\ A_X \\ \vdots \\ A_M \end{bmatrix}_{M\times n} = \begin{bmatrix} A_{1,1} & \cdots & A_{1,E} & \cdots & A_{1,n} \\ \vdots & \ddots & \vdots & \iddots & \vdots \\ A_{X,1} & \cdots & X_{X,E} & \cdots & A_{A,n} \\ \vdots & \iddots & \vdots & \ddots & \vdots \\ A_{M,X} & \cdots & X_{M,E} & \dots & A_{M,n} \end{bmatrix}_{M\times n} \tag{4.6}$$

$$\begin{aligned} A_{X,E} &= LB_E + s.(UB_E - LB_E) \\ J &= 1,2,.....,M \\ E &= 1,2,.....,n \end{aligned} \tag{4.7}$$

where, M is the number of data, LB_E is the lower bound, UB_E is the upper bound, s is a random number between 0 and 1, n is the number of decision variables, A_X is the candidate solution in the X^{th} input data, $A_{i,E}$ is the decision variable in the E^{th} dimension, and A is the population matrix for GAO. Equation (4.8) is used to evaluate the fitness function of this approach.

$$f = \begin{bmatrix} f_1 \\ \vdots \\ f_X \\ \vdots \\ f_M \end{bmatrix}_{M\times 1} = \begin{bmatrix} f(A_1) \\ \vdots \\ f(A_X) \\ \vdots \\ f(A_M) \end{bmatrix}_{M\times 1} \tag{4.8}$$

where, f_X stands for the best value determined from X^{th} data and f indicates an objective function. The best location and the green anaconda placements are modified for every iteration, which also modifies the values in the objective function.

4.2.1.1 Exploration stage

Anaconda females locate themselves in optimal areas according to the male species. The position of the female candidate is ascertained by applying equation (4.9).

$$fd_X = \{A_{it} : f_{i_A} < f_X \;\; and \;\; i_X \neq X\}, \;\; i_X \in \{1, 2, ... , M\} \tag{4.9}$$

where, i_X indicates the row number in the GAO population matrix and fd_X indicates the list of potential locations. The green anaconda with a higher objective function value than the X^{th} green anaconda is indicated by the position number of elements in the objective function vector. The probability function of this algorithm is as follows;

$$p = \frac{CF - CF_{\max}}{\sum_{m=1}^{m_j} CF - CF_{\max}} \tag{4.10}$$

where, $CF_{\max}$ shows the greatest value, p stands for the probability of pheromone concentration, and CF indicates the set of objective function values. Using equation (4.6), the position is updated.

$$A_{X,E}^{p1} = A_{X,E} + s_{X,E}.\left(R_E^X - \mathrm{I}_{X,E} \cdot A_{X,E}\right) \tag{4.11}$$

$$A_X = \begin{cases} A_X^{p1}, & f_X^{p1} < f_X \\ A_X & else. \end{cases} \tag{4.12}$$

where, E^{th} dimension of selected female for j^{th} green anaconda is indicated by R_E^X, E^{th} dimension of new recommended position based on GAO exploration phase is represented by $A_{X,E}$, random numbers from set {1, 2} are indicated by $s_{j,E}$, and random numbers within range [0, 1] are indicated by $\mathrm{I}_{X,E}$.

4.2.1.2 Exploitation stage

The deception method used by green anacondas, which are effective hunters, involves waiting for their target underwater. The victim is attacked and surrounded by the green anaconda, which then contracts to suffocate it before swallowing it when it stops drinking water or approaches it. Using the green anaconda's hunting tactics as a guide, the population's position is updated in the second phase of GAO. The use of this technique causes the positions of the green anacondas to shift somewhat throughout the search space, indicating the capacity of GAO to be exploited in local search to find potentially better solutions close to the answers that have already been found.

The new modifications to the solution are implemented based on the anaconda hunting behavior.

$$A_{X,E}^{p2} = A_{X,E} + \left(1 - 2S_{X,E}\right)\frac{u_E - l_E}{q} \tag{4.13}$$

$$A_X = \begin{cases} A_{X,E}^{p2}, & f_{iX}^{p2} < f_X \\ A_X & else. \end{cases} \tag{4.14}$$

In this instance, $A_{X,E}^{p2}$ stands for the maximum number of iterations and represents the updated position. After all anacondas' positions have been updated, the first set of iterations will be finished, and the second phase will operate using the results of the first phase. New position and fitness function values usher in the next cycle. Because the optimal placement will be chosen in this iteration, the inverter will be precisely positioned in an IEEE 9 bus system. Figure 4.3 displays the GAO algorithm's flow chart.

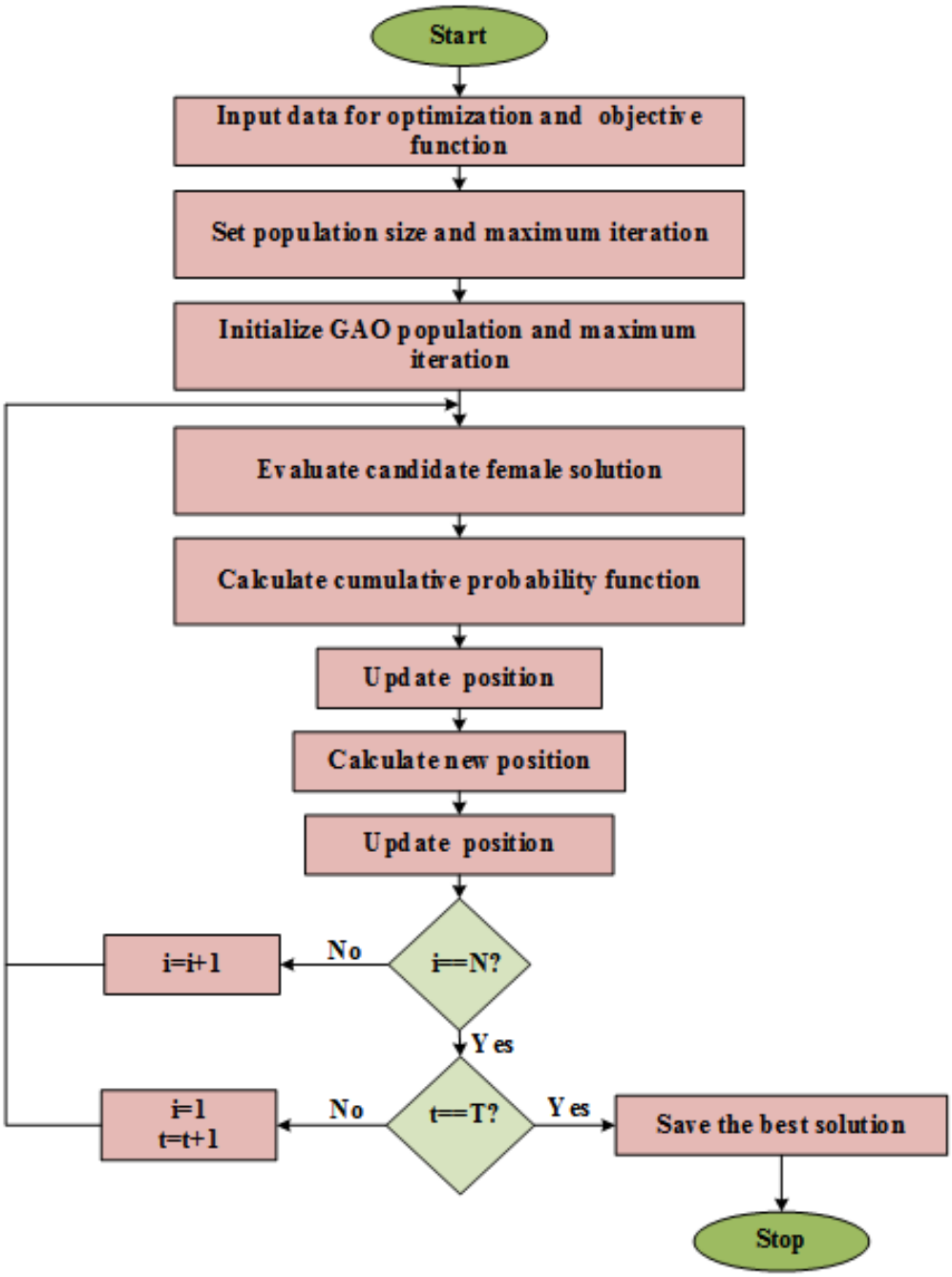


Figure 4.3: Flowchart for GAO

The first iteration of GAO is finished after revising the positions of all green anacondas in accordance with the first and second phases. Subsequently, the algorithm proceeds to the next iteration, updating itself with the new values of the objective function and the new locations of the green anacondas. The best candidate solution found during the algorithm's execution is offered as a solution for the given problem once GAO has been fully implemented.

Algorithm 1: Pseudocode of GAO
Start 1. Input optimization and objective function: variables, objective function, and constraints. 2. Set GAO population size (M) and iterations (Q) 3. Using Equation (4.7), generate the first population matrix at random. 4. Calculate the objective function 5. For *q*= 1 to *Q* 6. For i = 1 to *M* 7. **Phase 1: mating season (exploration)** 8. Identify the candidate females using Equation (4.9) 9. Calculate the concentration function of candidate females using Equation (4.10) 10. Calculate the cumulative probability function candidate females 11. Determine the selected female 12. Calculate the new position of ith GAO member using Equation (4.11). 13. Update ith GAO member using Equation (4.12). 14. **Phase 2: hunting strategy (exploitation)** 15. Calculate the new position of ith GAO member using Equation (4.13). 16. Update the ith GAO member using Equation (4.14). 17. **End** 18. Save the best candidate solution so far. 19. **End** 20**. Output:**Best quasi-optimal solution obtained with the GAO **End GAO**

4.2.2 Proposed 9 level inverter based STATCOM

The quality of the inverter voltage is influenced by the number of voltage steps. Inverter-based STATCOM detects actual power and reactive power boundaries by controlling the system current and voltage for grid utility scenarios [103]. The design of a novel switching capacitor-based 9-level MLI used in this work is shown in Figure 4.4.

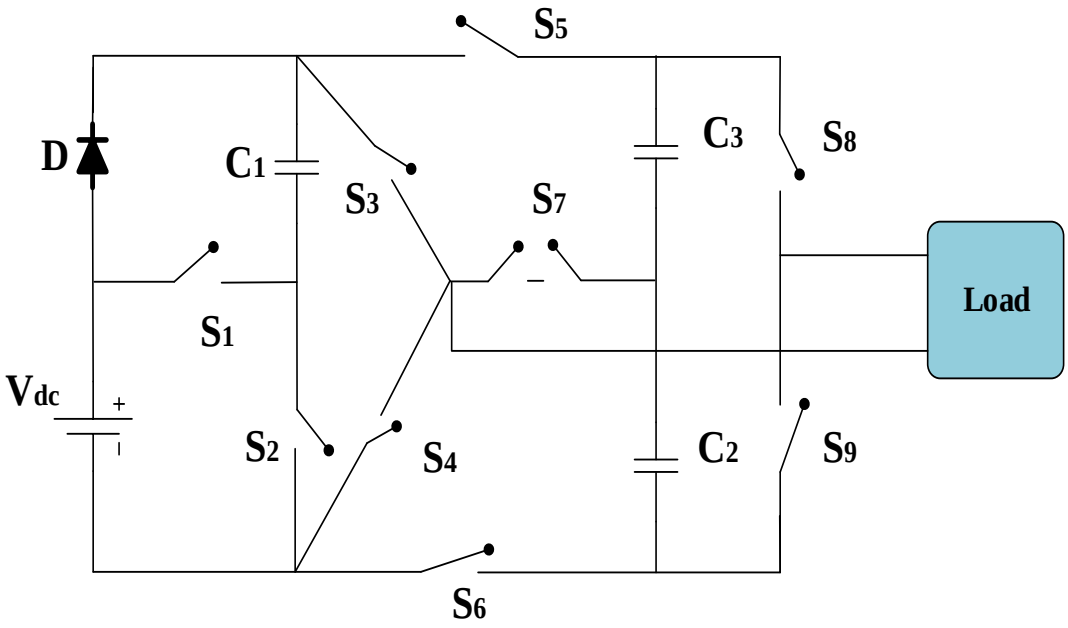


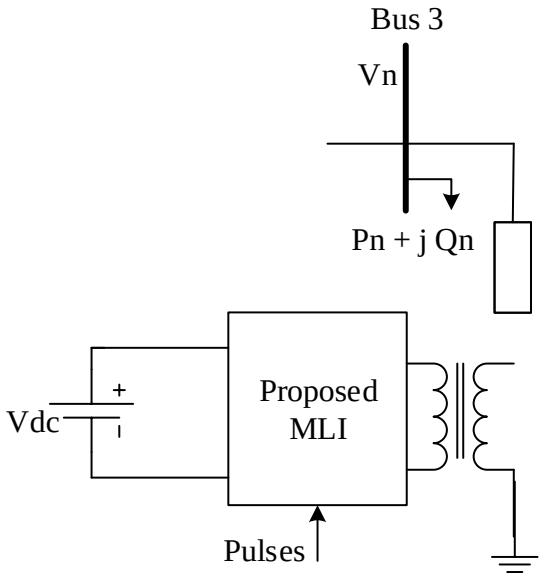
Figure 4.4: Proposed nine level inverter

This diagram shows that nine power switches, three capacitors, and one DC source make up the total architecture of the unique MLI. IGBT switches with a diode model are used in the unique inverter topology that has been suggested. S7 is the only one of these nine switches that runs in a bidirectional mode; the other switches only run in a unidirectional manner. Inverters are known as switched capacitor (SC) inverters because to their nature. A proposed inverter with capacitor charging and discharging characteristics is displayed in Table 4.2, with its switching pulses displayed.

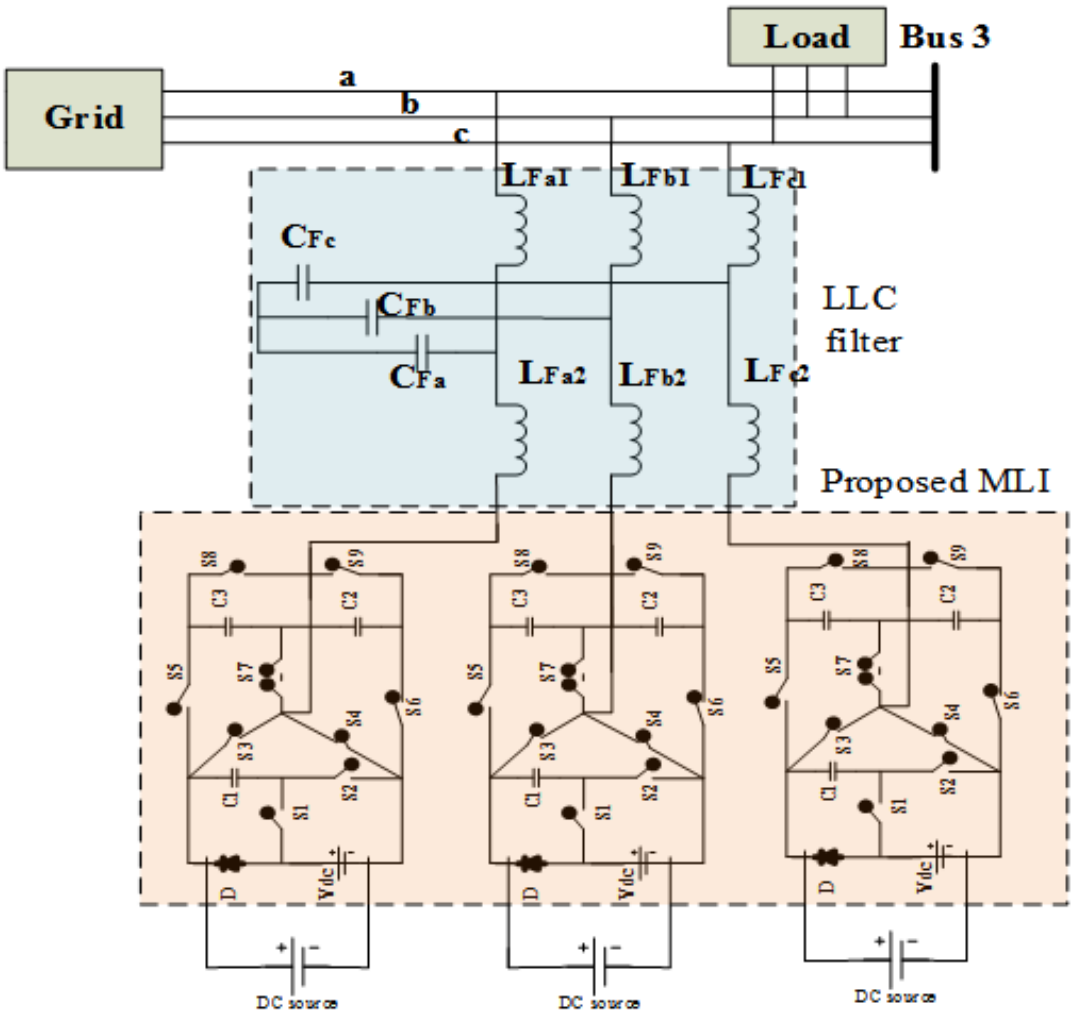
Table 4.1: Switching pulses for each switch

Modes	S1	S2	S3	S4	S5	S6	S7	S8	S9	C1	C2	C3	Voltage
1	1	1	0	1	1	1	1	0	1	C	D	D	4Vdc
2	1	1	0	1	0	1	1	0	1	N	D	C	3Vdc
3	1	1	1	0	1	0	1	1	0	N	C	D	2Vdc
4	1	1	0	1	0	1	0	0	1	N	D	C	1Vdc
5	1	1	0	1	0	1	1	0	1	N	N	N	0
6	0	1	1	1	1	0	1	1	0	D	N	C	-1Vdc
7	0	0	1	0	1	0	1	1	0	C	N	D	-2Vdc
8	0	1	0	1	1	0	0	1	0	D	N	C	-3Vdc
9	0	1	1	0	1	1	1	1	0	D	C	D	-4Vdc

With their charge pumping mechanism, these inverters simplify the process of adding levels and maintaining specific capacitor voltages.The voltage output of the inverter generation will be impacted by the converter type selected, with multi-pulse and multilayer being the two main converter topologies available for STATCOM. The converter's suitability for STATCOM implementation is further influenced by the switching method used and the harmonic content of its output [104]. MLI type converters need more switches and DC sources than multi-pulse type converters when it comes to CHB. These extra switches do, however, have a much lower rating than the multi-pulse switches. As a result, unlike with multi-pulse converters, the number of switches needed does not increase when creating an MLI. As shown in Figure 4.5, the proposed work adds an SC 9 level MLI to the PCC grid.



(a)



(b)

Figure 4.5: Bus network with MLI based STATCOM connection (a) basic connection (b) with proposed inverter

The STATCOM will supply reactive power to increase the power factor and take load harmonics into account if the network has a nonlinear load. The park transformation modifies the synchronous reference frame of the load current, as shown in Figure 4.6, in order to provide the reference current needed by the STATCOM for processing.

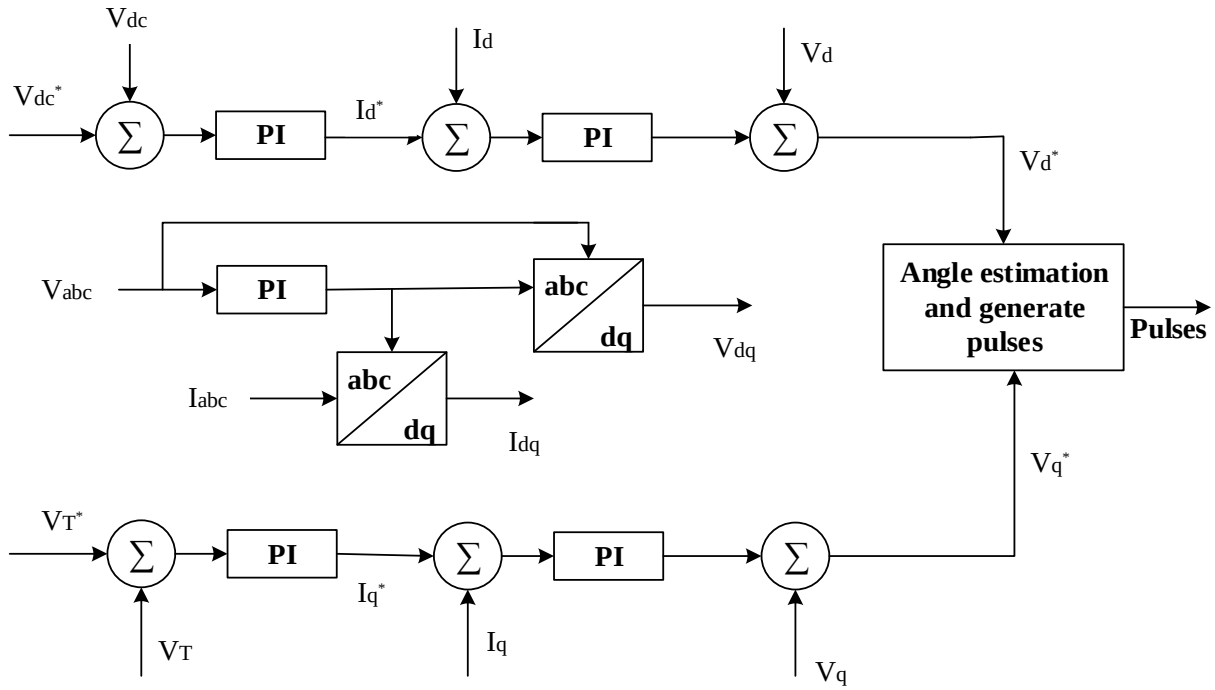


Figure 4.6: Control strategy for the proposed inverter

The PI controller is used to control the active current loss component because the voltage of the DC link capacitor needs to be maintained at its rated value in order to provide sufficient compensation. A control block for the suggested MLI is shown in Figure 4.6. The switches get the switching pulses from the controller through STATCOM, an inverter. IGBT switches with a broad frequency range were employed in this work by MLI STATCOM. MLI converters have the capacity to be switched at the fundamental frequency. Additionally, they don't require a coupling transformer for connection when the voltage isn't too high, which helps to lower overall switching losses.

The load currents of abc coordinates are converted to d-q-0 coordinates using a modified phase locked loop. These d-q-0 coordinates are oscillatory in nature because they combine an oscillatory component with an averaged component. Filters are employed to preserve averaged d-q-0 coordinate components while removing oscillatory response. These averaged components are also known as source current averaged components [105]. These reference currents regulate the unique switching capacitor based nine MLI in phases. To determine the STATCOM current, reference current values are compared to the load current. To maintain the STATCOM's currents at reference values, hysteresis current controllers are employed [106], [107].The gating signals for the IGBT switches are produced by comparing the measured (load) current with the reference source current and using the difference as the margin of error. Nine IGBT switches of the nine level switched capacitor MLI of the

STATCOM are gated in a current controller through a comparison of the reference and detected supply currents.

4.3 Results and discussion

The MATLAB/Simulink platform is utilized for implementing the suggested work. The inverter's current and voltage readings will be recorded, and several fault scenarios will be loaded. To demonstrate the effectiveness of the study effort, the performance is contrasted with more recent studies. The suggested Simulink model, which is simulated with a 50 Hz switching frequency, is shown in Figure 4.7.

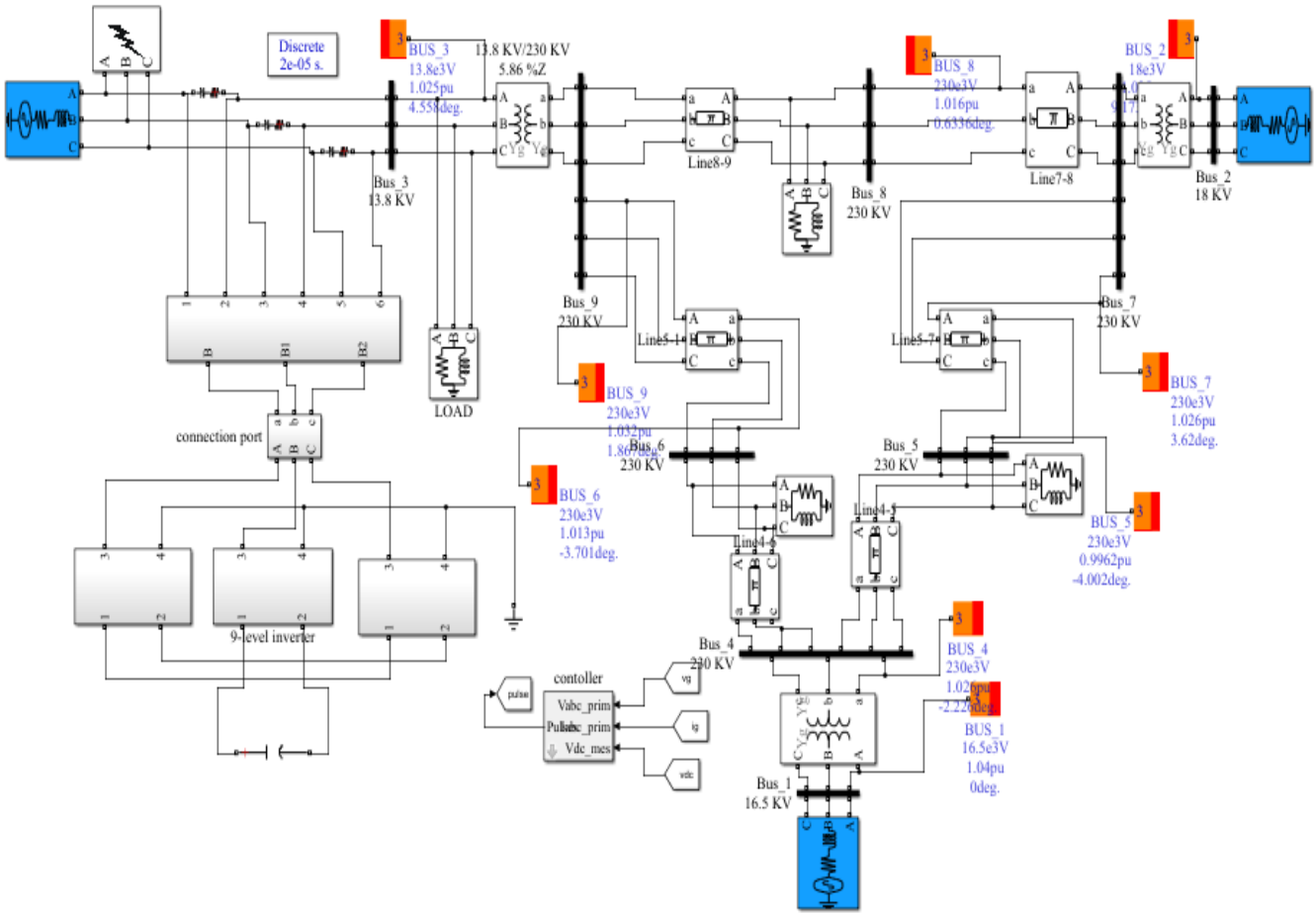
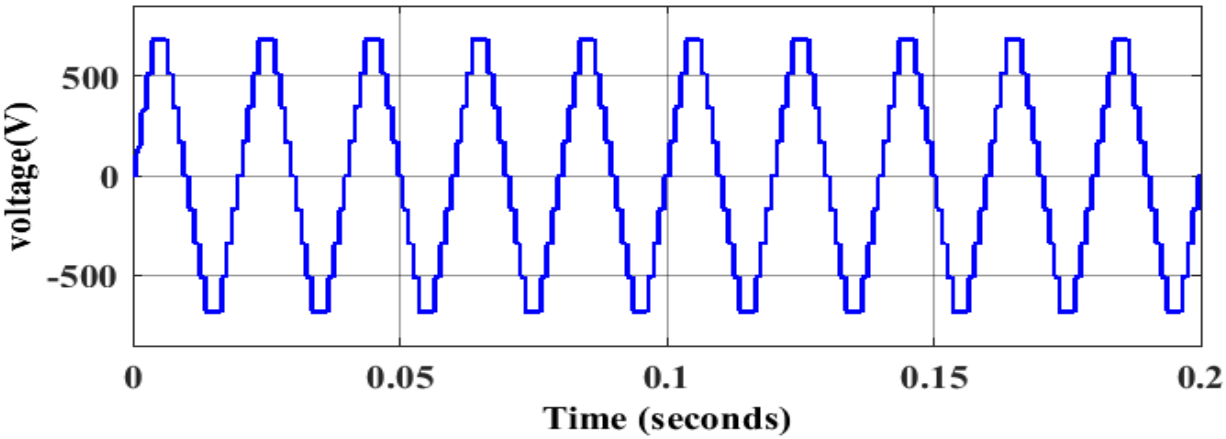


Figure 4.7: Simulink model of proposed work

The output voltage and current waveform of the suggested innovative MLI are shown in Figure 4.8.



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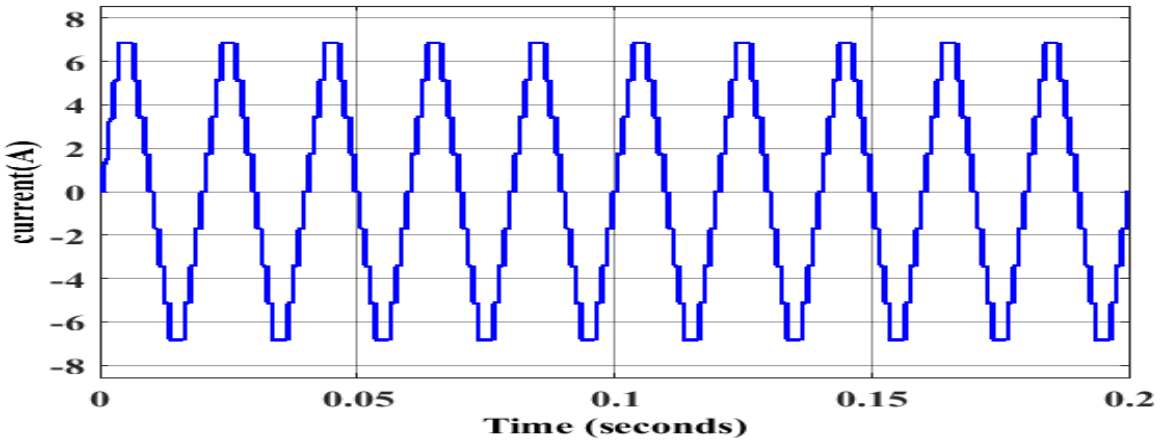
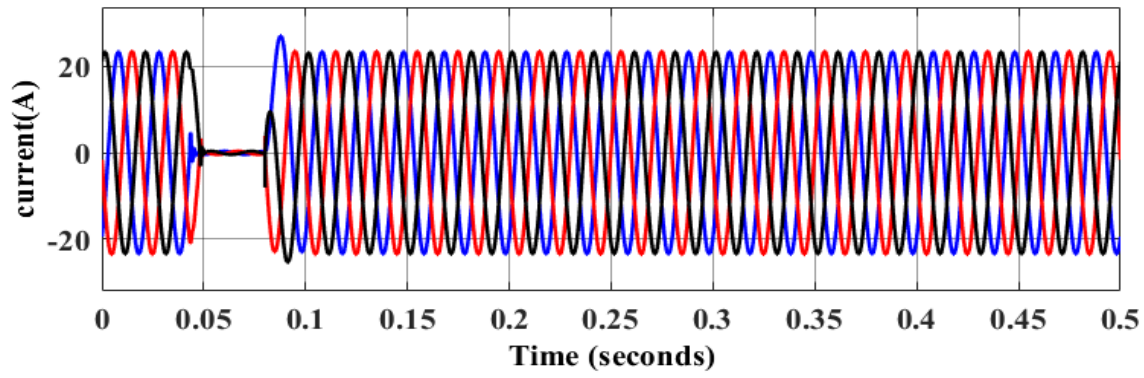


(b)

Figure 4.8: Proposed inverter output **(a)** voltage **(b)** current

This demonstrates the accuracy of the suggested nine-step result. For 0.2 seconds, the suggested inverter is simulated. With this approach, a stepped nine-level inverter image is obtained clearly. Voltage and current during swell conditions are shown in Figure 4.9.



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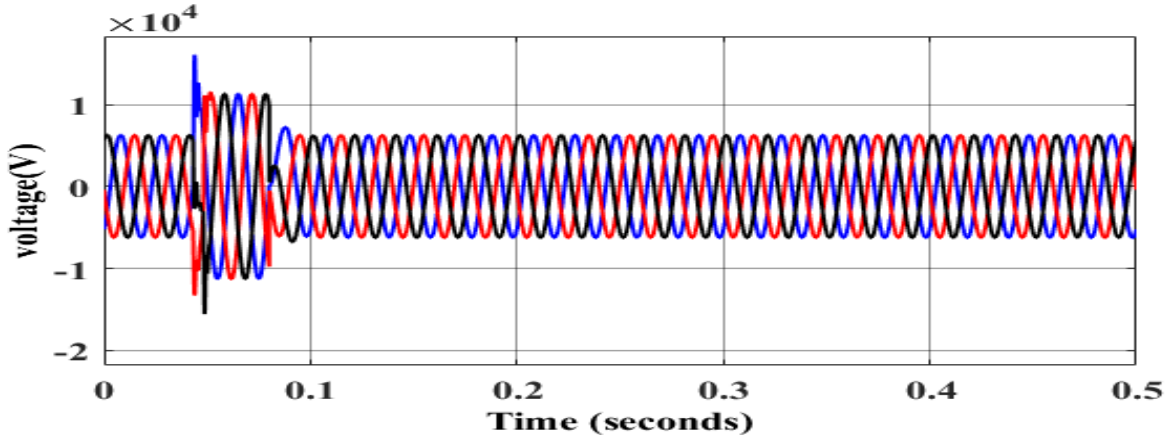
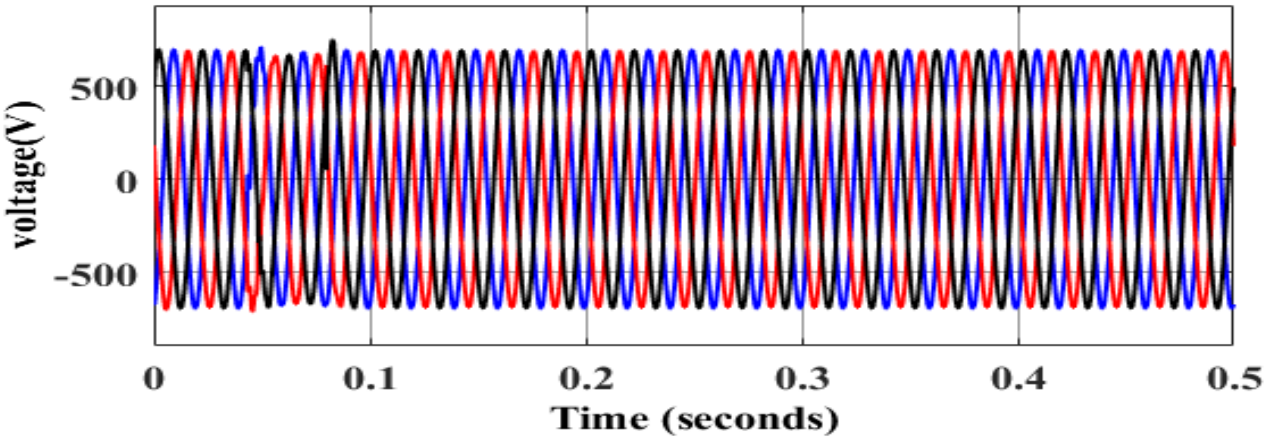


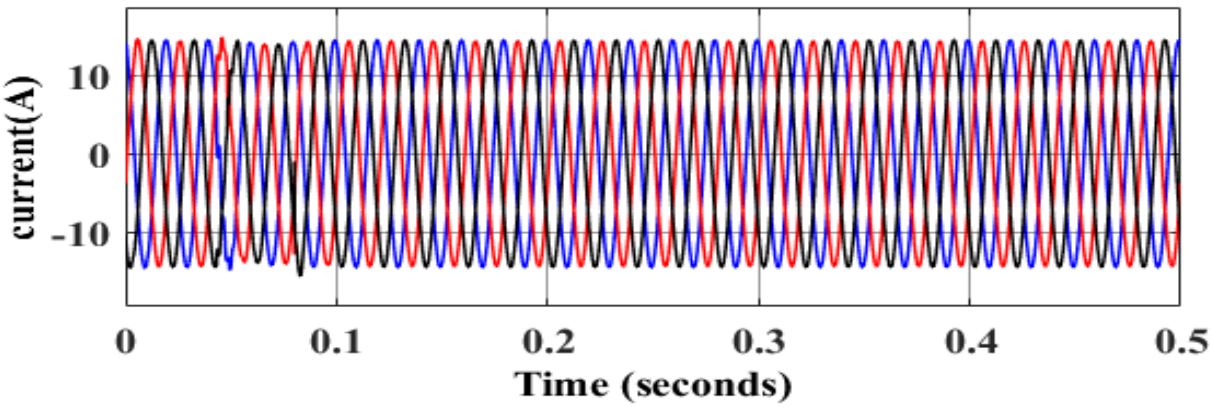
(b)

Figure 4.9: Current and voltage at swell condition

The suggested work applies a fault on the source side to demonstrate STATCOM performance, and shows the compensated result on the load side. The compensated output from the load side following the application of the fault is shown in Figure 4.10. A PI controller is used by the suggested MLI-based STACOM to efficiently correct the problem and provide the output to the load error-free.



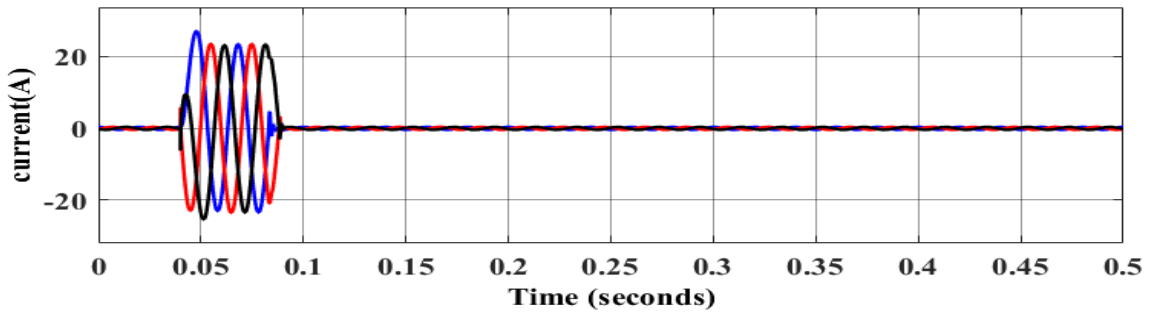
(a)



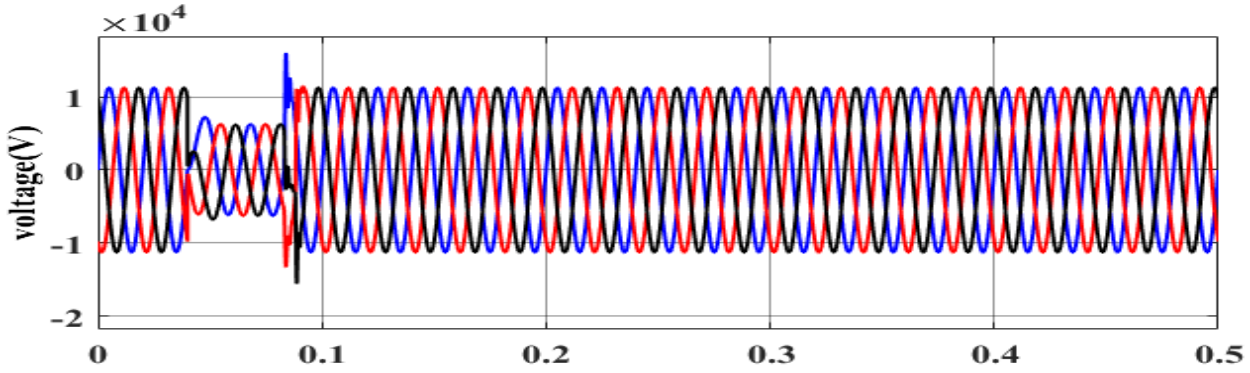
(b)

Figure 4.10: Compensate output after swell condition

The voltage and current followed the application of the sag condition are shown in Figure 4.11. In this instance, the load side obtains the STATCOM adjusted output while the source side experiences the problem. The voltage is lowered to assess the response. A network system fault causes voltage sagging, which is mimicked for 0.5 seconds. The corrected voltage and current characteristics of this situation are shown in Figure 4.12. The defect in this flawed scenario is applied between 0 and 0.1 seconds, modulating the amplitude of both waveforms. The THD achieved for the planned work is shown in Figure 4.13. With a THD of 1.04%, this approach demonstrates how the suggested strategy improves power quality.

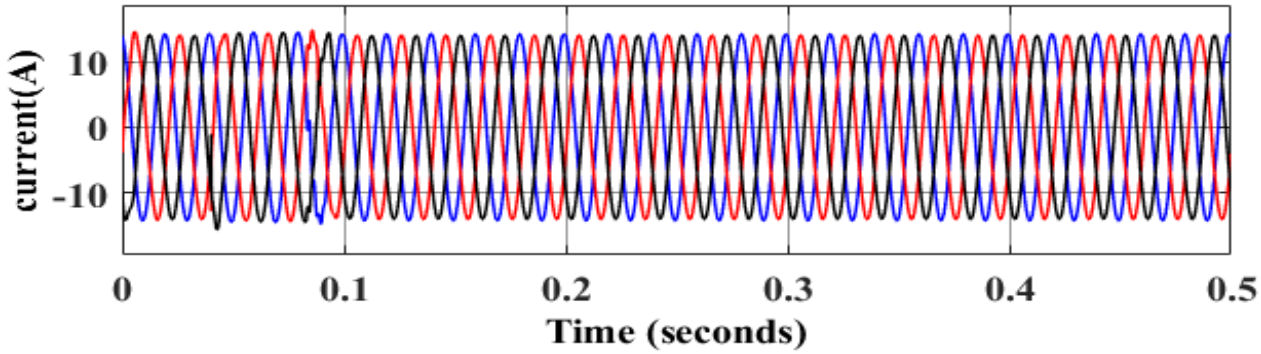


(a)

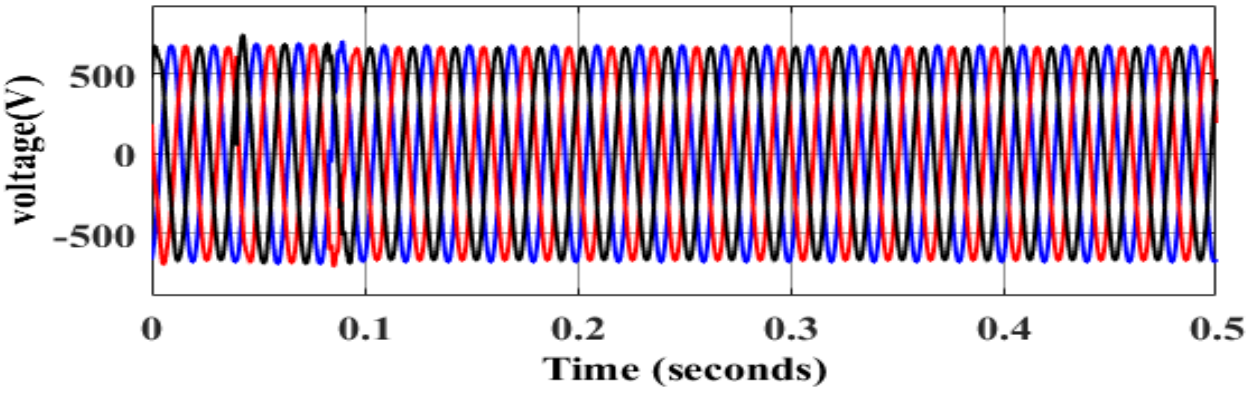


(b)

Figure 4.11: Sag applied current and voltage



(a)



(b)

Figure 4.12: Compensated current and voltage using STATCOM after a sag

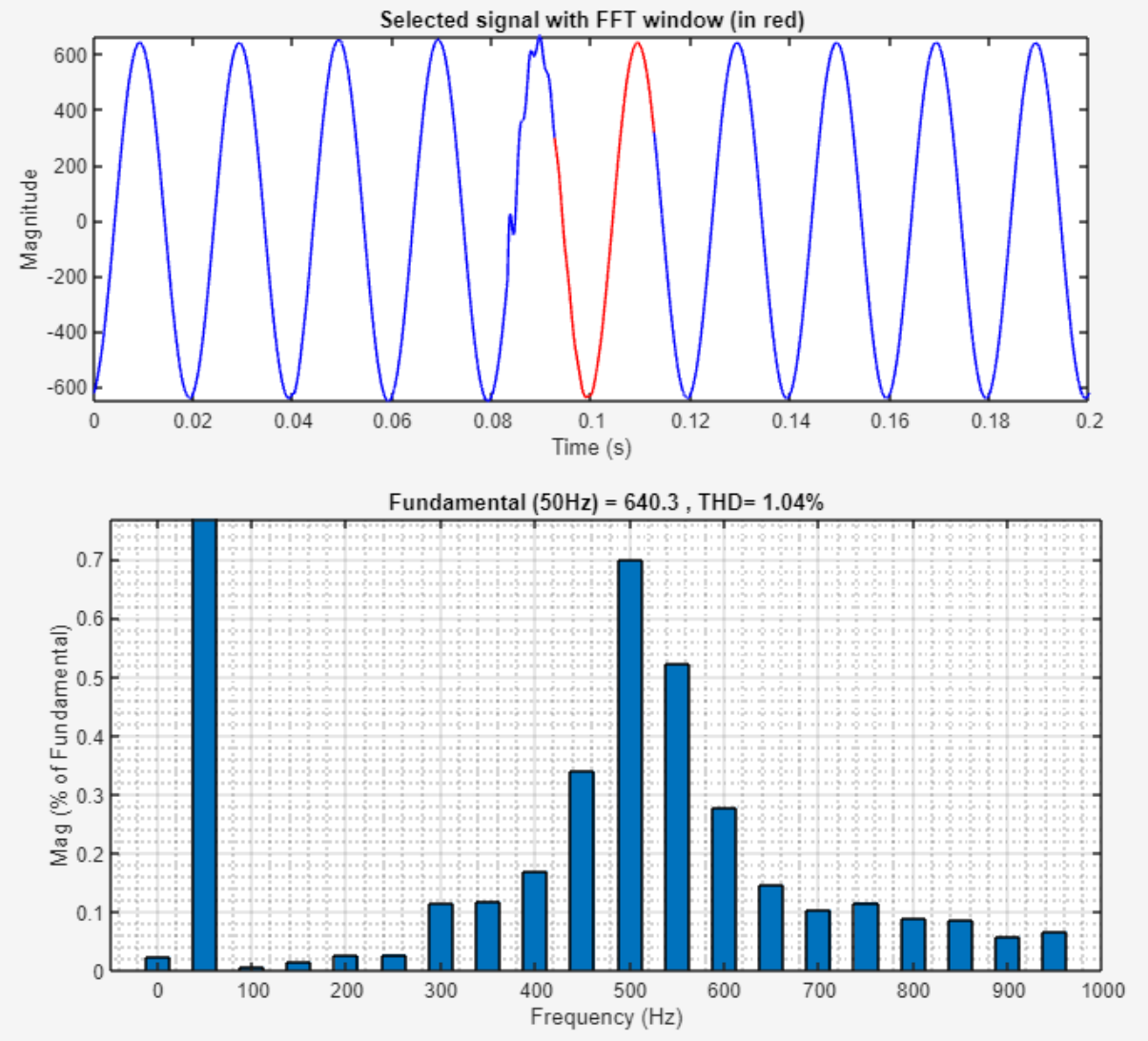


Figure 4.13: THD for proposed work

4.3.1 Comparative analysis

To demonstrate the smaller components and effectiveness of this technology, the THD and efficiency of the suggested switch inverters are contrasted with those of other current inverters. Additionally, this approach is contrasted with previous THD efforts to demonstrate the improvement in power quality through STATCOM. The comparative analysis of THD between the planned work and the existing work in [108]-[113] is tabulated in Table 4.3. The efficiency analysis comparative graph is shown in Figure 4.14.

Table 4.2: Comparative analysis of THD

Reference	Level	Switches	DC source	THD (%)

[108]	9	17	4	5.15
[109]	9	10	2	5
[110]	9	16	2	2
[111]	9	14	4	4.23
[112]	9	15	1	16.49
[113]	9	17	1	8.76
Proposed	**9**	**9**	**1**	**1.04**

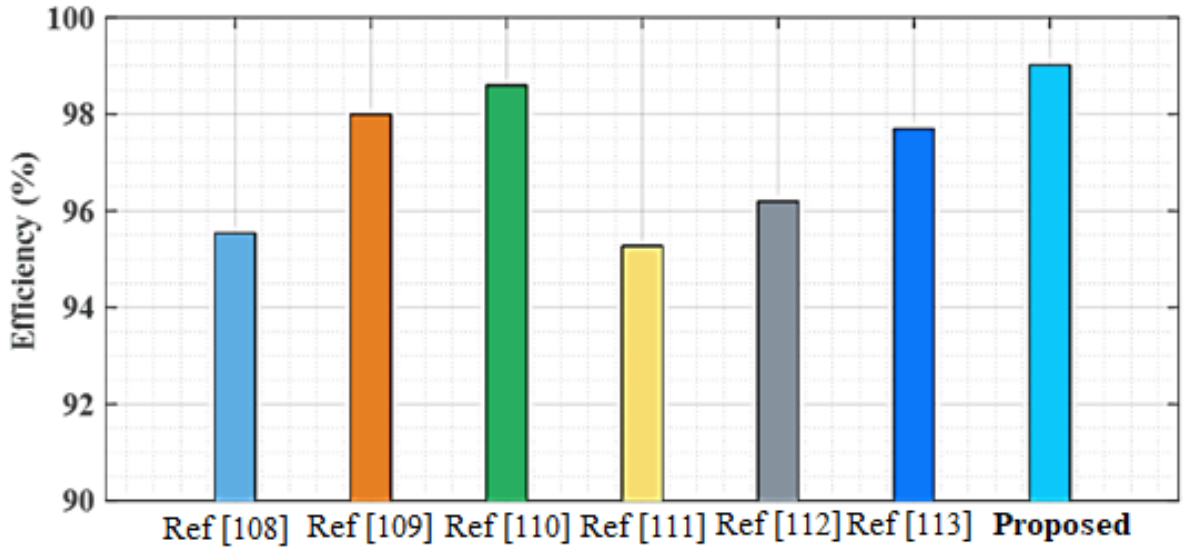


Figure 4.14: Comparative analysis of Efficiency

The following metrics are used to assess the effectiveness of the suggested innovative MLI:

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{in} + P_L} \tag{4.15}$$

where, P_L is a measure of overall loss of the MLI, which includes conduction and switching losses, and P_{out} stands for output power and P_{in} for input power.Voltage: $V = 685.2118V$, Current: $I = 6.8521A$, the output power P_{out} will be,

$$P_{out} = V \times I \tag{4.16}$$

$$P_{out} = 685.2118 \times 6.8521 \approx 4694.99W \tag{4.17}$$

Using, the equation $\eta = \frac{P_{out}}{P_{in}}$ efficiency will be,

$$\eta = \frac{P_{out}}{P_{in}} \times 100 \quad (4.18)$$

$$\eta = \frac{4694.99}{4741.47} \times 100 \approx 99.02\% \quad (4.19)$$

The nine level MLIs currently in use in [108]-[113] are taken into account for this efficiency comparison. The other approaches yielded lower efficiency than the suggested inverter, which achieved a high efficiency of 99.02%. The comparative analysis of Efficiency between the planned work and the existing work in [108]-[113] is tabulated in Table 4.4.

Table 4.4: Comparative analysis of Efficiency

Reference	**Level**	**Switches**	**DC source**	**Efficiency (%)**
[108]	9	17	4	95.54
[109]	9	10	2	98
[110]	9	16	2	98.6
[111]	9	14	4	95.27
[112]	9	15	1	96.2
[113]	9	17	1	97.7
Proposed	**9**	**9**	**1**	**99.02**

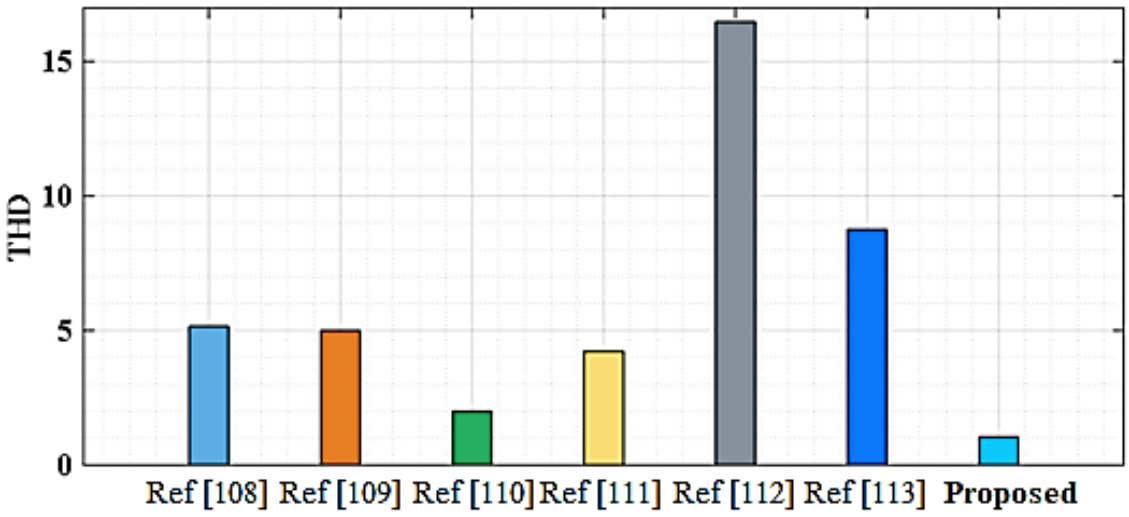


Figure 4.15: Comparative analysis of THD

The comparison study of THD with previous efforts is shown in Figure 4.15. THD in [112] is significantly higher than in any other technique. The suggested approach produced a THD reduction of 1.04%; this reduced THD range was attained by MLI functioning as STATCOM correctly. This lower amount of THD is obtained based on this optimal sinusoidal output waveform.This demonstrates the suggested method's correct operation and high level of efficiency. Furthermore, a new inverter successfully attained nine levels. A comparison between the suggested algorithm and other algorithms is shown in Figure 4.16.

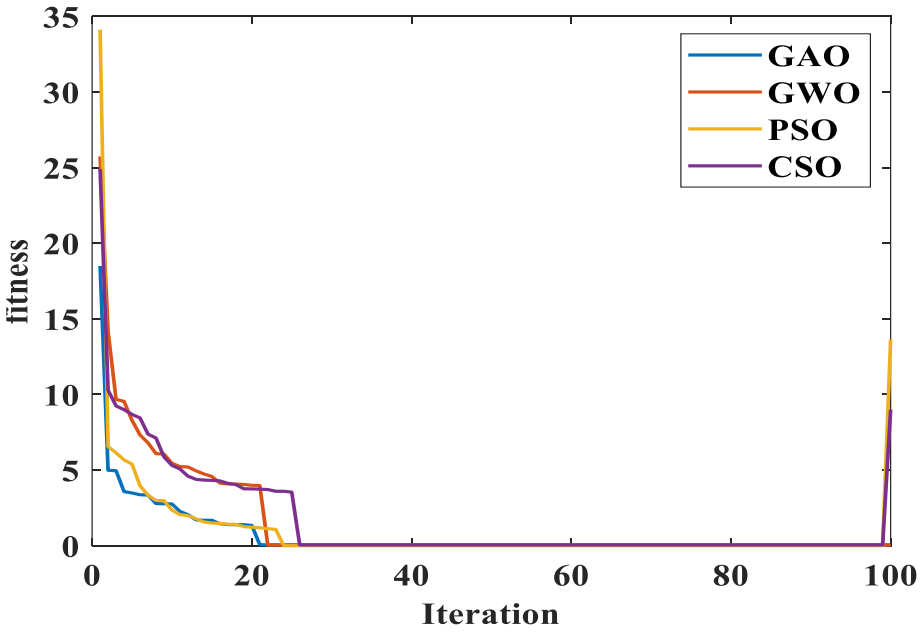


Figure 4.16: Comparative analysis of the algorithm

Figure 4.16 convergence curve clearly demonstrates the performance of the proposed GAO optimization algorithm when compared to GWO, PSO, and CSO. The proposed method, represented by the blue curve, shows the fastest and most stable convergence, achieving a very less fitness value in approximately 21 iterations. In contrast, the GWO algorithm stabilizes at a fitness value in approximately 22 iterations, while PSO of 24, and CSO of 26, more slowly than the proposed method. This indicates that the proposed algorithm not only reaches optimality more quickly but also ensures better accuracy and stability, making it the most effective among the compared methods.

With fewer iterations, the suggested method will locate the place ideally and has a high fitness range. The suggested approach is evaluated against grey wolf optimization (GWO), particle swarm optimization (PSO), and chameleon search optimization (CSO) in this comparison. When compared to alternative optimization techniques, the suggested approach produced stable results faster.

4.4 Summary

This research proposes a single DC-Link voltage of nine level MLI based STATCOM. This study offered a useful method for locating possible buses for STATCOM installation. This paper proposes a revolutionary nine-level MLI with fewer switches that is based on switched capacitors. In the IEEE 9 bus network, the MLI-based STATCOM is allocated using the GAO technique. The programming language MATLAB/Simulink is used to write the suggested approach. The optimum choice of planned parameters increases the efficiency of the suggested inverter. With little THD, the suggested new inverter generated an output voltage and current with precise 9-level steps. The suggested MLI as STATCOM effectively provided harmonics and fault compensation.The new 9 level switched capacitor based inverter achieved a THD of 1.04% with a high efficiency of 99.02%. Thus, improved power quality in the distribution network is made possible by the special nine-level switching capacitor MLI STATCOM. IEEE 9 distribution systems can greatly benefit from the increased power quality that STATCOM provides.

Chapter 5

Conclusion and Future scope

5.1 Conclusion

A unique MLI that was created by combining two SC units was presented initially in this study. Using one capacitor, one of the units increases the voltage to twice the input, and the second SC unit uses two capacitors to increase the output to four times the input. Thus, without combining several sources, a high-voltage step-up output is produced. The suggested NSC MLI is designed with a minimal number of switches. The extra complexity of voltage balancing that comes with traditional MLIs is avoided because the capacitors are naturally charged and discharged. Power losses are examined, and a thorough topological analysis is provided.The suggested MLI is more competitive than the recently created single-input MLI structures because it effectively lowers both the voltage stress and the number of components. Simulation testing under abrupt transient conditions validates the NSC MLI's operation. The real-time operation of the suggested MLI to generate a nine-level, four-times boosting voltage under various transient input/output side changes is confirmed experimentally under transient conditions.

The next research proposes a single DC-Link voltage of nine level MLI based STATCOM. This study offered a useful method for locating possible buses for the installation of STATCOM. This paper proposes a revolutionary nine-level MLI with fewer switches that is based on switched capacitors. In the IEEE 9 bus network, the MLI-based STATCOM is assigned using the GAO technique. The MATLAB/Simulink programming language is used to write the suggested approach. The optimal choice of intended parameters increases the efficiency of the suggested inverter. A precise 9-level step output voltage and current with low THD were generated by the suggested new inverter. The suggested MLI as STATCOM effectively provided harmonics and compensated for the defects.With a high efficiency of 99.02%, the innovative 9 level switching capacitor based inverter achieved a THD of 1.04%. Therefore, improved performance for improving power quality in the distribution network is offered by the special nine-level switching capacitor MLI STATCOM. An IEEE 9 distribution system's power quality could be greatly enhanced via STATCOM.

5.2 Future scope

- Investigate the benefits and challenges of integrating energy storage systems with STATCOM units to enhance stability and energy management capabilities.

- Assess the compatibility and integration of the MLI-based STATCOM with modern smart grid technologies for improved operational performance.
- Incorporate real-time monitoring and control strategies for the STATCOM system to adapt to changing network conditions quickly and efficiently.
- Investigate methods to make the proposed system more scalable and cost-effective for larger networks.
- Develop fault-tolerant methods and systems to ensure the resilience and reliability of the MLI-based STATCOM in the distribution network.
- AL drive predictive control is implemented to reduce the THD and improve the transient response.
- Machine learning techniques are developed for fault detection that can be designed to detect switch or capacitor failure in real-time applications.

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List of Publications

Research Related List of Publication

[1] H. Nanda, H. Sharma, and A. Yadav, "Design and Implementation of a High-gain Switched-capacitor Step-up Multi-level Inverter with Reduced Components Count," *Electric Power Components and Systems*, pp. 1–12, Jan. 2024, doi: https://doi.org/10.1080/15325008.2024.2304684.

Research Related List of Conferences

[1] H. Nanda and H. Sharma, "Comprehensive Review of Switched-Capacitor Boost Single-Source Nine-Level Inverters," *Lecture notes in electrical engineering*, pp. 207–220, Jan. 2024, doi: https://doi.org/10.1007/978-981-99-9439-7_15.

[2] H. Nanda and H. Sharma, "Design and Analysis of Switched Capacitor Multilevel Inverter with Higher VoltageGain" *presented at International conference of Industrial Electronics and ElectricalEngineering* on Feb. 2023 Volume-11,Issue-3.