Modeling And Performance Analysis of Multi-Gate Field-Effect Transistors

Thesis Submitted For the Award of the Degree of

DOCTOR OF PHILOSOPHY

in

Electronics and Communication Engineering

By

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2024

DECLARATION

I hereby attest that the research work presented in the thesis titled "Modeling And Performance Analysis of Multi-Gate Field-Effect Transistors", submitted in partial fulfillment of the requirements for the degree of Doctor of Philosophy (Ph.D.), is the result of my own investigation conducted under the guidance of **Dr. Yogesh Kumar Verma**, Associate Professor in the School of Electronics and Electrical Engineering at Lovely Professional University, Punjab, India. Consistent with academic standards, appropriate acknowledgments have been provided for any utilization of others' research findings. Furthermore, I confirm that this work has not been previously submitted, either in whole or in part, for any academic qualification at any other institution.

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CERTIFICATE

This serves to affirm that the research documented in the Ph.D. thesis titled 'Modeling And Performance Analysis of Multi-Gate Field-Effect Transistors,' submitted to satisfy the prerequisites for the conferral of the Doctor of Philosophy (Ph.D.) degree in Electronics and Communication Engineering, is the genuine product of the research efforts of Nagalakshmi Yarlagadda, student ID 42000326. This thesis represents an authentic account of original work conducted under my supervision, and no portion of it has been presented for the fulfillment of any other academic qualification, diploma, or equivalent course.

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ABSTRACT

The advancement of CMOS scaling encompasses two primary aspects: the refinement of device electrostatics and the improvement of transport properties. The progression of the semiconductor industry predominantly hinges on this scaling of devices. The adoption of a multi-gate structure serves to augment device electrostatics, particularly crucial as planar bulk CMOS technology faces susceptibility to short channel effects (SCEs) as dimensions shrink to the nanometer scale, leading to notable deterioration in the device's electrical characteristics. Consequently, our investigation in this study delves into the efficacy of the 'multi-gate' configuration of ‘Gate all-Around Junctionless Field Effect Transistor (GAA-JLFET)’ in addressing the imperative need for mitigating SCEs by offering enhanced gate control.

On the other hand, the improvement of transport properties is possible by utilizing wide band gap material, e.g., SiC. Thus, the amalgamation of superior electrostatic control of GAA-JLFET and distinguished transport properties of SiC material is a promising option for future advanced electronics.

In this study, a comprehensive examination of the multi-gate field-effect transistor, specifically the GAA-JLFET, has been conducted, encompassing the analysis of its electrical characteristics and parameters. The integration of a P+ pocket within both the source and drain regions serves to optimize volume depletion within the GAA-JLFET. Consequently, this expansion of the tunneling region at the channel-drain junction effectively mitigates the off-state current attributed to band-to-band tunneling (L-BTBT). Observations reveal that the incorporation of wide bandgap materials, such as SiC, in the construction of nanowires renders the device less susceptible to temperature fluctuations, particularly under elevated drain voltages.

In light of these findings, a compact model has been developed, which incorporates Poisson's equation for nanowires, facilitating the calculation of surface potential. The performance of this proposed compact model has been rigorously assessed through validation against simulation results obtained from SILVACO TCAD, demonstrating strong agreement between the model predictions and simulation outcomes.

Considering the above points, the work done in this thesis comprises of:

- A physics-based compact model has been developed for potential and electric field with consideration of P+ pocket in the SiC GAA-JLFET.
- Suppressing Short Channel Effects (SCEs) in Multi-Gate Field Effect Transistors for below 25 nm technology.
- Model and analyze Electrical characteristics of SiC GAA-JLFET
- A surface potential-based analytical model of “double-gate MOSFET” is developed for “short channel effects” and “drain current”

PREFACE / ACKNOWLEDGEMENT

This thesis would not have been possible without the support of glorious people who motivated me during my doctoral study. First and foremost, I am thankful to almighty for making things possible at the right time. I owe my success to my supervisor Dr. Yogesh Kumar Verma. I greatly appreciate his support, positive attitude. His guidance has been invaluable, offering ideas, resolving research challenges, and granting me the freedom to conduct research in my own unique manner, which has proven to be highly beneficial. I am deeply influenced by my supervisor's way of guidance and sincerely thankful for standing by my side in tough times. He always shed light whenever I was feeling stuck in my path of research ambitions. I consider myself fortunate to have been associated with an individual like him.

I would like to express my sincere gratitude to my husband N. Ravi, and my only son N.V Kushal Sai for their unconditional love, support, and encouragement. Their endless love, encouragement, and support provided to me, has been a constant source of inspiration. I dedicate this thesis to my husband and my son. I am grateful to my family and my spouse's family for their assistance. A special thanks to my brother Dr. Y. Srinivas Rao who was my strength to stand the monotony of a researcher's life.

I am grateful to my colleague Mr. Jugal Kishore Bhandari who constantly motivated and encouraged me during the course of my study. He has consistently provided assistance whenever I encountered difficulties or had questions related to my work.

I would also like to thank my professors at GCET for guiding me during my initial phase of work and providing technical inputs to proceed with my research work.

I would like express my sincere thanks to my Ph.D. colleagues for constant support.

I extend my heartfelt gratitude to my educators, whose guidance at various educational milestones has paved the way for me to reach this point. Their benevolence has played a pivotal role in enabling me to reach a stage where I am able to compose this thesis.

I would like to extend my gratitude toward the entire Lovely Professional University for providing suitable infrastructure and environment for completing my research work in a time-bound manner. Also, I would like to thank the division of research & development and School of Electronics and Electrical Engineering for their encouragement.

Finally, I like to thank almighty God who helped me to achieve my goal. His grace has been a constant source of blessing, guiding me forward at every step & special thanks to all the people who helped me to accomplish this work.

Date: Naga Lakshmi Yarlagadda

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LIST OF SYMBOLS

I_{ON}	On current
I_{OFF}	Off current
V_{Th}	Threshold Voltage
V_{GS}	Gate to source voltage
V_{DS}	Drain to source voltage
L_g	Gate length
C_{ox}	Oxide capacitance
P_S	Static power dissipation
P_D	Dynamic power dissipation
V_{DD}	Supply voltage
C_L	Load capacitance
α	Switching probability
f	Device operational frequency
E	Electronic charge
H	Planck's constant
t_{ox}	Oxide thickness
t_{Si}	Silicon body thickness
I_D	Drain current
T	Temperature
k	Boltzmann constant
SS	Subthreshold swing
μ	Mobility
N_S	Doping at the source region

N_D	Doping at the drain region
N_{ch}	Doping at the channel region
C_D	Depletion capacitance
$V_{D_{SAT}}$	Supply voltage during saturation mode
$V_{D_{LIN}}$	Supply voltage during linear mode
$V_{T_{LIN}}$	Threshold voltage during linear mode
$V_{T_{SAT}}$	Threshold voltage during saturation mode
ϕ	Gate work function
C_{GS}	Gate-source capacitance
C_{GD}	Gate-drain capacitance
C_{GG}	Total gate capacitance
f_T	Cut-off frequency
g_m	Transconductance
g_m/I_{DS}	Device efficiency
V_T	Thermal voltage

LIST OF ABBRIVATIONS

MOSFET	Metal oxide field effective transistor
SG	Single gate
DG	Double gate
SCE	Short channel effect
SRAM	Static random access memory
2-D	2-dimensional
3-D	3-dimensional
SOI	Silicon on inductor
CMOS	Complementary metal-oxide semiconductor
GAA	Gate all around
RF	Radio Frequency
TM	Triple material
DM	Dual material
JL	Junction less
SS	Subthreshold slope
DIBL	Drain induced barrier lowering
FET	Field effective transistor
AJ	Asymmetrical junction less
DSBO	Double step buried oxide
BP	Black phosphorus
RC	Recessed channel
GC	Graded channel
GBP	Gain-bandwidth product
SOI	Silicon-on-Insulator
PD/FD	Partially depleted/Fully depleted
VLSI	Very Large Scale Integrated Circuit
TCAD	Technology computer-aided design

CHAPTER 1

Introduction

The remarkable growth of the nanoelectronics era in the twentieth century has been characterized by the evolution of advanced electronic gadgets and devices. The semiconductor industry progress has played a significant role in driving a large portion of the productivity gains witnessed in the global economy since the 1990s. This progress can be attributed to the invention of various types of transistors and the discovery of new materials. The concept of the field-effect transistor (FET) was initially put forth in the early 1930s by Lilienfeld [Lilienfeld (1930)] and Heil [Heil (1935)] as a potential replacement for vacuum tube-based triodes [Riordan et al. (1997)]. The operational concept of the metal oxide semiconductor field-effect transistor (MOSFET) was initially proven successful in 1960 by D. Kahng. [D. Kahng (1960)], marked the initiation of a revolution within the semiconductor-based electronics industry at large, particularly impacting integrated circuit (IC) technology. MOSFETs have served as the fundamental active components for ICs over the preceding decades.

1.1 About Conventional MOSFETs

A MOSFET comprises a base material, typically silicon, referred to as the body or substrate, serving as the fundamental building block for the entire device. A layer of silicon dioxide is deposited on the substrate's surface. Both the drain and source regions are doped with the same type of material and they are connected through metallic contacts. The gate terminal is composed of polysilicon and remains electrically insulated from the channel by the SiO2 layer. [1]

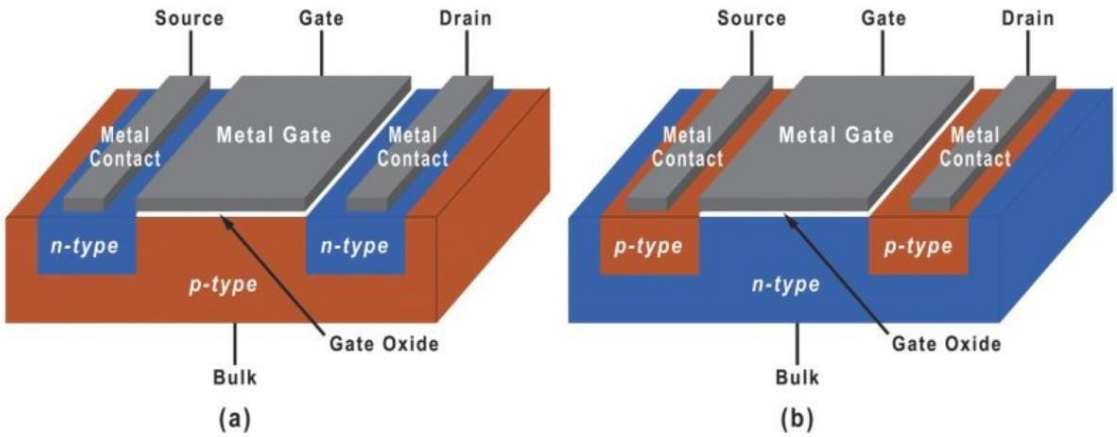


Fig. 1.1 MOSFET (a) n. channel (b) p. channel

The unending pursuit of developing energy-efficient computing systems has fueled the exponential advancement of MOSFET-based IC technology. The formation of the CMOS structure, achieved with integrating a p type channel and an n type channel MOSFET into a single unit, has become the foundational building block in the design of contemporary ICs for various applications in computing and communication. This is mainly because of its low static power dissipation characteristics.

MOSFETs can be divided into two main categories: n-channel and p-channel types. In an n-channel MOSFET, the drain and source regions are heavily doped with n+ type dopants, facilitating electron conduction as the primary charge carriers. Conversely, in a p-channel MOSFET, both drain and source regions are extensively doped with p+ style dopants, leading to hole conduction as the primary charge carriers. Figure 1.1 illustrates a cross-sectional diagram representing both N-channel and P-channel MOSFETs.

The gate-source voltage governs the current flow from the source

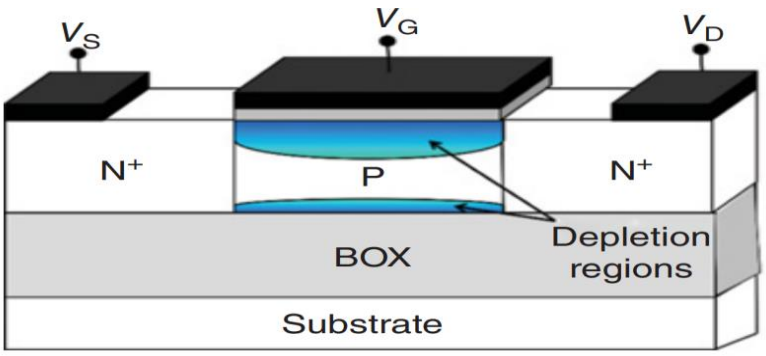
terminal to the drain. In NMOS transistors, a p-type substrate is typically connected to the ground, and the drain voltage is higher than that at the source. When there is no gate-source voltage applied, no current flows from the source to the drain because a conductive channel is absent, and the transistors are considered to be in the off state. As the gate-source voltage gradually increases, an electric field forms across the channel, attracting free electrons at the Si-SiO2 interface. When the gate voltage reaches a certain level, an inversion occurs. During this inversion, the number of free electrons in the channel surpasses the number of holes in the p-substrate, transforming the channel into an N-type region. This allows electrons to move from the source side to the drain, resulting in an increase in drain current.

In a similar manner, the n-type substrate of a PMOS transistor is usually connected to drain voltage, with the drain voltage being lower than that at the source. When either zero or gate-source voltage is positive, the absence of channel results in the non-existence of path for the current to flow from source to drain, and the transistor is in the off state. However, when a negative gate-source voltage is applied, an electric field develops across the channel, attracting free holes at the Si-SiO2 interface. As the gate voltage becomes sufficiently negative, the channel undergoes inversion, transitioning to a p-type region, enabling the movement of holes from the source to drain. This leads to an increase in current at drain. Consequently, when the gate voltage surpasses the MOSFET's threshold voltage, a substantial channel inversion occurs beneath the gate, and the material used to construct the MOS structure determines this threshold voltage. This inversion leads to the accumulation of holes in PMOS and electrons in NMOS beneath the gate, and the drain voltage sweeps these charge carriers, causing current to flow in the MOSFET.

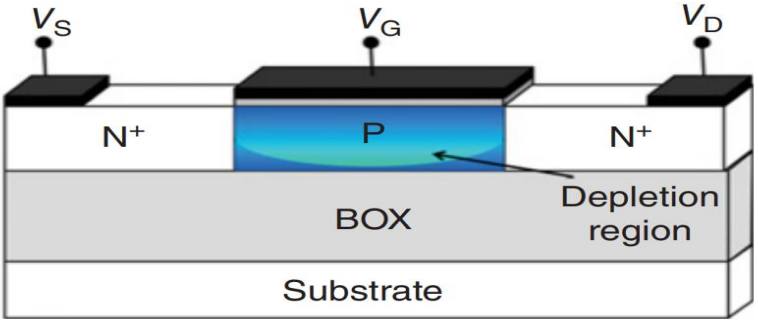
1.1.1 Silicon -on-Insulator

Figure 1.2 illustrates SOI-MOSFETs, where, the absence of a contact

electrode to the channel causes the channel region to float, leading to floating body effects. SOI-MOSFETs are categorized based on the depletion extent of the channel region: (a) partially depleted 'SOI-MOSFETs' ('PDSOI-MOSFETs'), as depicted in Figure 1.2(a), where the SOI channel thickness allows some channel region to remain un-depleted and neutral, and (b) fully depleted 'SOI-MOSFETs' ('FDSOI-MOSFETs'), shown in Figure 1.2(b), wherein the SOI film thickness is adjusted to deplete the entire silicon body, leaving no neutral region. In FDSOI MOSFETs, the floating body effects arising from impact ionization are relatively suppressed due to full channel depletion, hindering hole accumulation. Conversely, PDSOI MOSFETs are dominated by parasitic bipolar effects, leading to breakdown voltage degradation.



a) 'PDSOI MOSFET'



b) 'FDSOI MOSFET'

Fig. 1.2 Three- dimensional view of 'SOI-MOSFETs' a) 'PDSOI MOSFET'

and b) ‘FDSOI MOSFET’

The key applications of MOSFETs is their ability to function as switches when operated in the cutoff and saturation regions. Ideally, when a transistor is turned off, it should consume no power, and when turned on, it should efficiently deliver a substantial current. However, MOSFETs employed in real-world applications often exhibit a minor leakage current. Consequently, even when they are in the off state, a small amount of power is still consumed.

Integrated Circuits (ICs) fabrication, in particular, has ushered in a new era of nanoelectronics revolution. One of the key advancements in nanoelectronics has been device scaling or miniaturization, which has increased the speed and component density of nanodevices. This exponential increase in performance was accurately predicted by Gordon Earle Moore in 1965[1]. However, as devices continue to shrink in size, conventional transistors face challenges due to adverse effects. Short Channel Effects (SCEs), quantum tunneling effects, and subthreshold leakage issues become more prominent as the channel length reduces[2]. Although certain techniques have been developed to mitigate these adverse effects, fully nullifying them remains extremely difficult. As a result, researchers have been exploring novel techniques for making electronic devices and alternative materials for use in applications.

1.2 CMOS

Currently, CMOS technology play a pivotal role in worldwide semiconductor industry. It fuels a diverse range of electronic applications that consistently redefine our daily lives. The remarkable advancements in CMOS technology observed in the last four decades highlight its success and are at the core of the impressive scalability of the MOSFET. This growth momentum is pivotal to the enduring success of CMOS technology. The primary obstacle encountered during CMOS scaling arises from the excessive occurrence of the emergence of

short-channel effects as the device's channel length descends into the sub-100nm range. Strategies employed to facilitate CMOS technology advancement in the sub-100nm range encompass approaches like strained channels, High-k dielectrics, multiple gate configurations, back-gate use, and non-traditional MOS architectures comprise hybrid orientation technology (HOT). These measures contribute to the ongoing progress of CMOS scaling below the 100nm threshold.

Furthermore, CMOS scaling brings about certain benefits, such as a reduction in the input capacitance of MOSFETs and enhancement in their current driving capacity. Nonetheless, a constraint persists despite the increased current-carrying capability of MOSFETs. This constraint arises due to short channel effects induced by the reduced gate length, leading to an elevation in IOFF [9]. Due to the rise in IOFF, there is a statistically significant increase in power dissipation. Given the rapid pace at which CMOS scaling is advancing, researchers predict that the static power dissipation range in conventional MOSFETs will soon surpass the range of dynamic power dissipation. Another significant drawback of static power dissipation is its propensity to draw substantial power from the battery even when the device is switched off.

1.3 Moore's Law

CMOS scaling principle, established by Gordon Moore, would also be integrated at this point. According to ‘Moore's Law’, the number of transistors on a chip will roughly double every two years, a concept commonly referred to as Moore's Law [1]. Over the past four decades, the CMOS industry diligently followed Moore's Law, effectively advancing through CMOS scaling. As MOSFETs were scaled down, their dimensions started to approach the widths of depletion regions at the junctions between the source and channel, as well as the channel and drain. Short-channel MOSFETs have narrower channels than those with wider regions at junctions between source-channel or between

channel-drain.

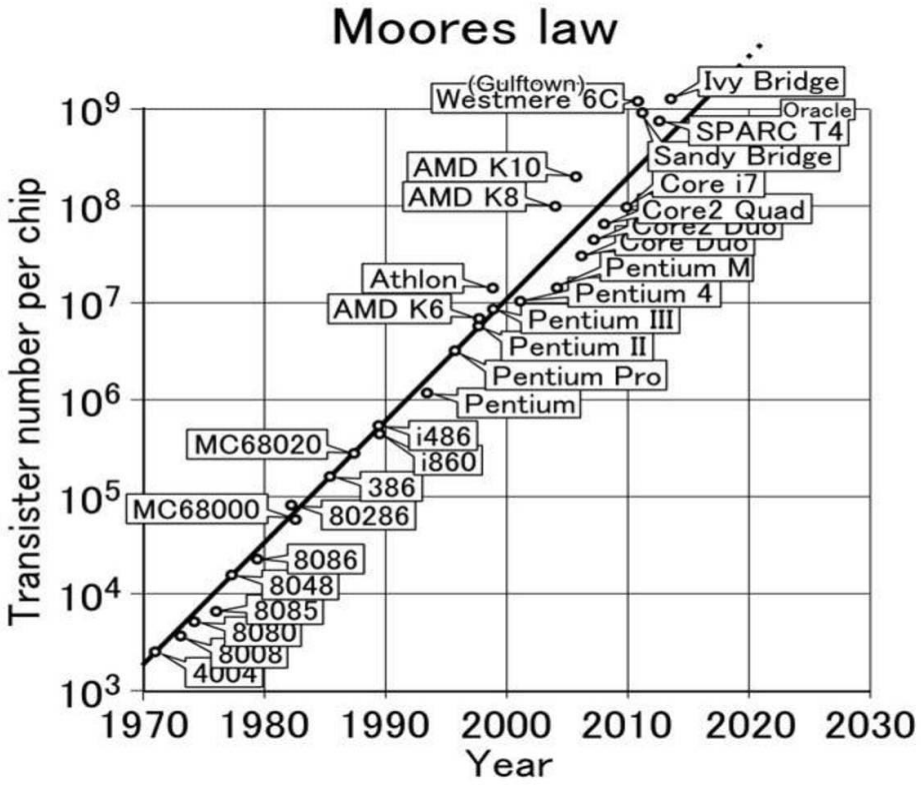


Fig.1.3 Moores Law [1]

1.4 Criteria for future technology nodes

In the field of logic technologies, it's conventional to categorize technology options into several groups, including:

• High-performance

• Low power consumption during active operation

• Minimal power consumption in standby mode

1.5 Device Scaling

Since Moore's law was introduced, the process of device scaling has endured for several decades. The aggressive scaling of MOSFETs has been instrumental in the significant expansion of the IC industry, resulting in channel lengths

shrinking to mere tens of nanometers.[3] This continual reduction became feasible following Robert Dennard's contributions to scaling theory.

Notably, Intel initiated production using a 32 nm feature size in late 2009, and Samsung disclosed their plans for a 5 nm process to potential customers in April 2019. The diminishing size of transistors, however, gives rise to the quantum tunneling effect through the gate dielectric layer when they become smaller than 7 nm. Researchers at Berkeley National Laboratory have successfully developed a functional transistor with a gate length of only 1 nm. This achievement has bolstered the belief that substantial opportunities exist for further miniaturization of electronic components through suitable material selection. The pivotal factor that has shifted the perspectives of many scientists, is the adoption of alternative materials to silicon. An alternative approach to address the challenges presented by scaling includes adopting multi-gate architectures like Double Gate (DG), Triple Gate (TG), and Gate All Around (GAA) or Surrounding Gate (SG). The GAA FET, in particular, is poised for use in the 3 nm technology node by 2020, offering a 40% performance enhancement with the same power consumption. Additionally, the emergence of monolithic 3D transistors looms on the horizon, poised to revolutionize the semiconductor industry by reducing area requirements by 50%. This innovation entails the sequential integration of transistor layers above the substrate in a three-dimensional arrangement.

1.6 Scaling Objective:

The primary aims of employing various scaling rules at each transition to a new technology node are as follows:

- Decreasing gate delay by 30%, achieved by a corresponding 30% reduction in parasitic capacitance, which results in an approximately 43% increase in operational frequency (as noted by Borkar in 1999).
- Achieving a transistor density per unit area that is nearly twice that of the

preceding technology node, following the insights offered by Davari and colleagues in 1995.

- Borkar's findings from 1999, Moore's Law reduces energy consumption and active power per transition by 65% and 50%, respectively.

The importance of metal–oxide–semiconductors (MOS) devices is improved extensively. Therefore, number of researchers are working on MOS devices from past few decades [1]. The complexity in fabrication of these devices is reduced with small modifications in electrical parameters and its scaling techniques increase the performance of the device [2]. Substantial challenges have been recognized in the scaling of MOS (Metal-Oxide-Semiconductor) devices, encompassing issues such as high off-state current, Drain Induced Barrier Lowering (DIBL) [3], low on-current, sub-threshold slope, heightened power consumption, high GIDL, and increased power dissipation, all of which negatively impact the electrical efficiency of these devices. Addressing these challenges necessitates a series of enhancements to MOS devices.

Control over gate current is achieved by the implementation of advanced technologies, such as Multi gate Field Effect Transistors, Gate All Around Field Effect Transistors (GAAFET), and MOSFETs with double gates [4]. These innovations are pivotal in mitigating the issues mentioned and improving the performance of MOS devices.

The reason for selecting Multi-gate devices is to improve the device electrostatics control, enhances gate control over channel, reduced leakage currents which contribute to low power consumption and improve transport parameters[1].

Efforts to minimize power dissipation are vital in the context of technology scaling, as this directly contributes to the enhancement of battery life in portable devices. On SOI (Silicon-On-Insulator) wafers, the development

of Multi gate MOSFET structures, which includes gate-all-around (GAA) MOSFETs, triple-gate, and double-gate configurations, is being actively pursued. These innovations aim to tackle the mentioned issues and push th3.e limits of device performance.

These structures are having control on subthreshold region gates and the process of less leakage with low power consumption in comparison to conventional MOSFETs [5].

1.7 Short-channel effects

The origins of short-channel effects can be traced in to two distinct physical phenomena:

- Limitations on the channel characteristics that affect electron drift.
- Alterations to the threshold voltage brought about by the reduction in channel length.

These effects appear as five distinct phenomena, which consist of:

• DIBL and Punch-through

• Surface scattering

• Velocity saturation

• Impact ionization

• Hot electrons

• Sub-threshold leakage current

1.7.1 ‘Drain-induced barrier lowering (DIBL)’: A reduction in channel length, coupled with pinchoff, exacerbates the reliability issues linked to Short Channel Effects (SCE). This escalation becomes more apparent as the drain voltage increases due to the hot-carrier effect [7]. Furthermore raising the gate voltage to control the drain-current can result in an increase in drain off-current and a

degradation in sub-threshold slope. If channel length is too short then, gate and drain terminals are very close to each other and bottleneck opens at high drain voltage which turns on the transistor in advance. Ideal output characteristics for MOS transistors are achieved when a low 'DIBL' is present. This is because the channel potential's susceptibility to the drain field effect is reduced, which, in turn, minimizes threshold voltage variations [8].

$$DIBL = \frac{V_{th}^{dd} - V_{th}^{low}}{V_{dd} - V_{th}^{low}} \dots\dots (1)$$

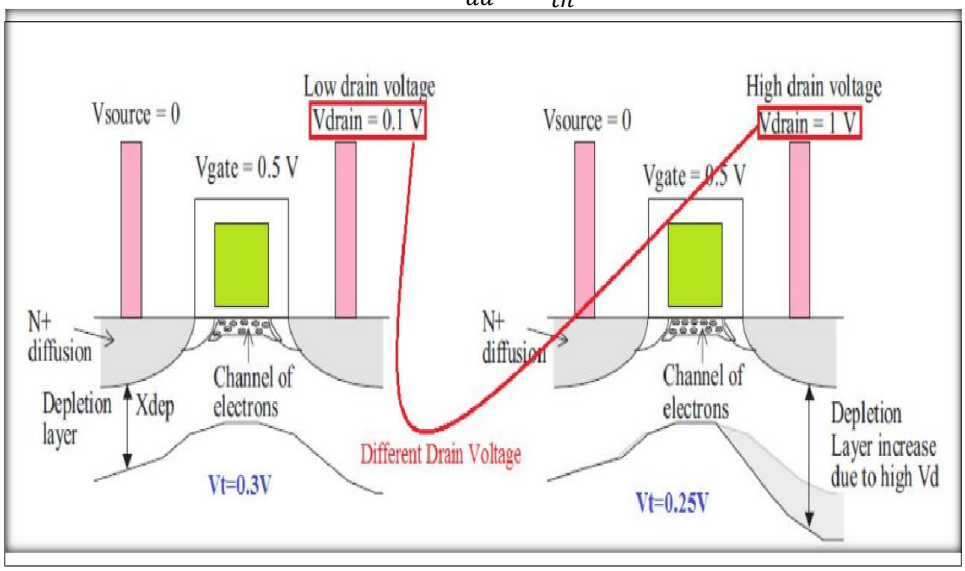


Fig. 1.4 DIBL effect in MOSFET [24]

1.7.2 Surface scattering**:** As the channel length decreases, the surface mobility undergoes a transition from being unaffected by the electric field for displaying an enhanced dependence on the longitudinal direction. In the restricted inversion layer of a MOSFET, carrier transport becomes constrained.

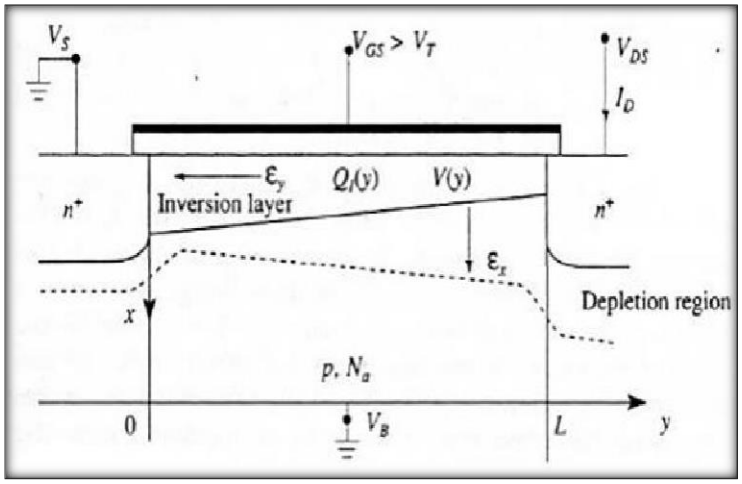


Fig. 1.5 Surface Scattering [24]

Decreased mobility arises due to surface scattering, making it difficult for electrons to move parallel to the contact. This is a crucial factor in maintaining the mean surface mobility at a level close to the average bulk mobility. Electrons directed towards the interface experience collisions with obstacles, leading to surface scattering. [28]

1.7.3 Velocity saturation:

Velocity saturation is primarily caused by scattering events and the interaction of charge carriers and lattice vibrations within the semiconductor material. As the electric field across the semiconductor increases, carriers gain kinetic energy and accelerate. However, at a certain point, they experience more frequent collisions with phonons, which limit their acceleration and prevent further increases in velocity. Velocity saturation has significant implications for the operation of semiconductor devices, especially MOSFETs. In these devices, carriers need to travel at high speeds to ensure fast switching and high performance. When velocity saturation occurs, carriers don't accelerate as

expected under high electric fields, which can limit the device's ability to carry current effectively. Velocity saturation becomes particularly important in nanoscale MOSFETs with short channel lengths. In these tiny transistors, the electric field can become very high, leading to early onset of velocity saturation velocity saturation is a limitation that arises in semiconductor devices when charge carriers can no longer increase their speed in response to higher electric fields. Understanding and managing this phenomenon is crucial for designing and optimizing modern electronic devices, particularly those with nanoscale dimensions.

1.7.4 Impact Ionization:

Beyond 100nm, conventional MOSFET performance remained consistent with scaling trends, but channel length decrease had different negative impacts. To address this issue, Multi-Gate MOSFET, tri-Gate MOSFET, and double-gate MOSFET structures have been designed to mitigate short channel effects. The DG-MOSFET, in particular, has proven effective in resolving numerous challenges. It reduces junction capacitance, mitigates short channel effects, and offers the advantage of dielectric isolation, such as SOI (silicon on insulator), which is conducive to low power consumption in MOS technology. and high-speed performance. Junction-less transistor is widely used device for increasing packaging density [9]. For reverse-biased junction, conventional MOSFET is turned off, but channel region full depletion turns off the Junction-Less-Double-Gate device [10].

According to the ON and OFF-state performance, several advance MOSFET structures are compared. MOSFET Channel inversion operation before region is called as subthreshold region. Reliable and required MOSFET performances are obtained by the deciding factor as sub threshold parameters [11].

1.7.5 Hot-Electron Effect:

In FETs the hot electron effect is a critical phenomenon that affects the device's operation and reliability. The regulation of current flow between the source and drain terminals through the semiconductor channel is governed by an electric field generated upon applying a voltage to the gate terminal of a MOSFET. The most critical aspect of the hot-electron effect is the hot carrier injection. High-energy electrons can attain adequate energy to surpass the energy barrier at the gate oxide-semiconductor interface. This can lead to the hot electrons into the gate oxide, causing damage over time. This phenomenon is commonly referred as hot carrier degradation (HCD) and reduce the lifespan and reliability of the MOSFET Shrinking the size of transistors can reduce the impact of the hot electron effect, as shorter channel lengths result in less energy being imparted to electrons. The hot electron effect in MOSFETs involves the high-energy electrons within the device that can negatively impact performance and reliability. Understanding and mitigating this effect is essential for designing and manufacturing advanced semiconductor devices.

1.7.6 Sub-threshold leakage current**:** Sub-threshold leakage current in MOSFETs states to the small, unintended electric-current which flows between source and drain terminals of the transistors and it operates in subthreshold region. In this region, Vgs is below the Vth which is required to turn the transistor fully on, resulting in partial conduction. subthreshold leakage current in MOSFETs is a noteworthy phenomenon that occurs when the transistor operates under its threshold voltage. It is crucial to address this issue in semiconductor design to optimize power consumption, particularly in low-power and battery-operated applications.

1.8 ON-State Current:

ON-State MOSFET is state at which MOSFET threshold voltage is less than the gate voltage. Because of this the current flow is defined as ON state current and it is represented as I_{ON}. From source, electrons are transferred towards to drain.

1.9 OFF-State current:

"OFF-state" condition in MOSFET occurs when Vgs is lower than the Vth, meaning that no current flows from the drain to the source. However, current flow is due to the minority charge carriers between the drain and the source, which is referred to as "sub-threshold current". This current flow is defined as OFF state current which is because of minority charge carriers and it is represented as I_{OFF}. The other name of the OFF-state current is subthreshold current.

1.10 Threshold voltage:

Channel inversion occurs when there is a minimum amount of voltage in between gate and source which is generally named as MOSFET threshold voltage (V_T). Gate-to-source voltage is minimum for nMOS transistor. Surface inversion is caused by the V_{gs} therefore, conducting channel is created among the drain and source. There is no flow of current for the condition $V_{gs} < V_{th}$ in between source and the drain. High channel current in source and drain through the minority charge carriers for the condition $V_{gs} > V_{th}$. But width of depletion region and surface potential are remains constant as beyond the threshold voltage V_{gs} is increased.

1.11 Transconductance:

The ratio between drain current variation and transistor gate-voltage,for small time interval in Id versus Vg curve is called Trans-conductance and it is denoted with g_m. Required amplifier gain is obtained with transconductance

with higher values [12].

$$g_m = \frac{2I_{ds}}{|V_P|}\left(1 - \frac{V_{gs}}{V_P}\right) \ldots\ldots (2)$$

1.12 Stability factor:

MOS transistors two-port equivalent circuit parameters mainly influences the stability factor (k). in RF frequencies range, transistors conditional stability is decided by this stability factor and it is expressed as:

$$K = \frac{2Re[Y_{11}]Re[Y_{22}] + Re[Y_{12}Y_{21}]}{[Y_{12}Y_{21}]} \ldots . (3)$$

Here, input and output admittance parameters are denoted as Y_{11} and Y_{22} at port 1 and 2 respectively. Transfer admittances are denoted with Y_{12} and Y_{21}.

1.13 Sub Threshold Slope (SS):

Within the sub-threshold region, the gate terminal governs the drain current, leading to an exponential decrease in current. It is essential to maintain a sub-threshold slope of approximately 60 mV/decade to mitigate heating effects in short-channel-devices. Control of drain-current through gate terminal results in its reduction. The "sub-threshold slope" is determined based on the bulk and source voltages, as well as the voltage across the drain, and is evident in the slope of the drain current plotted against these voltages. In short channel devices, heating effects are controlled by selecting the sub threshold slope with suitable value (approximately 60 mV/decade). The expression of subthreshold slope is denoted as follows:

$$SS_{th} = \ln(10)\frac{kT}{q}\left(1 + \frac{C_d}{C_{OX}}\right) \ldots . (4)$$

1.14 Junction capacitance:

In MOSFET junction capacitances are formed because of charge depletion between the substrate and source/drain. The source/drain voltage, changes are attained in charged depletion. Channel formed at the surface obtained when the gate voltage is more than threshold voltage. In RF frequency range, transistor small signal analysis uses the junction capacitances as deciding factors. New transistor structures and future scaling trends are decided by the factors of ON and OFF-state parameters of MOSFET [13]. Memory, digital circuit, biomedical applications and analog/ RF applications are different applications which influence the MOSFET structures designing. DC and AC performance parameters are calculated for performance analysis of MOSFET applications which are studied in this Chapter. Desired performance is achieved by using important circuit design analysis

1.15 Techniques to overcome Short channel effects:

To mitigate the challenges posed by “short-channel effects”, various state-of-the-art techniques have been presented, including:

1.15.1 Utilization of high-k gate metals.

Tunable work functions offer flexibility in adjusting the threshold voltage (Vth) of the device. Gate tunneling, which becomes significant in short-channel devices and can be suppressed by employing high-k gate metals with high tunneling barriers. High-k gate metals can improve the electrostatic coupling between the gate and the channel, enhancing gate control in short-channel devices

1.15.2 Implementation of "Silicon-on-Insulator (SOI)" structure.

In SOI devices, the ‘buried oxide’ (BOX) layer effectively isolates the transistor body from the substrate, reducing parasitic capacitance coupling between the source and drain regions. As a result, SCEs are minimized. SOI devices have

improved gate control on the channel. SOI technology facilitates the scaling of device dimensions to shorter channel lengths without significant degradation in performance. The improved electrostatic control, reduced parasitic capacitance, and absence of substrate doping effects in SOI devices enable the fabrication of short-channel devices with minimal SCEs. This scalability is crucial for advancing semiconductor technology and achieving higher integration densities.

1.15.3 Application of the "Strained-Silicon" technique.

Strained-silicon technology involves applying mechanical strain to the silicon lattice, which alters its atomic structure and increases carrier mobility. By inducing strain in the silicon channel, the mobility of electrons and holes is enhanced, leading to improved device performance. Higher carrier mobility allows for faster charge transport, mitigating SCEs such as drain-induced barrier lowering (DIBL) and improving the on-state current.

1.15.4 Adoption of multi-gate structures.

The primary benefit of multi-gate structures lies in their enhanced mitigation of short channel effects. By electrostatically controlling the channel (body) from multiple directions through the gate, these devices offer superior channel regulation compared to traditional transistor structures. Consequently, undesirable leakage elements are minimized, enabling the utilization of smaller transistors for cost-effective miniaturization. Furthermore, the enhanced gate control leads to reduced output conductance. This results in higher voltage gain, which proves advantageous for both analog and digital circuits by improving noise tolerance. Multi-gate structures improves on-state drive current (Ion) and therefore faster circuit speed is obtained[5].

1.15.5 HIGH-K Dielectric Materials

The use of high-k dielectric materials plays a crucial role in addressing short-

channel effects and advancing semiconductor technology. By offering improved gate electrostatics, reduced gate leakage, tunable threshold voltage, compatibility with advanced processes, and scalability to smaller dimensions, high-k dielectrics contribute to the development semiconductor devices for a wide range of applications.

1.15.6 Wide band gap materials

Employing wide bandgap materials in Multi gate MOSFETs offers several advantages, contributing to the improvement of device performance and enabling novel functionalities. Materials with wide bandgaps, such as silicon carbide (SiC) or gallium nitride (GaN), offer enhanced electron mobility compared to silicon (Si), resulting in improved ON-state performance in Multi gate MOSFETs. This enhancement leads to higher drive currents and faster switching speeds.

Furthermore, wide bandgap materials typically demonstrate lower leakage currents due to their larger bandgap energies. By integrating these materials into Multi gate MOSFETs, the reduction in OFF-state leakage occurs, contributing to enhanced power efficiency and decreased standby power consumption. This aspect is particularly crucial for low-power applications and energy-efficient electronics.

Moreover, wide bandgap materials inherently possess higher breakdown voltages than silicon, rendering them suitable for high-voltage applications. In Multi gate MOSFETs, this feature results in improved reliability and robustness, enabling the devices to function at higher voltages without experiencing breakdown.

Additionally, wide bandgap materials exhibit superior thermal conductivity compared to silicon. Consequently, Multigate MOSFETs based on these materials can operate at elevated temperatures while maintaining device performance and reliability. SiC has higher thermal conductivity than other

materials, allowing it to dissipate heat more effectively, and it has a wide bandgap which allows it to operate at higher frequencies.4H silicon carbide (4H-SiC) high thermal conductivity (4.9 W/(cm. K)), low dielectric constant (9.7), wide-band gap (3.26 eV), high breakdown electric fields (4 MV/cm), and fast electron saturation drift speed.

Currently, multi-gate JLFETs structures have risen to prominence as the primary candidates for the future of CMOS device technology.

1.16 Multi-Gate FET-The Future CMOS transistor and advantages

The key advantage of multi-gate devices lies in their superior ability to address short-channel effects. These devices excel in channel control because of the electrostatic influence exerted by multiple gate terminals from various directions, providing more efficient channel regulation when compared to conventional transistor configurations. This results in diminished undesirable leakage components and enables the utilization of smaller transistors, furthering cost reduction through size reduction. The improved gate control additionally leads to reduced output conductance.

Multi-gate devices offer an additional advantage in their ability to enhance the on-state drive current (Ion), leading to heightened circuit speed. This enhancement in Ion is influenced by a variety of factors [5]. The reduction in channel doping helps minimize impurity Coulombic scattering, and the decreased channel doping levels lead to a decrease in the electric field that is perpendicular to the SiO2 interface. As a result, surface roughness scattering is also diminished.

1.17 Research Gap and Motivation

To address the challenges posed by short channel effects in multigate devices, JLFET technology emerges as the most promising solution for applications requiring low power consumption and high frequencies. This motivates us to

initiate research endeavors focused on junctionless device[28]. The process of scaling down semiconductor devices has led to the emergence of numerous short channel effects (SCEs), impacting device functionality. In response to this challenge, researchers are increasingly motivated to explore novel structural designs such as 'double-gate', 'triple-gate', and 'gate-all-around' configurations. [93].

Research work need to be carried out in investigating electrical properties of Multi-gate-FETS with wide band gap materials to enhance analog/RF performance.

To analyze the effect of reduction in temperature on the DIBL parameter for 'P+ pocket SiC gate all around Junction less field effect transistor'.

To analyze the effect of decrease in the pocket length on the drain current in sub-threshold region for 'P+ pocket SiC gate all around Junction less field effect transistor'.

Simulations to characterize the thermal behavior of 'P+ pocket SiC GAA-JLFETs' over a range of temperatures need to be studied.

1.18 Comparative Study

PARAMETER-NAME	MOSFET	DGMOSFET	JLFET	GAA JLFET
SCE	Limited	Improved	Limited	Effective
Fabrication complexity	Low	Moderate	Moderate to High	High
Switching Speed	Moderate to High	Moderate to High	Moderate to Low	Very high
Ion/Ioff	Good	Better	Good	Excel

Ratio				lent
Threshold Voltage Control	Yes	Improved	Limited	Enha nced
Leakage Current	Low	Low to moderate	Low to moderat e	Low
Application Range	Broad	High performanc e Logic	High Power applicati ons	Nano Scale Ultra low power

1.19 Research Objectives

To analyze the electrical performance of Multi-gate Field effect transistors (i.e., 'P+ pocket SiC gate all around Junction less field effect transistor' and double-gate MOSFET).

1) To develop a mathematical model for the drain current and electric field of 'P+ pocket SiC gate all around Junction less field effect transistor'.

2) To analyze the influence of temperature in 'P+ pocket silicon carbide (SiC) gate all around junction less field effect transistor' (GAA JLFET).

3) To develop a physics-based analytical model of double-gate MOSFET for its electrical characteristics and high-voltage application.

1.20 Proposed Methodology for designing Multigate-FETs

- Literature Review:

Conduct a comprehensive review of existing research on Multigate-FETs, focusing on device structures, material properties, and simulation methodologies.

- Identify the latest advancements, challenges, and opportunities in design

and simulation using wide band gap materials.

- Define Device Specifications:

Consider application-specific requirements such as high-frequency operation, high-temperature performance.

- TCAD Tool Familiarization:

Acquire proficiency in Silvaco TCAD software for device simulation.

Explore capabilities of Silvaco TCAD relevant to SiC-based device modeling.

- Device Structure Design:

Design the physical structure of the device proposed on wide band gap material as substrate, including layer thicknesses, doping profiles, gate geometry, and source/drain contacts.

- Material Parameters and Models:

Material parameters for SiC into Silvaco TCAD, including carrier mobilities, doping concentrations.

- TCAD Simulation Setup

Identification of the Device structure

Material & Model specification.

Understanding the basic device physics and reliability.

Alternative semiconductor materials identification.

Two-dimensional device architecture to be developed with Silavco TCAD environment.

- Device Simulation:

Perform TCAD simulations to characterize electrical performance of the GAA-

JLFET, DGMOSFET, including current-voltage (I-V) characteristics, transfer characteristics, subthreshold behavior, and capacitance-voltage (C-V) characteristics.

Validate the simulated results against theoretical expectations and experimental data from literature, if available, to ensure accuracy and reliability.

- Performance Optimization:

Analyze the simulation results to identify opportunities for performance enhancement, such as optimizing gate oxide thickness, channel doping concentration.

- Documentation and Reporting:

Document the entire design process, simulation methodology, and key findings in a detailed report.

Present the results, insights, and recommendations to stakeholders, collaborators, or peers through presentations or publications in relevant journals or conferences.

1.21 Organization of thesis.

In thesis different advanced structure and their applications are explained. Proposed structures with its detailed dimensions are analyzed considering potential and electric-field, Ion /Ioff current ratio, DIBL and SS. Sensitivity parameters are also analyzed. Analytical modeling of the device is also derived.

Chapter 1 Explains the basics of MOSFET, its need and challenges, operating principle different advanced MOSFETs and performance parameter of MOSFET.

Chapter 2 Emphasizes that for the sub 45 nm technology node, many gate and channel developed advanced MOSFET architectures are evaluated and compared. The SS ION/IOFF and DIBL values of several MOSFET

architectures are compared.

Chapter 3 Explains the basic working principle of P+ Pocket SiC-GAAJLFET along with its analog and Rf parameters.

Chapter 4 explains about the designing of P+ Pocket SiC Analytical Model of GAAJLFET with impact of High Temperature. It also describes results obtained including ON /OFF current of the device. The sensitivity characteristics of the device, such as drain extension, gate overlapping length, and oxide thickness, were compared to those of GAA JLFET with doped channel regions.

Chapter 5 explains the Modeling and Simulation of Multi-Gate FET for High power applications with diminished SCE. The dimensions of the device is mentioned in tabular form and also SCEs like DIBL and SS are also calculated.

Chapter 6 Outlines the research's findings and potential applications in the future.

CHAPTER 2

Literature Review

Successful integration of the ICs with MOS technology is very efficient therefore in semiconductor industry this MOS technology is widely used. Aggressive and continuous MOS transistor scaling leads to exponential growth of IC industry for couple of years. As Device dimensions decreases continuously, the speed of operation and packaging density of MOSFET increases but, parasitic capacitances, Short-channel effects and leakage current become significant with channel length and MOSFET size reduction. Performance of the computer chip is doubled for every two years along with doubling transistor count. Diminishing the dimensions of a MOSFET results in a reduction in the channel length, consequently giving rise to short-channel effects and an increase in leakage current. The MOSFET design with Double gate is having a better performance in amplifiers over the MOSFET with single gate. Transistors current drive capability increased with increasing the number of gates. Quadruple gates in GAA MOSFET around four side's increases the controlling action of channel region. Therefore, reduction in leakage current, drain current improvement limits the short channel effects. Different materials based multi gate MOSFET's performance characteristics which are greatly used in their manufacturing are analyzed.

2.1 Literature Survey

Vibhaas Saxena et.al. presents a research study and analysis focused on a modified 18nm gate length. [14]. JL-SOI transistors limit by low sub-threshold slope, I_{on} to I_{off} ratio and high leakage current. Moderately doped p-type silicon is added to the buried oxide region of a typical JL-SOI MOSFET to

address these problems. Less chip area and electrical performances are improved with the new optimizing windows which are below the gate length, channel area and junction-less modification. The buried oxide thickness (BOX) of SOI MOSFETs is analyzed.

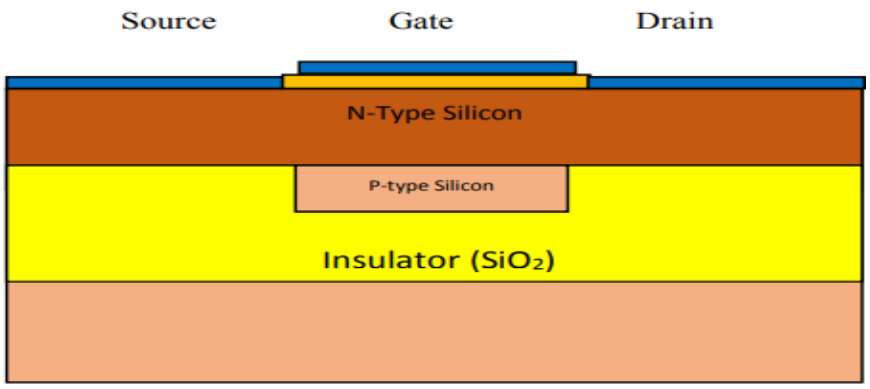


Fig. 2.1: 18NM GATE LENGTH STRUCTURE OF MODIFIED SOI-JLT [14]

The simulation of the modified junction-less SOI transistor, as depicted in Figure 2.1, is performed using the Sentaurus TCAD device simulator. The equations of charge continuity are used for calculation of holes and electrons movement. Band analysis and drain current calculations are used for transport model of energy equalization. Referenced conditions with self-heating condition combinations are considered along with the hot electron effects. Modified junction-less SOI transistor different input characteristics are analyzed . At buried oxide interface and channel, depletion region formation is the main advantage of the described method in order to obtain the more benefits than the conventional SOI-JLT. BOX thickness reduction is used in reduction

of leakage current in this study.

Main findings or conclusion relevant to proposed research work:

The low leakage pocket junction-less DGTFET with a biosensing cavity region is detailed in the work by Suman Lata Tripathi and colleagues [15]. $Si_{0.7}Ge_{0.3}$ Narrow band gap material pocket region with DGTFET shows increment in tunneling between bands and the threshold characteristics for achieving the digital and memory applications with high speed and low power. Atmospheric changes are effectively detected in the JLDGTFET with cavity region which automatically changes the threshold voltage and drain current.

2D structure of JLDGTFET with depth gate length L_g= 15 nm and height H_g = 4 nm is proposed. Gate contact materials (Al, Pt, etc.) and the gate (SiO_2, HfO_2, etc.) are different oxide materials which are used in investigation of described method. Because of gate influence, near the source region $Si_{0.7}Ge_{0.3}$ (energy band gap of < 1 eV) pocket region with 5 nm thickness is included for increasing the tunneling property of band to band. Oxide region made of SiO_2 (3.9) instead of high-K dielectric material HfO_2 (25) under Al/SiO_2 interface performance is compared, metal gate is having the high value of work function for achieving ON-state current.

Bio Sensing cavity region with JLDGTFET of 3 nm depth and 5nm width under both bottom and top gate contacts 2D view is represented.

Cavity region with the pocket $Si_{0.7}Ge_{0.3}$ JLDGTFET ON/OFF

performance is studied to improve the biomolecules sensing capability present in the atmosphere. Therefore, air present in the cavity dielectric constant is influenced then overall performance is changed. $Si_{0.7}Ge_{0.3}$ JLDGTFET novel thin body pocket is simulated by using the 2D/3D Visual TCAD tool.

In the analog domain, graded channel, dual material gate junction-less MOSFET (GC-DMGJL MOSFET) is described for applications by the Pathak et al. [16]

Short channel effects reduction, high trans-conductance and drain current are the results of GC-DMGJL MOSFET. There is a high doping area near the channel drain region of the device $N_{gd} = 2.5 \times 10^{19}\ cm^{-3}$ and remaining area uniformly doped with $N_d = 2 \times 10^{19}\ cm^{-3}$. $L_{M1}{:}L_{M2}(nm) = 15{:}15$ is the ratio of metal length. $W_{M1}{:}W_{M2}(eV) = 5.353 : 4.8$ is the metal work function ratio. 2nm is the oxide thickness. W_{SP}= 10 nm is spacer length. T_{Si} = 10 nm is silicon thickness.

The analysis of surface potential based on MgZnO/ZnO High Electron Mobility Transistors (HEMT) is conducted by Yogesh Kumar Verma et. al. [18]. The transistor structure with high electron mobility is designed and simulated. Simulation techniques are used to calculate the device parameters and results are clear that this method is efficiently used by the all for commercial circuit applications with all reliability criteria. Sapphire substrate, buffer layer and barrier layer are presented in the proposed structure.

Nitride and Gallium Arscenide based devices are having the less drain currents as compared to drain current method. low scattering effects are processed in the High Electron Mobility Transistors (HEMT) than the traditional MOSFETs.

Enhanced Electrical Performance of TFETs with Ferroelectric Dual Material Gates all around (FEDMGAA-TFETs) is described by Varun Mishra t. al. [19]. Drain current increased by the negative capacitance with the development of gate terminal internal positive feedback which is noticeable by the ferroelectric material. FEDMGAA-TFETs electrical characteristics are improved. Ferroelectric layer and ferroelectric material thickness changes are examining the device performance. Ferroelectric layer relation with polarization and coercive field are very difficult. Ferroelectric layer thickness impact is investigated by the practical analysis on the device performance at polarization and fixed coercive field. The high thickness of ferroelectric layer improves drain current which is observed from the results. Changes in ferroelectric material thickness have minimal effects on device off current.

Ferroelectric material uses the better contender as Si: HfO_2 in difference with PZT and SBT as perovskite material which gives the better scaling for nanometer range also. Switching ratio (I_{ON} /I_{OFF}) and ON current improvements are observed from the results. Therefore, low voltage and energy efficient applications are utilizes the described DMGAA-TFET fig 2.2.

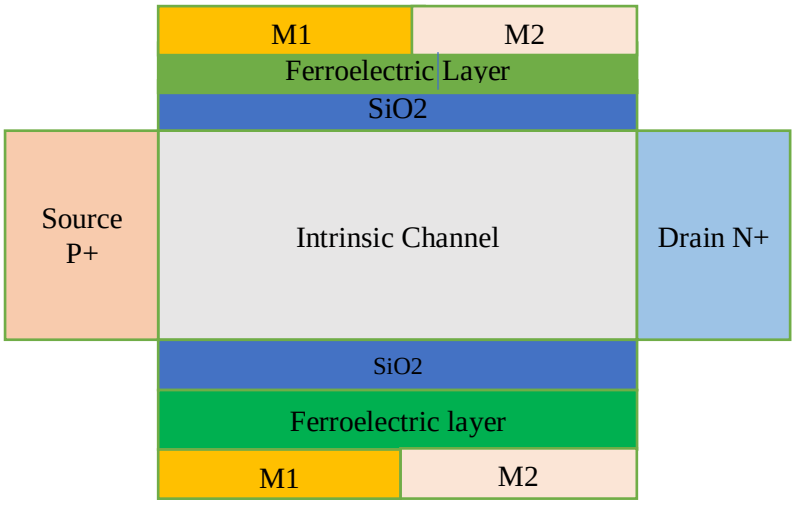


Fig 2.2: FE-DMGAA TFET CROSS-SECTION SCHEMATIC VIEW[19]

Yogesh Kumar Verma et al. have introduced extrinsic reliability issues and their impacts, including those related to radiation and temperature, on SiGe HBT (Silicon Germanium Heterojunction Bipolar Transistor). [20]. Intrinsic and extrinsic are two types in SiGe HBT reliability issues are analyzed. SiGe HBT cross-sectional view is presented. Inherent tradeoff between base resistance and dc current gain is the Si bipolar transistors fundamental limitation. Because of injected electrons back into the base and injected holes back into the emitter is the main reason for occurrence of tradeoff which means that, at same height potential barrier uses these electrons and holes. Hence in base, ionized acceptor concentration is reduced, current gain is increased which results the high base resistance.

To activate the high-speed mode, at 77K the maximum cut off frequency of 155 GHz is observed and called as cryogenic temperature. High Speed Mode Gain is maximum at 77K as 25.5dB. Therefore, it is clear that, maximum gain value and maximum cut off frequency are obtained at cryogenic temperatures of SiGe HBT. In Silicon transistor neutron radiation effect on transistor gain is also studied completely because these effect influences the performance of the transistor gain.

Abhinav gupta et.al. have conducted an analysis of Gate-Underlap Junction-less Double Gate MOSFETs (JLDG MOSFETs) [21]. Two cases are considered for evaluation. The channel region of JLDG-MOSFET source end portion having the underlapped gate region which included in the first case. The channel region of JLDG MOSFET drain end portion having the underlapped gate region which is included in the second case. Dielectric modulation techniques are used in detecting the biomolecules with these two types of structures. On JL DG MOSFET surface potential effect is produced by the charged biomolecules.

There is a movement for surface potential upwards because of positively charged biomolecules and movement for surface potential downwards because of negatively charged biomolecules. Device parameters 50nm as cavity length,

19nm as cavity thickness, 50nm as Gate length, 10nm as gate oxide thickness, 20nm as channel thickness, source drain channel doping is $1 \times 10^{24}\ m^{-3}$, 1nm as oxide layer thickness in open cavity.

Abhinav et al. addressed the concerns associated with JLDG MOSFETs. [22]. Thermal stability between 200 to 500 K and gate misalignments are studied. The current in these structures are reduced with the misalignments in gate. MOSFET performance also affected by the front and back gate alignments. Gate-misalignments give rise to non-ideal effects

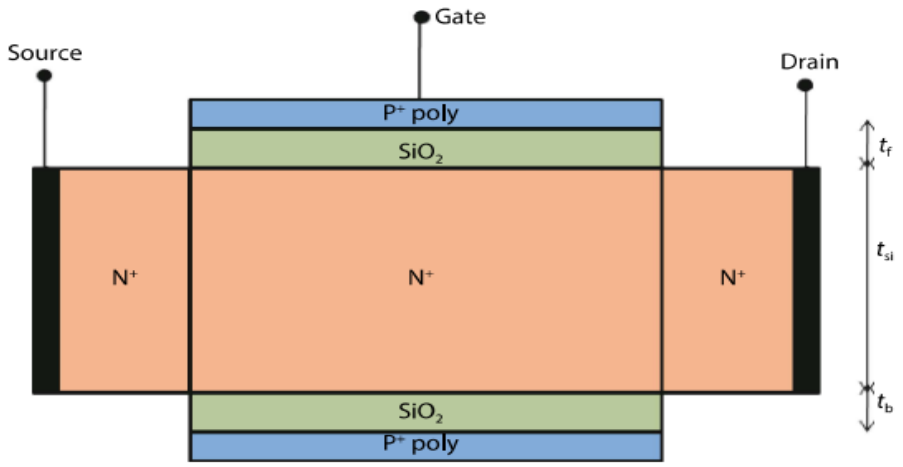


Fig. 2.3: N-TYPE JLDG MOSFET STRUCTURE [24]

Device dimensions are as follows: front gate oxide thickness of 1nm, 1nm thickness for back gate, 5nm thickness for silicon substrate, $3 \times 10^{19}\ cm^{-3}$ is value of doping concentration N_d, 5.2 eV as gate work function and 20nm of channel length.

Junction-less double gate (JLDG) MOSFET simulation, analytical

surface potential modeling for ultra low-power analog/RF circuits are presented by the Nirmal Ch. Roy et. al. [24]. Channel, Source and drain are uniformly doped with $N^+ - N^+ - N^+$ structure of N-channel JLDG Transistor as shown in below Figure 2.3. Channel length and channel thickness along with surface potential distribution of the described model is derived. The channel of the p-n junction of proposed junctionless MOSFET is not having the doping levels as Source/Drain region. The comparative numerical evaluation of analytical model is conducted using the ATLAS device simulator.

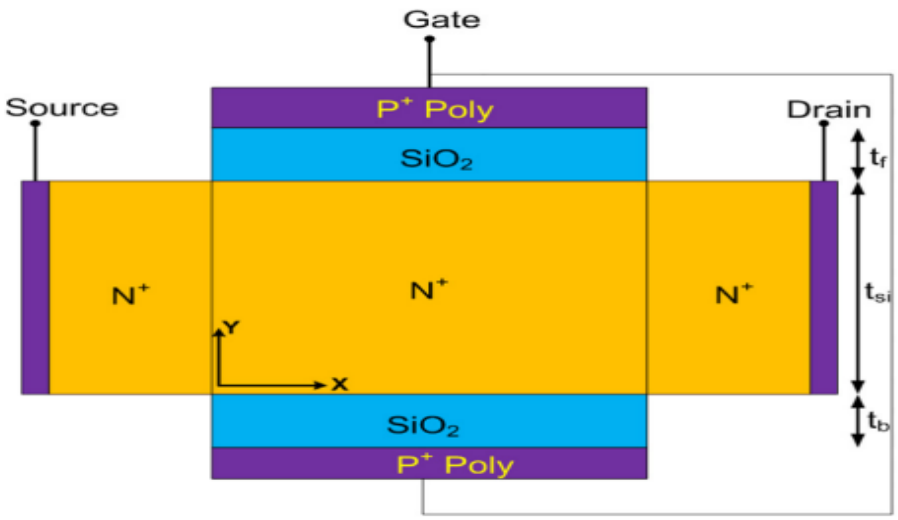


Fig. 2.4: N-TYPE 'JLDG MOSFET[24]

ATLAS device simulator is used comparative numerical evaluation of analytical model. The JLDG MOSFET demonstrates a better resistance to SCEs when compared to junction-based DG- MOSFET, as indicated by the results. Following comparative analysis, there is an observed increase of 17.08% in the current ratio (I_{ON}/I_{OFF}) a reduction of 4.52% in DIBL, and a decrease of 1.61%

in Sub-threshold Slope. It is evident that the junction-based DG MOSFET exhibits higher susceptibility to short channel effects when compared to the JLDG MOSFET. Therefore, I_{ON}/I_{OFF} ratio, sub-threshold swing and DIBL are influenced by doping concentration of JLDG MOSFET.

Engineering effect on DG MOSFET is discussed by the Sarkar et. al. [25] as shown in below Figure 2.4. Tri-Material Double Gate MOSFET (TM DG MOSFET) with fully depleted model is designed. The enhancements in the analog, linearity performance, and RF parameters of DM DG MOSFET are contrasted with those of a single material DG MOSFET for comparison. 35 nm CMOS technology is used for designing the proposed structure. Different work functions of different three gate materials are selected for the n-MOSFET. The selected work function are $\emptyset_{M1} = 5.0\ eV, \emptyset_{M2} = 4.75\ eV, \emptyset_{M3} = 4.5eV$.

Gate material with higher work function is positioned at source, while gate material with lower work function is positioned at drain. Polysilicon metal gates are used because of having dopant penetration effect and polysilicon depletion width. 10 nm is the Si film thickness and 2 nm is the SiO_2 thickness. $10^{20}\ cm^{-3}$ is the source and drain dopant concentration. Three material length ratio is considered as $(L_1 : L_2 : L_3 = 1:1:0)$. $10^{16}\ cm^{-3}$ is considered as p substrate doping concentration.

F. Djeffal et. al.[26] presented a GAAJLMOSFET with source-drain extensions for improved performance. Structure shown in figure 2.5 the doping

concentration of channel is low compared to source as well as drain. By extending the source/drain the drain current is observed to be improved. GAA junction less MOSFET with extended source/drain regions observed to have improved drain current when compared to conventional GAA MOSFET. The on current magnitude increases by 70% with source drain extensions. The channel length is 100nm, doping concentration of channel is 10^{18} cm^{-3} and source/drain extension is 10^{19} cm^{-3}. The oxide thickness is 5nm.

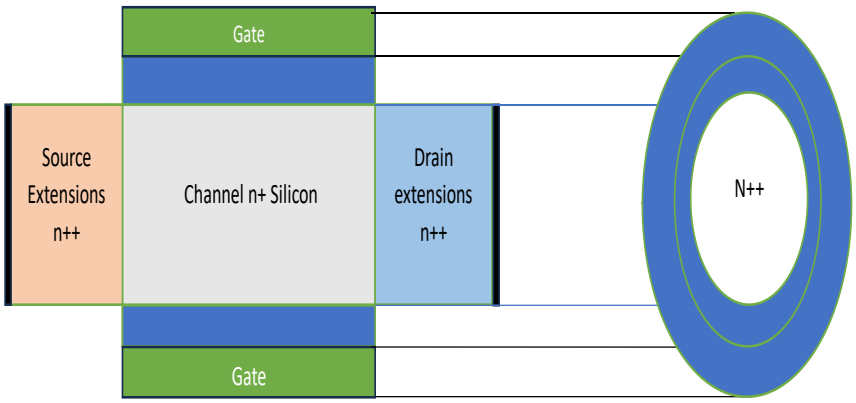


Fig. 2.5. GAA JLMOSFET with S/D extensions regions [26]

2.2 LITERATURE REVIEW TABLE

Author	Year of publication	Main findings or conclusion relevant to the proposed work
'Vibhaas Saxena, Yash Gupta, Suresh Kumar, Nitu Rao and Vimal Mishra'[72].	2020	An analysis was conducted on an 18nm length Junction less SOI MOSFET, utilizing slightly doped silicon as a novel channel material.
Suman Lata Tripathi, Raju PATEL, Vimal Kumar Agarwal [73]	2019	An analysis of pocket inclusion and influence of bio cavity region in junction less DGTFET.
Patak V, Saini G [74]	2018	Mitigates short channel effects while achieving high drain current and transconductance, even with a channel length of 30 nm.
Yogesh Kumar Verma, Santosh Kumar Gupta, Varun Mishra, Prateek Kishor Verma [76]	2018	MgZnO/ZnO HEMT structure is analyzed based on surface potential and compared with MOSFET.
'Varun Mishra, Y Kumar Verma, Prateek Kishor Verma, Santosh Kumar Gupta'[77].	2018	FEDMGAA-TFETs structure with enhanced electrical performance is designed. Investigated the effect of ferro electric layer thickness on drain current.
'Y Kumar Verma, Varun Mishra, Prateek Kishor Verma, Santosh Kumar Gupta'[78].	2018	An investigation was carried out on a SiGe HBT structure to assess extrinsic reliability concerns, radiation and temperature-related effects.
Abinav gupta, Sanjeev Rai[80]	2017	JLDGMOSFET is analyzed for gate overlap over source and drain end for 20nm channel length.
Nirmal Ch.Roy, Abhinav gupta, Sanjeev Rai[82]	2015	Gate Misalignment with thermal stability between 200k to 500k is investigated.The current is observed to be reduced due to misalignment of gate. DIBL decreased by 4.52 percent, the subthreshold slope reduced by 1.61 percent, and the ratio increased by 17.08 percent, all while maintaining a channel length of 20 nm.
Sarkar Angsuman,Aloke Kumar Das, Swapnadip De,Chandan Kumar Sarkar[83]	2012	The performance of the RF system exhibits improvement. In a comparison between the DM DG MOSFET and the SM DG MOSFET, it is evident that the DM DG MOSFET outperforms in terms of linearity and analog performance, all while maintaining a channel length of 35

		nanometers.
F. Djeffal, H. Ferhati, T. Bentrcia[84]	2016	The heavily doped regions have contributed to a notable 70 percent increase in the magnitude of the ION current.
'Vibhaas Saxena, Yash Gupta, Suresh Kumar, Nitu Rao and Vimal Mishra'[72]	2020	An analysis was conducted on an 18nm length Junction less SOI MOSFET, utilizing slightly doped silicon as a novel channel material.
Pratikhya Raut, Umakanta Nanda and Deepak Kumar Panda[99]	2023	A thorough examination of diverse JLFET structures was conducted, assessing numerous parameters and providing an overview of forthcoming generations of JLFET structures designed to enhance performance and streamline modeling.
Gupta, V., Kumar, N., Awasthi.[100]	2021	An analytical model has been proposed to predict the center channel potential for GC-GAAJLFET. The 3D Poisson's equations have been successfully resolved. Additionally, the research has investigated the effects of elevated temperature and doping concentration on the center potential and subthreshold current.

2.3 Summary of material properties of SiC with other semiconductors [99]

	Si	**GaAs**	**GaN**	**4H-SiC**
Bandgap, Eg (Ev At 300k)	1.2	1.43	3.4	3.3
Relative Dielectric Constant, ε_r	11.9	13.0	9.5	10.0
Saturated Drift Velocity, V_{sat} (10^7 Cm/S)	1.0	1.0	2.5	2.0
Critical Field, Ec (Mv/Cm)	0.25	0.3	3.0	3.0—4.0
Thermal Conductivity, Λ, (W/M· K At 300k)	150	50	130	300-400
Bulk Mobility, μ_e(Cm^2 / V. Sec At 300 K)	1350	8500	1000	950

2.4 Literature survey with respect to wide band gap materials

Author	Year of publication	Main findings or conclusion relevant to the proposed work
Baruah, R.K., Mahajan, B.K. & Routh, S[88].	2023	A double-gate junction-less SiC FET featuring an embedded P+ pocket within the oxide layer (P+-SiC JLT) has been developed to evaluate its DC and AC performance in high-temperature and high-voltage scenarios. This innovative device showcases enhanced volume depletion, improved Ion/Ioff ratio, and intrinsic gain.
Y. Wei, M. M. Hossain and H. A. Mantooth.	2023	Semiconductor devices based on Si, GaN, and SiC have been tested under both room temperature and cryogenic conditions. It was observed that Si and GaN semiconductor devices exhibit enhanced performance characteristics, including lower on-state resistance and faster switching speeds, particularly at lower temperatures.
G. Iannaccone, C. Sbrana, I. Morelli	2021	Power electronics applications benefiting from Wide Band Gap (WBG)

and S. Strangio [80]		semiconductors capitalize on the electrical and thermal characteristics of SiC and GaN for power device utilization. SiC, in particular, is preferred for high-output power applications.
Singh, S., Chaudhary, T. & Khanna, G. [34]	2022	Recent advancements in Wide Band Gap (WBG) semiconductors, namely GaN and SiC, are regarded as the future of power electronics. The key challenges and promising prospects of upcoming developments in ultra-high voltage SiC devices and vertical GaN devices are explored.
N. Yadava and R. K. Chauhan [98]	2020	An RF-focused MOSFET utilizing Ga2O3 is customized for RF applications. To address leakage concerns, p-type NiO pockets are strategically positioned near the channel/drain and channel/source-interface regions. Furthermore, a graphene/BP layer is integrated to augment the RF performance of the p-type NiO pocket β-Ga2O3 MOSFET.

2.5. Summary

The study involves the analysis of various MOSFET-based Multigate Field Effect Transistors architectures, examining their structural features and dimensions. This research explores different FET structures, primarily aimed at mitigating short-channel effects, such as DIBL and Hot electron effect. These modifications include the introduction of a biosensing cavity region in junction-less DGTFET, enhancements to the SOI transistor to create a modified junction-less SOI transistor, the utilization of JLDG MOSFET, GC-DMGJL MOSFET, and transparent gate recessed channel MOSFET.

The research employs TCAD to investigate the RF performance of various structures. The results specify that the Multi-gate junction-less

MOSFET exhibits superior performance, aligning with future scaling trends and offering increased compatibility with MOS technology for various applications, including RF, IoT, and digital/analog applications.

The SiC GAAJLFET has been proposed 4H-SiC as nanowire material and P+ pockets on source and drain side regions, gate electrode work function range from 4.2 to 5.1 eV and device allows to operate at high temperature range from to 400 to 500K.The channel length in proposed device varies from Lg= 5-20 nm .The oxide layer thickness varies from 1-3 nm and the doping concentration N_d=1x10^{19} cm^{-3} .The P+ pocket length L_p varies from 3-10 nm and P+ pocket concentration N_A=1x10^{19} cm^{-3}.

CHAPTER 3

Compact Model for Analog/RF Performance of P+ SiC GAA JLFETs

Introduction

A mathematical model is developed to describe the drain current and electric field behaviors of silicon carbide gate all-around junction less field-effect transistors (SiC GAA-JLFETs). The unique gate-all-around architecture enables efficient control of the channel charge by the gate, thereby minimizing the influence of the drain region on the channel's electrostatics. This design effectively suppresses short-channel effects like DIBL and threshold voltage roll-off in the FETs. Moreover, these transistors exhibit a subthreshold swing near to the ideal value of 60 mV/decade, owing to the enhanced gate control. The gate electrodes encompass the entire channel region, offering optimal gate control. The device is operated in depletion mode where the channel is depleted of carriers. Depletion of the channel is achieved by using a gate electrode work function ranging from 4.7 eV to 5.1 eV in order to increase ION/IOFF ratio. P+ pockets are used on both the source and drain of the SiC GAA. Incorporating a P+ pocket on both the source and drain side regions of the JLFET enhances the efficiency of volume depletion. Thus, the expansion of the tunneling width at the channel-drain interface results in a notable decrease in the OFF-state current caused by the L-BTBT, by approximately an order of magnitude $\sim 10^{-15}$. Utilizing this model enables the optimization of the drain current of the JLFET by adjusting the parameters of the P+ pocket. The model can also be used to study the impact of the P+ pocket on the electric field distribution in the JLFET.

An analytical model incorporating Poisson's equation for the nanowire has been formulated to analyze the analog performance of the P+ pocket SiC GAA JLFET. Subsequently, the analog performance of this model was validated through simulation results obtained from SILVACO TCAD, demonstrating a strong agreement between the simulation outcomes and the analytical model's

predictions.

Silicon carbide (SiC) boasts higher thermal conductivity compared to other materials, enhancing its heat dissipation capability, and its wide bandgap enables operation at higher frequencies. Among SiC polytypes such as 3C-SiC, 6H-SiC, and others, 4H silicon carbide (4H-SiC) stands out for its exceptional properties including high thermal conductivity (4.9 W/(cm·K)), low dielectric constant (9.7), wide band gap (3.26 eV), high breakdown electric fields (4 MV/cm), and rapid electron saturation drift speed. 4H-SiC has recently garnered attention for use in JLFETs for high-voltage applications to enhance breakdown voltage by mitigating L-BTBT due to its wide band gap and high electric field tolerance. Despite these advantages, there are challenges for JLFETs such as decreased mobility induced by heavily doped channels, impacting gain or transconductance, and thus energy efficiency. To address these, channel engineering techniques have been proposed to enhance analog/RF performance by improving carrier transport efficiency.

When silicon devices are operated at temperatures above 400-425 K, they can suffer from reduced mobility of the electrons, which reduces their performance. This is because at higher temperatures, atoms vibrate more quickly and can interfere with the operation of the device. The intrinsic carrier concentrations of WBG semiconductors such as SiC are much lower than those of Nc Nv, which means they are much less susceptible to thermal damage at high temperatures. Several factors contribute to reducing heat generation and energy loss, including the high ON current and ION/IOFF ratio. WBG semiconductors are also more resistant to thermal breakdown due to their wide bandgap, which means that the atoms don't need to vibrate as quickly in order to create a current. The wide bandgap also allows for a greater current flow with less energy loss, which reduces heat generation. [95]. There have been recent studies on planar junction less FETs fabricated with 4H-SiC where the high voltage characteristics have been significantly improved, thus reducing the L-BTBT. For example, it has

been reported that the planar junction less FETs have achieved an off-state breakdown voltage of up to 4.8 kV with a low leakage current of 2 pA. [44]. In SiC JLFETs, P+ pockets were employed to deplete SiC channels to below 10 nm. P+ pockets are located at the source and drain sides of planar JLFETs, which hinder the formation of BJTs in the channel region. This prevents the carriers from forming a bipolar junction, which would otherwise create a parasitic BJT in the channel region. P+ pockets also increase the electric field in the channel, resulting in higher drain current and better device performance. When a higher drain voltage (VDS) is applied to the channel-drain interface, the tunneling width of the channel increases due to the presence of P+, which stops electron flow in the lateral direction. Additionally, JLFETs with a gate all around junction less configuration (GAA JLFET) has been thoroughly investigated using quantum confinement effects and negative capacitance.

A temperature-dependent analytical model for drain currents in 4H-SiC-JLFETs is proposed to investigate the analog/RF figures-of-merits characteristics. The temperature variation of intrinsic electrical parameters are considered, providing more accurate predictions of the device's analog/RF performance such as transconductance, transconductance generation factor (TGF), and output resistance. The intrinsic gain, the gain (A_v), and the early voltage are also included.

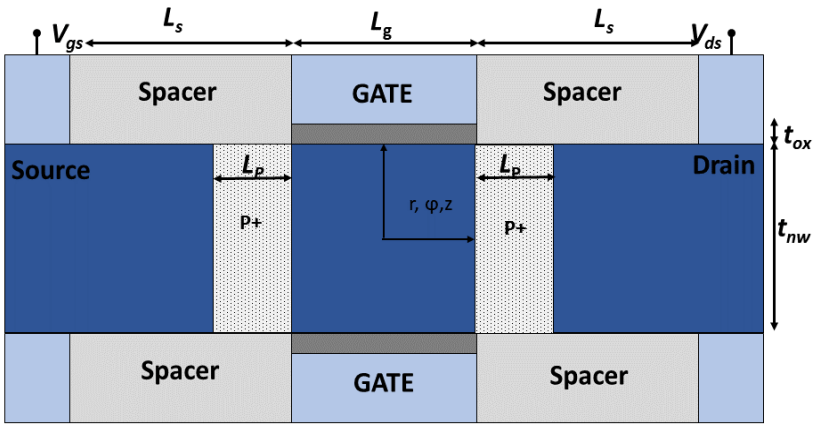
3.1 Device Parameters and Structure

A schematic representation of a P^+ pocket SiC GAA JLFET has been shown in Figure 3.1. This schematic demonstrates the physical structure of a P^+ pocket SiC GAA JLFET, and the associated parameters used in device simulations are provided in Table 3.1.

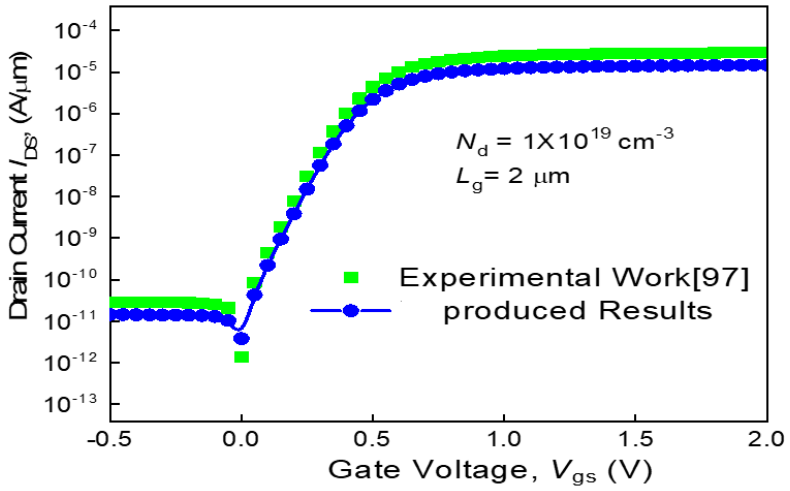
Table 3.1

Dimensions used for simulations

Parameters	Proposed Device
Nanowire Diameter (t)	5-10 nm
Oxide width (t_{ox})	1-3 nm
Doping Concentration (N_d)	1×10^{19} cm^{-3}
P+ Pocket Concentration (N_A)	1×10^{19} cm^{-3}
P+ Pocket Length (L_P)	3-10 nm
Gate metal (ϕ_m)	4.7 eV -5.1 eV
Channel length (L_g)	20 nm
Spacer Length (L_S)	20nm
Semiconductor Material	4H-SiC



(a)



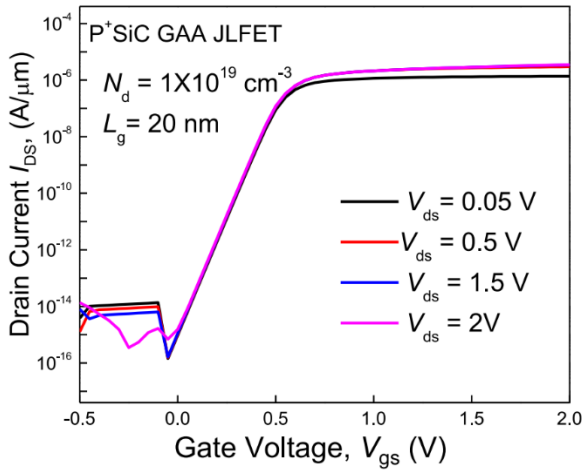
(b)

Fig. 3.1. (a) Schematic view of the P^+ SiC GAA JLFET and (b) Reproduction of results from TCAD [97].

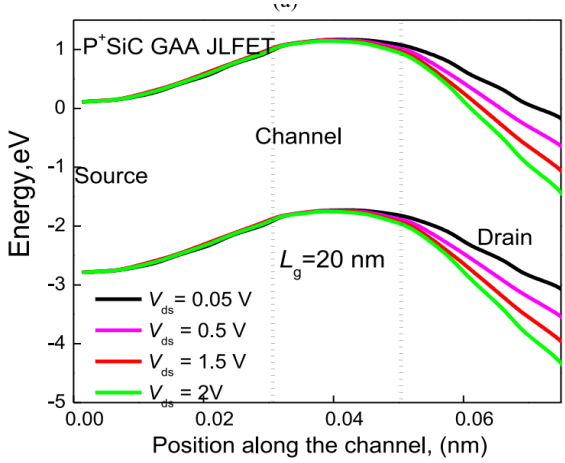
BTBT models with nonlocal properties have been integrated as the L-BTBT becomes apparent while scaling device below 20 nm regime. Such models are needed to accurately describe the carrier transport in nanoscale devices as short-range scattering effects become increasingly important. Nanowire recombination is modeled using the Shockley-Read-Hall model. Considering the use of 4H-SiC semiconductor material, our velocity saturation model uses a velocity of 2×10^7 cm^{-3}. Furthermore, this velocity saturation model is further enhanced by considering the scattering and deformation potentials for 4H-SiC, allowing for a more accurate modeling of the nanowire recombination. Considering the channel length of the proposed device ranges from L_g = 5 nm to 20 nm, taking quantum effects into consideration assists in improving simulation accuracy. In the P^+ pocket SiC GAA JLFET, quantum effects were captured using the Bohm quantum potential (BPQ) model. The BPQ model was able to accurately predict the quantum effects of the P^+ pocket SiC GAA JLFET, providing a reliable and accurate prediction. In addition to being independent of the

hydrodynamic model and drift-diffusion model, the BQP model has better convergence than the density gradient model. [98]-[99].

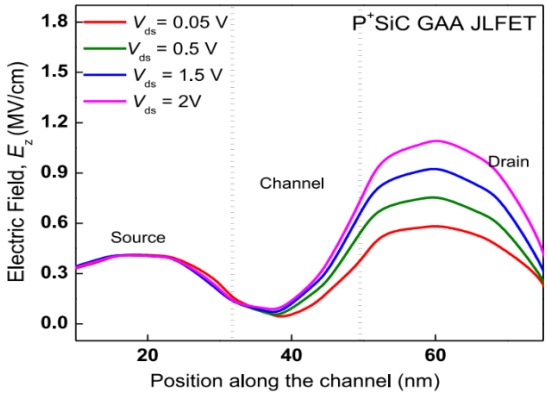
In order to increase the I_{ON}/I_{OFF} ratio, a gate electrode work function of 4.7 eV to 5.1 eV is used to fully deplete the channel. Source and drain are doped with P^+ pockets using $N_A = 1X10^{19}$ cm^{-3} and the whole SiC GAA uses $N_d = 1X10^{19}$ cm^{-3}. This work function for the gate allows for the maximum depletion of the channel, which maximizes the ION/IOFF ratio. The doping of the source and drain with P^+ pockets help to reduce the resistance and improve the performance of the GAA. Figure 3.1 illustrates how high-k gate side wall spacers must be used to achieve high ON state current in order to realize the nanowire. HfO2 is used as the gate oxide in SiC GAA JLFETs with a thickness of 1 nm in order to improve the device's electrical properties. This is because the gate oxide of HfO_2 is more resistant to leakage than traditional SiO_2, allowing for higher ON current. Additionally, using high-k gate side wall spacers helps to reduce the gate length of the device, resulting in higher transconductance and better performance. According to Figure 3.2 (a) SiC-JLFET have higher OFF-state currents than JLFET when compared to P^+ pocket SiC GAA-JLFETs. Figure 3.2(b) shows that the OFF-state current rises with varying drain voltages, but is still much lower than the current measured for JLFETs. As shown in figure 3.2 (c) the energy band diagram evolves with temperature as it goes from 300 K to 500 K. According to the L-BTBT effect, tunneling width decreases with increasing temperature. Figure 3.2 (d) illustrates the I_{ON}/I_{OFF} ratios as channel length changes. A decrease in channel length has been observed to decrease the I_{ON}/I_{OFF} ratio**.**


P+SiC GAA JLFET
Nd = 1X10^19 cm^-3
Lg = 20 nm
Vds = 0.05 V
Vds = 0.5 V
Vds = 1.5 V
Vds = 2V
Drain Current IDS, (A/μm)
Gate Voltage, Vgs (V)

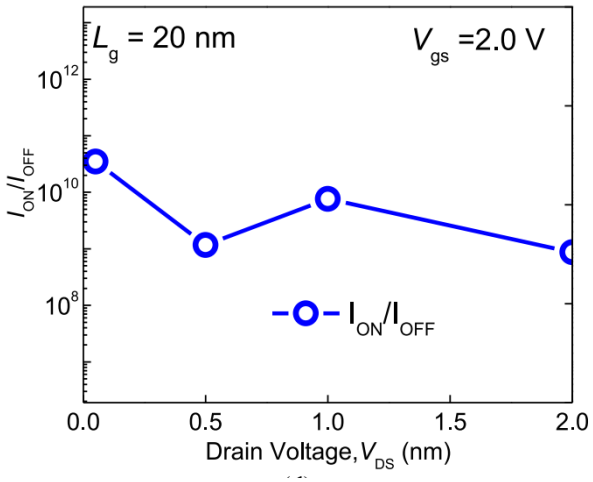
(a)


P+SiC GAA JLFET
Channel
Source
Drain
Lg=20 nm
Vds= 0.05 V
Vds = 0.5 V
Vds = 1.5 V
Vds = 2V
Energy,eV
Position along the channel, (nm)

(b)


Vds = 0.05 V
Vds = 0.5 V
Vds = 1.5 V
Vds = 2V
P+SiC GAA JLFET
Source
Channel
Drain
Electric Field, Ez (MV/cm)
Position along the channel (nm)

(c)



(d)

Fig. 3.2. (a) Ids–Vgs transfer characteristics at Vds=1.0 V of P+ pocket SiC GAA JLFET and (b) Energy band diagram (c) Electric field (d) ION/IOFF ratio of with Drain voltage of P+ pocket SiC GAA JLFET.

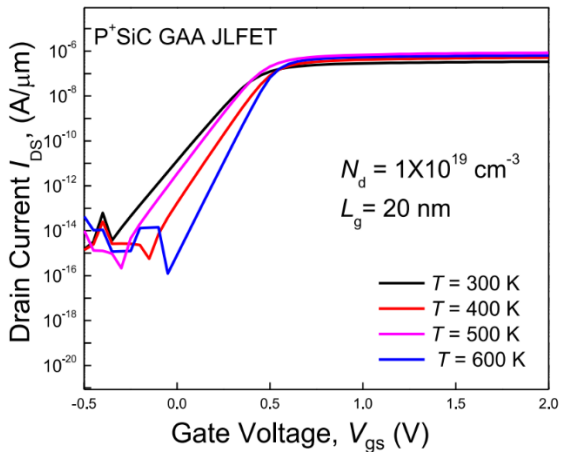
The Proposed SiC GAA JLFET with P+ pockets on both the source and drain sides perform significantly better than the conventional GAA JLFET even at temperatures up to 600 K shown in Figure 3.3. This improved performance is due to the additional electrons in the P+ pockets, which help reduce the surface potential and improve the gate control. When SiC WBG material is combined with JLFETs, it has a higher breakdown voltage than when used in isolation. This combination of WBG material and JLFETs are favorable for power electronics applications.

During the OFF-state of JLFET device, there is a requirement for the device to fully deplete the channel while the device is in the OFF-state, so the P+ pocket must completely deplete the channel outside the gate length. Due to the full volume depletion at the source-channel interface as well as the drain channel interface of the P+ pocket SiC GAA JLFET, the concentration of intrinsic charge carriers is low in the OFF-state. Further analysis has been conducted to assess the impact of temperature on the analog performance of the proposed

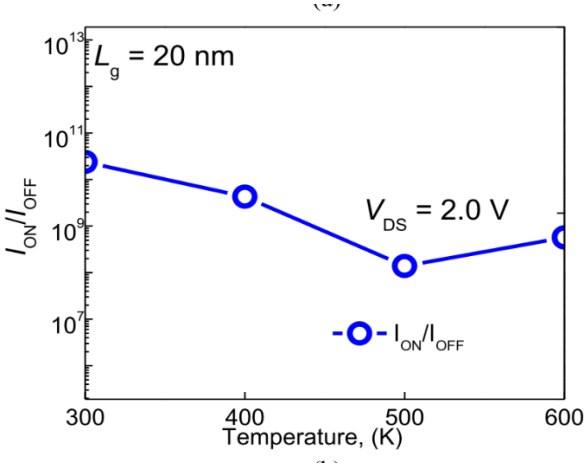
device

3.2 Impact of temperature in P+ SiC GAAJLFET

The drain current can vary from 300 K to 500 K depending on the temperature range in the P+ pocket SiC JLFET. The drain current is affected by the bandgap of the SiC JLFET, which is inversely proportional to the temperature. With rising temperature, there's a decrease in the bandgap and an increase in the drain current, considering the influence of the P+ pocket and its length on device performance. As illustrated in Figure 3.3, there are significant fluctuations in the OFF-state current as the temperature rises from T = 300 K to 600 K. These fluctuations are mainly due to the variation in mobility in even for low supply voltage. It can be seen that when V_{gd}= -0.5 V, the OFF-state current varies drastically, which shows the presence of surface scattering and acoustic scattering in P+ pocket SiC JLFET. This scattering is caused by the energy level transition of the electrons in the conduction band. As the temperature increases, the number of energy levels increases, which leads to higher scattering and more fluctuations in the OFF-state current. However, the increase temperature mobility of charge carriers decreases, which causes the increase in leakage current. In contrast, P+ pockets on the source and drain sides of the channel significantly reduce the OFF-state current by raising the potential barrier height. This barrier height is higher in the P+ regions, which makes it more difficult for the electrons to flow through the channel. As a result, the OFF-state current is lower, leading to a decrease in power losses.



(a)



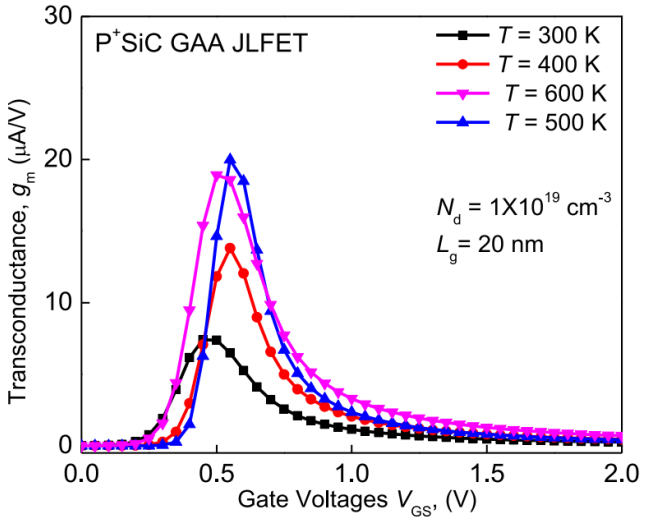
(b)

Fig. 3.3. (a) I_{ds}–V_{gs} transfer characteristics at V_{ds}=1.0 V with variation temperature (b) I_{ON}/I_{OFF} ratio at T= 300K, T= 400K, T = 500K and T = 600K for P^+ pocket SiC GAA JLFET.

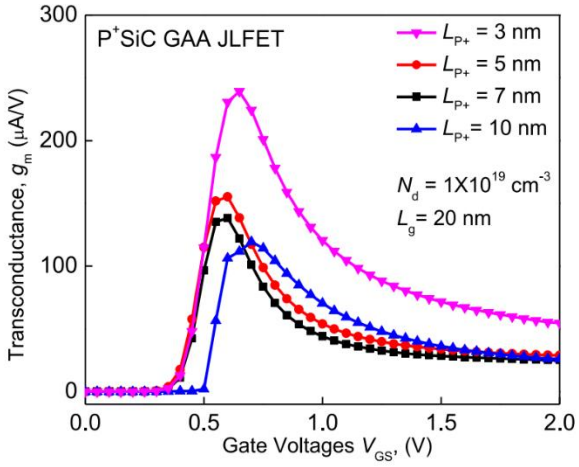
3.3 Impact of temperature and pocket length on the analog performance of the P+ SiC GAA JLFET

The transconductance of P+ SiC GAA JLFET varies with temperature as a function of gate supply voltage VGS. The variation is more pronounced at higher gate voltages. This can be attributed to the interaction between the

carriers and the electric field generated at the gate. The effect of temperature on the transconductance is also more pronounced at higher gate voltages. It can be seen in Figure 3.4(a) that the P+ SiC GAA JLFET shows the improved performance at low temperature. This is due to the increased mobility of the carriers and the lower resistance of the channel. At higher temperatures, the mobility of the carriers decreases and the resistance of the channel increases, resulting in lower transconductance. Similarly, Figure 3.4(b) the variation of transconductance with Pocket length with gate supply voltage. If the pocket length is short, the transconductance is high. If the pocket length is long, the transconductance is low. The transconductance is thus an important parameter in determining the performance of a transistor. The transconductance is a measure of how efficiently a transistor can amplify a small input signal. It is therefore an important factor to consider when designing a transistor circuit.



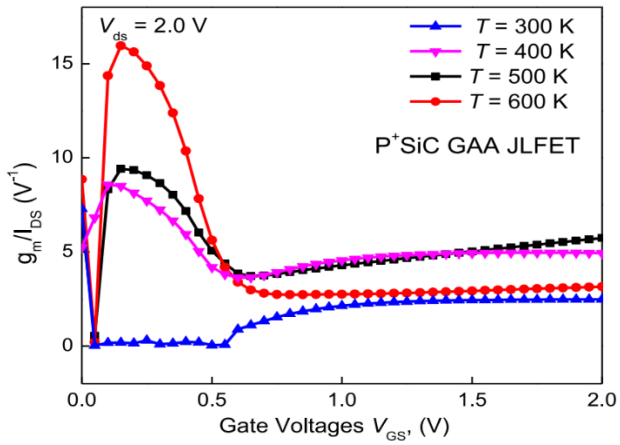
(a)



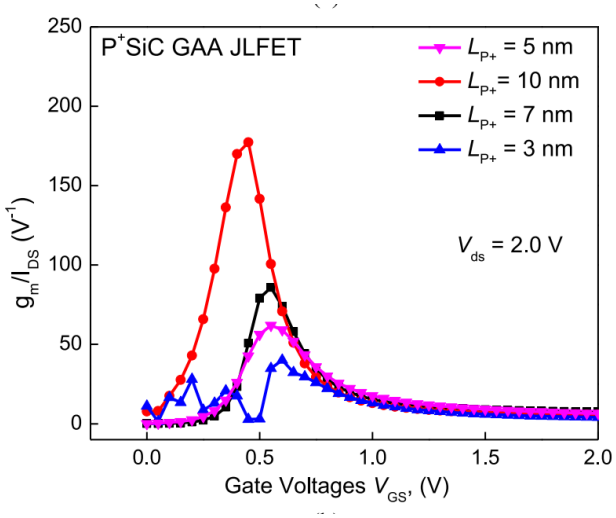
(b)

Fig. 3.4. Transconductance variation with (a) temperature and (b) Pocket length L_P of P+ SiC GAA JLFET

In the Figure 3.5(a) with temperature variation, the transconductance (gm) to drain (I_{DS}) current ratio is plotted in relation to gate voltage (V_{GS}). It can be seen from plot that as the temperature rises the g_m/ I_{DS} can yield higher. This means that transistors with higher g_m/ I_{DS} ratio can withstand higher temperatures and operate more efficiently. The gm/ I_{DS} ratio is a key factor in determining the performance of a transistor. Therefore, optimizing the gm/ I_{DS} ratio is essential for efficient operation. However, in Figure 3.5(b), g_m/ I_{DS} shows the variation with length of P+ Pocket. It can be seen that with variation of P+ pocket the g_m/ I_{DS} ratio increases with increase in supply gate voltage in P+ SiC GAA JLFET. This behavior is due to the increase in the gate oxide capacitance of the JLFET with increase in P+ pocket length. As the supply gate voltage increases, the g_m/ I_{DS} ratio also increases. This is due to the increase in the effective channel length of the JLFET. As a result, the JLFET can operate at higher supply voltages and provide better performance. Additionally, the g_m/ I_{DS} ratio is a measure of the effectiveness of the JLFET and it can be used to measure its performance



(a)

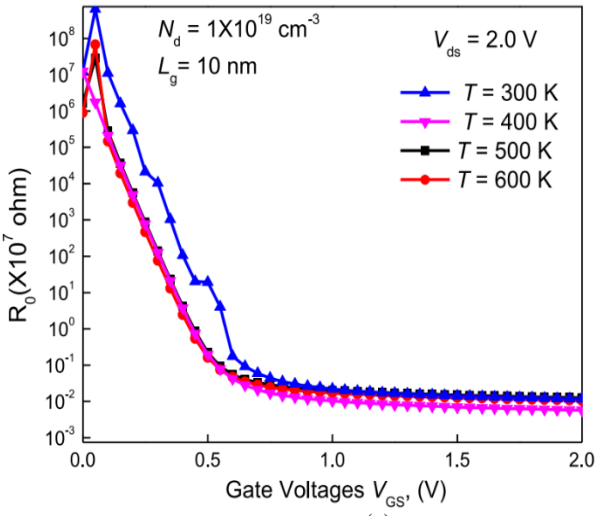


(b)

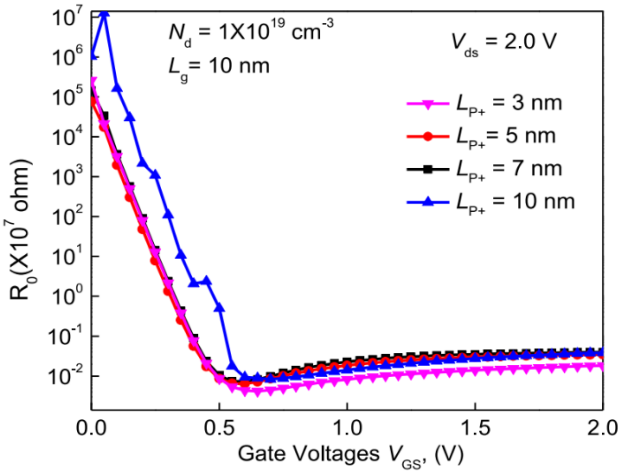
Fig. 3.5. gm/IDS ratio for P+ SiC JLFET with (a)variation of Temperature (b)variation of pocket length.

Figure 3.6 (a). Shows the variation in output resistance R0 with variation of temperature as function of gate supply voltage. Evident that the output resistance decrease as the temperature increases for P+ SiC GAA JLFET. This is due to the thermal activation of the carriers in the channel, resulting in more electrons available for conduction. This phenomenon is known as temperature-dependent saturation current and is observed in all types of

semiconductor devices. The temperature-dependent saturation current is an important factor to consider when designing SiC GAA JLFETs for applications in extreme environments. It is essential to analyze the impact of temperature variations on the device performance. However, in Figure 3.6(b), the output resistance varies with length of P+ pocket. As the P+ pocket length increases the output resistance increases in SiC GAA JLFET. This is because the increased length of the P+ pocket means more charge carriers are able to be stored in the channel region, and thus an increase in output resistance. This increased output resistance is beneficial in practical applications, as it helps to reduce the current leakage.



(a)



(b)

Fig. 3.6 Variation of Ro with (a) change in temperature (b) with change in pocket length for P+ SiC JLFET

In Figure. 3.7. The intrinsic gain has been shown with respect to gate voltage and variation of the temperature. Intrinsic gain declines with rise in temperature in P+ SiC JLFET. This decrease in intrinsic gain can be attributed to the increase in the mobility of the carriers at high temperatures. This decrease in intrinsic gain can be mitigated by increasing the threshold voltage and by reducing the gate oxide thickness. Finally, the use of certain materials with better thermal properties can also be helpful in reducing the intrinsic gain at high temperatures.

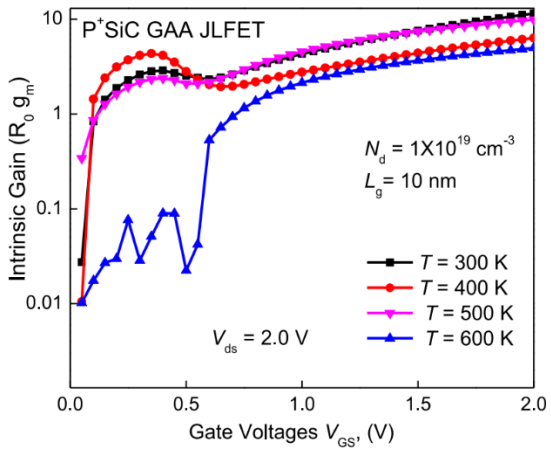


Fig. 3.7. Variation of Intrinsic gain with change in temperature for P+ SiC JLFET

Figure.3.8 shows the drain current with variation of p+ pocket. It can be depicted from the figure that increase in pocket length decrease the OFF-state current. The ON-state current also increases with longer pocket length. This is because the electric field strength is stronger for longer pockets, allowing for higher current. Additionally, the OFF-state current decreases for longer pockets, as there is less space for electrons to move.

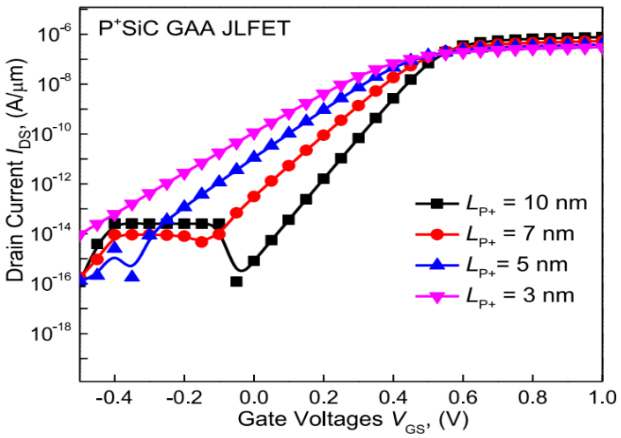


Fig. 3.8 Drain voltage variation of P + SiC GAA NW JLFET for different pocket lengths

3.4 Summary

The main focus is to develop a temperature-dependent compact model for the drain current and electric field of SiC GAA JLFETs that takes into account the P+ pocket. The proposed model is validated against existing experimental results and found to be in good agreement. The model can be used to predict the drain current and electric field of SiC GAA JLFETs over a wide range of temperatures. Furthermore, it can be used to optimize the design and performance of SiC GAA JLFETs. This chapter discusses the analog performance of the proposed device as a function of the temperature and the length of the P+ pocket. As a result of fully efficient volume depletion occurring even beyond the gate edges of the SiC GAA JLFETs with P+ pockets and into the source and drain regions, the OFF-state current has been significantly reduced. Consequently, The usage WBG material SiC tends to increase breakdown voltage even at higher temperature of JLFET. The ON-state current has also been improved due to the increased channel mobility of SiC. This improvement is due to the reduced channel resistance of SiC, which reduces the gate charge of the transistor. The ON-state current also increases as the P+ pocket is lengthened. This makes the SiC GAA JLFET with the P+ pocket a potential candidate for further scaling as well as for high temperature applications, which are increasingly important as IOT applications grow at a rapid pace today.

CHAPTER 4

Numerical Simulations and Electrical Characterization of P+ Pocket SiC GAA JLFET

Introduction

The need for low-power Very Large-Scale Integration (VLSI) devices has greatly increased as a result of the recent development in the digital industry. [25]. Further down scaling of these traditional MOSFETs can result in decreased performance and reliability [26]. To address this limitation, extensive research has been conducted, leading to the proposition of different non-planar transistor architectures like Multi-Gate Field-Effect Transistors [27], Gate-All-Around Field-Effect Transistors for applications in sub 20 nm regime [28]. Traditional approach of creating abrupt source, drain metallurgical junctions had introduced complexities in fabrication, particularly when doping the source, drain regions, thereby hindering scaling of devices [29]. As a solution to these challenges, junction less transistors (JLTs) have been proposed. They offer enhanced immunity to SCEs making them more suitable for IoT applications [30].

Achieving full channel depletion need complete volume depletion in Junction less Field-Effect Transistors (JLFETs). Therefore, various structural configurations for JL- FETs are explored in the literature [31]. To maintain full depletion channel in the sub-20 nm regime, it necessitates having an ultrathin channel and a high gate metal work function (approximately 5.5 eV) [32]. Because of reduction in channel length and thickness below 10nm regime causes triggering lateral band-to-band tunneling (L-BTBT) prematurely [31]. Occurrence of L BTBT in the channel region primes to an increase in OFF-state

current of the device, particularly at low Vds values [32]-[35].

In the recent years, the CMOS semiconductor industry exploit the wide band gap (WBG) semiconductor which include Silicon carbide (SiC) with band gap E_g = 3.3 eV, gallium Nitride (GaN) with band gap E_g = 3.4eV and β-Ga_2O_3 with band gap 5.4 eV has received much attention to achieve high break down voltage and high frequency operation [33]-[35]. A SiC JLTs have improved break down voltage as compared to silicon JLTs due to wide bandgap, which impeded the triggering of L-BTBT in channel. In addition, the use of SiC JLTs supress effect of interface trap charges which leads to avoid the need of counter doping and annealing process [36].

At elevated temperatures, particularly exceeding 400-425 K, traditional silicon devices often fail to operate at their optimal performance levels. However, Wide Bandgap (WBG) semiconductors like Silicon Carbide (SiC) exhibit a much lower intrinsic carrier concentration (ni = NcNv). This characteristic serves as a safeguard for Junction less Field-Effect Transistors (JLTs), protecting them from thermal damage even in high-temperature environments.

The electrical properties of 4H-SiC further enhance its suitability for high-temperature applications. It boasts a higher thermal conductivity of approximately 4-4.5W/cm K, electric field strength of 3.5 MV/cm, and saturation velocity of 2×107 cm/s [37]-[40]. These characteristics result in a high ON current and an impressive ION/IOFF ratio, which helps minimize the impact of heat generation and reduces energy loss [41]. Recently, a planar junction less FETs with 4H-SiC has been investigated in which high voltage characteristics significantly improved which reduce the L-BTBT [42]. A SiC JLFETs has used the P^+ pockets which results in complete volume depletion of SiC channel below 10 nm regime. P^+ pockets are placed at source and drain side of planar JLFET which impeded the formation of BJT in channel region. In the OFF-state when higher drain voltage is applied (V_{ds}), tunneling width at

interface of channel-drain becomes larger due to presence of P+ which reduced flow of electrons in lateral direction of channel [43]-[45]. Furthermore, 4H-SiC with a gate all around junction less FET (GAA JLFET) has been thoroughly investigated using negative capacitance including quantum confinement effects [46].

This chapter introduces a “GAA JLFET” employing 4H-SiC as the nanowire material, with P+ pockets located at source and drain side regions. The inclusion of P+ regions at the source-channel and channel-drain interface serves the purpose of achieving full depletion in the channel during the OFF-state. However, the existence of P+ regions in the source and drain sides tends to limit the ON-state current. To address these limitations and improve the Ion/Ioff ratio, the gate electrode's work function has been adjusted from 4.2 to 5.1 eV. This modification enables the device to function as a multiple threshold voltage device.

One of the notable features of this device is its reliance on 4H-SiC, a Wide Bandgap (WBG) semiconductor that allows it to operate effectively spanning a broad temperature range, often between 450 and 500 K. In order to evaluate the influence of temperature, an analytical model for the P+ pocket SiC GAA JLFET has been developed. In this mathematical model, the presence of the P+ pocket on both source and drain sides are taken into account, and model examines its influence on various aspects, including potential distribution in the channel, electric field characteristics, threshold voltage, DIBL, GIDL, and threshold voltage roll-off.

TABLE 4.1

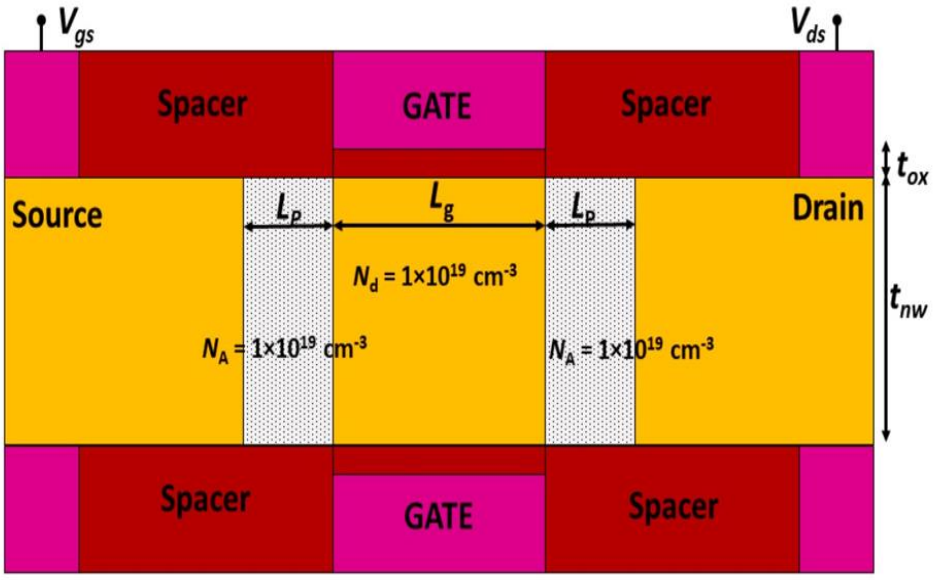
SIMULATION PARAMETERS USED FOR DEVICE

Parameters	Proposed Device
Nanowire Diameter (t)	5-10 nm
Oxide width (t_{ox})	1-3 nm
Doping Concentration (N_d)	1×10^{19} cm^{-3}
P+ Pocket Concentration (N_A)	1×10^{19} cm^{-3}
P+ Pocket Length (L_P)	3-10 nm
Gate metal (ϕ_m)	4.7 eV -5.1 eV
Channel length (L_g)	20 nm
Spacer Length (L_S)	20nm
Semiconductor Material	4H-SiC
Dielectric	HfO2

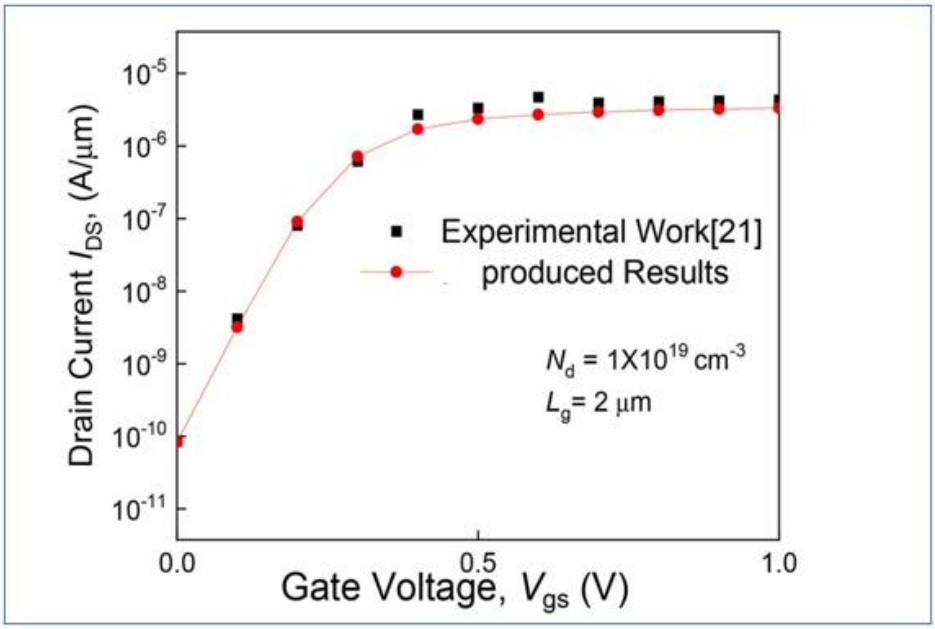
4.1 Device Parameters and Structure

Figure 4.1 depicts a schematic view of P^+ pocket SiC GAA JLFET has been shown. All device simulation parameters are enumerated in Table 4.1. SILVACO TCAD is used to carry out all device simulations. The carrier mobility degradation has been captured by models remote Column scattering, surface roughness scattering and remote phonon scattering are being used in simulation. As the L-BTBT comes into picture while scaling of device below 20 nm regime, nonlocal BTBT models has been incorporated. The Shockley-Read-Hall model is used for recombination effect in nanowire. As we use 4H-

SiC semiconductor material, velocity saturation model has been used with velocity 2×10^{7} cm^{-3}. The channel length in proposed device varies from L_g = 5–20 nm, therefore, in the sub-nanometer domain, it becomes imperative to integrate quantum effects into the simulation to ensure precise results. The Bohm quantum potential (BPQ) model is used to capture the impact of quantum effects in P^{+} pocket SiC GAA JLFET. The BQP model is independent of hydrodynamic model and drift-diffusion model have better convergence than density gradient model. The semiconductor-oxide interface trap charges are demonstrated utilizing Fixed trap charges (1.5×10^{13} cm^{-3}) and accepter traps densities (2×10^{13} cm^{-3}) at SiC-HfO_2 interface [47]-[48]. The gate electrode work function used to fully deplete the channel ranges from 4.7 eV to 5.1 eV to enhance the I_{ON}/I_{OFF} ratio with V_{gs} = 1.0 V, V_{ds} = 1.0 V. Use of P^{+} pocket on source and drain side doped with $N_A = 1\times10^{19}$ cm^{-3} and the whole SiC GAA have consistent doping profile of $N_d = 1\times10^{19}$ cm^{-3}. To realize nanowire, it is essential to use the high-k gate side wall spacers to obtain high ON state current as displayed in Figure 4.1. Gate oxide used in SiC GAA JLFET is HfO_2 with thickness t_{ox} = 1 nm to enhance the electrical characteristics of the device. In Figure 4.2 (a), displays the Ids-Vds characteristics of the P+ pocket SiC GAA JLFET and it is clear from the plot that SiC JLFET has much higher OFF-state current when related to GAA JLFET. In Figure 4.2(b), it is noticed that with the variation of drain voltages V_{ds}, the OFF-state current rises but much lower than that of GAA JLFET. In Figure 4.2 (c), the energy band diagram has been shown with variation of temperature T= 300K to T=500K. It is noticed that increase in temperature decreases tunneling width which induce the L-BTBT effect.

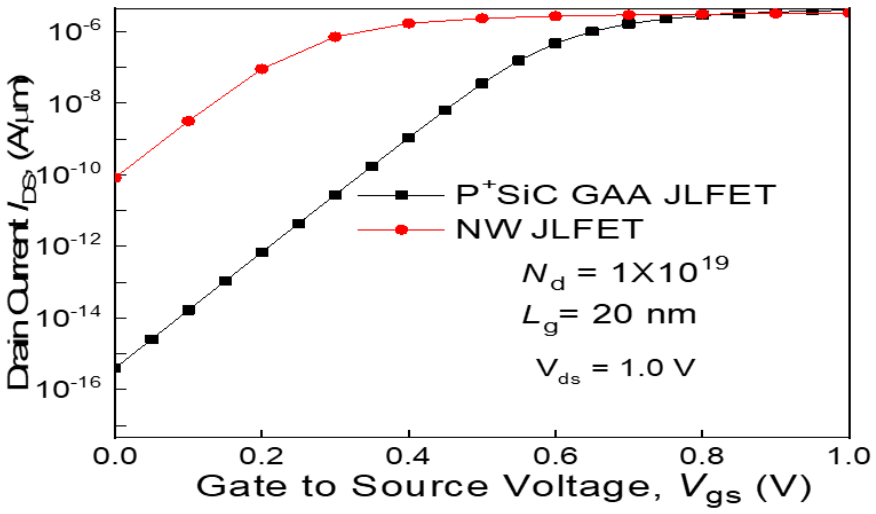

V_{gs}
V_{ds}
Spacer
GATE
Spacer
t_{ox}
Source
L_P
L_g
L_P
Drain
$N_d = 1\times10^{19}$ cm^{-3}
t_{nw}
$N_A = 1\times10^{19}$ cm^{-3}
$N_A = 1\times10^{19}$ cm^{-3}
Spacer
GATE
Spacer

(a)

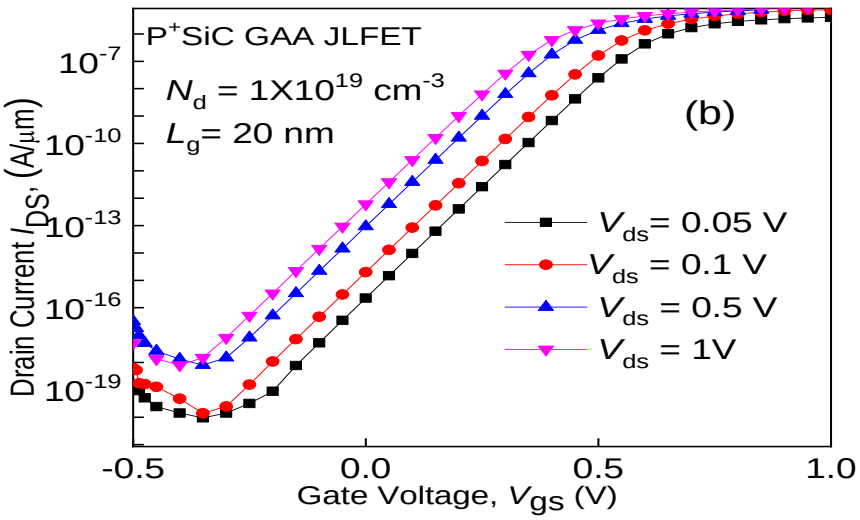

Drain Current I_{DS}, (A/μm)
10^{-5}
10^{-6}
10^{-7}
10^{-8}
10^{-9}
10^{-10}
10^{-11}
Experimental Work[21]
produced Results
$N_d = 1X10^{19}$ cm^{-3}
$L_g = 2$ μm
0.0
0.5
1.0
Gate Voltage, V_{gs} (V)

(b)

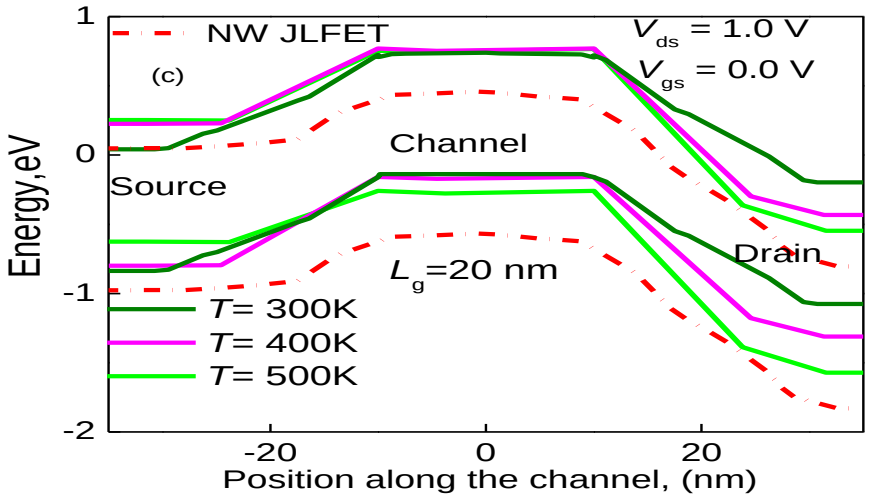
Fig. 4.1. (a) Schematic view of the P^+ SiC GAA JLFET and (b) Reproduction of results from TCAD [21].



(a)



(b)



(c)

Fig. 4.2. (a) I_{ds}–V_{gs} transfer characteristics at V_{ds}=1.0 V of P^+ pocket SiC GAA JLFET and (b) comparison of transfer characteristics at different V_{ds} (c) Energy band diagram of P^+ pocket SiC GAA JLFET and JLFET.

4.2 Model Description

4.2.1 Potential Distribution

The channel potential distribution of GAA JLFET has been solved through the Poisson's equation written as [49]

$$\frac{1}{r}\frac{\partial}{\partial r}\left[r\frac{\partial}{\partial r}\varphi_i(r,z,T)\right]+\frac{1}{r^2}\frac{\partial^2}{\partial r^2}\varphi_i(r,z,T)$$
$$+\frac{\partial^2}{\partial z^2}\varphi_i(r,z,T)=-q\frac{N_d}{\varepsilon_{si}}\left[e^{\left(\frac{\varphi_i(r,z,T)-V_{ch}}{V_T}\right)}-1\right] \qquad (1)$$

where i = 1, 2 for the source side P^+ pocket L_{PS} and drain side P^+ pocket L_{PD} regions, respectively. The electrostatic potential distribution in SiC channel is solving for φ_i (r, z,T) using V_{ch} and N_d are the quasi-fermi potential and uniform doping density in the channel region, respectively. ε_{si} and V_T is the dielectric of silicon and thermal voltage, respectively. To consider the impact of source side pocket and drain side pocket, the electrostatic potential calculated for L_{PS} and

L_g+L_{PD} respectively. Therefore, potential distribution can be calculated utilizing the superposition technique, in which the surface potential can be dissociated into two equations first one is 1-D Poisson's eqn $X_i(r, T)$ and second is 2-D Laplace's eqn $W_i(r, z, T)$ i.e.,

$$\varphi_i(r, z, T) = X_i(r, T) + W_i(r, z, T) \quad (2)$$

Therefore, Eq. (1) can be written as

$$\frac{\partial^2 X_i(r,T)}{\partial r^2} + \frac{1}{r}\frac{\partial X_i(r,T)}{\partial r} = -\psi \quad (3)$$

$$\frac{\partial^2 W_i(r,z,T)}{\partial r^2} + \frac{1}{r}\frac{\partial W_i(r,z,T)}{\partial r} + \frac{\partial^2 W_i(r,z,T)}{\partial z^2} = 0 \quad (4)$$

with $\psi = -q\frac{N_d}{\varepsilon_{si}}e^{\left(\frac{X_i - V_{ch}}{V_T}\right)-1}$

At the 4H-SiC-insulator interface the electric flux density is given by following equations [50]:

$$\varepsilon_{si}\frac{\partial \varphi_i(r,T)}{\partial r}|r = t_{NW} = C_{ox}\left[V_{gs} - V_{fb} - \varphi_i(t_{NW}, T)\right] \quad (5)$$

$$\varepsilon_{si}\frac{\partial \varphi_i(r,T)}{\partial r}|r = -t_{NW} = -C_{ox}\left[V_{gs} - V_{fb} - \varphi_i(t_{NW}, T)\right] \quad (6)$$

The capacitance C_{ox} is given by

$$C_{ox} = \frac{\varepsilon_{ox}}{r\, ln\left(1+\left(\frac{t_{ox}}{r}\right)\right)} \quad (7)$$

Using above boundary conditions and analytically apply Chambre's variable transformation, in which X_i (r = 0) = 0, equation has been (3) solved and given as

$$X_i(r,T) = V_{ch} + V_T\, ln\left(-\frac{8B}{\gamma(1+Br^2)^2}\right) \quad (8)$$

The *B* parameter used in equation (8) is defined in [51]. However, equation (8) has not provided definite solution particularly for surface potential distribution. Therefore, Lambert-*W* function is used to calculate an approximate solution of X_i as used in [52]-[54], and expressed as follows:

$$X_i(r,T) = V_{\mathrm{gs}} - V_{\mathrm{fb}} + C_R + V_{\mathrm{T}} - 2V_{\mathrm{T}}\mathrm{L}\left(\frac{C_R r\sqrt{2qN_{\mathrm{d}}/\varepsilon_{\mathrm{si}}V_{\mathrm{T}}}}{4V_{\mathrm{T}}}\times \mathrm{e}^{\left(\frac{V_{\mathrm{gs}}-V_{\mathrm{fb}}+C_R-V_{ch}}{2V_{\mathrm{T}}}\right)}\right) \tag{9}$$

Where $C_R = 4\varepsilon_{\mathrm{si}}V_{\mathrm{T}}/rC_{\mathrm{ox}}$

Further, the 2-D Laplace equation (4) has been solved using Fourier-Bessel series because the parabolic approximation has limitation and cannot solve the equation for potential across the center and surface. Hence, the resolved solution can be formulated as:

$$W_i(r,z,T) = \sum_{n=1}^{\infty} J_0(\lambda_n r)\left[A_n \exp(\lambda_n z) + B_n \exp(-\lambda_n z)\right] \tag{10}$$

A_n and B_n are Fourier coefficient which can be obtained by boundary conditions. The following equation gives the eigen values λ_n

$$J_1(t_{\mathrm{nt}}/\lambda_n) = C_{\mathrm{ox}}/\lambda_n \times J_0(t_{\mathrm{nt}}/\lambda_n) \tag{11}$$

The resultant solution for equation (1) is given by substituting (9) and (10) in (2)

$$\varphi(r,z,T) = V_{gs} - V_{fb} + C_R + V_T - 2V_T \mathrm{L}\left(\frac{C_R r\sqrt{2qN_d/\varepsilon_{si}\,V_T}}{4V_T} \times \mathrm{e}^{\left(\frac{V_{gs}-V_{fb}+C_R-V_{ch}}{2V_T}\right)} \right) + \sum_{n=1}^{\infty} J_0(\lambda_n r)\left[A_n \exp(\lambda_n z) + B_n \exp(-\lambda_n z)\right] \quad (12)$$

The electric field $E(r, z, T)$ in the 4H-SiC GAA channel is calculated by differentiating equation (12) with respect to lateral direction *i.e.* z. Therefore, electric field can be written

$$E_i(r,z,T) = -\frac{\partial \varphi_i(r,z,T)}{\partial z} \quad (13)$$

4.2.2 Surface Potential with consideration of P^+ pocket

To examine how the P+ pocket affects both the source and drain sides, we introduce the pocket lengths as LPS and LPD, respectively. The P+ pocket plays a crucial role in achieving full volume depletion in the SiC GAA channel, results in the extension of depletion region beyond the channel, as previously documented [55]-[57]. Because of this extended depletion region the presence of the P+ pocket stretches beyond gate length towards drain and source regions. This analysis assumes that the potential distribution in the channel region remains constant in the radial direction (independent of r) and varies solely in the lateral direction (z direction). Therefore, equation (1) becomes expressed as:

$$\frac{\partial^2}{\partial z^2}\varphi(r,z,T) = -\psi \quad (14)$$

In order to solve Poisson's equation, we integrate equation (14) with respect to z. We apply the conditions of an electric field of zero and a potential of Vbi at the length (-LPS). Therefore, the potential distribution in the source depletion

can be expressed as :

$$\varphi_1(r,z,T) = V_{\text{bi}}(T) - \psi(z + L_{PS})^2 \quad for - L_{PS} < z < 0 \qquad (15)$$

Similarly, at the drain side region the depletion length L_{PD}

$$\varphi_2(r,z,T) = V_{\text{bi}}(T) + V_{\text{ds}} - \psi(z - L_{PD})^2 \quad for\ L_{ch} + L_{PS} < z < L_{PD} \qquad (16)$$

Furthermore, the electric potential on the source side when z =0,

$$\varphi_1(r,z,T)\big|_{z=0} = \varphi_{\text{S}}(r,0,T) = V_{\text{bi}}(T) - \psi(L_{PS})^2 \qquad (17)$$

Similarly, at drain side when $z = L_{\text{g}} + L_{\text{PD}}$,

$$\varphi_2(r,z,T)\big|_{z=L_g+L_{PD}} = \varphi_{\text{i,D}}(r, L_g + L_{PD}, T) = V_{\text{bi}}(T) + V_{\text{ds}} - \psi(L_{PD})^2 \qquad (18)$$

The electric field due to introduction of P^+ Pocket at drain and source side can be calculated using equation (17) and (18) and expressed as:

$$\left.\frac{d\varphi_1(r,z,T)}{dz}\right|_{z=0} = \left.\frac{d\varphi_{\text{S}}(r,z,T)}{dz}\right|_{z=0} = -\psi L_{PS} \qquad (19)$$

$$\left.\frac{d\varphi_2(r,z,T)}{dz}\right|_{z=L_{ch}+L_{PD}} = \left.\frac{d\varphi_{\text{D}}(r,z,T)}{dz}\right|_{z=L_{ch}+L_{PD}} = \psi L_{PD} \qquad (20)$$

4.2.3 Minimum Surface Potential

Calculating the minimum surface potential is crucial, and it can be obtained by differentiating equation (12) at z = z_{min} to determine the minimum potential along the conduction path. This minimum potential is of utmost importance as it is instrumental in establishing the threshold voltage for the 4H-SiC GAA JLFET. Therefore, minimum surface potential can be calculated as

$$\varphi_{\min}(r,T) = \varphi(r,z,T)\Big|_{z=z_{\min}} = X(r,T) + W(r,z_{\min},T) \qquad (21)$$

where $z_{\min}$ is the lateral direction towards the channel.

Minimum surface potential can be written as

$$\frac{\partial\varphi(r,z_{\min},T)}{\partial z} = 0 \qquad (22)$$

Now, it is assumed that for practical devices $\lambda_n z \gg 1$ and

$$z_{\min} = \frac{1}{\lambda_n}\ln\sqrt{\frac{B_n}{A_n}} \qquad (23)$$

From (22) and (23), the minimum surface potential function can be expressed as

$$\varphi_{\min}(r,T) \approx X(r,T) + 2J_0(\lambda_n r)\sqrt{A_n B_n} \qquad (24)$$

4.2.4 Threshold Voltage Calculation V_{th}

The shift from full depletion mode to partial depletion mode happens when the gate voltage applied matches the voltage at which the channel starts conducting. This is the point at which the device switches from a state of complete depletion to a state where the channel allows partial conduction. [58]. Thus, one can write

$$\varphi_{s,\min}(r,T)\Big|_{V_{gs}=V_{th}} = V_F(r,T) \qquad (25)$$

Where $V_F(r,T)$ is fermi potential.

By solving equation (25), at $V_{gs} = V_{th}$, we get

$$p_1(V_{th} - D_n)^2 + p_2(V_{th} - D_n) + p_3 = 0 \qquad (26)$$

Equation (26) is solved to get the V_{th} which expressed as

$$V_{\text{th}} = D_n + \left(\frac{-p_2 + \sqrt{p_2^{\,2} - 4p_1p_3}}{2p_1} \right) \tag{27}$$

where,

$$p_1 = -\sinh^2\left(\lambda_n L_{\text{g}}\right) - 2\sinh\left(\lambda_n L_{\text{g}}\right) - 2 \tag{28}$$

$$p_2 = 2\left(2V_{\text{bi}} + V_{\text{ds}}\right)\sinh\left(\lambda_n L_{\text{g}}\right) + 4V_{\text{bi}} \tag{29}$$

$$p_3 = 2\left(V_{\text{bi}}^2 + V_{\text{bi}}V_{\text{ds}}\right)\sinh\left(\lambda_n L_{\text{g}}\right) - V_{\text{bi}} - \left(V_{\text{bi}} + V_{\text{ds}}\right)^2 \tag{30}$$

$$D_n = V_{\text{gs}} - V_{\text{fb}} + C_R + V_{\text{T}} - 2V_{\text{T}}\text{L}\left(\frac{C_R r\sqrt{2qN_{\text{d}}/\varepsilon_{\text{si}}\,V_{\text{T}}}}{4V_{\text{T}}} \times \text{e}^{\left(\frac{V_{\text{gs}} - V_{\text{fb}} + C_R - V_{ch}}{2V_{\text{T}}}\right)} \right) \tag{31}$$

4.2.5 Drain Induced Barrier lowering (DIBL)

The DIBL model describes how the drain voltage affects the change in threshold voltage when the supply voltage is zero. Thus, it is given by

$$\frac{\partial V_{\text{th}}}{\partial V_{\text{ds}}} = \frac{1}{2p_1}\left[\begin{array}{l} -2\sinh\left(\lambda_n L_{\text{g}}\right) + \dfrac{1}{\sqrt{p_2^{\,2} - 4p_1p_3}} \\ \times\left(2\left(p_2\right)'_{V_{\text{ds}}} - 4\left(p_1p_3\right)'_{V_{\text{ds}}} \right) \end{array} \right] \tag{32}$$

The parameters $\left(p_2\right)'_{V_{\text{ds}}}$ and $\left(p_1p_3\right)'_{V_{\text{ds}}}$ are the derivatives of p_2 and p_1, p_3 w.r.t V_{ds}, respectively are provided in Appendix B.

4.2.6 Gate Induced drain Leakage

The introduction of P^+ pocket on source-drain side region reduce the L-BTBT in SiC GAA JLFET, which significantly decreases the GIDL in device even at high temperatures [59]. The use of WBG material SiC, increases the tunneling

width which limits tunneling of electrons from channel conduction to drain valance band. The GIDL depends on the energy band gap and is given by

$$I_{\mathrm{GIDL}} = \frac{A}{B} E^2 \left(L_{\mathrm{g}}\right) \exp\left[-\frac{B}{E^2\left(L_{\mathrm{g}}\right)}\right] \tag{33}$$

A and B are temperature and energy band gap dependent parameters and are defined in [49], however, the electric field is denoted as E. The A and B constants are given as

$$A = \frac{q^2 m_r^{1/2}}{18\pi h^2 \left(E_g\left(T\right)\right)^{3/2}} \text{ and } B = \frac{\pi m_r^{1/2} \left(E_g\left(T\right)\right)^{3/2}}{2\sqrt{2} q h} \tag{34}$$

with $m_r = 0.2 m_0$ is the effective and m_0 is rest masses of electron. E_{g}, is the direct energy gap, h is Planck's constant and q is the electronic charge of silicon.

4.2.7 Threshold -Voltage Roll-Off

when device is scaled down in size, the channel length also undergoes scaling. A shortened channel length significantly influences the device's threshold voltage. The relationship below demonstrates how scaling the channel length affects the threshold voltage:

$$\frac{\partial V_{\mathrm{th}}}{\partial L_{\mathrm{g}}} = \frac{NM - QR}{N^2} \tag{35}$$

With

$$N = 2\sinh^2\left(\lambda_n L_{\mathrm{g}}\right) - 2\sinh\left(\lambda_n L_{\mathrm{g}}\right) - 2 \tag{36}$$

$$M = -\left(p_2\right)'_{L_{\mathrm{g}}} + \frac{1}{\sqrt{p_2{}^2 - 4p_1 p_3}}\left[2\left(p_2\right)'_{L_{\mathrm{g}}} - 4\left(p_1 p_3\right)'_{L_{\mathrm{g}}}\right] \tag{37}$$

$$Q = \sqrt{p_2{}^2 - 4p_1 p_3} \tag{38}$$

$$R = 4\left(p_1 p_3\right)'_{L_g} \quad (39)$$

The parameters $\left(p_2\right)'_{L_g}$ and $\left(p_1 p_3\right)'_{L_g}$ are the derivatives of p_2 and p_1p_3 with respect to L_g, respectively and are given in Appendix B.

4.3 Result and Discussion

4.3.1 Working of P^+ SiC GAA JLFET

Incorporating a P+ pocket in the source and drain regions of the SiC GAA JLFET significantly reduces the OFF-state current, even at higher temperatures such as 600 K. The utilization of SiC wide-bandgap (WBG) material enhances the breakdown voltage, especially when combined with the GAA JLFET structure. Adjusting the length of the P+ pocket on both the source and drain sides leads to a wider tunneling region at the interface between the channel and the drain. In the JLFET, achieving full volume depletion during the OFF-state is essential, and the P+ pocket accomplishes this by fully depleting the channel, even beyond the gate length.

During the OFF-state of the P+ pocket SiC GAA JLFET, the concentration of intrinsic charge carriers is low due to full volume depletion at the source-channel and drain-channel interfaces. In contrast, when the device is in the ON-state, the entire channel becomes N+ and exhibits a higher carrier concentration than the background concentration.

When Vds = 2 V, the P+ pocket on the source and drain regions depletes as a result of electron diffusion from the channel, effectively transforming the P+ pocket into an N-type region. Conversely, at Vds = 0.5 V, carrier transport occurs from the channel to the drain due to the presence of a sufficient electric field in the channel. Thus, P+ pocket plays a pivotal role in efficiently depleting the channel in the JLFET, especially when combined with an optimized gate electrode work function.

In Figure 4.3 (a)-(d), electron concentration contour plots are presented at various temperatures for the P+ pocket SiC GAA JLFET. These graphs clearly show that with rising temperature, both channel mobility and electron concentration in the channel increase, resulting in a higher OFF-state current for the proposed device. However, this increase is still lower than that observed in conventional JLFETs.

4.3.2 Surface Potential Distribution in P^+ SiC GAAJLFET

Figure 4.4 illustrates the variation of surface potential across a temperature range from T = 300 K to 500 K in the P+ pocket SiC JLFET. Equations (16), (21), and (22) provide smooth solutions that incorporate the influence of the P+ pocket and its length on the device's performance.

As indicated in Figure 4.3, both the source side and channel potential move dow ard as the temperature increases from T = 300 K to 600 K. This shift in surface potential distribution with increasing temperature primarily results from the prevalence of phonon scattering in the channel. It's worth noting that although higher temperatures tend to increase mobility of charge carriers, it also leads to an increase in leakage current.

However, the introduction of the P+ pocket on the source and drain sides of the channel serves to increase the potential barrier height, as evident from Figure 4.4. This barrier height enhancement is a noteworthy feature that can positively impact the device's overall performance.

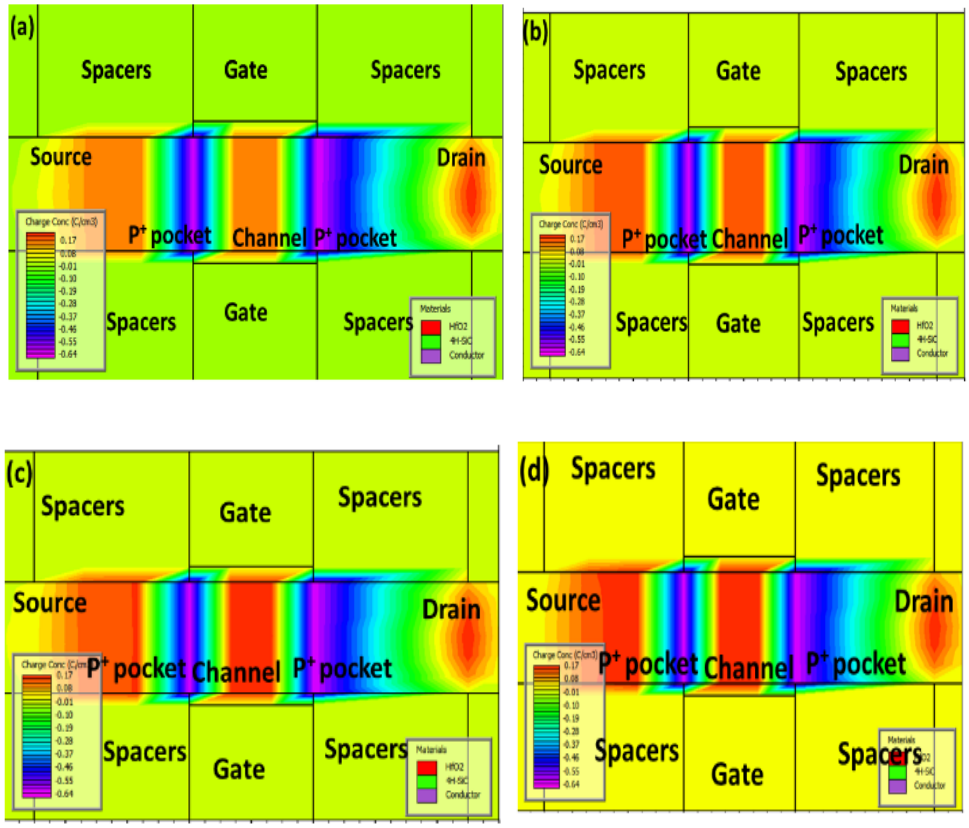


Fig. 4.3. Contour plot for electrons carrier concentration at (a) T= 300K, (b) T= 400K, (c) T = 500K, (d) T = 600K for P^+ pocket SiC GAA JLFET.

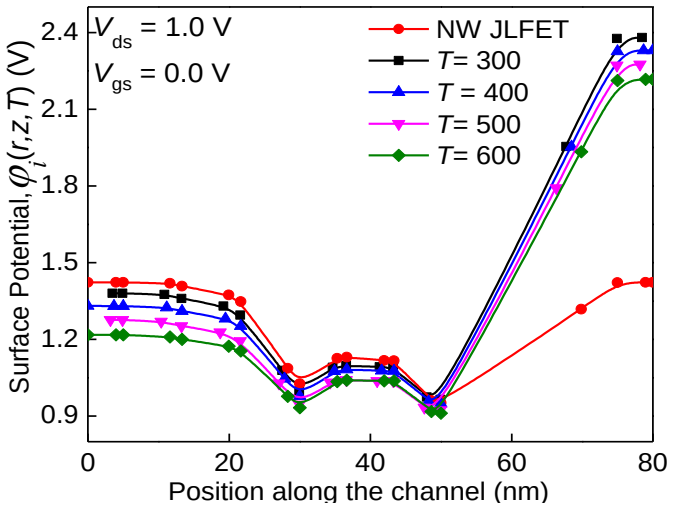


Fig. 4.4. Surface potential variation with temperature at P^+ Pocket Length L_{P+}

= 5 nm.

Figure 4.5 illustrates the change in surface potential as it relates to the position along the channel for various P+ pocket lengths, spanning from Lp+ = 3 nm to 10 nm. Adding the P+ pocket to the SiC GAA JLFET results in a prominent reduction in potential as the pocket length grows. As depicted in Figure 4.5, the potential at both the source and drain regions decreases due to the lower concentration of charge carriers at these points. This decline in potential leads to the depletion of charges at the source and drain side interfaces.

Moreover, Figure 4.6 illustrates how the surface potential changes with the doping profile of the P+ pocket at the source and drain sides. This figure suggests that when the doping profile in the P+ pocket increases at the source and drain sides of the SiC GAA JLFET, the potential at the interfaces decreases. This shift is mainly caused by the depletion of charge carriers within the P+ pocket, resulting in a dow ard movement of the Fermi potential. This depletion of charge carriers has a substantial impact on the threshold voltage and the OFF-state characteristics of the device.

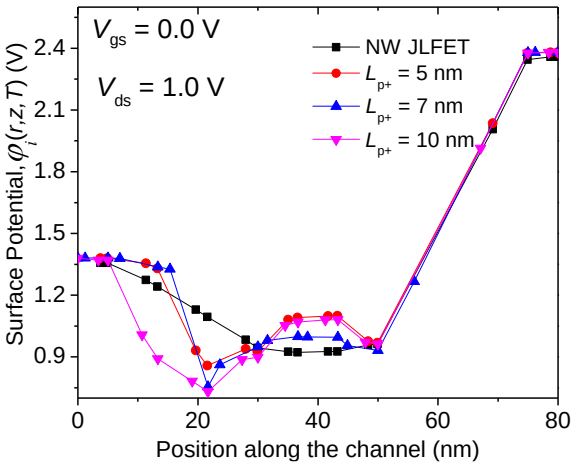


Fig. 4.5. Surface potential of P^+ pocket SiC GAA JLFET variation with P^+ Pocket Length L_P = 5 nm, 7nm, 10 nm.

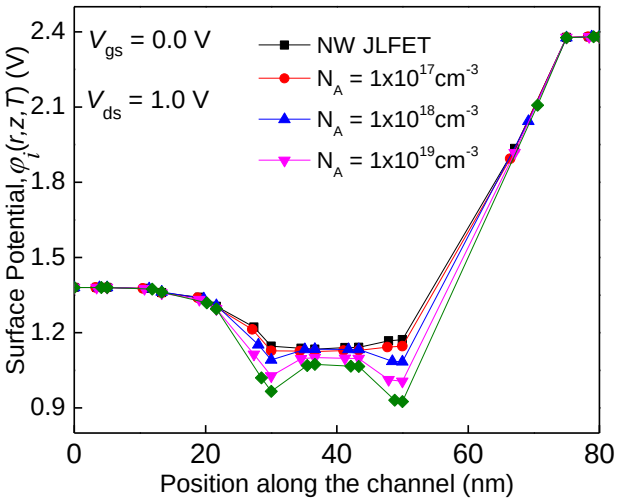


Fig. 4.6. Surface potential distribution of P^+ SiC GAA JLFET with variation of doping profile of Pocket length.

4.3.3 Electric Field Distribution (E_z) in SiC GAA JLFET with Temperature

In Figure 4.7, it's apparent that the P+ SiC GAA JLFET shows a reduced electric field when compared to the conventional JLFET. The existence of the P+ pocket causes depletion at the source-channel and channel-drain interfaces, and the channel undergoes depletion because of the gate metal's work function. Consequently, the overall electric field in the P+ pockets of the SiC GAA JLFET is reduced. On the other hand, the traditional nanowire does not achieve complete volume depletion of charge carriers in the channel.

The reduced electric field restricts the movement of charge carriers from the source region to the channel region and impedes the creation of a bipolar junction transistor (BJT) effect within the channel.

Figure 4.8 illustrates the behavior of the P+ pocket SiC GAA JLFET with temperature variations spanning from T = 300 K to 600 K. As the temperature rises from 300 K to 600 K, the intrinsic carrier concentration within the device also increases, leading to a higher recombination rate in the channel region. The

increased rate of recombination, as a result, raises the strength of the electric field at the source-channel junction and reduces the reduction of charge carriers. As a result, the higher electric field leads to a greater OFF-state current in the device

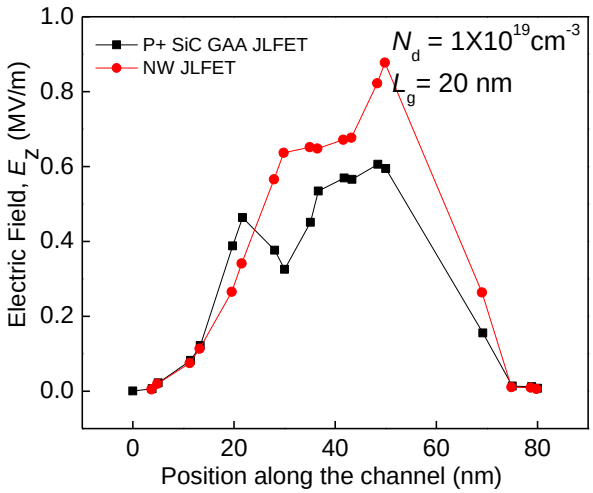


Fig. 4.7. Electric field of P^+ pocket SiC GAA JLFET and JLFET.

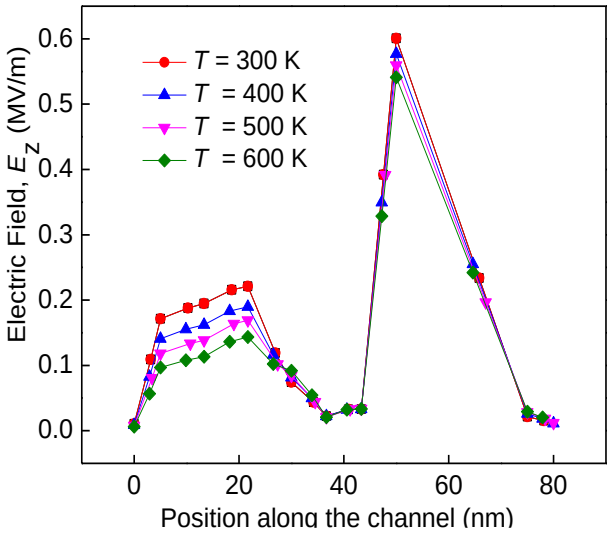


Fig. 4.8. Electric field variation of P^+ SiC GAA JLFET with variation of Temperature T=300 K to 600 K.

4.3.4 Threshold voltage (V_{th}) variation with Temperature (T)

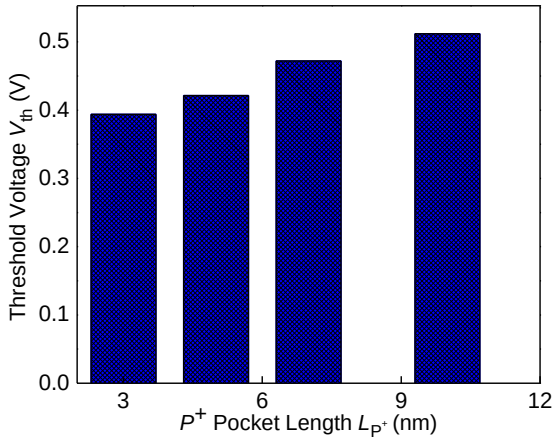


Fig. 4.9. Threshold voltage (V_{th}) variation of P^+ SiC GAA JLFET with variation of Pocket length L_P.

Figure 4.9. In relation to the P+ pocket length, which ranges from LP = 3 nm to 10 nm. The plot clearly shows that as the P+ pocket length increases, the threshold voltage also goes up.Increase in threshold voltage is attributed to full volume depletion that extends beyond the gate length. As the P+ pocket length grows, the channel's depletion region also expands toward the source and drain side regions. Consequently, the barrier height between the source and channel increases, necessitating a higher gate voltage to transition from partial depletion mode, in which current conduction initiates. As a result, this leads to a higher threshold voltage for the SiC GAA JLFET.

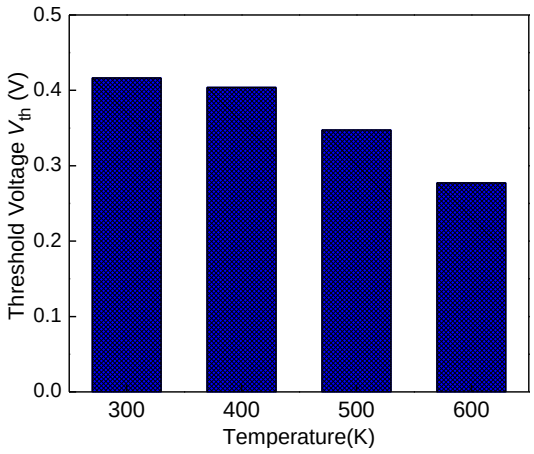


Fig. 4.10. Threshold voltage (V_{th}) variation of P^+ SiC JLFET with variation of Temperature T=300 K to 600 K.

In Figure 4.10, the graph displays the variations in threshold voltage across different temperature levels, ranging from T = 300 K to T = 600 K. The graph clearly indicates that as the temperature increases, the threshold voltage decreases.

When the device operates at 300 K, which is room temperature, it performs as anticipated. Nevertheless, as the temperature starts to climb, the natural concentration of charge carriers within the channel goes up. This heightened carrier concentration leads to more electrons available for recombination, which, in turn, boosts the rate of recombination within the channel.

Furthermore, with the rise in temperature, the height of the potential barrier between the source and the channel decreases. This decrease in barrier height also plays a role in lowering the threshold voltage. In essence, the threshold voltage goes down as the temperature increases, thanks to the combined impact of an increased carrier concentration and a diminished potential barrier height at the source-channel interface.

Figure 4.11 shows the changes in Drain-Induced Barrier Lowering (DIBL) as the temperature varies. Given that the scalability of a device

significantly impacts its performance in terms of DIBL, it's crucial to assess how temperature affects these aspects. The chart makes it clear that DIBL rises as the temperature goes up. This increase is primarily due to the drop in the barrier height at the channel-drain junction. Consequently, this reduction in potential at the drain side encourages electron tunneling from the channel's valence band to the drain's conduction band, resulting in increase of DIBL.

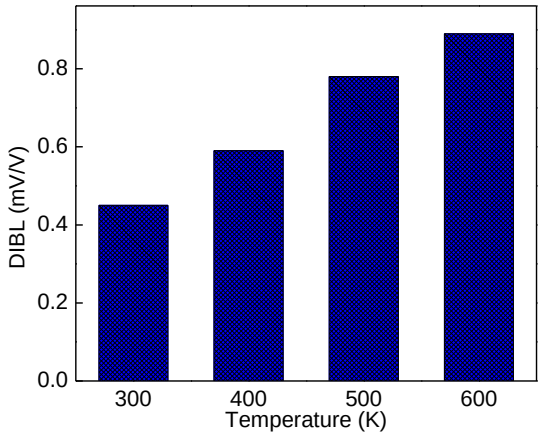


Fig. 4.11. DIBL variation of P^+ SiC GAA JLFET with variation of Temperature T=300 K to 600 K.

In addition to the impacts on DIBL and threshold voltage, mathematical equations have been developed to describe the threshold voltage roll-off and Gate-Induced Drain Leakage (GIDL) current at various temperatures. In Figure 4.12, it's clear that at different channel lengths, the threshold voltage decreases as the channel length is reduced from 20 nm to 5 nm as the temperature increases. Remarkably, the threshold voltage roll-off for SiC GAA JLFETs is less significant, and this can be attributed to the P+ pocket introduced at the source and drain sides. This feature effectively increases the tunneling width and potential barrier height at the source and drain side interfaces, thus reducing the threshold voltage roll-off.

Figure 4.13 displays the threshold voltage roll-off for the SiC GAA JLFET with varying pocket lengths. With an increase in pocket length, the threshold voltage roll-off diminishes. This is primarily because of the reduced intrinsic carrier concentration in the channel, which necessitates a higher gate voltage for minimal current conduction

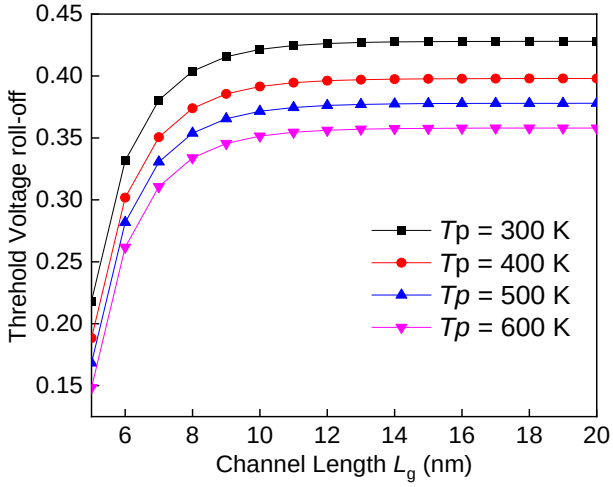


Fig. 4.12. Threshold voltage roll-off for P^+ SiC GAA JLFET with variation of Temperature T=300 K to 600 K.

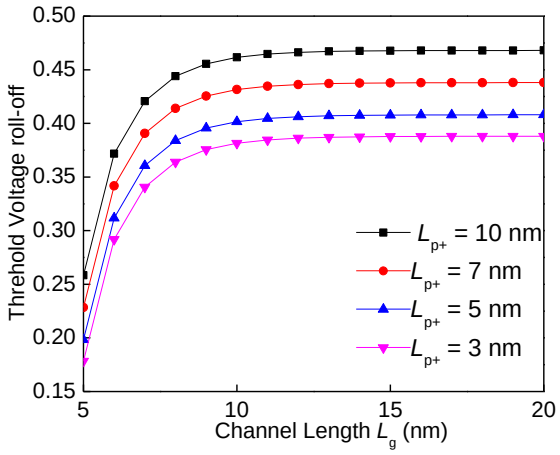


Fig. 4.13. Threshold voltage roll-off variation of P+ SiC GAA JLFET with variation of P^+ channel length.

In Figure 4.14, Gate-Induced Drain Leakage (GIDL) current is presented with variations in drain voltage for different P+ pocket lengths. It is evident from the plot that as the P+ pocket length increases, the GIDL current decreases. Incorporating the P+ pocket in the SiC GAA JLFET effectively results in complete depletion of the channel during the OFF-state.

As the P+ pocket length increases, the tunneling width on the drain side also increases. This impedes the onset of Low-Field Band-to-Band Tunneling (L-BTBT) at lower drain voltages. Furthermore, the utilization of SiC as a Wide-Gap (WGP) material contributes to a reduced occurrence of L-BTBT-induced GIDL. Reducing the P+ pocket length from 10 nm to 3 nm results in an approximately two-orders-of-magnitude increase in GIDL current, highlighting the significant influence of pocket length on the OFF-state current of the P+ SiC GAA JLFET.

Moreover, in Figure 4.15, the change in Gate-Induced Drain Leakage (GIDL) with temperature at various drain voltages is shown. With increasing temperature, the channel is no longer completely depleted and retains some intrinsic charge carriers, leading to L-BTBT (band-to-band tunneling) in the channel and a reduction in the tunneling width. As a result, the GIDL current rises with higher temperatures, and the OFF-state current also increases.

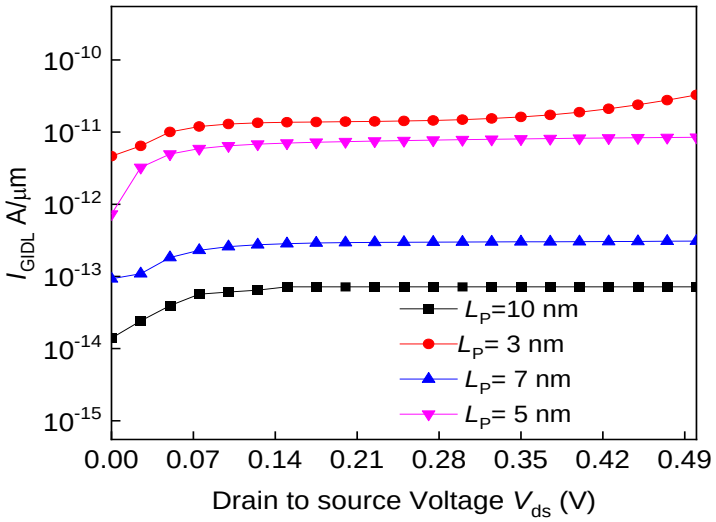


Fig. 4.14. GIDL variation of P^+ SiC GAA JLFET with variation of P^+ channel length.

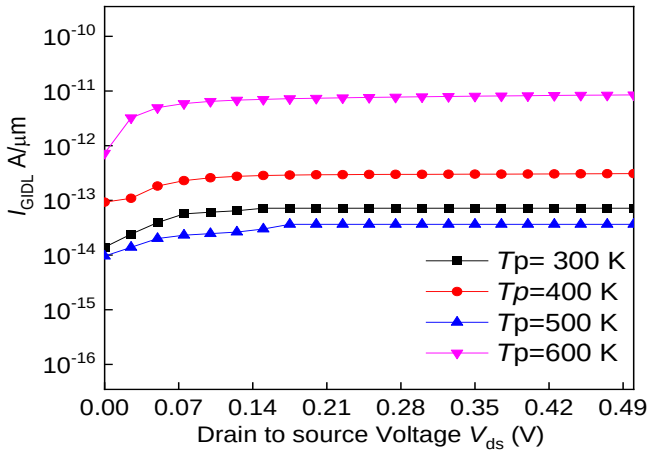


Fig. 4.15. GIDL variation of P^+ SiC GAA JLFET with variation of Temperature T=300 K to 600 K.

4.4 Summary

In this chapter, a model that considers temperature effects has been developed to analyze the electric field and potential, considering the presence of P+ pocket in the SiC GAA JLFET. This model significantly reduces the OFF-state current by achieving efficient depletion, which extends beyond the gate

edges towards the source and drain regions in the P+ pocket SiC GAA JLFET. This extension enhances the tunneling width at the channel-drain junction, restricting the movement of electrons from the channel's conduction band to the valence band on the drain side. The potential and electric field have been studied for various temperatures and various P+ pocket lengths.

Utilizing Wide-Bandgap (WBG) materials like SiC improves the breakdown voltage, even at high temperatures in the JLFET. The JLFET can be scaled down further, as the threshold voltage can be controlled by changing the P+ pocket length in the nanowire, and the threshold voltage roll-off is minimal. As a result, the P+ pocket SiC GAA JLFET stands out as a promising choice for further miniaturization and applications in high-temperature settings, rapidly growing Internet of Things (IoT) sector.

APPENDIX A

$$A_1 = \frac{(V_{bi}+V_{ds}-X(r))-(V_{bi}-X(r))\,exp\left(-\lambda_n\left(L_g+L_{PD}\right)\right)}{2\,sinh(\lambda_n\left(L_g+L_{PD}\right))J_0(\lambda_n r)} \quad \text{(A1)}$$

$$B_1 = \frac{V_{bi}-X(r)-A_1 J_0(\lambda_n r)}{J_0(\lambda_n r)} \quad \text{(A2)}$$

$$A_2 = -\frac{(V_{bi}+V_{ds}-X(r))-(V_{bi}-X(r))\,exp(-\lambda_n L_{PS})}{2\,sinh(\lambda_n L_{PS})J_0(\lambda_n r)} \quad \text{(A3)}$$

$$B_2 = A_1 - A_2\,exp(\lambda_n L_{PS}) + B_1\,exp(-\lambda_n L_{PS}) \quad \text{(A4)}$$

APPENDIX B

The values of p'_{2L} and $(p_{1L}p_{3L})'$ are given as

$$k'_{2L_g} = 2\,cosh\left(\lambda_n L_g\right)(2V_{bi} + V_{ds}) \quad \text{(B7)}$$

$$\left(p_{1L_g}p_{3L_g}\right)' = \begin{Bmatrix} 2\left(sinh^2\left(\lambda_n L_g\right) - 2\,sinh\left(\lambda_n L_g\right) - 2\right) \\ \left(\left(V_{bi}^2 + V_{bi}V_{ds}\right)cosh\left(\lambda_n L_g\right)\right) \end{Bmatrix}$$

$$+ \begin{Bmatrix} 4\left(\left(V_{bi}^2 + V_{bi}V_{ds}\right)sinh\left(\lambda_n L_g\right)\right) \\ \left(sinh\left(\lambda_n L_g\right) - 1\right)cosh\left(\lambda_n L_g\right) \end{Bmatrix} \qquad \text{(B8)}$$

$$p'_{2ds} = 2\,sinh\left(\lambda_n L_g\right) \qquad \text{(B9)}$$

$$\left(p_{1ds}p_{3ds}\right)' = \left\{2\left(V_{bi}\,sinh\left(\lambda_n L_g\right) - 2\left(V_{bi} + V_{ds}\right)\right)\right\} \qquad \text{(B10)}$$

CHAPTER 5

Analytical Modeling and Electrical Characterization of Multi-Gate FET

Introduction

In modern chip design, both low and high-voltage devices are often integrated onto a single chip to serve specific applications, where low-power circuits govern the switching of high-voltage circuits [60]. The reduction of channel length has become crucial for accommodating high-density circuits within a chip while mitigating the occurrence of short channel effects [64]. One approach to mitigate these effects involves the implementation of ultra-thin layers in multi-gate MOSFET structures. However, even with the utilization of ultra-thin channel layers, addressing short channel effects remains a significant concern [68]. Utilizing numerical device simulations, thin layers within the device can be meticulously designed [69]. This chapter focuses on modeling short channel effects using ultra-thin layers, overlapped contact regions, and constant potential distributions. The potential distribution is examined at various points including the drain, source, and center of the channel. Despite heavy doping in the source and drain regions, the device's performance remains largely unaffected, and an increase in current density may occur due to enhanced conductivity [70].

MOSFETs play a crucial role in applications requiring high voltage and power handling [72]. To meet these demands, MOSFETs have been fine-tuned to operate efficiently at high voltages, particularly at the drain contact boundary [77]. This high-voltage capability is achieved by increasing the drain contact length and reducing the doping concentration in the drain region, consequently raising the drain resistance. The present study is centered on modeling the short-channel effects and drain current of multi-gate (double-gate) MOSFETs tailored for high-voltage/power applications, focusing on the voltage ranges of 2 V to 3 V for high voltage and 1 V to 1.3 V for low voltage. Also, The device’s

performance is assessed using various gate and drain voltages. The drain resistance effect and short channel effects are also studied in the proposed model and can be valid for both high and low voltages. In the process of model development, the entire potential distribution within the device is considered, and this encompasses the influence of both drain and gate overlap length effects. The Multigate FET (DGMOSFET) has been put forward for high voltage and high-power applications aiming to reduce short channel effects and drain current through gate overlap. This proposed model addresses short-channel effects (SCEs) in thin-layered MOSFETs that feature substantial drain regions by including the influence of drain resistance in the device. As a result, the device's SCEs are reduced. The overlapping region of the gate contact plays a vital role in determining the operation of high-voltage FET. Multi-gate devices offer notable advantages in mitigating Short Channel Effects (SCE) and increasing on-state current, leading to faster circuit operation. The developed model can be employed to address size constraints in multi-gate FETs.

5.1 Device Structure

Figure 5.1 illustrates Multi-gate FET (double gate MOSFET) cross sectional view. The device structure is meticulously designed and comprehensively analyzed using a 2D numerical TCAD (Technology Computer-Aided Design) tool, which integrates device physics into the simulations.[78].

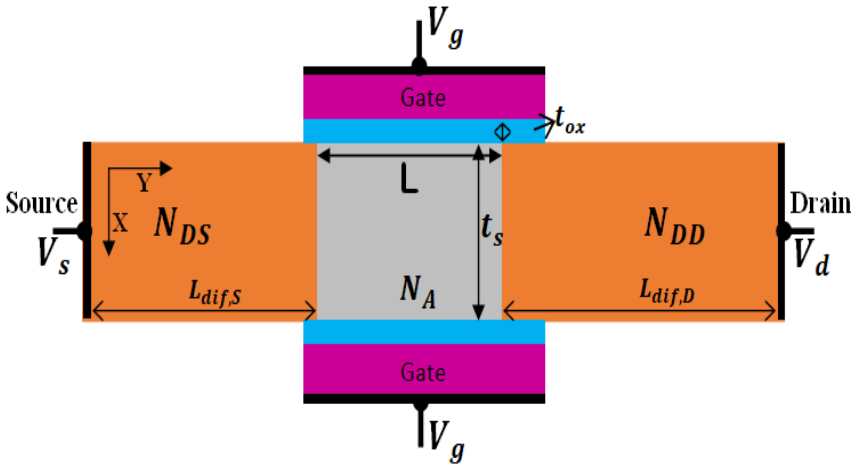


Fig.5.1: Schematic view of multi gate (double gate) MOSFET.

The double-gate (DG) MOSFET incorporates a sparsely doped lengthy drift region to ensure effective operation under specified high voltages. Simulation analysis at 300 K employs the drift-diffusion model, integrating the Poisson equation and carrier-continuity equation. This approximation facilitates the understanding of transitions under various bias conditions. To introduce the quantum confinement effect into the energy sub-bands in two dimensions, the diffusion and drift space mode method is utilized. Furthermore, model derivations make use of the Newton-Raphson method.

Meshing of the device structure should be meticulously selected using the Deck Build Editor to ensure precise simulation of all corners and intricacies of the proposed device, enhancing simulation efficiency. These numerical-based simulations leverage physical parameter models, including FLDMOB, CONMOB, and CVT (Fowler-Nordheim) to accurately represent the device's behavior. To consider the recombination of minority carriers, the SRH (Shockley-Read-Hall) and Auger recombination models have been included. Results generated by these models and methods are thoroughly analyzed, and the output data is extracted and visualized in the Tony-plot window for further examination and interpretation. The symbols, parameters, values employed in

the calculations, and the development of the model are listed in Table 5.1.

Table 5.1: The definitions along with the parameter values used in the calculation and model development of the proposed device structure.

Parameter	Definitions	Values
L	Channel Length	$25\ nm$
W	Channel width	$1\ \mu m$
N_A	Channelregion dopingconcentration	$10^{15}\ cm^{-3}$
N_{DS}	Sourceregiondoping concentration	$10^{20}\ cm^{-3}$
N_{DD}	Drainregiondoping concentration	$10^{19}\ cm^{-3}$
t_{ox}	Oxide equivalent thickness	$1.5\ nm$
t_s	Silicon material thickness	$10\ nm$
$L_{diff,d}$	Drain length	$75\ nm$
$L_{diff,s}$	Source length	$75\ nm$
L_{over}	Channeloverlap region length	$10\ nm$
DOS	Conductionband density of state	3.24e17 $m^{-2}V^{-1}$

μ_0	Low field mobility	$900\ cm^2.V^{-1}s^{-1}$
v_{sat}	Velocity Saturation	$1 \times 10^7\ cm/^{s}$

5.2 Model Development

5.2.1. Short Channel Effects

SCEs manifest when there is a significant current flow deep within the device. Current density of the channel and between two gate regions with V_{ds} = 50 mV and V_{gs} = −0.5 V is shown in Figure 5.2. The maximum current density is typically observed at the center of the channel.

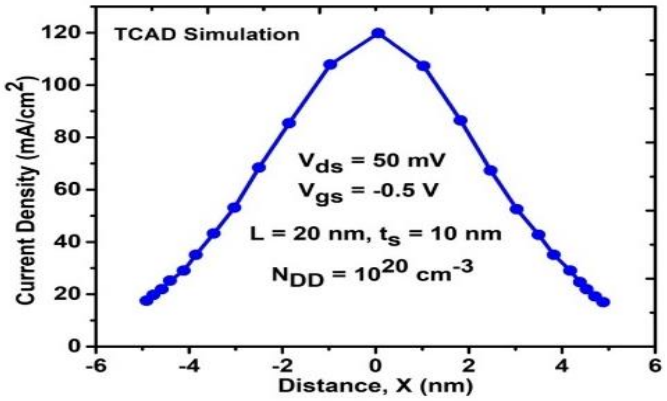


Fig. 5.2: Current density at the center of the channel.

The existence of an inversion layer at the interface between gate and the channel can cause a decline in the deep current flow, leading to an increase in Vgs (gate-source voltage). When modeling the effects of short-channel devices, the charge distribution within the channel region is considered and the movement of charges from the source-channel-drain junctions within the channel region along the y-direction, is typically represented by a cubic function [20].

$$\emptyset(y) = K_0 \cdot (y + K_1)^3 + K_2 \qquad (1)$$

The parameters K_0, K_1 and K_2 are the function of the charge present at source-

channel-drain junctions and other parameters used in model development are described in Table 5.2.

Table 5.2: The parameters and their expressions for model development

Parameter	Definitions	Expression
K_0	Channel potential gradient	$sign(y).\left(V_{bi,source} - \phi_{min}\right)/(L_0/2)^3$
K_1	Minimum charge present at a position along the y-direction	y_{min}
K_2	Minimum potential	ϕ_{min}
$V_{bi,source}$	Built-in-potential at channel-source interface	$\beta^{-1}.ln\left(\frac{N_{ds}.N_A}{{n_i}^2}\right)$
$V_{bi,drain}$	Built-in-potential at channel-drain interface	$\beta^{-1}.ln\left(\frac{N_{dd}.N_A}{{n_i}^2}\right)$
E_{source}	Maximum electric field present at channel-source	$\frac{\left(V_{bi,source} + V_s - \phi_{min}\right)}{XJ_0}$

	interface	
E_{drain}	Maximum electric field present at channel-drain interface	$\frac{(V_{bi,drain} + V_s - \phi_{min})}{XJ_0}$
XJ_0	Scaling parameter for length	$\sqrt{(\varepsilon_s t_s t_{ox}/2\varepsilon_{ox})(1 + \varepsilon_s t_s/4t_{ox})}$

The potential gradient K_0 is determined by solving Poisson's equation for proposed structure [80]. Minimum potential K_1 allows the maximum drain current along the y direction at a subthreshold state when $y_{min} = K_1$. The potential distribution at channel, drain, and source junctions would overlap by decreasing the length of the channel, and its consequences would be the increase of minimum potential ($K_2 = \phi_{min}$), as shown in Figure 5.3.

The ϕ_{min} will increase along with the long channel structure, and it is denoted as [79]

$$\Delta\emptyset_{min}(V_{gs}, V_{ds}, L) = -2A_0\left(Y_{min} - \frac{L_0 - L}{2}\right)^3 \quad (2)$$

Here, Y_{min} is denoted as minimum potential position along the direction of the channel, which is determined from the potential fields originating at the channel-source, channel-drain junctions and is written as

$$y_{min} = -V_{di}/E_{source} + E_{Drain} \quad (3)$$

V_{di} is potential difference at source channel drain junction edges.

E_{drain} and E_{source} are the electric fields originating at drain and source junction

regions which are determined from the doping concentrations at the respective junction. The lateral distribution of potential influencing the device characteristics is modelled by considering the change in ϕ_{min} [81] as

$$V'_G = V_{gs} - V_{FB} + \Delta\emptyset_{min} \quad (4)$$

Here, V'_G is utilized to determine surface potential (ϕ_S) at channel to gate interface, determined by Gauss law and the self-consistent solution of Poisson's equation is expressed as follows

$$\emptyset_S(y) = V'_G + \frac{Q_{si}(y)}{C_{ox}} \quad (5)$$

Here, Q_{si} is charge present in channel, C_{ox} is gate oxide capacitance. The function $\emptyset_S(y)$ is iteratively solved by the Newton-Raphson method, which includes analytical initial accurate value to improve the speed of calculations. Drain and source side channel regions are solved in place of the complete channel's Poisson equation solution by taking quasi-Fermi distribution in the channel region with approximations of drift-diffusion.

Gate capacitance characteristics concerning the applied gate voltage are examined to assess the impact of short-channel device effects.

The SCE exerts its influence on parameters like threshold voltage roll-off, threshold voltage reduction, and subthreshold swing. These effects are graphically depicted in Figure 5.6, where a higher drain-side doping of $10^{20}cm^{-3}$ is considered. From these results, it is observed that the reduction of short-channel effects is improved.

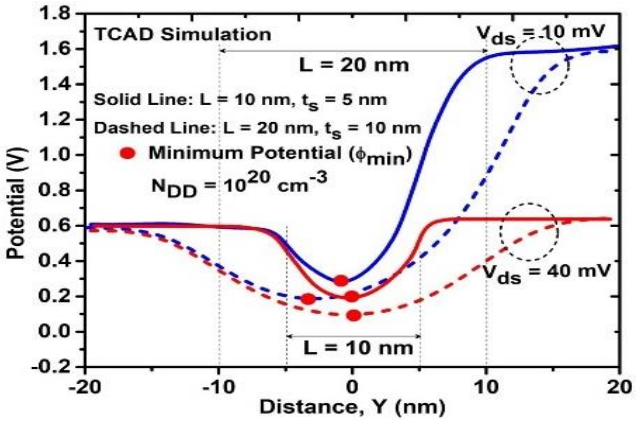


Fig. 5.3: Simulation results for potential distribution at center of the channel for different channel lengths and thicknesses at V_{ds} = 10 mV and 40 mV.

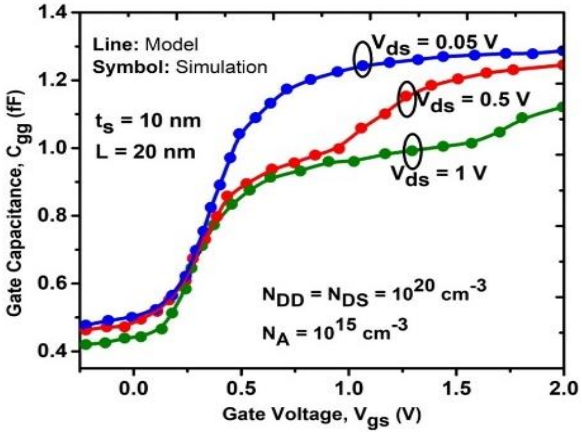


Fig. 5.4: Characteristics of gate capacitance in respect of applied gate voltage for applied drain voltages with L=20 nm and t_s=10 nm.

5.3 Effect of depletion region and drain resistance

Two effects arise when low doping is applied at the drain region are: 1) Extension of depletion region through operation of short channel device's sub-threshold swing 2) The effect of drain side resistance region through applied high drain and gate voltages. These two effects are included to the development of DG-MOSFET [82]. The effect of drain region resistance increases due to the

distribution of potential expansion into the deep drain region with low doping concentration [77]. The gate region expands in the direction of the drain side near the gate edge, influenced by the drift region and the current flow within the channel. The potential generated at the gate region edge towards the deep drain side causes increasing drain resistance with small N_{DD}. The local point V_{DP} surrounded by the overlapped gate region refers to the gate control endpoint, and it is calculated by flow of current in the channel. Current flow in the channel region is expressed as

$$I_{ds} = 2\frac{W}{L} \cdot \frac{\mu_{eff}}{\beta} \times \left[(Q_{nL} - Q_{n0}) - \frac{\beta}{2} \cdot (Q_{nL} - Q_{n0}).(\emptyset_{SL} - Q_{S0})\right] \quad (6)$$

The flow of current in the drift drain region (I_{DPP}) is given as [24]

$$I_{ddp} = W \cdot X_{OV} \cdot W_q \cdot N_{DD} \cdot \mu_{drift} \cdot \frac{V_{ddp}}{L_{drift}} \quad (7)$$

$$V_{ddp} = V_{ds} - V_{dp} \quad (8)$$

Here, X_{OV} and W are the current flow under the extended depth of overlap region and width. The V_{ddp} can be determined by the difference in the concentration of drift drain, channel region, and drift-channel length. The V_{di} is calculated by the potential drop at the depletion side of the drain region[78] .

$$V_{di} = V_{dp} + V_{bidrain} - V_{bisource} - E_{drain} \cdot w_{dep\_D}/2 \quad (9)$$

The $E_{drain} \cdot w_{dep\_D}/2$ is the additional potential drop generated at the drain side due to low charge density.

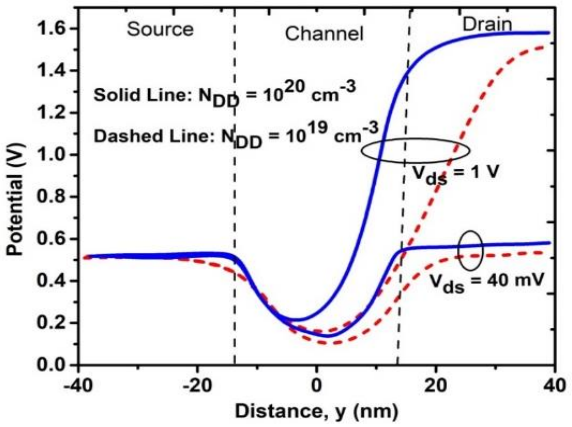
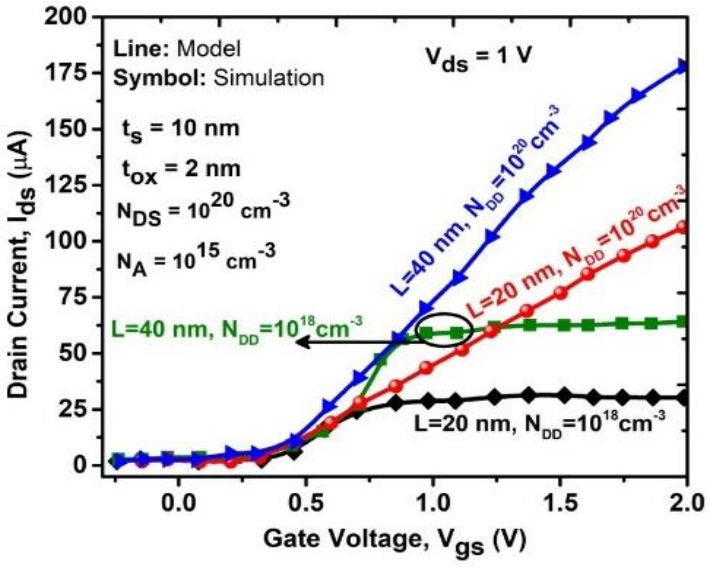
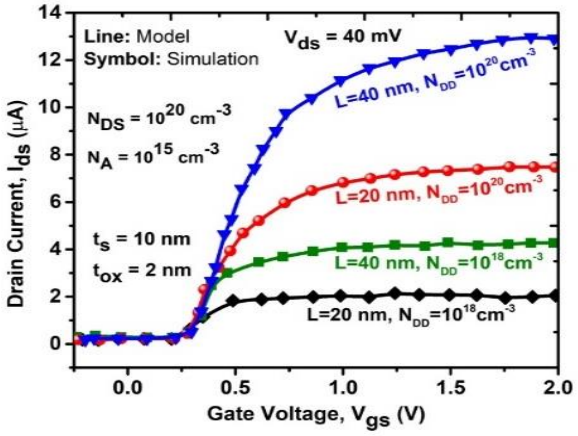


Fig.5.5: The potential distribution for various drain side doping concentrations and drain voltages at the middle of the channel (x=0).

V_{gs}-I_{ds} characteristics of Modelled and simulated graph is shown in Figure. 5.6(a) for V_{ds}=40 mV and Figure. 5.6(b) for V_{ds}=1V with various channel lengths and concentration near drain side. The degradation of sub-threshold swing enhanced with both high and low drain voltages for N_{DD} reduction. Also, the effect of drain resistance is drastically improved with decreasing channel length.

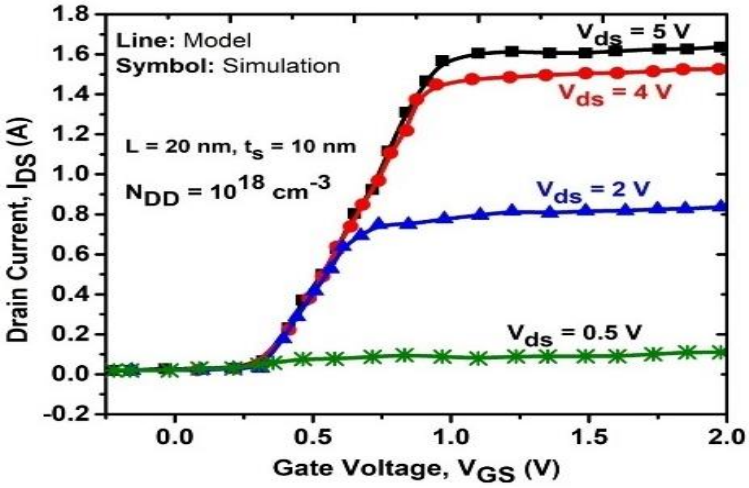


(a)

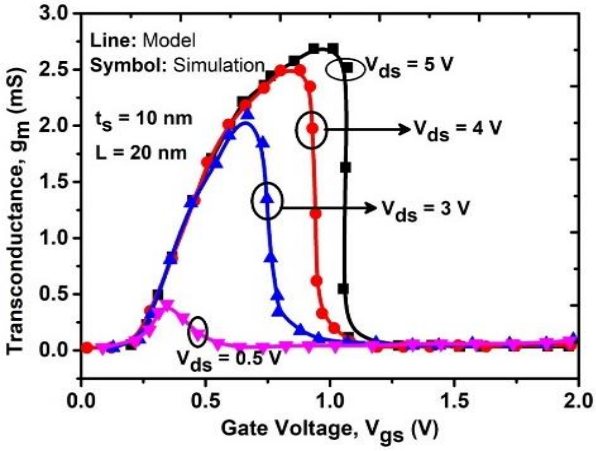


(b)

Fig. 5.6 Modeled and simulated V_{gs}-I_{ds} characteristics at (a). V_{ds}=40 mV (b). Different channel lengths and drain side doping concentrations for V_{ds}=1V.



(a)



(b)

Fig. 5.7: (a). V_{gs}-I_{ds} characteristics with different drain voltages with $L = 20\,nm$, $t_s = 10\,nm$, and $N_{DD} = 10^{18}cm^{-3}$ and (b). Transconductance characteristics with different drain voltages.

Upon validation with 2D numerical simulation for higher voltages, proposed device structure exhibited favorable agreement between simulation results and the model. The modeled and simulated V_{gs}-I_{ds} characteristics for different drain voltages with $L = 20\,nm$, $t_s = 10\,nm$, and $N_{DD} = 10^{18}cm^{-3}$ is shown in Figure. 5.7(a). Figure 5.7(b) shows the transconductance characteristics of DG-MOSFET for different values of V_{ds}. The transconductance has no dependency on V_{gs}, which is called quasi-saturation behavior. An abrupt change in g_m has been observed with an increase in the applied voltage V_{ds}.

5.4 Summary

An analytical model utilizing surface potential has been devised for high-voltage applications to tackle Short Channel Effects and drain current behavior in double-gate MOSFETs. Analytical modeling integrates various biasing conditions through drift-diffusion approximations. The developed model accounts for the presence of a highly resistive drain region and addresses

the impact of short-channel devices by considering potential distribution along the channel. The results demonstrate a clear reduction in short-channel effects by minimizing the resistive region at the drain side and mitigating the influence of potential distribution at the overlapped drain region. The increasing overlap length can reduce the effects of short-channel devices. The analytical model that has been developed is substantiated by comparing it with numerical simulation results, and the two are found to be in excellent alignment. This model can be effectively employed even when the device dimensions vary, making it a valuable tool for modeling multigate MOSFETs.

CHAPTER 6

CONCLUSION AND FUTURE SCOPE

6.1 Conclusion

The continual scaling of MOSFET devices results in the deterioration of their performance, primarily due to current leakage and the occurrence of SCEs.

To enhance CMOS technology's functionality, innovative approaches have been incorporated into field effect transistors and the development of non-classical multi-gate FETs.

It is crucial in IC design, to possess a precise device model that accurately characterizes the device's electrical properties. Continuous research on device optimization techniques, including gate engineering, doping profiles, and fabrication processes, and reliability in extreme temperature environments

The thesis successfully presented an analytical framework for P+ pocket SiC Gate-all-around Junction less field-effect transistors and assessed its accuracy under various conditions. The research demonstrated the model's effectiveness in predicting device behavior.

The effect of high-temperature was also examined in the study. It highlighted the challenges associated with high-temperature operation and provided insights into potential improvements and mitigation strategies.

The research assessed the performance of P+ pocket SiC gate-all-around JL FETs, including their electrical characteristics and thermal behavior. This evaluation contributes to a comprehensive understanding of the device's capabilities and limitations.

The thesis has laid a solid foundation by developing an analytical model and addressing the impact of high temperatures on P+ pocket SiC gate-all-

around JL FETs. Future research can build upon these findings to further advance the understanding and practical applications of these devices in demanding environments.

The thesis has effectively characterized multi-gate FETs with a focus on mitigating short-channel effects. The research demonstrated the device's potential for high-power applications and its improved performance compared to traditional FETs.

The research findings indicate that the novel configuration of multi-gate FETs serves as a highly efficient solution for minimizing short-channel effects, notably addressing concerns like DIBL, subthreshold slope. This reduction is crucial for maintaining device performance at high power levels. The research has highlighted the enhanced electrical properties of multi-Gate FETs, including improved transconductance, subthreshold swing, and ON/OFF current ratios, which are essential for high-power applications.

The future research scope involves further development, optimization, for high-performance and efficient use of power electronics in various domains.

The work has demonstrated that these multi-gate FETs can operate at high power while maintaining reasonable power efficiency, making them suitable candidates for various high-power electronic systems.

6.2 Future Scope

Future work should include experimental validation of the analytical model. This step would confirm the model's accuracy and applicability in practical scenarios.

Explore applying alternative materials or advanced SiC processing techniques. Investigate the use of advanced materials and fabrication processes to enhance the device's performance and reliability in high-power applications.

Explore the integration of these transistors into larger electronic systems and circuits, assessing their compatibility and potential benefits in specific applications, such as aerospace, automotive, or power electronics.

Analog and RF study of the short-channel of 10 nm nanowire devices can be carried out.

Explore strategies for further scaling and miniaturization of multi-gate MOSFETs to improve their power-handling capabilities while maintaining reliability.

Consider the influence of quantum effects as devices continue to shrink and investigate how these effects may change the performance and reliability of Multi Gate FETs.

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