IMPLEMENTATION OF NINE LEVEL MULTISTRING MULTILEVEL INVERTER WITH LESS DEVICE COUNT FOR OFF GRID PV SYSTEM

Thesis Submitted for the Award of the Degree of

DOCTOR OF PHILOSOPHY
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DECLARATION

I, hereby, declare that the presented work in the thesis entitled "Implementation of nine level multi-string Multilevel inverter with less device count for OFF Grid PV System" in fulfillment of degree of **Doctor of Philosophy (Ph. D.)** is outcome of research work carried out by me under the supervision Dr. N. Karthick, working as Associate Professor, in the School of Electronics and Electrical Engineering of Lovely Professional University, Punjab, India. In keeping with general practice of reporting scientific observations, due acknowledgments have been made whenever work described here has been based on findings of other investigators. This work has not been submitted in part or full to any other University or Institute for the award of any degree.

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CERTIFICATE

This is to certify that the work reported in the Ph. D. thesis entitled "Implementation of nine level multistring Multilevel inverter with less device count for OFF Grid PV System" submitted in fulfillment of the requirement for the reward of degree of **Doctor of Philosophy (Ph.D.)** in the School of Electronics and Electrical Engineering, is a research work carried out by Bulbul Sharma, 11814176, is bonafide record of her original work carried out under my supervision and that no part of thesis has been submitted for any other degree, diploma or equivalent course.

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LIST OF ABBREVIATIONS

Abbreviations	Full Form
SVC	Space Vector Control
PWM	Pulse Width Modulation
DSP	Digital Signal Processors
IEA	International Energy Agency
TPES	Total Primary Energy Supply
REGS	Renewable Energy Generating Systems
THD	Total Harmonic Distortion
BIPV	Building-Integrated Photovoltaics
VSD	Variable Speed Drives
CMLI	Clamped Multilevel Inverter
NPC	Neutral-Point Clamped
SVM	Space Vector Modulation
FBI	Full Bridge Inverter
SFC	Static Flicker Compensator
NPC	Neutral-Point-Clamped
CHB	Cascaded H-Bridge
MLI	Multilevel Inverter
MLDCLs	Multilayer DC Links
MPC	Multiple Point Clamped
FCMLI	Flying Capacitance Multi-Level Inverter
NP	Neutral Point
TCI	Transistor-Clamped Inverter

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ABSTRACT

Industrial power conversion systems frequently employ multilevel inverters for driving and utility applications. Recently, multilevel inverter technologies have drawn more attention in high voltage, high power applications due to their capacity to fulfill rising needs for power rating & power quality associated with decreased harmonic distortion and reduced electromagnetic interference. Minimizing the total harmonic distortion in voltage output waveform is main goal of this thesis. This study is the component of such programmers, with the reduction of circuit complexity and cost as the expected improvement.

This dissertation focuses on a cascaded multilayer inverter with variable or unbalanced dc sources. Energy conversion systems employ power inverters that use pulse width modulation (PWM) techniques. Only equal dc sources can be used with the conventional PWM methods, sinusoidal PWM methods, and space vector control (SVC) methods. Additionally, classic SVM algorithms use pre-computed tables or trigonometric functions the majority of the time, which increases their complexity and processing cost, the more levels of the inverter there are. In addition, this research has presented a new multilevel inverter topology based on switch-sharing technique to achieve this. Three modules make up the topology. It brings about a configuration of traditional full-bridge circuit having three bidirectional switches with usage of Modules 1 and 2. Bidirectional switches that are coupled to DC sources make up Module 3. The switches here work in their optimal mode. Each switch's action is separated into its three phases in this manner. The (m + 1)-level structure is created by adding 1 bidirectional switch to Module 3 of the m-level structure. For this architecture, a new modulation strategy built on the PWM principle and utilizing virtual vectors has been devised. The problem in decomposing the reference vector in some zones due to the deletion of many voltage vectors can be efficiently handled by using the virtual vectors.

The suggested 9-level inverters have been the subject of a thorough analysis. Through simulation utilizing MATLAB/SIMULINK, performance of suggested inverter is examined. “Digital Signal Processors” (DSPs) have been utilized to implement current

control & proposed modulation algorithms in the hardware prototype of proposed multilevel inverter, which has been created for validation.

CHAPTER- 1

INTRODUCTION

1.1 Research Background

1.1.1 Introduction

This chapter offers comprehensive summary of research described in this thesis. 1st, relevance of energy sustainability & how it sparked desire to do this study are discussed. Next, goals & methods of study are laid forth. The last portion of this thesis provides a summary of the various chapters.

1.1.2 Study Motivation

Today, one of the most pressing global issues is how to keep using energy indefinitely. If we don't address this issue, we risk damaging the environment, which must be protected for future generations. International Energy Agency (IEA) 2012 Key World Energy Statistics show that 81 percent of 2010's Total Primary Energy Supply (TPES) originated from fossil fuels. Fossil fuels, despite their high energy density per unit weight and cheap production costs, are short-lived. Depletion of fossil fuel stocks occurs on a regular basis. Given that fossil fuels aren't renewable, there will come a moment when they can't keep up with the demand for energy. In the event that such a scenario arises in the future, we will face a severe energy crisis.

The rising levels of CO2 emissions caused by the combustion of fossil fuels are yet another major worry with relation to their usage. This gas contributes to global warming and climate change by being released into the atmosphere in excessive amounts. According to the IEA's executive summary of its World Energy Outlook 2013 report, the energy sector is responsible for almost two-thirds of all worldwide emissions of greenhouse gases. More than twice as much carbon dioxide was emitted from the atmosphere as it was in 1973. According to an executive summary cited above, energy-related CO2 emissions are estimated to climb by 20% through 2035 as a result of rising energy consumption. The average worldwide temperature will rise by 3.6 degrees Celsius as a consequence, exceeding the 2-degree objective. A two-pronged approach

has been taken to ensure long-term energy sustainability. Increasing renewable energy's share of the world's total TPES is the first step in this strategy. A great alternative to fossil fuels is the use of renewable energy as solar, wind, tidal, biomass, & geothermal power. Renewable energy is ideal for dealing with the problem of fossil fuel depletion since it can be produced indefinitely. Renewable energy is also ecologically beneficial, which is a major factor in making it a winning policy. It's easier to combat global warming and climate change when there aren't any emissions of CO2. Not only does this mean that there will be no pollution generated, but it will also mean that future generations will have a safer planet to inhabit. However, the high expense of developing renewable energy generating systems (REGSs) remains a barrier to widespread use of renewable energy as power source. Consequently, the strategy to increase usage of renewable energy is a long-term one.

Energy efficiency may be improved by lowering the quantity of energy used by certain applications in the short and medium term. Reduced energy usage may be achieved by reducing waste. In this approach, power electronic converters might play a crucial role. Due to ASDs' ability to guarantee that the electric machine only uses enough energy to accomplish a certain job when it is used in a variety of applications, such as pumps and fans, ASDs may save a significant amount of energy (Mohan, 2003). An inverter, a kind of power electronic converter, is necessary for an ASD to work effectively. It is the converter that controls the power given to the machine, making it essential to the drive's variable-speed capability [1]. As with REGSs based on wind and solar photovoltaics, this is also the case. To provide the grid with AC power, the inverter transforms the DC electricity it receives. It is preferred if the inverter is very efficient in its work.

ASDs and REGSs are becoming increasingly interested in multilevel inverters. It is more difficult for multilevel inverters to create voltage waveforms with high total harmonic distortion (THD) than standard two-level inverters due to the fact that the waveform has more levels and hence approaches a pure sinusoidal shape. In turn, this important property results in lower voltage derivatives (dv/dt), minimal filter needs, higher voltage capacity, enhanced efficiency, and sinusoidal currents [2]. An additional benefit of multilayer inverters is their capacity to produce high voltage ratings that

exceed maximum voltage ratings of current semiconductor power switches. This was the initial rationale for their invention. Due to this unique characteristic, ASDs and REGSs prefer to use multilayer inverters for average & high-power applications. Using a 2-level inverter to provide equitable voltage sharing across series-connected power switches was difficult because of the economics and technical problems of constructing precise resistive and capacitive components. Due to the switch's limited extreme voltage rating, serial connecting of switches is required to achieve greater voltages. Regarding high-power applications, multilevel inverters are often employed. However, they have also been explored for low-power apps, especially now that the issue of energy sustainability is becoming more pressing. Multilevel Inverters Innovative solutions like microgrids and building-integrated photovoltaics'(BIPV) have been presented as part of a concerted effort to increase the deployment of renewable energy. These small-scale distributed power production devices are capable of generating their own electricity for buildings. Using photovoltaic (PV) panels, fuel cells, and micro turbines, they may create a small-scale power-generating network which may be hooked up to the utility grid and use a variety of renewable energy sources.

They increase the resilience of generating systems in the event of a power grid disruption caused by islanding. The PV modules in BIPV systems replace the roof, skylight, and façade of a building. To put it another way, the building itself may be used to generate enough electricity to meet the building's needs while simultaneously supplying any excess back to the grid. The usage of multiple inverters in microgrids and BIPV systems has already begun. Multilevel inverters may be advantageous for certain applications, even though two-level inverters are usually adequate for low-power use cases. The issue of individual PV modules connected in series is partially shaded has been addressed, for example, by the use of multilevel inverters [3]. PV modules are affected by partial shade when they are exposed to varying levels of sunlight, which results in a considerable decrease in output power. Multi-level inverters may also be used to decrease conversion losses in micro grids and boost efficiency [4]. The airplane system is another low-power application where multilevel inverters have been found to have considerable promise [5]. Compressors, hydraulic pumps, gasoline meters, electronic brakes, and engine starters all appear to require inverters these days.

The inverters, on the other hand, must adhere to a number of tight rules. The limit on one's weight is one such condition. Using strong differential mode and common mode filters is compulsory for 2-level inverters. Increasing frequency of switching is the only option to lower the size of these filters. As a consequence, the weight of the cooling system increases as a result of significant heat dissipation. As a result, multilayer inverters have been presented as a viable alternative to the two-level inverter's shortcomings.

Despite their advantages, multilayer inverters have one major problem. With an increased level count comes an increase of power switches [6]. As a result, a more difficult and expensive control issue arises. A careful balance must be struck between circuit complexity and implementation cost so that the inverters may still provide high-quality outputs while still achieving high-efficiency performance.

This investigation is then carried out in an effort to find a middle ground. There are two parts to the research. The open-loop system's multilevel inverter is defined in detail in first section. Inverter's new pulse width modulation (PWM) architecture is designated in detail. Digital signal processor (DSP) is utilised in laboratory prototypes to implement PWM algorithm. For closed-loop systems [7], 2nd part discusses the creation of the current controller, which employs a feedback channel to accomplish this goal. Closed-loop hardware testing is performed using a DSP-based current controller. The suggested multilevel inverter's performance is then evaluated using a comprehensive review of the simulation and experiment data.

1.2 Research Objectives

These studies are aimed at creating improved power quality and energy efficiency by creating a new multilayer inverter architecture and using a new control technique. As the expansion of voltage levels, the inverter's design places a greater focus on minimizing the circuit's component count. Harmonic content and power losses are important considerations in developing the control approach. Listed below is the particular study, aiming at three distinct perspectives:

- Topology:

Just a few circuit components are needed for a 3-phase, multi-level voltage source design with an increase in voltage levels

- Modulation technique:

Create a new PWM scheme that can fit the unique characteristics of the proposed multilayer inverter while still achieving an increased efficiency rating and a reduced harmonic part, and lesser value of overall harmonic distortion in O/P of inverter.

- Controller:

To develop a novel tuning method for an adaptive current control controller in order to maintain acceptable output current quality under variable load situations.

1.3 Methodology

Introduction of suggested multilevel inverter topology kicks off research's design phase. Using this configuration, the number of semiconductor components may be kept to a minimum while yet allowing several power switches [8] to be shared throughout the three phases. At low switching frequencies, the suggested topology's operational principles are studied utilizing the analytical technique in the preliminary study. The PWM [9] approach is then used to achieve high switching frequencies. Virtual vectors are used to alter the standard PWM in order to fit the suggested architecture.

The suggested PWM is shown using seven and nine-level architectures. When using modified PWM, a full technique for calculating on-state times of the closest vectors has been devised in order to adapt to shifting loads.

Use of power electronic converters in industry has grown as a consequence of their many advantages, including reduced power consumption, increased system efficiency, better product quality, and ease of maintenance.

It’s challenging to connect single power semiconductor switch to a medium-voltage grid. 2 to 3 Multilayer power converter structure is recommended for high & medium voltage applications such as conveyors, mills, laminators, compressors, blowers, & pumps. Solar, wind, & fuel cell [10] systems may be easily integrated into a high-power system because to the multilayer converter's cheap cost.

Traction has been the most typical use of multilevel converters in the early stages of development [11]. High-voltage dc (HVDC) transmission, medium-voltage induction motor variable speed drives (VSDs), active filtering and VAR correction are among the most current applications of power system converters. There are several applications for multilayer converters, including electric traction drives, flexible AC transmission systems (FACTS), utility interfaces for renewable energy systems, and industrial medium voltage motor drives. [12].

These high-voltage, high-power use cases need inverters that are able to handle necessary voltage and power levels. These inverters have been designed to take use of the fact that switching devices like GTOs, IGCT and IGBT may be coupled in series [13], allowing higher voltage and more power. In transient and steady-state switching operations, the applied voltage for each device may be significantly greater than the blocking voltage of the devices because series-connected switching power devices do not have an equal distribution of applied device voltage throughout their associated circuits.

A wide range of multilayer inverter & converter circuit topologies has been investigated and utilised to effectively address challenges outlined above. Several separate DC voltage sources combine to create multilayer output (o/p) voltage of inverter [14]. The quantity of output filters needed decreases as number of voltage levels increases.

There has been talk about multilevel converters since 1975 [15]. An inverter with many levels of cascading was first suggested in 1975. Using two full-bridge DC cells in series, staircase AC voltage may be generated; term "multilevel" was initially used in the context of a three-level converter. [16]. Different topologies for many levels of conversion followed [17]. Diode-clamped multilevel inverter (CMLI) methods, known as Neutral-Point Clamped (NPC) inverters, were first developed in 1981 [18]. Cascaded multilevel inverters [19-20] were first presented in 1996, whereas capacitor-clamped multilevel inverters were first suggested in 1992. But it wasn't until the mid-1990s when cascading multilayer inverters became commonplace. As a result, motor drives and utility applications benefited greatly from cascade multilayer inverters. The growing need for medium-voltage high-power inverters has sparked great interest in the cascade

inverter. Also, the cascade inverter may be utilised to drive regenerative-type motors. Some innovative multilayer inverter topologies have recently appeared. [21, 22] and [23, 24] soft-switched multi-level inverters are included in this group of inverters. [25]. Increased voltage and power ratings are possible with the use of multiple inverters. They may also increase equivalent switching frequency without raising real switching frequency by reducing electromagnetic interference effects and ripple components of inverter output voltage. There are several approaches to constructing a multilayer converter. To create multilayer waveforms, the easiest method is to link standard converters in parallel or series [26]. The more intricate the structure, the more converters are inserted into converters. As a result, the converter's voltage or current rating may surpass that of the individual switches, allowing it to operate at a higher voltage or current level.

It is possible to create an ascending voltage waveform using several low-voltage dc power semiconductor switches, and this is the underlying notion of a multilayer converter. Capacitors and other types of DC voltage sources might be utilised in combination with batteries and renewable energy sources. There are two power semiconductor switches, one of which depends on a dc voltage source connected to it to obtain a high output voltage.

Compared to traditional 2-level converters that utilise high switching frequency PWM, multilayer converters offer various benefits. Many benefits may be summarised as follows for multilayer converters, including the following:

1. Staircase waveform quality: Due to the fact that multilevel converters may lower dv/dt strains while simultaneously generating output voltages with minimal distortion, they can help with EMC issues.
2. Common-mode voltage: With multilevel converters, a motor's bearing load may be reduced by a significant amount. Furthermore, sophisticated modulation schemes such as those presented in [29] may be used to eliminate CM voltage.
3. Input current: Multilevel converters provide little distortion of the input current.
4. Switching frequency: Multilevel converters are frequency and PWM-capable. The decreased switching frequency [28], smaller switching loss and greater

efficiency of the system. There are certain drawbacks to using multilevel converters. The necessity for more switching devices is one drawback. A multilevel converter might be used switches, rated for lower voltages, but each switch must have its own gate-driving circuit. System complexity and expense may rise as a result of this.

Only a handful of the modulation and control paradigms for multilevel converters have been established, such as SHE-PWM [29] and space vector modulation (SVM) [30]. We'll be using something called sinusoidal pulse width modulation (SPWM) in this work.

1.4 Why Hybrid-bridge multilevel inverter?

A shift is taking place in the energy landscape. A sense of dependency on fossil fuels, coupled with a rise in their price, has led to massive investments in economic and human resources in order to discover alternative, less expensive and cleaner sources of energy [31]. Various kinds of power inverters have been created throughout the years to make usage of renewable energy sources reality. High-power electronic systems are also essential in transmission lines to ensure power distribution &energy quality. Since these activities must be completed with great efficiency, electronic power inverters must be used. To meet the ever-increasing global need for energy, a variety of novel power converter designs and new semiconductor technologies have been developed. High-power semiconductors [32] are still in the midst of constant competition to create higher voltage and greater current power semiconductors. Traditional high-voltage converter topologies and novel medium-voltage topologies [33] are now in a fierce battle, with both having their advantages and disadvantages. When used in conjunction with electric motor systems, power inverters are a really remarkable piece of equipment. A broad number of industries might benefit from them, including transportation (train traction and ship propulsion), manufacturing, energy conversion, petrochemical [34], and mining. In order to achieve better production rates, lower costs, and greater efficiency, several of these procedures have been steadily growing their power requirements. [35].

In response to this need, power electronics research [36] and industry have developed semiconductor technology to achieve higher nominal voltages & currents & have used older semiconductor technology to create unique converter topologies known as multilevel inverters. The advantages of well-known circuit topologies and control approaches were passed down in the first attempt. In addition, newer semiconductors are more expensive, & to meet other power-quality criteria, more power filters may be necessary. This is why power is growing. This means that a new converter architecture based on the multilevel notion will be a viable option. Right now, this is the most difficult problem to solve [37].

Conventional power inverters that are utilising high-power semiconductors are still under development & have not yet reached maturity in the multilayer technology with medium voltage semiconductors. Traditional inverters work well in low-power applications, but in high-power settings, they fall short of the requirements. In light of the future, we should be aware of the advantages of multilayer technology to recover drawbacks of traditional inverters [38]. Multilevel inverters are a suitable option for power applications since they are capable of providing high power utilising established technology [39].

Medium-power microelectronics are available. Multilevel inverters outperform the well-known 2-level converter in relation of both performance and dependability [40]. With these benefits, the output signal quality (voltage and current) is improved while the converter's nominal power is increased. [41].

Since these characteristics make multilevel inverters so appealing to the industry, many researchers from around the world are currently working hard to find ways to improve their performance, such as by simplifying controls and implementing various optimization algorithms, to improve output signal's THD [42], DC capacitor voltage's balance [43], and the t-sharpness ripple of the signal. Among the current research, priorities are the creation of novel multilevel converter topologies (new or hybrid) and new control schemes, for example, the elimination of harmonics through the use of pre-calculated switching functions, the mitigation of harmonics in order to meet specific grid codes [43]. Let us first take a look at the traditional inverters and the issues they

face before moving on to discuss multilayer inverters. Inverters in medium-to-high-power range & the problems they present are essential for resolving the problems with classic inverters. The following are a few of the most important points to keep in mind.

1. Currently, inverter circuits employing the fundamental "inverter leg" construction block have a wide range of application power (from 1 kW to 10 MW+).
2. These PWM-controlled induction motor drives (figure.3) are used in many different applications, from 3kW to 100kW in the industrial arena. IGBT devices are almost universally used in this range of power.
3. Power levels (>1 MW) have recently become a new application area for these circuits.
   (a) Locomotives on the railway
   (b) Powering a ship
   (c) FACTS, a flexible AC transmission system, can provide output power of up to 100 MW.
4. Devices like IGBT, GTO, and IGCT are used in all applications. Insulated Gate Commutated Thyristor, Megawatt-class inverters, on the other hand, have serious design flaws.

The V and I can't be handled by a single device.

- Using a 1 MW drive as an example, a DC connection of 5 to 7 kV is often provided at either 4.16 kV (US) or 3.3 kV (UK). Additionally, the motor is supplied with a voltage of 3.3 kV (or 4.16 kV).
- An 8-10 kV device voltage rating is not available.
- Paralleling devices (or inverters) to handle large currents is a well-established technique. The challenge persists in obtaining the necessary voltage handling capacity.

As a result, certain traditional methods are available to address the above-mentioned issues.

- Using common converter topologies in a series configuration.

- Distributing the voltage stress across low-voltage devices using various topology inverters (Multi-level inverters).

In any event, the first instance it's dubbed a "classical" converter since it employs semiconductor devices in series [44]. Observe the layout. Another way of looking at it is that the voltage capability of a set of devices increases [45]. Inverters are able to handle large power demands in some way, thanks to this setup. However, output voltage quality is one of main drawbacks. However, converter's output can only be two levels when used with a classical arrangement. Such waveforms, in reality, have a lot of harmonic content. Harmonics of the 3rd, 5th, and 7th orders are particularly interesting. The equipment's performance is severely harmed by its harmonics. A variety of low-pass filters are often utilised to diminish unwanted output harmonics and thereby enhance sound quality. However, if the filter is of low quality, the overall size will be higher. Design of Low Pass Filter is also known to be time-consuming and physically demanding [46]. There is a lot of work being done to minimise the size of the filters in electronic circuits [47-48]. Classical inverter difficulties may be summarised as follows based on the above observations:

- This means that all DC voltage flows across a switch when its power is shut off. To avoid damaging the devices, this voltage must be increased.
- Using high-value parallel resistors may help address the problem of devices not sharing voltage in off state due of variances in LC (static sharing).
- In more severe terms, the devices' switching speeds will not allow them to share a common supply of power. Gate driving methods and/or snubbers unique to each application are necessary (dynamic sharing). There is still a long way to go.
- Voltage sags may be a concern for motor insulation because of the two-level output
- It is possible to achieve lower switching frequencies using multi-level techniques because they reduce harmonic content.
- It is possible to utilize standard PWM approaches.
- Comparatively speaking, the power circuit has fewer components than other (multilevel) circuits.

- It is possible to provide redundancy (to increase the circuit's dependability) by utilising more series devices than are really needed.

Although traditional inverters have a lot of shortcomings, this example shows that they have much more disadvantages than advantages. In order to accommodate the increased demand for electricity, a multi-level approach might be used.

Classical inverters, on the other hand, offer a limited number of benefits.

Cascading, multi-level inverters are being considered to minimise the number of inverters.

- Conventional multi-pulse inverters need large transformers that are difficult to transport.
- For diode-clamped inverters with many levels of clamping diodes.
- Multilevel flying-capacitor inverters, flying capacitors are needed.

Also, it has the following features:

- High-voltage, high-power applications are better suited to this inverter than traditional inverters.
- A multistep staircase voltage waveform is generated by switching each device just once each line cycle & increasing the number of levels.
- Voltage balancing (sharing) and voltage matching are not required since the Inverter Structure comprises several single-phase inverters, inverter units and each bridge is provided with distinct DC source.
- The smaller component count and simpler structure make packaging design considerably easier.
- By adopting soft switching in this setup, lossy & bulky resistor-capacitor-diode snubbers could be prevented.

In order to validate the theoretical study, MATLAB/ SIMULINK software is employed. There are several technical domains where this programme is often used. To begin, a simulation of an open-loop system is run in which no feedback channel is required. Switching frequency is simulated for both seven- and nine-level designs [49]. On the

basis of simulation outcomes obtained at different reference voltage levels, suggested PWM is judged to be viable. There is an evaluation of the harmonic content, waveform pattern, voltage magnitude, and total harmonic distortion (THD) [50]. There is also hint of looking into power outages. Next, for closed-loop system with feedback route, the adaptive PI controller's performance under changing load situations is simulated [51]. Using the simulation results, the step responses and output current quality may be evaluated. Hardware implementation & experimental studies are utilised to verify simulation findings. A prototype of multilayer inverter is built for laboratory testing. The DSP is utilised to carry out PWM and control algorithm calculations [52]. There is both open and closed-loop testing. To bring this project to a close, all of the data from the experiments have been thoroughly evaluated.

1.5 CHAPTER OVERVIEW

Six chapters make up this report. The description is a quick summary of the chapters that follow:

Chapter 2 discusses three-phase multilevel inverters. At the start of the article, there is brief introduction to multilevel inverters. Multilevel inverter topologies, both old & modern, are examined in detail in this thorough examination. This chapter also covers multilayer inverter-friendly modulation and current control approaches.

The suggested multilevel inverter architecture is the subject of Chapter 3, which delves into its design. Before describing the operational principles using four and five-level structures, generalised structure of suggested topology is provided. At conclusion of this chapter, we'll go into the specifics of the PWM technique and the controller's architecture.

The suggested multilayer inverter based on 4 & 5-level structures is discussed in Chapter 4. The findings come from both conventional PWM and the new PWM scheme while the inverter is working at low and high switching frequencies, respectively. An evaluation of dynamic performance and power loss is also included. This chapter also includes some comparative analysis with respect to certain standards.

In Chapter 5, the suggested multilayer inverter's hardware implementation is described in depth. This chapter explains how to build a lab prototype of the inverter for seven

and nine-level structures. It's also possible to find information about the algorithms' underlying code. In this section, we'll go through the key data and findings from the experiments.

There are some final observations in Chapter 6. It also offers contributions of research and recommendations for further work.

CHAPTER- 2

MULTILEVEL INVERTERS: REVIEW OF TOPOLOGY, MODULATION TECHNIQUES AND CONTROL

2.1 Literature Review

Prathviraj Shetty, S. Dawnee [1]: - The fuel prices increasing the environmental impact of burning fossil fuels has directed to increase in requirement for hybrid electric vehicles. As a result, to fulfill the higher performance demands of the HEV, a thorough understanding of the whole electric power train is required. Accordingly, in this study, an E-motor that is most suited for HEV applications will be modeled in this article's electric power train. Here, a three-phase, two-level VSI uses the SVPWM approach to regulate the switching of the PMSM. E-motor. Controlling speed & torque is accomplished via the PI controller using error signals generated from speed & current feedback. The SVPWM module receives the magnitude & reference angle from the PI controllers, which provide two voltage references. As the user requests, the SVPWM module provides VSI with the pulses it needs to produce the desired voltages. MATLAB Simulink was utilised for the modeling & simulation of suggested electric power train, which is environmentally friendly & efficient enough for use in hybrid electric cars.

B. Zhu et al. [2]. A 3-phase open-end winding inductive motor drive is controlled by an input-switched multilevel inverter design in this research. An SPMT setup then chooses any desired level of voltage from the resultant "n" possible levels of voltage after an equal number of steps are made to split the DC link voltage collected from one voltage source. The required AC voltage is then produced by an H-bridge by switching polarity of voltage at its O/P. When compared to more typical systems which employ neutral-point-clamped (NPCI) converters or flying capacitor converters, this multilayer inverter drive method utilizes far fewer switches. Only 2 switching devices/phases are needed to get two more voltage levels at O/P. Any needed voltage steps at machine terminals are easy to get using an input-switched inverter structure. The use of symmetrical sinusoidal PWM in conjunction with standard SPWM is also advocated as

a hybrid modulation approach. A seven-level input-switched inverter drive circuit analysis, modulation method, & software simulations are provided.

Mariusz Malinowski, K. Gopakumar [5] Research & development of multilevel inverters has been ongoing for over three decades, with successful industrial applications. There have been several new contributions & industrial topologies described in the recent few years; however, this technique is still in progress. Grouping & reviewing these recent contributions to identify current state-of-the-art & trends to offer readers thorough & informative overview of where the multi-level inverter technique stands & where it is headed is the goal of this study. Multilevel converters, which have been around for long period, are initially discussed in this article, & then focus shifts to newer models which have just come into use in industry. New potential topologies are also addressed. Modulation & control of multilayer inverters have recently made significant strides, & they are discussed as well. Nontraditional technologies driven via multilevel converters & how multilevel converters have become an important technique in several industrial domains are the focus of this presentation. Last but not least, some potential trends & obstacles in continued growth of this technique are deliberated to stimulate upcoming contributions, which discourse unresolved issues & explore novel prospects.

FarhadShahnia et al. [7] One-phase 1x25 or two-phase 2x25 kV AC systems are used in the architecture of the electrified railroads' electrical distribution system. Because of their superior qualities & lower prices as compared to other motor types, AC induction motors are the electric drives of choice for the majority of electric trains. Catenary voltage was formerly reduced using a transformer; however, this has been done away with for efficiency reasons. In this study, a transformerless method of feeding induction motors is discussed. PWM-controlled inverter transforms DC voltage from the catenary's single-phase AC power to three-phase AC voltage using this arrangement. Fewer harmonic currents are introduced into the power system when using this kind of arrangement. PSCAD/EMTDC program is used throughout the article to simulate the current harmonics. The simulation's output includes the present system's waveforms & the THD's magnitude. Induction motors fed by a transformer may be avoided, & the

quantity of harmonic distortion in the power supply is considerably reduced by using such a design.

José Rodríguez et al. [9] As multilayer inverter technology improves, high-power medium voltage energy control is now an option. An inverter with a clamped diode, a flying capacitor inverter, and a cascaded multicell are all instances of this kind of topology. These two technologies, both of those are in the early phases of development, are being examined by authors. Multilayer sinusoidal PWM, multilevel harmonic removal, & SVM are all discussed in this study as important control & modulation approaches for this particular converter family. Converters that may be used for laminating, conveyor belting, & unified power-flow controllers are given special attention in this section. Those inverters that provide regenerative loads need an active front end, & circuit architecture possibilities are also offered. Optical sensors, high-voltage, high-power devices, & other frontiers of technology advancement are also discussed.

Leon M. Tolbert et al. [11] Due to high-frequency switching of conventional inverters for motor drives, common-mode voltage &change in high voltage (dV/dt) rates in motor windings may create several issues. Because of their lower switching frequencies, multilevel inverters are an effective solution to these issues. As an electric drive converter, a cascade converter having distinct DC sources & consecutive diode-controlled converter were found. There are several advantages to using a cascade inverter for large automobile all-electric drives as its high VA ratings & the usage of wide-range sources of DC Voltage. The back-to-back diode-controlled inverter is perfect for hybrid electric vehicles, which have an ac voltage supply. These two converters outperform PWM-based motors in simulations and experiments.

Krishna Kumar Gupta et al. [12] The use of multi-level converters for high-power DC-AC conversion is on the rise. MLIs are also being considered for low-power applications, which is something that has just recently emerged. However, increasing the number of layers still presents a barrier in terms of component count. 6 active switches and an asymmetric source configuration are utilised to create 7-level waveform in this paper's inverter. Eight high switching frequency active power

switches are required for cascaded H-bridge (CHB) inverter with comparable source arrangement. In a suggested modulation technique, switches with the greatest blocking voltages are activated at fundamental frequency. The workings of suggested inverter are discussed & ideas are proven via simulation & experimental data.

Peter W. Hammond [13] Torque spikes may be reduced by modifications to the motor's voltage & current waveforms. Motor insulators are not subjected to more stress than they can handle because the zero-sequence voltage is not applied to them. Over 96% of the drive is efficient. A novel technique & some of the outcomes are described in this study.

H. Ertl et al. [14] This research shows switched-mode power supply (SMPS class D) current dumping stage in tandem with a linear amplifier integrated power amplifier system. It is possible to avoid the significant loss of standard linear power amplifiers by employing this design. This solution does not need a separate output filter to reduce switching frequency harmonics. Due to its frequent usage, the system's transitory responsiveness is often degraded (often a multi-stage variety). They can avoid the low-frequency distortion caused by the power transistor interlock delay seen in switching amplifiers by employing the switched-mode amplifying linear amplifier system described here. With linear amplifier & class D slave device, this is a master-slave system. The article describes the operating concept, analyses crucial circuit design relationships, and provides simulated findings for the circuit design. Other topologies for switched-mode linear amplifiers are presented, too, as in the last note.

Jih-Sheng Lai et al. [15] High-power applications now have a unique kind of power converter: multilevel voltage source converters. A staircase voltage wave is often generated by mixing numerous layers of dc capacitor voltage in multilayer voltage source converters. Multilevel converters have a major downside in the form of a voltage imbalance between the several levels. To maintain a constant voltage, techniques such as voltage clamping or capacitor charge management are often used. Multilayer converter voltage balancing can be accomplished in several ways. These 3 newly constructed converters for multiple voltage sources: flying capacitors, cascaded inverters, & diode-clamp using various DC sources, are addressed in this research.

They'll go over the basics of how these converters work, as well as their advantages, disadvantages, & prospective uses.

Bakari Mwinyiwiwa, Boon-Teck Ooi [16] Shunt & series VAR controllers, as well as unified power flow controllers (UPFC) in flexible AC systems, have all been suggested to use the Pulse Width Modulation (PWM) approach. When applying feedback controls, nonlinear linear control system theory may be applied more easily when PWM converters are employed as linear amplifiers having a constant gain. In laboratory dummies, both active filtering and pole placement have been effectively tested. Tutorials like this one teach the processes of signal processing, which includes modulation and amplification but not power electronics.

Y. Yoshioka, SKonishi, N.Eguchi. [17] The researchers have established self-commutated Static Flicker Compensator to reduce the flicker which happens in power systems using arc furnaces (SFC). The authors used an analog simulator & a mini-model to test compensating performance of SFC. As a result of these tests, it was found that the SFC output current variance was less than 5%, & the reaction time of current control was around one millisecond. Additionally, they examined the flicker compensation capabilities of a genuine SFC that had been placed in a real power system. With an SFC flicker suppression factor of 36% implemented in April 1995, there have been no issues subsequently.

Fang Zheng Peng et al. [18] For fuel cells and solar utility systems, a novel multilayer voltage source inverter having separate dc sources could provide advantages like flexible AC transmission, static var generation, or power-line conditioners for the correction of phase-shifting & voltage balancing. Each full-bridge in the new M-level inverter has its dc source: (M - 1)/ 2 single-phase full bridges. Only one switch per cycle is required to obtain a nearly sinusoidal waveform voltage from this inverter. Conventional transformer-based multi-pulse inverters have size & weight issues, whereas flying-capacitor & diode-clamp inverters have component count issues. New inverter architecture for SVG systems is explored via analysis, modeling & experimentation to illustrate its advantages.

Frank M. Flinders, Peter J. Wolfs, Member [21] It is shown how to create a control system for an amplifier with a 45-kVA current source & a dc to 10 kHz bandwidth appropriate for geophysical research. A four-switch modified bridge topology was used to build a five-level modulation method. Switching ripple & control performance is improved by a factor of ten over 2-level modulation using this method. A 20 kHz, -3dB bandwidth may be readily created with a 50 kHz switch frequency with this approach. The results of tests on a tenth-scale model and a simulation are shown. For dc to 10kHz frequency range, current output waveform reproduction quality is excellent.

Mario Marchesoni [22] High-power converters provide a wide range of challenges, and a multi-level strategy seems to be the best way to address them. To achieve acceptable switching utilization, high accuracy in steady-state operation & outstanding dynamic responses, new current control algorithms have been designed. Many dc potentials have been used to their utmost potential. The digital simulation findings & associated control systems are given & debated.

Nam S. Choi et al. [23] Multilevel voltage source inverter circuit topologies up to five levels are described as a generalized circuit architecture depending on direct extension of the 3-level inverter to higher levels. As a result, harmonic reduction & full utilization of semiconductor devices as GTOs may be achieved with the suggested multilayer inverter that is capable of implementing any multilevel PWM scheme. Capacitor voltage balancing is addressed, & a circuit solution is also provided.

Akira Nabae et al. [25] novel neutral-point-clamped (NPC) PWM-based inverter has been created, consisting of primary switching devices which act as PWM switches & supplementary power devices which clamp a terminal output potential to NP potential. When compared to a traditional type, this inverter output has reduced harmonic content. Analytically & empirically, two inverters are compared. This inverter also uses a novel PWM approach that is suited for an ac driving system. The novel PWM method's neutral-point clamped PWM inverter has a high drive system performance, together with motor performance, & is suitable for wide-range variable-speed drive systems.

T.a.Meynard et al. [27] High-voltage power conversion is the primary focus of this project. The benefits and drawbacks of traditional serial connection and 3-level voltage

source inverter approaches were examined and contrasted. This paper introduces a novel adaptable multilevel commutation cell; it is depicted with this new architecture is safer, easier to regulate, & produces purer O/P waveforms. Researchers demonstrate how this approach may be used on choppers or voltage-source inverters & how it may be expanded to any number of switches.

A. Ravi [28] This research describes a grid-connected PV system's 3-phase, 5-level neutral clamped inverter. Using MPPT, every DC link voltage level may capture maximum power from PV array. Fuzzy logic controllers are used to solving MPPT algorithm. As a consequence, no DC-DC converter is required, &O/P is exact & responsive. A digital PI current control approach is utilised to keep grid current sinusoidal & achieve high dynamic efficiency with little THD while maintaining constant voltage. A MATLAB/Simulink validation of system's validity is performed, & the findings are compared to those of 3-phase, 3-level NPC inverter connected to grid to calculate THD.

Anup Kumar Panda [29] The multilayer inverter is among the most important breakthroughs in power electronics in current years. The quality of output power may be improved by utilizing this idea in the power conversion process. Cascade H-bridge multilevel (CHBMLI) is an outstanding inverter in this situation because of its modular form, its ability to be simply created by connecting similar H bridges in series, & its ability to provide near sinusoidal voltages with just fundamental frequency switching. Many applications, such as medium-range of voltage industrial motors, electric cars, & grid connections for photovoltaic cell generating systems, use the CHBMLI architecture because of its adaptability. Since every H-bridge requires individual DC voltage source, cost & dependability of a cascaded multi-level converter are both hampered by this need. This shortcoming serves as the driving force for the current project. Different CMI-based topologies with decreased dc sources are investigated in this article, & eventually, the suggested CMI with a single DC source is shown by using low-frequency transformers. The suggested system is smaller & more reliable than standard topologies while also reducing size. Prototype tests are carried out to test the suggested architecture's performance & appropriate findings are reported.

Ebrahim Babaei [30] Switches are decreased, gate driver circuits are isolated, & voltage is practical to switches of cascaded multi-level inverters in this research. The topology that has been presented reduces installation space & costs while also making the control system simpler. Sub-multilevel inverter blocks are joined in series to form this design. In addition, 3 strategies for finding magnitudes of DC voltage sources have also been discussed. It has been shown via simulation & experimentation that the analysis is accurate.

Feel-soon Kang [31] For standalone solar inverters which employ half& full-bridge cells as well as cascade transformers, it suggests a modified multilevel inverter. An earlier inverter (3n-1 + 2) is required for the circuit. A half-bridge cell replaces one of the preceding inverter's full-bridge cells. A simple modification to the inverter's design provides three fascinating benefits. Just to name a few benefits, it might raise the quantity of output voltage levels while also improving the value of those voltages produced. Secondly, by using a half-bridge cell, it is possible to minimize two power switches. Thirdly, it may lower the power used by a transformer linked to a half-bridge unit. For example, a transformer attached to a low switching inverter generates the fundamental O/P voltage levels, whereas transformer connected to high switching inverter enhances the final O/P voltage waves. This is good in terms of performance & efficiency. It evaluates proposed inverter's efficiency as stand-alone solar inverter by comparing it to previous inverter. Computer-aided models & experimental findings validate the suggested inverter's validity.

N.A. Rahim [32] Using a revolutionary dual reference modulation method, we present our single-phase, 5-level grid-connected PV inverter in this article. An offset of the same magnitude as the triangular carrier signal serves as reference for generation of PWM signals. Both inverters & the auxiliary circuit use a full-bridge inverter or switch. The inverter's O/P voltage levels are 0Vdc, 1/2Vdc, Vdc, 1/2Vdc, & Vdc, respectively. With the DSP TMS320F2812, good dynamic efficiency & reduced THD may be achieved by using a digital PI current control method. Using modeling or a prototype, the suggested inverter is shown to be accurate & efficient. Using single-phase 3-level grid-connected PWM inverter, THD values were compared.

IlhamiColak [33] M-level inverter topologies & control systems have been examined in this work. More and more medium and high-power applications are using multilevel inverter systems because of their numerous benefits, including low harmonic content, low EMI outputs, and low power dissipation on power switches. Additionally, the switching strategy used to regulate the inverter will play an important part in eliminating harmonics and providing the optimal output voltage. In open-loop of inverters, much research has been done on carrier-based, space vector, sinusoidal, & sigma-delta PWM approaches. According to the inverter's power requirements, the architecture & control approaches used may differ. This study, as well as the review findings, provides a valuable framework for selecting the appropriate inverter architecture & control strategy for various application sectors.

Ebrahim Babaei[33] In recent years, numerous researchers have focused on multilayer inverters. Because of several benefits, like better output power quality, this is a portion of reason. The O/P voltage from the multiple inverters is almost sinusoidal. Voltage output quality relies on the inverter's counting of output voltage levels. In this study, cascaded multilevel inverter architecture with fewer switching components is proposed and examined. Because it is a universal topology, the suggested topology may be used to create any kind of multilevel inverter; additionally, it is demonstrated that while constructing a cascaded m-level system, a variety of factors, including the quantity of switching devices and quantity of output voltage levels, may be taken into consideration. The suggested multilevel inverter may also be developed from the typical CHB m-level inverters (both symmetric & asymmetric). Mathematical proofs are also provided for some aspects of standard CHB topologies. Trinary CHB topology is shown to be optimal topology when asymmetric conditions exist, for example. Thirteen-level inverter has been modeled & experimentally constructed to validate the suggested architecture.

AlaaeldienHassann[34]One of most important needs for some industrial applications is the use of multilevel DC/AC inverters (MLIs). MLIs have replaced traditional inverters in academic research because of their several benefits over conventional inverters, such as the following. There are many stages in the output voltage waveform, which makes it possible to remove harmonics & produce clear and clean waveforms,

& lessen voltage stress on switching devices. In terms of total cost, MLIs have a bad grade for switching devices, which has a substantial influence. To decrease power losses and increase efficiency. Higher & lower switching frequencies can be used with MLIs. Researchers in the area of multilevel inverters have a major challenge: figuring out how to create a topology that employs the fewest possible components while yet achieving great efficiency. This study provides an overview of the many MLI topologies which have been studied over the last two decades, highlighting the advantages & disadvantages of every. It has been detailed how the MLI topologies were evaluated using a set of performance metrics.

N. Prabaharan [35] With an asymmetric dc source configuration, this study proposes novel architecture for Multilevel-Inverter (MLI) with decreased switch count. Adding two switches with DC sources doubles O/P voltage of m-level inverter depending on switched dc sources. Filtering isn't as necessary since the output voltage has more levels. The suggested asymmetric inverter's operating concept is shown by the single-phase fifteen-level inverter model. Modulation indices are studied in terms of their harmonic content. As compared to trapezoidal and sine wave modulation (SPWM), inverter performance is examined in terms of THD, fundamental rms voltage (Vrms), and Crest Factor (FF) (CF) MATLAB/SIMULINK is used to assess the simulated results.

Natarajan Prabaharan [36] MLIs, or m-level inverters, have recently gotten improved attention in academia & business due to their emergence as a viable technology in a variety of fields. To connect renewable energy sources with high power & high/medium voltage systems, MLI was established. Research towards the development of a reduced switch MLI architecture has accelerated during the last decade, although no comprehensive overview of the issue has yet been published. Thus, this study concentrations numerous reduced switch MLI topologies, which may be divided into 3 categories: symmetric, non-symmetric, & mixed. To better comprehend the fundamental characteristics of MLI topologies, the relevant information about these topologies is meticulously collected using 3 categories in comparison tables. In addition to increasing voltage levels to enhance quality of power, these arrangements also minimize the need for passive filters. Additionally, this paper provides an in-depth look

at the different modulation and control methods available for MLI topologies. Mathematically, the MLI's many performance parameters and computation methodologies are also explored in detail. FACTS, motor drives, & renewable energy applications will benefit from this review's discussion of MLI topology.

Ebrahim Salari [37] Advances in power electronics area allow for the introduction of new & improved multi-inverter topologies to be introduced. For example, a minimal number of switches, good staircase sinusoidal output voltage, and a small inverse voltage peak are all intrinsic benefits of such designs. Here, an innovative modular asymmetrical multilevel inverter is given, which reduces component count and therefore creates a cost-effective structure with outstanding voltage step-generating capabilities. The suggested structure can deliver a high-step staircase sine wave without requiring a large increase in the number of semiconductors. Consider the fact that the suggested structure's symmetrical condition also requires less number of switches than previous symmetrical structures. Finally, the proposed multilayer inverter's correct functioning & voltage-step production capabilities have been proven using MATLAB/SIMULINK & experimental findings.

K.Gobinath [38] It is among the most popular developments in power electronics to use a multilevel inverter. Several dc sources are utilized as inputs to the multilayer inverter to create the required output voltage waveform. Here, we'll show you 2 methods for enhancing voltage quality as well as energy efficiency. Firstly, a new unique architecture for multilevel inverters is developed that minimizes number of switches compared to others for same amount of O/P voltage. Secondly, the SHESW technique is utilised to eliminate lower-order harmonics. To regulate inverter power electronics switches, the inverter employs a fundamental switching strategy. Any number of layers may be accommodated by the suggested topology. Compared to a normal CHBMLI, the number of switches utilized when the levels were raised is minimized. Seven-level inverters are the topic of this research. It was decided to employ just seven switches in the design. As a result of choosing the correct switching angles, harmonics are reduced. As a result, it is well-suited for industrial use since it offers the promise of reducing initial costs & complexity. There are no third or fifth-level

harmonics in this work. The suggested technique is validated by MATLAB simulations, & a THD comparison is supplied for further research.

Adel NazemiBabadi [39] A lower harmonics staircase pseudo sinusoidal voltage waveform by minimal THD may be generated using multilevel inverters. A significant number of switches & power supplies might be required in such topologies. As an outcome, converter's cost & volume grow up, & the control algorithms get more difficult. For small power-conversion units, there has evolved a new branch of multilevel converters, which employ lower number of active or passive components than other topologies. A novel reduced-structure multilevel converter, known as Packed U-Cell, has just been published in literature to minimize number of parts required for production. Packed UCell has fewer active switches than its predecessors, making it more efficient. This design has several drawbacks, including high voltage stress on switches & restricted efficiency in low-voltage applications. There is a limit on the maximum voltage that can be produced. Asymmetrical source-ratio topologies have been described in the literature, but no systematic investigation of cascaded setups using changed structures or alternative symmetrical or asymmetrical source ratios has been carried out. According to the findings of this study, there are 2 methods for dealing with PUC issues. PUC efficiency in relation to total blocking voltage switch ratings & high-voltage applications is improved by using the conventional converter's redesigned design as a starting point for cascaded topologies. As a result, the design of an innovative 147-level cascade inverter & 49-level modified structure depending on a traditional PUC are studied to determine the best feasible topology. Finally, laboratory prototypes are used to conduct experimental validations.

Kannan Ramani [40] Multilevel converters (MLI) have been popular in recent years because of their failure management, modularity, reliability, & multi-stepped O/P waveform with decreased THD. In this research, stepped sine waveform is created using an inverter design with fewer switching components. To decrease the total number of conducting switches for every O/P voltage level, series and parallel switch configurations are employed. A comparison of this topology with another one from the literature is also included. Simulated findings utilizing MATLAB/Simulink are

compared to experimental data obtained from a prototype model to confirm the suggested topology.

Y.Sai.Bhargav[41] MLDCI with a decreased number of IGBTs is proposed in this study. In high-voltage & high-power applications, an MLI decreases size & quantity of passive filters while maintaining low switching losses & low total harmonic distortion. There are 10 switches, 3 DC voltage sources, & 2 diodes in the suggested diode-clamping architecture for a total of 15 levels of output. H-bridge & diode clamped inverter topologies are combined in this novel multilevel inverter design. In addition to achieving high power ratings, this suggested solution may be implemented using renewable energy sources. As a result, it reduces switching losses, the number of power electronic switches required & costs. Total harmonic distortion may be reduced by reducing low-order harmonics. It will be possible to mimic a 15-level inverter using Pulse Width Modulation methods. MATLAB/Simulink will be used to make modifications to the platform.

AtaollahMokhberdoran [42] Increasingly, high-power applications use multilevel inverters. The advantages of a multilayer inverter over a regular voltage source inverter have been stated as high & low blocking voltages of semiconductor switches. As the fundamental building component, new multilevel inverter topologies are obtainable in this work. The projected topology is extended by connecting fundamental blocks in series. Both symmetric & asymmetric modes of operation have been tested for the proposed multilevel inverter's performance. In both symmetric & asymmetric modes, a high degree of perfection in voltage level numbers was achieved with a minimum of switching devices. After that, a thorough analysis of the suggested multilayer inverter's losses and Peak Inverse Voltage (PIV) is provided. Continuing, a comparison is made between the suggested topology & the standard one, as well as a newly constructed topology. Finally, a Matlab/Simulink computer simulation is shown, & the findings are verified in a laboratory prototype implementation.

S. Nagaraja Rao [43] Bridge inverters & multilayer DC links (MLDCLs) are utilised to create an innovative 3-phase, seven-level power converter. Cascaded inverters, flying capacitor inverters, and diode-clamped inverters all fall within this category. This

inverter has no extra clamping diodes or capacitors because every stage is constructed in the same way. There is no correlation between voltage levels & number of active switches in CHBMLI. This new CHB inverter is more effective than the present cascaded MLDCL inverter at reducing number of switches and gate drivers required. Multilevel inverters need 2 active switches (m-1) for each level of voltage, while MLDCL inverters require 3 active switches (m+3) for each level of voltage. MLDCL's suggested output is synthesized using the staircase wave, whose properties are closer to the required sinusoidal output than those of the suggested MLDCL. Pulse width modulation (PWM) may improve the efficiency of suggested MLDCL inverter topologies. It also discusses and compares the performance of a novel reference/carrier depending on the PWM scheme for an MLDCL inverter with an old cascading H-bridge multilevel inverter in this study. As a final step, simulation outcomes are provided to assess the performance of both topologies and corroborate the hypothesis. For single-phase, 7-level DC-Link inverter design, a hardware arrangement was developed.

Nandagopal Arun [44] The goal of a novel cascaded multilayer inverter (MLI) is to use fewer switches, improve flexibility, and lower the voltage stress on the system. In both symmetric and asymmetric modes, a new structure generates all odd and even voltages. To synthesize sinusoidal output voltage waveform, a succession of semi-half-bridge cells is linked in a crisscross fashion using switches. Sub-inverters produced from the proposed MLI are cascaded in addition to the suggested architecture to provide more voltage levels while requiring less standing voltage. The suggested MLI or its enhanced version requires fewer semiconductor switches than the cascading H-bridge design. The experimental and MATLAB R2013b-based simulation findings support the suggested structure.

E. Babaei [45] For an asymmetrical cascade multilevel converter, this study provides a new topology. In comparison to previous topologies, the suggested circuit can create more dc voltage levels since it is made up of series-connected sub-multilevel converter blocks. There are fewer DC sources & switches, in addition to reduced losses, installation space, & converter cost with the suggested topology. A DVR without a coupling transformer utilized this converter. Simulation findings suggest that the projected converter-based DVR is able of addressing power quality issues. A single-

phase 147-level multilevel converter has been used to verify the suggested multilevel converter's operation & efficiency.

Marco Rivera [46] Due to their function in high or medium-power applications, multilevel inverters have received lot of interest from academics and research community in recent decades. In this research, complete assessment of newly constructed multilayer inverters is conducted to determine appropriateness of inverters for certain applications. To discover the challenges with creating additional levels at the output, research is conducted on several kinds of multilevel inverters like hybrid, & symmetric, asymmetric modularized multilevel inverters. A description of several challenges in multilayer inverters with decreased switch counts is offered, allowing for the construction of a unique multilevel inverter architecture in the future. Multilevel switching ladder inverter with unidirectional and bidirectional switches has 81 levels of switching. For testing the inverter's ability to handle variations in resistive and impedance loads, MATLAB/Simulink is used. A 110 V, 186.5 W single-phase induction motor is attached to 81-level inverter output for the examination of characteristics. Moreover, the effects of different voltage inputs on the motor are illustrated for speed control.

Mohamad Reza Banaei [47] According to this research, the SHSI (series H-bridge with stacked multicell inverter) may be used to generate all output levels using just a few circuit elements, including switches and the gate drivers associated with each switch. There is a four-fold upsurge in counts of output voltage levels and 2-fold rise in root-mean-square value for a proposed topology compared to typical flying capacitor multicell & stacked multicell inverters. The O/P voltage harmonic content of SHSI is better than that of previously mentioned structures, & this is because the number and rating of elements are reduced, which lowers the cost & installation space requirements while also reducing amount of energy stored and rating of flying capacitors. Four low-frequency switches and a DC supply are all that are required to boost the standard SM inverter's output to these levels of efficiency. The proposed inverter is based on modeling and experimental findings that show it is feasible & performs well.

ArashKhoshkbarSadigh [48] For medium and high-power applications, M-level converters are a viable option. Increased output voltage levels and perceived frequency are mostly to blame. This study introduces a novel flying capacitor multicell converter arrangement. While rms & output voltage levels of FCM & stacked multicell converters are comparable, the recommended converter has a superior output voltage frequency spectrum and does away with halfway dc source as its key advantage. As a result, just 2 low-frequency switches are added to standard FCM converter design, but there is no change to the number of high-frequency switches, capacitor or switch voltage ratings, or the overall frequency at which the high-frequency switches flip. Because it is measured by a modified phase-shifted PWM, projected converter maintains the flying capacitor converter's self-balancing functionality. Power systems computer-aided application design/electromagnetic transients in DC software is used as a model to suggested configuration, & simulation results are shown to demonstrate its efficacy and benefits. In addition, data from an experimental setup is given to further understand the real-world application.

K. Sivakumar [49] During the course of this research, an open-end winding IM drive inverter design is dissected. A standard two-level inverter is linked to one end of an open-end winding IM, and another two-level inverter is connected in series with a capacitor-fed H-bridge cell using the other end of the winding. Comparable voltage space-vector sites are present in this device, just as they are in a standard 5-level inverter. The 2744 space-vector pairings will be distributed throughout 61 unique space-vector locations, according to the technique that has been provided. It is possible to balance any kind of operational environment, even over modulation, because there are so many switching state redundancies. In addition, the proposed design lacks the 18 clamping diodes with varying voltage ratings that are present in the neutral point clamped inverter. This feature is present in the neutral point-clamped inverter. While on the other hand, a 5-level design calls for the utilisation of more than one capacitor bank per phase in order to successfully execute a flying capacitor system. Switch failure in the H-bridge cell can be used in the recommended design to operate a 3-level inverter across the whole modulation range. As a consequence of this change, the dependability

of the system will increase. In order to verify the notion, a five-horsepower, four-pole IM drive is utilised.

Zhongming Ye [50] HFAC electrical distribution devices are now being researched as a potential solution to the control problem. In order to generate high-voltage, high-frequency, and low-current alternating current (AC) buses, these devices use a series of several high-frequency resonant inverters. The first thing that will be looked at is the system's main circulating current. For the purpose of developing a one-of-a-kind control mechanism, the active and reactive current decomposition technique was applied. In the proposed system, there are provisions made for both a voltage feedback loop and a current-sharing control loop. As was mentioned, the active and reactive currents of the current sharing loop can be modified separately from one another. It is possible to reduce the amount of circulating current by ensuring that the active and reactive currents of an equivalent load are distributed uniformly across all of the activated inverter modules. When only the current magnitudes are controlled, this control method works significantly better than the alternative. For the sake of simulation and testing, an HFAC prototype power distribution system consisting of two two-stage resonant inverter modules with 500 kHz and 100 W has been linked in parallel to a 500 kHz 28-V rms HFAC bus through tiny connecting inductors.

CHAPTER- 3

MULTILEVEL INVERTERS

3.1 Multilevel Inverter structures

The fewest amount of voltage levels in multilevel converter topology is three [53]. The multilayer VSC may function as a rectifier or an inverter [54], thanks to the bi-directional switches. As a result, this dissertation uses the term "converter" rather than "inverter" to describe the device. Several (more than two) voltage or current levels may be swapped between input & output nodes of a multilevel converter [55]. A decrease in THD is seen as the number of layers approaches infinity. There are only so many voltage levels that can be reached because of problems with voltage imbalance, the need to clamp voltage, circuit design and packaging constraints, and the complexity of the controller [56].

Cascading bridges with distinct, diode-clamped DC sources [57] and flying capacitance are three of the most often used multilevel converter architectures in industrial applications. This chapter focuses on multilayer inverter designs; however, the shown designs may also be used for rectifying operations. There are several benefits and downsides to multilayer voltage source inverters; therefore, it's important to know which sort of converter is best for a certain application [58]. In the following sections, we'll go through the operation and construction of a few popular varieties of multilevel converters.

VSIs have several levels, and DC-link voltage Vdc may be derived from any device that is able to provide a steady dc supply [59]. As an energy storage device, series-connected capacitors act as nodes to which a multilayer inverter may be linked. All voltage sources with same value are presumed to be series-connected capacitors. Vc=Vdc/(n-1); here, n specifies number of levels, is formula for each capacitor voltage Vc.

Figure 3.1 displays a variable-level inverter phase leg. Power semiconductors work like a switch with multiple positions. To put it another way, a two-level inverter

produces two levels of output voltage in respect to a capacitor's negative terminal, whereas 3-level inverter generates same voltage.

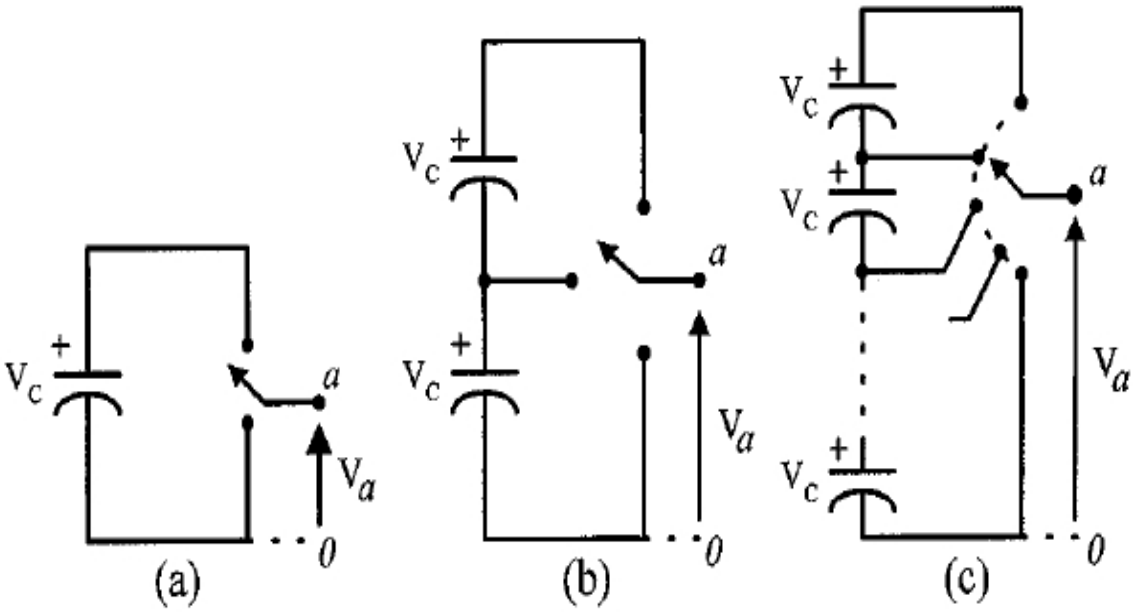


Figure 3.1: Inverter's one-phase legwith (a) 2-levels, (b) 3-levels, &(c) n-levels.

3.2 Diode-Clamped Multilevel Inverter (DCMLI)

To create output voltage steps, diode clamped inverter is most typical multilayer construction. This device clamps DC bus voltage with the help of diode. In 1981, Nabae, Takahashi, and Akagi came up with the idea of a 3-level diode-clamped inverter [60]. 2 sets of switches & diodes make up a diode-clamped inverter. Diodes provide each switch pair's halfway voltage. In 3-level inverter, a common DC bus is split into 3 levels so that each phase of the inverter can access it. By connecting DC capacitors C1 and C2 in series, you can split the voltage from the power supply into 3 different voltage levels. Clamping diodes Dc1 & Dc2 set Vdc on each switching device. Assuming a dc connection has a total voltage of Vdc and a half-voltage midway, voltage across every capacitor equals Vdc/2 (Vdc1 = Vdc2 = Vdc/2). With 3-level diode clamp, an inverter may choose between 3 modes for applying the stair case voltage to DC link capacitor output voltage. Three-level inverters have two switches that are always active [61]. In 5-level inverter, four of the switches are always on, and so on. An inverter with three or five levels of diode clamping is shown in Figure 3.2.

Table 3.1: Changing state of 3-level clamped diode inverter on one of its legs

Switch Status	State	Pole Voltage
S_1=ON,S_2=ON S_1=OFF,S_2=OFF	S=+Ve	$V_{ao}=V_{dc/2}$
S_1=OFF,S_2=ON S_1=ON,S_2=OFF	S=0	$V_{ao}=0$
S_1=OFF,S_2=OFF S_1=ON,S_2=ON	S=-Ve	$V_{ao}=-V_{dc/2}$

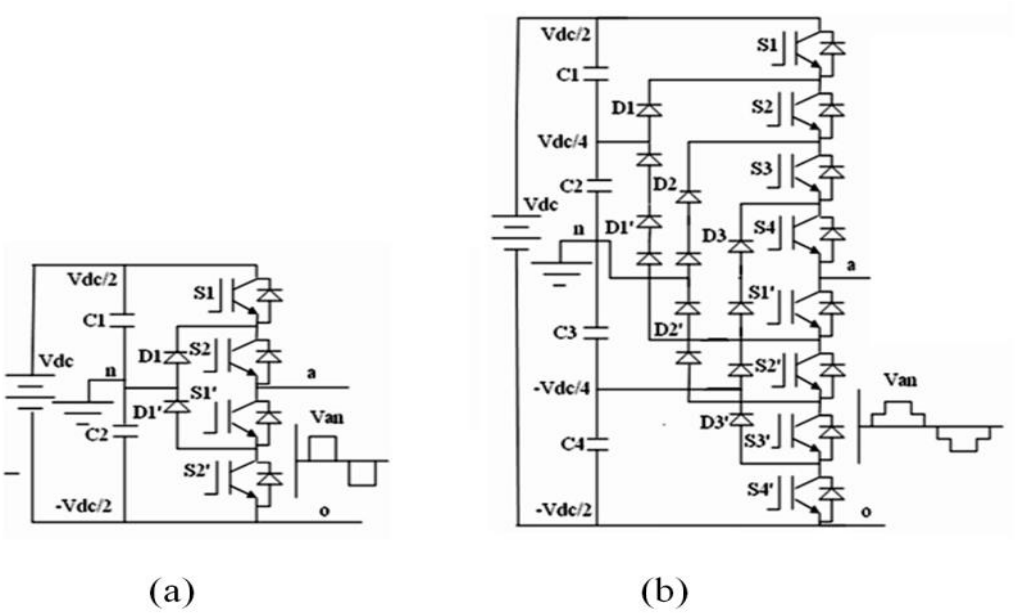


Figure 3.2: Diode-clamped inverter (DCI) architecture (a) 3-level inverter, (b) 5-level inverter.

When it is balanced, phase & line voltages of 3-level inverter are shown in Figure 3.3. Line voltage Vab is comprised of voltages on phase legs a and b. With a three or five-stage inverter, the voltage output exhibits a 5 or nine-level staircase waveform, respectively. For N-level DCI, this means that output phase voltage is N-level, while the out-of-phase line voltage is N-level (2N-1 level). An N-level diode-clamped inverter's DC/volt potential difference across each capacitor is about volts in steady

state (N -1). Although clamping diodes need different ratings to stop reverse voltage, every switching device only needs to block one level of Vdc.

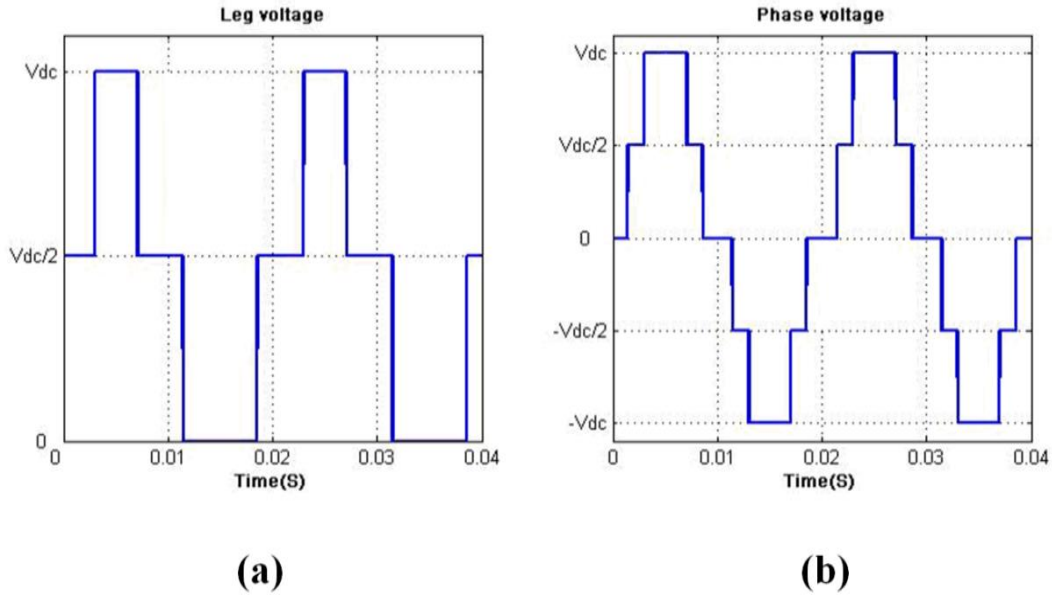


Figure 3.3: Diode-clamped inverter O/P voltage (a) leg voltage (b) O/P phase voltage

For N-level clamped inverters, each leg of the 2(N-1) switching devices needs (N-1) *(N-2) clamping diodes & (N-1) DC link capacitors. An increase in amount of voltage levels consequences in more sinusoidal-looking waveform as well as better-quality output voltage. However, with high-level inverters, capacitor voltage balancing will be the most important problem to deal with. It is impractical to create a system with a high enough number of diodes and switching devices when N is large enough. PWM is used by PWM inverters, so the clamping diode's diode reverse recovery becomes a significant design concern [63].

3.2.1 Operation of DCMLI

Figure 3.2 illustrates a 3-level diode-clamped converter with two capacitors on dc bus (a). Use clamping diodes to limit each device's voltage stress to Vdc/2 for Vdc DC-bus voltage. As reference point for generating staircase voltage, utilise the output phase voltage at neutral point n. To produce voltages with three levels, we may use three different switch combinations across a and n.

- Voltage level $V_{an}= V_{dc/2}$, turn on the switches S_1andS_2.
- Voltage level $V_{an}= 0$, turn on the switches S_2 and S_1' .
- Voltage level $V_{an}= - V_{dc/2}$ turn on the switches S_1', S_2

Fig. 3.2 displays a 5-level diode-clamped converter's DC bus (b). Clamping diodes restrict each switching device's voltage stress to one capacitance level at Vdc. Vdc/4 across each capacitor. Listed in table-3.2 are the many states of 5-level inverter.

Table 3.2: Five-level diode clamped inverter has one state-changing leg.

Voltage V_{ao}	Switch state							
Voltage V_{ao}	S_1	S_2	S_3	S_4	S_1''	S_2''	S_3''	S_4''
$V_{ao}=V_{dc}$	1	1	1	1	0	0	0	0
$V_{ao}=Vdc/2$	0	1	1	1	1	0	0	0
$V_{ao}=0$	0	0	1	1	1	1	0	0
$V_{ao}=-V_{dc/2}$	0	0	0	1	1	1	1	0
$V_{ao}=-V_{dc}$	0	0	0	0	1	1	1	1

It is helpful to think of n as an output phase voltage reference point when discussing what goes into creating the staircase voltage. For the purpose of generating five different levels of voltage [63], we may use five different switch combinations.

- Voltage level $V_{an}= V_{dc}$; turn on all upper switches S_1, S_2, S_3 and S_4.
- Voltage level $V_{an}= V_{dc/2}$, turn on the switches S_2, S_3, S_4 and S_1'.
- Voltage level $V_{an}= 0$, turn on the switches S_3, S_4, S_1' and S_2'.
- Voltage level $V_{an}= - V_{dc/2}$ turn on the switches S_4, S_1', S_2', S_3'.
- Voltage level $V_{an}= - V_{dc}$; turn on all lower switches S_1', S_2', S_3' and S_4'.

In each phase, we have a pair of complimentary switch pairs. One of the switches must be turned on in order for the other to be turned on, as shown by the complementary switch pair definition S1 and S1′ are the four complementary pairs in this scenario. S2 and S2′ are the other two.

Reverse voltage blocking requires unique voltage ratings for clamping diodes, even though every active switching device only has to block voltage level of Vdc/ (m-1). When lower devices S 2′ - S 4′ are on, D1 must block 3 capacitor voltages (or 3Vdc/4), for example. D2 & D2′ must also be able to block 2Vdc/4 and 3Vdc/4. According to this equation, each phase will need (m-1)* blocking diodes, assuming that each diode's voltage rating is same as that of active device (m-2). It shows a quadratic growth in the value of m. Since some dead time is introduced between gating signals and their compliments in the real implementation, it is possible for both switches in a complimentary pair to be turned off briefly during a transition. Dead time shall be disregarded for the sake of this debate.

3.2.2 Diode clamped MLI Features

1) Blocking Diodes Require High Voltage Rating:
   To avoid reverse voltage, clamping diodes require distinct voltage ratings, even if they simply need to block Vdc/. (m l). When all lower devices S1′–S4′ are on, D1′ must block 3Vdc/4 (5-level diode clamped inverter). D2 and D2 must block 2Vdc/4 and D3 3Vdc/4. Each phase requires (m-1) x (m+1) diodes to obtain active device voltage (m - 2). The value of m increases by four times. It's impractical to build the system if the number of diodes necessary is too great at this point [64].
2) Figure-2 demonstrates that switch S1 only conducts when Vdc = Vao, but switch S4 conducts throughout cycle except when Vao = 0. Switching devices must have varied current ratings to accommodate the uneven conduction duty. Oversized outer switches and undersized inner switches might occur if inverter is designed to employ average duty for all of its components. There will be 2x (m + 2) outside devices for each phase in the worst-case scenario. It is preferable to traditional transformer coupling multi-pulse converters, which use 6-step operation for each converter, requiring maximum duty in each device and

circulating current across transformers, to use unbalanced conduction duty.

3) Capacitor Voltage Unbalance [65]:

   Some conditions call for power converter that can transfer real power from AC to DC or DC back into AC. Varied capacitances have different charging and discharging times while functioning in a unity power-factor rectifier or inverter. Capacitor charging profile that repeats itself every half cycle results in imbalanced voltages throughout the capacitors' voltage ranges. There are a number of ways to tackle the voltage imbalance issue in a multilayer converter, such as using PWM voltage regulators or batteries to replace capacitors. Use of regulated DC voltage adds to complexity of system and to the overall cost. EMI and switching losses may be reduced by keeping the converter switching frequency low in utility power systems. At zero power factor[66], equal charging and discharging in one-half of a complete charge cycle may balance the capacitor voltages. The converter ensures that reactive power may be transmitted without causing voltage imbalances [67].

3.2.3 Benefits and Drawbacks of DCMLI

Benefits:

1) A single DC bus connects all the phases of converter to decrease the capacitance needs. Using a back-to-back architecture for applications such as high voltage connectors or a variable speed drive is both possible and practicable.
2) Pre-charging the capacitors all at once is possible [68].
3) Fundamental frequency switching has a high rate of efficiency.
4) To prevent the necessity for filters, the number of layers must rise over a certain threshold [69].

Drawbacks:

1. Due to their propensity to overcharge or discharge, the intermediate DC levels of an inverter make it impossible for real power flow to occur [70].
2. For units with several levels, the need for clamping diodes is inversely proportional to number of levels [71].

3.2.4 Conclusion

Using a chain of capacitors, the diode-clamped inverter provides a range of voltages. Infinite expansion of the concept is possible by increasing number of capacitors. A 3-level configuration with two capacitors coupled across the DC bus was the only early description of this design. Additional levels of DC bus were denoted as "neutral point clamped" (NPC) inverters [72]. If number of voltage levels is odd, neutral point cannot be reached; hence this phenomenon is referred to as "multiple points clamped" (MPC)[73]. The diode-clamped inverter solution is restricted to three levels because of capacitor voltage balance difficulties. The three-level inverter is currently widely employed in industrial applications as a result of recent technological advancements.

3.3 Flying Capacitor Structure

Maynard and Foch [74] proposed capacitor clamped inverter, sometimes known as the flying capacitor, in 1992 [75]. Unlike the diode-clamped inverter, this one employs capacitors instead of clamping diodes [76]. Capacitor-clamped switching cells are used to power the flying capacitor. The ladder structure of this architecture's DC side capacitors has voltages that differ from one capacitor to next. The voltage difference between consecutive capacitor legs determines output waveform's voltage steps [77].

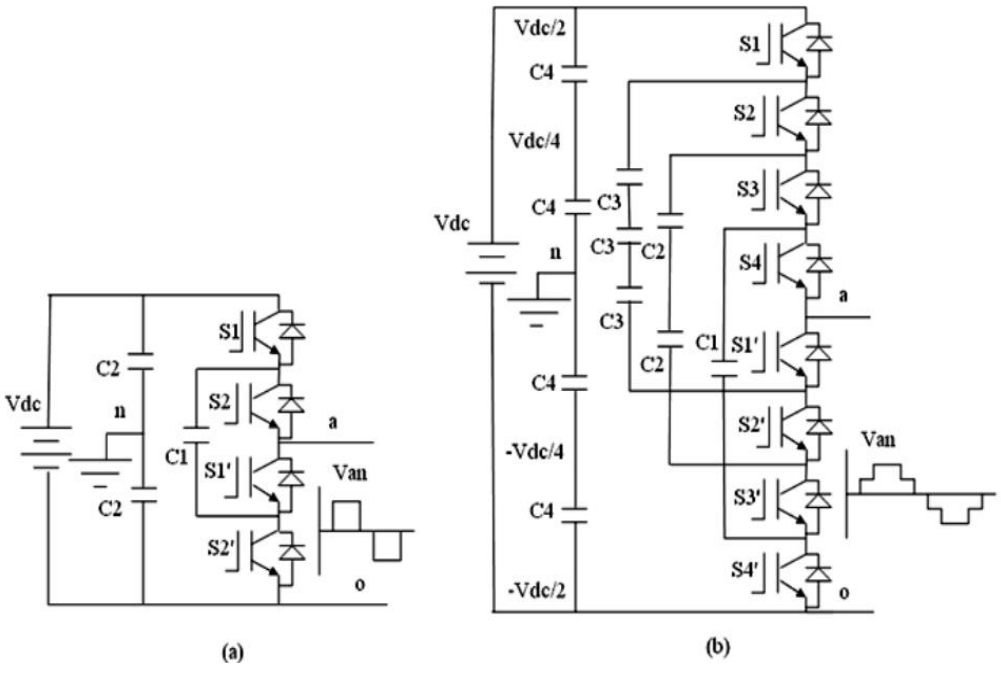


Figure 3.4: displays 3-level and 5-level capacitor-clamped inverters

3.3.1 Operation of FCMLI

All three phase nodes may be connected to any capacitor bank node during the operation of flying capacitance multi-level inverter (FCMLI) (V3, V2, V1). S1′ is linked to neutral point voltage while S1 & S2 are on. On S1′ & S2′, V1 and 2 are linked. Turning on S1 and S1′, charges and drains C1. Correctly picking zero states balances the capacitor's charge. Compared to 3-level diode-clamped inverter, there is one extra switching state. There are two transistor states at voltage level V3. Charge or discharge a capacitor depending on phase's flying capacitor current (Ia) in redundant states. This allows for fine-tuning the capacitor voltage to a desired value via internal phase switching. It is just like the flying capacitor inverter, which has three levels of switching; the highest and lowest switching states don't affect the capacitance. In order to control both capacitors to their optimal voltages, the intermediate voltage levels have sufficient redundant states. Bulk capacitors are required for capacitance clamping, much like diode clamping, to keep voltage in control. N-level converter needs (N-1) * (N-2)/2 clamping capacitors per phase in addition to (N-1) main dc bus capacitors if capacitor voltage rating is same as main power switch.

When using a flying-capacitor inverter, there is no need for all of the switches to be on at the same time. To make matters worse, diode-clamped inverter provides just line-line redundancy, whereas flying-capacitor inverter has both phase and line-line redundancies. Using these redundancies, it’s probable to balance voltages across the different levels by charging or discharging certain capacitors [78].

Capacitor-clamped converters are more flexible than diode-clamped converters in terms of voltage synthesis. Employing switch combinations given in Fig 2.4, output voltage of phase leg "a" with respect to neutral point (NP) n (e.g., Van) may be generated (b).

1) Set the voltage to $V_{an}= V_{dc/2}$ and turn on the S1-S4 top switches.
2) Voltage level $V_{an}= V_{dc/4}$; there are 3 combinations.

a) Turn on switches S_1, S_2, S_3 and S_1'. (V_{an}= $V_{dc/2}$ of upper C_4"s - $V_{dc/4}$ of C1"s).

b) Turn on switches S_2, S_3, S_4 and S_4'. (V_{an}= $3V_{dc/4}$ of upper C_3"s - $V_{dc/2}$ of C_4"s).

c) Turn on switches S_1, S_3, S_4 and S_3'. (V_{an}= $V_{dc/2}$ of upper C_4"s - $3V_{dc/4}$ or C3"s + $V_{dc/2}$ of upper C_2).

3) Turn on the top and lower switches S3, S4 and, S1′, S2 if Van is 0 volts.
4) Voltage level V_{an}= -$V_{dc/4}$, turn on upper switch S_1 and lower switches S_1', S2′and S_3'.
5) Voltage level V_{an}= -$V_{dc/2}$, turn on all lower switches S_1', S_2', S_3' and S_4'.

3.3.2 Features of FCMLI

Using this inverter is a significant challenge due to the high quantity of essential storage capacitors. This means that in addition to main (m1) DC bus capacitors for each phase leg, there will need to be an additional pair of capacitors with voltage ratings equal to the main power switch (m - 2)/2. Because all capacitors are assumed to have same voltage rating, just one capacitor is required in an M-level DCI. In order to do this, one or more basic cycles may utilise switch combinations for intermediate voltage levels (e.g., 3Vdc/4, Vdc/2, and Vdc/4). A flying-capacitor multilevel (FC-MLI) converter may be employed in practice." Consequently, picking switch combinations becomes more involved, & switching frequency must be higher than for actual power conversions [79]. Flying capacitor multilevel voltage source converters have the following benefits and disadvantages [80]:

3.3.3 Benefits and Drawbacks of (FCMLI)

Benefits

This architecture differs from the diode-clamped inverter in various ways, which we'll go over here:

1. Adding more clamping diodes is unnecessary.
2. A switching redundancy is included in the phase in order to counteract flying capacitors [81].
3. Without the use of a transformer, the needed voltage levels may be attained.

Minimizes the converter's price and also reduces the amount of energy lost [82].

4. Contrary to diode-clamped construction, where series string of capacitors all shares same voltage, capacitors inside a phase leg of a voltage source converter with capacitors clamped are charged to different voltage levels.
5. It is possible to regulate the flow of reactive and real power.
6. The inverter is able to survive short-term power disruptions and significant voltage sags because of its large number of capacitors [83].

Drawbacks

1. It is necessary to set up capacitors with a specified voltage level as an initial charge before a converter may be designed by any modulation technique. As a result, the modulation process becomes more difficult, and the converter becomes a bottleneck.
2. Keeping track of every capacitor voltage level is challenging [84].
3. Batteries have to be pre-charged to a certain level before they may be started.
4. Real power transmission is hampered by inadequate switching usage and efficiency.
5. It is difficult to rate the capacitors since they have a substantial proportion of DC bus voltage across them [86].
6. Large number of capacitors required in multilayer diode-clamped converters makes them both more expensive and bulkier than lamping diodes.
7. High-level inverters make packaging more challenging [87].

3.4 Cascaded multilevel inverter

Additionally, a CHB or a SHB are two additional options for multilevel converters. The series H-bridge inverter was first launched in 1975. Two researchers, Lai and Peng, were the first to completely develop the cascaded multi-level inverter. As far back as 1997, they patented and demonstrated the product's many benefits. There have been several uses for the CMI since then. Shunt and series-connected FAC TS controllers benefit greatly from the CMI's versatility and adaptability in high-power applications [88]. Through the combination of several separate voltage levels, the CMI generates output voltage waveforms that are almost exactly sinusoidal in shape. Increased redundancy against H-bridge converter (HBC) failure may be achieved by

simply adding additional H-bridge converters without having to modify the power stage [89]. Using a single-phase complete bridge, the inverter generates one phase. Using a three-phase CMI design with H bridge converters in sequence [90], an AC system's phase may be balanced. The use of a shared DC connection in other VSC designs precludes this functionality. Using series power conversion cells allows for easy scaling of voltage and power [91]. Bridge converters generally employ diode rectifiers to provide the dc link supply, and this is often done by feeding the isolated secondary windings of 3-phase transformer. In medium-voltage systems, phase-shifted transformers may feed cells with high-quality power to the utility connection [92].

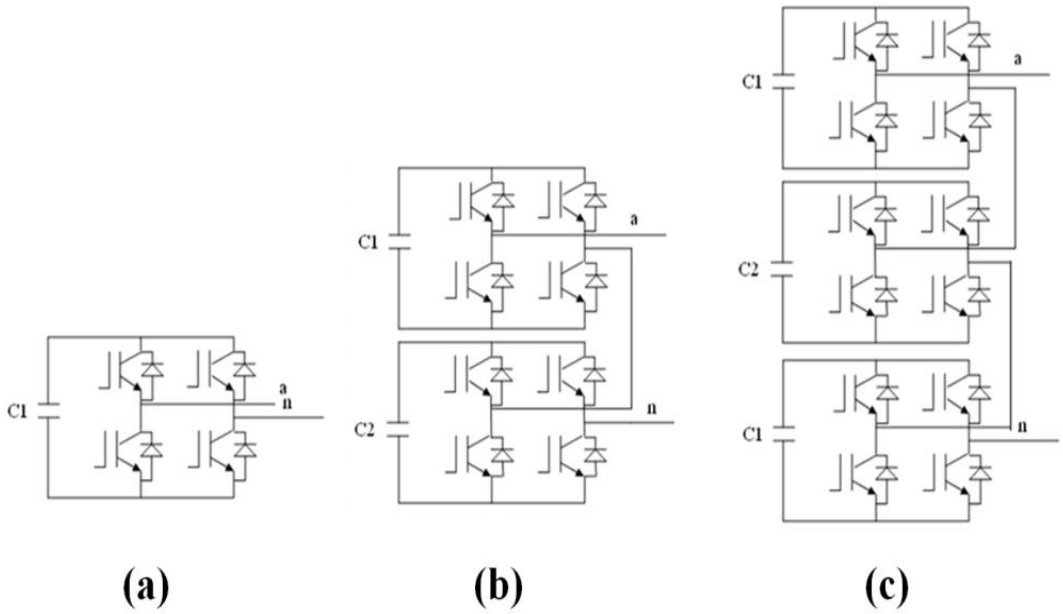


Figure 3.5: Cascaded single-phase inverters (a) 3level, (b)5level, (c) 7level

3.4.1 Operation of CMLI

Converter topology is formed by connecting single-phase inverters with various DC sources in series. Figure 3.6 displays cascaded inverter's power circuit for a single-phase leg with 3, 5, or 7 levels. Total phase voltage is sum of all different cell voltages. In 3-level cascade inverter, single-phase full bridge inverters provide 3 output voltages: +Vdc, 0Vdc, and -Vdc. Using the power switches, you may successively connect the capacitors to the ac side. If you use a three-level inverter, you may get voltage swings of –Vdc to –Vdc; five-level inverters can get voltage swings of -2 to +2, and seven-level inverters can get voltage swings of -3 to +3Vdc. Even without the use of a filter,

the staircase waveform is virtually sinusoidal.

In a three-phase system, cascaded converter output voltage might be wye (Y) or delta (). Fig. 3.6 shows example of wye-configured 7-level converter that makes use of a CMC and separate capacitors.

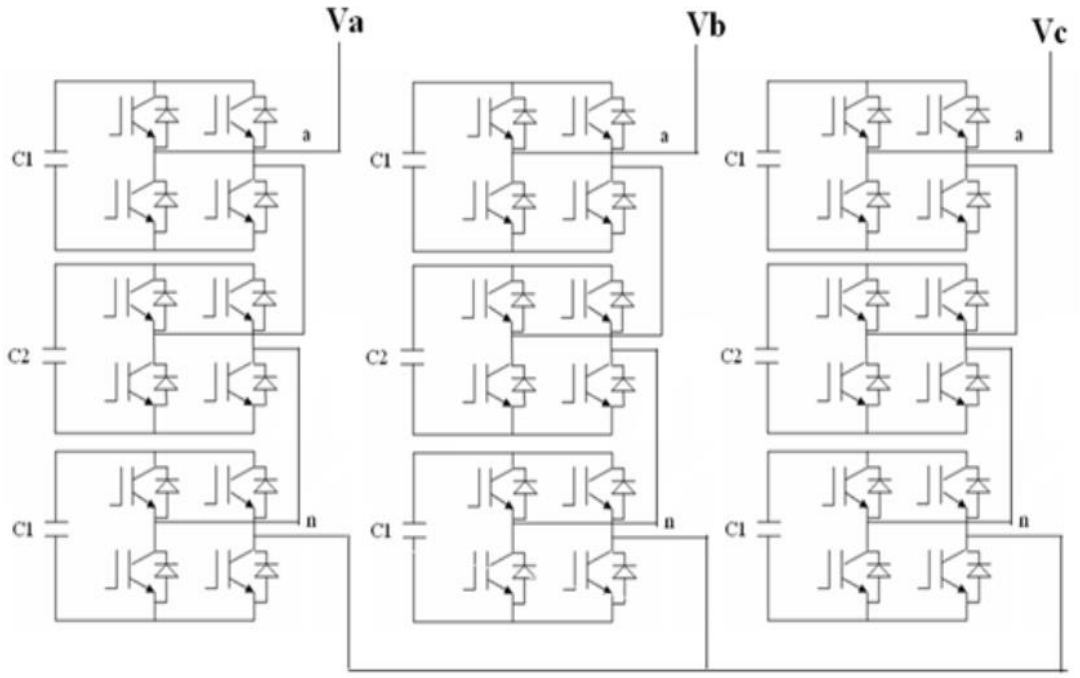


Figure 3.6: Cascaded 3-phase 7-level inverter (Y -configuration)

3.4.2 CMLI Features

Cascaded inverters need unique DC sources for real power conversions. Fuel cells, photovoltaic [92], biomass, and other renewable energy sources may all benefit from independent DC sources. A short circuit should be created if 2 back-to-back converters aren't switching simultaneously; hence connecting independent dc sources between them is not feasible [93]. The following list summarises the benefits and drawbacks of a multilayer voltage source converter based on cascaded inverters [94].

3.4.3 Benefits and drawbacks of CMLI

Benefits

1. DC buses may be easily regulated [95].
2. Control may be broken down into smaller units. Full-bridge inverters with

cascaded models may be modulated independently, unlike diode and capacitor-clamped inverters, which need a central controller for each phase leg.

3. In comparison to other multilevel converters, this one uses the fewest components [96].
4. Soft-switching may be utilised to reduce the need for large and inefficient resistor-capacitor-diode snubbers in this configuration [97].

Drawbacks

1. The reference and carrier waveforms must be synchronised using full-bridge communication.
2. For genuine power conversions, it requires independent DC sources, which limits their applicability.

3.4.4 Conclusion

These multilevel converter topologies will be shown in this chapter. They all have their own pros and weaknesses, but for a certain application, they may be better than the others. According to what has been done previously, certain topologies are selected even though they are not ideal for their intended use. Research and engineering community expertise may outweigh other technology restrictions.

3.5 Emerging Topologies

New multilevel inverter topologies have emerged in part as a result of concerns that the 3 traditional multilevel inverters fall short in some areas [98]. Each of these novel topologies was developed to address a particular problem from the circuit's point of view, including size, weight, cost overall, switching frequency, output quality, efficiency, reliability, power loss, device utilisation, fault-tolerance capability [99], & many more. With slight modifications, the majority of these kinds of topologies were attained from conventional multilevel inverter [100]. Several topologies that fall under this category and are also referred to as developing topologies are presented in this section.

3.5.1 Active Neutral-Point-Clamped Inverter

Power semiconductor loss distribution is unequal in each inverter leg [102] is

one of key problems with diode-clamped or NPC inverters [101]. It was found that during a basic cycle, the outer switches in 3-level NPC inverter conduct for longer period of time than inner switches. For switches that produce high & low losses, this necessitates use of various heat sinks and cooling systems. Additionally, a specific range must be maintained for the output current, maximum power rate, and switching frequency [103]. With the advent of active NPC, a solution was suggested [104]. In this inverter, clamping switches are used in place of the traditional NPC inverter's clamping diodes. Active NPC inverter for 3-level structure is depicted in Figure 3.7[105].

The clamping switches give the neutral current another route. There are2 possible trails for neutral current to pass in order to produce 0 voltage level, to use phase A in Figure 3.7 as an example. The first way involves DA3 & SA2, while 2nd path involves SA3' and anti-parallel diode of SA1' if current flows to load. If current originates from load, 2 pathways may also be used. The distribution of power lost amid semiconductor devices can be regulated by forcing current to flow in the two routes alternately through the appropriate regulation of SA2 and SA3'. As there is a single path in which neutral current can travel, it is evident that the NPC inverter does not exhibit this behavior.

By merging the 3-level active NPC leg & 3-level flying-capacitor cell, a five-level structure based on 3-level active NPC concept has been developed [106]. This pairing enables the integration of the NPC and flying-capacitor inverters' strengths into a superior architecture. One of the five levels of active NPC inverter is depicted in Figure 3.8. Despite active NPC topology's apparent superiority in some areas, the usage of additional switches may result in a control method that is more intricate. It can be difficult to balance capacitor voltages when using flying-capacitor cells [107].

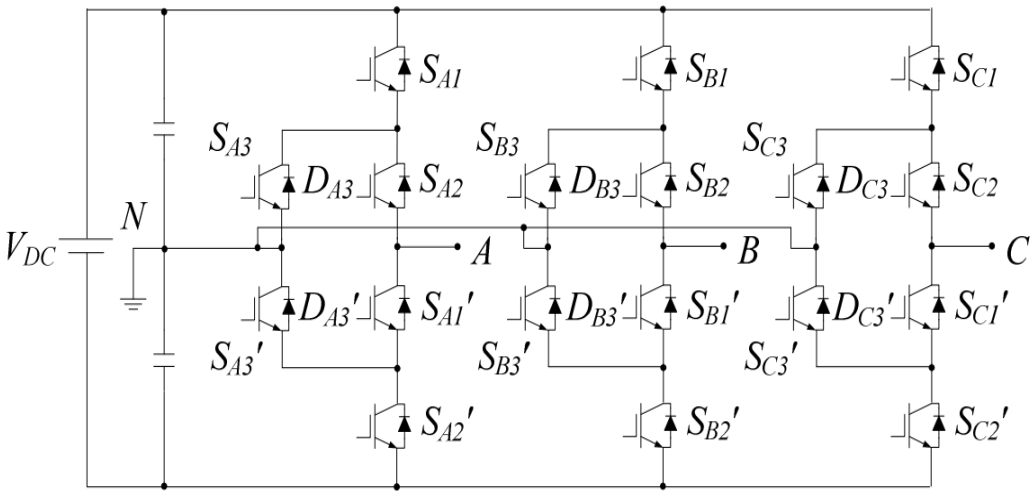


Figure 3.7: 3-phase 3-level active NPC inverter.

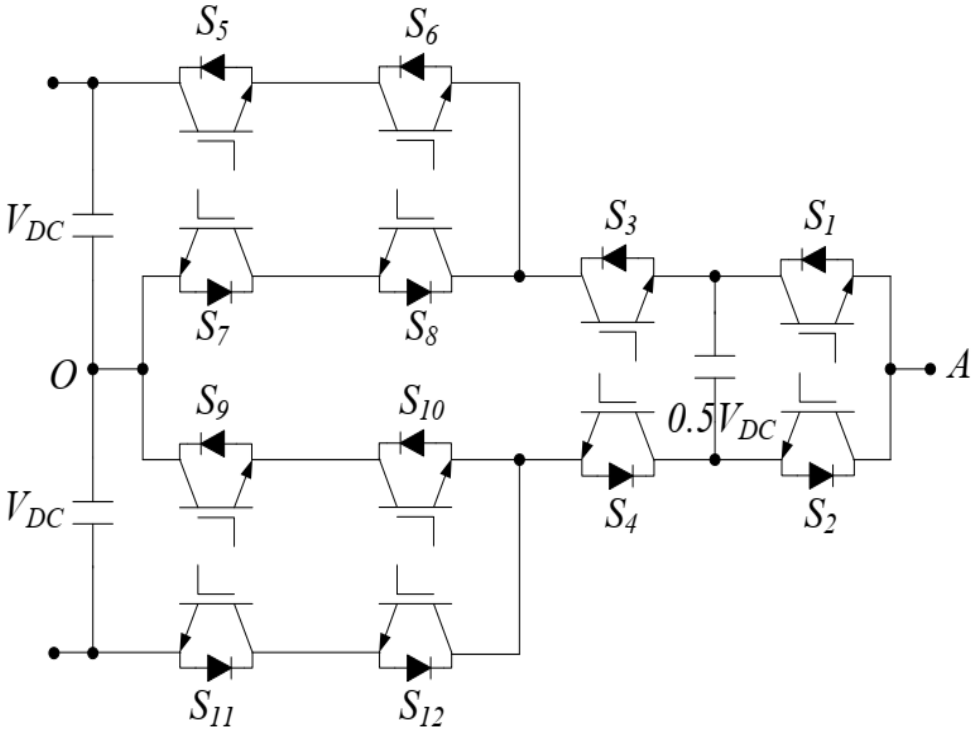


Figure 3.8: One leg of 5-level active NPC inverter

3.5.2 Modular Multilevel Converter

One of era multilevel converters, the Modular Multilevel Converter (MMC or M2C), is designed to convert high or medium-voltage power without the use of

transformers [108]. Particularly in area of high voltage DC or HVDC transmission, this converter has garnered a lot of interest lately [109]. The 3-phase MMC's structure is displayed in Figure 3.9. Both flying-capacitor converter & series-connected HBC are included in this converter [110]. The converter contains six arms, each of which makes up two phase legs. Each arm is made up of an inductor, numerous similar cells or sub-modules connected in series along with other components. The development of full-bridge and clamp-double (DC-MLI) cells has also been done in lieu; half-bridge cells are most frequently used [111]. In the event of short circuit on DC side, inductor offers protection by limiting the AC current. There are two switching states that can be produced for a half-bridge cell. While top switch is ON & lower switch is in OFF state, system is in the on state, which brings about cell output voltage made equivalent to capacitor voltage. If vice -versa takes place, the cell output voltage is zero, which is known as the off state. A multilayer voltage waveform can be produced by connecting the right amount of cells in series and controlling the switching of the cells in two arms of each phase leg. The arm currents are unchopped and flow continuously [112]. The modular structure and the straightforward voltage scaling achieved by connecting cells in series are two appealing aspects of the MMC topology. A filterless system is feasible because the stepped voltage waveform can approximate ideal sinusoid with very low harmonic distortion when large number of cells are included in the architecture. Without sacrificing power quality, the device's average switching frequency can likewise be decreased [113]. The use of numerous semiconductor devices is implied by the rise in the number of cells, though. A suitable voltage balancing control is also crucial for floating capacitors [114].

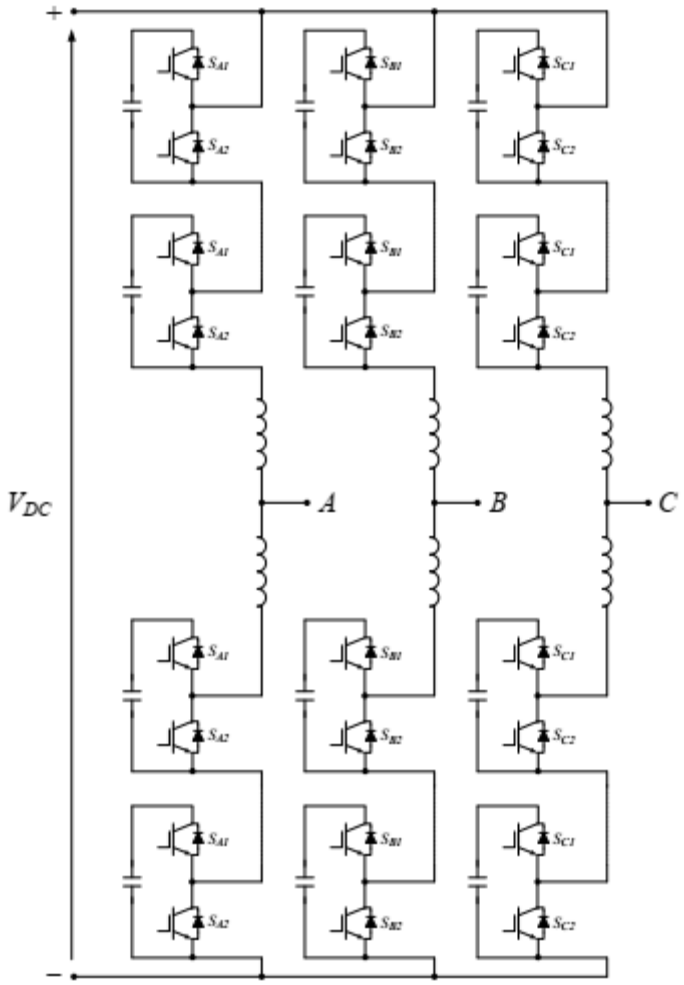


Figure 3.9: Modular multilevel converter

3.5.3 Asymmetric Cascaded H-Bridge Inverter

By using disparate DC voltage sources, it is hypothesised that output voltages produced by CHB inverter can have more levels [115]. The term "asymmetric cascaded H-bridge inverter" refers to this particular type of inverter. An illustration of an inverter circuit can be found in Figure 3.10. Cells 1 and 2 are provided by 2 separate DC voltage supplies, namely, 2VDC & VDC; if we only take one phase, let's say phase A. This results in 7 output voltage levels being produced across nodes A & O as opposed to the 5 levels that are produced when both cells are supplied with equal DC voltage inputs.

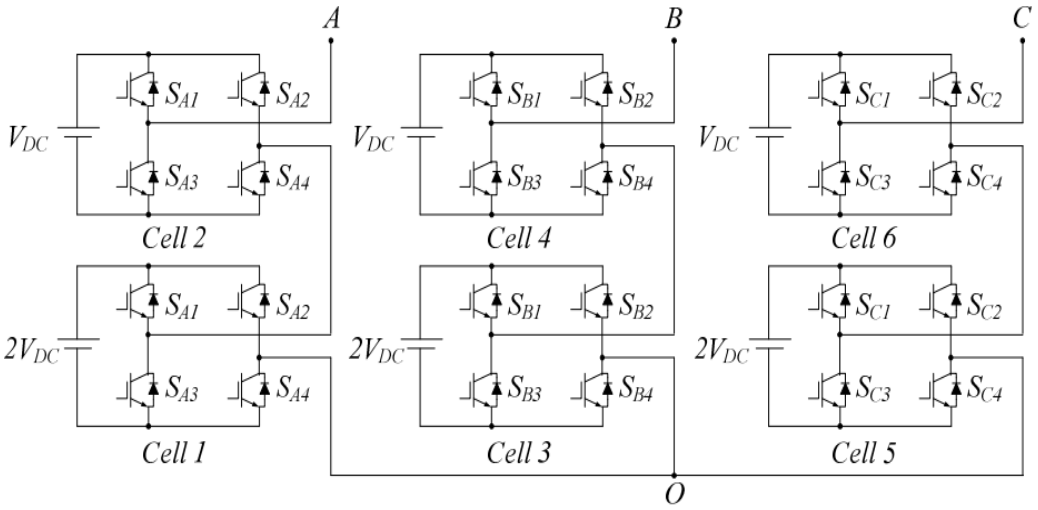


Figure 3.10: 3-phase asymmetric cascaded H-bridge inverter

Voltage ratios in powers of 3 were suggested to upsurge number of voltage levels even more [116]. 3m Voltage levels can be produced for an inverter with this setup and m cells per phase leg [117]. Additionally, a different strategy suggested using capacitors in many cells to cut down on number of distinct DC sources [118]. In a single-phase arrangement, first cell is the only one to use a DC source, and the subsequent cells all use capacitors. However, this method necessitates a sophisticated control technique since capacitor voltage balancing is an extra need that must be addressed. Asymmetric cascaded H-bridge inverters not only exponentially increase the number of levels but also enable high-power cells to operate at low switching frequencies [119], lowering switching losses. Uneven power distribution among cells is caused by use of various switching frequencies by high & low-power cells. To accommodate the diverse properties of cells, numerous switching device categories with various thermal designs are required. Since cells are no longer identical, CHB inverter loses its modularity advantage. Additionally, it is still thought that this inverter has a significant drawback due to the utilisation of two DC sources [120].

3.5.4 Mixed-Level Cascaded H-Bridge (CHB) Inverter

The CHB inverter and the other two traditional multilevel inverters are fundamentally combined to create the mixed-level CHB inverter. This is accomplished by using flying-capacitor or diode-clamped converter cells in place of H-bridge cells

[121]. The quantity of independent DC sources can be decreased in this way. The 9-level mixed-level CHB inverter utilising flying-capacitor converter cells is shown in Figure 3.11. This configuration requires only 6 separate DC sources as opposed to 12 if H-bridge cells were utilised. This explains significant 50 percent decrease in the number of DC supplies. Since flying-capacitor converter cells have 5-level structure as opposed to H-bridge cell's 3-level structure, these cost savings is made achievable. However, using five-level cells increases control complexity [122]. Voltage balance issues must be fixed in the case of capacitor utilisation in the cells.

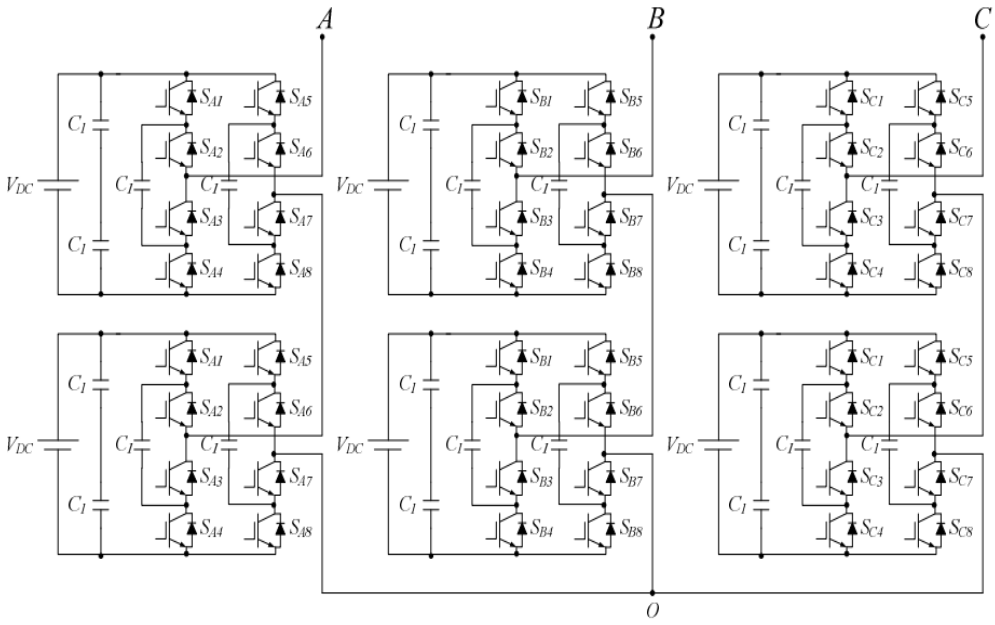


Figure 3.11: Three-phase mixed level CHB inverter.

3.5.5 Hybrid Multilevel Inverter

In order to essentially decrease number of isolated DC supplies in CHB inverters, hybrid multilevel inverters are also introduced, along with asymmetric and mixed-level versions [123]. A hybrid inverter combines 2 distinct topologies into 1 and is anticipated to have better properties & performance [12]. Asymmetric and mixed-level cascaded H-bridge inverters were included in the hybrid inverter family according to this definition in the literature. Figure 3.12 illustrates a new hybrid inverter type where two stages with various topologies are coupled [125]. This inverter connects 3-phase full-bridge circuit, which serves as first stage, to single-phase H-bridge cell per

phase leg, which serves as 2nd stage, by series connection. In the first step, three independent DC sources can be substituted by single DC supply.

The second stage performs the role of an active filter, which improves power quality and lowers common mode voltages [126]. The ratio of the first stage's DC voltage to second stage is changed to get the required counts of voltage levels. In addition, hybrid inverters can generate an even number of voltage levels, which may be required in particular applications to achieve optimal device usage, unlike symmetric/asymmetric cascaded H-bridge inverters, which can only generate odd numbers of voltage levels [127]. NPC inverter has also been used in the first stage to replace the six-switch full-bridge circuit [128]. Capacitors are used in place of DC voltage sources for H-bridge inverter in 2nd stage. The hybrid inverter uses fewer DC sources because of the utilisation of capacitors. Inverter becomes more challenging to control, though and operates in a highly nonlinear manner. Floating capacitors must be controlled specifically [129].

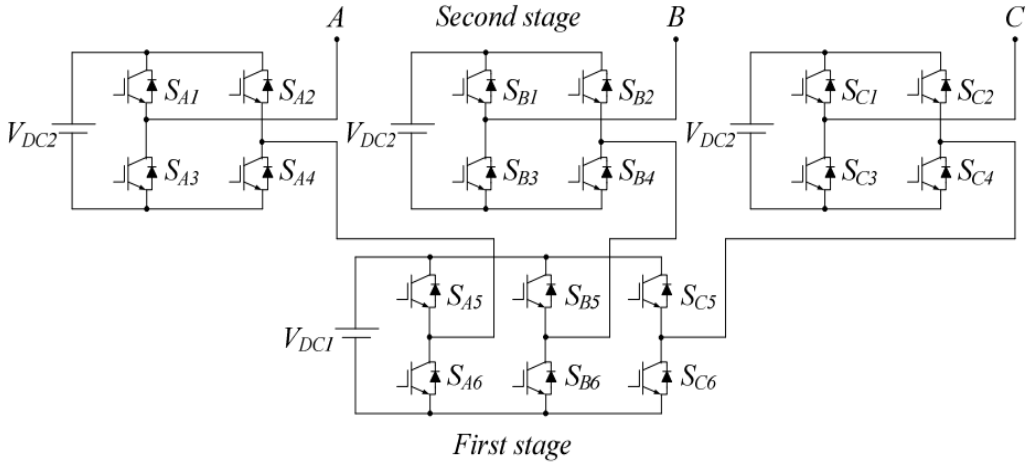


Figure 3.12: H-bridge and 6-switch full-bridge inverters are connected in series to create hybrid inverter.

3.5.6 Multilevel DC Link Inverter

A multilayer inverter with an H-bridge inverter in each phase leg is presented with goal of reducing number of switches, clamping diodes, or capacitors [130]. A series connection of several half-bridge cells can be used to create the multilevel DC

link, as displayed in Fig 3.13. There are 2 switches in each cell, and they work in unison. By turning on one switch and shutting off other switch at same time, DC voltage of each cell is added to or bypassed [131]. Adding voltages across each cell yields DC link voltage between nodes M and O. The switches in each cell must operate with distinct duty cycles at twice frequency of output voltage to achieve DC link voltage with staircase-like structure across 2 nodes [132].

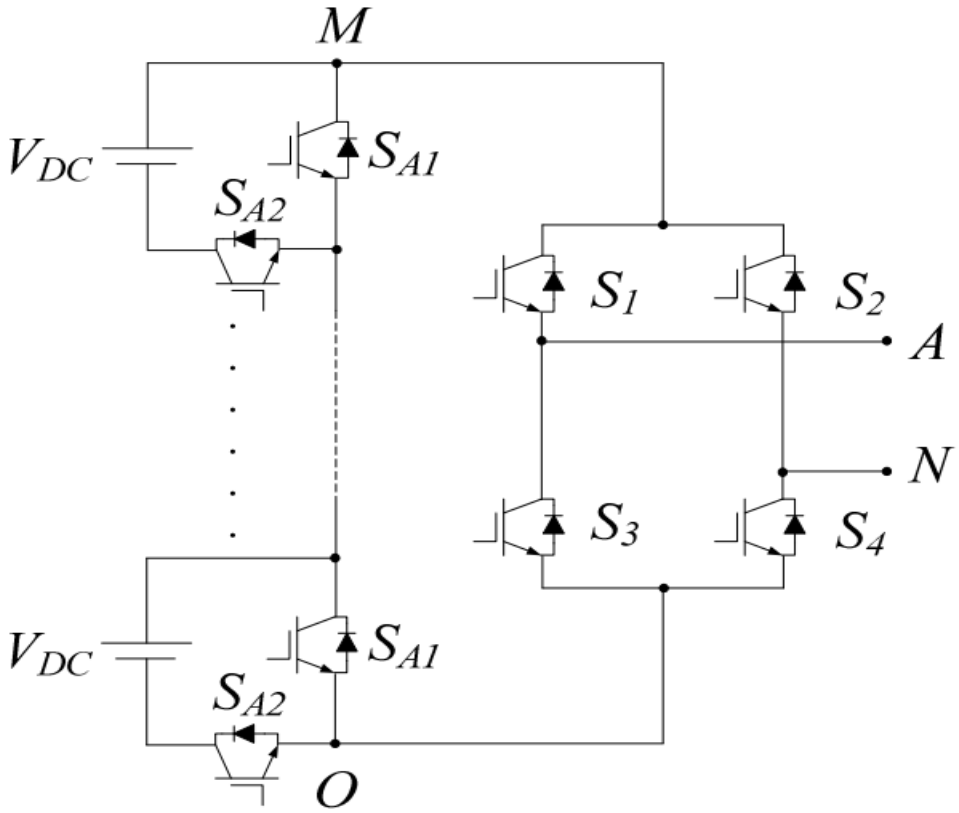
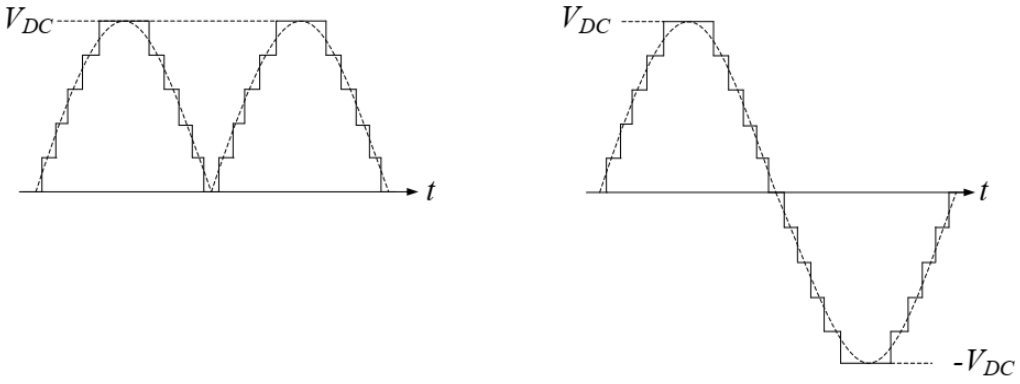


Figure 3.13: 1-phase leg of multilevel DC link inverter based on CHB Cells.

Rectified waveform of a commanded sinusoidal wave can be roughly compared to staircase voltage waveform of DC link [133]. The DC link staircase waveform is alternatively reversed in polarity using the H-bridge inverter at frequency equal to output voltage to convert into an AC voltage. Waveforms for output of multilevel DC link inverter, VAN, and DC link, VMO, are displayed in Fig 3.14. For multilevel DC link inverters, as number of voltage levels m rises, number of active switches also rises in accordance with (m + 3) per phase leg as opposed to 2(m - 1) for traditional multilevel inverters. The staircase DC link voltage can also be produced utilising diode-clamped and flying capacitor phase legs in addition to the series-connected half-bridge cells.

Figure 3.15, for instance, depicts a multilevel DC link inverter built on a phase leg with a diode clamp that can produce 11 voltage levels across nodes A & N. Additionally, multilayer DC link inverters can be used with unbalanced voltage sources [134]. The inverter still needs numerous distinct DC sources despite the benefit of fewer switches. If diode clamped or flying-capacitor phase leg is utilized [135], capacitor voltage balance is another problem that needs to be solved.



(a) DC link voltage waveform, *VMO* (b) Output voltage waveform, *VAN*

Figure 3.14: Voltage waveforms of DC link and inverter's output.

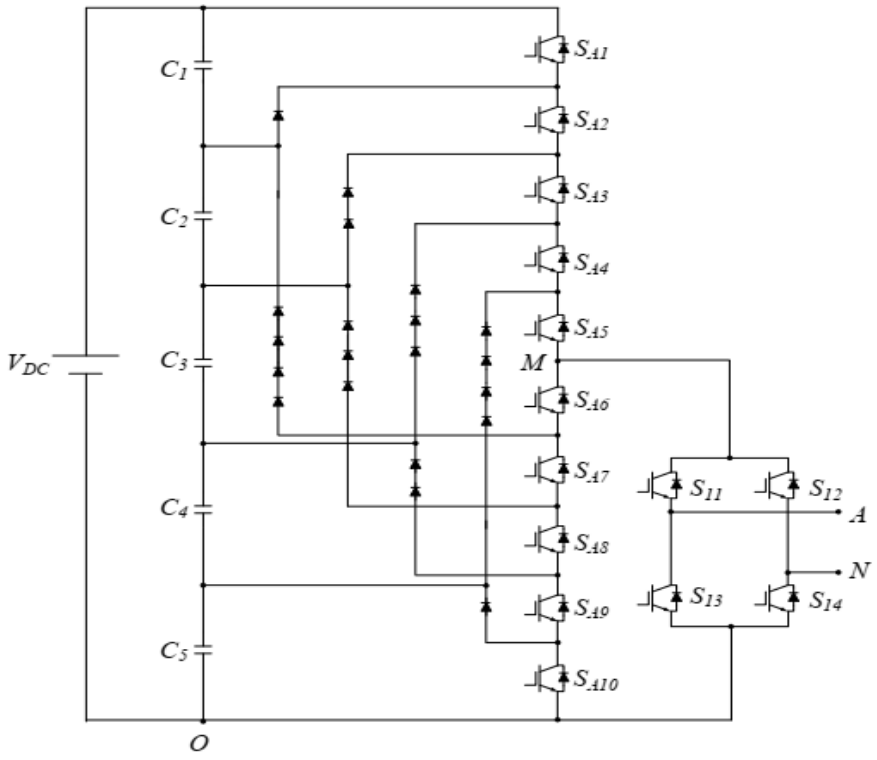


Figure 3.15: One phase leg of diode-clamped-phase-leg-based multilevel DC link inverter.

3.5.7 Transistor-Clamped Multilevel Inverter

The principle of a diode-clamped converter is utilised to create transistor-clamped multilevel inverters [136]. In transistor-clamped inverters, clamping diodes aren't required because bidirectional switches are employed to secure connections between main switches & capacitors. Figure 3.17 [137] shows one type of bidirectional switch that is used. There are four diodes and one transistor in the bidirectional switch. Five voltage levels can be produced at output by adding one of these bidirectional switches to a single-phase H-bridge inverter in configuration displayed in Fig 3.17 [138]. Additional research on the inverter has been done for photovoltaic applications [139]. By simply adding another bidirectional switch, the inverter can be further modified to provide an output voltage waveform with seven levels [140].

Figure 3.18 [141] depicts a 3-phase variation of 3-level transistor-clamped inverter (TCI). A different kind of bidirectional switch is utilised for this inverter. Two transistors, two diodes make up the switch. The inverter's construction resembles that of the corresponding NPC inverter [142]. The TCI is able to distribute losses across devices more evenly than NPC inverter, which suffers from an uneven loss distribution among devices [143]. This makes inverter appropriate for variable high-speed applications by enabling it to operate at high switching frequency.

However, as more switches are needed, the price rises significantly.

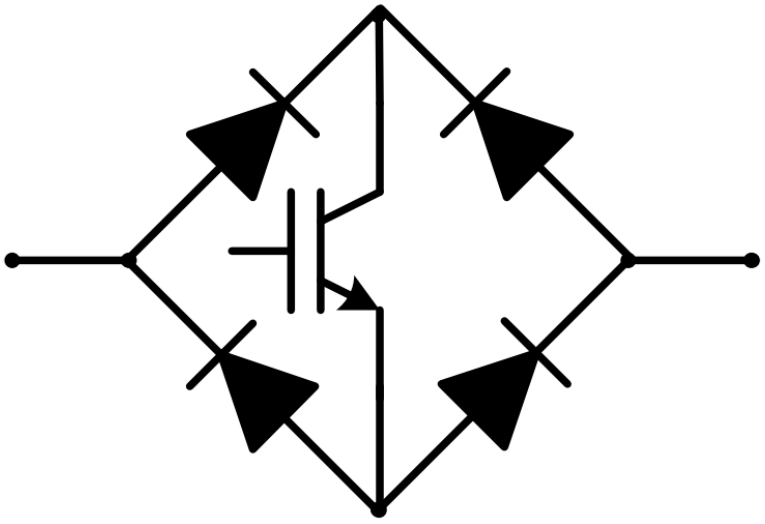


Figure 3.16: One type of bidirectional switch.

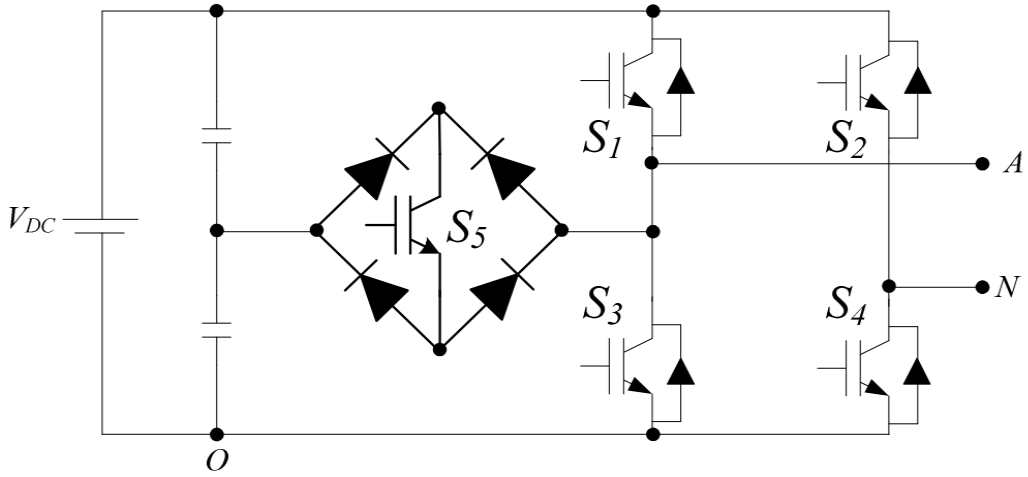


Figure 3.17: H-bridge inverter with single-phase transistor clamping.

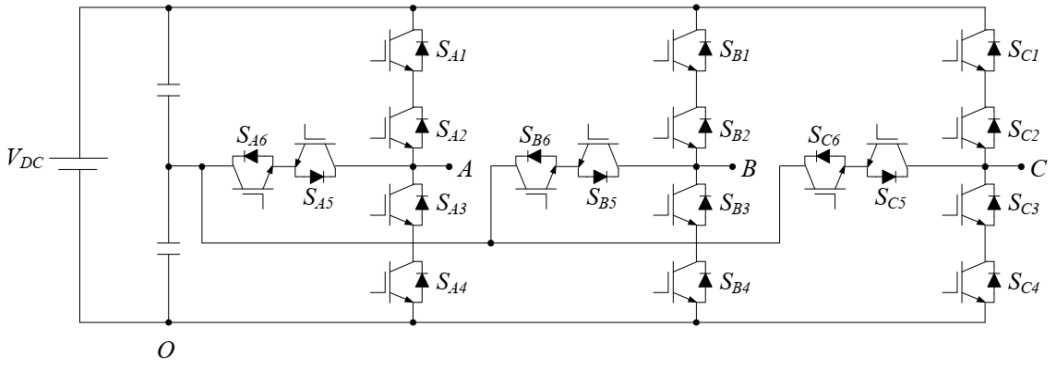


Figure 3.18: A 3-phase 3-level transistor-clamped inverter.

For medium voltage drive applications, cascaded multilevel inverter using transistor-CHB cells has recently been proposed [144]. When the same modulation mechanism is used, inverter has advantage of producing lower power loss when compared to equivalent cascaded NPC inverter, and traditional 9-level cascaded H-bridge inverter. Despite this benefit [145], it is necessary to adopt a complex voltage balancing procedure.

CHAPTER- 4

MODULATION TECHNIQUES

4.1 A DEFINITION OF MODULATION

The "switched mode" is the most common mode of operation for power electronic converters [146]. There are only two possible states for each switch in the converter - either turned off (no electricity is flowing) or turned on. Only when the conductor goes from conducting to non-conducting does it make sense to use the linear area? Otherwise, the switch power dissipation increases significantly. Power flow via the converter is controlled by switches that alternate between 2 states (on & off). Capacitors and inductors at converter's I/P and O/P nodes average or filter switched signal since it occurs so quickly. You may keep your intended DC or low-frequency AC signal while eliminating any unwanted noise from the switched part of the signal path. To get the required average value, PWM is utilised to control the pulse width [147].

The switching frequency, fc, must be set as high as feasible to minimize switching noise, with the important AC component at I/P or O/P terminals being many orders of magnitude larger. Switching losses in large converters set a maximum frequency limit. Square wave switching in GTO converters (fc/f1 = n, the pulse number) is possible at a switching frequency of one, which is known as fundamental frequency switching. This is also true for converters, which are more accurately defined as amplifiers [148] due to their high fundamental peak output frequency. Servo and audio amplifiers, active power filtering, and test signal creation are just some of the uses for these high-power switch-mode amplifiers. Because of the low pulse counts, the distortion is more difficult to eliminate without using effective modulation [149].

To minimise distortion, low pulse counts need the use of efficient modulation. Staggering the switching times and raising the apparent pulse number may significantly minimize distortion in multi-level converters in certain situations [150].

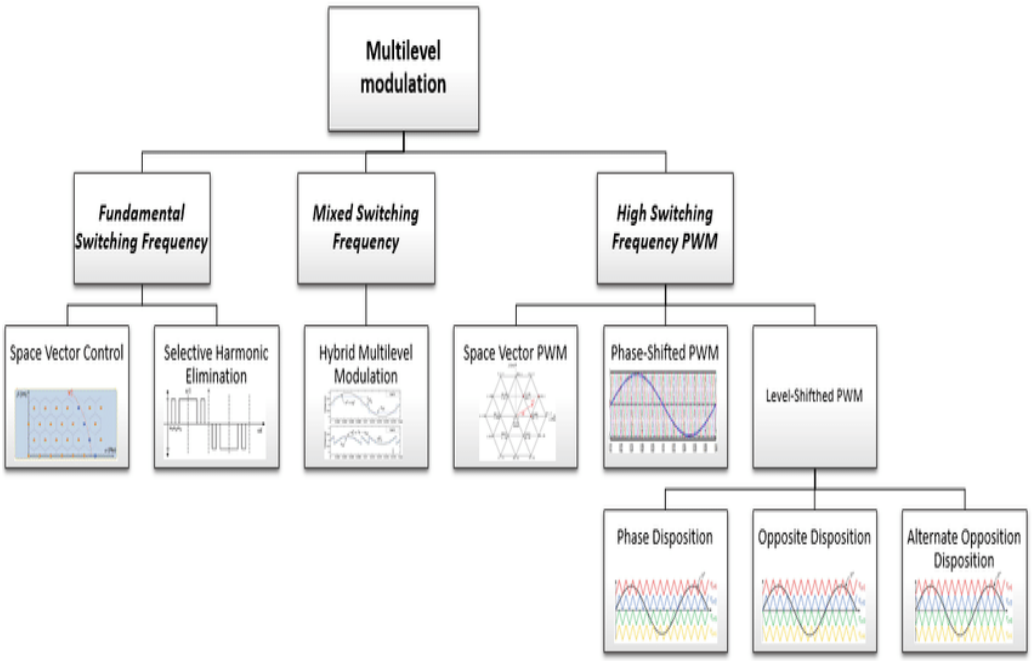


Figure 4.1: Details of PWM techniques

4.2 PWM Techniques

Voltage-source PWM and current-regulated PWM [151] are the two major types of power modulation (PM). DSPs and PLDs are more likely to be implemented using voltage-source approaches since they are easier to implement. Because they are based on event scheduling, most current controllers can only dependably work at a limited amount of power and are consequently analogue in nature. The harmonic performance of discrete current-regulated systems falls short of that of voltage-source approaches. The following is an example of a PWM approach, as shown in fig 4.2.

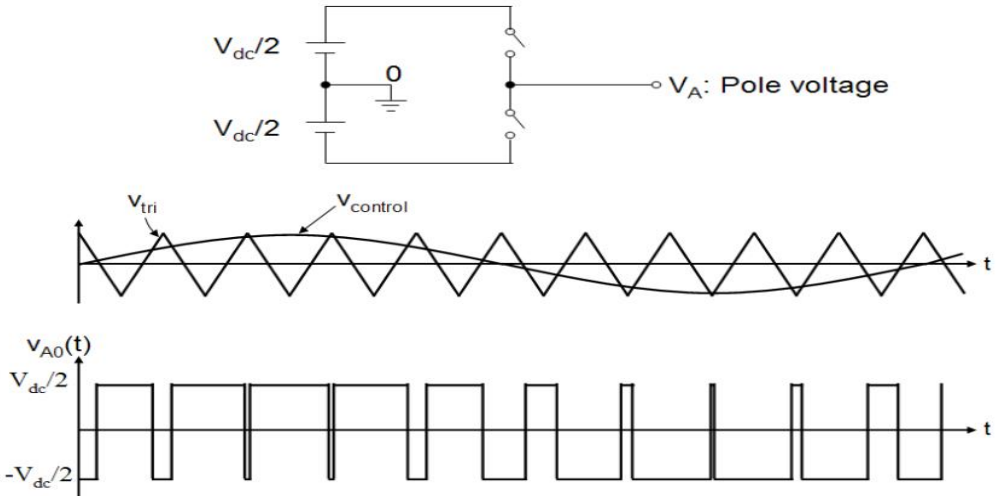


Figure 4.2: Pulse-width modulation (PWM)

O/P voltage of inverter, V_{A0}, is $V_{dc}/2$ when Vcontrol is more than Vtri, and VA0 is negative when Vcontrol is less than Vtri. It is the same as Vtri's frequency that the PWM frequency is set to Amplitude, and fundamental frequency is regulated by Vcontrol's peak value and frequency, respectively. m is modulation index, & it is calculated as:

$$M=\frac{Vcontrol}{Vtri}=\frac{peakof\ (VA0)}{Vdc/2}$$

Here, $(V_{A0})1$ represents fundamental frequency component of V_{A0}.

4.2.1 Voltage-source methods

Two important pathways have been pursued by voltage-source modulation: time domain sine triangle modulation and q-d stationary reference frame SVM [152]. The modulation of a sine wave with a triangular amplitude and a space vector amplitude are mathematically identical. The sine-triangle scheme's triangle form and sine wave harmonics are identical to the space vector scheme's other characteristics.[153]. The switching state of the inverter may be utilised to directly regulate inverter line to ground voltage. Switching state of a given inverter is broken down into transistor signals for that inverter. A control purpose would be to regulate the voltages between line and neutral. The words dc offset and any triple harmonics [154] are often used in 3-phase system. Here, commanded line-to-ground voltages are specified as follows:

$$V_{ag}\,V_{bg}\,V_{cg} = \frac{mV_{dc}}{2}\left[cos(\theta_c)\,cos\left(\theta_c - \frac{2\pi}{3}\right)\,cos\left(\theta_c + \frac{2\pi}{3}\right)\right] + \frac{V_{dc}}{2}\left[1 - \frac{m}{6}cos(3\theta_c)\right][1\;1\;1]$$

Modulation index (m) & electrical angle (c) are utilized to describe modulation range.

Since m controls both the frequency and magnitude of first set of terms on right, we may deduce that this represents an oscillating, sinusoidal set of commanded voltages (m and c). Common-language terminology may be found on right-hand side of page. There must be a suitable range of voltages from ground to dc for the applied dc offset to operate. The inclusion of third harmonic component to maximise dc source voltage is another example of a common-mode term. Discontinuous waveforms may be used to increase switching frequency or harmonics by commanding extra line-to-ground voltages [155].

We'll start with some basic definitions before getting into the specifics of the modulation techniques. For starters, duty cycles are calculated by multiplying the prescribed voltages by a scaling factor. The duty cycles have been changed to-

$$d_{am}\,d_{bn}\,d_{cm} = \frac{n-1}{2}\left[cos(\theta_c)\,cos\left(\theta_c - \frac{2\pi}{3}\right)\,cos\left(\theta_c + \frac{2\pi}{3}\right)\right] + \frac{n-1}{2}\left[1 - \frac{m}{6}cos(3\theta_c)\right][1\;1\;1]$$

By defining a vector of commanded voltage, we'll go on to the following stage.

$$V_{qds}^{s} = V_{qs}^{s*} - jV_{ds}^{s*}$$

Here, the q & d-axis voltage commands are linked to a-b-c variables of eqn.3.2

$$V_{qds}^{s*} = \frac{2}{3}V_{ag}^{*} - \frac{1}{3}V_{bg}^{*} - \frac{1}{3}V_{cg}^{*}$$

$$V_{qds}^{s*} = \frac{1}{\sqrt{3}}(V_{bg}^{*} - V_{cg}^{*})$$

I. Sine-triangle modulation

For n-level inverters, the sine-triangle technique compares a-phase duty cycle to triangle waveforms. The following are the rules for switching:

$$S_{ai}=\{1,\; d_{am} > tri\;0 \quad elsewise$$

$$S_a=\sum_{i=1}^{n-1} \quad sai$$

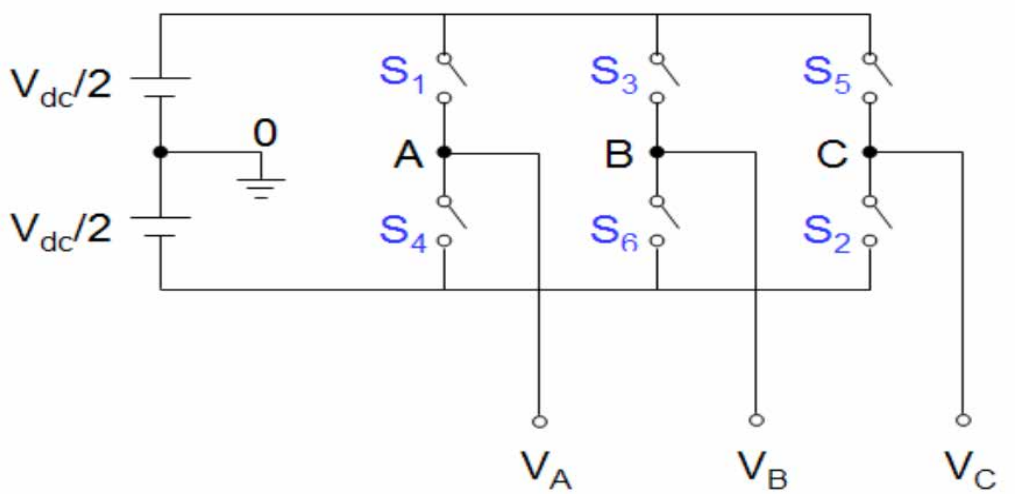


Figure 4.3: Three-phase Sinusoidal PWM inverter

If you're trying to demonstrate voltage-source modulation, it's feasible to illustrate how duty cycle and triangle waveforms cross.

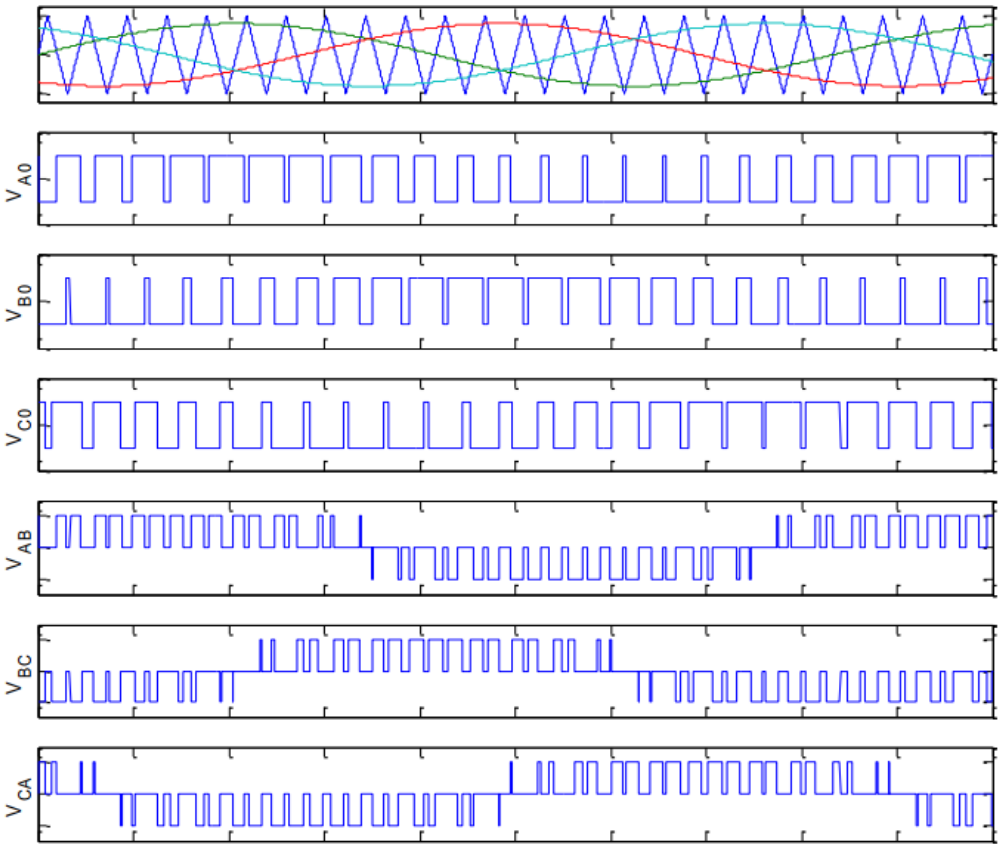


Figure 4.4: Waveforms of 3-phase SPWM inverter

Let fs be the PWM frequency, and f1 be the fundamental frequency for vtri and vcontrol, respectively. “VAB = VA0 – VB0, VBC = VB0 – VC0, and VCA = VC0 – VA0” are the values of VAA in the preceding figure.

m_a is an acronym for the following formula:

$$\mathbf{m_a}=\frac{peak\ amplitude\ of\ V_{control}}{amplitude\ V_{tri}}=\frac{peak\ value\ of(V_{A0})}{V_{dc}/2}$$

the fundamental frequency component (V) of VA0, for instance

There are several ways to represent frequency modulation ratio (m_f).

Sum of m_f's digits is undoubtedly unusual. It is possible that the output voltage will have sub-harmonics if mf is not an integer. The output voltage may include a DC component and even harmonics if the $m_f$is within standard limits. For a three-phase PWM inverter, Mf must be a multiple of 3[156].

Phase- & level-shifted carrier-based modulation methods are available for multilevel inverters. There are two ways to modulate a system using cascaded H-bridge inverters (CHBs)[157]. There is significant difference between phase-shifted & level-shifted modulation in terms of THD. As a result, level-shifted modulation has been suggested. (m-1) triangular carriers are required for m-level CHB inverter with a level-shifted multicarrier modulation method. The bands occupied by (m-1) triangular carriers are continuous due to their vertical placement. Three distinct PWM [158] techniques for level-shifted multicarrier modulation are available:

- Carriage waveforms are all in phase.
- Each of the carrier waveforms above 0 is 1800 cycles out of phase with the others. This is known as phase opposition disposition (POD).
- This leads to a different phase arrangement in 1800 when every carrier waveform was out of phase with its next-door neighbor.

(a) In Phase Disposition (IPD)[159]

The current state of affairs, the carrier-based implementation of this work employs the PWM approach. A three-level inverter's sine-triangle technique is seen in Figure 4.4.

These two triangular waveforms are used in this comparison of the a-phase modulation signal.

Principles for the in-phase disposal procedure are as follows when N is 3:

- (N – 1 = 3-1=2) carrier waveforms are structured such that each carrier is in phase with others.
- When reference voltage is bigger than the carrier waveforms, converter changes to +Vdc/2.
- In order for converter to be zeroed, the lower carrier waveform must be greater than or equal to 0.
- When reference is lower than both carrier waveforms, converter switches to -Vdc/ 2 mode.

Switching pulses are produced by comparing modulation signals to carriers at each instant of time in the carrier-based technique.

Fig. 4.4 shows the carrier-based PWM method's switching pattern. The upper triangle is from 1 to 0 while the bottom one is the opposite, from –1 to –1 in PWM scheme. Peak-to-peak value of each of (N –1) triangles is 2/, making them identical to N –level inverter (N -1). Thus, magnitudes of highest triangle, the second carrier waveform, and the bottommost triangle vary from (1-2/ (N-1)) to –1, respectively. Carrier-based PWM system with in-phase disposition simulation is shown in Figure 4.5. (IPD). It is the function of these devices to flip between modes that is

- H_a> Triangle -1 & Triangle -2; H_{a3}=1, otherwise H_{a3}=0.
- H_a< Triangle -1 & H_a > Triangle -2; H_{a2}=1, otherwise H_{a2}=0.
- H_a< Triangle -1 & Triangle -2; H_{a1}=1, otherwise H_{a1}=0.

As seen in the graph, S1ap and S2ap are triggered when the modulation signal exceeds the thresholds of Triangle 1 and Triangle 2. + Vdc/ 2 becomes the converter's output voltage when S1ap and S2ap are activated. This is done by switching on both the S1an and S2an, which forces the converter to transition from + Vdc / 2 (S1an) to zero (S2ap)

during its positive cycle (S1an). To put it another way: The converter moves from zero to Vdc/2 during the modulation signal's negative half cycle. Input nodal voltage and existence function formulas for three-phase loads linked in a star configuration.

- $V_{a0}= H_{a3}\ V_{30}+ H_{a2}\ V_{20}+ H_{a1}\ V_{10}$
- $V_{b0}= H_{b3}\ V_{30}+ H_{b2}\ V_{20}+ H_{b1}\ V_{10}$
- $V_{c0}= H_{c3}\ V_{30}+ H_{c2}\ V_{20}+ H_{c1}\ V_{10}$

(b) Phase Opposition Disposition (POD).

Carriers above 0 reference are in phase with each other, whereas carriers below 0 reference are 180 degrees out of phase with each other. When number of levels N is three, phase opposition disposition rules apply [160].

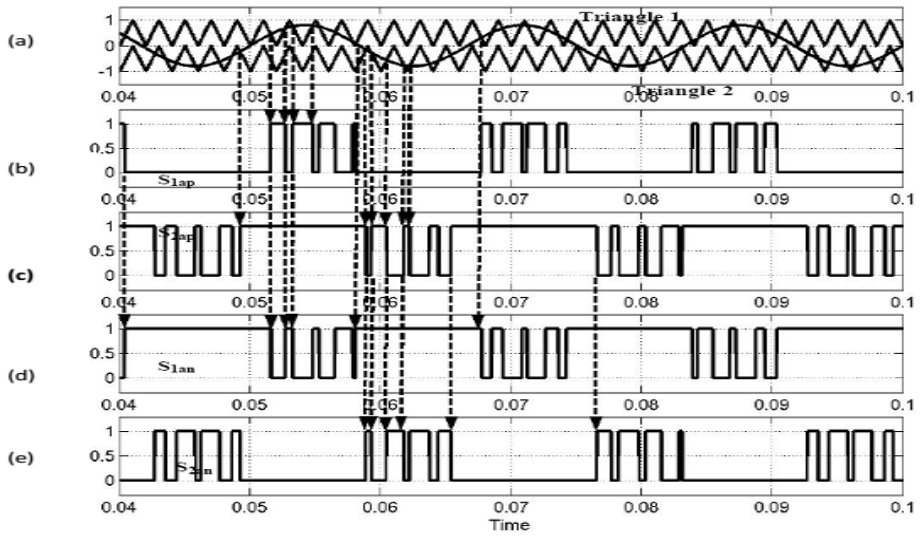


Figure 4.5: IPD-based PWM switching pattern: 2 triangles & modulation signal (b) S_{1ap} (c) S_{2ap}(d) S_{1an} (e) S_{2an}.

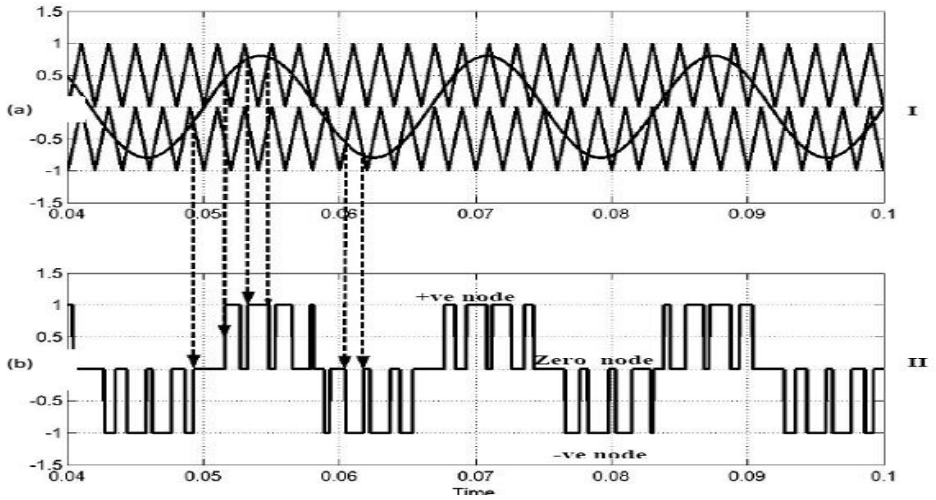


Figure 4.6: In phase allocation simulations of a carrier-based PWM scheme (IPD). (a) Waveforms of modulation signal and the carrier wave (b) Phase "a" output voltage.

1. N –1 = 2 carrier waveforms have all waves above 0 in phase, whereas all waves below 0 are out of phase.
2. When the reference voltage exceeds the sum of the two carrier waveforms, converter changes to + Vdc/ 2.
3. The converter is reset to 0 if reference value is greater than or equal to lower carrier waveform.
4. When reference is smaller than the sum of two carrier waveforms, converter defaults to -Vdc / 2.

Figure 4.7 depicts the PWM switching functionalities that may be achieved using the POD carrier-based PWM. The PWM system employs two triangle waveforms, the top of which has an amplitude range of 1 to 0 and the lower of which has an amplitude range of 0 to –1. Turn on S1ap and S2ap when modulation signal exceeds both carrier waveforms; S2ap/S1an when modulation signal is less but larger than the upper carrier waveform; neutral point conversion when modulation signal exceeds both carriers. S1an and S2an are activated when the reference voltage for both carrier waveforms is lower than reference voltage for both carrier waveforms. The waveform of Phase A's output voltage clearly shows three separate phases of development.

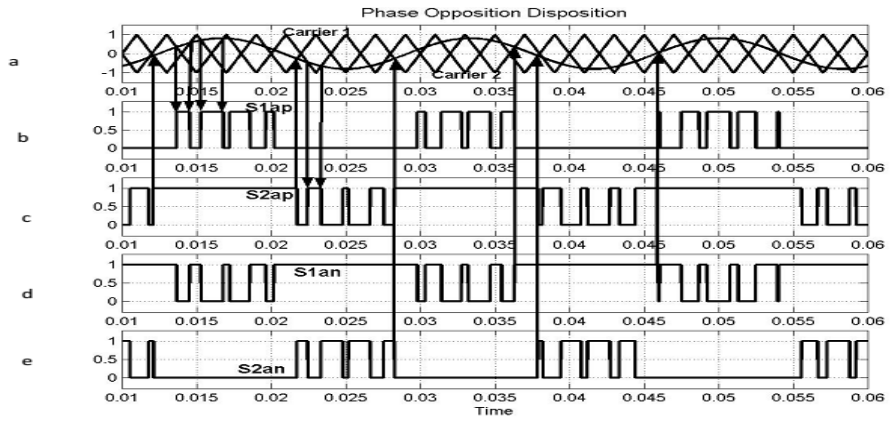


Figure 4.7: The POD carrier-based PWM technique produces the following switching pattern: (a) 2 triangles& modulation signal (b) S_{1ap} (c) S_{2ap} (d) S_{1an} (e) S_{2an}.

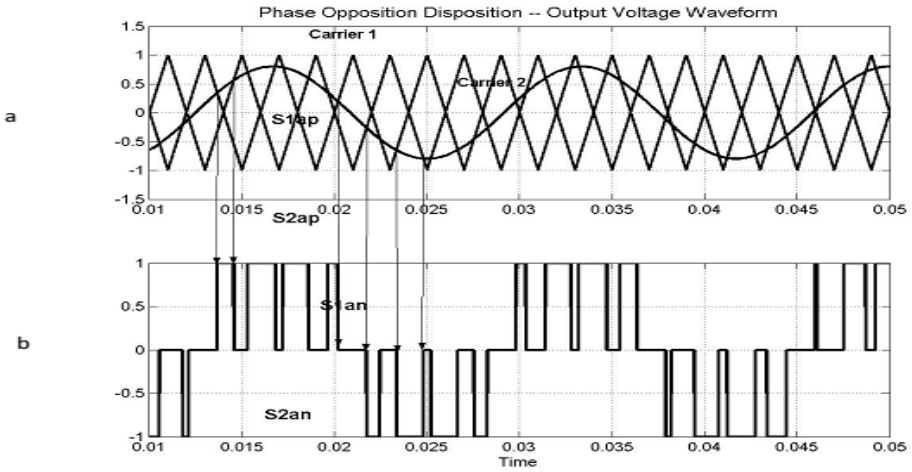


Figure 4.8: Carrier-based PWM utilising POD simulation. (a). Modulation signal & phase carrier waveforms (b) Phase "a" output voltage.

(c) Alternate Phase Opposition Disposition (APOD).

This modulation technique uses carrier waves that are 180 degrees out of sync with each other. Three-level inverters are comparable to five-level inverters when it comes to the APOD system [161]. When N is 5, the APOD rules alter, as seen in the example below.

1. There are N – 1 = 4 carrier waveforms, each of which is 180 degrees out of

phase with the one next to it. Vdc/ 2 is activated when the reference surpasses all carrier waveforms.

2. Converter changes to Vdc/4 when reference waveform is higher than all other carriers and lower than the highest carrier waveform.
3. It is just a matter of time until a converter flips to zero if the reference is below the two highest carrier waveforms and above the two lowest carrier waveforms
4. Vdc/4 becomes reference voltage if and only if reference voltage is bigger than and less than all other carrier waveforms.
5. As soon as the reference falls below all carrier wave forms, converter changes to -Vdc/2 mode.

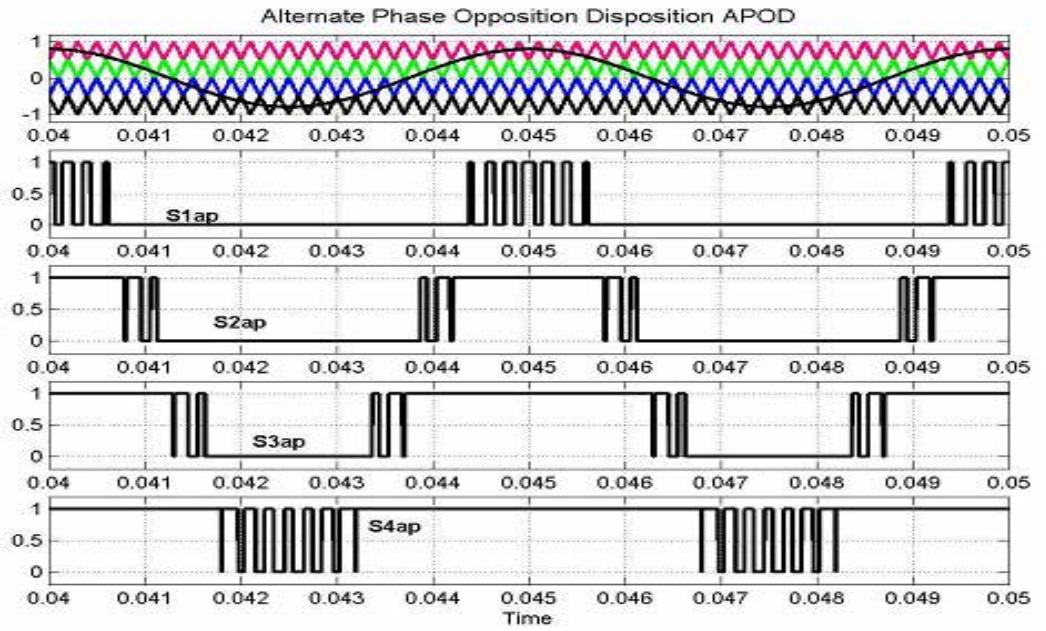


Figure 4.9: Five-level inverter: APOD carrier-based PWM approach for switching pattern (a) 4 triangles & modulation signal (b) S_{1ap}(c) S_{2ap}(d) S3ap(e) S4ap.

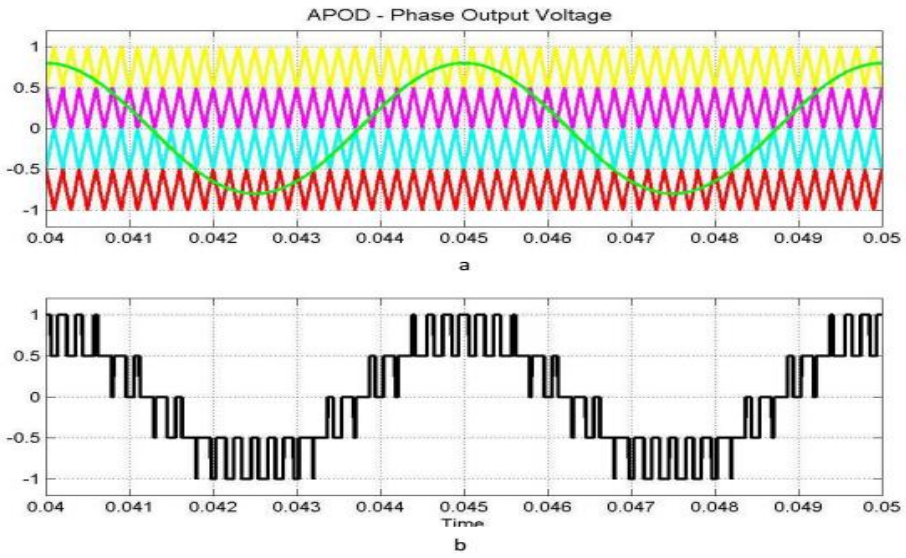


Figure 4.10: A five-level inverter's carrier-based PWM scheme is simulated utilising APOD. (a) Modulation signal & carrier waveforms (b) Phase “a” output voltage.

4.2.2 Multilevel SVM

"Space vector modulation" is an implementation of PWM in which reference and inverter switching states are represented by three-phase space vectors instead of being represented by the reference and output levels per phase in time. However [162], large number of vector states may be employed to modify reference in multilayer converters. In addition, as seen in Fig. 4.11, each state vector contains several redundant elements. The search for modulating vectors must be optimized, and a suitable switching sequence must be applied by Multilevel SVM taking care of this behavior [163].

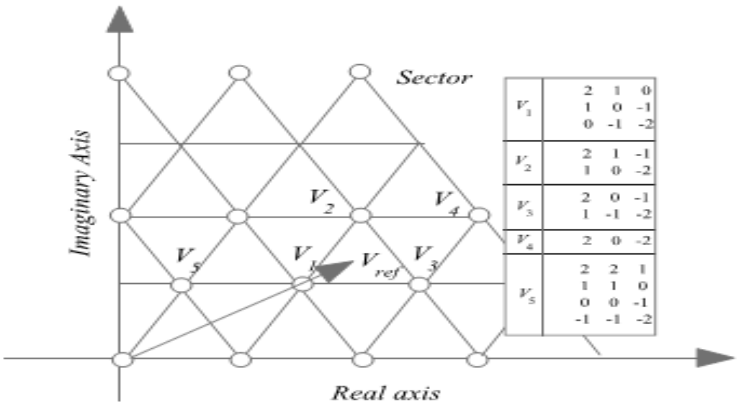


Figure 4.11: Multilevel Space Vector Modulation

To counter this, the same characteristics of state and switching redundancy make it possible to achieve other goals. Improved modulation techniques may also be used for extra purposes, such as achieving greater redundancy in state and switching losses.

4.2.3 Selective Harmonic elimination

a. Fundamental switching frequency

It is another name for Patel's basic switching frequency hypothesis's selective harmonic elimination technique [164–165]. An example of an output from 11-level multilevel converter using basic frequency switching method may be seen in Figure 31.2. Figure 31.2's waveforms' Fourier series expansion is shown in figures (31.1) and (31.2).

For instance, the conducting angles 1-s may be chosen to reduce overall harmonic distortion of voltage. These angles are frequently employed because lower frequency harmonics frequently take precedence [25].

Fifth, seventh, eleventh, and thirteen harmonics can all be eliminated from 11-level scenario in Figure 31.2 by using the appropriate conductor angles. To ensure that magnitude of fundamental waveform and amplitude or modulation index o reference waveform, m_a, are same, one degree of freedom is used. The inverter's amplitude command for sine wave O/P phase voltage is VL*, but converter's maximum amplitude, or VLmax=sVdc, is VLmax. The equations starting with (31.2) are as follows:

$$\cos(5\theta_1)+\cos(5\theta_2)+\cos(5\theta_3)+\cos(5\theta_4)+\cos(5\theta_5)=0$$
$$\cos(7\theta_1)+\cos(7\theta_2)+\cos(7\theta_3)+\cos(7\theta_4)+\cos(7\theta_5)=0$$
$$\cos(11\theta_1)+\cos(11\theta_2)+\cos(11\theta_3)+\cos(11\theta_4)+\cos(11\theta_5)=0$$
$$\cos(13\theta_1)+\cos(13\theta_2)+\cos(13\theta_3)+\cos(13\theta_4)+\cos(13\theta_5)=0$$
$$\cos(\theta_1)+\cos(\theta_2)+\cos(\theta_3)+\cos(\theta_4)+\cos(\theta_5)=5m_a$$

These nonlinear transcendental equations can be iteratively solved utilising the Newton-Raphson method (31.21). As an illustration, the numerals 1 through 5 are produced when a modulation index of 0.8 is used. Therefore, if inverter output is symmetrically switched during positive half cycle of fundamental voltage to +Vdcat

6.57°, +2Vdcat 18.94°, +3Vdcat 27.18°, +4Vdcat 45.14°, & +5Vdcat 62.24°, and similarly if inverter output is Genetic algorithms [69] [70-72], O/P voltage of an 11-level inverter shall not have harmonic components of harmonics.

The pre-calculated switching angles are really stored in memory as data. Microcontrollers may be utilised to create PWM gate drive signals.

b. Selective harmonic elimination PWM

To accomplish wide variety of modulation indices with little THD, a generalised selective harmonic modulation technique called virtual stage PWM was designed. The waveform of O/P signal is displayed in Fig 4.12. With Virtual Stage PWM, you may use both Unipolar Programmed PWM & basic frequency switching techniques. Figure 4.13 depicts the Unipolar Programmed PWM's output waveform. Multilevel converters commonly use Unipolar Programmed PWM, which involves switching on and off switches attached to a single DC voltage several times every fundamental cycle. Output voltage waveform is determined by switching pattern.

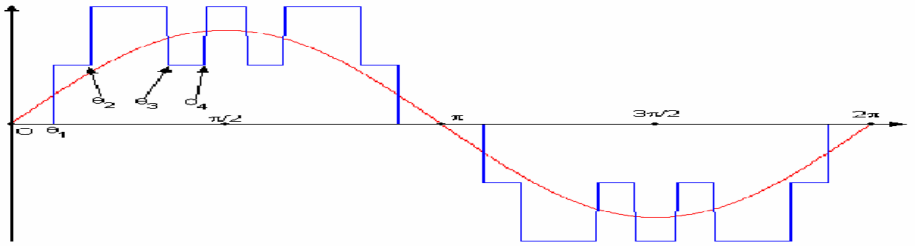


Figure 4.12: The waveform of the PWM control of a virtual stage

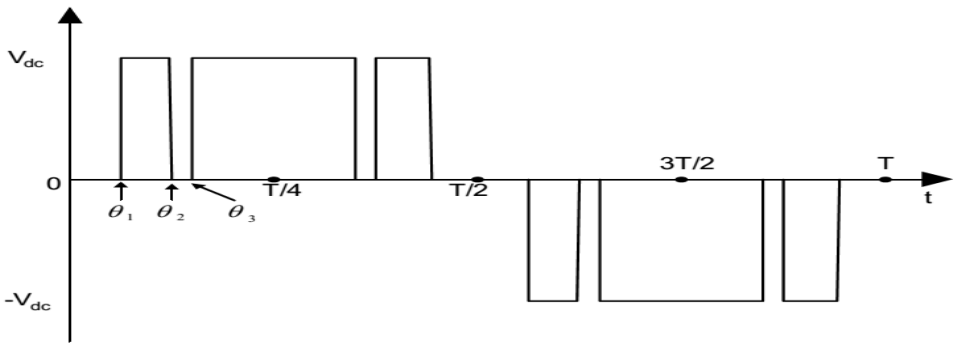


Figure 4.13: Output waveform of a unipolar switch

As there are as many DC sources as switches in the basic frequency switching method, there are an equal number of switches. Virtual Stage PWM, on the other hand, does not have as many switching angles as there are DC voltages. Modulation indices too low to use multilayer fundamental frequency switching may be used using bipolar and unipolar PWM. Low modulation indices may also be achieved using Virtual Stage PWM. With Virtual Stage PWM, THD waveforms tend to be less pronounced. As a result, Virtual Stage PWM offers a control option with a low modulation index for Bipolar Programmed PWM & Unipolar Programmed PWM.

For processes like Virtual Stage PWM method & fundamental switching frequency method of selective harmonic removal, transcendental equations 31.21 for switching angles must be solved. Newton's method can be utilised to resolve equation 31.21; however, the outcomes are not guaranteed. As a result, Newton's method cannot be used to resolve equations for a large number of switching angles if adequate initial estimates aren’t given. [41].

In order to resolve transcendental equations requiring switching angles, researchers have discovered a new approach. [30-35]. Polynomial equations may be created using transcendental equations that reflect harmonic content. In order to exclude particular harmonics like 5th, 7th, 11th, and 13th, a theory called elimination resultant has been used to estimate switching angles. Polynomials in these equations grow more complex when more DC voltages or switching angles are included. Newton's approach is used to tackle the issue of the fundamental frequency switching angle. As a starting point, lower-order transcendental equations may be used to produce an initial estimate. [165-172]

4.3 Hybrid Modulation Methods

In essence, hybrid modulation techniques use mixed-switching frequencies. Initially, approaches were developed for CHB inverters with different DC sources[173]. Since no two cells in a cascaded H-bridge inverter are exactly alike, each cell's power rate varies. As a result, different switching frequencies can be used by the cells. Low switching frequency is used for high-power cells to create square waveform patterns.

Only low-power cells use PWM switching, which occurs at a considerably greater frequency. Inverter switching losses can be decreased in this way, increasing total efficiency [174].

The control block diagram displayed in Figure 4.14 can be utilised to demonstrate fundamentals of hybrid modulation method. There are introduced three levels of modulation. A first-stage control cell of high power produces square waveform VA1 by comparing a sinusoidal reference Vref with predefined maximum and lowest voltage levels at fundamental switching frequency. The second stage's input is determined by the difference between Vref and VA1, which stands for the first stage's unmodulated component. The second-stage square waveform VA2 is created by further comparison at 2nd-stage control cell of lower power at low switching frequency. In order to create PWM waveform, VA3, final un-modulated component from 2nd stage, Vref,3 is then sent to 3rd-stage PWM cell with lowest power. This cell uses a high switching frequency. VA1, VA2, and VA3 are added together to provide VAN, total O/P voltage.

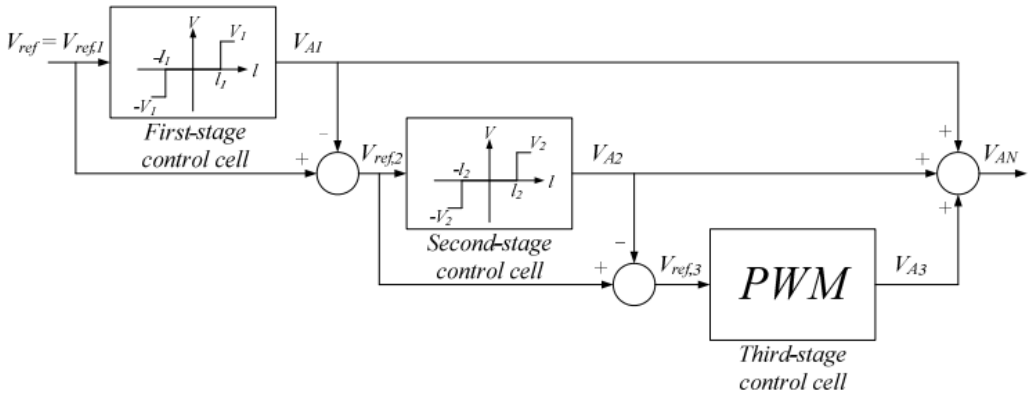


Figure 4.14: Hybrid modulation method.

It is suggested that the best symmetry to use for 3-cell inverter is VDC1: VDC2: VDC3 = 1: 2: 6[178] to get a maximum number of O/P levels for CHB inverter with uneven DC sources. Additional research has been done on a number of hybrid topologies with different cell counts, and a number of design concerns, particularly those pertaining to hybrid modulation, have been suggested [179]. The effects of hybrid multilevel modulation approach on harmonic content of input currents & output voltages have also been thoroughly studied [180]. To advance harmonic input performance of variable

speed drives, modifications have been proposed that eliminate unwanted low-frequency harmonics from input currents across all operating ranges. Alternative study [181] examines scenario in which load consumes active power, resulting in the operation of some power cells in regeneration mode. A 13-level asymmetric inverter has a new hybrid modulation technology that guarantees unidirectional power flow in every power cell as a solution to this issue. In one hybrid modulation technique, level-shifted multilevel PWM is used for low-power cells, while selective harmonic removal is applied to high-power cells [182]. By using fewer H-bridge cells, triplen harmonic injection also reduces semiconductor losses and improves the balancing of the cell capacitor voltage.

4.4 Current Control Techniques

The degree to which an inverter system performs is significantly influenced by current control techniques [183]. A system is said to perform well if it can achieve a number of desired goals, including low harmonic distortion of high dynamic response, output current, small current ripple, good DC voltage utilisation, and limited or constant switching frequency to ensure power devices are operated safely[184]. A benefit of the system in some circumstances is the capacity to deliver bidirectional power flow [185]. A current control scheme's primary job is to guide real currents to be as near to reference currents as is reasonably achievable. In a perfect world, there should be no discrepancy between the real and reference currents' amplitude and phase. The discrepancy does, however, always exist in the real world and is typically identified as the present mistake.

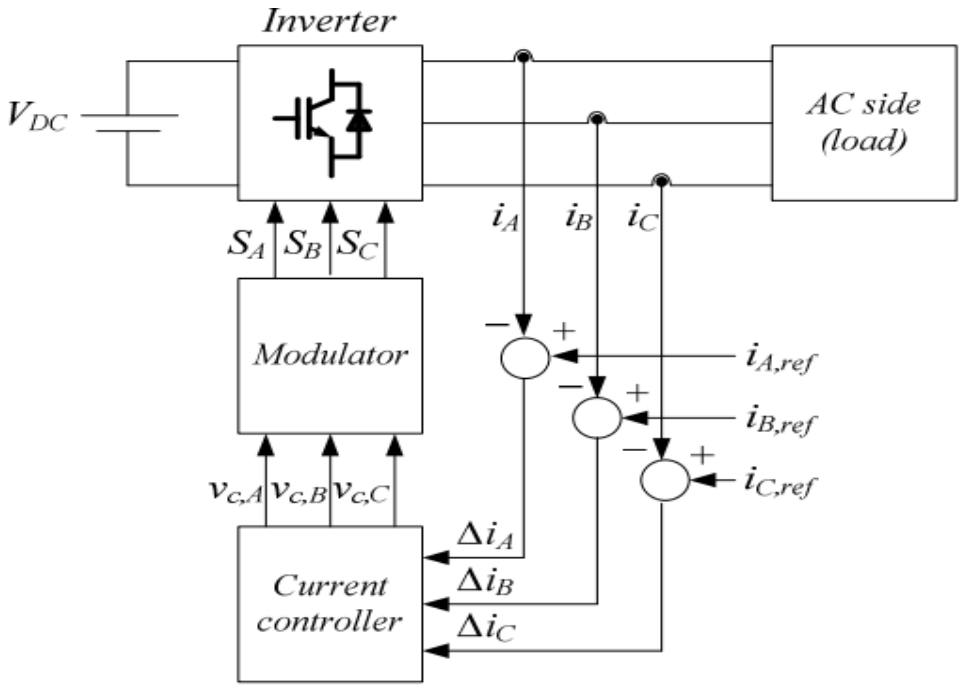


Figure 4.15: General current control scheme.

A general current control scheme's block diagram is displayed in Fig 4.15. Measured output currents iA, iB, & iC are provided by feedback path in figure so that they can be compared to desired output currents iA, iB, & iC, individually. The current controller then processes difference between measured & desired currents—which stands for current errors ΔiA, ΔiB, and ΔiC—to produce the control signals vcA, vcB, and vcC. Using control signals, modulator then generates switching states SA, SB, and SC for inverter's power switches. In order to ensure that current errors stay within acceptable bounds depending on switching states, inverter functions in such way that output currents constantly try to closely match their references. It is preferable for these limitations to be close to zero. Numerous current control systems have been documented in literature; some of most significant ones are briefly discussed below.

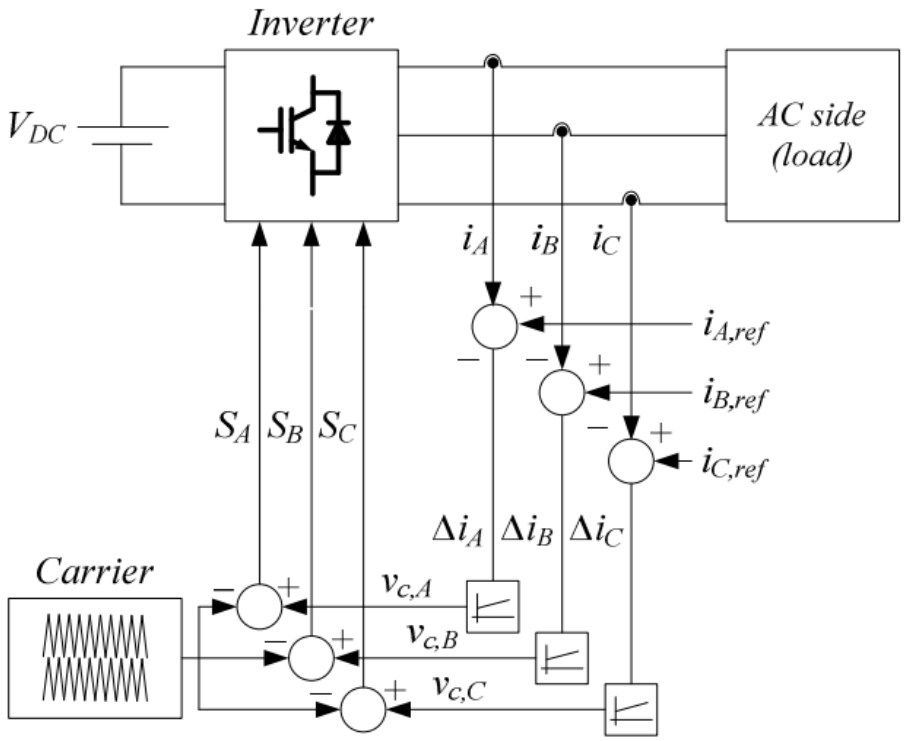


Figure 4.16: Ramp-comparison current control scheme.

4.5 Ramp-Comparison Control

Carrier-based modulation is essentially used in the ramp-comparison control approach to produce the switching states. The ramp-comparison control technique is displayed in Fig 4.16. To create control signals vcA, vcB, & vcC in this control system, proportional-integral (PI) controllers are utilised to receive current errors ΔiA, ΔiB, & ΔiC. Next, triangular carrier signals are compared with these control signals as modulating signals. The switching signals SA, SB, & SC for inverter switches are provided by comparison findings. When modulating signals are stronger than carrier signals, switches are triggered to provide positive O/P voltages. Conversely, switches are triggered to provide negative O/P voltages when modulating signals are lower than carrier signals. Through integral part and proportional gain, and zero placement, the PI controller is essential in reducing errors and managing the amount of ripple [186]. As a result, there is number of factors that must be taken into account when designing PI controller. To prevent modulating signals' slope from exceeding the triangle signal slope, the gain needs to be correctly restricted. This prevents numerous crossings, which could raise switching frequency &cause switching losses. At same time, gain must be

just right to prevent the tracking error from getting out of hand. The inverter's switching frequency is constant since it tracks the carrier signal's frequency. After that, the generated harmonics are defined at set frequency. Carrier frequency must be chosen carefully because choosing the wrong frequency can result in many crossover issues. In one study[187], an analytical method for choosing the right carrier frequency was described. Since the PI controller must analyse AC signals, there is also intrinsic amplitude and phase error[188]. This causes a systemic transmission delay. Additionally, feedback path, which heavily depends on load characteristics, affects the system response. Additionally, a 0-voltage vector is functional to load, which results in multiple instants within fundamental period of output voltage where load is disconnected[189]. Nevertheless, a fix has been suggested that involves the employment of three triangular carriers that are phase-shifted by 120 degrees. The use of ramp comparison has been covered in a number of researches. To actualize ramp comparison control method for grid-connected applications, digital PI controller was built using DSP in one study[190].

4.6 Hysteresis Control

Hysteresis current control is independent of changes in the load parameters, in contrast to ramp-comparison control [191]. In this method, as shown in Figure 4.17, hysteresis comparators are employed to process current faults before directly producing switching signals of power switches. Hysteresis band, which is predetermined tolerance boundary around reference current for each hysteresis comparator, is utilised to directly measure current to remain consistently within band's range. The dynamic performance is then outstanding since switching signals are created by direct comparisons in hysteresis comparators, which can result in quick reactions. This plan is simple to implement practically because it is built on a straightforward idea. The system is also reliable and free of tracking errors[192].

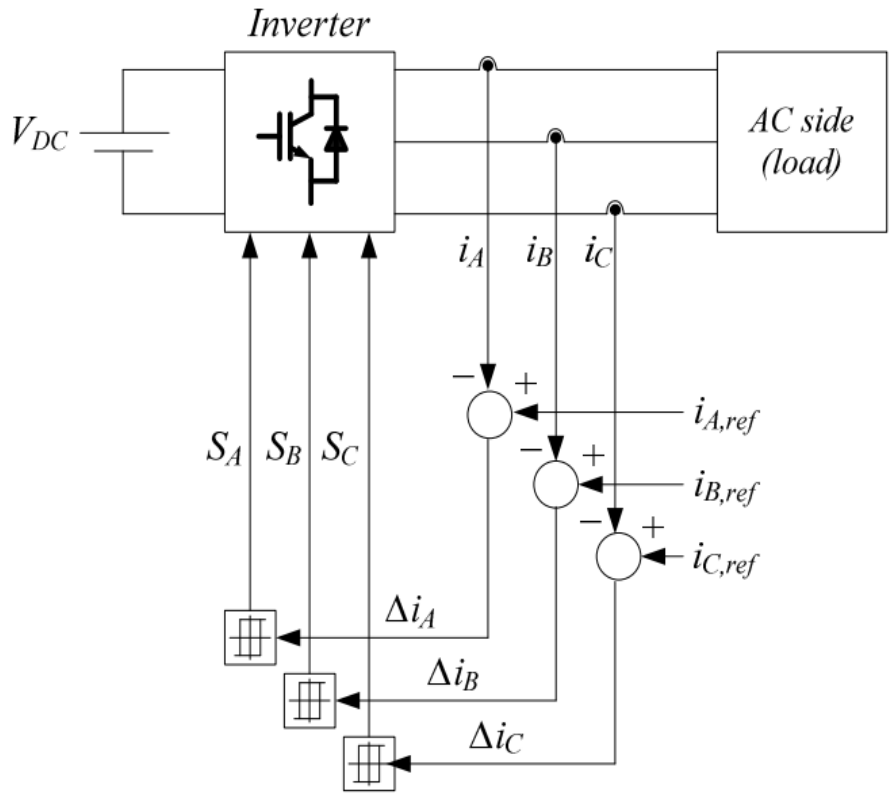


Figure 4.17: Hysteresis current control scheme.

Despite the benefits, the key characteristic of hysteresis control scheme is inverter's changing switching frequency throughout the fundamental period. [193]. This causes the inverter to occasionally operate irregularly, which in turn causes switching losses to rise [194]. Grid-connected inverter systems may also experience undesirable spread of ripple current harmonics, which complicates design of O/P filter & causes unwanted grid resonances [195]. The current error for system lacking neutral links may quadruple hysteresis band's value[196]. Since variable switching frequency is caused by the interaction of 3 independent hysteresis comparators, which causes phase current in one phase to also be affected by voltages of the other phases, it is suggested that three dependent hysteresis comparators with application of 0 voltage vector be used. Since the development of the space-vector hysteresis current controller [198], additional advancements have been realised. Hysteresis controllers with constant switching frequency have been offered as a way to completely prevent the negative impacts of variable switching frequency. According to fluctuations in load current, motor speed, & neutral-point voltage, an adaptive hysteresis controller is proposed in one study to

retain switching frequency constant under all operating conditions [199]. Another study[200] suggests using a space vector-based hysteresis controller with the concept of parabolic hysteresis band to achieve practically constant switching frequency for 2-level inverter-fed drive. By taking into account derivative of current error while choosing voltage level, time-based hysteresis controllers have also been developed [201]. This allows the current error to be pushed to zero. In order to enhance transient response and stabilise the switching frequency, multiband hysteresis has also been researched[202, 203]. A brand-new space-vector-based hysteresis current controller for induction motor drives fed by multiple inverters has just been reported[204]. The control method makes use of a shifting parabolic hysteresis band to regulate variance in switching frequency & specific voltage vector selection method to guarantee optimal switching of inverter.

4.7 Voltage-Oriented Control

It uses a coordinate transformation between fixed and synchronously revolving dq reference frames and employs the voltage-oriented control (VOC) approach. By converting AC phase values to DC components by coordinate transformation, synchronous controller can control these components with no steady-state error. [205]. Figure 4.18 demonstrates the fundamental idea behind the VOC design. First, stationary frame AC currents iα and iβ are created from the measured output currents iA, iB, & iC. In order to create synchronous rotating frame DC quantities id & iq, a second transformation is then applied. The mistakes produced, Δid and Δiq, are fed into the PI synchronous controllers after these DC amounts are compared to their respective references. PI controllers produce proper control signals vd & vq to correct these faults. Before being employed by the modulator, vd & vq must first be translated back to stationary frame & then to phase quantities in order to produce switching signals of power devices for execution of command signals. The VOC system is regarded as an indirect active & reactive power control method. Active & reactive power flows are determined by DC values id & iq, respectively. It is preferable for iq to be set to 0 to attain unity power factor. As outcome, reference command, iq- ref, for q-component is set to zero. The fact that id & iq are 2 different numbers suggests that active &reactive powers can be managed separately. Cross-coupling components in rotating frame

voltage equations prevent PI controllers from performing satisfactorily in terms of tracing performance.

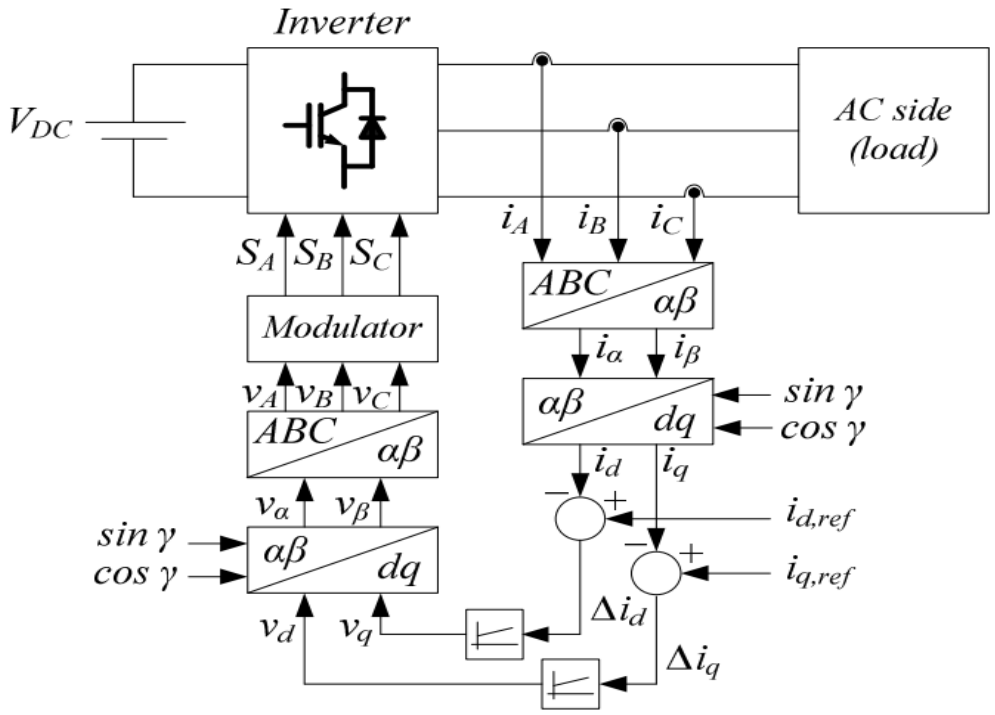


Figure 4.18: Voltage-oriented current control scheme.

[206]. A feedforward decoupling network is utilised to eliminate cross-coupling effect and make controllers independent of one another for controlling id and iq. This method enables the PI controllers to perform accurately in terms of current tracking [207]. The use of the virtual flux idea has been claimed to result in further improvement. A grid-connected system using the VOC technique executes coordinate transformation to synchronous rotating frame using angle of line voltage vector in stationary frame. Fluctuations in line voltages have significant impact on accuracy of the estimated angle [208]. Since virtual flux is less susceptible to aforementioned disturbances, angle of the virtual flux vector is employed instead to produce more precise coordinate transformation in order to reduce this effect. Additionally, using this method, the VOC technique can achieve robustness without implementing a phase-locked loop (PLL). The VOC method often produces adequate, steady state operation and good transient response [209]. Additionally, it is capable of using a fixed switching frequency [210]. VOC method is typically used for applications connected to the grid. For grid-

connected wind energy conversion systems, dynamic Volt Ampere Reactive (VAR) compensator based on VOC scheme has been reported in one study [211]. The series inductor filter has been replaced by LCL filters to provide interface between inverter & grid in order to accomplish low switching frequency operation, which is typically encountered in high power applications [212]. However, one issue with LCL filter is that resonance damping is necessary. As a result, the effectiveness of PI controllers in VOC scheme using LCL filters has been researched (Dannehl, Wessels, & Fuchs, 2009). A better maximum power point tracker has been suggested as a solution to the changing irradiation problem based on the VOC system as well [213].

Field oriented control (FOC) scheme is analog of VOC method in motor drive applications [214]. The stator currents in a fundamental FOC system (Jasinski, 2005) are compared in dq frame before being supplied to PI controllers to produce commanded stator voltage of the d-axis & q-axis components. To provide switching signals for power switches, space vector modulator converts these specified voltage components from spinning frame back to stationary frame. In this approach, reference stator current for q-axis component is also supplied by a speed controller. Regarding d-axis component, reference stator current is derived using rotor flux linkage.

Numerous studies have been carried out to enhance plan so that other machines, like bearingless [215] and five-phase [216] induction motors, can be used with it.

4.8 Direct Power Control

By directly regulating instantaneous active & reactive powers, the direct power control (DPC) scheme governs the phase currents. [216] DPC uses power control loops without any synchronous rotating coordinate transformation, in contrast to VOC, which uses inner current control loops with coordinate transformation. The DPC scheme's block diagram is displayed in Figure 4.19. The voltage & power estimation block uses3-phase currents and voltages to estimate instantaneous active power (p) and reactive power (q). Following that, calculated p & q are contrasted with the corresponding pref and qref references. A voltage controller can be used to calculate pref, but qref is often left at 0 to obtain unity power factor. After feeding hysteresis controllers with the power errors Δp and Δq, they generate the digitised signals vp & vq, which, along with output

of voltage position detector θ, are used to choose correct voltage vector in accordance with switching table. The method of selection limits power errors inside hysteresis band. Switching table is created offline & stores inverter's switching states in accordance with operational circumstances.

DPC system can also be enhanced utilising the virtual flux notion, much like the VOC scheme. Numerous voltage & current sensors are wanted for the calculation of instantaneous powers, which raises the cost and reliability problem.

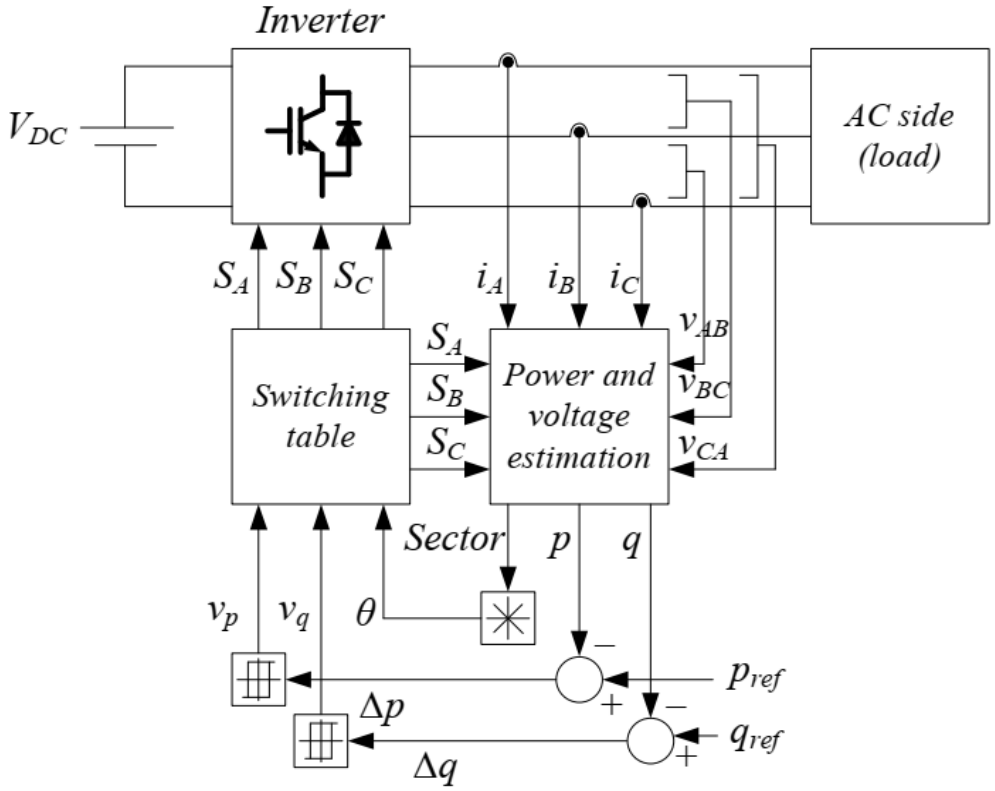


Figure 4.19: Direct power control scheme.

To use fewer sensors, a voltage estimate method is suggested [217]. Practical implementation has become a problem, nevertheless, because computation of instantaneous powers requires time derivatives of measured currents. Additionally, the derivatives have the ability to amplify the noise, which raises the distortion level. The virtual flux concept has been used to address this issue [218]. Virtual flux is utilised to calculate instantaneous powers rather than voltages. Both the dq frame and the αβ frame can be used for power estimation. Since dq transformation can be avoided, estimation

using quantities is typically preferred.

The DPC scheme's primary benefit is that it can deliver a quick and reliable dynamic response [219]. This is because synchronous rotating frame transformation, which generally requires significant processing effort, is not present. DPC scheme implementation can be made simpler, particularly when power calculation is done via virtual flux. The DPC has continued to advance, according to numerous researches. In one study, the DPC technique is combined with 3rd-order LCL output filter to reduce harmonic distortion for inverter that runs at low switching frequency [220].

A modified virtual flux DPC method involving power-based active damping & individual harmonic control loops has been proposed as a solution to the steady-state & transient distortion of O/P current that can be caused by LCL filter resonances. When applied to a 5-level active NPC inverter, another variant of the virtual flux DPC method incorporates a block to equalise voltage across DC link & floating capacitors[221].

Using hysteresis controllers is one way in which the DPC's switching frequency varies. Also, the digital implementation of hysteresis controllers requires high sampling frequency [222]. To solve this issue, a PI controller and a space vector modulator are substituted for the traditional DPC scheme's hysteresis controllers and switching table. This results in direct power control with SVM (DPC-SVM) [223], a variant of the original DPC technique. DPC-SVM scheme is shown in Fig2.20. To create control signals, the PI controllers must first convert the power errors from dq frame to the frame. The space vector modulator then uses the control signals' amounts to produce switching signals. In order to better serve grid-connected applications, increased harmonic and voltage dips compensating modules [224] have been integrated into the DPC-SVM scheme. Moreover, a single-chip floating-point microcontroller has been developed with the modified DPC-SVM algorithm.

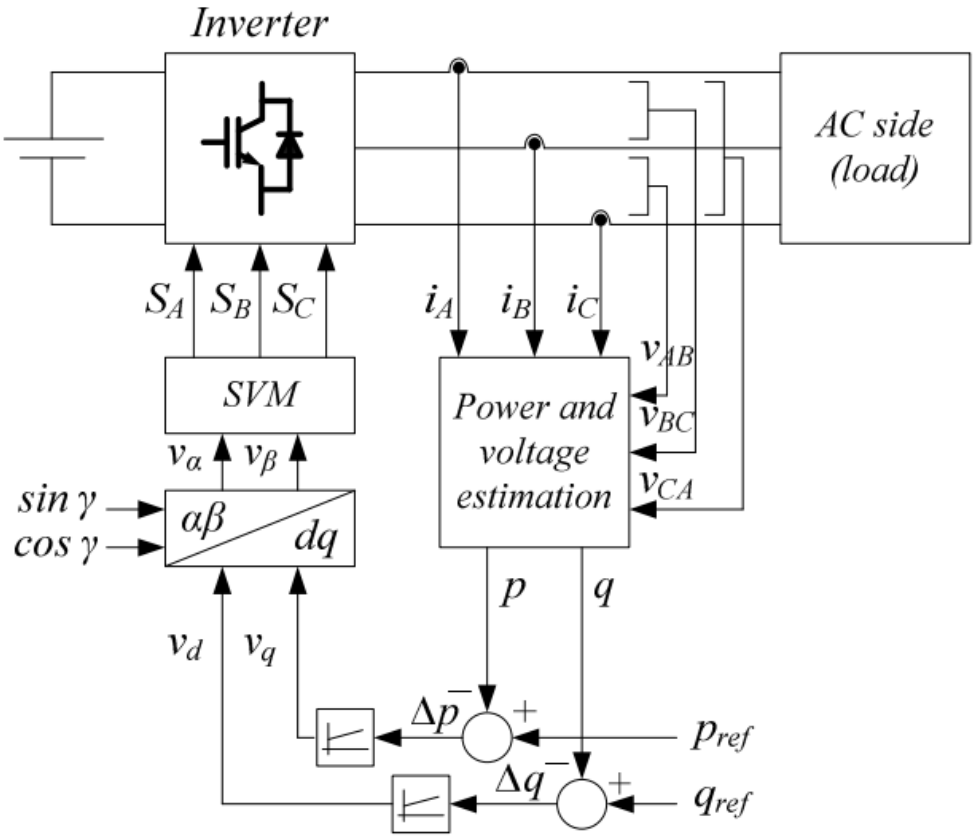


Figure 4.20: Direct power control with SVM scheme.

DPC is based on direct torque control (DTC), a vector control commonly used with AC machines [225]. Motor drive applications often use DTC instead than DPC since DPC is reserved for usage with grid-connected devices. The DTC is analogous to the torque and stator flux control in place of active & reactive powers. DTC has been the subject of extensive research because of its many benefits, which include a straightforward control structure, the elimination of the need for coordinate transformation, and the achievement of a high level of dynamic performance in torque control loops[226]. Despite these benefits, DTC has a number of downsides, including torque pulsation & a high and variable switching frequency, which need to be studied further if they are to be mitigated. These include efforts to better estimate reference torque & reference flux [228] and eliminate torque pulsation [227].

4.9 Predictive Control

The premise of predictive current control scheme [229] is that behaviour of current can

be predicted utilising load and inverter models according to specific predetermined criteria. After making a forecast, the models produce a set of possible control actions, one of which is chosen and applied to inverter. To evaluate future values of output currents, preset criteria are typically stated as a quality function. A block diagram of predictive current control technique is displayed in Fig. 2.30. The predictive model block is the first to receive the output current measurements. Discrete-time form of O/P currents at next sampling instant, i(k+1), are provided by predictive model block along with all conceivable voltage vectors produced by inverter. Predictions of output current at next sampling interval are made for each voltage vector and forwarded to the block that calculates the quality function's value. The most popular quality function evaluates tracking performance based on deviation of anticipated current from reference current. Extra criteria, including minimum switching frequency and voltage balancing [230], can be attained by adding additional terms to quality function. Then, inverter receives the voltage vector that produces the lowest quality function value.

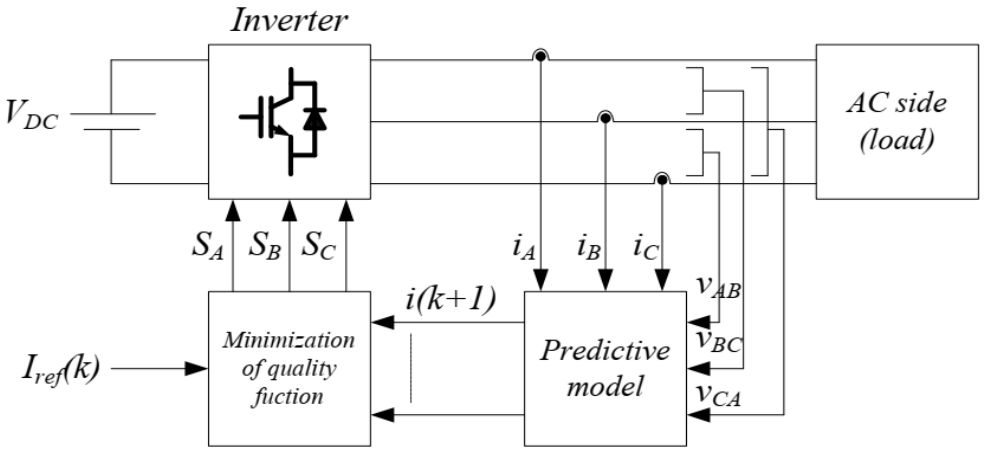


Figure 4.21: Predictive current control scheme.

The ability to account for the system's nonlinearities in the predictive model is a distinct benefit of the predictive current control scheme [231]. Adding phrases that correspond to requirements in quality function can also guarantee satisfaction of several criteria. As a result of these merits, there is a growing desire to use predictive part of this control scheme to make up for deficiencies of other, more conventional methods of control. One study, for example, found that the issue of variable switching frequency with the

DPC scheme could be resolved by adding a predictive element to the DPC scheme. This element computes the voltage vector application times in way that makes predicted active & reactive powers converge towards their respective reference values over fixed, predefined switching periods. In this way, variable switching frequency issue with DPC scheme could be resolved [232]. We can have a look at a block diagram, like that in Figure 4.22, to better comprehend this so-called predictive DPC (P-DPC) system. The predictive module, which is made up of the quality function minimization block and the power predictive model block, chooses the voltage vector sequence that can provide the least amount of line current ripple and computes application timings in way that minimises total amount of tracking error. Both of these functions are performed by the predictive module.

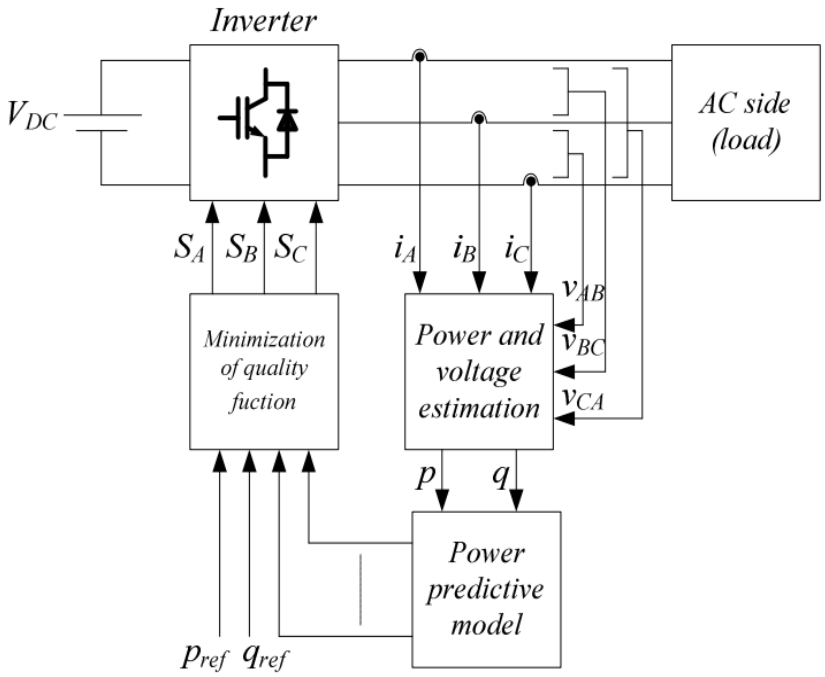


Figure 4.22: Predictive direct power control scheme.

Updates on P-progress DPCs have also been shared. The algorithm for the optimum vector selection system (OVSS) is anticipated, which uses closed-form formula to determine voltage vector needed to achieve quality function's minimum value. [233] To create synthesised vector, the calculated vector is modulated using a conventional space vector modulator. Instantaneous corrections of active & reactive powers decreased harmonic content in the current, less power & current ripple, and reduced

computing stress on the processor are all touted benefits of this technique. To cancel active and reactive power tracking errors concurrently, predictive control method based on the deadbeat control principle is proposed in another P-DPC study [234]. This algorithm calculates the necessary average voltage vector. The voltage vector switching state sequence is also generated by a space vector modulator. Predictive control for multilevel inverters has also been studied and commented on. To decrease number of calculations required for selection of ideal voltage vectors for case of 5-level CHB inverter, one study proposes an optimised technique of model predictive current control [235]. Due to great complexity of implementing predictive control scheme for multilevel inverters, it is essential that computation time be minimised.

4.10 Carrier-Based PWM Techniques (Carrier & Fundamental waveform relation)

This system operates as predicted since the switching frequency and carrier frequency are the same. When modulation is lowered to 0 or DC value, PWM spectrum just contains carrier & any harmonics, as well as components at 0 frequency, if existing. To get more information about the carrier and its harmonics, you may increase the modulation amplitude. Waveform sidebands enlarge with increasing modulation frequency.

If the pulse number is low, the carrier frequency should be synchronized with the fundamental frequency. Any even harmonics in the carrier spectrum are prevented from being included since the carrier spectrum is made up of odd multiples. Using the same carrier signal for all 3-phase leg PWM signals in 3-phase inverter ensures that all phase leg carrier spectral terms are equivalent. You can effectively remove everything except the carrier sidebands and modulating terms from a set of waveforms. Regardless of the pulse number N, this is accurate.

It’s recommended which slopes of triangular carrier and modulating waveforms should have the opposite polarity at coincident zero crossings, even if the phase connection between them is arbitrary. This is particularly true for low N. Keeping analog implementations accurate and facilitating the transition between pulse numbers in systems where this may change during operation is a practical advantage of the method. An inductive load might also benefit from this 180-degree phase mismatch. Odd N's

are the only ones that can have a connection like this. A precise phase connection between the modulating function and the carrier reduces harmonic losses exclusively for odd N. odd multiple of 3 (N = 3, 9, 15, 21, etc.) is required for all 3 phases of the inverter to accomplish carrier cancellation in phase-phase O/P of the three inverters.

The remaining carriers in M-level converter by integer pulse number are typically phase shifted with respect to the one that may fulfill these criteria. However, a multilevel converter may make use of a non-integer synchronous pulse number (such as N = 21/4) to guarantee that this phase relationship is once again relevant.

When using a multi-level converter, this requirement can only be met by one carrier since other carriers are typically phase-shifted in relation to it. If the multilevel converter uses a non-integer synchronous pulse number, such as N = 21/4, the phase connection is still acceptable.

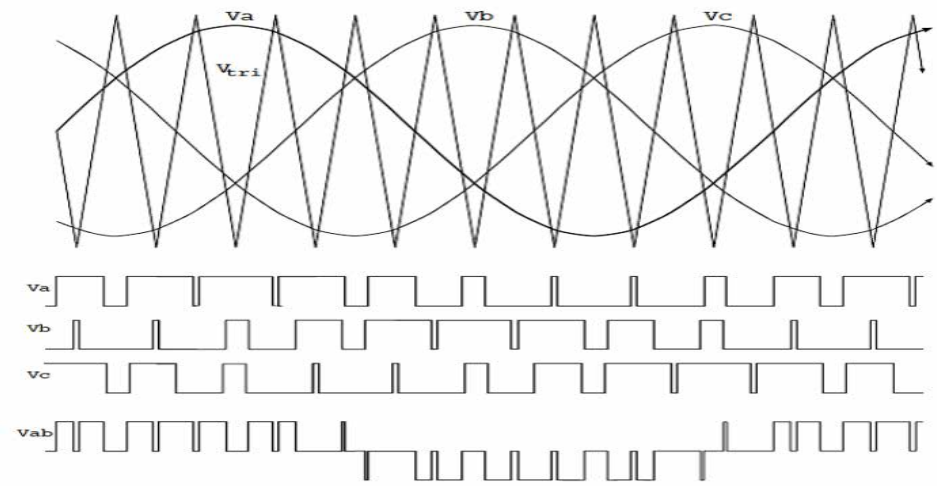


Figure 4.23: Phase leg and line-to-line waveforms in 3-phase inverter PWM.

CHAPTER- 5

MATLAB/SIMULATION & RESULTS

5.1 Introduction

As we above seen in figure.5.1 modification of the basic main circuit to modified circuit, as we have taken consideration of multilevel inverter (MLI) base circuit for the modification and enhanced the performance.

We observe that Base circuit, modified with an additional IGBT and one DC source, effectively circuit's output voltage increase one level, resultant circuit output voltage waveform improved; next stage, the same circuit is modified with one additional DC voltage source and IGBT's, effectively increases no. of output voltage levels so output of circuit will be improved.

Here are some reasons to move this multilevel inverter modification.

- We will not be able to get multilevel inverter as displayed in figure.2(c) without development of circuit (b)
- Another one, we will not be able to use an asymmetric voltage source to achieve higher number of levels with circuit (b), so it is mandatory part to modify another stage, as shown in figure.2(c).

Circuit (c) can be used to achieve 31 levels of voltage output with help of asymmetric voltage source.

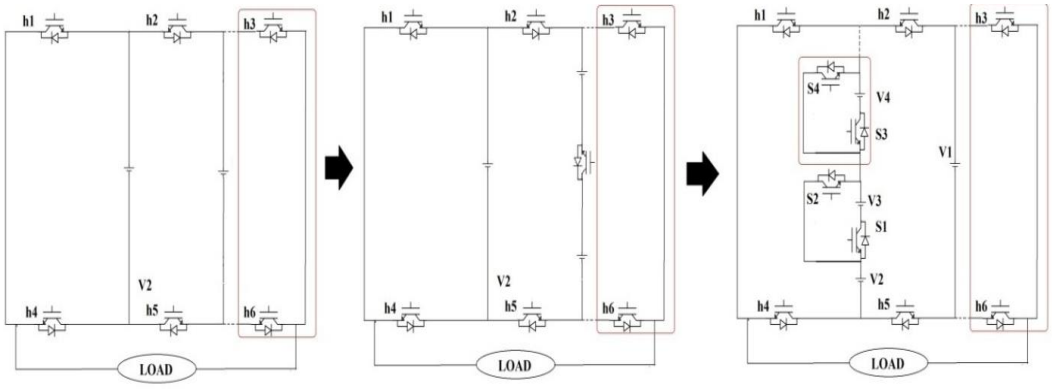


Figure 5.1: General single-phase circuit of MLI (a) Base Circuit (b)semi Cross Switched Multi-Level Inverter (c) Semi-Cascaded Multilevel Inverter

5.2 Generalized Structure of main Multi level Inverter

Figure 5.2 depicts this architecture's singular-phase generic structure. There are n different, abundant DC sources. The linking arrangement will function similarly to how a switching device might connect a prior source's higher prospective node to a following source's relatively lower terminal or vice versa. Authorities for input voltage fall within the Ej and E2j categories (wherever j is equal to 1- n). From each source, the source current is denoted by ij(t). Using a transistor unit [such a MOSFET or an IGBT] and an anti-parallel diode, it was possible to activate power switches. Numerous powered semiconductor switches, such as anti-parallel diode IGBTs, have been shown in fig. 5.2 alone. A parallel pair has also been demonstrated to be (Tj, Tj) (where j ranges from 1 to n + 1). The numerous nodal voltages are designated as vj(t) (where j ranges from 1 to n + 1). The symbols for load voltage and load current are, respectively, vL(t) & iL(t).

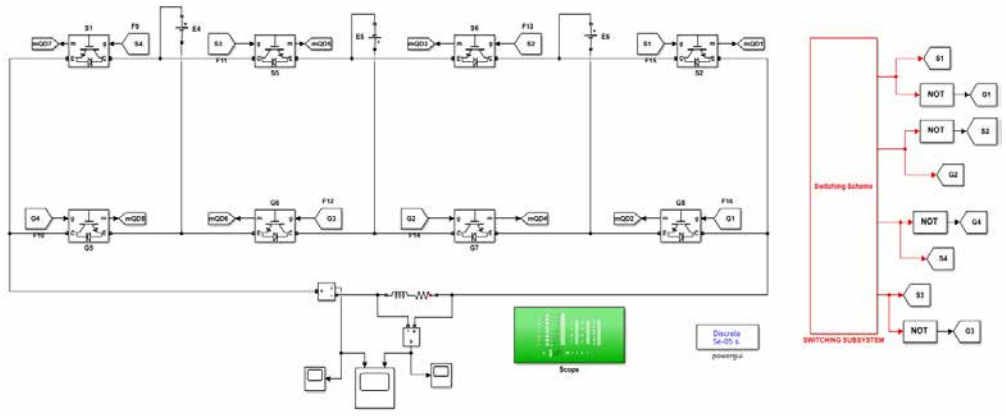


Figure 5.2: 3 input suppliers for single-phase converters that depend on topology

5.3 Working Principle

As illustrated in Figure 5.2, assistance of 1-phase dc to ac converter with 3(E1, E2, and E3) dc input sources define the working theory of this topology. Four switch pairs (Tj, Tj) (j = 1, 2, 3, 4) are currently active in this circuit. Due to the complementary nature of the elements that make up these teams, appropriate functioning modes have existed.

Through use of the modes of operation, the load is transferred to the 10 working stages (E1, E2, E1+E2, E1+E2+E3).

- Stage 1: - When G1, G2, G3, and G4 are on, circuit's output at the load side is 0V.
- Stage 2: -When S1, G2, G3, and G4 are on, circuit's output at the load side is E1=12V.
- Stage 3: -When S3, S4, G1, G2 are on, circuit's output at the load side is E2=24V.
- Stage 4:- When S1, S2, S3, and G2 are on, circuit's output at the load side is E1+E2=36V.
- Stage 5: -When S1, S3, G2, and G4 are on, circuit's output at the load side is E1+E2+E3=48V
- Stage 6: -When S1, S2, S3, S4 are on, circuit's output at the load side is 0V as expected.
- Stage 7: -When G1, S2, S3, and S4 are on, circuit's output at the load side is -E1=-12V.
- Stage 8: -When G1, G2, S3, and G4 are on, circuit's output at the load side is -E1-E2=-24V.
- Stage 9: -When G3, G4, G1, S2 are on, the circuit's output at the load side is -E1-E2=-36V.
- Stage 10: -When G1, S4, G3, S2 are on, the circuit's output at the load side is -E1-E2-E3=-36V.

5.4 Numeric Formulations

As per fig. 1, T_j & T_j (*wherever j is equal to 1 to n + 1*) switches function successively. Suppose S_j be switch equation equivalent to T_j switch specified as

if $T_j$is on, S_j= 1,

if $T_j$is off , S_j= 0,

Node load voltage $v_L(t)$, in contrast to nodal voltages $v_j(t)$, can then be defined as

$$v_L(t) = \sum_{j=1}^{n+1} v_j(t)$$

Where

$$v_j(t) = (-1)j(1 - S_j)(E_j + E_j - 1)$$

Taking j = 1 to n + 1 & $E_0 = E_{n+1} = 0$ as No such type of sources are available. Using (1) & (2)

$$v_L(t) = \sum_{j=1}^{n+1} [(-1)^j(1 - S_j)(E_j + E_{j-1})]$$

Also, input current i_j(t) could be defined with context of switch functions and load current i_L(t) via a specified input source

$$E_j(j = 1\ ton)asi_{L(t)}$$

$$i_j(t) = (-1)j + 1(S_j - S_j + 1)i_L(t)$$

Voltage stress $V_{stress, j}$ for 2 switch pair switches jth (Tj, Tj) can be expressed as

$$V_{stress,\ j} = E_j\text{-}1 + E_j$$

Even if there are multiple DC voltage sources that can be used as input, anywhere j is equal to 1 to n + 1, E0 = 0, and En+1 = 0, none of these sources exist. Switch pairs (T1, T1) and (Tn+1, Tn+1) raised voltage stresses corresponding to Vdc for each with anti-symmetric DC source inputs, i.e. E1 = 12V, E2 = 24V, E3 = 12V, whereas voltage stress is equivalent to 2Vdc for each residual witch.

Additionally, topology synthesises a certain number of layers, which is provided by

$$N = 2n + 1$$

5.5 Switching Scheme

For MLI modulation control, high switching frequency modulation techniques can be utilised, like multicarrier PWM and SVM approaches. As opposed to that, fundamental frequency, active harmonic, and selective harmonic removal techniques may be utilised as low switching frequencies. Such a framework can be adjusted using any of these methods for optimal adaptation. In the current job, a multi-carrier PWM structure is being used. In a multi-carrier PWM method, carrier signals are compared to reference signals. Devices with input voltages equivalent to those received have been transferred using the signals received. At the output voltage of this design, each switch has the potential to result in the synthesis of many additional layers. The proper use of ten modes (i.e., modes 1, 2, 3, 5, and 10) would also aid in the critical switching for T2 & T2, each with a 2Vdc voltage stress, as opposed to residual switches with a Vdc voltage stress. To achieve the nine-stage output stated in this section, control strategy where such modes are utilised is necessary. High-stage inverters can be added to the technique, though.

5.6 Modulation Scheme

Related waveforms are shown in the schematic representation of the modulation technique in Figures 5.3 and 5.4. As carriers, there are four triangular signals with frequency of 18 kHz. The alternative opposing stage layout is how the carrier waves are constructed. As a signal for comparison, a sinusoidal waveform with frequency of 50 Hz has been used. Carrier waves are labeled as c+ k(t), where k's values are well above the reference of "0," and as c- k(t), where k's values are well below the reference of "0." The reference and the carriers underwent a consistent analysis. The comparator supplies 'k' in all other cases, and 'k - 1.' is provided. The reference is low in comparison to carrier c+ k(t). The comparator grants '-(k - 1)' when the reference is greater than carrier c-k(t). As an alternative, it offers "-k." Applying the gathered signals results in a consolidated (t) signal. A 1:1 link between levels utilised in the (t) signal and their equivalent levels in output signal is employed to produce switching pulses from the (t) signal. A (t) signal is compared to constant levels in order to get the same result, and the output is then provided using a lookup table, as shown in table II, with switches

referring to stage. The O Red pulses gate each and every switch for each level to which it contributes.

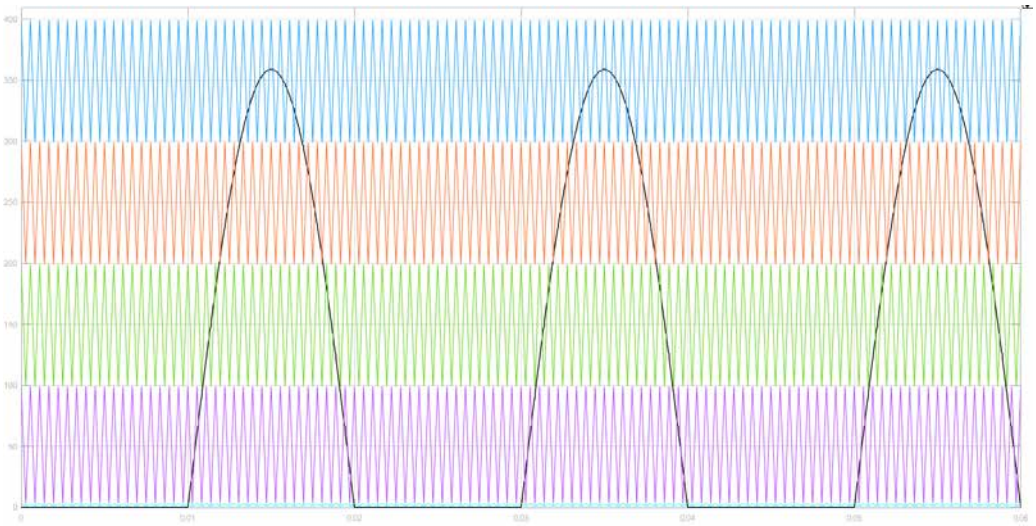


Figure 5.3: Waveforms of carrier and reference for arrangement for Output Nine-level

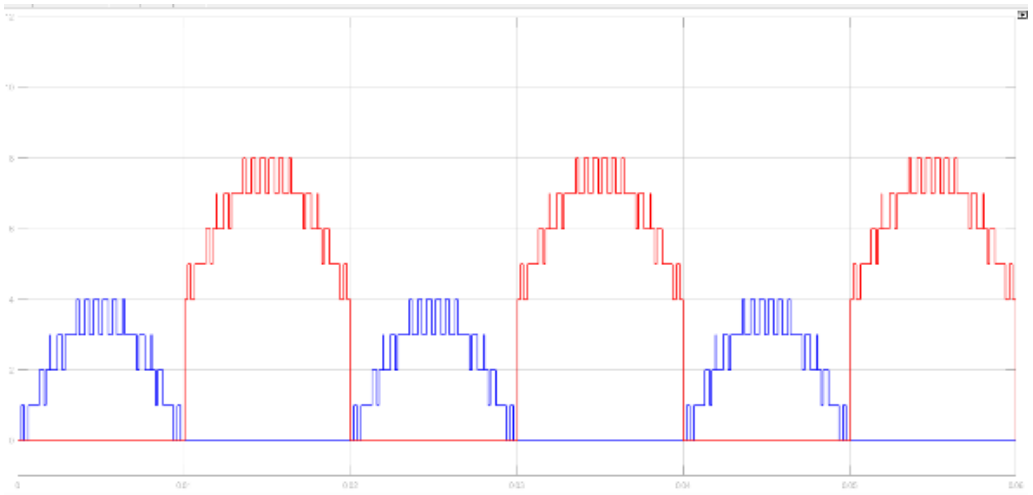
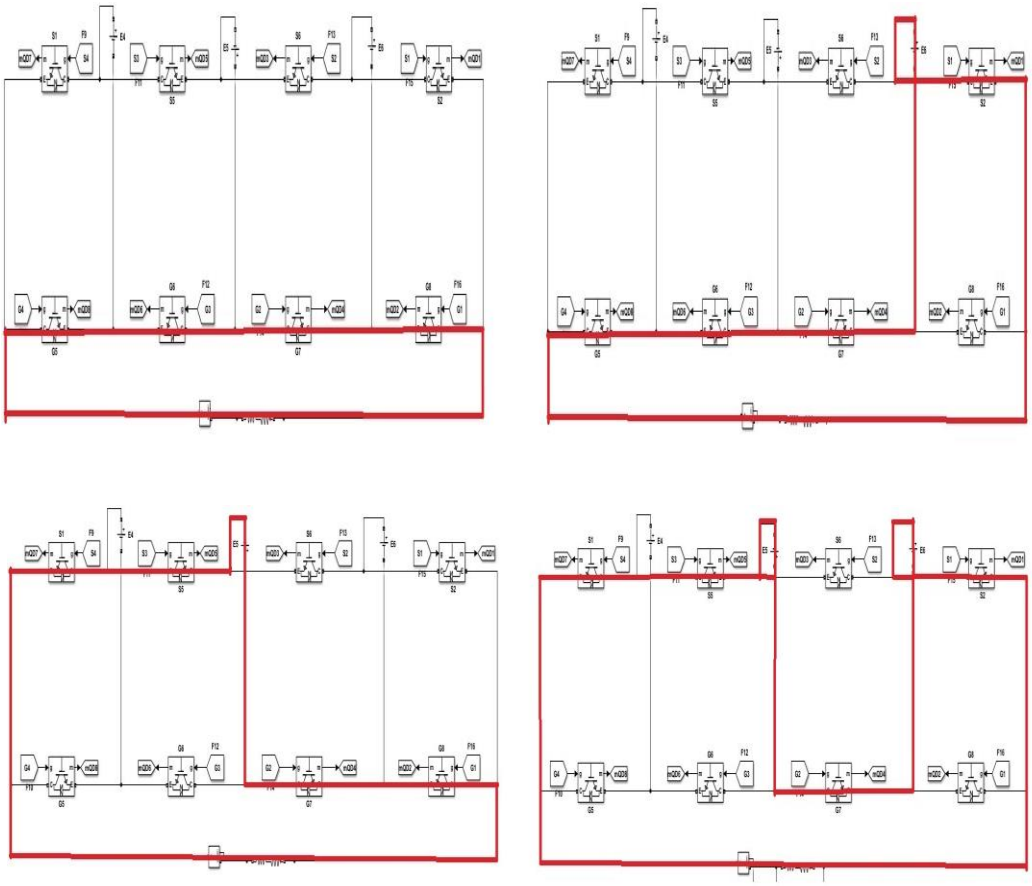


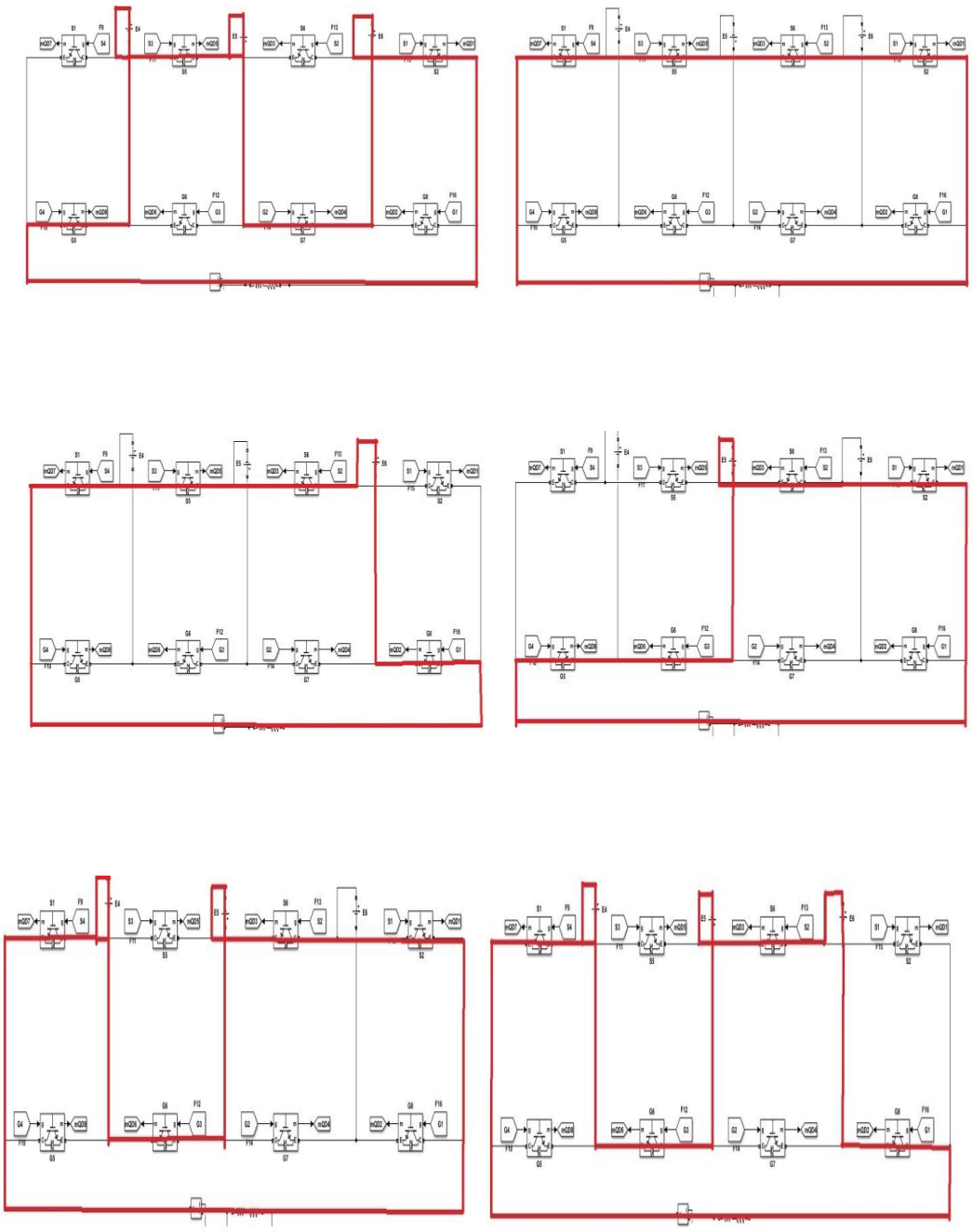
Figure 5.4: Aggregated signal

To evaluate effectiveness of this topology and the control mechanism, a single-phase nine simulation framework is used.

Table 5.1: Lookup Table Based on Topology for the 9-Level Inverter

Voltage Levels	Modes	Load Voltage[V]	Switches ON State
0	1	0	G1, G2, G3, G4
E1	2	12	S1, G2, G3, G4
E2	3	24	S3, S4, G1, G2
E1+E2	4	36	S1, G2, S3, S4
E1+E2+E3	5	48	S1, G2, S3, G4
0	6	0	S1, S2, S3, S4
-E1	7	-12	G1, S2, S3, S4
-E2	8	-24	S1, S2, G3, G4
-(E1+E2)	9	-36	S1,S2, G3, S4
(E1+E2+E3)	10	-48	G1, S2, G3, S4





The multi-level inverter is conceptualised using MATLAB software. When E1 = 12V, E2 = 24V, and E3 = 12V are employed, 3 input DC sources must be utilised. The switching pulses that were thusly acquired are shown in figure 3, which shows that T2 and T2 switches operate at fundamental 50 Hz frequency, whereas T1, T1, T3, and T3 switches operate at an 18-kHz frequency. High-voltage switching operates at a fundamental frequency and causes more conduction losses, whereas low-voltage

switching operates at very high frequencies that cause maximum switching losses. This is how total losses between switches are allocated.

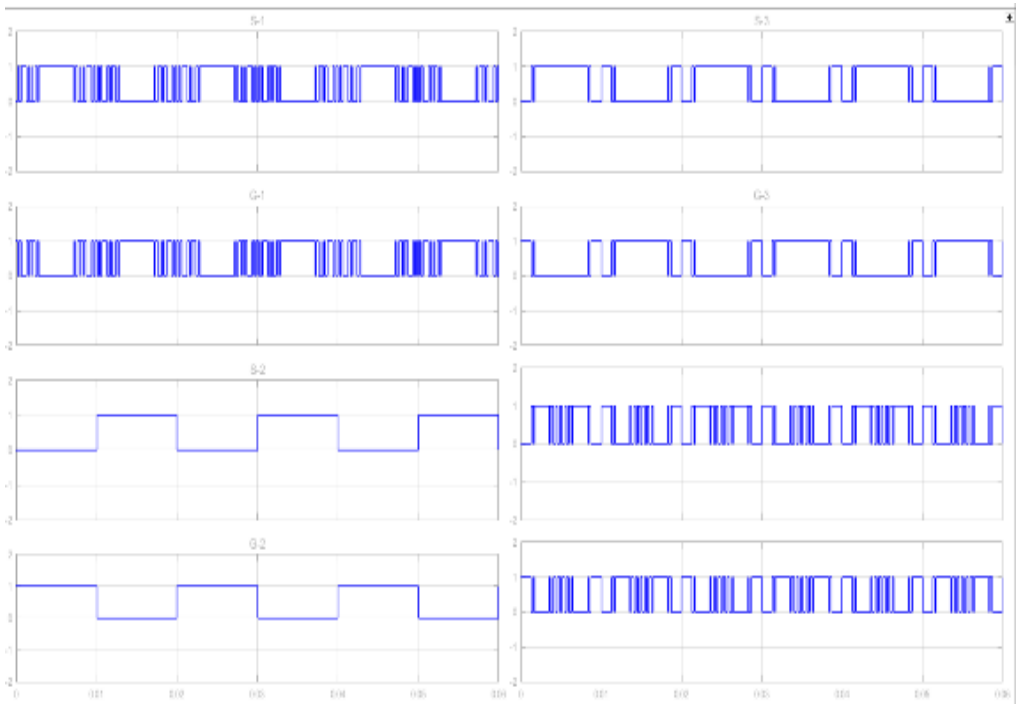


Figure 5.5: Waveform design switching for 9-stage converters

Table 5.2: System Specification -1

Parameters	Value		
Frequency of reference	50 Hz		
Frequency of Carrier	1800 Hz		
Resistance to Load	1Ω		
Inductance of load	Three mH		
Source from DC	E1=12v	E1=24v	E1=12v

THD profile for load voltage and harmonic continuum is illustrated in Figures 9 and 10, which shows that 9-level voltage waveform has equivalent 24 V per step and 2.78 percent THD (total harmonic distortion). Furthermore, with R-L load (L = 2 MH and R = 2Ω), its harmonic spectrum and load current signals are displayed in figures 6 and 7, respectively.

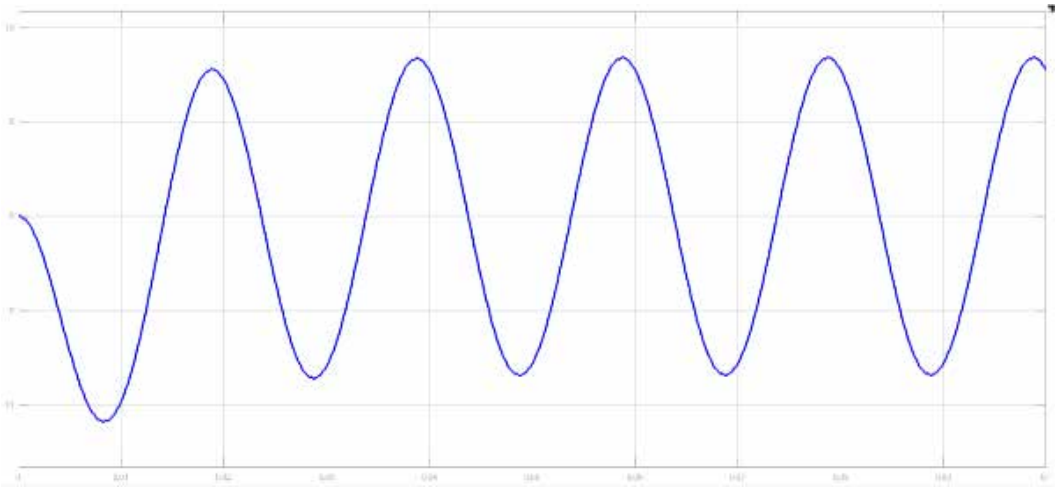


Figure 5.6: 9- level Inverter output current simulations outcome

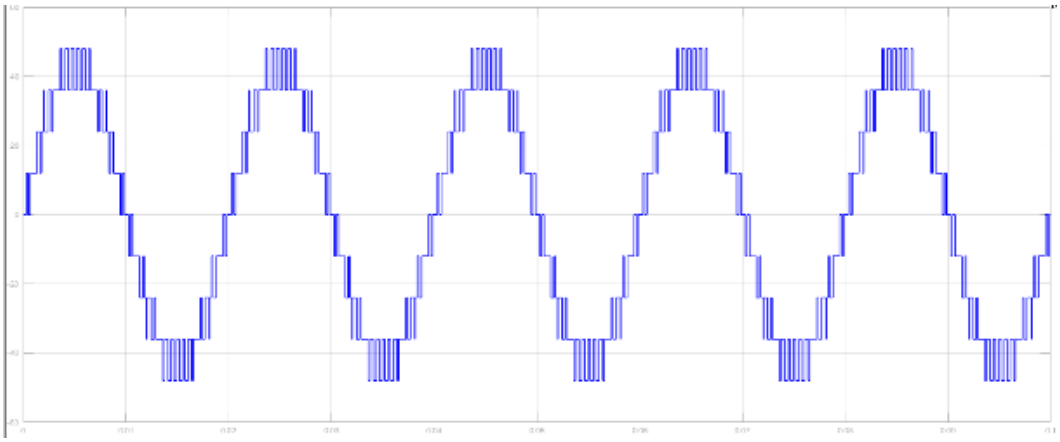


Figure 5.7: 9-level Inverter output voltage simulations outcome

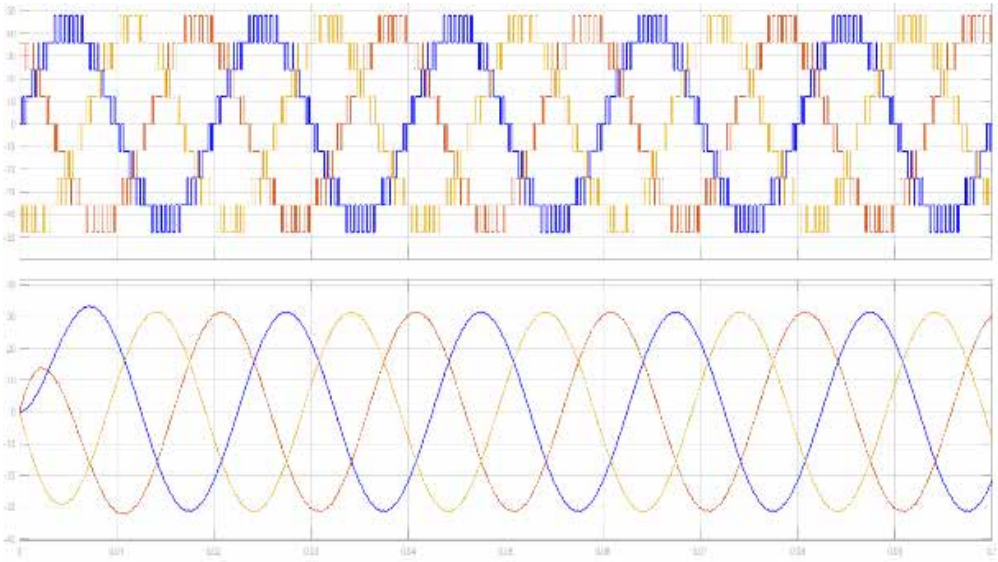


Figure 5.8: Outcomes of the simulation. (a) Three Phase Nine-level output voltage.

(b) Nine-Level Three-phase Current Output

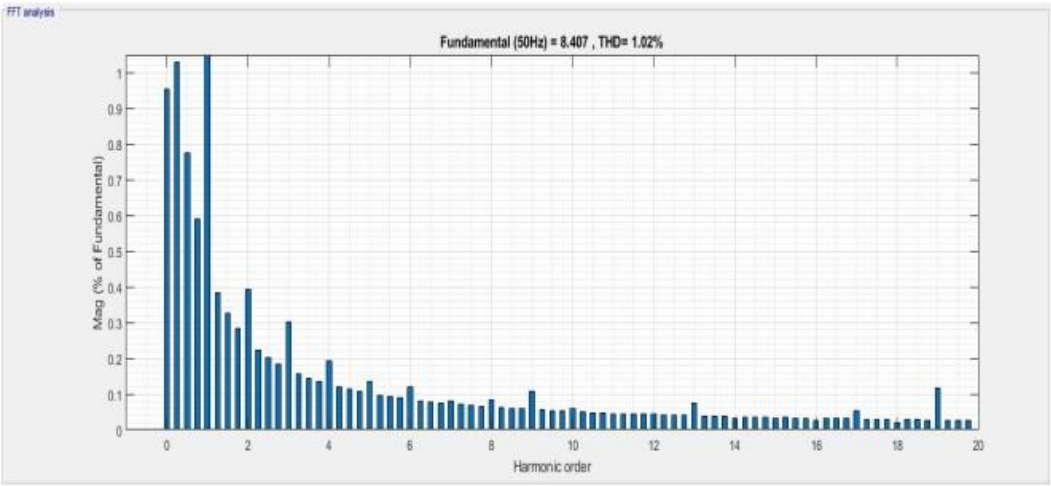


Figure 5.9: Simulation performance of load current harmonic spectrum

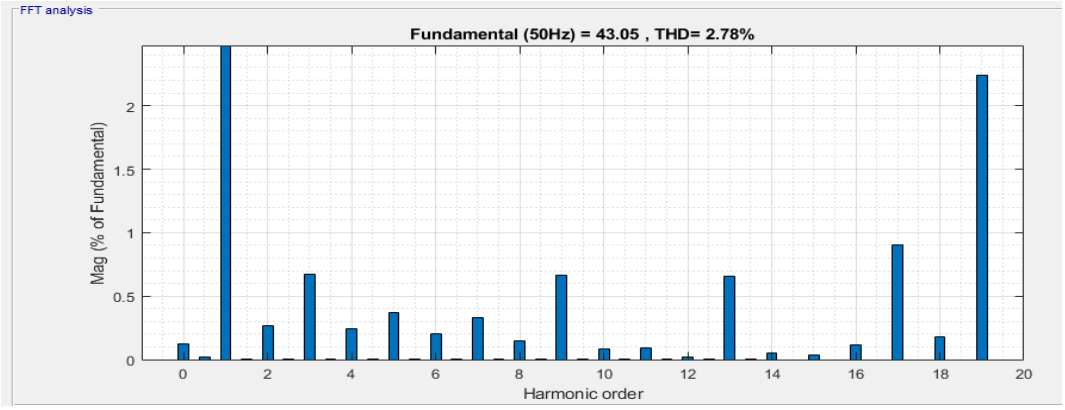


Figure 5.10: Simulation outcomes of load voltage harmonic spectrum

5.7 Generalised Structure of Semi-Cross Cascaded Multilevel Inverter

As illustrated in Fig. 5.11, assistance of 1-phase DC to AC converter with 3 E1, E2, and E3 DC input sources defines this topology's operational theory. There are four active switch pairs in this circuit: Tj, Tj (j = 1, 2, 3), and H_i. As a result of the complementary nature of the members of such teams, appropriate working modes have existed. \

Table 5.3. System Specification - 2

S.no.	Parameters	Specification
1	Number of DC Voltage	3
2	IGBT	7
3	Diode	7
4	Switching Frequency	1.2e3
5	Input voltage	100
6	Load resistance	1 ohm

Through use of the modes of operation, the load is transferred to the 10 working stages (E1, E2, E1+E2, E1+E2+E3).

Table 5.3 shows the specification of the circuit, and circuit continuous working with same configuration.

Also observation shows that every different circuit has the different carrier frequency which clearly responsible for the lowest THD profile, as already discussed about pulse width define the on period and off period of the IGBT, which is control the THD profile so carrier frequency play main role, this carrier signal compared with the reference signal, this compared signal produces gate firing pulses, this discussion clearly shows that frequency also play main role to width control of firing pulse as number of devices increases and need to increase the carrier frequency accordingly.

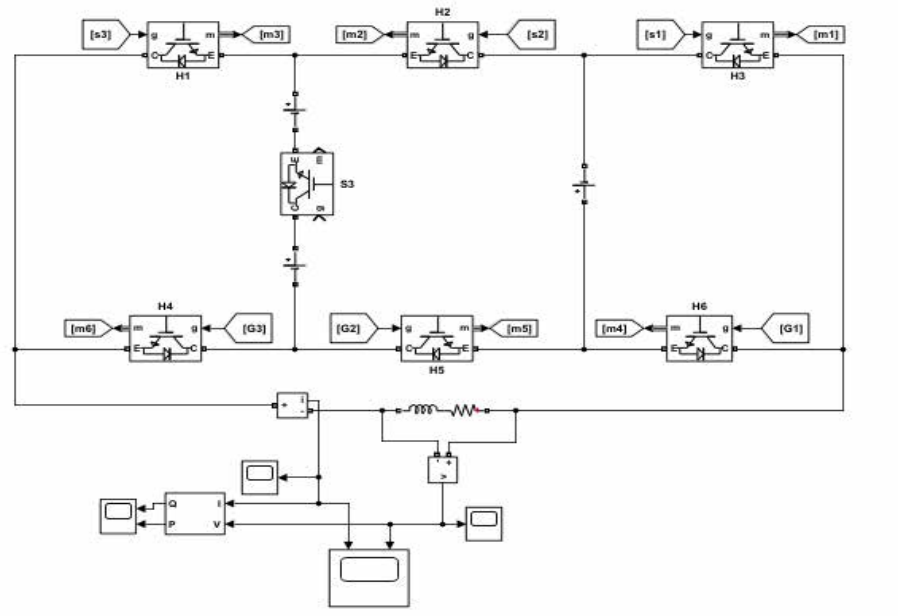


Figure 5.11: Generalized Structure of Semi-Cross Cascaded Multilevel Inverter

- **Stage 1: -**

  The switches s1, s2 and s3' are in ON state.

  The voltage across this load is +Vdc.

- **Stage 2: -**

  The switches s1, s2', s3' and s4' are in ON state.

  The voltage across load is +2Vdc.

- **Stage 3: -**

  The switches s1, s2', s3' and s4' are in ON state.

  The voltage across load is +2Vdc.

- **Stage 4: -**

  The switches s1, s2', s3' and s4' are in ON state.

  The voltage across load is +2Vdc.

- **Stage 5: -**

  The switches s3, s1' and s2' are in ON state.

  The voltage across this load is –Vdc.

- **Stage 6: -**

  The switches s2, s3, s1'and s4'are in ON state.

  The voltage across this load is -2Vdc.

- **Stage 7:-**

  The switches s1, s3, s2'and s4' are in ON state.

  The voltage across this load is -3Vdc.

It's also important to note that in this study, input dc voltages were regarded as being equal. These could change if the sources are PV (photovoltaic) devices (Because of different battery power states or because certain cells are illuminated, for instance). Due to this variation, either hardware-based methods (such as using independent converters [8]) or power-aglow methods (such as the battery handling method [19]) could be used.

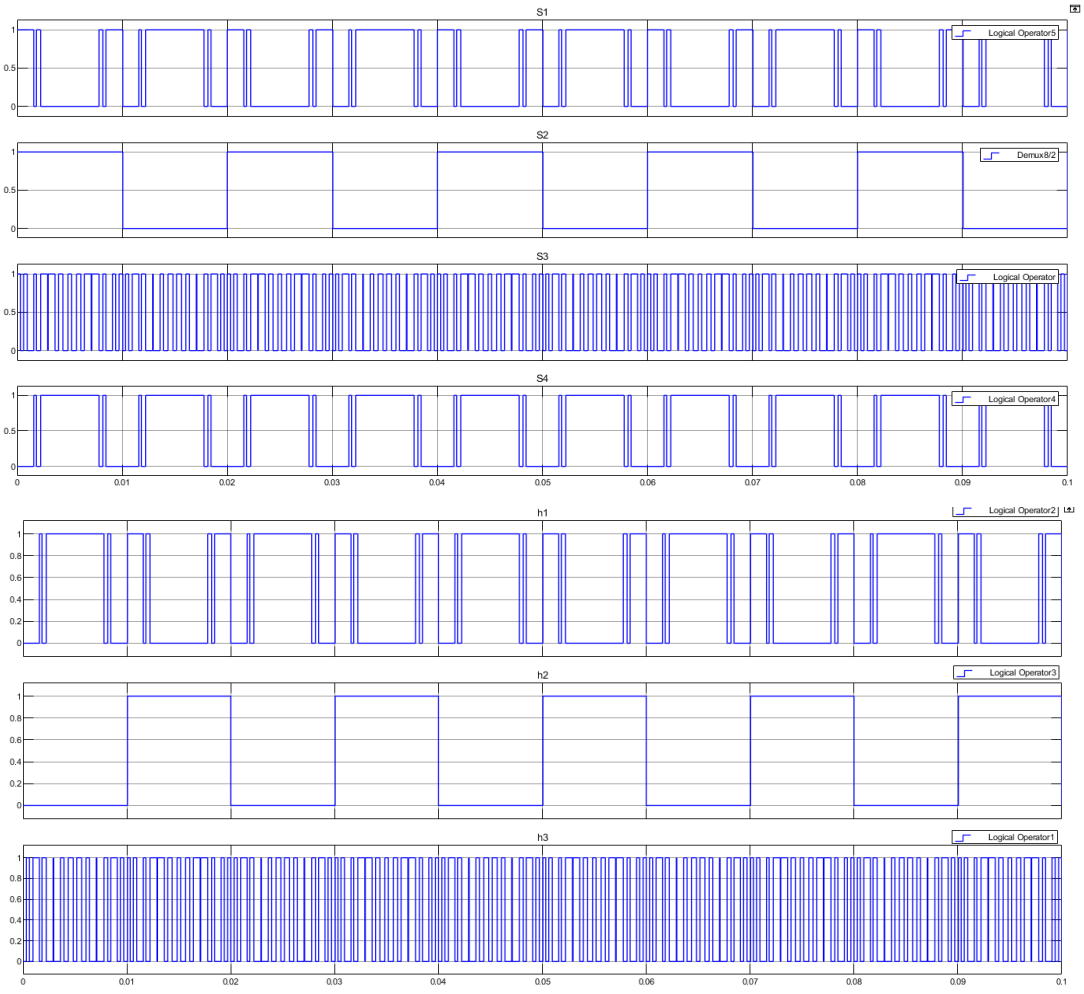


Figure 5.12: Firing pulses of Semi-Cross Cascaded Multilevel Inverter

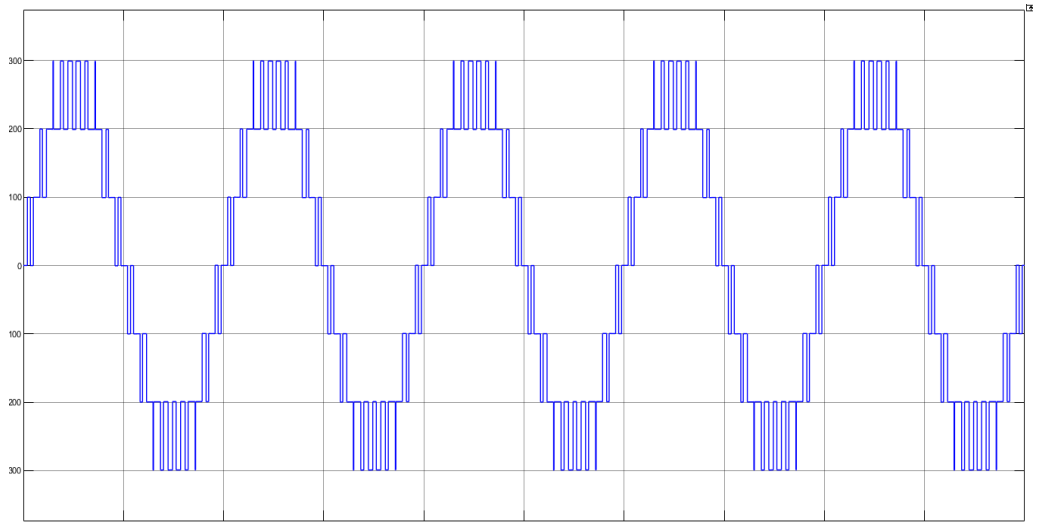


Figure 5.13: Output Voltage wave form of Semi-Cross Cascaded Multilevel Inverter

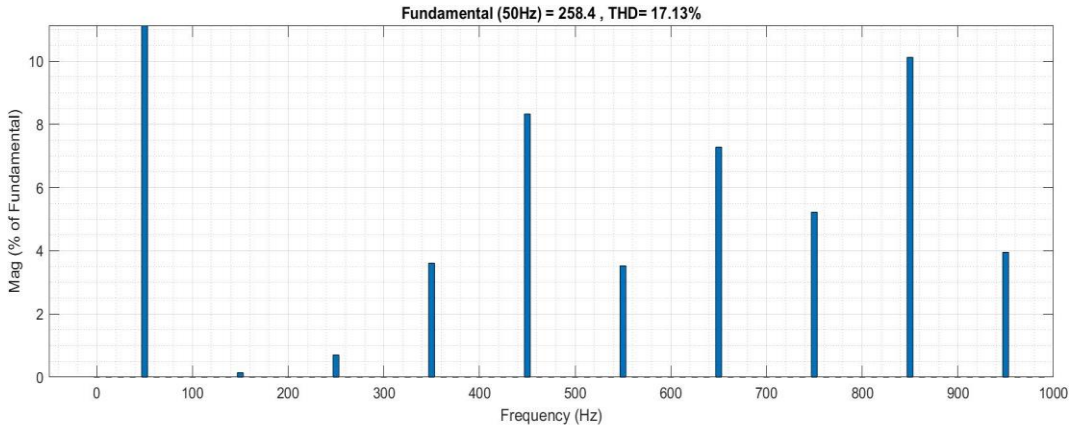


Figure 5.14: Total harmonic distortion profile of voltage waveform of Semi-Cross Cascaded Multilevel Inverter

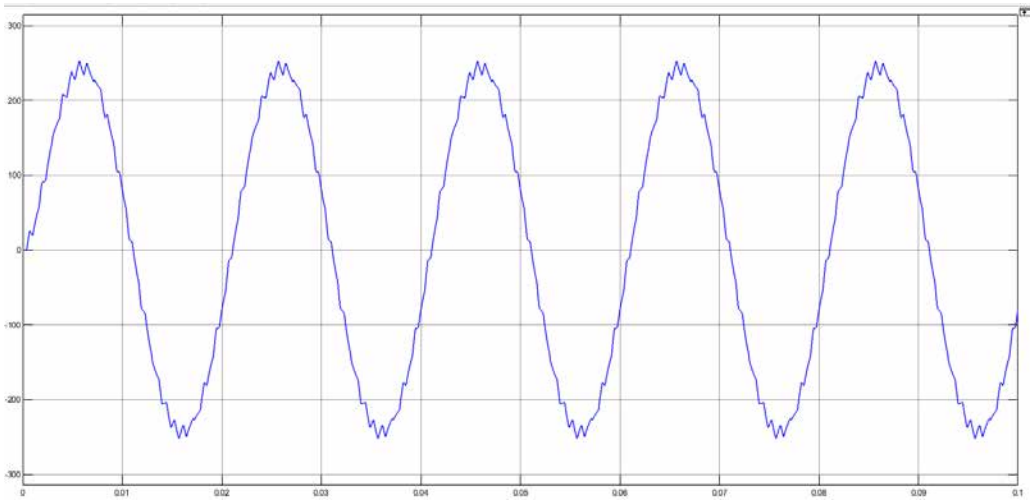


Figure 5.15: Output current wave form of Semi-Cross Cascaded Multilevel Inverter

5.8 Generalized Structure of Semi-Cascaded Multilevel Inverter

The no. of components needed in Multilevel Inverter topologies according to the input DC voltage. It indicates that no. of levels increase as input DC voltage increases. The essential components in the configuration of a multi-level inverter are semiconductor devices and accompanying simple drive circuits. As even the no. of components rises, the size and price of the multilevel inverter will also increase, as well as the complexity of control system will upsurge. Figure 5.16 depicts the structure of a Multi-Cell Multilevel Inverter.

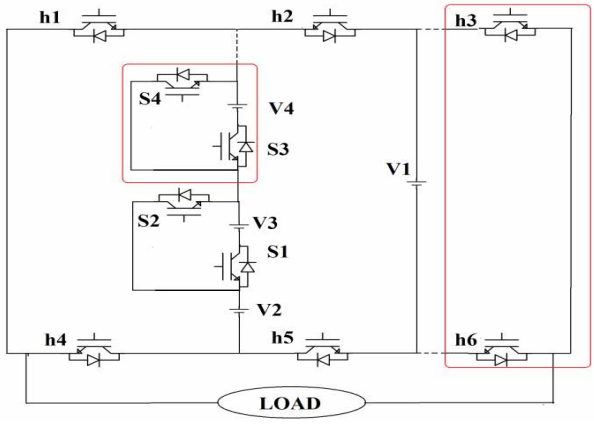


Figure 5.16: Semi-Cascaded MLI

This circuit is implemented with help of the symmetric DC voltage supply, and when taking 4 symmetric voltage sources, it can achieve 9-level of output, and it can further

increase its output level by increasing number of cells or employing asymmetric DC voltage supply; it can achieve 31-level of output voltage with the same circuit by some modification in firing scheme, this is the one advantages of this circuit.

The presented circuit is motivated by preceding semi Cross Circuit switching Multilevel Inverters as mentioned Figure 5.16 and the appropriate linkage of many forms of cells with the help of 10 semiconductor devices that provide divergent routes to start generating the output voltage waveform within all phases with both positively and negatively polarization in output. Every cell is made up of semiconductor devices and one direct current source (DC voltage source). It's also worth noting that $V_1 = V_{dc}$ inside described architecture. Unique DC sources voltage in each cell are used to generate a given output voltage waveforms. The offered inverters are capable to supply the number of each DC supply in the outputs. As a result, the highest voltage inside the outputs would equal the total of the amplitudes of DC supply. The max output voltage ($V_{o,\,max}$) of architecture has represented by Eqn. (1)

$$V_{o,Max}=\sum_{i=1}^{n} V_i \qquad (1)$$

Wherever = no. of DC sources

Each switching causes unwanted drop of voltage, which seems referred to as power losses in the form of switching and conduction loss. Switching loss occurs whenever the switch is moved from an OFF to an ON and conversely. Conduction loss will create on duration of ON state. To compute the maximal voltage output, the ON-mode power loss of switching is considered to be Vdc, therefore eqn. (2) assesses the maximal voltage output when everyone switching power loss is included.

$$V_{o,\,Max}=\sum_{i=1}^{n} V_i - (n+2)V_d \qquad (2)$$

For asymmetric topology

$$V_{o,Max}=\sum_{i=1}^{n} V_i - (n+1)V_d \qquad (3)$$

For symmetrical topology

The switch voltage ratings are a key issue in multilayer inverters. The overall peak inverse voltages (PIV) of the switch is determined using the eqn. (4) below.

$$PIV=\sum_{j=1} \quad PIV_{Switchj} \tag{4}$$

1. Symmetrical

Magnitude value of all DC voltage sources is equivalent to V_{dc} for symmetric inverters. In considering the symmetric architecture, the switch associated with a single DC supply, figure 3, depicts the symmetrical inverter provided. The possible max voltages and also the number of operating voltages (m) inside the intended symmetrical inverters are described in the subsequent formula.

$$Vo \ max = n \times Vdc \tag{5}$$

$$m = 2n + 1$$

2. Asymmetric

DC power supplies of different cells in intended asymmetrical MLI are not equivalent. The same cell count, asymmetrical inverters deliver more stages in the output current than in its symmetrical equivalent.

The DC voltage of the separated cell in Figure 3 is determined as per a geometric sequence with a component of p in the asymmetrical scheme.

$$V_i = p_{i-1}V_{dc} \tag{6}$$

wherever p is 2,i belongs from 1 to n

For n DC source, Max. Voltage and no. of Voltage stages are as follows

$$V_{o,Max}=\frac{1-p^n}{1-p}V_{dc} \tag{7}$$

$$M=2\frac{1-p^n}{1-p}+1 \tag{8}$$

Wherever, n = no. of Dc source

3. Switching Scheme

The inverter's modulation schemes are critical since they are directly connected to total performance of system. MLI has investigated many forms of modulation schemes. It's utilized to manage output voltage/current and to calculate MLI's two key parameters, low switching & percentage of THD. A modulating signal's goal was to provide a stepwise waveform which is the closest estimate of the particular reference signal, including variations in amplitude level, frequencies, and a vital element, i.e., typically sine's wave in steady-state. The simple visual depiction of total modulation approaches is displayed. Depending on the switch's frequencies, the two main kinds of modulation methods used in Multi-cell multilevel inverters are Fundamental carrier frequency & fast switching frequency. The 2 basic kinds of fast switching frequencies are PWM and space vector modulations.

In Multi-cell Multi-level inverter modulator controls, high-switching-frequency modulation approaches such as multi-carrier levels switch PWM has been applied. Low-switching-frequency approaches, on the other side, include proactive harmonics removal, selective harmonic, and also the Fundamental switching frequency technique. This design may be changed using any one of these ways with appropriate adaption. The multi-carrier PWM system is employed in this article. Inside a multi-carrier PWM system, carrier's signals are equated by the reference signals, & also the resulting waveforms are utilized to switch tools at different voltage levels. In this design, 1 switch can assist in the synthesizing of many levels at the output terminals. Furthermore, as previously stated, appropriate usage of 10 modes (namely, modes 1, 2, 3..., & 10) would result in basic T2 and T2 switches that carry voltage stress of 2-V_{dc} each one as opposed to other switches that carry voltage stress of Vdc respectively. As a result, in this part, a control method is provided where such a move is used to generate 9-level outputs. Nevertheless, the operation could be applied to high-level inverters.

5.8.1 Modulation Scheme

The modulation scheme's circuit illustration is represented in Figure. 5.17, & also waveform is represented in Figure 5.18. For carrier, the 4 triangular waves with frequencies of 2.2 kilo Hertz each are employed. Carrier's signals are typically arranged in alternating phases oppositional [3]. This reference signal is a sine waveform with a

frequency of 50 hertz, but it has been converted sine wave into full wave rectified signal because ease of use, so half rectified signal finished at 0.01 another rectified signal has started after phase shift of 0.01 and finished at 0.02, which is similar to the 50hz frequency. Carrier signals that are higher than the 0 reference value are denoted by way of "$C^{+}_{k(t)}$"where k ϵ 1, 2, 3 and 4, whereas all individuals who are lower than the 0 reference value are marked by way of "$C^{+}_{k(t)}$" where k ϵ 1, 2, 3 and 4. This reference is compared to the carriers continually. Then comparator returns "k" if the references are higher to carriers $C^{+}_{k(t)}$; else, it returns "k(t)". Whether the reference frequency is more than the frequency of carrier "$C^{+}_{k(3)}$" then comparator returns "$C^{+}_{k(2)}$" else returns "$C^{+}_{k(1)}$". The acquired signals have combined for making aggregate signal, i.e., a(t). To generate the switching signal via signaling a(t), a 1:1 correspondence between both the level in aggregate signal a(t) displayed in figure 6 and level in output waveforms are used. To do this, signals a(t) are checked to constant current density, and also the outputs are sent to switching correlating to a level to use the hash table provided in Table II. The ORed signals for the levels give 0s to gates for every switch.

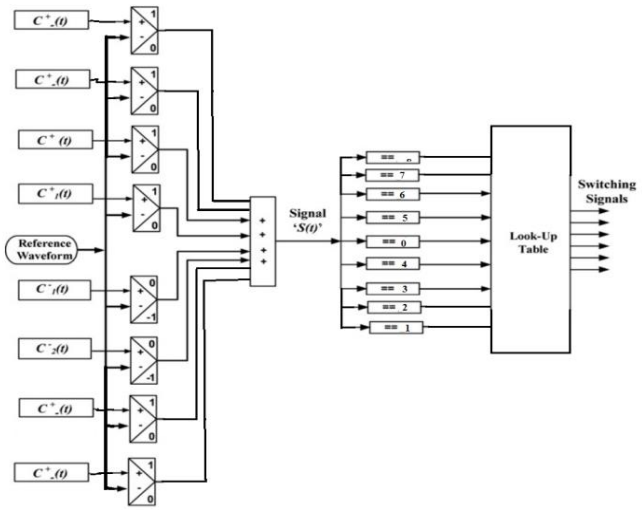


Figure 5.17: Multi-level inverter using a control scheme

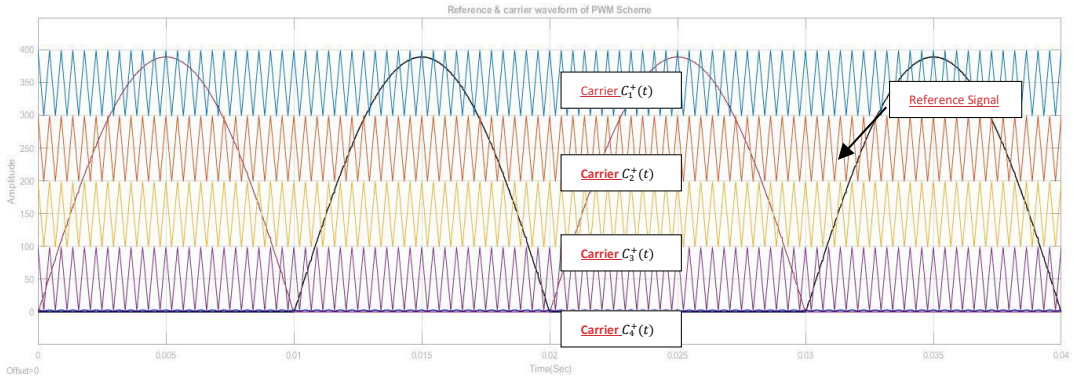


Figure 5.18: Reference waveform & carrier waveform for 9-level output scheme.

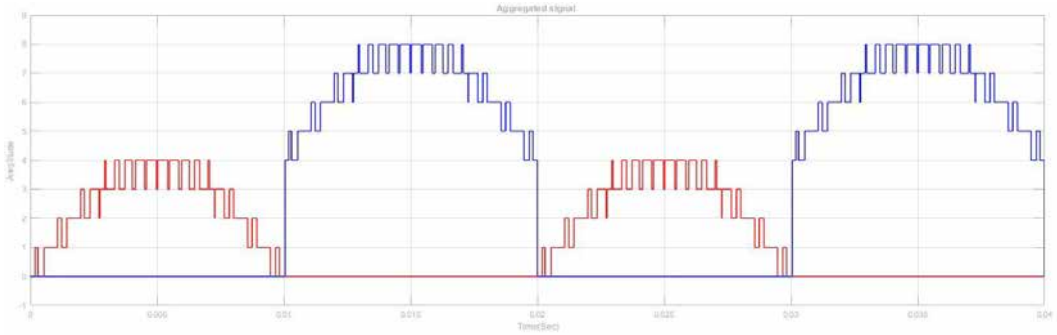


Figure 5.19: Aggregated signal

The MATLAB/Simulink tool is employed to make a MLI. 4 input DC sources are employed, where E_1 = 100V, E_2 = 100V, E_3 = 100V, and E_4 = 100V. The resulting switch pulses are displayed in Fig. 5.19, and their switch statistics are presented in Table 5.5; this reveals that switching h_2 & h_5 function at a core frequency of approximately 50 Hz, whereas switching h_1, h_4, h_3, and h_6 work at a freq. of 2.2 kHz. Therefore, lower-voltage-rated switches run at the higher frequencies, incurring switching loss, whereas higher-voltage-rated switches work at core frequencies, incurring a higher conductive loss. The net loss among the switching is allocated in this way.

Table 5.4: Parameters for System

Parameters	**Values**			
Reference freq.	50 Hertz			
Carrier freq.	2200 Hertz			
Load inductance	3 mH			
Load resistance	1ohm			
Dc source	E1=100V	E_2=100V	E_3=100V	E_4=100V

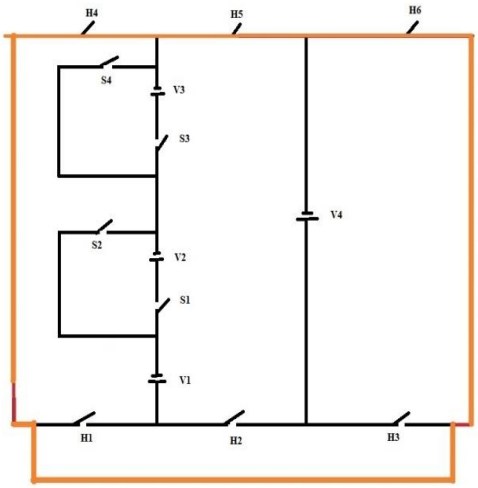
Figures illustrate the load voltage waveforms and also its harmonic spectra; results reveal that the 9-level reference voltage has equivalent stages at 100 Volts each and a THD of 1.07 percent. Furthermore, given an R–L load, the load current waveforms (where R = 2 & L = 2 mH), then also its harmonics spectra, that is 0.14 percent.

Table 5.5: Number of modes, Nodal Voltages, Switch States & Source Currents for Topologies on 4-input sources

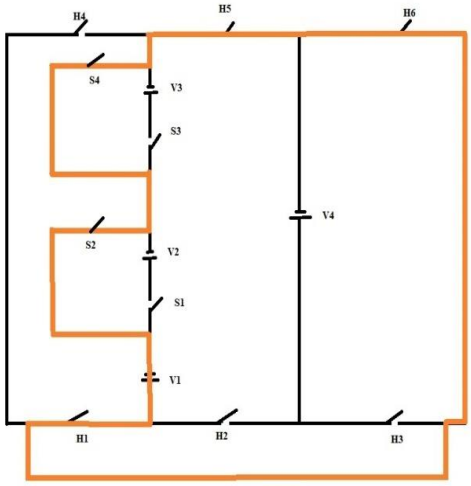
Voltage Levels	**Modes**	**Load Voltage[V]**	**Switches ON State**									
			S_1	**S_2**	**S_3**	**S_4**	**H_1**	**H_2**	**H_3**	**H_4**	**H_5**	**H_6**
0	1	0	0	1	0	1	1	1	1	0	0	0
E1	2	100	0	1	0	1	0	1	1	1	0	0
E1+E2	3	200	1	0	0	1	0	1	1	1	0	0
E1+E2+E3	4	300	1	0	1	0	0	1	1	1	0	0
E1+E2+E3+E4	5	400	1	0	1	0	0	1	0	1	0	1
0	6	0	1	0	1	0	1	0	0	1	1	1
-E1	7	-100	0	1	0	1	1	0	0	0	1	1
-(E1+E2)	8	-200	1	0	0	1	1	0	0	0	1	1
-(E1+E2+E3)	9	-300	1	0	1	0	1	0	0	0	1	1
-(E1+E2+E3+E4)	10	-400	1	0	1	0	1	0	1	0	1	0

There are ten working states of the proposed circuit, by which got different nine levels, four different output produce positive half wave another four states produce negative half wave which as follows: -

- **State I.: -** To achieve voltage level (V_L= '0') on connected load side, switches H_4, H_5 and H_6 are ON. In this state, total output voltage is zero at Load.
- **State II.-** To achieve a voltage level (V_L= '+V_1' =100V) on the connected load side, switches H_1, S_2, S_4, H_5, and H_6 are ON. In this state, total output voltage is 100V at Load.



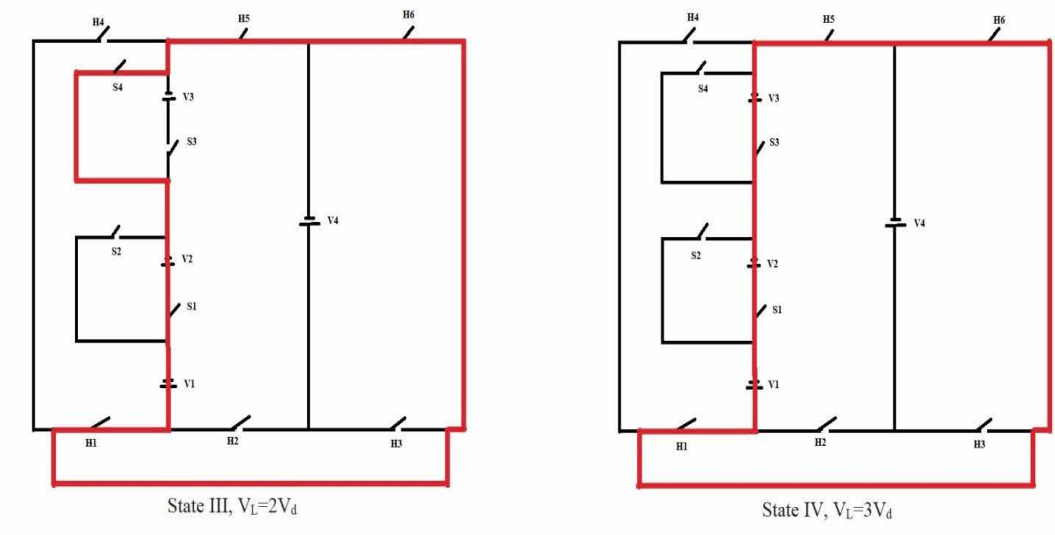
State I, V_L=0



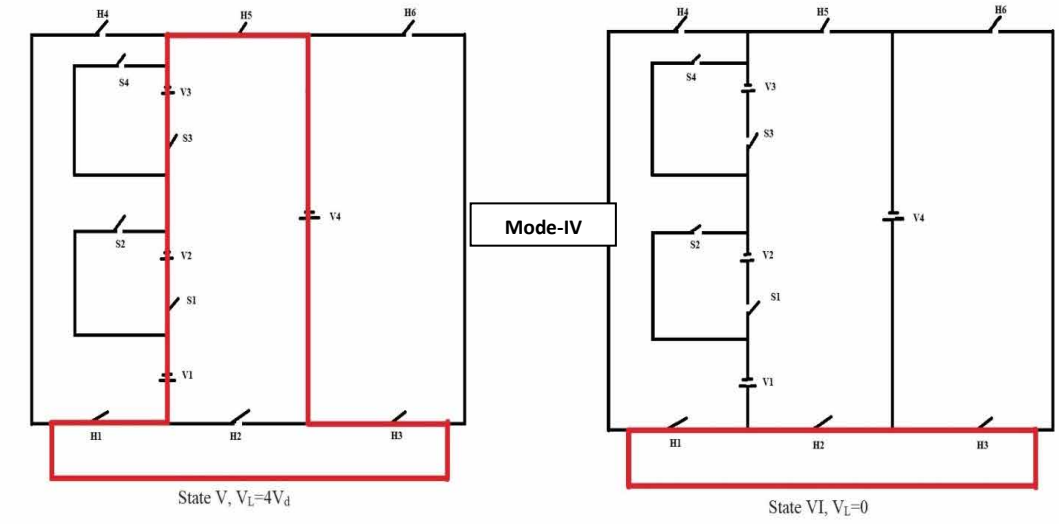
State II, V_L=V_d

- **State III.-** To achieve a voltage level (V_L= 'V_1 + V_2' =200V) on the connected load side, switches H_1, S_1, S_4, H_5 and H_6 are ON. In this state, total output voltage is 200V at Load.

- **State IV.: -** To achieve a voltage level (V_L= '+V_1+ V_2+ V_3' =300V) on the connected load side, switches H_1, S_1, S_3, H_5, and H_6 are ON. In this state, total output voltage is 300V at Load.

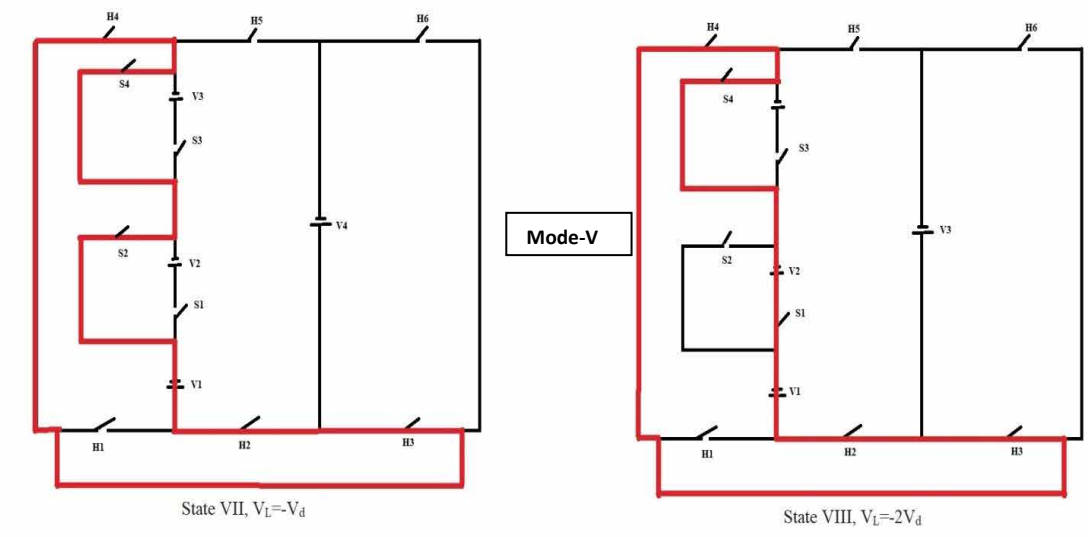


- **State V.-** To achieve a voltage level (V_L= 'V_1 + V_2 +V_3+V_4' =400) on the connected load side, switches H_1, S_1, S_3, H_5, and $H_3$are ON. In this state, total output voltage is 400V at Load.
- **State VI.: -** To achieve a voltage level (V_L= '0') on the connected load side, switches H_1, H_2 and H_3 are ON. In this state, total output voltage is 0V at Load.



- **State VII. -** To achieve a voltage level (V_L= '-V_1' =-100) on the connected load side, switches H_3, H_2, S_2, S_4, and H_4 are ON. In this state, total output voltage is -100V at Load.

- **State VIII.-** To achieve a voltage level (V_L= '-V_1-V_2 = -200') on the connected load side, switches H_3, H_2, S_1, S_4, and H_4 are ON. In this state, total output voltage is -200V at Load.



- **State IX. -** To achieve a voltage level (V_L= ''-V_1-V_2-V_3" =-300) on the connected load side, switches H_3, H_2, S_1, S_3, and H_4 are ON. In this state, total output voltage is -300V at Load.

- **State X.: -** To achieve a voltage level (V_L= '-V_1-V_2 -V_3-V_4 "= -400') on the connected load side, switches H_6, H_2, S_1 S_3, and H_4 are ON. In this state, total output voltage is -400V at Load.

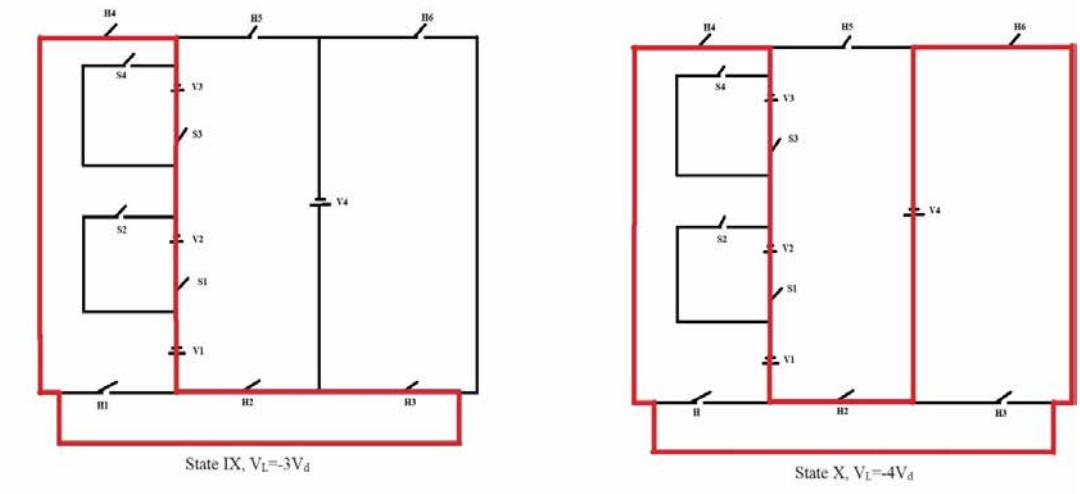


Figure 5.20: Multi-level Working Modes

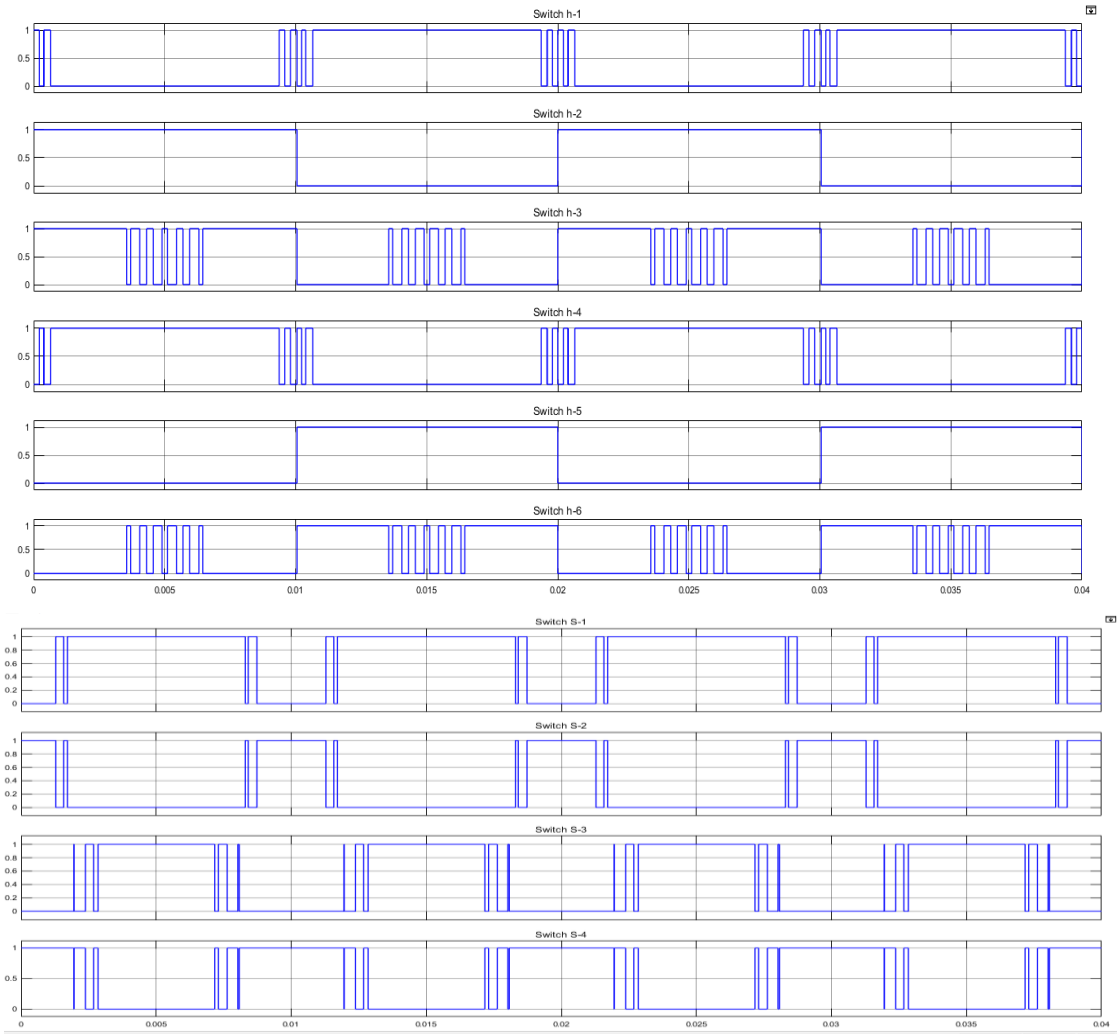


Figure 5.21: Gate switching pulses for the 9-level inverter

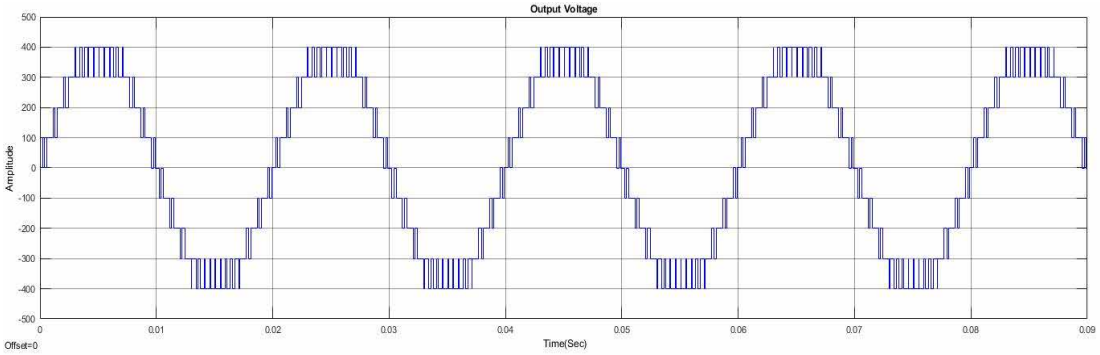


Figure 5.22: Simulation result of 9-level voltage output

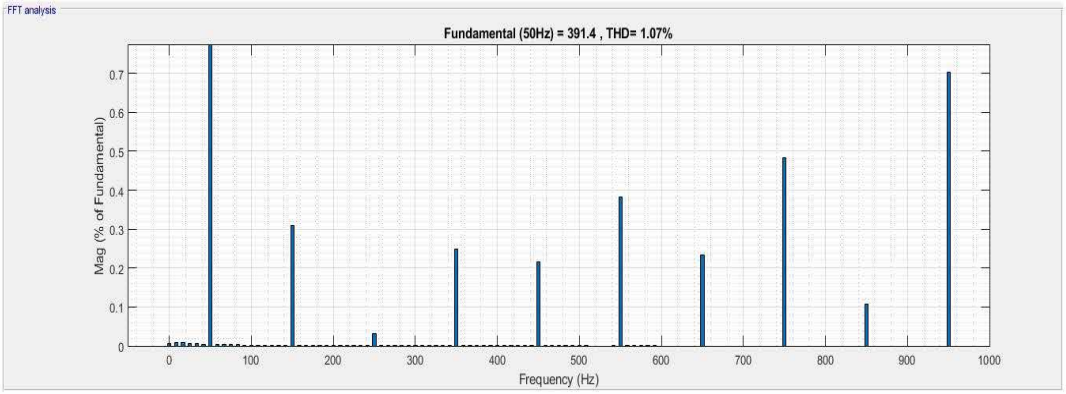


Figure 5.23: Output voltage's total harmonic distortion (THD)

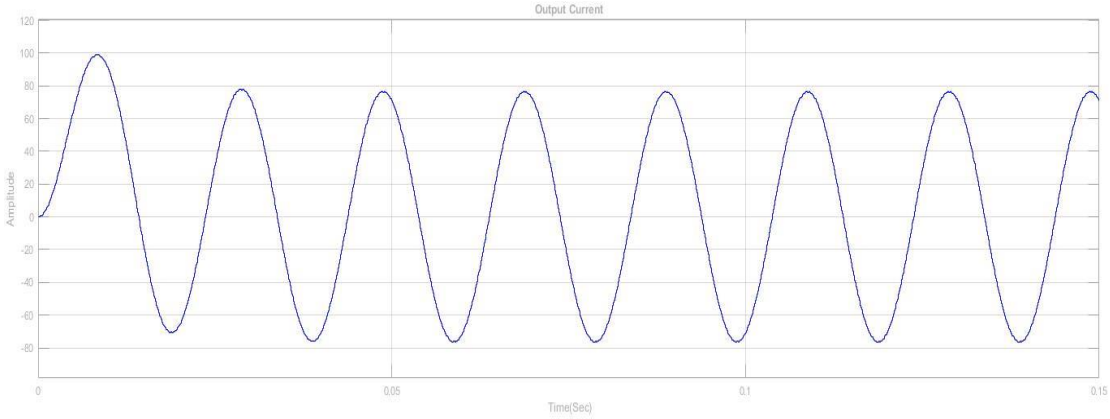


Figure 5.24: Simulating outcome of 9-level MLI current output

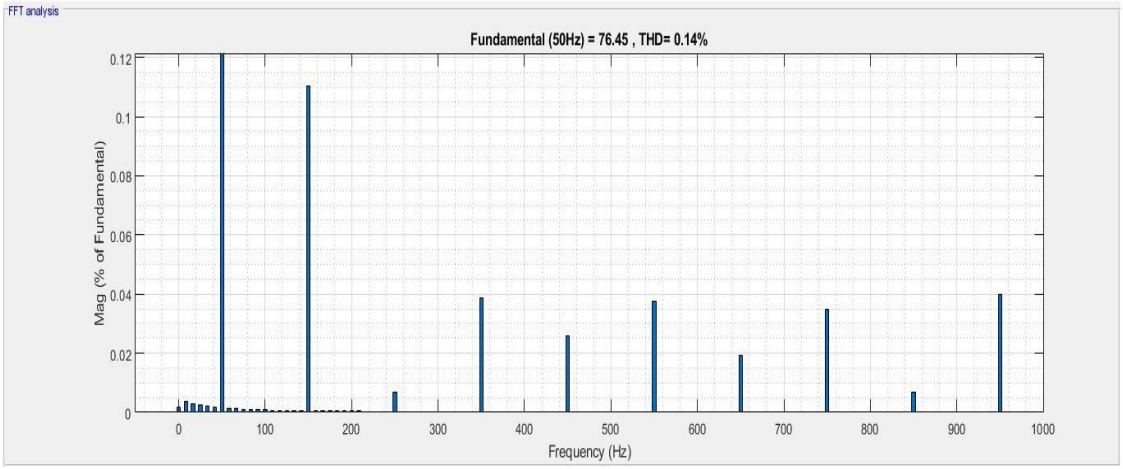


Figure 5.25: THD of output Current

Losses Calculation

The related loss of voltage source converters is equivalent to the sum of energy losses caused by individual semiconductors. Loss sustained by a semiconductor diode is often classified into 3 types:

1) Whenever the circuit is in a block condition (that is, OFF-mode);
2) Whenever the circuit is in a conduct condition (that is, ON-mode)

While the circuit switches (that is, the changing mode from ON mode to OFF mode or conversely). Because leakage currents have been almost non-existent during block conditions [8], the loss remains small. As a result, just conduct & switch loss were taken into account when calculating loss related to these inverters.

5.8.2 Conduction Loss

All switching needed in this architecture is unidirectional conduct & bidirectional block. The instant conduction loss of conventional transistors and diodes is.

$$\tau_c T(t) = [V_T + R_T i_\alpha(t)]\, i(t) \quad (8)$$

$$\tau_c D(t) = [V_D + R_D i(t)]\, i(t) \quad (9)$$

Here,

$\tau_c, T(t) \& \tau_c, D(t)$ = instant conduction loss of the transistors circuit & diodes, correspondingly

VT & VD=ON-mode voltage drops

RT & RD=equivalent ON-mode resistance of the transistors circuit & diodes, correspondingly

α = constant governed by transistors features.

The conductive switch must carry the load current $si_L(t)$at any specified period. Furthermore, based on output voltage level & $i_L(t)$ Direction, specific switch's transistors circuit or diodes operates. As illustrated in fig. 10, in modes 4, if the $i_L(t)$Is greater than zero, the transistors circuits of switching h3 & h2 current, whereas the

diodes of switching q1 flow. Whenever$i_L(t) = 0$, the transistors circuit of switching T1 current, together with the diode of switching T3 & T2. Letting $N_D(t)\&N_T(t)$ represent the number of current diode and transistor circuits, correspondingly, at every point in time. The averaged conduction loss may therefore be stated by following eqn. (9) and eqn. (10):

$$\tau_c, avg = \frac{1}{\pi}\int_0^{\pi} \quad [\{N_T(t)V_T + N_D(t)V_D)i_L(t) + \{N_T(t)R_T i_L^{\alpha+1}(t)\} + \{N_D(t)i_L^{\alpha 2}(t)\}]\, d(wt) \tag{10}$$

5.8.3 Switching Loss

To determine the overall switch loss, a standard switch is firstly analyzed, then separate power loss is therefore summed to give the overall switch loss of these inverters. For evaluating the isolated switch loss, current linear function & voltage linear function are utilized throughout the transient cycle (transit as OFF mode to ON mode & conversely) [21]. Power loss at start-up may be computed like

$$E_{on,j}=\int_0^{t_{on}} \quad V(t)i(t)dt \tag{11}$$

$$\int_0^{t_{on}} \quad \left[\left\{V_{o,j}\frac{t}{t_{on}}\right\}\left\{-\frac{I}{t_{on}}(t - t_{on})\right\}\right]dt \tag{12}$$

$$\frac{1}{6}V_{o,j}I\, t_{on} \tag{13}$$

Where,

$E_{on,j}$= j[th] switch loss of turn-ON

t_{on}=time for turn-ON

I = when switching upon that switch; electric current flows through all of it

$V_{o,j}$= voltage that must be blocked by the jth switch

Likewise, the j[th] switch's energy dissipation when turned off may be computed as

$$\int_0^{toff} \quad v(t)i(t) = \int_0^{toff} \quad \left[\left\{V_{o,j}\frac{t}{t_{off}}\right\}\left\{-\frac{I}{t_{off}}(t - t_{off})\right\}\right] \tag{14}$$

$$=\left(\frac{1}{N}\right)V_{o,j}*I* t_{off} \tag{15}$$

Where t_{off} the time it takes for the jth is switches to turn it off, and I indicate the current that flows using switches before this turns off?

The jth switch performs fj changes in 1 s, wherein fj would be its carrier frequency. As a result, given I = I, total switch power loss may be estimated as:

$$\tau_s = \sum_{j=1}^{2n+2} \quad [\frac{1}{10} V_{o,j} I\left(t_{on} + t_{off}\right) f_j] \qquad (16)$$

The next Section V (14) can be used to demonstrate that such a topology has reduced switch loss than the traditional CHB design. The overall inverter loss may now be calculated by eqn. (11) and eqn. (14) as functions.

$$\rho_{losses} = \rho_{c,avg} + \rho_s \qquad (17)$$

Component Requirements and its comparison

In this section, the presented topology has been compared in the manner of component requirement with the existing traditional topology such as NPC, CHB, and FC-MLI; As per above discussion, seen that proposed multi-level inverter is the family of CHB multilevel inverter, proposed converter has four symmetrical input dc voltage, 10 IGBT switches producing stepped output with 1.07% THD without any type filter, in this category circuit has lowest THD profile with lower component count moreover level can be further increased by increasing number of cell or using asymmetrical DC voltage source. Table 5.6 shows comparison of component needs for this proposed topology concerning number of DC input sources for a single-phase 9-level arrangement. The table indicated that number of components throughout this architecture is lower than that of other architecture, specifically for a greater level of voltage. Furthermore, the overall voltage load carried by the primary switches and diodes throughout this design is almost the same as conventional topologies.

Table 5.6: Component Require For 1-Phases multilevel inverters (L_n is Levels Number in the Phase Voltage)

type of Inverters	NPC	FC	Cascaded H-bridge	Used Symmetrical DC voltage Topology
Number of main Switch	$6(L_n\text{-}1)$	$6(L_n\text{-}1)$	$6(L_n\text{-}1)$	(L_n+1)
Number of main diodes	$6(L_n\text{-}1)$	$6(L_n\text{-}1)$	$6(L_n\text{-}1)$	(L_n+1)
Number of (DC) diode clamping	$3(L_n\text{-}1)$ $(Ln\text{-}2)$	0	0	0
Isolated Supply	$(L_n\text{-}1)$	$(L_n\text{-}1)$	$3(L_n\text{-}1)/2$	$(L_n\text{-}1)/2$
Number of FC (flying capacitor)	0	$(3/2)$ $(Ln\text{-}1)$ $(Ln\text{-}2)$	0	0
Aggregate Components count	$(L_n\text{-}1)$ $(3L_n+7)$	$(1/2)$ $(Ln\text{-}1)$ $(3L_n+20)$	$(27/2)$ $(L_n\text{-}1)$	$(2*L_n+2)$

Listed table 5.7 shows the comparative analysis of THD with some existing topologies, which clearly shows that the 10-component based semi cascaded MLI has the lowest total harmonics distortion, comparative analysis has cleared its best performance.

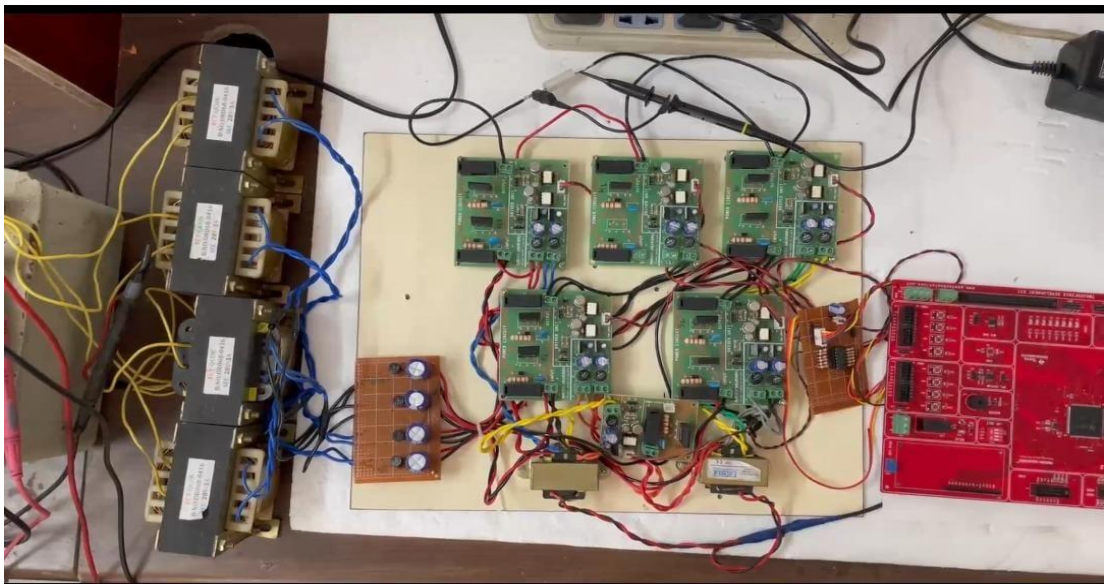
Table.5.7. Comparative Analysis of THD with some Existing Topologies

S. No.	Topology	Output Voltage Levels	Amplitude Modulation index	THD-Sinusoidal PWM (%)
1	Existing Topology [215]	15	1	8.01
		13	0.85	9.64
		11	0.7	11.82
		9	0.55	15.29
2	Cascaded MLI [216]	15	1	8.18
		9	1	10.13
		7	1	11.86
3	Symmetric HT-type MLI [214]	11	0.663	5.02
4	Presented Semi Cross Switched MLI Topology	7	1	17.13
5	**Presented Semi-Cascaded MLI**	**9**	**1**	**1.07**

CHAPTER- 6

HARDWARE IMPLEMENTATION AND EXPERIMENTAL INVESTIGATIONS

To execute research topology, design of single phase 9 level inverter is being created prototype model with same logic as utilised in MATLAB simulation, as Figure 13 (a) demonstrates experimental setup, and Figure 13 (b) shows a picture of the output waveform, in which MOSFETs (IRF460) are employed as power electronic switches. They are being driven by the appropriate gate drivers; four input dc sources as voltages $E_1 = E_2 = E_3 = E_4 = 40$ V are used. An inductor load with R = 2 ohm & L = 2 mH is applied to inverters. We utilize carrier signals and reference signals that have frequencies of 2.2 kilohertz and 50 Hertz, respectively. A TMS320F2812 Development kit is utilised to implement control scheme. The voltage waveforms & associated THD seem to be in close accord with the findings of the corresponding simulations. The load voltage is a stepping waveform with levels of equal magnitude. It's also very important to note that power balance amongst input dc supplies is required with all dc sources to be having equivalent lifespan. So, when DC sources, like PV cells, are used, power rebalancing is especially critical.



(a)

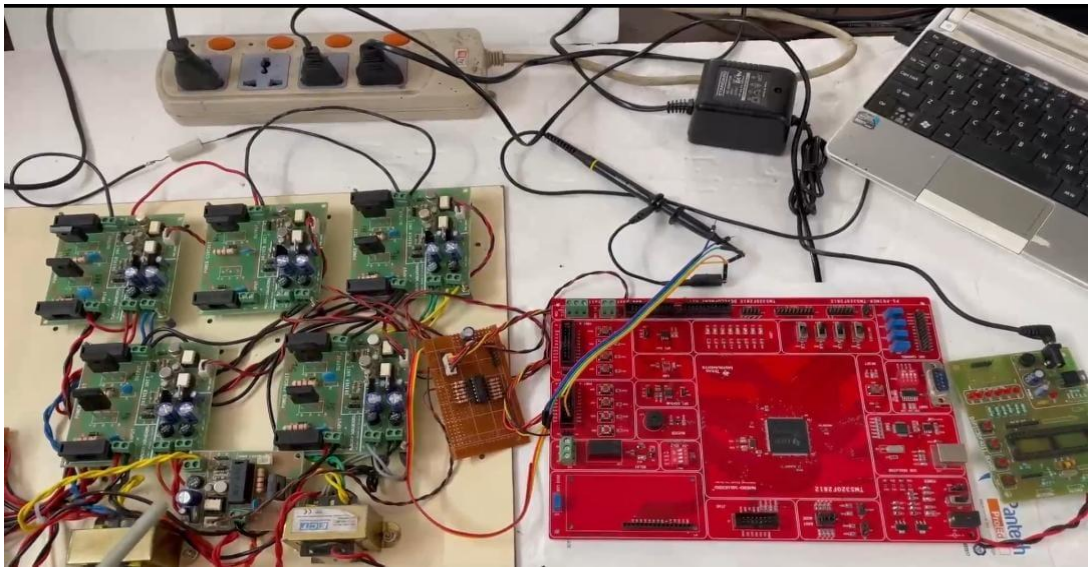


Figure 6.1: Experimental setup

Components required: -

1. DSP 2812 controller
2. Auto transformer
3. 4 power supplies
4. Two transformers for supply to driver circuit
5. 10 Mosfet
6. Not gate IC 7404
7. Matlab
8. CRO

Theory

DSP 2812 controller

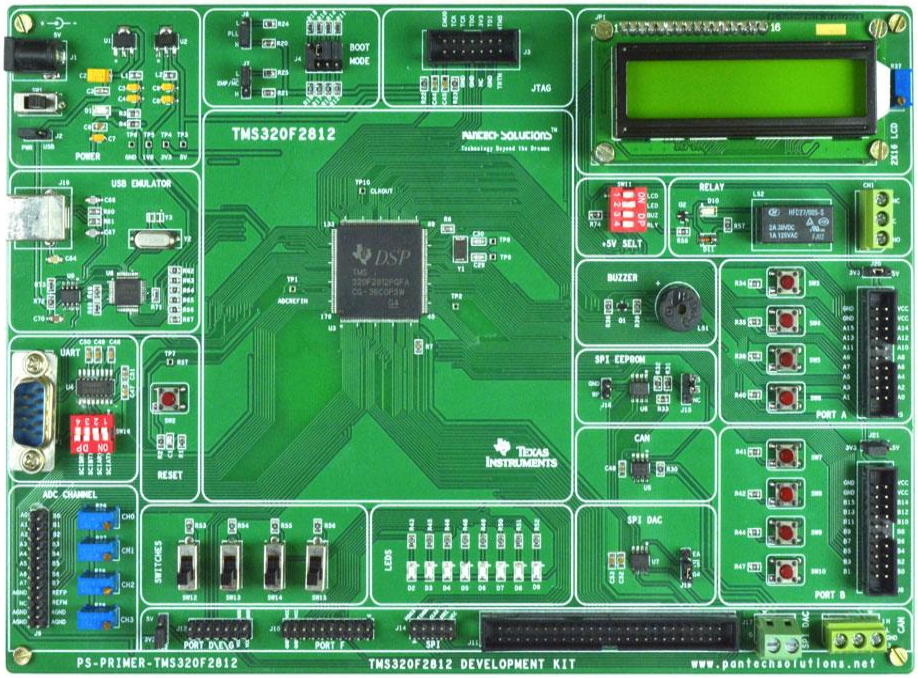


Figure 6.2: TMS320F2812 Development kit

Power Supply

The external power can be DC, with a voltage 5V/1A output at 230V AC input. The TMS320F2812 board produces 3.3V using an ADP3339 voltage regulator. This Voltage provides supply to the Controller & related peripherals. LM1117 voltage regulator will produce the 1.8V and used for core voltage of Digital Signal Controller. Here, USB is meant for power supply as well as XDS100 USB V1 Emulator. Separate power source selects Jumper available.

Test point Details

The following test points are used to check or test the boards,

1. TP1 – ADCREFIN
2. TP2 – READ/WRITE
3. TP3 – 5V
4. TP4 – 3.3V
5. TP5 – 1.8V
6. TP6 – GROUND
7. TP7 – RESET

8. TP8 – XCLK IN
9. TP9 – XCLC OUT
10. TP10 – CLKOUT

6.1 TMS320F2812

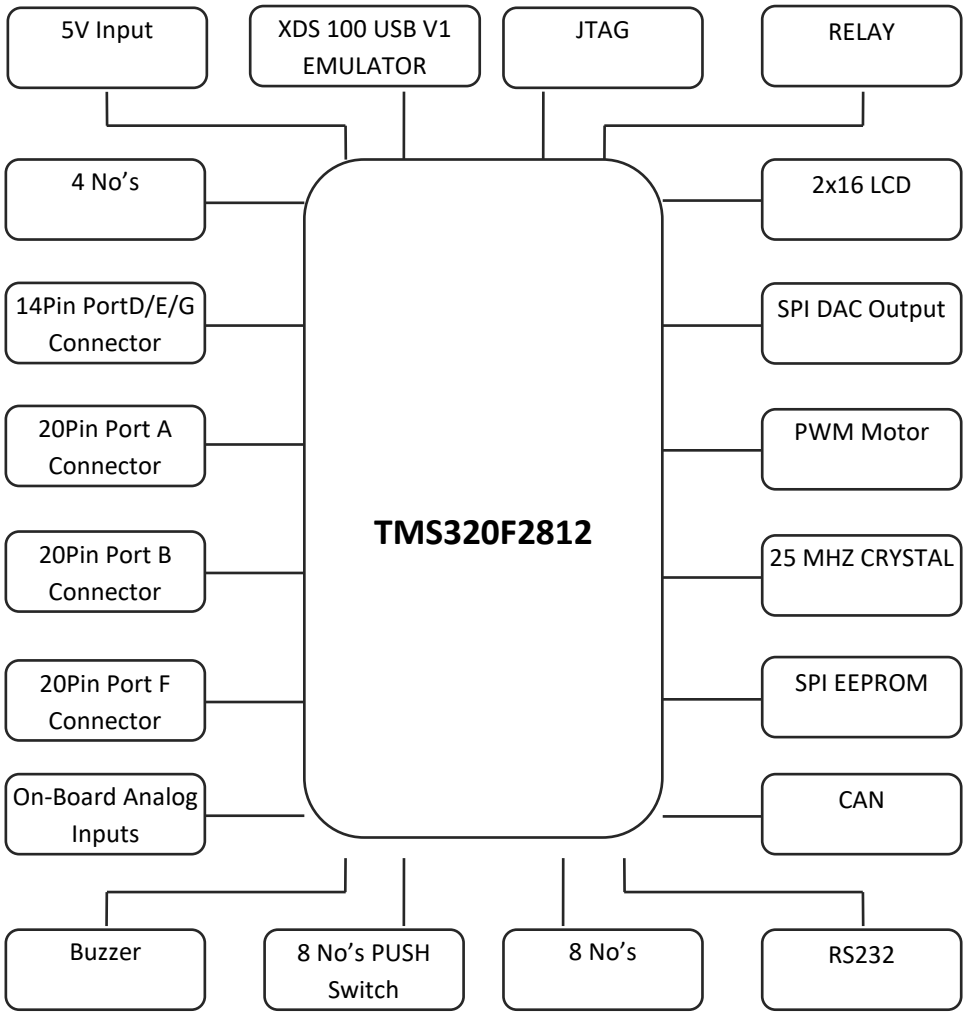


Figure 6.3: General Block Diagram

6.2 Features of TMS320F2812 DSP Development Board

- Motor Control Peripherals.
- 12-Bit ADC, 16 Channels.
- On board RS-232 connector with line driver.
- SCIA or SCIB can configure single UART.
- 8 Digital LED Output.

- 8 Digital Inputs (Push Switch).
- 4 Digital Inputs (Slide Switch).
- 4 Analog Inputs (Trimpot).
- 16×2 Numeric LCD.
- 1 Buzzer.
- 1 Relay.
- 12-bit SPI DAC.
- 4K SPI EEPROM.
- CAN interface.
- Multiple Booting Option Connectors.

6.3 Benefits of TMS320F2812 DSP Development Board

- Advanced Motor Control.
- Solar Power Systems.
- Servo drives and Motion control.
- Renewable Energy and Uninterrupted Power Supplies.

General Procedure to Work F2812

1. Open MATLAB
    - Go to Model file.
    - Open Simulink block for the project
2. Simulink library browser
    - Open embedded coder support package for 281X (we can find digital output block).
3. DSP system toolbox HDL support
    - Sources – sine wave
4. Set configuration parameters.
    - Open hardware implementation
    - Select board as TIF281X.
    - In target hardware resources, choose boot from flash and set clocking parameters.
5. To generate the code, click build model.

- View diagnostics.
- Finally, .out file for CCS is created.

6. Open code composer studio 5.5.0 software
   - Select workspace location.
7. Open device manager
8. Connect TMS320F2812 starter kit with PC.
   - Check system devices.
   - Check TIXDS100 channel A, channel B.
   - Now it is ready to program.
9. In CCS, select view.
   - Target configuration
10. Basic→General step→ select emulator.
    - TIXDS100V1 USB emulator →TMS320F2812
    - Click save.
11. Right click →launch →select configuration.
    - Click connect target→ load program →open .out file →ok.
12. Click resume RF8 →click terminate.
13. Connections:
    - Connect the USB cable, PC to KIT.
    - Connect the 5V adapter and Power on the kit.

Procedure: -

This is a nine-level inverter using SPWM technique. We have auto transformer and 4 isolation step-down transformers. There is a bridge rectifier with a filter circuit, 4 power supplies, and we have an inverter circuit forming 9 levels. The two transformers are going to supply the driver circuit. In each of the inverters, each mosfet is having individual driver circuit inbuilt. We have a not gate IC 7404, which is used to generate PULSE FROM THE 2812 CONTROLLER. 2812 is going to generate pulse from Matlab. It will generate 6 pulses, after that, we have not agte IC, which we get 4 pulses. So, we have used 10 mosfets or 10n power devices. So 10 pulses we are going to apply to inverter circuit, and We are going to see the results

1. First, we switch on the driver circuit

2. Switch on 2812 controller
3. Switch on driver unit
4. Switch on auto transformer
5. We will apply auto transformer input gradually
6. Give the input voltage to see corresponding waveform

Results: -

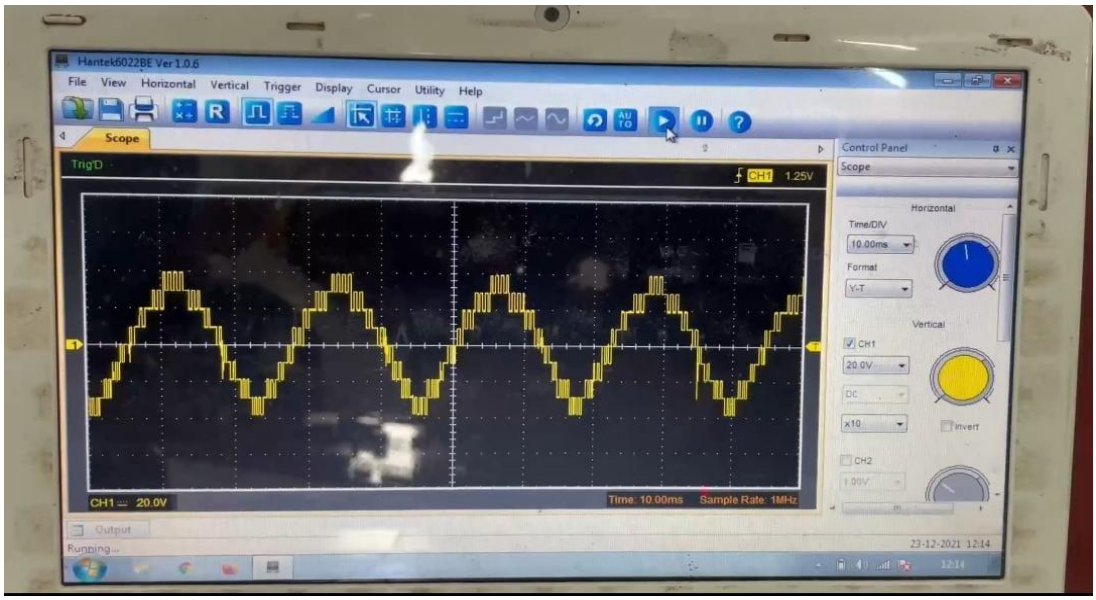


Figure 6.4: Result

The input to the DC bus was 230/24 V transformer, which by passed through a diode bridge rectifier to give an input of 40 V. The output voltage waveform is as obtained above with voltage levels of 0V, 40V, 80V, 120V, 160V, -40V, -80V, -120V, -160V. The advantages of modularity, lower switching stress, switching losses and THD has been achieved using the above topology.

CHAPTER- 7

CONCLUSIONS

Power electronic converters are sought after as a means of improving energy efficiency. Multi-level inverter converters are capable of providing such capability. Like any other new technology, it has its own set of obstacles. To better understand the design and implementation concerns of multilevel inverters and to suggest feasible solutions to those issues, this research is being done.

The additional costs that multilevel inverters entail are usually taken into account when deciding whether or not to put them into commercial use. In most circumstances, economic concerns take precedence over any other issues that may be taken into account. When the increased cost cannot be justified by the enhanced functionality provided by multilayer inverters with high performance and high efficiency, it comes as no surprise that they are not considered. By minimizing the amount of components required as the quantity of layers upsurges, increased cost of this project is kept to a minimum. The innovative multilayer inverter architecture explored in this paper is responsible for this.

Three components make up the multilevel inverter structure. A full-bridge circuit with eight switches is used in Module 1, whereas a seven-switch circuit is used in Module 2. 10 switches are linked to DC sources in Module 3. There is only 1 additional bidirectional switch needed in Module 3 when upgrading inverter's structure from one level to another, regardless of how many layers there are in the inverter's structure. Module 3's switches work in an optimized manner that divides switch operation into three phases, which is a significant feature of the topology. That is, rather than being devoted only to one phase, the bidirectional switches are shared by all three.

For this research, the seven-level and nine-level designs of inverters are examined in depth. The suggested topology necessitates the development of a new sine-PWM method. Virtual vectors are added to substitute voltage vectors that were deleted as consequence of switch-sharing strategy used in Module 3 because of this. Dependent

on whether or not the matching determined triangular zone has virtual sides or not. The on-state times may also be determined using a novel approach.

7.1 Author's Contributions

Work done may be seen from three separate perspectives: multilayer inverter topologies and modulation methods. The following is a summary of each of them:

1. Using the capabilities of power-switching devices to create three phases, the suggested multi-level inverter architecture is a new design. The total number of parts used may be drastically decreased in this way. According to the proposed topology, just 10 components are needed compared to diode-clamped structure, flying capacitor structure, & a CHB structure that needs 89, 70, and 60 components, respectively. This means lower costs, more dependability, and reduced complexity for implementation. It's also possible to get the same performance out of the recommended topology in certain cases. The suggested topology, for example, beats the diode-clamped topology in terms of efficiency.
2. A new Sine-PWM technique has been created with the purpose of designing pulse width. This method provides the solution of low THD; in this phenomenon, we will be able to find a Low THD profile for this; we selected one reference voltage as the sine wave with 50Hz frequency and the remaining carrier wave as triangular pulses; these comported waves produce IGBT firing pulses.

7.2 Recommendations for Further Work

Although the research goals have been met, there are still several difficulties that need additional exploration. The suggested multi-level inverter has one drawback. Each switch in Module 1 must tolerate the same amount of voltage stress as the entire DC input voltage. This means that if Module 1's voltage rating changes, so does Module 1's inverter's voltage rating. The current switches in the inverter are only rated for a few kilovolts; hence they can not be utilized for medium or high-power applications. There's no assurance that voltage stress on switches in Module 1 will be evenly distributed if each switch is replaced by a series connection of many switches. The unequal features of solid-state switches are caused by the fact that they are produced

from crystals. There must be accurate values of resistive, capacitive, and inductive components in the auxiliary circuits to guarantee that the series-connected switches are equally stressed during both transient & steady-state operations. Inappropriately, due to high cost of R&D, most industrial players have given up on developing the necessary skills to design these circuits. Consequently, a variety of ways may be used to further emphasize Module 1 by altering the structure or the like.

Since it cannot be utilized for medium or high-power applications because of its defect, suggested multilayer inverter isn't as unlikely to be used in low-power ones. The suggested multilayer inverter may offer advantage over two-level inverter in certain situations, despite severe competition. A growing interest in microgrids and the need to enhance efficiency may make it easier to use a device like this inverter. This inverter might also be utilised to boost output power of small-capacity PV generating systems by overcoming the partial shading problem. The aviation industry's strict standards for reducing the weight of the components fitted in new aircraft are another consideration. It's possible that massive filters utilised with 2-level inverters in hydraulic pumps, compressors, & electronic brakes aren't up to snuff when it comes to modern aircraft's transition to electric propulsion. This might open the door to a broader range of uses for the inverter under consideration.

The suggested multilayer inverter may be beneficial in certain low-power applications; thus, further work may be done to resolve a few concerns that demand better solutions. To put the closed-loop system into action,

Batteries are employed as DC sources in this project. A power supply & voltage divider capacitor may also be utilised in place of batteries. For the suggested architecture, more research may be done to observe problem of capacitor voltage balancing. In addition, the suggested topology may be used for low-powered REGS, like PV applications, as well. It has also not been investigated in this study how the PI controller with the automated tuning module performs under fluctuating DC source circumstances. The tuning algorithm requires some tweaking, and this merits more examination. SHE or other carrier-based modulation approaches may also be researched for the multilayer inverter under consideration. AI-based approaches like

neural networks and genetic algorithms may also be included in the tuning procedure. Fuzzy logic controllers, hysteresis controls, predictive controls, and emotional controls may be researched to replace the adaptive PI controller. These controllers may also include emotional controls.

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APPENDICES

voltage across every capacitor equal	Vdc/2 (Vdc1 = Vdc2 = Vdc/2)
Turn on the switches S_1 and S_2	V_{an} $V_{dc/2}$
3 output voltages	+Vdc, 0Vdc, and -Vdc
Voltage waveforms of DC	V_{DC}
q & d-axis voltage commands are linked to a-b-c	$V_q = V_a - V_b - V_c$
Large Operator	$\sum_{i=1}^{n-1}$
modulation ratio	m_f
switching pattern: 2 triangles & modulation signals	S_{1ap}, S_{2ap}, S_{1an}, S_{2an}.
Beta	β
Alpha	α

LIST OF PUBLICATIONS

S. No	Type of Paper (Journal Paper/Conference proceeding/Book Chapter)	Name of the Journal/Conference/Book	Journal indexing (Scopus/UGC/Web of Science)	Title of the Paper
1	Conference paper	4th International e-conference on intelligent circuits and systems (ICICS-2022)	Scopus	Comprehensive Survey on topology of Multilevel inverter (MLI)
2	Conference paper	2022 2nd International conference on Intelligent Technologies (CONIT)	Scopus	A Circuit analysis on Multilevel inverter using multistring topology for minimize THD profile
3	Journal Paper	Energy Engineering, Tech Science Press	Scopus	Design and Analysis of Cascaded Hybrid-Bridge Multi-Cell Multilevel Inverter with Reduced Total Harmonic Distortion Profile

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1	Conference paper	4th International e-conference on intelligent circuits and systems (ICICS-2022)	Scopus	Comprehensive Survey on topology of Multilevel inverter (MLI)
2	Conference paper	2022 2nd International conference on Intelligent Technologies (CONIT)	Scopus	A Circuit analysis on Multilevel inverter using multistring topology for minimize THD profile